

PLUMMER

SILICON
VLSI
TECHNOLOGY

TK

7874

.75

P58

2000

FN01

Silicon VLSI Technology

Fundamentals, Practice and Modeling

James D. Plummer

Michael Deal

Peter B. Griffin

*Department of Electrical Engineering
Stanford University*



Prentice Hall

Upper Saddle River, NJ 07458

Library of Congress Cataloging-in-Publication Data

Silicon VLSI technology

p. cm.

ISBN 0-13-085037-3

1. Integrated circuits—Very large scale integration—Design and construction. 2. Silicon. 3. Silicon oxide films. 4. Metal oxide semiconductors. 5. Silicon technology.

TK7874.75.S54 2000

621.39'5—dc21

99-42745

CIP

Publisher: Tom Robbins

Associate Editor: Alice Dworkin

Editorial/Production Supervision: Rose Kernan

Vice President and Editorial Director, ECS: Marcia Horton

Vice President of Production and Manufacturing: David W. Riccardi

Executive Managing Editor: Vince O'Brien

Marketing Manager: Danny Hoyt

Managing Editor: David A. George

Manufacturing Buyer: Pat Brown

Manufacturing Manager: Trudy Piscioti

Art Director: Jayne Conte

Cover Design: Bruce Kenselaar

Editorial Assistant: Jesse Power

Copy Editor: Martha Williams

Composition: D&G Limited, LLC

Prentice
Hall

©2000 by Prentice Hall, Inc.

Upper Saddle River, New Jersey 07458

All rights reserved. No part of this book may be reproduced, in any form or by any means, without permission in writing from the publisher.

The author and publisher of this book have used their best efforts in preparing this book. These efforts include the development, research, and testing of the theories and programs to determine their effectiveness. The author and publisher make no warranty of any kind, expressed or implied, with regard to these programs or the documentation contained in this book. The author and publisher shall not be liable in any event for incidental or consequential damages in connection with, or arising out of, the furnishing, performance, or use of these programs.

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

ISBN 0-13-085037-3

Prentice Hall International (UK) Limited, *London*

Prentice Hall of Australia Pty. Limited, *Sydney*

Prentice Hall Canada Inc., *Toronto*

Prentice Hall Hispanoamericana, S.A., *Mexico*

Prentice Hall of India Private Limited, *New Delhi*

Prentice Hall of Japan, Inc., *Tokyo*

Pearson Education Pte., Ltd., *Singapore*

Editora Prentice Hall do Brasil, Ltda., *Rio de Janeiro*

Contents

T K
7874
.75
P58
2000
ENGI

Preface.....	xi
--------------	----

Chapter 1 Introduction and Historical Perspective 1

1.1	Introduction.....	1
1.2	Integrated Circuits and the Planar Process—Key Inventions That Made It All Possible.....	7
1.3	Semiconductors.....	13
1.4	Semiconductor Devices.....	33
1.4.1	PN Diodes.....	33
1.4.2	MOS Transistors.....	36
1.4.3	Bipolar Junction Transistors.....	39
1.5	Semiconductor Technology Families.....	41
1.6	Modern Scientific Discovery—Experiments, Theory, and Computer Simulation.....	43
1.7	The Plan For This Book.....	45
1.8	Summary of Key Ideas.....	46
1.9	References.....	46
1.10	Problems.....	47

Chapter 2 Modern CMOS Technology 49

2.1	Introduction.....	49
2.2	CMOS Process Flow.....	50
2.2.1	The Beginning—Choosing a Substrate.....	51
2.2.2	Active Region Formation.....	52
2.2.3	Process Option for Device Isolation—Shallow Trench Isolation.....	57
2.2.4	N and P Well Formation.....	60
2.2.5	Process Options for Active Region and Well Formation.....	63
2.2.6	Gate Formation.....	71
2.2.7	Tip or Extension (LDD) Formation.....	76
2.2.8	Source/Drain Formation.....	80
2.2.9	Contact and Local Interconnect Formation.....	82
2.2.10	Multilevel Metal Formation.....	84
2.3	Summary of Key Ideas.....	90
2.4	Problems.....	91

Chapter 3	Crystal Growth, Wafer Fabrication and Basic Properties of Silicon Wafers	93
3.1	Introduction	93
3.2	Historical Development and Basic Concepts	93
3.2.1	Crystal Structure	94
3.2.2	Defects in Crystals	97
3.2.3	Raw Materials and Purification	101
3.2.4	Czochralski and Float-Zone Crystal Growth Methods	102
3.2.5	Wafer Preparation and Specification	105
3.3	Manufacturing Methods and Equipment	109
3.4	Measurement Methods	111
3.4.1	Electrical Measurements	111
3.4.1.1	Hot Point Probe	112
3.4.1.2	Sheet Resistance	113
3.4.1.3	Hall Effect Measurements	115
3.4.2	Physical Measurements	117
3.4.2.1	Defect Etches	117
3.4.2.2	Fourier Transform Infrared Spectroscopy (FTIR)	118
3.4.2.3	Electron Microscopy	119
3.5	Models and Simulation	121
3.5.1	Czochralski Crystal Growth	122
3.5.2	Dopant Incorporation during CZ Crystal Growth	125
3.5.3	Zone Refining and FZ Growth	128
3.5.4	Point Defects	131
3.5.5	Oxygen in Silicon	138
3.5.6	Carbon in Silicon	142
3.5.7	Simulation	143
3.6	Limits and Future Trends in Technologies and Models	144
3.7	Summary of Key Ideas	146
3.8	References	147
3.9	Problems	148
Chapter 4	Semiconductor Manufacturing—Clean Rooms, Wafer Cleaning, and Gettering	151
4.1	Introduction	151
4.2	Historical Development and Basic Concepts	154
4.2.1	Level 1 Contamination Reduction: Clean Factories	157
4.2.2	Level 2 Contamination Reduction: Wafer Cleaning	159
4.2.3	Level 3 Contamination Reduction: Gettering	161
4.3	Manufacturing Methods and Equipment	165
4.3.1	Level 1 Contamination Reduction: Clean Factories	165
4.3.2	Level 2 Contamination Reduction: Wafer Cleaning	166
4.3.3	Level 3 Contamination Reduction: Gettering	167
4.4	Measurement Methods	169
4.4.1	Level 1 Contamination Reduction: Clean Factories	169

4.4.2	Level 2 Contamination Reduction: Wafer Cleaning.	173
4.4.3	Level 3 Contamination Reduction: Gettering.	176
4.5	Models and Simulation.	180
4.5.1	Level 1 Contamination Reduction: Clean Factories.	181
4.5.2	Level 2 Contamination Reduction: Wafer Cleaning.	184
4.5.3	Level 3 Contamination Reduction: Gettering.	186
4.5.3.1	Step 1: Making the Metal Atoms Mobile	186
4.5.3.2	Step 2: Metal Diffusion to the Gettering Site.	187
4.5.3.3	Step 3: Trapping the Metal Atoms at the Gettering Site.	190
4.6	Limits and Future Trends in Technologies and Models	193
4.7	Summary of Key Ideas	196
4.7	References	196
4.9	Problems	198

Chapter 5 Lithography 201

5.1	Introduction.	201
5.2	Historical Development and Basic Concepts	203
5.2.1	Light Sources.	206
5.2.2	Wafer Exposure Systems	208
5.2.2.1	Optics Basics—Ray Tracing and Diffraction	209
5.2.2.2	Projection Systems (Fraunhofer Diffraction).	212
5.2.2.3	Contact and Proximity Systems (Fresnel Diffraction)	219
5.2.3	Photoresists	221
5.2.3.1	g-line and i-line Resists	223
5.2.3.2	Deep Ultraviolet (DUV) Resists.	225
5.2.3.3	Basic Properties and Characterization of Resists	227
5.2.4	Mask Engineering—Optical Proximity Correction and Phase Shifting.	230
5.3	Manufacturing Methods and Equipment.	234
5.3.1	Wafer Exposure Systems	234
5.3.2	Photoresists	238
5.4	Measurement Methods.	241
5.4.1	Measurement of Mask Features and Defects	242
5.4.2	Measurement of Resist Patterns.	244
5.4.3	Measurement of Etched Features.	244
5.5	Models and Simulation.	246
5.5.1	Wafer Exposure Systems	247
5.5.2	Optical Intensity Pattern in the Photoresist	253
5.5.3	Photoresist Exposure	259
5.5.3.1	g-line and i-line DNQ Resists.	259
5.5.3.2	DUV Resists.	263
5.5.4	Postexposure Bake (PEB).	264
5.5.4.1	g-line and i-line DNQ Resists.	264
5.5.4.2	DUV Resists.	266
5.5.5	Photoresist Developing	267
5.5.6	Photoresist Postbake	270

5.5.7	Advanced Mask Engineering	271
5.6	Limits and Future Trends in Technologies and Models	272
5.6.1	Electron Beam Lithography	273
5.6.2	X-ray Lithography	275
5.6.3	Advanced Mask Engineering	277
5.6.4	New Resists	278
5.7	Summary of Key Ideas	281
5.8	References	281
5.9	Problems	283

Chapter 6 Thermal Oxidation and the Si/SiO₂ Interface 287

6.1	Introduction	287
6.2	Historical Development and Basic Concepts	290
6.3	Manufacturing Methods and Equipment	296
6.4	Measurement Methods	298
6.4.1	Physical Measurements	299
6.4.2	Optical Measurements	299
6.4.3	Electrical Measurements—The MOS Capacitor	301
6.5	Models and Simulation	312
6.5.1	First-Order Planar Growth Kinetic —The Linear Parabolic Model	313
6.5.2	Other Models for Planar Oxidation Kinetics	322
6.5.3	Thin Oxide SiO ₂ Growth Kinetics	326
6.5.4	Dependence of Growth Kinetics on Pressure	328
6.5.5	Dependence of Growth Kinetics on Crystal Orientation	329
6.5.6	Mixed Ambient Growth Kinetics	332
6.5.7	2D SiO ₂ Growth Kinetics	333
6.5.8	Advanced Point Defect Based Models for Oxidation	339
6.5.9	Substrate Doping Effects	343
6.5.10	Polysilicon Oxidation	345
6.5.11	Si ₃ N ₄ Growth and Oxidation Kinetics	347
6.5.12	Silicide Oxidation	350
6.5.13	Si/SiO ₂ Interface Charges	352
6.5.14	Complete Oxidation Module Simulation	357
6.6	Limits and Future Trends in Technologies and Models	359
6.7	Summary of Key Ideas	361
6.8	References	361
6.9	Problems	364

Chapter 7 Dopant Diffusion 371

7.1	Introduction	371
7.2	Historical Development and Basic Concepts	374
7.2.1	Dopant Solid Solubility	375
7.2.2	Diffusion from a Macroscopic Viewpoint	377
7.2.3	Analytic Solutions of the Diffusion Equation	379
7.2.4	Gaussian Solution in an Infinite Medium	380

7.2.5	Gaussian Solution Near a Surface	381
7.2.6	Error-Function Solution in an Infinite Medium	382
7.2.7	Error-Function Solution Near a Surface	384
7.2.8	Intrinsic Diffusion Coefficients of Dopants in Silicon	386
7.2.9	Effect of Successive Diffusion Steps	388
7.2.10	Design and Evaluation of Diffused Layers	389
7.2.11	Summary of Basic Diffusion Concepts	392
7.3	Manufacturing Methods and Equipment	392
7.4	Measurement Methods	395
7.4.1	SIMS	396
7.4.2	Spreading Resistance	397
7.4.3	Sheet Resistance	398
7.4.4	Capacitance Voltage	399
7.4.5	TEM Cross Section	399
7.4.6	2D Electrical Measurements Using Scanning Probe Microscopy	400
7.4.7	Inverse Electrical Measurements	402
7.5	Models and Simulation	403
7.5.1	Numerical Solutions of the Diffusion Equation	403
7.5.2	Modifications to Fick's Laws to Account for Electric Field Effects	406
7.5.3	Modifications to Fick's Laws to Account for Concentration-Dependent Diffusion	409
7.5.4	Segregation	413
7.5.5	Interfacial Dopant Pileup	415
7.5.6	Summary of the Macroscopic Diffusion Approach	417
7.5.7	The Physical Basis for Diffusion at an Atomic Scale	417
7.5.8	Oxidation-Enhanced or -Retarded Diffusion	419
7.5.9	Dopant Diffusion Occurs by Both I and V	422
7.5.10	Activation Energy for Self-Diffusion and Dopant Diffusion	426
7.5.11	Dopant-Defect Interactions	426
7.5.12	Chemical Equilibrium Formulation for Dopant-Defect Interactions	432
7.5.13	Simplified Expression for Modeling	434
7.5.14	Charge State Effects	436
7.6	Limits and Future Trends in Technologies and Models	439
7.6.1	Doping Methods	440
7.6.2	Advanced Dopant Profile Modeling—Fully Kinetic Description of Dopant-Defect Interactions	440
7.7	Summary of Key Ideas	442
7.8	References	443
7.9	Problems	445

Chapter 8 Ion Implantation 451

8.1	Introduction	451
8.2	Historical Development and Basic Concepts	451
8.2.1	Implants in Real Silicon—The Role of the Crystal Structure	461
8.3	Manufacturing Methods and Equipment	463

8.3.1	High-Energy Implants	466
8.3.2	Ultralow Energy Implants	468
8.3.3	Ion Beam Heating	469
8.4	Measurement Methods	469
8.5	Models and Simulations	470
8.5.1	Nuclear Stopping	471
8.5.2	Nonlocal Electronic Stopping	473
8.5.3	Local Electronic Stopping	474
8.5.4	Total Stopping Powers	475
8.5.5	Damage Production	476
8.5.6	Damage Annealing	479
8.5.7	Solid-Phase Epitaxy	482
8.5.8	Dopant Activation	484
8.5.9	Transient-Enhanced Diffusion	486
8.5.10	Atomic-Level Understanding of TED	488
8.5.11	Effects on Devices	497
8.6	Limits and Future Trends in Technologies and Models	499
8.7	Summary of Key Ideas	500
8.8	References	500
8.9	Problems	502

Chapter 9

Thin Film Deposition		509
9.1	Introduction	509
9.2	Historical Development and Basic Concepts	511
9.2.1	Chemical Vapor Deposition (CVD)	512
9.2.1.1	Atmospheric Pressure Chemical Vapor Deposition (APCVD) .	513
9.2.1.2	Low-Pressure Chemical Vapor Deposition (LPCVD)	525
9.2.1.3	Plasma-Enhanced Chemical Vapor Deposition (PECVD)	527
9.2.1.4	High-Density Plasma Chemical Vapor Deposition (HDPCVD)	530
9.2.2	Physical Vapor Deposition (PVD)	530
9.2.2.1	Evaporation	531
9.2.2.2	Sputter Deposition	539
9.3	Manufacturing Methods	554
9.3.1	Epitaxial Silicon Deposition	556
9.3.2	Polycrystalline Silicon Deposition	558
9.3.3	Silicon Nitride Deposition	561
9.3.4	Silicon Dioxide Deposition	563
9.3.5	Al Deposition	565
9.3.6	Ti and Ti-W Deposition	566
9.3.7	W Deposition	567
9.3.8	TiSi ₂ and WSi ₂ Deposition	567
9.3.9	TiN Deposition	568
9.3.10	Cu Deposition	570
9.4	Measurement Methods	572

9.5	Models and Simulation.....	573
9.5.1	Models for Deposition Simulations	573
9.5.1.1	Models in Physically Based Simulators Such as SPEEDIE	574
9.5.1.2	Models for Different Types of Deposition Systems.....	582
9.5.1.3	Comparing CVD and PVD and Typical Parameter Values	587
9.5.2	Simulations of Deposition Using a Physically Based Simulator, SPEEDIE	590
9.5.3	Other Deposition Simulations	598
9.6	Limits and Future Trends in Technologies and Models	601
9.7	Summary of Key Ideas	602
9.8	References	603
9.9	Problems	605

Chapter 10 Etching 609

10.1	Introduction.....	609
10.2	Historical Development and Basic Concepts	612
10.2.1	Wet Etching.....	612
10.2.2	Plasma Etching	619
10.2.2.1	Plasma Etching Mechanisms	621
10.2.2.2	Types of Plasma Etch Systems	628
10.2.2.3	Summary of Plasma Systems and Mechanisms	636
10.3	Manufacturing Methods.....	637
10.3.1	Plasma Etching Conditions and Issues	638
10.3.2	Plasma Etch Methods for Various Films	643
10.3.2.1	Plasma Etching Silicon Dioxide.....	644
10.3.2.2	Plasma Etching Polysilicon.....	647
10.3.2.3	Plasma Etching Aluminum.....	649
10.4	Measurement Methods.....	650
10.5	Models and Simulation.....	653
10.5.1	Models for Etching Simulation.....	653
10.5.2	Etching Models—Linear Etch Model	656
10.5.3	Etching Models—Saturation/Adsorption Model for Ion-Enhanced Etching.....	663
10.5.4	Etching Models—More Advanced Models.....	669
10.5.5	Other Etching Simulations	671
10.6	Limits and Future Trends in Technologies and Models	675
10.7	Summary of Key Ideas	676
10.8	References	677
10.9	Problems	679

Chapter 11 Back-End Technology 681

11.1	Introduction.....	681
11.2	Historical Development and Basic Concepts	687
11.2.1	Contacts	688
11.2.2	Interconnects and Vias.....	695

11.2.3	Dielectrics	707
11.3	Manufacturing Methods and Equipment.	715
11.3.1	Silicided Gates and Source/Drain Regions	716
11.3.2	First-level Dielectric Processing	718
11.3.3	Contact Formation	719
11.3.4	Global Interconnects	721
11.3.5	IMD Deposition and Planarization	723
11.3.6	Via Formation	724
11.3.7	Final Steps	725
11.4	Measurement Methods.	725
11.4.1	Morphological Measurements	726
11.4.2	Electrical Measurements	726
11.4.3	Chemical and Structural Measurements	732
11.4.4	Mechanical Measurements	734
11.5	Models and Simulation.	737
11.5.1	Silicide Formation.	738
11.5.2	Chemical-Mechanical Polishing	744
11.5.3	Reflow	746
11.5.4	Grain Growth	753
11.5.5	Diffusion in Polycrystalline Materials	762
11.5.6	Electromigration.	765
11.6	Limits and Future Trends in Technologies and Models	776
11.7	Summary of Key Ideas	780
11.8	References	781
11.9	Problems	784

Appendices 787

A.1	Standard Prefixes	787
A.2	Useful Conversions.	787
A.3	Physical Constants	788
A.4	Physical Properties of Silicon	788
A.5	Properties of Insulators Used in Silicon Technology	789
A.6	Color Chart for Deposited Si_3N_4 Films Observed Perpendicularly under Daylight Fluorescent Lighting.	789
A.7	Color Chart for Thermally Grown SiO_2 Films Observed Perpendicularly under Daylight Fluorescent Lighting	790
A.8	Irwin Curves	791
A.9	Error Function.	793
A.10	List of Important Symbols	797
A.11	List of Common Acronyms	798
A.12	Tables in Text.	801
A.13	Answers to Selected Problems	802

Index 805

5.2.3.3 Basic Properties and Characterization of Resists

Two basic parameters are often used to describe the properties of photoresists: contrast and the Critical Modulation Transfer Function (*CMTF*). We will define these terms and explain their importance in the following paragraphs. Contrast is really a measure of the resist's ability to distinguish light from dark areas in the aerial image the exposure system produces. As we have seen, diffraction effects and perhaps other imperfections in the exposure system result in an aerial image that does not have abrupt transitions from dark to light. An important question is how the resist responds to the "gray" region at the edges of features in the aerial image.

Contrast is an experimentally determined parameter for each resist and its value is extracted from plots like that shown in Figure 5–20. The data from which these plots can be derived are obtained by exposing resist layers to a variety of exposure doses. Each of the samples is then developed for a fixed period of time and the thickness of the photoresist remaining after developing is measured. For positive resists, samples receiving small exposure doses will not be attacked by the developer to any appreciable extent; those receiving large doses will completely dissolve in the developer. Intermediate doses will result in partial dissolution of the resist. For negative resists, the opposite behavior occurs. Given data like those shown in the figure, the contrast is simply the slope of the steep part of the curve, defined as

$$\gamma = \frac{1}{\log_{10} \frac{Q_f}{Q_0}} \quad (5.13)$$

where Q_0 is the dose at which the exposure first begins to have an effect and Q_f is the dose at which exposure is complete.

Typical g-line and i-line resists achieve contrasts of 2–3 and Q_f values of about 100 mJ cm⁻². DUV resists achieve significantly better contrast and better sensitivities than this.

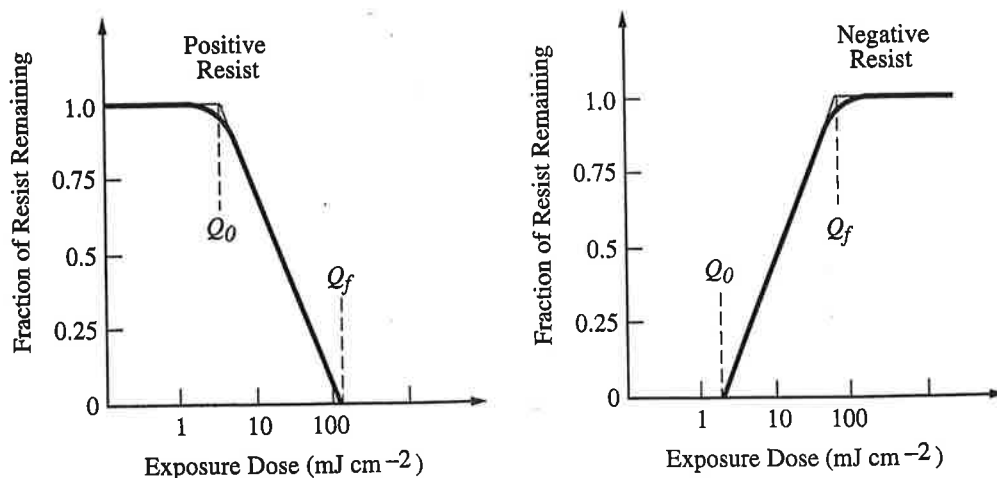


Figure 5–20 Idealized contrast curves for positive and negative resists.

This is basically because the chemical amplification that occurs in DUV resists steepens the transition from the unexposed to the exposed condition. (Once the reaction is begun, the catalytic nature of the process carries it to completion unlike DNQ resists where the *PAC* molecules in the resist must be exposed one by one by incoming photons during the exposure.) Thus DUV resists typically achieve γ values of 5–10 and Q_f values of about 20–40 mJ cm^{-2} .

It is important to note, however, that γ is not a constant for a particular resist composition. Rather, the experimentally extracted value of γ depends on process parameters like the development chemistry, bake times, temperatures before and after exposure, the wavelength of the exposing light, and the underlying structure of the wafer on which the resist is spun. In general it is desirable to have a resist with a high contrast because this produces better (steeper) edge profiles in the developed resist patterns. (See Figure 5–21.) Intuitively, this arises because a high contrast implies that the resist sharply distinguishes between dark and light areas in the aerial image. Thus resists with high contrast can actually “sharpen up” a poor aerial image.

The Modulation Transfer Function (*MTF*) of the aerial image was defined in Eq. (5.9) and in Figure 5–10. The *MTF* is simply a measure of the “dark” versus “light” intensities in the aerial image produced by the exposure system. It is often useful to define a similar quantity for the resist, in this case called the Critical *MTF* or *CMTF*. The *CMTF* is roughly the minimum optical transfer function necessary to resolve a pattern in the resist.

$$CMTF_{\text{resist}} = \frac{Q_f - Q_o}{Q_f + Q_o} = \frac{10^{1/\gamma} - 1}{10^{1/\gamma} + 1} \quad (5.14)$$

Typical *CMTF* values for g-line and i-line resists are around 0.4. With their higher γ values, chemically amplified DUV resists achieve significantly smaller *CMTF* values ($\approx 0.1 - 0.2$). The significance of this number is that the *CMTF* must be less than the aerial image *MTF* if the resist is going to resolve the aerial image.

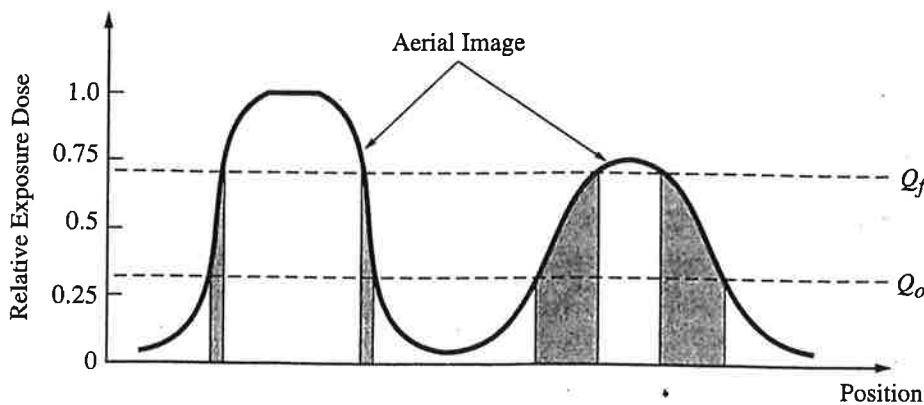


Figure 5–21 Example of how the quality of the aerial image and the resist contrast combine to produce the resist edge profile. The left side shows a sharp aerial image and steep resist edges (gray area). The example on the right shows a poorer aerial image and the resulting gradual edges on the resist profile.

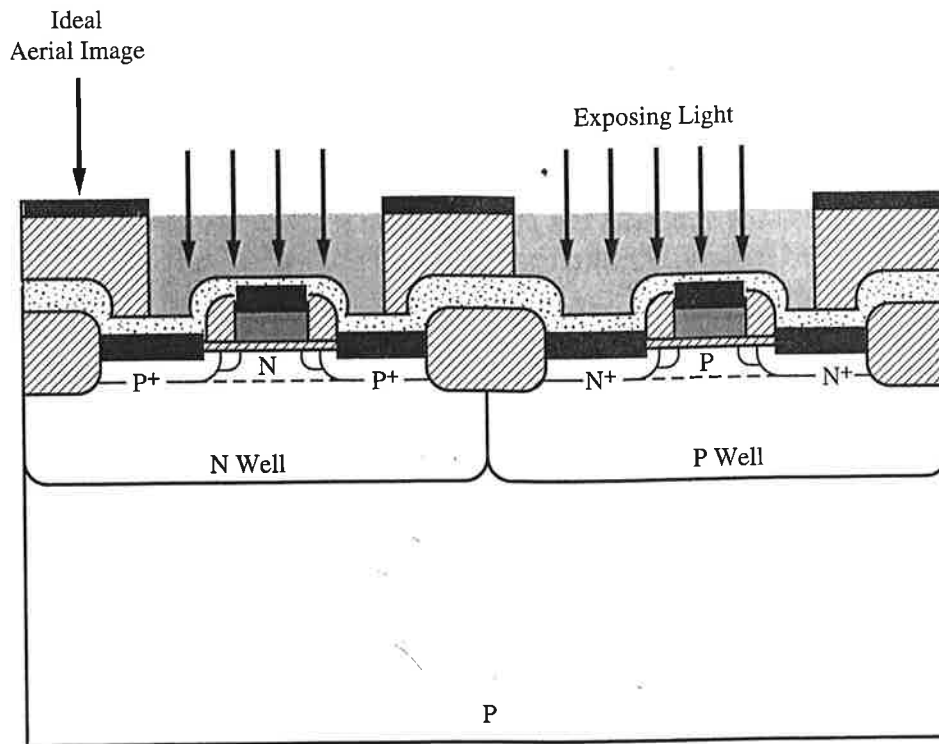


Figure 5-22 Exposure process associated with Figures 2-36 and 2-37 in the CMOS process in Chapter 2. The black bars in the aerial image represent areas on the mask that are opaque and hence ideally no photons strike the resist in these areas.

To this point in our discussion of resists we have effectively treated them as having uniform thickness and we have also treated the exposure process as occurring simultaneously throughout the volume of the resist material. In fact, neither of these is a very good assumption in many cases. Figure 5-22 illustrates some of these issues. Notice in that figure that the resist thickness tends to be nonuniform across the wafer because it is spun on as a liquid and therefore tends to fill in the “hills and valleys” of the underlying topography. The exposure process therefore often has to contend with exposing different regions with different thicknesses of resist. Effectively the resist is thinner on top of high structures and thicker over low lying structures. This may be a particular problem at the edges of underlying thin films where the resist thickness can change abruptly. The result of these effects is that the resist can be effectively underexposed where it is thicker and overexposed where it is thinner. This can result in linewidth variations, particularly where the photoresist features cross steps in the underlying structures.

A second issue is that the light absorption by the resist varies with depth below the surface of the resist and it also changes with time during the exposure process. Again imagine in connection with Figure 5-22 that the exposure process has just begun. The *PAC* concentration is assumed uniform throughout the resist. As *PAC* molecules near the resist surface absorb light photons, those photons are not available for exposing the deeper layers of the resist. Thus the light concentration falls off with depth. We will model this more carefully in Section 5.5, but to first order, the light intensity falls off exponentially with distance into the resist.

$$I = I_0 E^{-\alpha z} \quad (5.15)$$

where z is the depth below the surface, I_0 is the intensity at the surface, and α is the optical absorption coefficient in the resist. Thus the resist is first exposed near the top surface.

Fortunately a process known as “bleaching” occurs in g-line and i-line DNQ resists. As the resist is exposed, the *PAC* is altered, absorbing less and less light, and therefore it becomes more and more transparent. Thus as the top layers of the resist are exposed, they transmit more of the light to the deeper layers which are subsequently exposed. This results in a more uniform exposure. The bleaching process is not surprising since as the *PAC* component of these resists reacts and converts to carboxylic acid, more of the light will pass through to the deeper layers. Detailed modeling of these effects also has to include the light absorption by the novolac base component of the resist, as we will see in Section 5.5. Bleaching typically does not occur in DUV resists. This is a problem with these materials because the light can reflect off surfaces below the resist during the entire exposure. This can be mitigated by using antireflection coatings below the DUV resist (see below) and dyes in the resist itself to minimize reflections.

If there are highly reflective layers below the photoresist, light which passes all the way through the resist without being absorbed will be reflected by these underlying layers and pass back up through the resist again. While this may speed up the exposure process, it also has the potential for setting up standing wave light patterns in the resist because of constructive and destructive interference between the incoming and outgoing waves. Furthermore, if the light is scattered sideways, image resolution can be degraded. Figures 5–23 and 5–24 illustrate these issues. In some cases an Antireflective Coating (ARC) is deposited on the wafer prior to spinning on the resist. This can greatly help in minimizing standing wave effects, but of course increases process complexity. Another approach that is often used in g-line and i-line resists is to add dyes to the resist, which absorb light and minimize reflections.

The “scalloped edges” illustrated in Figure 5–24 are also strongly affected by post-baking of the resist after exposure but before development, since this heat treatment allows diffusion of the *PAC* in g-line and i-line resists or the *PAG* in DUV resists on a limited basis. This smoothes out the standing wave pattern. It is quite possible to model these standing wave effects and to predict the resulting resist edge patterns that result. We will consider these issues more carefully in Section 5.5.

5.2.4 Mask Engineering—Optical Proximity Correction and Phase Shifting

In our discussion to this point, we have considered the mask to be simply a digital device. That is, it has clear areas and dark areas and the patterns of these areas represent exactly the pattern that we wish to print in the resist on the wafer. It is actually possible to do better than this in designing the mask if the objective is to produce the highest quality aerial image. We will briefly discuss two approaches to doing this: Optical Proximity Correction (OPC) and Phase Shift Masks (PSMs). These approaches might be considered “mask engineering.” These methods are also sometimes called “wavefront engineering” [5.12].