

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01376
Patent 6,197,696 B1

PETITIONER'S UPDATED EXHIBIT LIST

In accordance with 37 C.F.R. § 42.63(e), Petitioner hereby submits a current listing of Taiwan Semiconductor Manufacturing Company, Ltd.'s exhibits to counsel for Patent Owner.

LIST OF EXHIBITS

Exhibit No.	Description	Previously Filed
Exhibit 1001	U.S. Patent No. 6,197,696 to Aoi et al.	x
Exhibit 1002	Expert Declaration of Dr. Bruce W. Smith, Ph.D.	x
Exhibit 1003	U.S. Patent No. 3,617,824 to Shinoda et al.	x
Exhibit 1004	U.S. Patent No. 3,838,442 to Humphreys.	x
Exhibit 1005	U.S. Patent No. 6,140,226 to Grill et al.	x
Exhibit 1006	U.S. Patent No. 5,635,423 to Huang et al.	x
Exhibit 1007	U.S. Patent No. 5,741,626 to Jain et al.	x
Exhibit 1008	C. Akrouit et al., "A 480-MHz Microprocessor in a $0.12\mu\text{m}$ L_{eff} CMOS Technology with Copper Interconnects," IEEE J. of Solid-State Circuits, Vol. 33, no. 11 (November 1998).	x
Exhibit 1009	J.N. Burghartz et al., "Monolithic Spiral Inductors Fabricated Using a VLSI Cu-Damascene Interconnect Technology and Low-Loss Substrates," International Electron Devices Meeting (December 1996).	x

Exhibit No.	Description	Previously Filed
Exhibit 1010	U.S. Patent No. 6,100,184 to Zhao et al.	x
Exhibit 1011	U.S. Patent No. 6,103,616 to Yu et al.	x
Exhibit 1012	File History of U.S. Patent No. 6,197,696 to Aoi et al.	x
Exhibit 1013	Japanese Patent Application No. 10-079371 to Aoi.	x
Exhibit 1014	Certified Translation of Japanese Patent Application No. 10-079371 to Aoi.	x
Exhibit 1015	Japanese Patent Application No. 11-075519 to Aoi.	x
Exhibit 1016	Certified Translation of Japanese Patent Application No. 11-075519 to Aoi.	x
Exhibit 1017	U.S. Provisional Patent Application No. 60/071,628.	x
Exhibit 1018	U.S. Patent No. 5,592,024 to Aoyama et al.	x
Exhibit 1019	Transcript of Teleconference with the Board, dated November 16, 2016.	x
Exhibit 1020	http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4251	Served only.
Exhibit 1021	“International Electron Devices Meeting. Technical Digest, Technical Digest of the International Electron Devices Meeting from December 8–11, 1996”	Served only.

Exhibit No.	Description	Previously Filed
Exhibit 1022	Burghartz et al., “Monolithic spiral inductors fabricated using a VLSI Cu-damascene interconnect technology and low-loss substrates”	Served only.
Exhibit 1023	http://ieeexplore.ieee.org/xpl/tocresult.jsp?isnumber=15684	Served only.
Exhibit 1024	G. Gerosa, “Introduction To The Digital Section, Publication Year: 1998,” IEEE Journal of Solid-State Circuits, Vol. 33, No. 11, Nov. 1998	Served only.
Exhibit 1025	J. Dreibelbis, “Introduction to the memory section, Publication Year: 1998,” IEEE Journal of Solid-State Circuits, Vol. 33, No. 11, Nov. 1998	Served only.
Exhibit 1026	L. E. Thon, “Introduction To The Signal Processing Section, Publication Year: 1998,” IEEE Journal of Solid-State Circuits, Vol. 33, No. 11, Nov. 1998	Served only.
Exhibit 1027	http://ieeexplore.ieee.org/xpl/tocresult.jsp?isnumber=15684&filter%3DAND%28p_IS_Number%3A15684%29&pageNumber=2	Served only.
Exhibit 1028	C. Akrouit et al., “A 480-MHz RISC microprocessor in a 0.12- μ m L_{eff} CMOS technology with copper interconnects,” IEEE Journal of Solid-State Circuits, Vol. 33, No. 11, Nov. 1998	Served only.
Exhibit 1029	Declaration of J. Preston Long	Served only.

Exhibit No.	Description	Previously Filed
Exhibit 1030	Excerpts from James D. Plummer et al., “Silicon VLSI Technology: Fundamentals, Practice, and Modeling” (2000).	
Exhibit 1031	Excerpts from C.Y. Chang & S. M. Sze, “ULSI Technology” (1996).	
Exhibit 1032	Excerpts from S. Wolf & R.N. Tauber, “Silicon Processing for the VLSI Era: Volume 1: Process Technology” (1986).	
Exhibit 1033	U.S. Patent No. 5,091,047 to Cleeves et al.	
Exhibit 1034	U.S. Patent No. 6,287,973 to Aoi et al.	
Exhibit 1035	U.S. Patent No. 4,560,436 to Bukhman et al.	
Exhibit 1036	U.S. Patent No. 6,091,081 to Matsubara et al.	
Exhibit 1037	U.S. Patent No. 4,473,437 to Higashikawa et al.	
Exhibit 1038	U.S. Patent No. 5,880,018 to Boeck et al.	
Exhibit 1039	U.S. Patent No. 4,832,789 to Cochran et al.	
Exhibit 1040	U.S. Patent No. 4,855,252 to Peterman et al.	
Exhibit 1041	U.S. Patent No. 5,786,276 to Brooks et al.	
Exhibit 1042	U.S. Patent No. 5,756,216 to Becker et al.	
Exhibit 1043	U.S. Patent No. 5,821,168 to Jain.	
Exhibit 1044	J.M. Moran & D. Maydan, “High Resolution, Steep Profile Resist Patterns,” J. Vac. Sci. & Tech., vol. 16, no. 6 (Nov./Dec. 1979).	

Exhibit No.	Description	Previously Filed
Exhibit 1045	M.M. O'Toole et al., "Linewidth Control in Projection Lithography Using a Multilayer Resist Process," IEEE Transactions on Electron Devices, vol. ED-28, no. 11 (Nov. 1981).	
Exhibit 1046	E. Bassous et al., "A Three-Layer Resist System for Deep U.V. and RIE Microlithography on Nonplanar Surfaces," J. Electrochem. Soc.: Solid-State Sci. & Tech. (Feb. 1983).	
Exhibit 1047	Transcript of the Deposition of Dr. A. Glew (June 30, 2017).	
Exhibit 1048	U.S. Provisional Patent Application No. 60/071,628 (with line numbering appended).	
Exhibit 1049	Expert Declaration of Dr. Bruce W. Smith, Ph.D. in Support of Petitioner's Reply	

Petitioner hereby certifies that copies of all listed documents above have been served on counsel for Godo Kaisha IP Bridge.

Dated: July 21, 2017

Respectfully submitted,

By: /Darren M. Jiron/
Darren M. Jiron, Lead Counsel
Reg. No. 45,777

Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), this is to certify that I caused to be served true and correct copies of the **PETITIONER'S UPDATED EXHIBIT LIST and TSMC Exhibits 1030-1049** by electronic mail, this 21st day of July, 2017, on counsel of record for the Patent Owner as follows:

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