UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01376
Patent 6,197,696 B1

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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Exhibit 1019: Transcript of Teleconference with the Board, dated November 16, 2016.

Exhibit 1020: http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=4251.

Exhibit 1021: IEEE, "Technical Digest of the International Electron Devices," 1996 International Electron Devices Meeting at San Francisco, CA, Table of Contents (December 8-11, 1996).

Exhibit 1022: J.N. Burghartz et al., "Monolithic spiral inductors fabricated using a VLSI Cu-damascene interconnect technology and low-loss substrates," 1996 International Electron Devices Meeting at San Francisco, CA, pp. 99-102 (December 8-11, 1996).

Exhibit 1023: http://ieeexplore.ieee.org/xpl/tocresult.jsp?isnumber=15684.

Exhibit 1024: G. Gerosa, "Introduction to the Digital Section," IEEE Journal of Solid-State Circuits, vol. 33, no. 11, p. 1599 (Nov. 1998).

Exhibit 1025: J. Dreibelbis, "Introduction to the Memory Section," IEEE Journal of Solid-State Circuits, vol. 33, no. 11, p. 1649 (Nov. 1998).

Exhibit 1026: L.E. Thon, "Introduction to the Signal Processing Section," IEEE Journal of Solid-State Circuits, vol. 33, no. 11, pp. 176-643 (Nov. 1998).

Exhibit 1027: http://ieeexplore.ieee.org/xpl/tocresult.jsp?isnumber=15684&filter%3DAND%28p_IS_Number%3A15684%29&pageNumber=2.

Exhibit 1028: C. Akrout et al., "A 480-MHz RISC Microprocessor in a 0.12-μm L_{eff} CMOS Technology with Copper Interconnects," IEEE Journal of Solid-State Circuits, vol. 33, no. 11, pp. 1609-16 (Nov. 1998).

Exhibit 1029:	Declaration of J. Preston Long dated February 15, 2017.
Exhibit 1030:	Excerpts from James D. Plummer et al., “Silicon VLSI Technology: Fundamentals, Practice, and Modeling” (2000).
Exhibit 1031:	Excerpts from C.Y. Chang & S. M. Sze, “ULSI Technology” (1996).
Exhibit 1032:	Excerpts from S. Wolf & R.N. Tauber, “Silicon Processing for the VLSI Era: Volume 1: Process Technology” (1986).
Exhibit 1033:	U.S. Patent No. 5,091,047 to Cleeves et al.
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Exhibit 1042:	U.S. Patent No. 5,756,216 to Becker et al.
Exhibit 1043:	U.S. Patent No. 5,821,168 to Jain.
Exhibit 1044:	J.M. Moran & D. Maydan, “High Resolution, Steep Profile Resist Patterns,” J. Vac. Sci. & Tech., vol. 16, no. 6 (Nov./Dec. 1979).
Exhibit 1045:	M.M. O’Toole et al., “Linewidth Control in Projection Lithography Using a Multilayer Resist Process,” IEEE Transactions on Electron Devices, vol. ED-28, no. 11 (Nov. 1981).

Exhibit 1046:	E. Bassous et al., "A Three-Layer Resist System for Deep U.V. and RIE Microlithography on Nonplanar Surfaces," J. Electrochem. Soc.: Solid-State Sci. & Tech. (Feb. 1983).
Exhibit 1047:	Transcript of the Deposition of Dr. A. Glew (June 30, 2017).
Exhibit 1048:	U.S. Provisional Patent Application No. 60/071,628 (with line numbering appended).
Exhibit 1049:	Declaration of Dr. Bruce W. Smith, Ph.D. in Support of Petitioner's Reply.

I. INTRODUCTION

IPB does not dispute the *Grill-Aoyama* combination teaches every limitation of claims 13 and 15. All IPB argues is *Grill* is not prior art and a POSITA would not have combined the references.

On the first issue, IPB must overcome two obstacles to remove *Grill* as prior art but cannot. First, IPB fails to establish support for claim 13 in JP '371 because it misapplies the Board's construction of "using the [designated layer] as a mask." Second, IPB cannot credibly challenge *Grill*'s entitlement to the benefit of its parent application because its sole argument—that one sentence in *Grill* constituted new matter—ignores disclosures in the parent that convey the same information.

On the second issue, a POSITA would have found it obvious to combine *Grill* and *Aoyama* because they complement one another to minimize the consequences of misalignment during photolithography. IPB's contrary arguments address combinations TSMC never proposed and contain manifest factual errors.

Because IPB could not provide any credible challenges to the Board's preliminary findings, and because a preponderance of evidence supports the instituted obviousness combination, the Board should cancel the challenged claims.

II. ARGUMENT

A. *Grill* is prior art because its Japanese parent, JP '371, does not support the challenged claims, and because *Grill*'s priority date predates JP '371.

Grill is presumptively prior art because it was filed before the application for the '696 patent. For IPB to remove *Grill* as prior art, it must (1) show JP '371, the Japanese parent to the '696 patent, supports the challenged claims, and (2) deny *Grill* the benefit of its parent's filing date for prior art purposes. IPB cannot clear either hurdle.

1. IPB has the burden of proving JP '371 supports the challenged claims, and TSMC had no obligation to disprove that in its petition.

IPB bears the burden to establish earlier priority for the challenged claims. Paper 9, 1-3. *Grill* is presumptively prior art, so TSMC did not need to rebut a priority claim until IPB made one. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1379-80 (Fed. Cir. 2015).

Priority is assessed claim-by-claim, *Lucent Techs., Inc. v. Gateway, Inc.*, 543 F.3d 710, 718 (Fed. Cir. 2008), and contrary to IPB's allegation (Paper 19, 32), a priority document listed on the patent's face does not indicate whether or how a patent owner might allege priority for any particular claim.[1] In *Tech. Licensing*

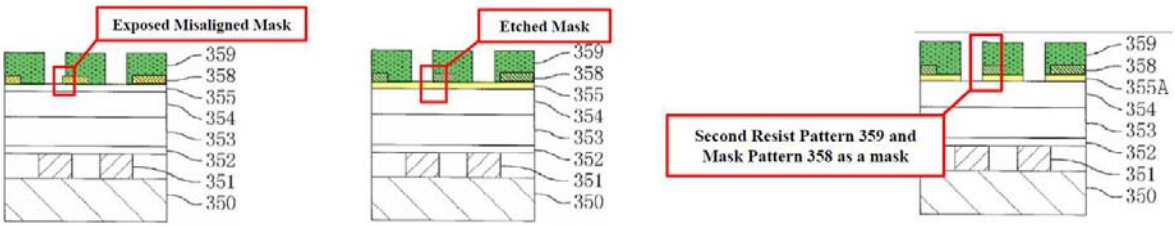
[1] For example, IPB alleges priority for claim 13 but not claim 15.

Corp. v. VideoTek, Inc., 545 F.3d 1316, 1327-28 (Fed. Cir. 2008), from which *Drinkware* draws extensively, and *Core Survival, Inc. v. S&S Precision, LLC*, PGR2015-00022, Paper 8, 8-10 & n.3 (P.T.A.B. Feb. 19, 2016), the patents-at-issue listed priority documents, but the patent owner still bore the burden of proof.

Although the law did not require TSMC to guess IPB's strategy and preemptively dispute it, TSMC put IPB on notice of its arguments as the Board recommends. Paper 2, 20-29 & n.3; EX1002 (App'x B); *see also Core Survival*, Paper 8, 9-10 & n.3.

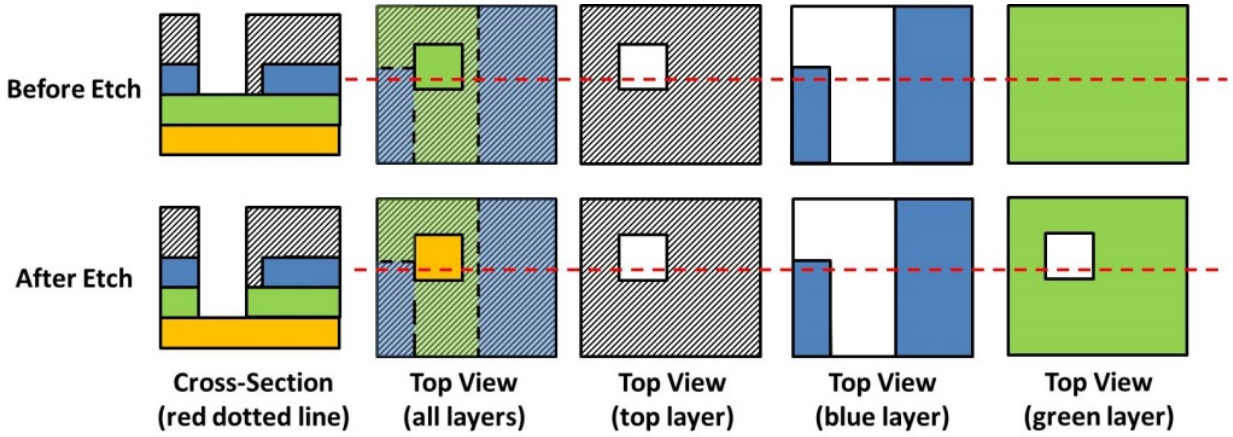
2. The Board's claim construction does not support IPB's argument that JP '371 discloses claim 13.

The Board adopted IPB's proposed construction that "using the [designated layer] as a mask" means using the designated layer to "define areas for etching." Paper 11, 18. To argue JP '371 supports claim 13, IPB relies on the false premise that a buried layer "define[s] areas for etching" whenever it has a vertical sidewall "in line and flush with an edge of overlying layer" (e.g., layer 358 below). Paper 19, 8-14, 24-27. The Board already rejected IPB's argument (Paper 11, 17), and it should continue to do so.



a. IPB has no support for its misapplication of "mask."

IPB asserts a buried layer "defines an area for etching" even when it has nothing to do with the etch. *See* Paper 19, 24-28. To illustrate IPB's mistake, consider the images below. The striped layer contains the via (i.e., contact-hole) pattern, the blue layer contains a wiring pattern, and the etch transfers the via pattern into the green layer.

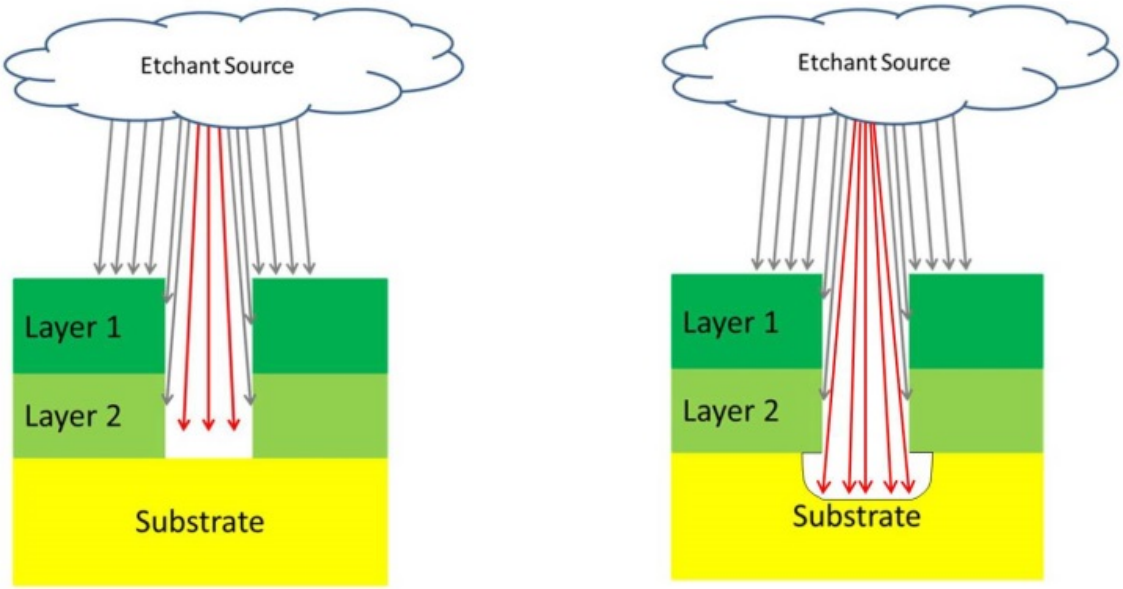


IPB believes the blue layer is a mask even though it plays no role defining the square-shaped via pattern, which is what a mask does. EX1049, ¶29.

IPB speculates a buried layer blocks laterally traveling particles (Paper 19, 16), but the etches at issue are highly directional with negligible lateral deviation. EX1030, 25 ("[M]odern fabrication methods tend to employ directional etching and vertical steps with little undercutting."), 39 ("[I]t is usually assumed that all the ions arrive normal to the wafer surface, as shown in Figure 10-11(b)."), 41 ("Since the ions are striking normal to the wafer surface, the enhancement will occur

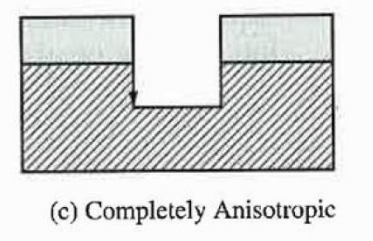
normal to the wafer surface."); EX1031, 56 ("[T]ransport must be perpendicular to the surface so that only the etch rate of the bottom surface is enhanced."); EX1049, ¶11.

IPB introduced the figure on the left below (Paper 19, 16), but it inaccurately depicts what occurs in reactive ion etching ("RIE"). The non-vertical trajectories IPB posits would undercut the layer being etched, as shown on the right. EX1049, ¶12. This does not occur in practice (*id.*), disproving IPB's speculation.



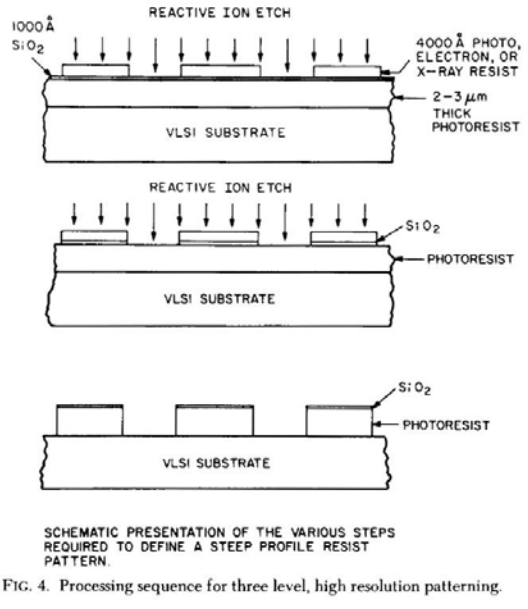
In RIE, "the profiles are not just a linear combination of isotropic chemical etching and anisotropic physical etching," but are "much more like the case for physical etching acting alone, as in Figure 10-3(c) [below]." EX1030, 40. "Since the ions are striking normal to the wafer surface," RIE "result[s] in directional, anisotropic etching." EX1030, 41. "If the chemical component in the etch system is

increased, the vertical etching is increased but not the lateral etching, which is not what would be expected." EX1030, 40; *see also* EX1049, ¶¶13-15.

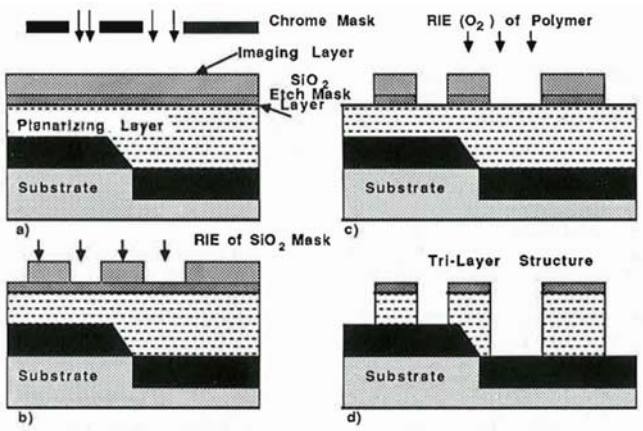


EX1030, Figure 10-3(c)

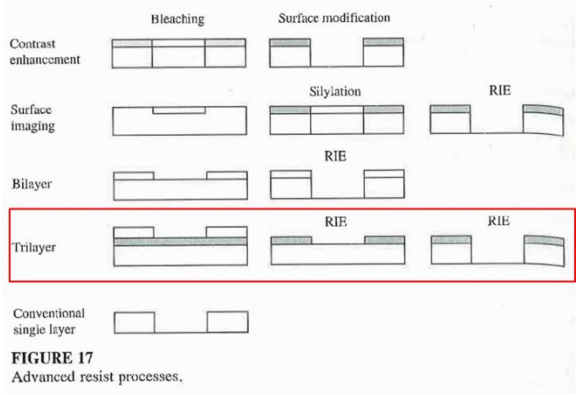
IPB's discussion of tri-layer "masks"—more aptly tri-layer resist "processes" (EX2015, 7-8; EX1031, 41-42, 70; EX1032, 13-14)—fails to support its position. A tri-layer resist process (depicted in the figures below) begins with an intermediate hard mask layer (e.g., SiO_2) sandwiched between a top photoresist layer and a bottom planarization/primary layer. EX1031, 41-42; EX1032, 14; EX1033, 2:28-35; EX2015, 8; EX1049, ¶18.



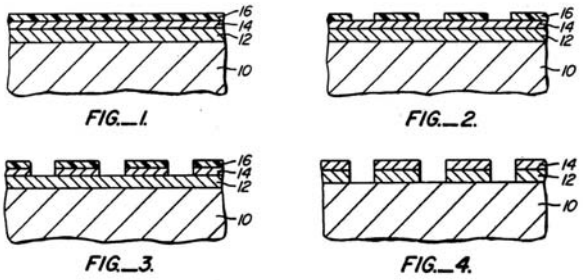
EX1044, Figure 4



EX1032, Fig. 11



EX1031, FIGURE 17



EX1033, FIGS. 1–4

The top resist layer is the mask for patterning the intermediate layer, and afterward, the intermediate layer acts as the mask for etching the bottom layer. EX1033, Abstract; EX1031, 41-42, 70, FIG. 17; EX1032, 14, Fig. 11; EX2010, 60:22-63:2; EX1033, 3:20-22, 3:29-30; EX1049, ¶18. The intermediate layer is not a mask because of its sidewalls; it becomes a mask after eliminating the top resist layer, as shown above. EX1031, 41-42, FIG. 17; EX1032, 14, Fig. 11; EX1033, 3:20-41; EX2010 at 61:14-63:2; EX1044, 4-6; EX1045, 3; EX1046, 2-3; EX1049, ¶18. The bottom layer is also not a mask for etching the layer below it. Contrary to IPB's allegations, neither TSMC's expert nor his textbook suggests otherwise.[2] EX1049, ¶¶16-19.

[2] IPB mistakenly suggests Figure 12.3(c) in Dr. Smith's book contradicts this understanding (Paper 19, 17-18), but it misinterprets Figure 12.3(c), which does not depict a structure. EX2010, 61:14-63:2. Citing EX1044 through EX1046

b. Inconsistencies in the intrinsic evidence do not justify IPB's priority argument.

IPB cherry-picks three examples where the specification incorrectly refers to a buried layer as a "mask" (EX1001, 17:35-40, Figs. 13(b), 13(c) (layer 305A); 19:50-54, Figs. 16(c), 16(d) (layer 355A); 26:22-29, Figs. 28(b), 29(a) (layer 556B)), ignoring at least seven contrary examples (EX1001, 11:51-55, Figs. 2(c), 3(a) (103A not a mask), 13:37-41, Figs. 6(a), 6(b) (103A not a mask), 14:41-45, Figs. 8(a), 8(b) (103A not a mask), 16:7-11, Figs. 10(c), 11(a) (203A not a mask), 17:20-29, Figs. 13(a), 13(b) (305A and 304A not masks), 19:33-38, Figs. 16(a), 16(b) (355A not a mask), 21:33-39, Figs. 18(c), 19(a) (405A not a mask)). *See* EX1049, ¶¶21, 27.

Even IPB's declarant admits the '696 patent sometimes uses "mask" incorrectly. EX1047, 97:12-99:21 (admitting layer 509 not a mask in EX1001, 23:40-46, Figs. 22(b), 22(c), despite contrary textual description); *see also* EX1049, ¶¶23-26.

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as sources, Dr. Smith's figure illustrates a tri-layer process sequence using one composite image instead of 3-4 discrete images as in the figures above. EX1049, ¶18; EX2018, 18-19 (Ref. [7]), 33 (Refs. [53], [56]).

The specification does not consistently use "mask" in the manner IPB suggests, and three inconsistent examples do not redefine the term "mask." EX1049, ¶¶20-28; *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir. 1995) ("[A]ny special definition given to a word must be clearly defined."); *see also* EX1049, ¶¶20-28. "The patentee cannot rely on its own use of inconsistent and confusing language in the specification to support a broad claim construction which is otherwise foreclosed." *Trs. of Columbia Univ. v. Symantec Corp.*, 811 F.3d 1359, 1366 (Fed. Cir. 2016); *see also Bayer CropScience AG v. Dow Agro Sciences LLC*, 728 F.3d 1324, 1328-29 (Fed. Cir. 2013).

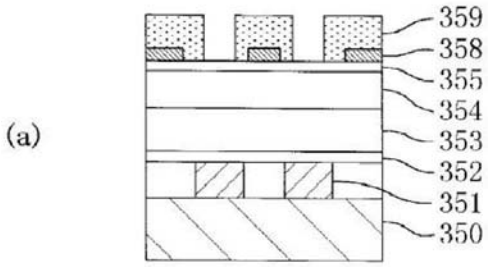
IPB has no basis for asserting the district court would have applied the construction differently. The district court never addressed this issue.

3. Even if the Board applies the construction the way IPB advocates, IPB's priority claim fails.

Although the Board denied claim 13 entitlement to priority before March 23, 1999[3] (Paper 11, 19-26), IPB recycled its flawed argument that "claim 13 is fully supported under §112 ¶1 by at least the third embodiment variant disclosed in [JP] '371." Paper 19, 20.

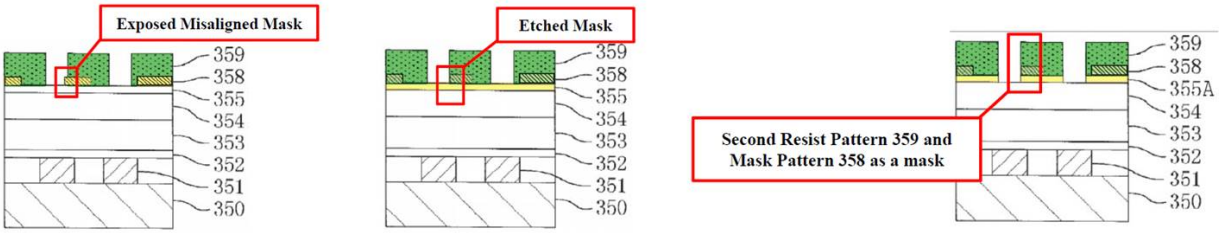
[3] IPB does not allege earlier priority for claim 15.

Step h) of claim 13 requires "dry-etching the third insulating film using . . . the mask pattern as a mask," but layer 358 ("mask pattern") is not a mask for etching layer 355 ("third insulating film"). Instead, "the second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask." EX1014, ¶93, Fig. 16(a);[4] EX2012, 38:10-13.



EX1014, Fig. 16(a)

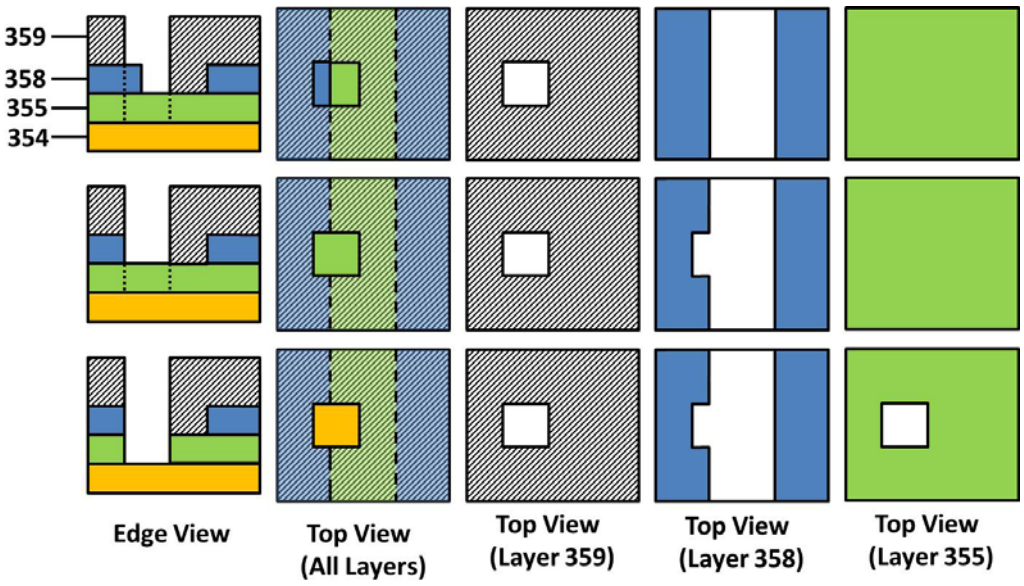
IPB argues JP '371 discloses step h) through a description of how to mitigate misalignment damage (Paper 19, 24-27 (see figures below); EX2012, 39:12-23), but this description actually contradicts IPB's position. EX1049, ¶¶30-33.



[4] Although TSMC does not believe its translation to be in error, none of IPB's alleged inconsistencies affects TSMC's arguments.

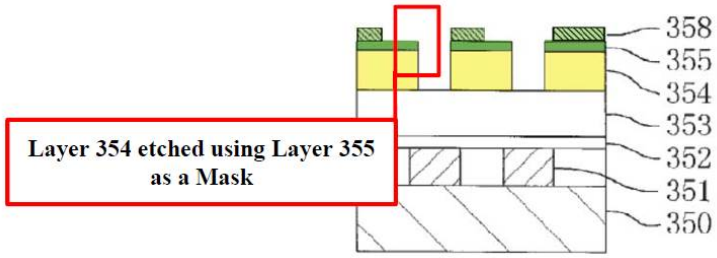
The specification identifies layer 359, not layer 358, as the mask for etching layer 355 above. EX2012, 39:12-16 ("[T]he mask pattern 358 should be dry-etched using the second resist pattern 359 as a mask before the second silicon dioxide film 355 is dry-etched using the second resist pattern 359 as a mask."). In fact, the sole purpose of the process is to eliminate exposed portions of layer 358 so it does not act as a mask. EX1014, ¶96; EX2012, 39:16-21; EX1049, ¶31. By leaving the exposed portions of layer 358 in place, layer 358 would define a narrower via than designed, causing increased contact resistance, void formation during metallization, reduced reliability, and failed contacts. EX1001, 13:51-55, Fig. 6(c); EX1049, ¶31.

IPB offers no reason a POSITA would have thought layer 358, which contains the wiring pattern, would define the via pattern, especially when the goal of the process is to faithfully reproduce the via pattern from layer 359 in layer 355. EX1014, ¶93; EX2012, 38:13-17; EX1049, ¶32. EX1049, ¶¶29-33. The following images show the plan view corresponding to the process IPB describes, and confirm that only layer 359 defines the area etched in layer 355. EX1014, ¶¶93, 96; EX2012, 38:13-17, 39:12-16; EX1049, ¶32.

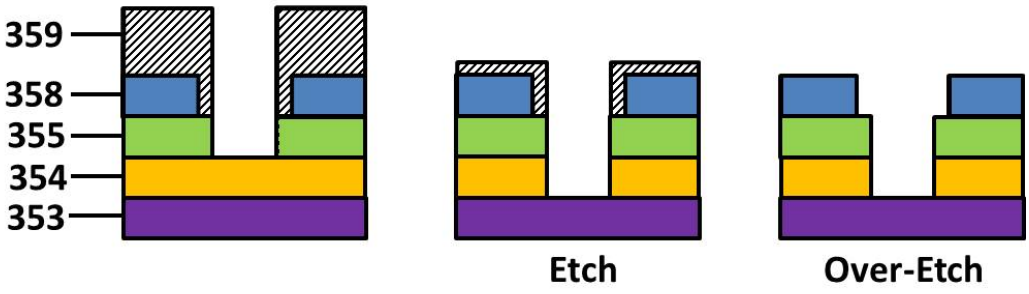


This situation differs from the all of the examples in the specification IPB suggests are buried "masks." In those examples, the buried layer contains the same pattern as the top layer. In contrast, buried layer 358 above contains the wiring pattern, and top layer 359 contains the via pattern. IPB provides no evidence a buried layer containing a different pattern than the top layer is a mask as IPB's priority argument requires. EX1049, ¶33.

JP '371 also fails to disclose step i) of claim 13. EX1049, ¶¶34-36. The image below illustrates IPB's flawed argument to the contrary. *See* Paper 19, 26-27.

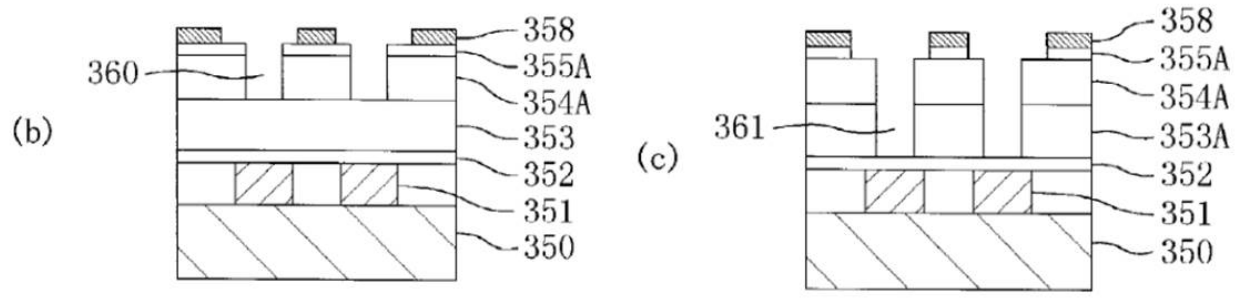


IPB suggests layers 359 (not shown) and 355 together define areas for etching layer 354, but JP ’371 states that only layer 359 is the mask for etching layer 354. EX1014, ¶93. When JP ’371 explains layer 359 acts as a mask for etching layer 354 and “is removed during the step of etching the organic film 354” (EX1014, ¶93; EX2012, 38:13-19), it does not mean layer 355 is exposed partway through the etch to act as a mask. Because only layer 359 is identified as a mask (and not layer 355), a POSITA would have understood layer 354 is fully patterned before layer 359 is completely removed. EX1049, ¶¶35-36. This is consistent with a well-known “overetch” technique (see below) often used to remove residual material over stepped structures as in JP ’371. EX1030, 28 (“[O]veretching is also required to remove residual film from steps.”); EX1049, ¶36.



If, as IPB suggests, layer 355 were a mask for etching layer 354, it would be identified as such together with layer 359 the way JP ’371 identifies both layers 355A and 354A as masks for etching layer 353 (see below). EX1014, ¶94, FIGS. 16(b), 16(c). Unlike layer 359, layer 355A is relatively thin and is eliminated

before layer 353 is fully patterned. *Id.* This leaves layer 354A exposed to act as a mask partway through the etch, consistent with the Board's use of "mask." *See* Paper 11, 18 n.7. This does not happen with layer 355 while layer 354 is being etched (see above).



Claim 13 is not entitled to a priority date before March 23, 1999, and *Grill* remains prior art.

4. *Grill* benefits from the filing date of the '628 application because that application supports *Grill*'s claim 28.

Even if claim 13 were entitled to the filing date of JP '371, *Grill* would remain prior art to the challenged claims because it is entitled to the filing date of its parent '628 application, filed before JP '371. The '628 application contains all of *Grill*'s relevant teachings and supports *Grill*'s claim 28.[5] *See Drinkware*, 800 F.3d at 1381-82.

[5] The Board recognizes *Grill*'s §102(e) date is the filing date of its parent if the parent supports one of *Grill*'s claims. *See* Paper 19, 33-34 n.18.

The table below shows the '628 application's support for *Grill*'s claim 28, establishing *Grill*'s §102(e) date as January 16, 1998. *See also* EX1049, ¶¶37-54.

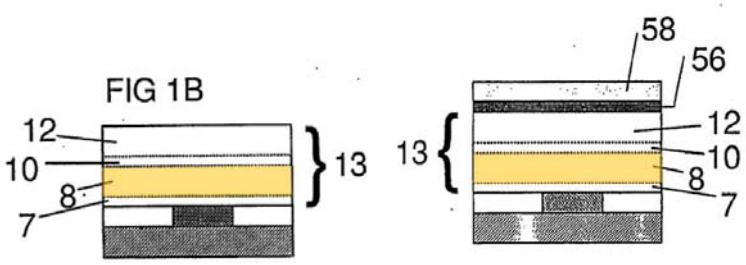
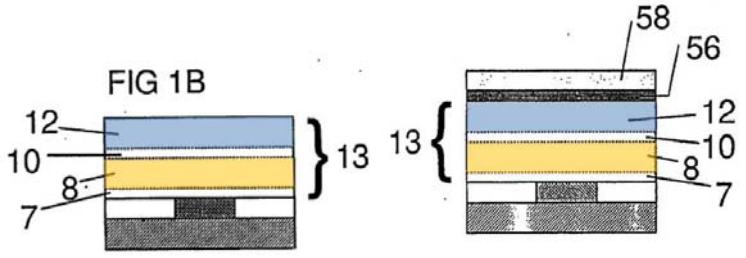
***Grill* Claim 28**	**'628 application**
A method for forming an interconnect structure on the upper surface of a **substrate** having conductive regions comprising the steps of:	See below.
forming over said **substrate** a **first dielectric layer** having a thickness corresponding to the thickness of an interconnect via,	EX1048, 15:11-12, 12:31-40. FIG 5A FIG 1B 
forming over said **first dielectric layer** a **second dielectric layer** having a thickness corresponding to the thickness of an interconnect wiring layer,	EX1048, 15:11-12, 12:31-40. FIG 5A FIG 1B 
forming a **first hard mask layer** over said **second [dielectric] layer**,	EX1048, 15:11-13.

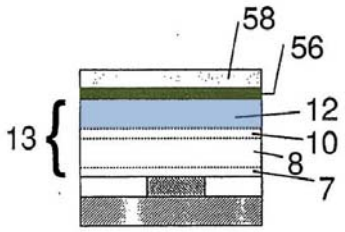
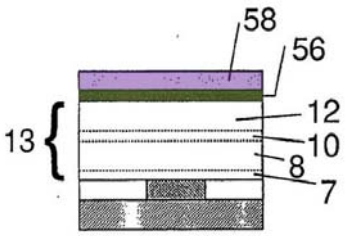
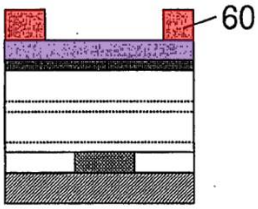
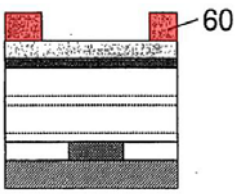
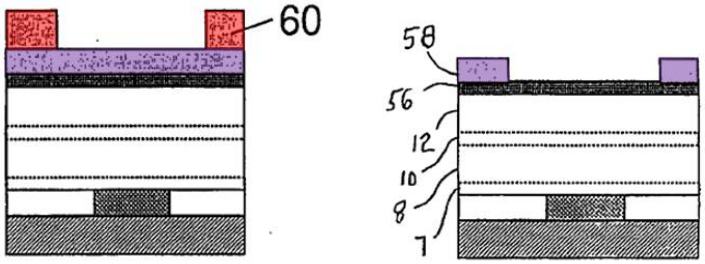
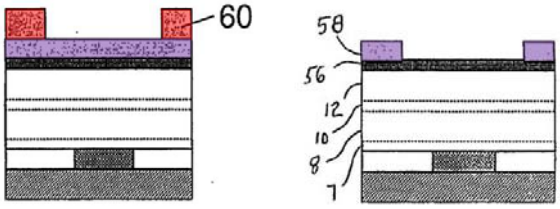
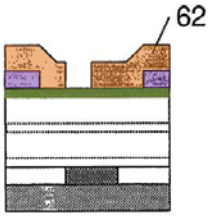
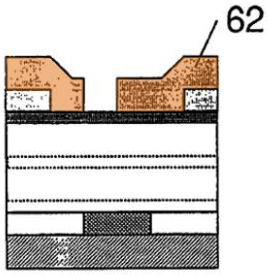
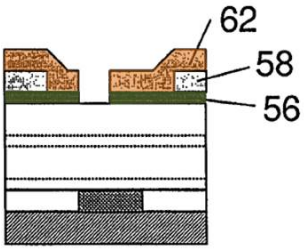
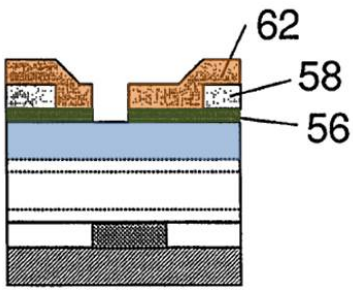
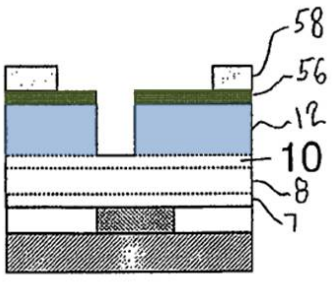
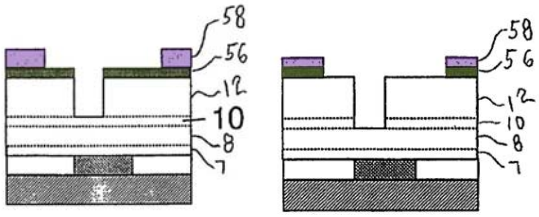
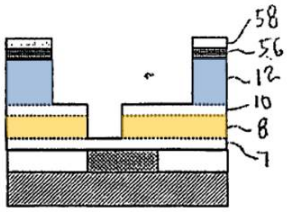
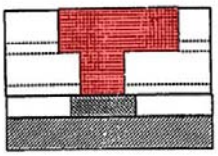
	FIG 5A 
forming a **second hard mask layer** over said **first hard mask layer**, said **second hard mask layer** preferably formed of a material different from said **first hard mask** to permit selective etching of said **second hard mask layer** with respect to said **first hard mask layer**,	EX1048, 15:11-22. FIG 5A 
forming a **first layer of resist** over said **second hard mask layer**,	EX1048, 15:17-18. FIG 5B 
patterning said **first layer of resist** with a wiring pattern,	EX1048, 15:17-18.

	FIG 5B 
patterning said **second hard mask layer** using said wiring-patterned **first layer of resist** as a mask,	EX1048, 15:19-22. FIG 5B FIG 5C 
removing said wiring-patterned **first layer of resist**,	EX1048, 15:17-22. FIG 5B FIG 5C  Layer 58 may be SiO_2 (EX1048, 15:14-17), and a POSITA would have known photoresist layer 60 would resist an SiO_2 etch, requiring subsequent removal. EX2020, 44-45 ("[T]he durability of commonly used positive resists is quite high, especially those used for the selective etching of SiO_2 and Si_3N_4.").
forming a **second layer of resist** over said **first** and **second** hard mask	EX1048, 15:23-24.

layer,	FIG 5D 
patterning said **second layer of resist** with a via pattern,	EX1048, 15:23-24. FIG 5D 
patterning said **first hard mask layer** using said via-patterned **second layer of resist** as a mask,	EX1048, 15:25-26. FIG 5E 
transferring said via pattern in said patterned **first hard mask layer** into said **second dielectric layer**, while concurrently removing said via-patterned **second layer of resist**, and	EX1048, 15:29-30. FIG 5E  FIG 5F 

	Although *Grill* added a statement that the "[p]atterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12," a POSITA understood this to be part of the disclosure. Photoresist layer 62 is concurrently removed while etching DLC layer 12 because they have similar etch characteristics. EX1048, 11:12-15, 12:37- 39, 15:23-24; *see also* EX1010, 6:43-53, 7:30-46, 8:9-18; EX1038, 6:19-26; EX1036, 13:54-59; EX1037, 1:30-35.
patterning said via-patterned **first hard mask layer** using said wiring-patterned **second hard mask layer** as a mask,	EX1048, 15:30-32. FIG 5F FIG 5G 
transferring, at least partially concurrently, said via pattern into said **first dielectric layer** to form via cavities corresponding to said **via pattern**, and said **wiring pattern** into said **second dielectric layer** to form wiring cavities corresponding to said wiring pattern, and	EX1048, 15:32-34. FIG 5H 
filling said cavities with **conductive material** to make electrical contact with said conductive	EX1048, 15:34-35.

regions and to form said vias and said wiring pattern.	FIG 1L 

The only element of claim 28 IPB challenges is the step of concurrently removing the via-patterned photoresist. Paper 19, 32-47; EX1005, 13:47-50 ("transferring said via pattern in said patterned first hard mask layer into said second dielectric layer, while concurrently removing said via-patterned second layer of resist"). IPB argues a POSITA would not have understood layer 62 ("via-patterned second layer of resist") to be removed while patterning layer 12 ("second dielectric layer") in the process shown below from the '628 application.

FIG 5E

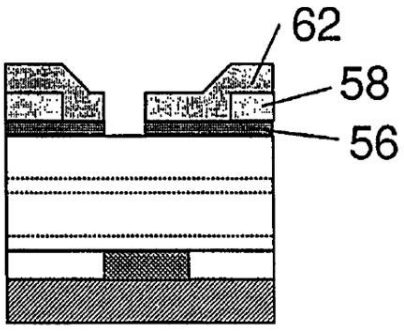
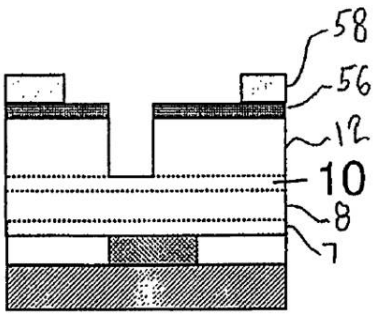


FIG 5F



Layer 62 is photoresist, and layer 12 is a carbon-based material, such as diamond-like carbon (DLC) or fluorinated DLC. EX1048, 12:37-38, 15:23-24. The '628 application explains photoresist and carbon-based dielectrics like DLC "have

similar etch characteristics" (EX1048, 11:12-15), so a POSITA would have known any process for patterning/etching layer 12 concurrently removes layer 62.[6] EX1049, ¶46.

Even without this explicit teaching, a POSITA would have understood photoresist layer 62 is removed while patterning carbon-based layer 12 because of their similar etch properties. *See, e.g.*, EX1036, 13:54-59 ("[T]he silicon oxide film can be etched until the DLC film 44 is exposed without removing the resist. It may then be removed at the same time that the DLC film 44, the amorphous carbon fluoride film 43, and the DLC film 42 are etched."); EX1010, 6:43-53 ("[T]he photoresist strip step can cause the removal of some of the low-$\in$ material of layer 14 residing below the opening 17, as shown in FIG. 5."), 7:30-46, 8:9-18; EX1038, 6:19-26 ("[P]hotoresist mask 44 used to define the opening within dielectric layer 40 is removed at the same time that dielectric layer 40 is etched."); EX1037, 1:30-35 ("[O]rganic material layer 2 is etched off anisotropically and resist layer 4 is removed as shown in FIG. 1(b)."); EX1049, ¶¶47-52.

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[6] IPB insists *Grill*'s claim 28 "requires 'removing' an entire layer" (Paper 19, 39"), but claim 28 reads "while concurrently removing," indicating the removal process need not be completed. The '696 patent also uses "removing" to include partial removal. EX1001, 11:19-31, 23:51-65, 26:3-14, 28:55-67, 30:62-31:6.

From the layer chemistries the ’628 application discloses and describes, a POSITA would have understood photoresist layer 62 is removed while patterning carbon-based layer 12. EX1049, ¶53.

IPB denies the ’628 application discloses concurrent removal of layer 62 because *Grill* added a sentence that reads, “Patterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12.” EX1005, 7:64-66. This sentence, though, merely confirms that it would be unusual not to remove layer 62 while patterning layer 12. This adds nothing to the disclosures of the ’628 application, which already explains layers 62 and 12 have similar etch characteristics. EX1048, 11:12-15. As such, the new sentence is a clarification, not new matter. *See TurboCare Div. of Demag Delaval Turbomachinery Corp. v. General Elec. Co.*, 264 F.3d 1111, 1118 (Fed. Cir. 2001) (“[T]he amendment served merely to clarify that [certain elements] were not illustrated.”) (reversing summary judgment premised on finding new matter); EX1049, ¶53.

B. A POSITA would have been motivated to combine *Grill* and *Aoyama* with a reasonable expectation of success.

Aoyama is one of many references that disclose well-known technology for making vias. *See, e.g.*, EX1039, 2:64-3:45, FIGS. 1-4; EX1040, 3:39-45, FIG. 6.

Applying that technique to *Grill* would have yielded predictable results and reduced the likelihood of misalignment. Paper 2, 52-56.

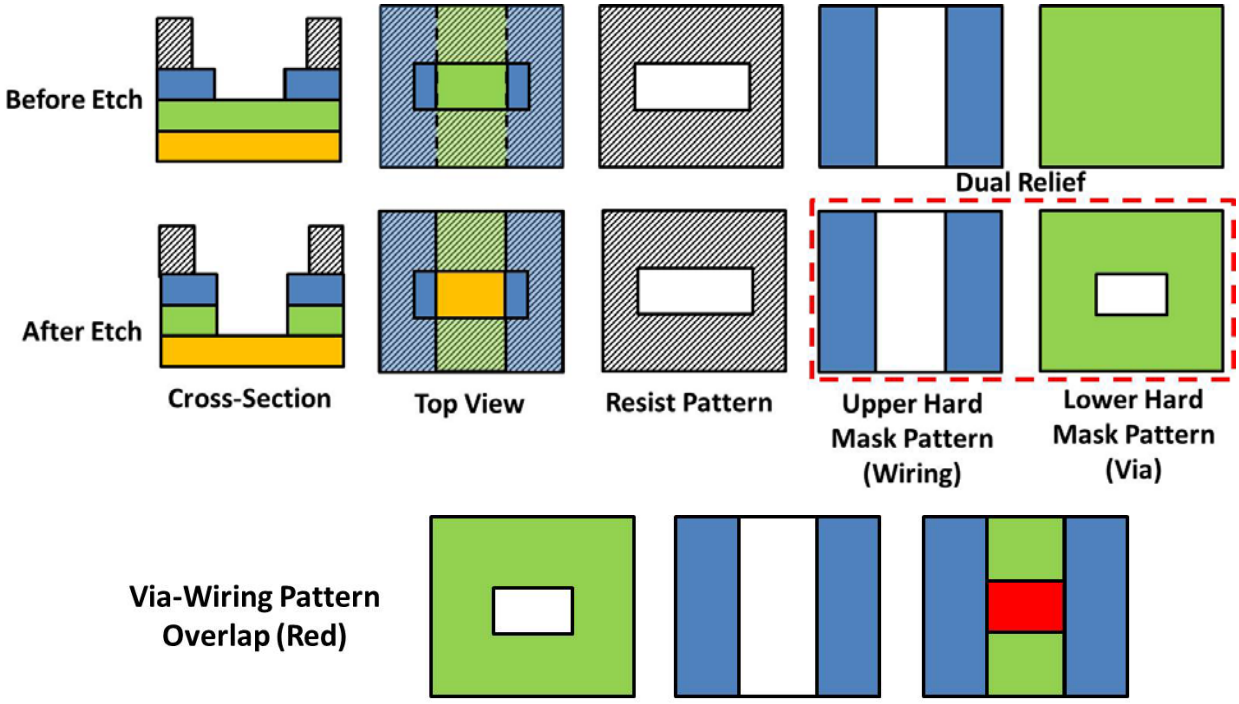
1. *Aoyama*'s via pattern complements *Grill*.

a. *Aoyama*'s via pattern is consistent with *Grill*'s "dual relief pattern."

"Dual relief pattern" refers to dual damascene technology: making wiring and via levels in the same processing module. EX1005, Abstract ("dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels"). IPB argues, without any technical reason or support, that a dual-relief pattern must have a cross-section like the figure on the left below. Paper 19, 50-54. But cross-sections like the figure on the right below are also dual relief patterns when the top layer (blue) contains a wiring pattern and the middle layer (green) contains a via pattern. EX1049, ¶56.

Nothing prohibits the wiring and via levels in a dual-relief pattern from having the same width. EX1049, ¶¶56-57. A dual-relief pattern is any structure "in which all features of a smaller area (via) pattern substantially overlap with the features of a larger area (wiring) pattern." EX1005, 7:22-30. The dual-relief pattern on the left is just "a special case of the general category of dual relief patterns." *Id.*

IPB's contrary argument neglects the three-dimensional aspect of dual relief patterns like the one on the right. The illustrations below provide the complete picture a POSITA would have understood. EX1049, ¶57. The dual relief pattern consists of the openings in the blue layer (wiring pattern) and the green layer (via pattern). Consistent with *Grill*, "all features of a smaller area (via) pattern substantially overlap with the features of a larger area (wiring) pattern." EX1005, 7:22-30. IPB has no basis for its suggestion that the via pattern in the *Grill-Aoyama* combination lacks a dual-relief pattern. EX1049, ¶¶55-57.



b. Using *Aoyama*'s via pattern would not change *Grill*'s operating principles.

IPB never argues a POSITA could not have implemented the *Grill-Aoyama* combination, nor does IPB deny the benefits of using *Aoyama*'s via patterning

scheme. IPB only argues *Grill* alone would be preferable to the *Grill-Aoyama* combination. Although TSMC disagrees (*see* Paper 2, 52-56), this argument is irrelevant because the law does not require a combination be the best alternative, only that a POSITA would have found it obvious. *In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012) ("[J]ust because better alternatives exist in the prior art does not mean that an inferior combination is inapt for obviousness purposes.").

IPB also suggests the *Grill-Aoyama* combination would "prematurely degrade[]" *Grill*'s upper hard mask 58 (Paper 19, 54-64 & n.25), but *Grill* teaches the opposite. "Hard mask layers 56 and 58 . . . have different etch properties from each other and from the dielectric underlayers 12 and 8." EX1005, 7:31-35. Because layer 58 has different etch properties from layers 56 and 12, a POSITA would not have been concerned about "premature" exposure of layer 58 while etching layers 56 and 12, because layer 58 resists those etches. EX1049, ¶¶58-65.

This error stems from a misunderstanding IPB and Dr. Glew have about etching and selectivity, arguing *Grill*'s SiO_2 layer 58 is necessarily etched "at a much faster rate" than a Si_3N_4 layer 56 "when both films are exposed to a silicon nitride etch process." Paper 19, 57-58. When, for example, a Si_3N_4 etch has a selectivity of 2-3 with respect to SiO_2, the Si_3N_4 etches 2-3 times faster than SiO_2, not the reverse as IPB and Dr. Glew state. EX1030, 27 (defining etch selectivity);

compare EX2020, 36, *with* EX2009, ¶155; *see also* EX1049, ¶¶59, 61-63. This fundamental mistake pervades IPB's analysis and renders it invalid.

A POSITA would have known many processes for selectively etching Si_3N_4 relative to SiO_2. EX1049, ¶60. IPB's own evidence explains that "favorable selectivity [of Si_3N_4 over SiO_2] (e.g. 9-10) can be obtained with the use of NF_3 plasmas." EX2020, 36; *see also* EX1031, 67 ("Si_3N_4 can be etched anisotropically in an RIE mode with high selectivity to Si and SiO_2 by CHF_3/O_2, CH_2F_2, or CH_3F."); EX1041, tbls. 3C, 3D, FIG. 4 (Si_3N_4/SiO_2 selectivity as large as 872); EX1030, 45 (noting the etch chemistries in EX1041 and EX1031 are "[v]ery anisotropic; selective over Si and SiO_2"); EX1042, 3:42-45 ("[T]he nitride 3 is removed at a rate 49 times faster than the oxide 2 is removed."). A POSITA would have known any of these well-known processes would prevent premature degradation of SiO_2 layer 58. EX1049, ¶60.

IPB also reads too much into *Grill*'s figures. The appearance of layer 58 in FIG. 5G as thinner than in FIG. 5F does not mean layer 58 is etched to any meaningful degree. *Grill*'s FIGS. 6G and 6H provide a counter-example. Layer 70 is SiO_2 and layer 68 is Si_3N_4, analogous to layers 58 and 56 in FIGS. 5G and 5H, but layer 70 is not thinner in FIG. 6H than in FIG. 6G after etching Si_3N_4 layer 68.

Even if were IPB correct that *Grill*'s layer 58 would be prematurely thinned, a POSITA would have known to avoid any conceivable negative consequences by

making layer 58 slightly thicker. EX1049, ¶65. Although IPB argues "widely varied" and "arbitrary" thickness variations would have caused problems with photolithography, the thickness variations at issue would have been negligible. *Id.*

2. *Grill* does not teach away from *Aoyama*'s via pattern.

a. *Aoyama*'s via pattern does not depend on a carbon etch-stop.

IPB has no basis for insisting the *Grill-Aoyama* combination must incorporate *Aoyama*'s carbon etch-stop. *See* Paper 19, at 65-70. "[A] determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements." *In re Mouttet*, 686 F.3d 1322, 1332-33 (Fed. Cir. 2012); *see also In re Applied Materials, Inc.*, 692 F.3d 1289, 1298 (Fed. Cir. 2012) ("A reference must be considered for everything that it teaches, not simply the described invention or a preferred embodiment.").

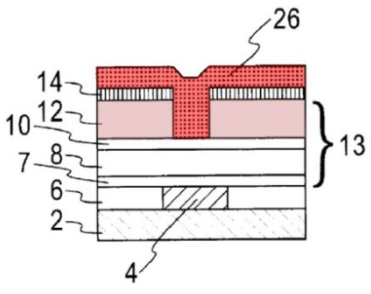
TSMC never suggested a POSITA would use any of *Aoyama*'s materials, so the Board should disregard IPB's analysis as irrelevant. TSMC only argued a POSITA would have combined *Aoyama*'s via pattern (i.e., using a via mask pattern wider than the wiring pattern) with *Grill*'s process, which already includes a layer functionally equivalent to *Aoyama*'s carbon etch-stop. Paper 2, 59-63. Via patterns wider than the wiring groove were well-known and did not require carbon etch-

stops. EX1039, 2:64-3:45, FIGS. 1-4; EX1040, 3:39-45, FIGS. 5-6; EX1049, ¶¶66-68.

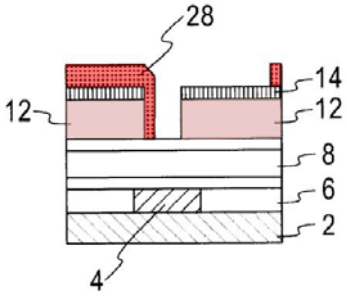
Aoyama's method is suitable for *Grill*'s process, as TSMC's Petition explains. Paper 2, 52-74. IPB's false comparison of *Aoyama*'s structure with and without stopper 45 (*see* Paper 19, 66) is irrelevant.

b. The *Grill-Aoyama* combination would not have caused misalignment or reduced critical dimension control.

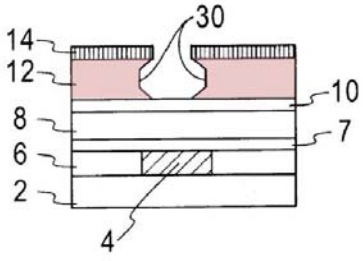
Grill describes a potential problem, illustrated below, which IPB incorrectly argues would be present when combining *Grill* with *Aoyama*'s via patterning scheme. *Grill*'s FIG. 2B below shows the result of misalignment during photolithography: a portion of photoresist 28 remains inside the opening in layer 12. Fixing this problem requires "rework" (removing the remaining photoresist 28 and re-doing the lithography steps). Rework damages carbon-based dielectric 12 as FIG. 2C shows, because photoresist 28 and carbon-based dielectric 12 have similar chemistries and etch characteristics. It is not feasible to remove layer 28 without also removing portions of layer 12. *See* EX1005, 5:9-33; EX1049, ¶¶71-72.



***Grill*, FIG. 2A**

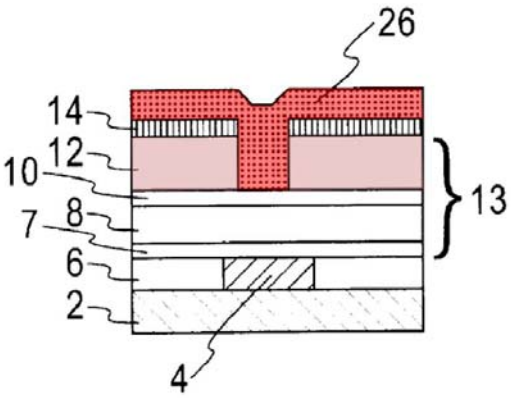


***Grill*, FIG. 2B**

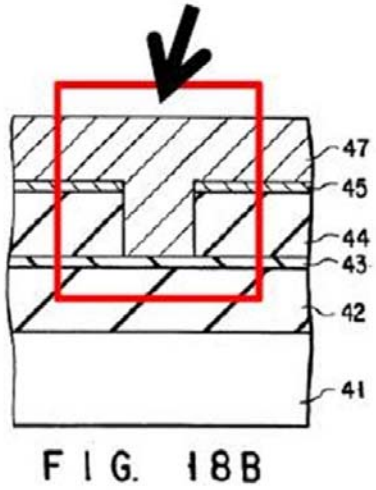


***Grill*, FIG. 2C**

IPB compares *Grill*'s FIG. 2A with a modified version of *Aoyama*'s FIG. 18B (below) to suggest this problem would occur in the *Grill-Aoyama* combination. Paper 19, 72; *see also* EX1049, ¶70. But neither figure depicts the *Grill-Aoyama* combination.

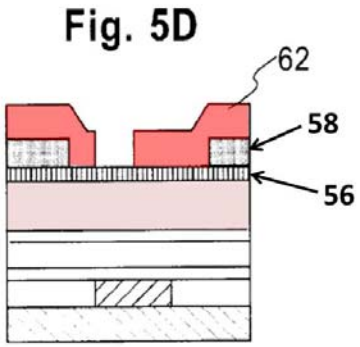


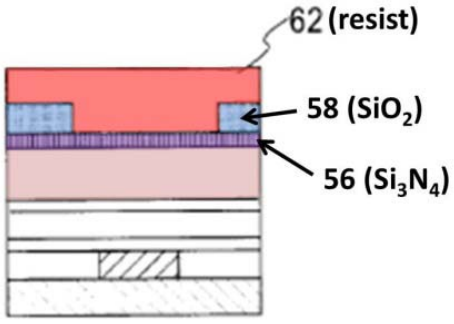
***Grill*, FIG. 2A**



***Aoyama*, FIG. 18B (modified by IPB)**

Unlike the single-hard mask processes above (layer 14 in *Grill*'s FIG. 2A and layer 45 in *Aoyama*'s FIG. 18), the *Grill-Aoyama* combination TSMC proposed uses *Grill*'s dual hard mask (e.g., layers 56 and 58 in FIG. 5D below). Additional hard-mask layer 56 shields carbon-based layer 12 (pink) from photoresist 62 (red) so the chemicals removing photoresist layer 62 never contact layer 12. *See* EX1005, 7:55-57 ("[L]ower hard mask layer 56 is still in place to protect dielectric 12."); EX1049, ¶¶71-72.





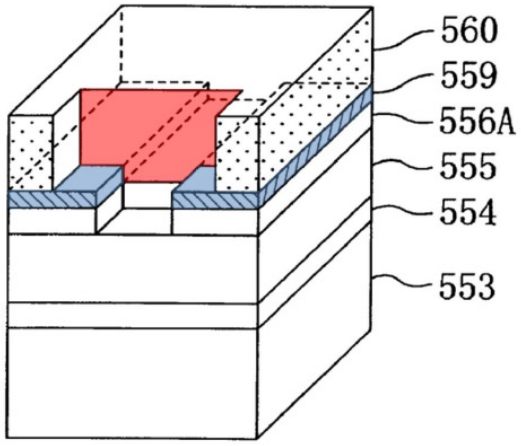
***Grill*, FIG. 5D** ***Grill*, FIG. 5D (modified for *Grill-Aoyama*)**

IPB further errs by suggesting the step height caused by layer 58 in the figure to the right above "would have created problems for dimensional control" because of allegedly "widely varied exposure requirements" between the thicker resist inside the wiring groove and the thinner resist in other areas. Paper 19, 72; *see also* EX1049, ¶¶73-74. IPB's argument is baseless because hard mask layer 58 in FIG. 5D above is only about 20 nm to 50 nm thick (*see* EX1005, 8:24-31), and photoresist layer 62 would have been about 1000 to 2000 nm thick, making the thickness variation about 1-5%. EX1049, ¶73. The example IPB identifies (EX1005, 5:28-33, Fig. 2A), on the other hand, involves an interlevel dielectric layer about 300 to 1000 nm thick (EX1010, 6:58-60; EX1043, 3:8-9), making the thickness variation about 15-50%. EX1049, ¶73. Comparing these two situations is inappropriate. *Id.*, ¶¶73-74.

Accommodating such a small step in the *Grill-Aoyama* combination would not have been problematic, as the '696 patent confirms. In the Modified Example

of Embodiment 5, photoresist 560 includes a 50 nm photoresist step due to layer 559, but it describes no photolithography or exposure requirements for patterning layer 560 with via patterns wider than the wiring groove. EX1001, 25:9-11, 25:26-36, Fig. 27(b) (below with highlights). This suggests a POSITA would not have viewed this small step as an obstacle. *See* EX1049, ¶¶73-74.

Fig. 27 (b)



IPB provides no credible reason a POSITA would have been dissuaded from combining *Aoyama*'s self-aligned via method with *Grill*'s dual damascene process. *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994) (explaining that a "teaching away" requires a POSITA to be discouraged from pursuing this solution); *see also* EX1049, ¶¶69-74.

III. CONCLUSION

Because its theories regarding priority are legally and factually flawed, IPB cannot remove *Grill* as prior art. And because a POSITA would have been

motivated to combine *Grill* and *Aoyama* (a combination that discloses all features of the challenged claims) with a reasonable expectation of success, TSMC asks the Board to find the challenged claims unpatentable.

IV. CERTIFICATION UNDER 37 C.F.R. §42.24(d)

This Petition complies with 37 C.F.R. §42.24. As calculated by the "Word Count" feature of Microsoft Word 2010, it contains 5,097 words, excluding the words contained in the following: Table of Contents, Table of Authorities, List of Exhibits, this Certification Under §42.24(d), and the Certificate of Service.

Dated: July 21, 2017

Respectfully submitted,

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Lead Counsel for Petitioner

IPR2016-01376
Patent 6,197,696 B1

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I served a true and correct copy of the **PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE** by electronic mail, on this 21st day of July, 2017, on counsel of record for the Patent Owner as follows:

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