Petitioner's Demonstratives

Taiwan Semiconductor Manufacturing Co.

v.

Godo Kaisha IP Bridge 1

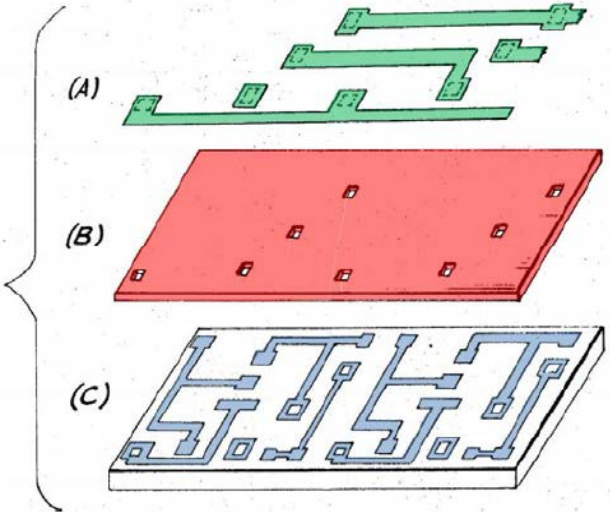
Case Nos. IPR2016-01376, -01377, -01378, -01379

U.S. Patent No. 6,197,696

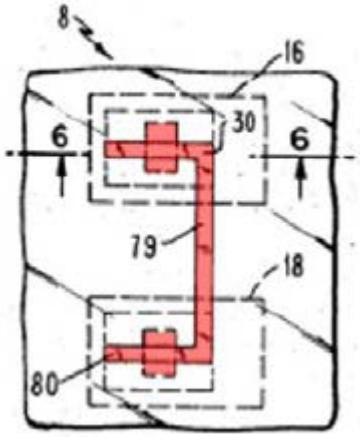
BACKGROUND

Interconnection Technology

- **Wiring Levels Have Wiring Patterns (i.e., Trenches) (A, C)**
- **Via Layers Have Contact Holes (i.e., Vias) (B)**



IPR2016-01376, EX1003, FIG. 6

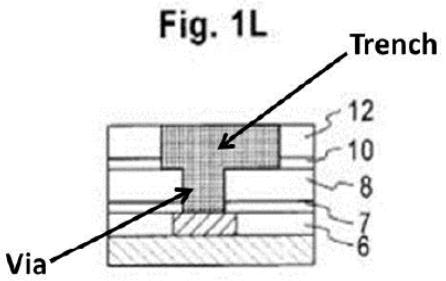


IPR2016-01376, EX1005, FIG. 6A

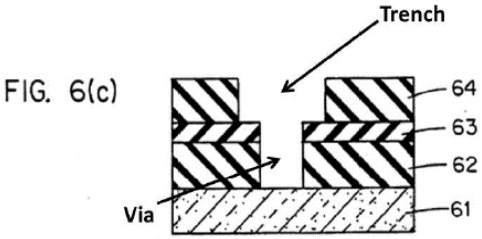
IPR2016-01376, Paper 2, at 2–3; IPR2016-01377, Paper 2, at 2–3; IPR2016-01378, Paper 2, at 2–3; IPR2016-01379, Paper 2, at 2–3.

Dual Damascene Technology

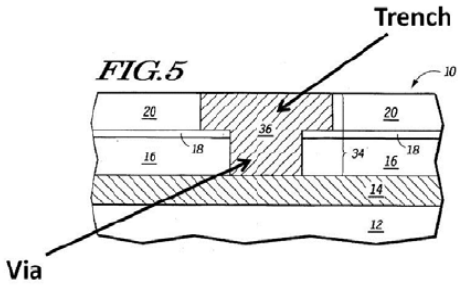
- **Dual Damascene Processes Allow Vias and Trenches to be Made in Same Module**



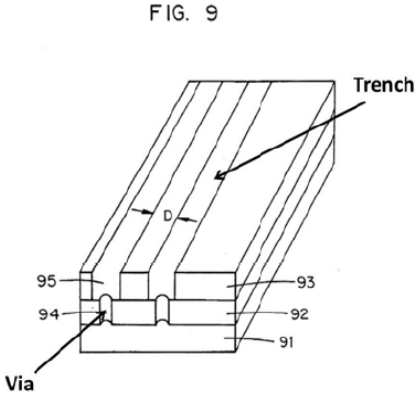
IPR2016-01376, EX1005, FIG. 1L



IPR2016-01376, EX1006, FIG. 6(c)



IPR2016-01376, EX1007, FIG. 5

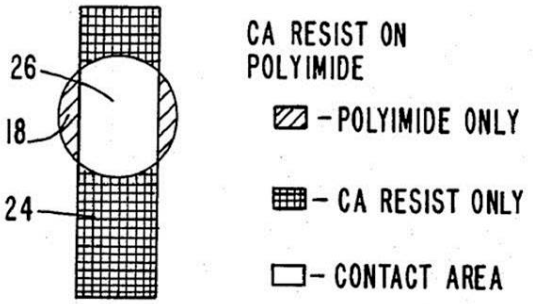


IPR2016-01376, EX1006, FIG. 9

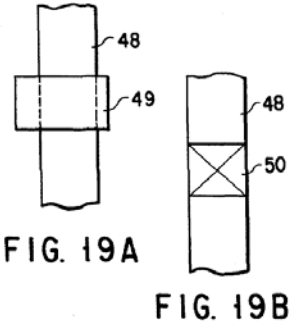
IPR2016-01376, Paper 2, at 4; IPR2016-01377, Paper 2, at 4; IPR2016-01378, Paper 2, at 4; IPR2016-01379, Paper 2, at 4.

Self-Aligned Contact Holes

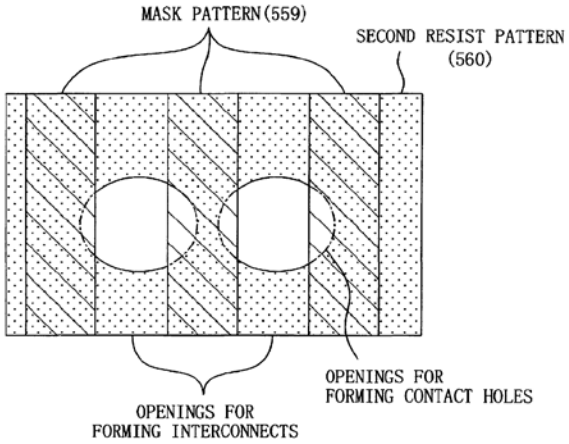
- **Resist Pattern Ensures Via Openings are the Designed Width**



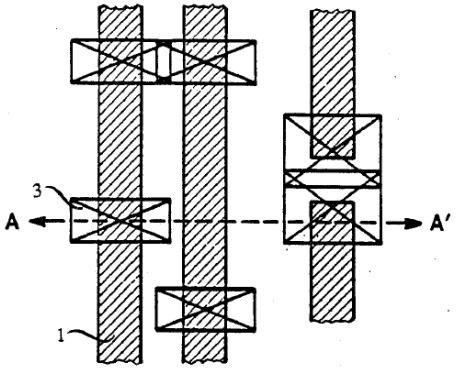
IPR2016-01376, EX1040, FIG. 6



IPR2016-01376, EX1018, FIGS. 19A, 19B



IPR2016-01376, EX1001, FIG. 36



IPR2016-01376, EX1039, FIG. 1

See, e.g., IPR2016-01376, Paper 2, at 35–36, 54–55, 70–74; IPR2016-01376, EX1001, at FIG. 36; IPR2016-01376, EX1018, at FIGS. 19A, 19B IPR2016-01376, EX1039, at FIG. 1; IPR2016-01376, EX1040, at FIG. 6.

References and Instituted Grounds

REFERENCES

Inventor	Application Date	Publication No.
Grill et al.	July 30, 1998*	U.S. Patent No. 6,140,226
Aoyama et al.	October 28, 1994	U.S. Patent No. 5,592,024
Weztel et al.	August 29, 1997	U.S. Patent No. 5,920,790

***Grill claims priority to the filing date of U.S. Patent Application Ser. No. 60/071,628, filed on January 16, 1998.**

GROUNDS

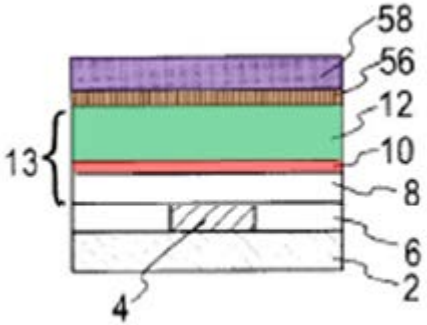
IPR Number	Prior Art	Claims
IPR2016-01376	Grill, Aoyama	13 and 15
IPR2016-01377	Grill, Aoyama	10–12
IPR2016-01378	Grill, Aoyama	13 and 14
IPR2016-01379	Grill, Aoyama, Wetzel	10 and 12

Institution Decisions, IPR2016-01376, Paper 11, at 43; IPR2016-01377, Paper 11, at 44; IPR2016-01378, Paper 11, at 44; IPR2016-01379, Paper 11, at 45.

Structure of the Petitions

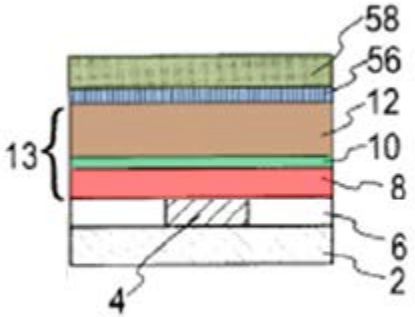
Different Layer Mappings + Different Claim Sets

Fig. 5A



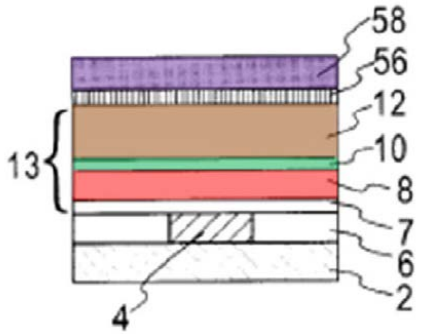
Claims 13 and 15 (No Optional Layer 7)

Fig. 5A



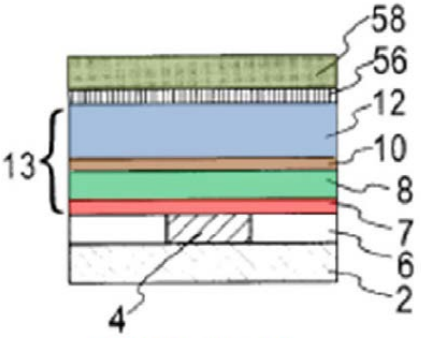
Claims 10–12 (No Optional Layer 7)

Fig. 5A



Claims 13 and 14

Fig. 5A



Claims 10 and 12

See, e.g., Petitions, IPR2016-01376, Paper 2, at 75; IPR2016-01377, Paper 2, at 83; IPR2016-01378, Paper 2, at 68; IPR2016-01379, Paper 2, at 81.

Uncontested Issues

- **Claim Construction**
  - The parties do not dispute the language of the Board's construction, only its application
- **Disclosure of Claim Limitations**
  - IPB does not dispute the proposed combinations satisfy all limitations of the challenged claims
- **Wetzel**
  - IPB raises no issue about Wetzel
- **Dependent Claims**
  - Patent Owner did not argue that any dependent claim is entitled to an earlier priority date
- **Level of Ordinary Skill in the Art**
  - Patent Owner does not contest Petitioner's definition

See generally, e.g., Petition, IPR2016-01376, Paper 2; Patent Owner's Response, IPR2016-01376, Paper 19; Reply, IPR2016-01376, Paper26.

Contested Issues

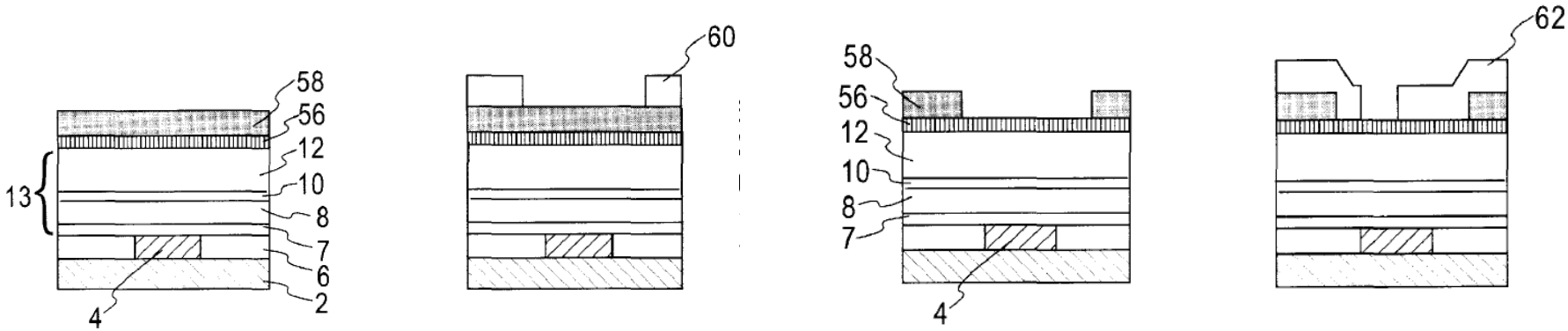
- **Priority of Challenged Claims**
  - Whether the claims of the ’696 patent are entitled to the benefit of the Japanese ’371 application
  - Whether the effective date for Grill under 35 U.S.C. §102(e) (pre-AIA) is the date of its provisional ’628 application
- **Motivation to Combine**
  - Whether there is sufficient motivation to combine Grill and Aoyama

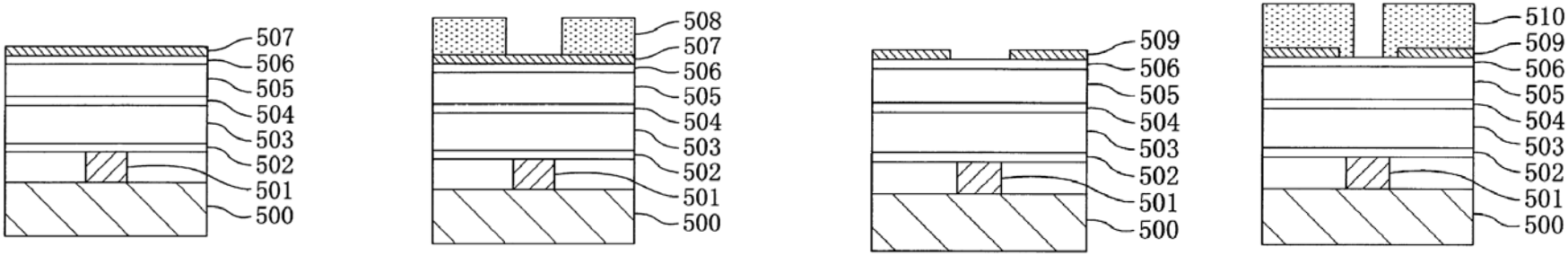
See generally, e.g., Petition, IPR2016-01376, Paper 2; Patent Owner’s Response, IPR2016-01376, Paper 19; Reply, IPR2016-01376, Paper26.

OBVIOUSNESS

Grill Is Almost Identical to Embodiment 5 of the ’696 Patent

Grill



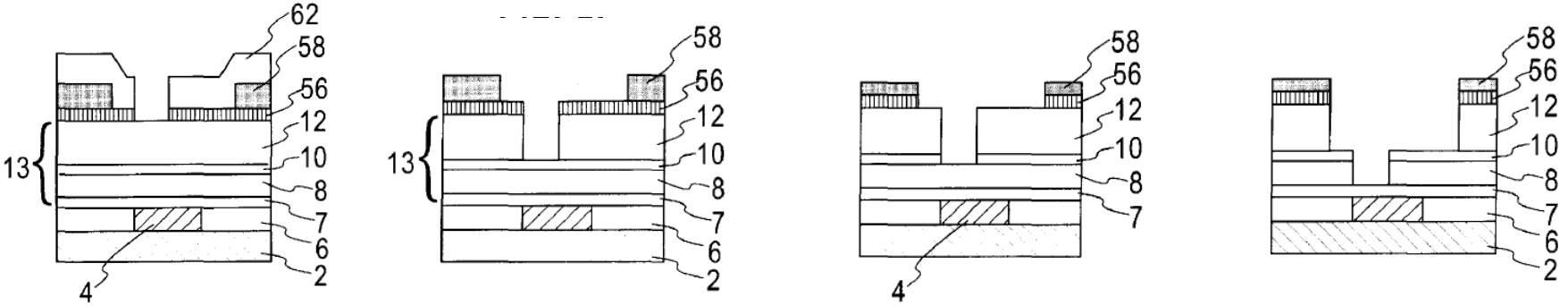


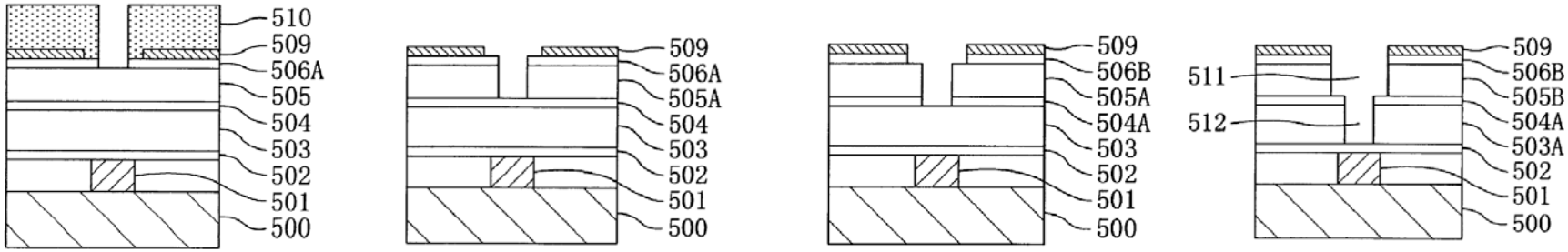
’696 Patent

See, e.g., IPR2016-01376, EX1001, at FIGS. 21(a)–22(b); IPR2016-01377, EX1005, at FIGS. 5A–5D.

Grill Is Almost Identical to Embodiment 5 of the ’696 Patent

Grill



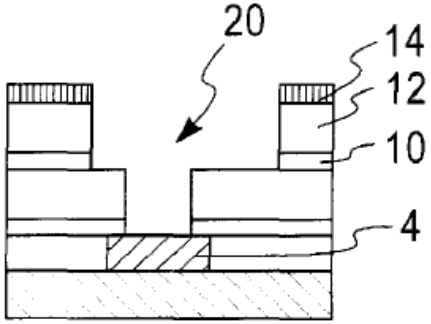


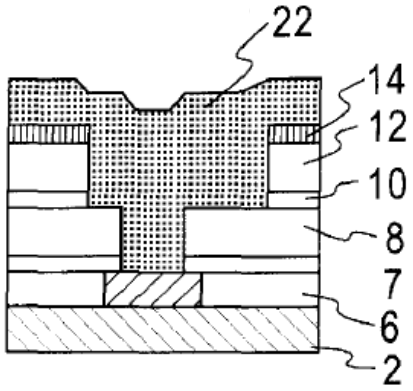
’696 Patent

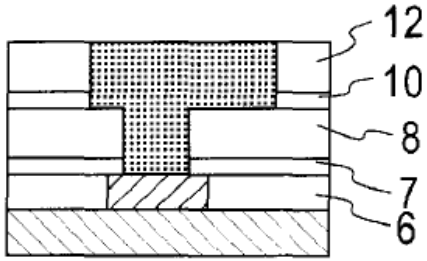
See, e.g., IPR2016-01376, EX1001, at FIGS. 22(c)–23(c); IPR2016-01377, EX1005, at FIGS. 5E–5H.

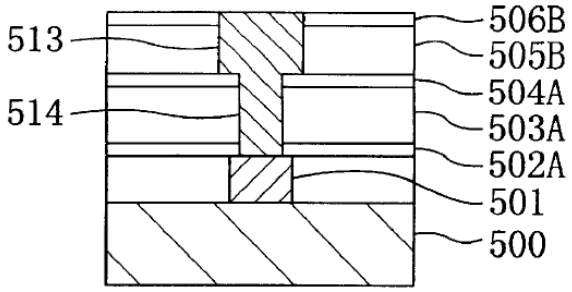
Grill Is Almost Identical to Embodiment 5

Grill









’696 Patent

See, e.g., IPR2016-01376, EX1001, at FIGS. 23(d); IPR2016-01377, EX1005, at FIGS. 1J–1L.

Aoyama Addresses the Same Problem as the '696 Patent

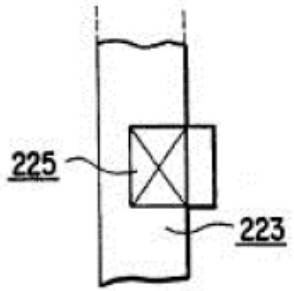


FIG. 5D PRIOR ART

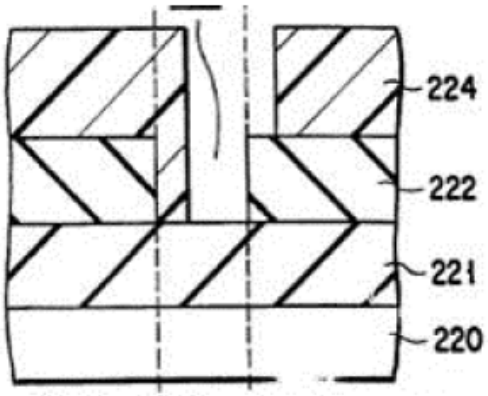
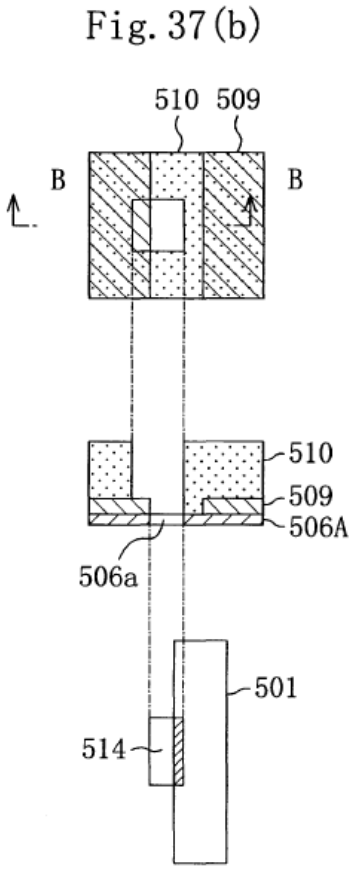


FIG. 5B PRIOR ART

Aoyama, FIGS. 5B, 5D



'696 Patent, Fig. 37(b)

See, e.g., Petitions, IPR2016-01376, Paper 2, at 73; IPR2016-01377, Paper 2, at 76; IPR2016-01378, Paper 2, at 47; IPR2016-01379, Paper 2, at 78.

Aoyama Provides the Same Solution as ’696 Patent

Aoyama, FIGS. 18B, 19A

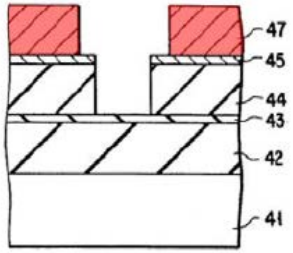


FIG. 18B

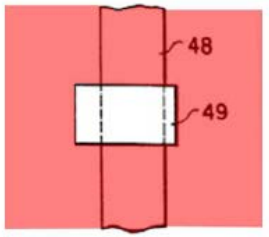


FIG. 19A

’696 Patent, Figs. 25(c), 37(b)

Fig. 25(c)

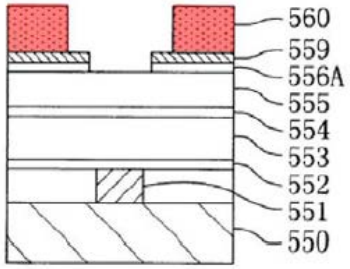
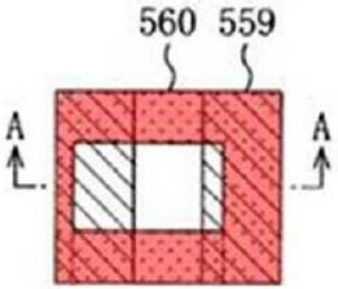


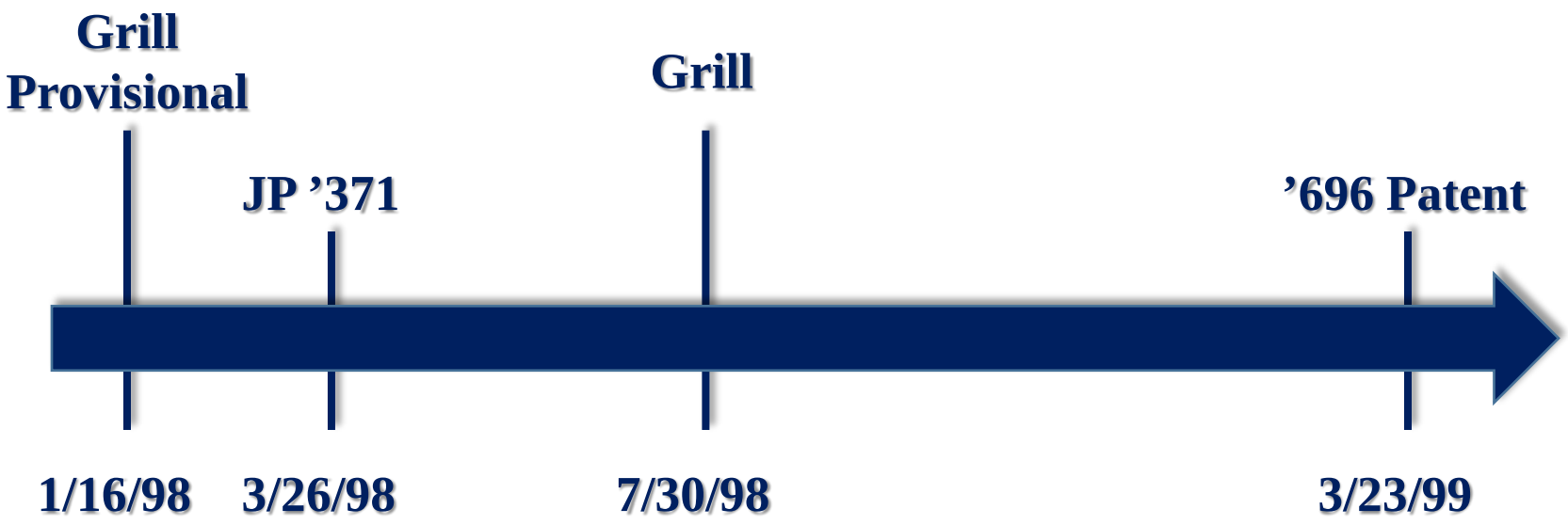
Fig. 37(a)



See, e.g., Petitions, IPR2016-01376, Paper 2, at 74; IPR2016-01377, Paper 2, at 77; IPR2016-01378, Paper 2, at 48; IPR2016-01379, Paper 2, at 79.

PRIORITY

Priority Timeline



See, e.g., IPR2016-01376, Paper 2, at 19–20, 28; IPR2016-01376, EX1001, at 1 (fields 22 and 30); IPR2016-01376, EX1005, at 1 (fields 22 and 60).

The Burdens for Proving Priority Are Clear

- Once Petitioner shows a reference is prior art, the burden of production shifts to Patent Owner to show the challenged claims benefit from earlier priority
  - ***Tech. Licensing Corp. v. VideoTek, Inc.***, 545 F.3d 1316, 1327–28 (Fed. Cir. 2008)

Here, TLC, the plaintiff in the suit, has the initial burden of going forward with evidence to support its allegation that Gennum infringes claim 33. Gennum, having the ultimate burden of proving its defense of invalidity based on anticipating prior art, then has the burden of going forward with evidence that there is such anticipating prior art, which in Gennum's view means art that is prior to the 1995 application date of the #250 patent. *See Ralston*, 772 F.2d at 1573.

At that point TLC has the burden of going forward with evidence either that the prior art does not actually anticipate, or, as was attempted in this case, that it is not prior art because the asserted claim is entitled to the benefit of a filing date prior to the alleged prior art. *See id.* This requires TLC to show not only the existence of the earlier application, but why the written description in the earlier application supports the claim. In the context of the allegedly anticipating Elantec prior art, that means producing sufficient evidence and argument to show that an ancestor to the #250 patent, with a filing date prior to the Elantec date, contains a written description that supports all the limitations of claim 33, the claim being asserted.

***1328** Assuming then that TLC's evidence and argument in support of the earlier filing date is now before the court, the burden of going forward again shifts to the proponent of the invalidity defense, Gennum, to convince the court that TLC is not entitled to the benefit of the earlier filing date. "Convince" is the operative word, because if the court is not persuaded by clear and convincing evidence that Gennum is correct, Gennum has failed to carry its ultimate burden of persuasion, and its defense of invalidity, based on anticipation by the Elantec art, fails.

See, e.g., IPR2016-01376, Paper 9, at 1–3; IPR2016-01376, Paper 26, at 2–3.

The Burdens for Proving Priority Are Clear

- Once Petitioner shows a reference is prior art, the burden of production shifts to Patent Owner to show the challenged claims benefit from earlier priority
  - ***Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.***, 800 F.3d 1375, 1379–80 (Fed. Cir. 2015)

> **4 In this case, Dynamic, as the petitioner, had the burden of persuasion to prove unpatentability by a preponderance of the evidence, and this burden never shifted. Dynamic also had the initial burden of production, and it satisfied that burden by arguing that Raymond anticipated the asserted claims of the #196 patent under § 102(e)(2).
>
> *1380 The burden of production then shifted to National Graphics to argue or produce evidence that either Raymond does not actually anticipate, or, as was argued in this case, that Raymond is not prior art because the asserted claims in the #196 patent are entitled to the benefit of a filing date (constructive or otherwise) prior to the filing date of Raymond. National Graphics produced evidence that the invention claimed in the #196 patent was reduced to practice prior to the filing date of Raymond, and thus contended that the asserted claims were entitled to a date of invention prior to that of the Raymond patent.

See, e.g., IPR2016-01376, Paper 2, at 28–29 n.3; IPR2016-01376, Paper 9, at 1–3; IPR2016-01376, Paper 26, at 2–3.

The Burdens for Proving Priority Are Clear

- Once Petitioner shows a reference is prior art, the burden of production shifts to Patent Owner to show the challenged claims benefit from earlier priority.
  - ***Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.***, 800 F.3d 1375, 1379–80 (Fed. Cir. 2015)

> As a result, the burden of production returned to Dynamic to prove that either the invention was not actually reduced to practice as argued, or that the Raymond prior art was entitled to the benefit of a filing date prior to the date of National Graphics' reduction to practice. As the Board found, however, Dynamic failed to carry its burden of proving that Raymond's effective date was earlier than the date that the invention claimed in the #196 patent was reduced to practice. The burden of production was on Dynamic to prove that, under § 119(e)(1), Raymond was entitled to the benefit of the filing date of its provisional application, and it failed to do that.
>
> In contrast, Dynamic's proffered approach would create a presumption that a patent is entitled to the benefit of the filing date of its provisional precursor, but that would be unsound because the PTO does not examine provisional applications as a matter of course; such a presumption is therefore not justified. The PTO's Manual of Patent Examining Procedure ("MPEP"), which is "commonly relied upon as a guide to patent attorneys and patent examiners on procedural matters," *Litton Sys., Inc. v. Whirlpool Corp.*, 728 F.2d 1423, 1439 (Fed.Cir.1984), explains this:

See, e.g., IPR2016-01376, Paper 2, at 28–29 n.3; IPR2016-01376, Paper 9, at 1–3; IPR2016-01376, Paper 26, at 2–3.

Identifying a Priority Document Does Not Shift Burdens

- ***Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.***, 800 F.3d 1375, 1379 (Fed. Cir. 2015)

These burdens are illustrated in *Technology Licensing*, where the patentee, TLC, sued Gennum for infringement, and Gennum argued that TLC's patent was anticipated by certain prior art. *Id.* At issue was whether the asserted patent was entitled to the benefit of the priority date of a related nonprovisional application. *Id.* TLC argued that the asserted claim was entitled under 35 U.S.C. § 120 to the benefit of the earlier filing date of its parent nonprovisional application. *Id.* Section 120, which has language similar to that found in § 119(e)(1), provides that a patent application for an "invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States ... *shall have the same effect, as to such invention, as though filed on the date of the prior application*...." (emphasis added).

Gennum, having the ultimate burden of proving its defense of invalidity based on anticipating prior art, also had the initial "burden of going forward with evidence that there is such anticipating prior art." *Tech. Licensing*, 545 F.3d at 1327. In response, TLC then had "the burden of going forward with evidence either that the prior art does not actually anticipate, or, as [TLC] attempted in this case, that it is not prior art because the asserted claim is entitled to the benefit of a filing date prior to the alleged prior art." *Id.* We noted that "[t]his requires TLC to show not only the existence of the earlier application, but why the written description in the earlier application supports the claim." *Id.* We concluded that once "TLC's evidence and argument in support of the earlier filing date is ... before the court, the burden of going forward again shifts to the proponent of the invalidity defense, Gennum, to convince the court that TLC is not entitled to the benefit of the earlier filing date." *Id.* at 1328.

See, e.g., IPR2016-01376, Paper 9, at 1–3; IPR2016-01376, Paper 26, at 2–3.

The Board Follows the Same Law

- ***Core Survival, Inc. v. S&S Precision, LLC***, PGR2015-00022, Paper 8, 8 (P.T.A.B. Feb. 19, 2016)

> We do not agree with Patent Owner that Petitioner has the initial burden of showing that the '292 patent is not entitled to an earlier priority date for unpatentability purposes. As explained in a number of cases, although the patent challenger has the ultimate burden of persuasion, a patentee must demonstrate entitlement to a priority date when the patentee relies on that priority date to overcome an anticipation or obviousness argument. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1379–80 (Fed. Cir. 2015) (discussing burdens in *inter partes* review to show entitlement to provisional filing dates and relying on infringement cases involving continuation-in-part applications); *In re NTP, Inc.*, 654 F.3d 1268, 1276 (Fed. Cir. 2011) (noting "a patent's claims are not entitled to an earlier priority date because the patentee claims priority . . . [r]ather, for a patent's claims to be entitled to an earlier priority date, the patentee must demonstrate that the claims meet the requirements of 35 U.S.C. § 120"); *Research Corp. Techs., Inc. v. Microsoft Corp.*, 627 F.3d 859, 870–71 (Fed. Cir. 2010); *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1327–29 (Fed. Cir. 2008); *PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1305–06 (Fed. Cir. 2008). As the Federal Circuit explained most recently in

See, e.g., IPR2016-01376, Paper 2, at 28–29 n.3; IPR2016-01376, Paper 9, at 1–3; IPR2016-01376, Paper 26, at 2–3.

The Board Follows the Same Law

- ***Core Survival, Inc. v. S&S Precision, LLC***, PGR2015-00022, Paper 8, 8 (P.T.A.B. Feb. 19, 2016)

> 1379. Contrary to Patent Owner's position, the only showing Petitioner needed to make is that "the art must have existed as of the date of invention, presumed to be the filing date of the application until an earlier date is proved." *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 796 F.2d

See, e.g., IPR2016-01376, Paper 2, at 28–29 n.3; IPR2016-01376, Paper 9, at 1–3; IPR2016-01376, Paper 26, at 2–3.

The Board Follows the Same Law

- ***Core Survival, Inc. v. S&S Precision, LLC***, PGR2015-00022, Paper 8, 9 (P.T.A.B. Feb. 19, 2016)

> Patent Owner's reliance on *Polaris Wireless, Inc. v. TruePosition, Inc.*, Case IPR2013-00323, slip op. at 29 (PTAB Nov. 15, 2013) (Paper 9), is misplaced. As an initial matter, Patent Owner fails to direct us to, and we do not discern independently, any support in *Polaris Wireless* for the proposition that a Petitioner has any initial burden to contest entitlement to a provisional filing date. In contrast, the law is clear that there is no initial burden on Petitioner to rebut a provisional date. *See Dynamic Drinkware*, 800 F.3d at 1379–80. Thus, Patent Owner's contention that Petitioner has

See, e.g., IPR2016-01376, Paper 2, at 28–29 n.3; IPR2016-01376, Paper 9, at 1–3; IPR2016-01376, Paper 26, at 2–3.

The Board Follows the Same Law

- ***Core Survival, Inc. v. S&S Precision, LLC***, PGR2015-00022, Paper 8, 9 & n.3 (P.T.A.B. Feb. 19, 2016)

present Petition. As *Dynamic Drinkware* makes clear, the initial burden of production for showing an earlier priority date rests with the patent owner, not the petitioner. *See Dynamic Drinkware*, 800 F.3d at 1379–80.[3]

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[3] To be sure, the suggestions in *Polaris Wireless* about what the Petition should contain in this regard represent the best practice for a petitioner. Although the patent owner initially bears the burden of production on the issue of priority, there is generally no opportunity for a petitioner to submit additional evidence or argument at the institution stage. Thus, if the patent owner meets its burden and the petition contains nothing to rebut preemptively patent owner's evidence supporting a priority claim, the petitioner's case is in peril. However, we are not confronted by that situation here because Patent Owner in this case has produced no evidence or argument to support any claim to the earlier priority dates. Also, we note

See, e.g., IPR2016-01376, Paper 2, at 28–29 n.3; IPR2016-01376, Paper 9, at 1–3; IPR2016-01376, Paper 26, at 2–3.

The Challenged Claims are Not Entitled to Claim Priority to the Japanese ’371 Application

The Disclosure in Japanese ’371 Does Not Support Claims 10 or 13

Board's Claim Construction of "Using . . . as a Mask"

Institution Decision

Based on the above, and for purposes of this Decision, we construe "using the [designated layer] as a mask" as proposed by Patent Owner: "using the [designated layer] to define areas for etching."[5] For purposes of this Decision, and based on the record now before us, however, we need to discuss further the metes and bounds of this phrase.

See, e.g., IPR2016-01376, Paper 11, at 15.

Board's Claim Construction of "Using . . . as a Mask"

Institution Decision

We, therefore, are not persuaded that a layer, positioned between an overlying layer and the layer being etched and having an edge in line and flush with an edge of the overlying layer, is "used as a mask" within the meaning of claim 13. Instead, to be "used as a mask," the between layer would need to define an additional portion of the layer being etched that is to be shielded from etching.[7] An example of this is described above with respect to Figures 25(c) and 27(b) of the '696 patent.

* * *

[7] Our construction does not preclude, for example, a layer positioned between an overlying layer and the layer being etched from acting as a mask, within the meaning of claim 13, in an instance where the overlying layer also is removed during the etching, and thus, the between layer acts to shield the layer being etched during etching.

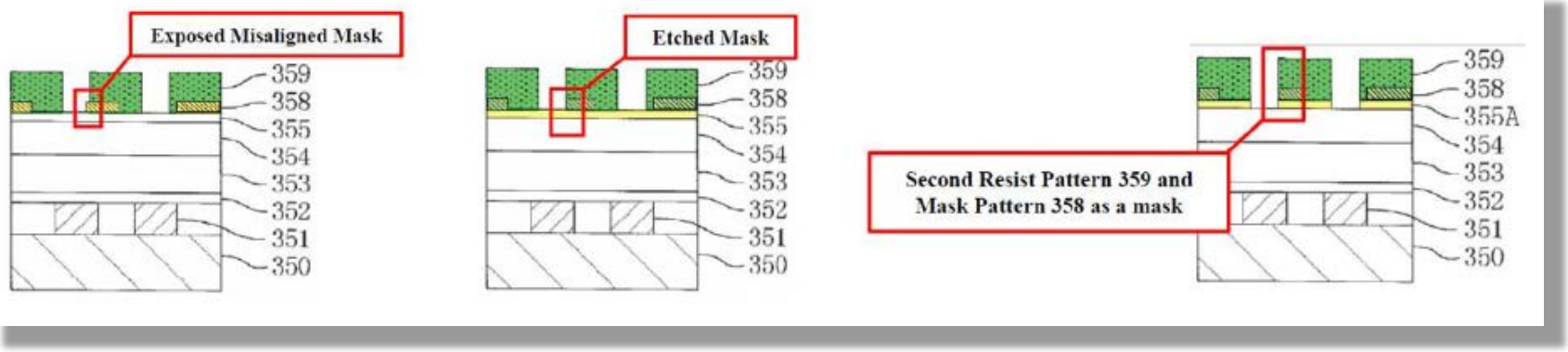
See, e.g., IPR2016-01376, Paper 11, at 18 & n.7.

Patent Owner's Argument Has No Support: Steps 10(i) and 13(h)

- **Japanese '371 teaches etching the intermediate layer to prevent it from acting as a mask**

[0096]
If there is a concern that the second resist pattern 359 has been misaligned with the first resist pattern 357, then the mask pattern 358 should be dry-etched using the second resist pattern 359 as a mask before the second silicon dioxide film 355 is dry-etched using the second resist pattern 359 as a mask. That is to say, if the mask pattern 358 is exposed to the openings of the second resist pattern 359 for the formation of contact holes because of the misalignment of the second resist pattern 359 with the first resist pattern 357, then the mask pattern 358 is dry-etched using the second resist pattern 359 as a mask. In this manner, the openings of the mask pattern 358 are expanded to include the openings for the formation of wiring grooves and contact holes.

JP '371 Application, ¶0096

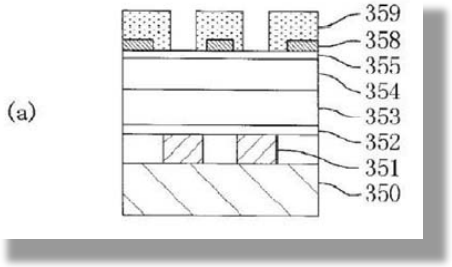


IPR2016-01376, Paper 26, at 10

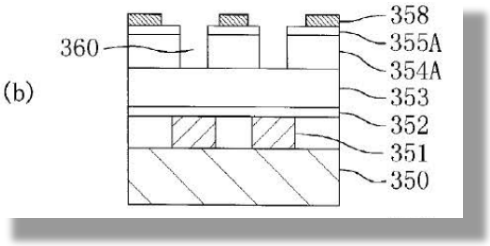
See, e.g., IPR2016-01376, Paper 26 at 10; IPR2016-01376, EX1014 at ¶0096; IPR2016-01376, Paper 19, at 24–26; IPR2016-01376, EX2012 at 35:12–23.

JP '371 Teaches To *Avoid* Using the Intermediate Layer As a Mask

- **The process is intended to proceed in this manner:**

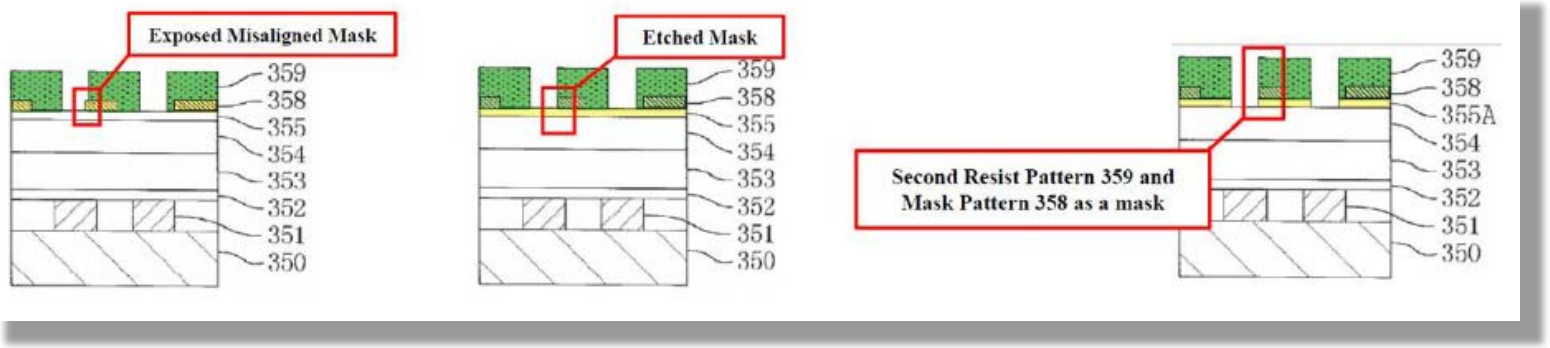


IPR2016-01376, EX1014, at FIG. 16(a)



IPR2016-01376, EX1014, at FIG. 16(b)

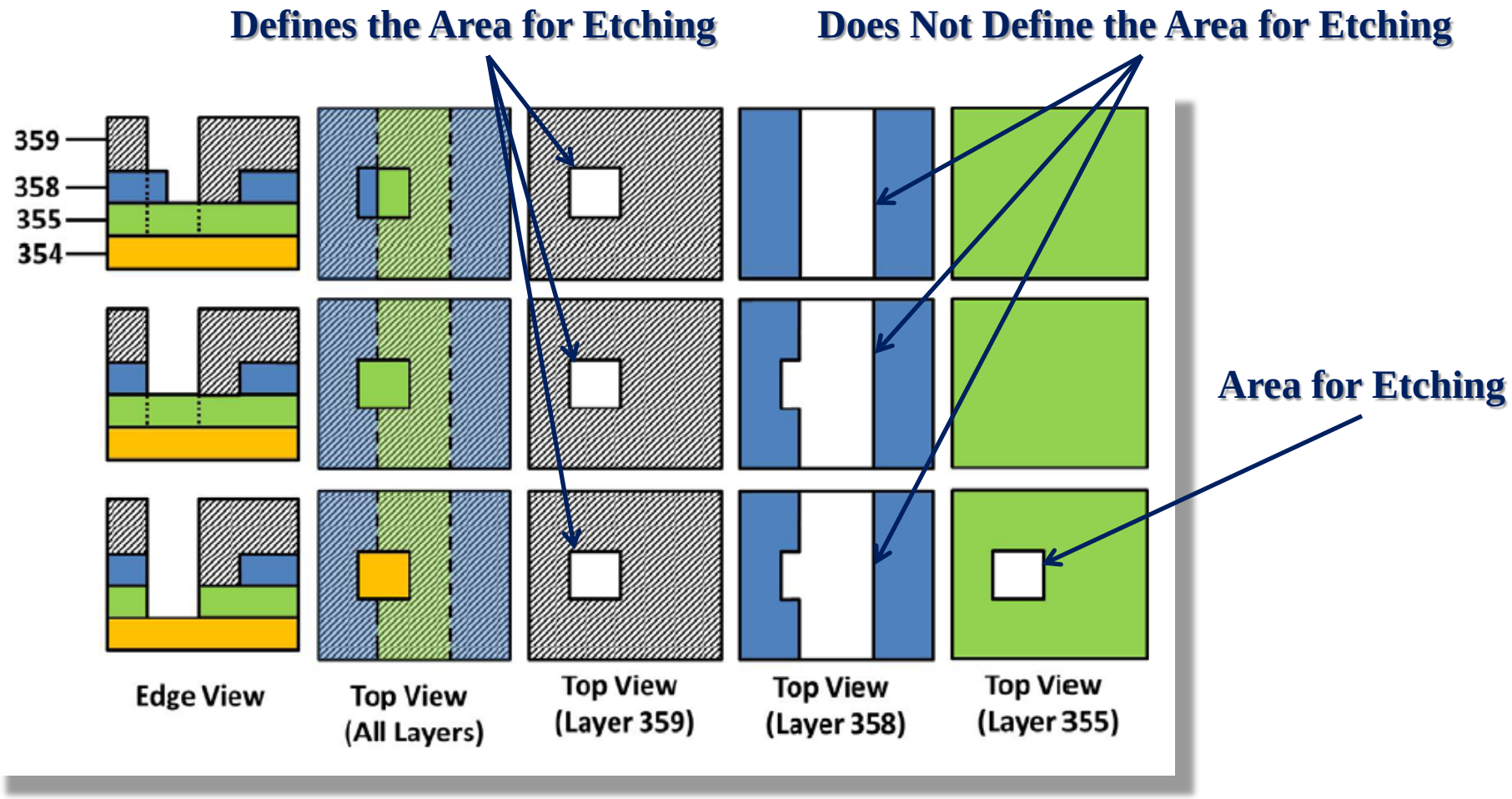
- **When there is misalignment that may expose layer 358, the patent says to remove the exposed part of layer 358:**



IPR2016-01376, Paper 19, at 24–26

See, e.g., IPR2016-01376, *EX1014, at ¶0093, FIGS. 16(a), 16(b);* IPR2016-01376, *EX2012, at 34:10–19, FIGS. 16(a), 16(b);* IPR2016-01376, *Paper 19, at 24–26;* IPR2016-01376, *Paper 26, at 10.*

The Correction Prevents Layer 358 from Acting as a Mask



IPR2016-01376, Paper 26, at 12

See, e.g., IPR2016-01376, *Paper 26, at 10–12; IPR2016-01376, EX1049, at ¶¶29–33.*

JP '371 Says Only That Layer 359 Is a Mask For Etching Layer 355

[0093]
Subsequently, as shown in Figure 16(a), the first resist pattern 357 is removed and then a second resist pattern 359 having openings for the formation of contact holes is formed on the second silicon dioxide film 355. Then, the second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask, thereby forming a patterned second silicon dioxide film 355A and a patterned organic film 354A having openings 360 for the formation of contact holes as shown in Figure 16(b). In this case, the second resist pattern 359 is removed during the step of etching the organic film 354.

JP '371 Application, ¶0093

[0096]
If there is a concern that the second resist pattern 359 has been misaligned with the first resist pattern 357, then the mask pattern 358 should be dry-etched using the second resist pattern 359 as a mask before the second silicon dioxide film 355 is dry-etched using the second resist pattern 359 as a mask. That is to say, if the mask pattern 358 is exposed to the openings of the second resist pattern 359 for the formation of contact holes because of the misalignment of the second resist pattern 359 with the first resist pattern 357, then the mask pattern 358 is dry-etched using the second resist pattern 359 as a mask. In this manner, the openings of the mask pattern 358 are expanded to include the openings for the formation of wiring grooves and contact holes.

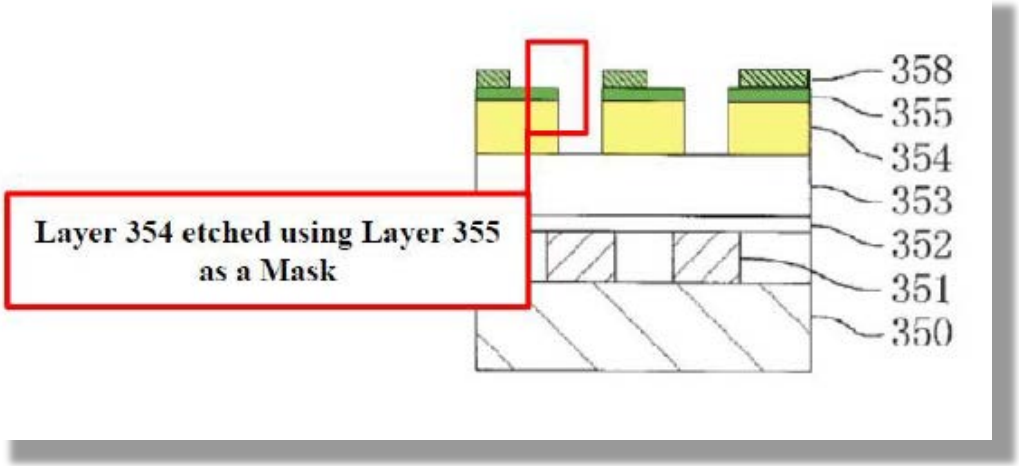
JP '371 Application, ¶0096

See, e.g., IPR2016-01376, *EX1014, at ¶¶0093, 0096;* IPR2016-01376, *EX2012, at 34:10–19, 34:10–19, 35:12–23.*

Patent Owner's Argument Has No Support: Steps 10(j) and 13(i)

[0096]
If there is a concern that the second resist pattern 359 has been misaligned with the first resist pattern 357, then the mask pattern 358 should be dry-etched using the second resist pattern 359 as a mask before the second silicon dioxide film 355 is dry-etched using the second resist pattern 359 as a mask. That is to say, if the mask pattern 358 is exposed to the openings of the second resist pattern 359 for the formation of contact holes because of the misalignment of the second resist pattern 359 with the first resist pattern 357, then the mask pattern 358 is dry-etched using the second resist pattern 359 as a mask. In this manner, the openings of the mask pattern 358 are expanded to include the openings for the formation of wiring grooves and contact holes.

JP '371 Application, ¶0096



IPR2016-01376, Paper 26, at 12

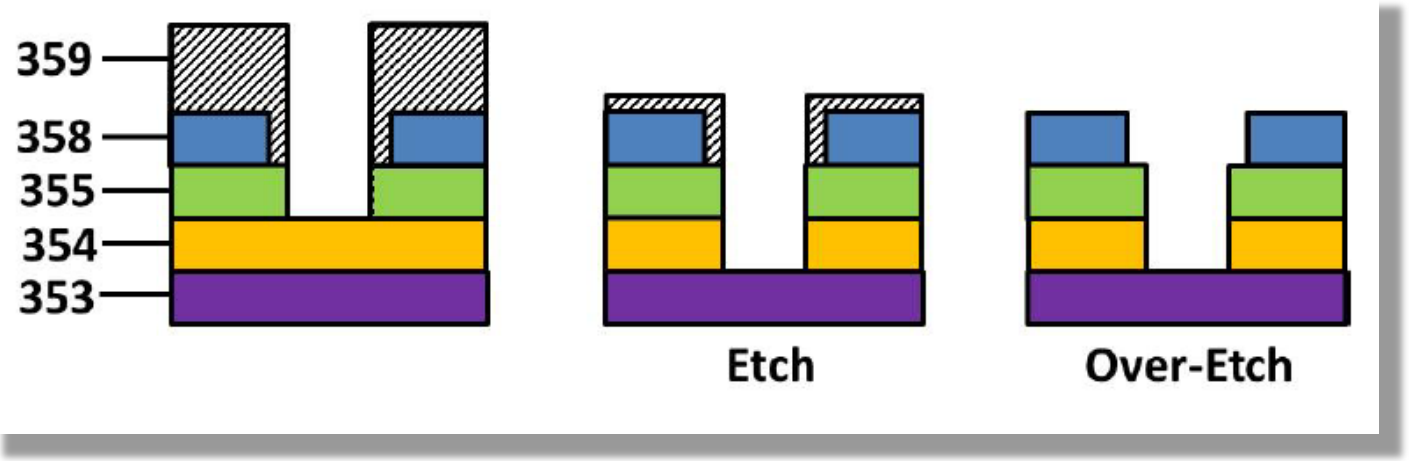
See, e.g., IPR2016-01376, Paper 26 at 12; IPR2016-01376, EX1014 at ¶0096; IPR2016-01376, Paper 19, at 27–28; IPR2016-01376, EX2012 at 35:12–23.

The JP ’371 Application Describes Overetch

Only layer 359 is identified as the mask for etching layer 354.

[0093]
Subsequently, as shown in Figure 16(a), the first resist pattern 357 is removed and then a second resist pattern 359 having openings for the formation of contact holes is formed on the second silicon dioxide film 355. Then, the second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask, thereby forming a patterned second silicon dioxide film 355A and a patterned organic film 354A having openings 360 for the formation of contact holes as shown in Figure 16(b). In this case, the second resist pattern 359 is removed during the step of etching the organic film 354.

JP ’371 Application, ¶0093



IPR2016-01376, Paper 26, at 13

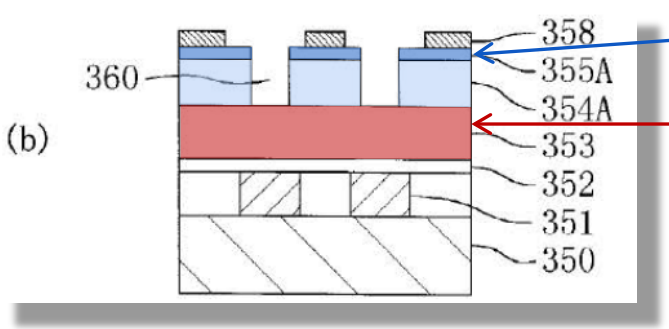
See, e.g., IPR2016-01376, Paper 26 at 13; IPR2016-01376, EX1014 at ¶0093; IPR2016-01376, EX2012 at 34:10–19; IPR2016-01376, EX1049, at ¶36.

Only One Layer Is Named As a Mask, Not Two Layers

- **<u>Example:</u> In this example, layers 354A and 355A are both identified as masks for etching layer 353 because layer 355A is completely removed before layer 353 is patterned, making layer 354A a mask.**

[0094]
Next, as shown in Figure 16(c), the first silicon dioxide film 353 is dry-etched using the patterned second silicon dioxide film 355A and the patterned organic film 354A as masks, thereby forming a patterned first silicon dioxide film 353A having contact holes 361. In this etching process step, the mask pattern 358 is transferred to the patterned second silicon dioxide film 355A. Accordingly, openings for the formation of wiring grooves are formed in the patterned second silicon dioxide film 355A.

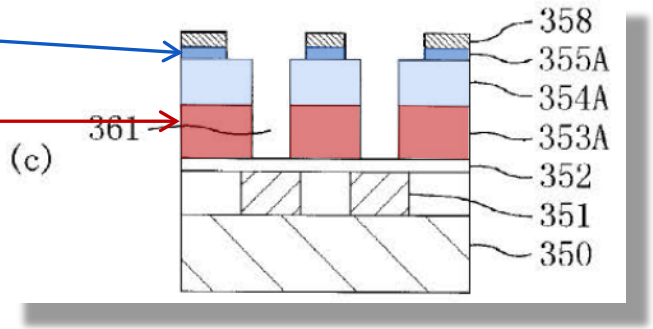
JP '371 Application, ¶0094



JP '371 Application, Fig. 16(b)

50 nm SiO_2

1,000 nm SiO_2



JP '371 Application, Fig. 16(c)

See, e.g., IPR2016-01376, Paper 26, at 13; IPR2016-01376, EX1014 at ¶¶0090, 0093, 0094; IPR2016-01376, EX2012 at 33:20–21, 33:23–24, 34:10–27; IPR2016-01376, EX1049, at ¶36; IPR2016-01376, Paper 35, at 2–3; IPR2016-01376, EX2040, at 57:22–60:3.

Embodiments of the ’696 Patent

- The ’696 patent contains the following:
  - **First Embodiment** (EX1001 at 10:23–14:56, FIGS. 1(a)–8(c))
  - **Second Embodiment** (EX1001 at 14:57–16:38, FIGS. 9(a)–11(c))
  - **Third Embodiment** (EX1001 at 16:40–18:58, FIGS. 12(a)–14(c))
  - **Modified Example of Third Embodiment** (EX1001 at 18:60–20:49, FIGS. 15(a)–17(c))
  - **Fourth Embodiment** (EX1001 at 20:51–22:44, FIGS. 18(a)–20(c))
  - **Claims 1–9** (EX1001 at 32:11–33:67)
  - **Fifth Embodiment** (EX1001 at 22:45–24:51, FIGS. 21(a)–23(d))
  - **Modified Example of Fifth Embodiment** (EX1001 at 24:53–27:60, FIGS. 24(a)–29(b))
  - **Sixth Embodiment** (EX1001 at 27:62–29:60, FIGS. 30(a)–32(c))
  - **Modified Example of Sixth Embodiment** (EX1001 at 29:62–32:9, FIGS. 33(a)–35(c))
  - **Claims 10–15** (EX1001 at 34:1–36:18)

Support for claims 10 and 13

See, e.g., IPR2016-01376, Paper 2, at 20–21. Compare also, e.g., IPR2016-01376, EX1001, with IPR2016-01376, EX1014 and IPR2016-01376, EX2012.

The Board's Construction is Proper

Summary of the Specification's Inconsistencies

- **Patent Owner Identified Three Examples of an Intermediate Layer With a Flush Sidewall Being Called a "Mask"**
  - '696 Patent at **17:30–40, FIGS. 13(b), 13(c)**
  - '696 Patent at **19:40–49, FIGS. 16(c), 16(d)**
  - '696 Patent at **26:22–29, FIGS. 28(b), 29(a)** (not in JP '371)
- **Petitioner Identified Seven Examples of an Intermediate Layer With a Flush Sidewall not Being Called a "Mask"**
  - '696 Patent at **11:51–55, FIGS. 2(c), 3(a)**
  - '696 Patent at **13:37–41, FIGS. 6(a), 6(b)**
  - '696 Patent at **14:41–45, FIGS. 8(a), 8(b)**
  - '696 Patent at **16:7–11, FIGS. 10(c), 11(a)**
  - '696 Patent at **17:20–29, FIGS. 13(a), 13(b)**
  - '696 Patent at **19:33–40, FIGS. 16(a), 16(b)**
  - '696 Patent at **21:33–39, FIGS. 18(c), 19(a)**

See, e.g., IPR2016-01376, EX1049, at ¶¶ 20–28; IPR2016-01376, Paper 26, at 8–9.

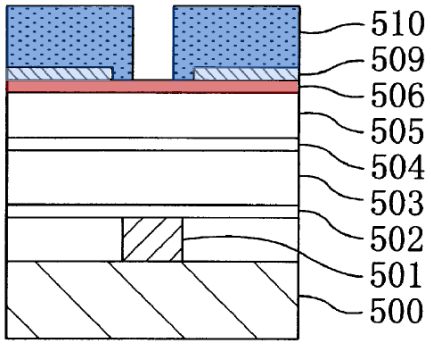
’696 Patent Error in Identifying a Mask

At Least One Incorrect Description: Layer 509 is not a “mask”

Then, as shown in FIG. **22**(*b*), a second resist pattern **510**, having openings for forming contact holes, is formed by lithography on the mask pattern **509**. Thereafter, the second silicon dioxide film **506** is dry-etched using the second resist pattern **510** and the mask pattern **509** as a mask, thereby forming a patterned second silicon dioxide film **506A** having openings for forming contact holes as shown in FIG. **22**(*c*).

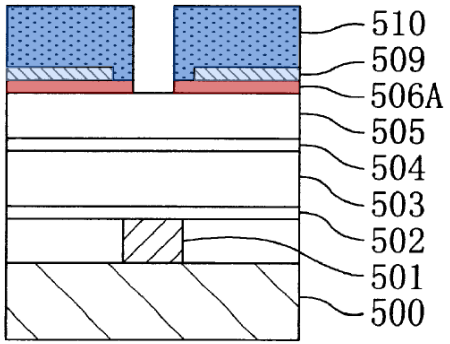
’696 Patent, 23:40–46

Fig. 22(b)



’696 Patent, Fig. 22(b)

Fig. 22(c)



’696 Patent, Fig. 22(c)

See, e.g., IPR2016-01376, EX1001 at 23:40–46, FIGS. 22(b), 22(c); IPR2016-01376, EX1049, at ¶¶ 23–26; IPR2016-01376, Paper 19, at 13–14.

Patent Owner's Expert Agrees Layer 509 Is Not a Mask

Dr. Glew's Testimony

Q You see the sentence after that that says, "Thereafter the second silicon dioxide film 506 is dry etched using the second resist pattern 510 and the mask pattern 509 as a mask"? You see that?

A Yes.

In Figure 22-B do you understand layer 510 to be a resist that includes a contact hole pattern?

A Yes, I understand 510 is a resist for forming a contact hole.

Q Okay. And do you understand that pattern 509 has openings -- is a layer that has openings performing wiring grooves out of a titanium nitride film? Is that your understanding?

A That's my understanding, yes. 507 is etched from a pattern for wiring groove and thereafter called 509.

Q Going from Figure 22-B to 22-C, what's being depicted here is an etch of layer 506, is that correct?

A Yes. 506 is shown as etched, a silicon dioxide film.

Q So in this particular case certainly 510 is functioning as a mask to transfer the contact hole pattern to layer 506, right?

A I understand that 510 is described as that in the text.

IPR2016-01376, EX1047, at 95:4–96:21

See, e.g., IPR2016-01376, Paper 26, at 8; IPR2016-01376, Paper 35, at 11–12; IPR2016-01376, EX1047, at 95:10–99:21.

Patent Owner's Expert Agrees Layer 509 Is Not a Mask

Dr. Glew's Testimony

As I see Figure 22-B and C, 509 is completely covered and there is no chemical contact between the etchant and 509, so it can't determine the transfer to pattern.

Q (By Mr. Jiron) So in other words, it doesn't have a role in transfering the pattern?

MR. DAVIS: Objection to form.

THE WITNESS: Well, due to its being chemically isolated, it can't contact the reactive chemistry of the etchant, it can't determine the pattern that's transferred.

IPR2016-01376, EX1047, at 98:21–99:9

Q (By Mr. Jiron) So looking at that Figure 1, wouldn't you understand layer 509 to be a mask in transfering the pattern from layer 510 into layer 506? Right?

A It may be a mask for later purposes. In this particular step, 509 is not functioning as a mask to transfer a pattern or feature into 506 because the etchant cannot chemically contact it.

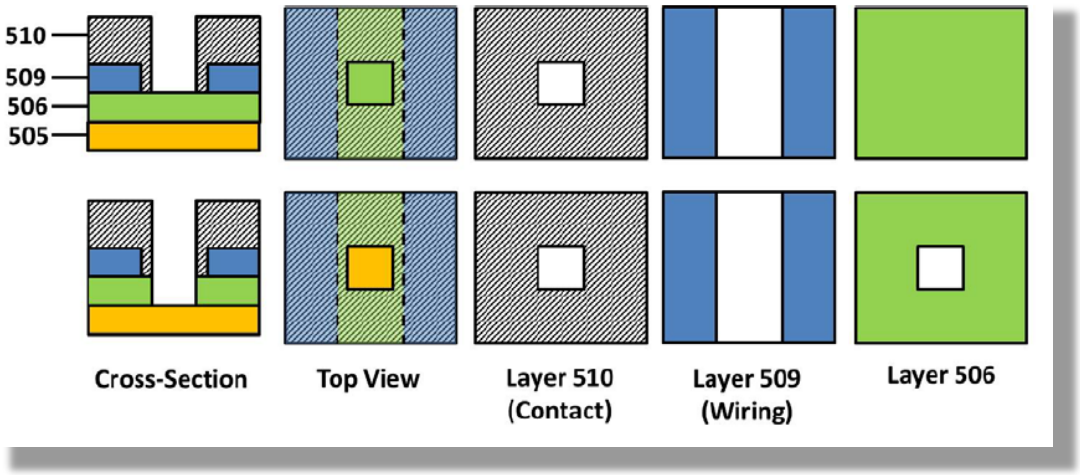
There is no interaction between the etchant species, the reactive species to do the work and the material 509.

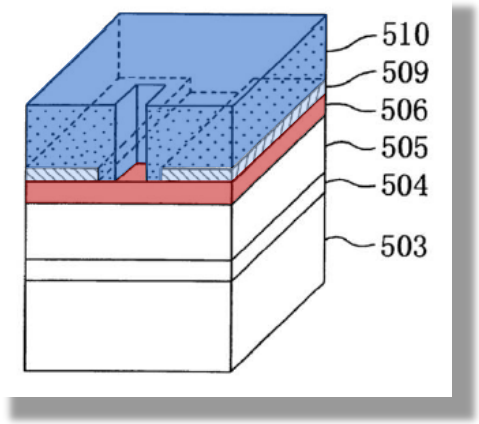
IPR2016-01376, EX1047, at 99:10–21

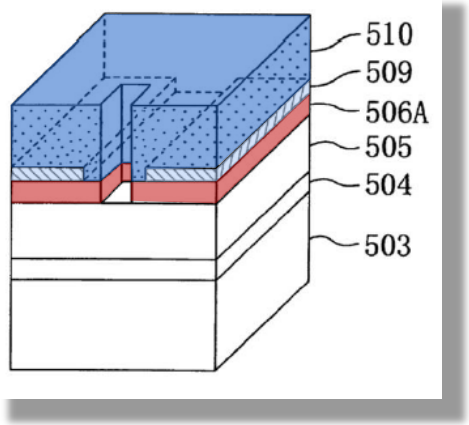
See, e.g., IPR2016-01376, EX1047, at 95:10–99:21.

’696 Patent Error in Identifying a Mask

At Least One Incorrect Description: Layer 509 is not a “mask”







IPR2016-01376, EX1049 at ¶25

See, e.g., IPR2016-01376, EX1001 at 23:40–46, FIGS. 22(b), 22(c); IPR2016-01376, EX1049, at ¶25.

The Experts Agree Layer 509 Is Not a Mask

Dr. Smith's Testimony

26. As these images illustrate and Dr. Glew's testimony confirms, a person of ordinary skill in the art would have understood the draftsperson made an error in the '696 specification by identifying layer 509 as a mask in Figures 22(b) and 22(c). The rationale proposed by IPB (Paper 6, at 42) makes no sense, because it would limit the example above to obscure, restrictive, and difficult-to-imagine circuit layouts with complex and unnecessary shapes. This would run contrary to the general nature of this processing technology and other examples in the '696 patent. In fact, the '696 patent does not discuss circuit layouts at all, nor is there any technical reason for such restrictive and incomprehensible circuit layouts. To deem layer 509 a "mask" in this etch step would, in my view, would be contrary to the way a person of ordinary skill would have viewed the disclosure.

IPR2016-01376, EX1049 at ¶26

See, e.g., IPR2016-01376, EX1049, at ¶26.

Inconsistent Disclosures Do Not Alter Plain Meaning

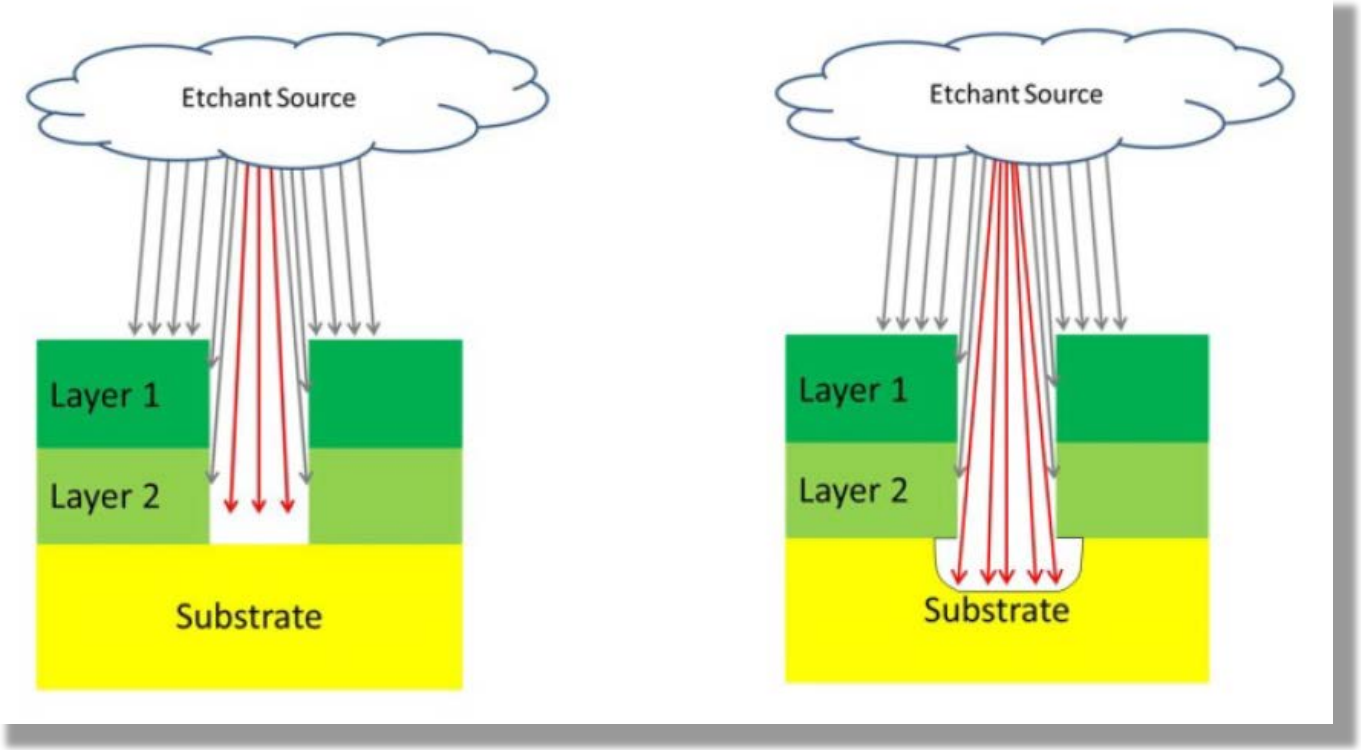
- **These Inconsistencies Do Not Justify Modifying the Board's Claim Construction**
  - ***Trs. of Columbia Univ. v. Symantec Corp.***, 811 F.3d 1359, 1366 (Fed. Cir. 2016) ("The patentee cannot rely on its own use of inconsistent and confusing language in the specification to support a broad claim construction which is otherwise foreclosed.").
  - ***Bayer CropScience AG v. Dow Agro Sciences LLC***, 728 F.3d 1324, 1328–29 (Fed. Cir. 2013) ("The patent and its history, however, do not clearly indicate that the patent uses the language at issue without its accepted scientific descriptive meaning. On the contrary, Bayer's usage in the intrinsic record is at the very best inconsistent. Much of it actually reinforces the straightforward descriptive meaning of the claim terms. . . . The conclusion we draw is that there is no clear message that the patent gives Bayer's broad meaning to [the term] in place of the term's accepted scientific meaning.").
  - ***Digital Biometrics, Inc. v. Identix, Inc.***, 149 F.3d 1335, 1345 (Fed. Cir. 1998) ("It is clear from the entirety of the written description that this is not an accurate statement. . . . [It] therefore does not alter our construction, which is based on the entire written description.").

See, e.g., IPR2016-01376, *Paper 26, at 8–9.*

Anisotropic Etches for Dual Damascene Processes

Patent Owner's Theory of Masking is Flawed

- **An intermediate layer with flush edges cannot prevent undercutting of the layer being etched**



IPR2016-01376, Paper 26, at 5

See, e.g., IPR2016-01376, Paper 26, at 4–6; IPR-2016-01376, EX1049, at ¶¶11–15.

Patent Owner Does Not Explain How the Intermediate Layer is a Mask

12. If lateral particles were a problem as IPB suggests, those particles would cause significant undercutting in the layer being etched. IPB and Dr. Glew cite as evidence the figure on the left below, but that is not an accurate representation of what occurs during reactive ion etching. Even if it were, IPB and Dr. Glew ignore the resulting undercutting (shown to the right below). IPB's figure is inaccurate because such undercutting does not occur in these RIE processes, which produce nearly vertical sidewalls. If such undercutting did occur, it would lead to problems like void formation and electromigration, increased contact resistivity, and possibly contact failure. IPB's misleading figure does not provide evidence that the internal sidewall plays any role in defining areas for etching. What matters instead are sizes and shapes of the openings as seen from above in the plan view, not the internal sidewalls of a buried layer.

IPR2016-01376, EX1049, at ¶12

15. As a matter of physics, the interior surfaces of the layers above the layer being etched do not play the masking role IPB and Dr. Glew suggest. Such usage of the term "mask" is therefore improper even in the hyper-technical sense IPB and Dr. Glew suggest.

IPR2016-01376, EX1049, at ¶15

See, e.g., IPR2016-01376, Paper 26, at 4–6; IPR-2016-01376, EX1049, at ¶¶11–15.

Dual Damascene is Very Anisotropic

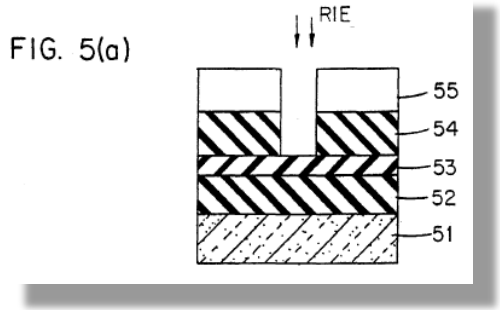
Q Would you agree that in -- or is it your testimony that even in anisotropic etches, there can be some finite angle less than 90 degrees from the base of the feature towards the top?

MR. GOLDBERG: Objection. Form.

A The desired attribute of a multi-layer process like dual-damascene and the requirements for such a process to operate is the side wall angle needs to be vertical. If it's less than 90 degrees, it would need to be determined through analysis and engineering of that process that its impact would influence its use to yield good results.

Smith Dep. Tr. at 23:6–17

insulative layer. A first opening is formed in second insulative layer **54** but not penetrating etch stop layer **53** by a first etching process as shown in FIG. **5**(*a*), preferably anisotropic etching, most preferably reactive ion etching. The size of the first opening is about the size of the ultimate via. As



IPR2016-01376, EX1006, at 6:19–23

112 patterned and etched. All etch process discussed herein are anisotropic etch processes, that is, etch processes that are directional as opposed to isotropic etch processes that etch in all directions. In addition, the etch processes and chemistries are well known in the art and will not be discussed as each etch process can be easily determined by a person of ordinary skill in the semiconductor manufacturing art. The

IPR2016-01376, EX1011, at 4:9–15

See, e.g., IPR2016-01376, Paper 2, at 3–4, 6; IPR2016-01376, EX2040 at 26:20–27:12, IPR2016-01376, EX1006 at 6:19–23, FIG. 5(a); IPR2016-01376, EX1011 at 4:9–15.

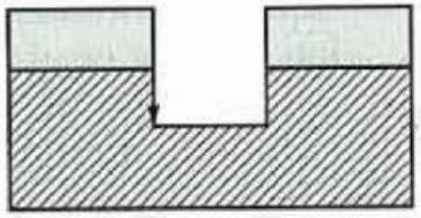
RIE Allows for Very Anisotropic Etch Profiles

Q Is it your testimony that there are certain dry etches that give perfectly vertical side wall profiles?

A Within the capability of measurement or within the requirements of manufacturing, yes.

I -- the word "perfectly" would have to be defined in that context.

Smith Dep. Tr. at 22:6–12



(c) Completely Anisotropic

chemical etching and anisotropic physical etching as illustrated in Figure 10-3(b). Instead, the profile for ion-enhanced etching is much more like the case for physical etching acting alone, as in Figure 10-3(c). If the chemical component in the etch system is increased, the vertical etching is increased but not the lateral etching, which is not what would be expected from chemical etching. . . .

* * *

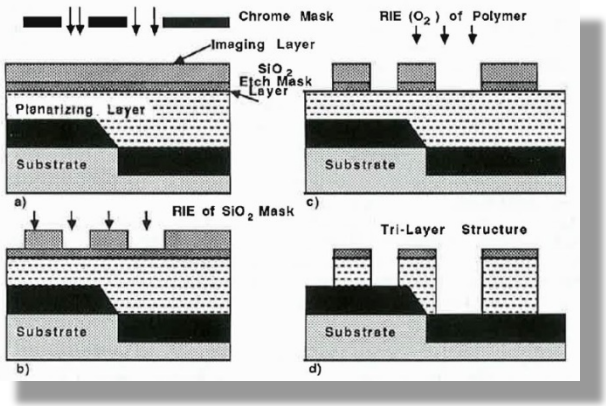
Whatever the exact mechanism for ion-enhanced etching, . . . directional etching occurs because of the directionality of the ions. The enhancement of the process . . . occurs only where the ions strike the surface. Since the ions are striking normal to the wafer surface, the enhancement will occur normal to the wafer surface. This directional enhancement will result in directional, anisotropic etching.

IPR2016-01376, EX1049, at ¶14

See, e.g., IPR2016-01376, EX2040 at 26:20–27:12; IPR2016-01376, EX1049 at ¶14; IPR2016-01376, EX1030, at 40–42.

Multi-Layer Resist Processes

Why Tri-Layer Resists Are Irrelevant

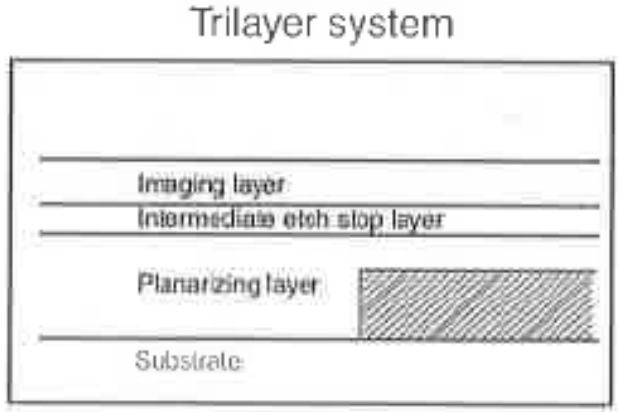


- **Tri-Layer Resist Process:**
  - **Three Layers:**
    - Bottom Planarizing Layer
    - Middle Etch-Stop Layer
    - Top Photoresist Layer
  - **Step 1:** Expose and Develop Top Photoresist Layer
  - **Step 2:** Etch the Resist Pattern Into the Middle Etch-Stop Layer Using the Top Photoresist as the Mask
  - **Step 3:** Etch the Pattern Into the Bottom Planarizing Layer Using the Middle Etch-Stop Layer as a Mask.
  - **Note:**
    - The Middle Etch-Stop Layer Is a Mask Because the Top Photoresist Layer Comes Off First, Not Because of Its Sidewalls
    - Nothing In Any of the Evidence Suggests an Intermediate Layer Is a Mask During a Subsequent Etch

See, e.g., IPR2016-01376, Paper 26, at 6–7; IPR2016-01376, EX1032, at 14; IPR2016-01376, EX1049, ¶¶16–19.

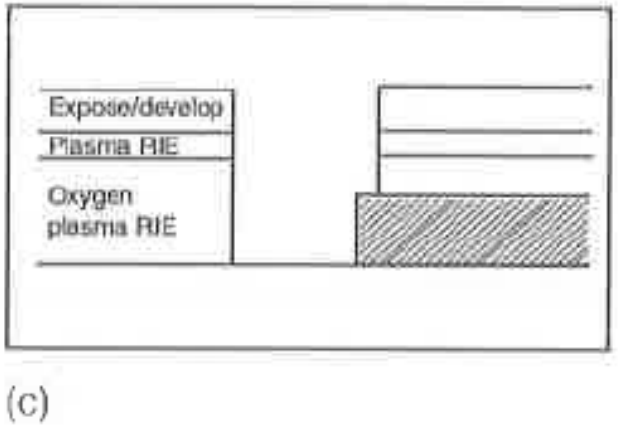
Patent Owner Mischaracterizes Dr. Smith's Book

Contrary to the additional negative limitation and Petitioner's expert's (Dr. Smith) arguments during his deposition, Petitioner's expert has admitted in prior publications that a "multiple layer resist" having ***flush*** edges can be used to define a "substrate film material" to be etched—*i.e.*, can be used as a mask. EX2018 642-643, 657; EX2010 49:6-50:9; EX2009 ¶¶70-71; *see also* EX2017 574, 592. For



12.3 Wet-Development/Dry-Pattern Transfer Approaches to Multilayers

Anisotropic pattern transfer can allow significant improvement over the isotropic processing of wet-etched multilayer approaches. Through the use of a plasma-reactive-ion-etch (RIE) pattern transfer process, near anisotropy can be approached, allowing high-aspect ratio, fine-feature resolution [12,13]. The three-layer scheme, depicted in Figure 12.3, makes use of a polymeric planarizing layer (such as novolac resin or polyimide) and a thin intermediate etch-stop layer. This etch-stop layer can be a spin-on organosilicon compound (spin-on glass), a low-temperature oxide, a silicon oxinitride, or a metallic layer, which provide oxygen etch resistance. A thin resist imaging layer is coated over this etch-stop, exposed, and wet developed. Pattern transfer into the intermediate etch-stop layer can be achieved with wet-etch or dry-plasma techniques with suitable chemistry. Anisotropic pattern transfer through the thick polymeric planarizing layer can be achieved via an oxygen RIE process. Variations on this technique have been used for both optical and electron beam applications [14].



IPR2016-01376, EX2018, at 19 (643)

IPR2016-01376, EX2018, at 18 (642)

See, e.g., IPR2016-01376, Paper 19, at 17; IPR2016-01376, EX2018, at 18–19.

Dr. Smith Testimony

This bottom figure is not intended to show what the structure would look like after the processing. Instead, this is intended to show, and it's consistent with the words that I just read, how the integrity of that pattern is transferred through those three layers.

IPR2016-01376, EX2010, at 61:14–19

The reason I've drawn the picture the way I did, as I've said before, to show that pattern transfer from top to bottom can retain that same sidewall angle if it's done in a way that I've described. It's not meant to depict what the final result would be, and you can tell that based on the words I've used. I've not labeled these in terms of what they are but the process that's used to transfer those layers, exposed developed plasma RIE and then oxygen plasma RIE.

IPR2016-01376, EX2010, at 62:15–63:2

See, e.g., IPR2016-01376, Paper 19, at 17–18; IPR2016-01376, Paper 26, at 6–7; IPR2016-01376, EX1049, at ¶17; IPR2016-01376, EX2010, at 60:22–65:8.

Dr. Smith Testimony

That etch-stop layer provides resistance to etch the planarizing layer. The functionality is then not part of the photoresist. The photoresist, as I've said, is a thin resist imaging layer, so it's used for imaging only, and it's only used to transfer the pattern into the etch-stop.

What happened since I've said the planarizing layer is polymeric, and I had in parentheses "such as novolac resin or polyimide," novolac resin is the same resin that we used in a photoresist. So it would be obvious that what would happen as you do the oxygen plasma RIE is the resist would be gone.

IPR2016-01376, EX2010, at 62:2–14

A. So there are two etch processes and a develop process involved. The imaging layer is exposed and developed. The etch-stop is etched in a plasma RIE. If it's a -- I have used examples, for instance, let's say a spin-on glass, that plasma RIE would be a fluorine-containing plasma, for example, SF6 maybe, fluorine-containing plasma. Then the plasma etch conditions, and in particular the reactive-ion etch conditions, would be changed to etch the planarizing layer. So it would be an oxygen plasma.

After all is said and done, after the exposed developed and the two plasma reactive-ion etch steps, then that layer is defined to etch something underneath that. So in the diagram, that very bottom horizontal line would be whatever that substrate thin film material is. That then would be etched using this process.

So this doesn't address what would be etched underneath that hasn't been etched yet. This is just defining that multiple layer -- multiple layer resist.

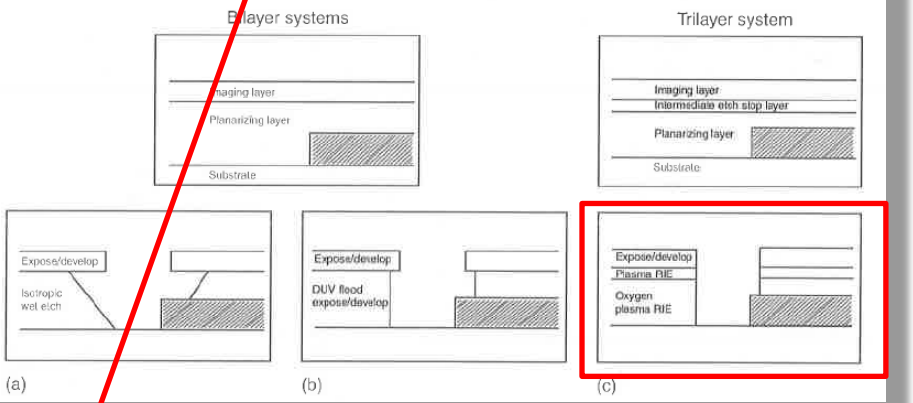
IPR2016-01376, EX2010, at 64:9–65:8

See, e.g., IPR2016-01376, Paper 19, at 17–18; IPR2016-01376, Paper 26, at 6–7; IPR2016-01376, EX1049, at ¶17; IPR2016-01376, EX2010, at 60:22–65:8.

Source Material Confirms Dr. Smith's Testimony

12.2 Multilayer Planarizing Processes—Wet Development Approaches

Various multilayer techniques have been introduced that employ polymeric planarization layers to reduce substrate topography and allow the use of a thin top-coated imaging resist layer, as depicted in Figure 12.3 [4]. Methods have included a wet-processed thick planarization layer [5], a two-layer portable conformable mask (PCM) [6], and a three-layer plasma transfer process [7]. The wet-processed approach leads to isotropic dissolution



IPR2016-01376, EX2018, at 18

4. J.A. Bruce, B.J. Lin, D.L. Sundling, and T.N. Lee. 1987. *IEEE Transactions on Electron Devices*, **34:** 2428.
5. B.J. Lin, E. Bassous, W. Chao, and K.E. Petrillo. 1981. *Journal of Vacuum Science and Technology B*, **19:** 1313.
6. B.J. Lin. 1980. *Journal of the Electrochemical Society*, **127:** 202.
7. E.D. Lin, M.M. O'Toole, and M.S. Change. 1981. *IEEE Transactions on Electron Devices*, **28:** 1405.
8. C.H. Ting and K.L. Liauw. 1983. *Journal of Vacuum Science and Technology B*, **1:** 1225.
9. M.P. de Grandpre, D.A. Vidusek, and M.W. Leganza. 1985. *Proceedings of SPIE*, **539:** 103.
10. Y. Todokoro. 1980. *IEEE Transactions on Electron Devices*, **27:** 1443.
11. P.A. Lamarre. 1992. *IEEE Transactions on Electron Devices*, **39:** 1844.

IPR2016-01376, EX2018, at 46

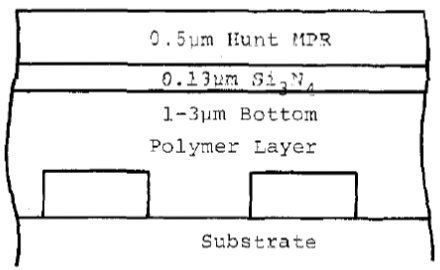


Fig. 6. Tri-layer resist system.

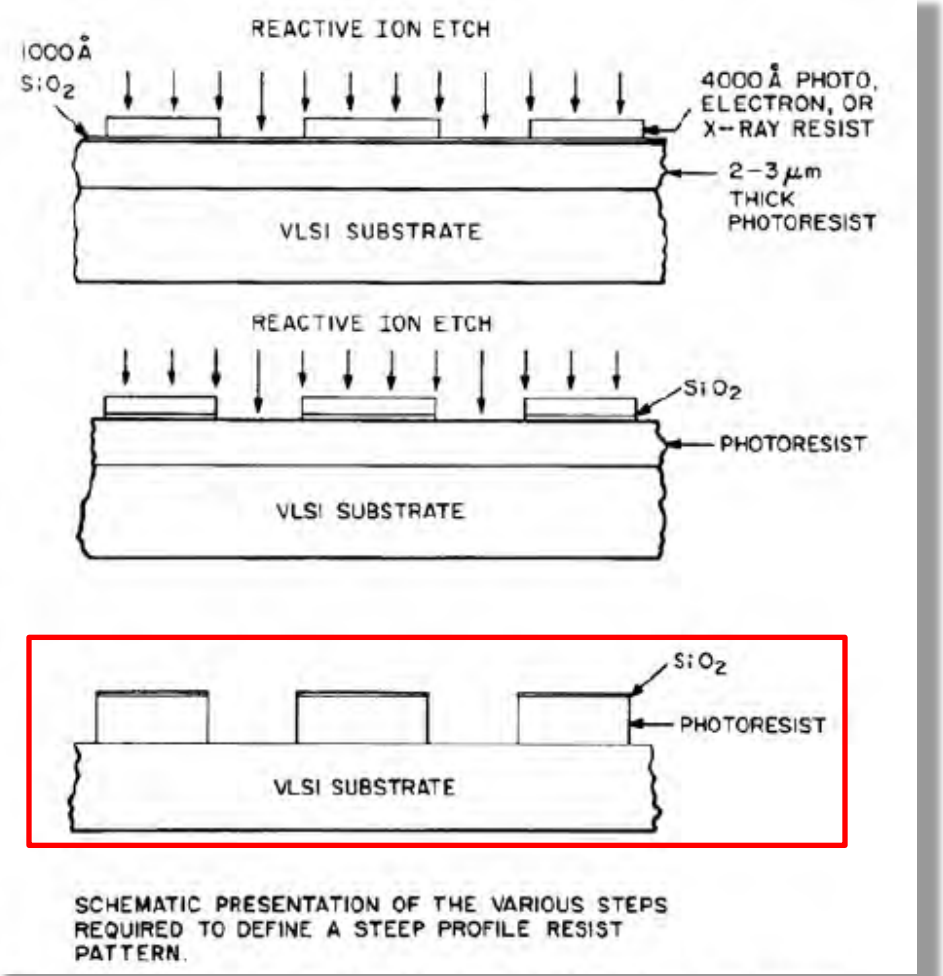
IPR2016-01376, EX1045, at 3

reflecting substrate. The purpose of multilayer systems is to approximate the ideal surface conditions for exposure. Fig. 6 illustrates the multilayer structure used. An absorbing polymer, 1 to 3 μm thick, is used to planarize the substrate topography. The planarized surface enables the uniform dispense of the top resist layer and thus suppresses the bulk effect. The absorption of the bottom polymer eliminates reflections from the substrate topography and reduces the standing-wave effect. An intermediate silicon nitride layer serves as a reactive ion etch shield for the pattern transfer to the bottom layer. The silicon nitride has an index of approximately 1.8, which minimizes reflections from the nitride–resist interfaces. If the differential etch rate between the top and bottom polymers were sufficient, an intermediate layer would not be required.

IPR2016-01376, EX1045, at 3

See, e.g., IPR2016-01376, Paper 26, at 6–8 & n.2; IPR2016-01376, EX2017, at 61, 96; IPR2016-01376, EX2018, at 18–19, 46; IPR2016-01376, EX1045, at 3; IPR2016-01376, EX1049, at ¶18.

Source Material Confirms Dr. Smith's Testimony



SCHEMATIC PRESENTATION OF THE VARIOUS STEPS REQUIRED TO DEFINE A STEEP PROFILE RESIST PATTERN.

IPR2016-01376, EX1044, at 3

51. J.R. Havas. 1973. U.S. 3,873,361.
52. B.J. Lin and T.H.P. Change. 1979. *Journal of Vacuum Science and Technology*, **1:** 1969.
53. J.M. Moran and D. Maydan. 1979. *Journal of Vacuum Science and Technology*, **16:** 1620.
54. F. Buiguez, P. Parrens, and B. Picard. 1983. *Proceedings of SPIE*, **393:** 192.
55. B. Lin. 1983 in *Introduction to Microlithography*, L. Thompson, M. Bowden, and G. Wilson, eds., Washington, DC: American Chemical Society, pp. 287 349.
56. E. Bassous, L. Ephrath, G. Paper, and S. Mikalsen. 1983. *Journal of the Electrochemical Society*, **130:** 478.

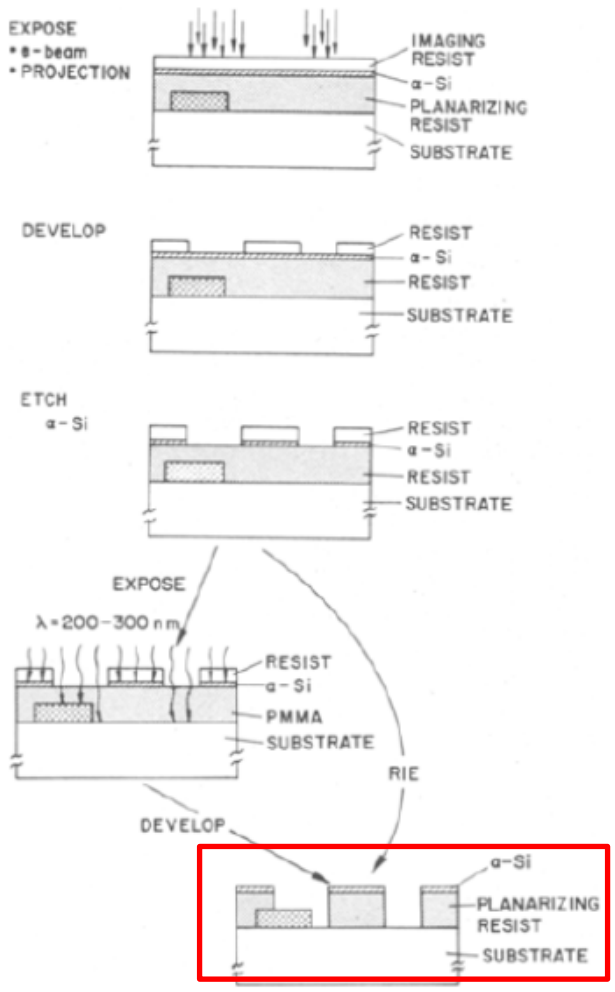
IPR2016-01376, EX2018, at 47

The top layer of x-ray resist was exposed and developed to a final thickness of 0.45 μm using an x-ray exposure tool.[1,2] With the x-ray resist as a mask, the SiO_2 was reactive ion etched with a CHF_3 gas. The pattern was then transferred into the thick organic (resist) layer using reactive ion etching, with pure O_2 gas forming the plasma and the SiO_2 acting as the mask. The rf power density was 0.30 W/cm² and the time

IPR2016-01376, EX1044, at 4

See, e.g., IPR2016-01376, Paper 26, at 6–8 & n.2; IPR2016-01376, EX2018, at 47; IPR2016-01376, EX1044, at 3–4; IPR2016-01376, EX2017, at 97.

Source Material Confirms Dr. Smith's Testimony



IPR2016-01376, EX1046, at 2

51. J.R. Havas. 1973. U.S. 3,873,361.
52. B.J. Lin and T.H.P. Change. 1979. *Journal of Vacuum Science and Technology*, **1:** 1969.
53. J.M. Moran and D. Maydan. 1979. *Journal of Vacuum Science and Technology*, **16:** 1620.
54. F. Buiguez, P. Parrens, and B. Picard. 1983. *Proceedings of SPIE*, **393:** 192.
55. B. Lin. 1983 in *Introduction to Microlithography*, L. Thompson, M. Bowden, and G. Wilson, eds., Washington, DC: American Chemical Society, pp. 287 349.
56. E. Bassous, L. Ephrath, G. Paper, and S. Mikalsen. 1983. *Journal of the Electrochemical Society*, **130:** 478.

IPR2016-01376, EX2018, at 47

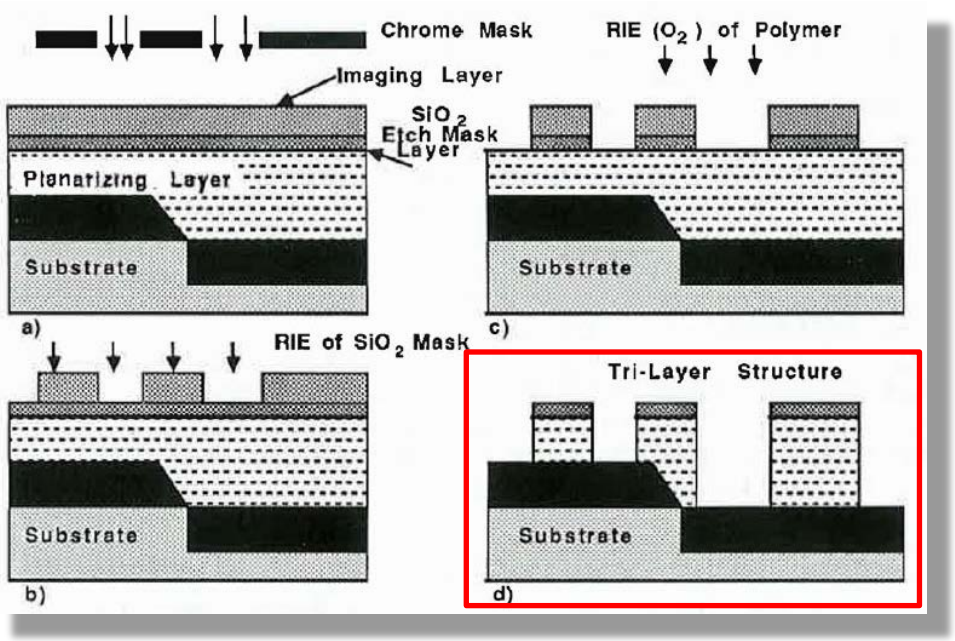
Pattern replication.—Transfer of the image pattern from the top AZ layer to the Si film was performed by RIE in a diode reactor with a perforated grounded aluminum catcher plate positioned between the electrodes to minimize backscattering of sputtered aluminum

Etching of the underlying PMMA or polymer layer was performed in an oxygen plasma at 20 mTorr pressure and 0.06 W/cm^2 rf power density. Overetching varied between 50 and 100% depending on the topography present and the maximum thickness of resist. The etch rates of the 3 layers viz., Si, AZ1350J, and PMMA in CF_4 were 40, 50, and 70 nm/min, respectively, while in O_2 the etch rates of the same films were 0, 35, and 70 nm/min, respectively. Replication of the AZ image pattern in an Si film 100 nm thick resulted in an AZ film loss of 200 nm, while replication into a PMMA layer $\leq$1 μm resulted in the total loss of the AZ film.

IPR2016-01376, EX1046, at 3

See, e.g., IPR2016-01376, Paper 26, at 6–8 & n.2; IPR2016-01376, EX2018, at 47; IPR2016-01376, EX1046, at 2–3.

Independent Evidence Confirms Dr. Smith's Testimony

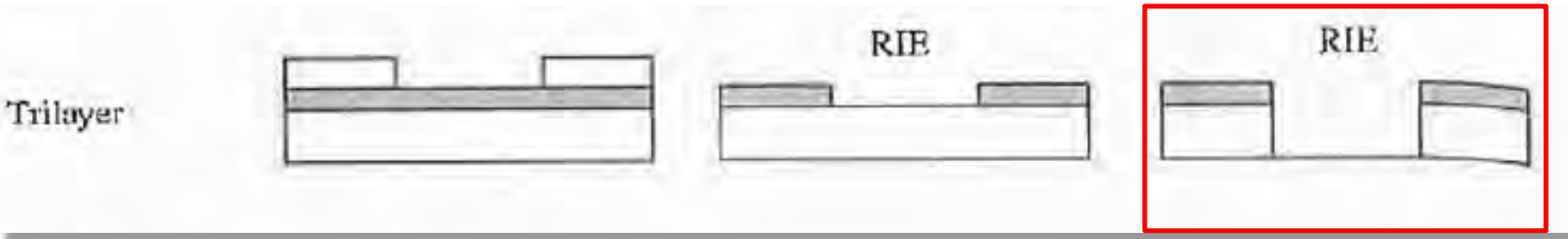


IPR2016-01376, EX1032, at 14

In the *tri-layer resist* process (Fig. 11), a thick organic layer is again used to partially planarize the surface[23]. Materials investigated for this layer have included conventional positive optical photoresist, polyimide, and polysulfone. A thin layer of SiO_2 (spin-on or PECVD) is then deposited to act as an etch mask for the bottom layer. An imaging resist layer is finally applied, and patterned in a conventional manner (e.g. near-UV exposure and wet development). To minimize effects from standing waves and reflections from the substrate, the lower layer is treated to increase its optical density (see the section on *Resist Processing: Exposure*). The SiO_2 and lower layer are dry etched anisotropically to precisely transfer the pattern from the thin imaging layer into the thick lower layer. The main disadvantage of the tri-layer process is the added complexity that it requires.

See, e.g., IPR2016-01376, Paper 26, at 6–7; IPR2016-01376, EX1032, at 14.

Independent Evidence Confirms Dr. Smith's Testimony



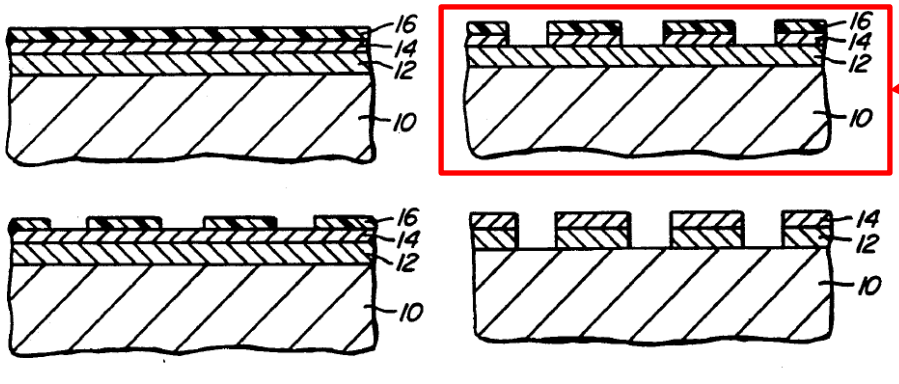
IPR2016-01376, EX1031, at 41

Recently, multilayer lithography has become increasingly important for ULSI processing because it provides high resolution that is independent of the underlying materials and substrate topography. The trilayer scheme is a very popular multilayer lithography method. It uses a conventional resist to pattern an intermediate layer, such as silicon dioxide or nitride, that acts as a mask during the subsequent planarization of the organic layer by oxygen RIE. A high degree of anisotropic and selective etching is required in these applications. This implies that both chemical

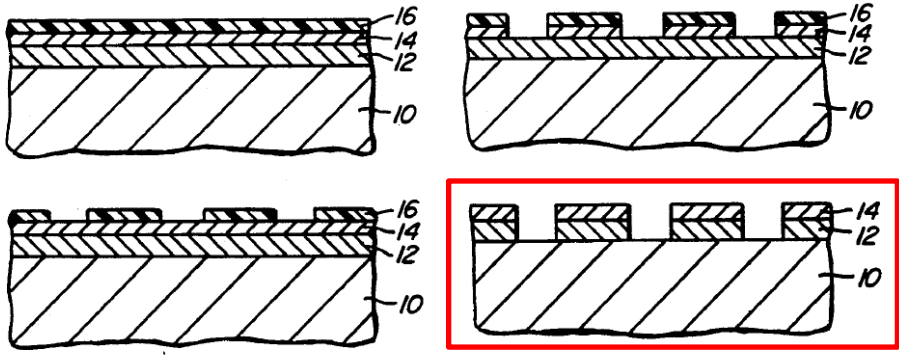
IPR2016-01376, EX1031, at 70

See, e.g., IPR2016-01376, Paper 26, at 6–7; IPR2016-01376, EX1031, at 41, 70.

Independent Evidence Confirms Dr. Smith's Testimony



IPR2016-01376, EX1033, at FIGS. 1–4



IPR2016-01376, EX1033, at FIGS. 1–4

Once the resist layer **16** has been patterned, it is used as a mask for etching the metal image layer **14**, as illustrated in FIG. **3**. The chromium metal imaging layer **14** may be etched using conventional wet etchants, such as ceric ammonium sulfate-based etchants, at room temperature. The aluminum metal imaging layer **14** may be wet etched using a phosphoric/nitric acid mixture, or may be dry etched using a chlorine plasma, such as CCl_3, CCl_4, HCl, Cl_2, or BCl_3.

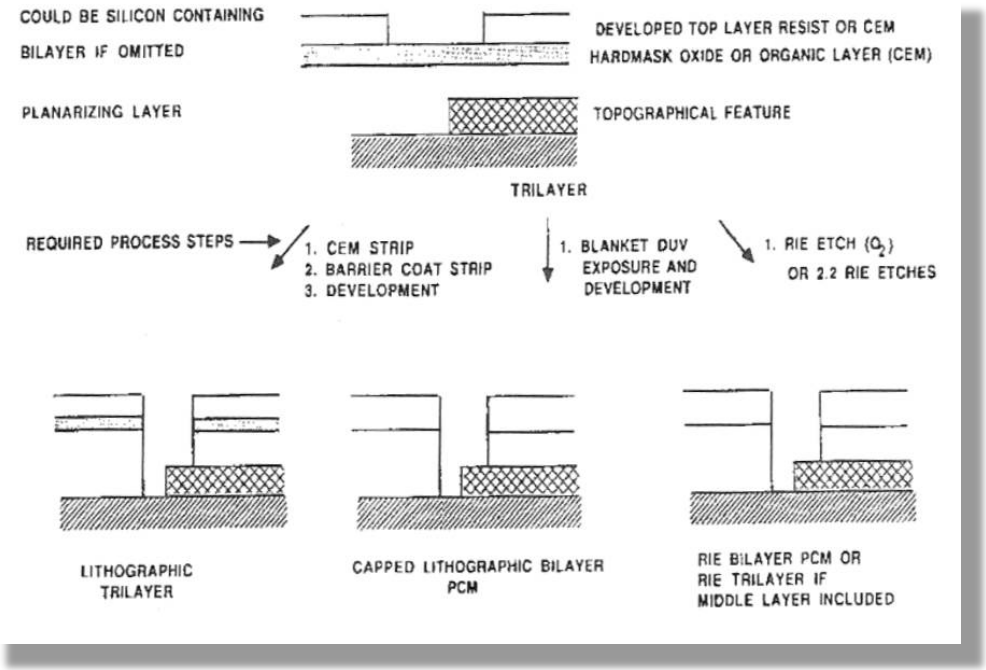
After patterning, the metal imaging layer **14** is used as a mask for plasma etching the primary layer **12**. In the case of an aluminum primary layer **12**, a chlorine plasma i employed as described above. In the case of a dielectric primary layer, the nature of the plasma will depend on the nature of the dielectric. In the case of organic dielectrics, such as polyimides, an oxygen plasma is suitable. In the case of inorganic dielectrics, such as silicon dioxide and silicon nitride, fluorine plasmas such as CF_4, CHF_3, and the like, will find use.

After etching, the substrate will appear as illustrated in FIG. **4**, with the resist layer **16** having been removed during the plasma etch of the primary layer. If desired, the metal imaging layer **14** may be removed by conventional techniques. The chromium imaging layer can be removed by wet etching with ceric ammonium sulfate-based etchants or with an oxygen plasma. An aluminum metal imaging layer **14** can be removed by wet etching using a phosphoric acid/nitric acid mixture at an elevated temperature, typically about 70° C., or by dry etching with a chlorine-based plasma.

IPR2016-01376, EX1033, at 3:20–49

See, e.g., IPR2016-01376, Paper 26, at 6–7; IPR2016-01376, EX1033, at 3:20–49, FIGS. 1–4.

Exhibit 2015 Describes the Same Processes



IPR2016-01376, EX2015, at 8

5.2 Introduction to Multilayer Applications

Multilayer processing techniques, where layers of radiation sensitive (top), non-photosensitive organic, and/or inorganic materials sandwiched together to become the total patterning layer, have become common in semiconductor and computer manufacturing R&D labs. (See Fig. 114.)[3] Due to their complexity and problems that have appeared at bilayer interfaces, these techniques have not been widely accepted in high volume production.

Photolithography image edge and dimension quality is limited by two basic effects, bulk and substrate reflectivity.[13][154] The bulk effect arises when lithography patterns are required at two different topographical layer levels of the vertically-fabricated monolithic circuit. Reflectivity effects occur when patterned areas of the circuit have different reflectivity coefficients, as well as topographical levels.

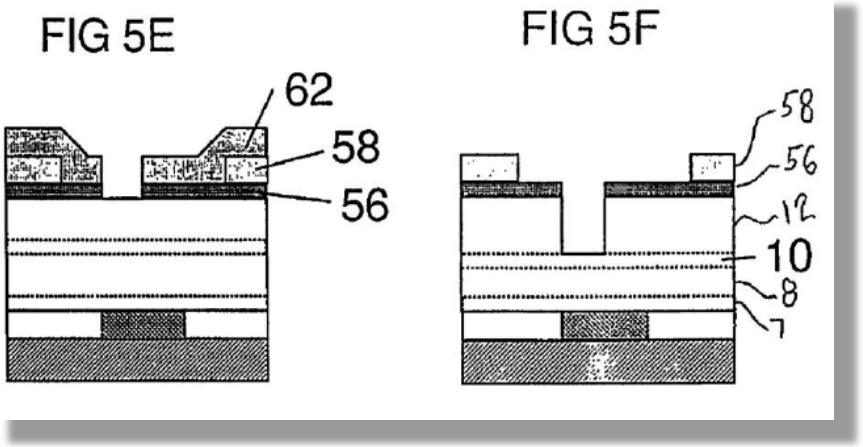
IPR2016-01376, EX2015, at 7

See, e.g., IPR2016-01376, Paper 19, at 18; IPR2016-01376, EX2015, at 7–8.

Grill's 102(e) Date Is January 16, 1998

"Concurrently"

- **Patent Owner does not dispute that the provisional application teaches etching or transferring the via pattern into carbon-containing dielectric layer 12 ("second dielectric layer") while etching or removing photoresist layer 62 ("via-patterned second layer of resist"). EX1018, pp. 12, 15**



See, e.g., IPR2016-01376, Paper 19, at 37–40; IPR2016-01376, Paper 26, at 20–22 & n.6; IPR2016-01376, Paper 35, at 7–9; IPR2016-01376, EX1049, at ¶¶44–53 & n.1.

"Removal"

- Patent Owner argues the limitation in claim 28 of transferring said via pattern in said patterned first hard mask layer into said second dielectric layer, **while concurrently removing said via-patterned second layer of resist**" requires "completely" removing layer 62.
- Claim 28, however, does not have the word "completely" before "removing."

See, e.g., IPR2016-01376, Paper 19, at 39–40; IPR2016-01376, Paper 26, at 21 n.6; IPR2016-01376, Paper 35, at 7–9; IPR2016-01376, EX1049, at ¶46 n.1.

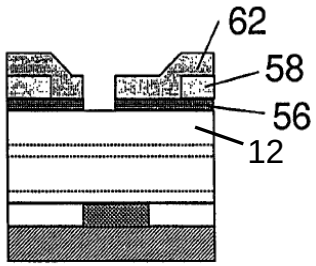
“Partially Concurrently”: Different Context

transferring said via pattern in said patterned first hard mask layer into said second dielectric layer, while concurrently removing said via-patterned second layer of resist, and

IPR2016-01376, EX1017, at cl. 28

- **“transferring . . . while concurrently removing”** means there is no time while etching layer 12 that resist layer 62 is not also being etched
- Allows for layer 12 etch to finish before layer 62 removal finishes, but not vice versa (which makes sense because layer 62 is the etch mask)

FIG 5E

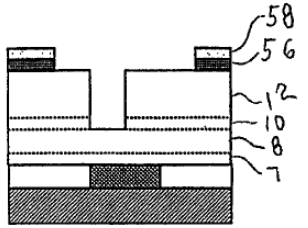


transferring, at least partially concurrently, said via pattern into said first dielectric layer to form via cavities corresponding to said via pattern, and said wiring pattern into said second dielectric layer to form wiring cavities corresponding to said wiring pattern, and

IPR2016-01376, EX1017, at cl. 28

- **“transferring, at least partially concurrently, [two layers]”** means there exists a time during which both layer 12 and layer 8 are being etched
- Allows for either layer to finish etching before the other (which makes sense because they likely have different thicknesses)

FIG 5G



See, e.g., IPR2016-01376, EX2040, at 45:1–6, 46:4–48:5; IPR2016-01376, Paper 35, at 7–9.

A Comparison of Grill and Its Provisional Parent

FIGS. 5A-5E show a first preferred embodiment of a method for forming a dual pattern hard mask comprising a first layer of a first material with a first pattern, and a second layer of a second material with a second pattern; FIGS. 5F-5H show how this dual pattern hard mask may be used to fabricate a dual relief cavity for use in a Dual Damascene process. For purposes of illustration, one of said first and second patterns will be a via level pattern, and the other of said first and second patterns will be a wiring level pattern. However, ~~the~~this combination of via and wiring level patterns should be viewed as a special ~~cases~~case of the general category of dual relief patterns in which all features of a smaller area (via) pattern ~~completely fit within~~substantially overlap with the features of a larger area (wiring) pattern.

FIG. 5A shows the structure of FIG. 1B after application of lower hard mask layer 56 and upper hard mask layer 58. Hard mask layers 56 and 58 are preferably formed from different materials which have different etch properties from each other and from the dielectric underlayers 12 and 8. For example, lower hard mask layer 56 might be formed from Si3N4 and upper hard mask layer 58 might be formed from SiO2. Other suitable hard mask materials may include SiO2-based materials, other oxides, nitrides other than Si3N4, carbon-based dielectrics, ~~and~~SiC-based dielectrics, polycrystalline silicon, ~~and~~ amorphous hydrogenated silicon, and metals. A first resist layer 60, patterned with a first (wiring level) pattern, is formed on layer 58 to form the structure of FIG. 5B. If resist layer 60 is misaligned, rework at this stage presents no problem. The pattern of resist layer 60 is transferred into upper hard mask layer 58 by an etching process to form the structure of FIG. 5C. The etching process is preferably selective, for example a selective SiO2 to Si3N4 etch, so that lower hard mask layer 56 will remain intact during any overetching of hard mask layer 58.

Patterned resist layer 60 is then removed by a process such as ashing or wet chemical etching, and a second resist layer 62, patterned with a second (via level) pattern, is then formed on the structure of FIG. 5C to produce the structure of FIG. 5D. Again, resist rework at this stage presents no problem because lower hard mask layer 56 is still in place to protect dielectric 12. The pattern of resist layer 62 is then transferred
into lower hard mask layer 56. FIG. 5E shows the completed dual pattern hard mask, comprising patterned hard mask layers 56 and 58, with patterned resist layer 62 still in place.

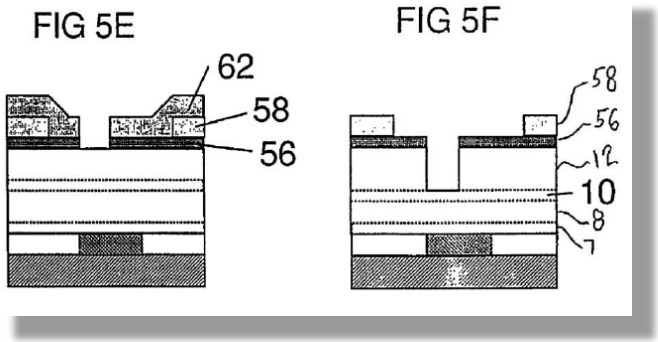
The via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching, to produce the structure of FIG. 5F. Patterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12. The etching conditions are then changed to removed exposed portions of lower hard mask layer 56 and optional etch stop 10, to form the structure of FIG. 5G. Dielectrics 8 and 12 are then etched to transfer said second pattern into the entire thickness of dielectric 12, and said first pattern into the entire thickness of dielectric 8, as shown in FIG. 5H. The cavity structure may then be completed as shown in FIG. 1J, and, for interconnect applications, filled with wiring material 22 as shown in FIGS. 1K ~~to~~and 1L.

IPR2016-01376, EX2011, at 13–15

See, e.g., IPR2016-01376, EX2011, at 13–15.

These Minor Changes Do Not Constitute New Matter

- **"Patterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12."**
  - **This occurs whenever an organic photoresist is used (and organic resists are generally implied, unless specified otherwise)**
  - **The statement clarifies that atypical situations are within the scope of the invention (e.g., inorganic resists are within the scope of the invention)**
  - **That it would be unusual for layer 62 *not to be removed* by the process for etching layer 12 shows a POSITA already would have understood the disclosure of a process in which layer 62 *is removed***



While this "twice patterned single mask layer" process has the virtue of simplicity, difficulties in reworking the second lithography step may occur if the interconnect dielectric and the photoresist stencil used to pattern the hard mask have similar etch characteristics. Such would be the case with an organic photoresist and a carbon-based interconnect dielectric such as DLC. A typical cause for

IPR2016-01376, EX1017, at 11

See, e.g., IPR2016-01376, EX1017, at 11, 15, FIGS. 5E, 5F; IPR2016-01376, Paper 26, at 20–22; IPR2016-01376, EX1049, at ¶¶44–53.

MOTIVATION TO COMBINE

Combining Grill and Aoyama

- **The Petitions and Institution Decisions explain why a POSITA would have been motivated to combine Grill and Aoyama:**
  - Both references are directed to the problems of lithographic misalignment and avoiding rework
    - Grill teaches how to use dual hard masks so rework does not damage carbon-containing interlevel dielectric films
    - Aoyama reduces the probability of requiring rework
  - The Grill and Aoyama solutions are complementary.

See, e.g., IPR2016-01376, Paper 2, at 52–56; IPR2016-01376, EX1002, at ¶¶157–65; IPR2016-01377, Paper 2, at 39–42; IPR2016-01377, EX1002, at ¶¶183–91; IPR2016-01378, Paper 2, at 46–49; IPR2016-01378, EX1002, at ¶¶157–65; IPR2016-01379, Paper 2, at 36–37, 54–59; IPR2016-01379, EX1002, at ¶¶188–96.

Patent Owner's Technical Errors

- Patent Owner and its expert mistakenly argued the combination of references would cause the silicon oxide upper hard mask in Grill to etch faster than the silicon nitride lower hard mask in the presence of a silicon nitride etching process

- This conclusion resulted because Patent Owner and its expert inverted the definition of selectivity, and reversed SiO_2 and Si_3N_4 etches

- Instead, as one would expect, a selective silicon nitride etch removes a silicon nitride mask faster than a silicon oxide mask.

See, e.g., IPR2016-01376, Paper 19, at 58; IPR2016-01376, EX2009, at ¶¶156.

Patent Owner Misunderstands the Terminology

with the film, forming the soluble byproducts. The selectivity, S, of an etch process between two materials, 1 and 2, is simply the ratio of their etch rates, r, in that etchant, or

$$S = \frac{r_1}{r_2} \qquad (10.4)$$

Material 1 is usually the film being etched, and material 2 is either the masking material (photoresist or perhaps silicon dioxide) or the material below the film. We often speak of an etch process for material 1 having a certain selectivity over (or "with respect to," or just "to") material 2. For a large selectivity ($S>>1$) we say that the etch process for material 1 has good selectivity over material 2.

IPR2016-01376, EX1030, at 27

See, e.g., IPR2016-01376, Paper 26, at 24–27; IPR2016-01376, EX1030, at 27.

Patent Owner Misunderstands the Terminology

In most applications, nitride films are patterned with relatively coarse lateral dimensions (e.g. the opening of bonding pads in nitride passivation layers, or the patterning of a thin nitride layer [~1000 Å thick] in the LOCOS process), and thus a high degree of anisotropy is not usually necessary for patterning the nitride. In the LOCOS application, however, sufficient selectivity with respect to SiO_2 must exist so that the thin oxide layer under the nitride (~250 Å thick) is not etched away. This would expose the silicon under the SiO_2 to a fast-etching plasma, which as noted above, would etch the silicon ~8 times as rapidly as the nitride. The selectivity of a CF_4 isotropic Si_3N_4 etching process with respect to SiO_2 is ~2-3, but more favorable selectivity (e.g. 9-10) can be obtained with the use of NF_3 plasmas[26].

IPR2016-01376, EX2020, at 27 (556)

and upper hard mask 58 may be formed from silicon oxide. EX1005 7:34-39.[10] A person of ordinary skill in the art would have understood that silicon oxide etches at a faster rate than silicon nitride when both films are exposed to a silicon nitride etching process. For example, silicon oxide may etch at rate that is at least 2-3 times as fast, and from about 7 to 13 times as fast, depending on the type of silicon oxide film, type of silicon nitride film and etch conditions. EX2020 at 555-556; EX2014 at Fig. 2. Any similar situation wherein the upper hard mask etches more

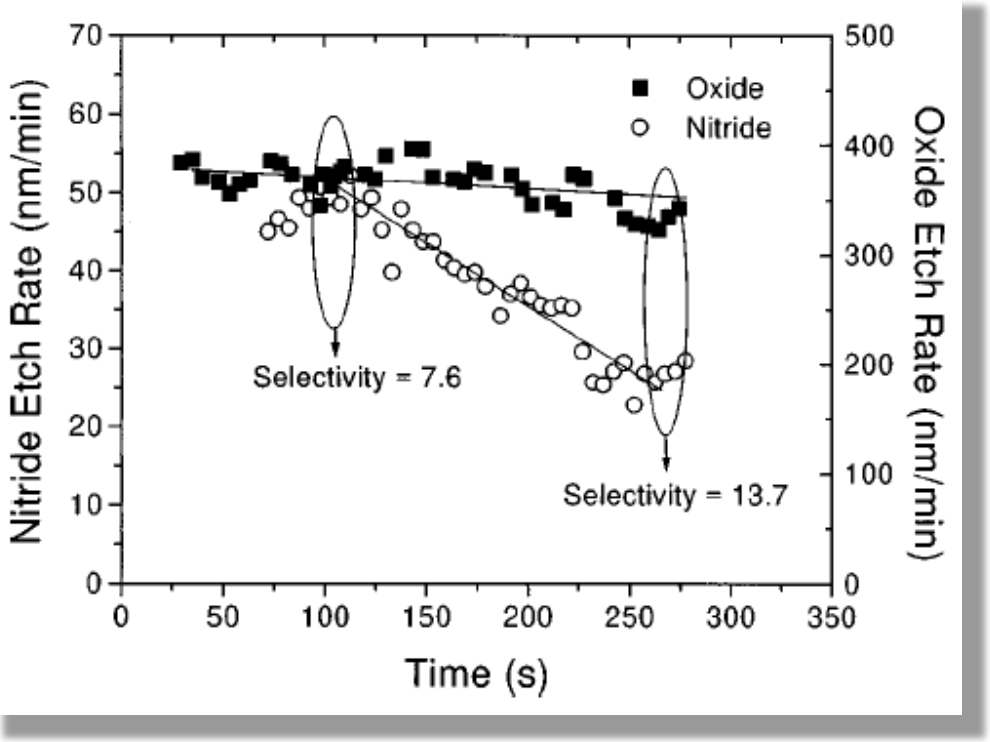
IPR2016-01376, EX2009, at ¶155

See, e.g., IPR2016-01376, EX2009, at ¶155; IPR2016-01376, EX2020, at 27; IPR2016-01376, Paper 26, at 24–27.

Patent Owner's Example Is not a Si_3N_4 Etch

It was found in an earlier study by this group that oxide could be etched at a high rate and at the same time selectively to nitride in a C_3F_6/H_2 (40 sccm/15 sccm) discharge at high inductive power (1400 W) and low operating pressure (6 mTorr) when a sufficiently high RF bias power (200 W corresponding to −100 V self-bias) is applied to the wafer.[12]

IPR2016-01376, EX2014, at 2



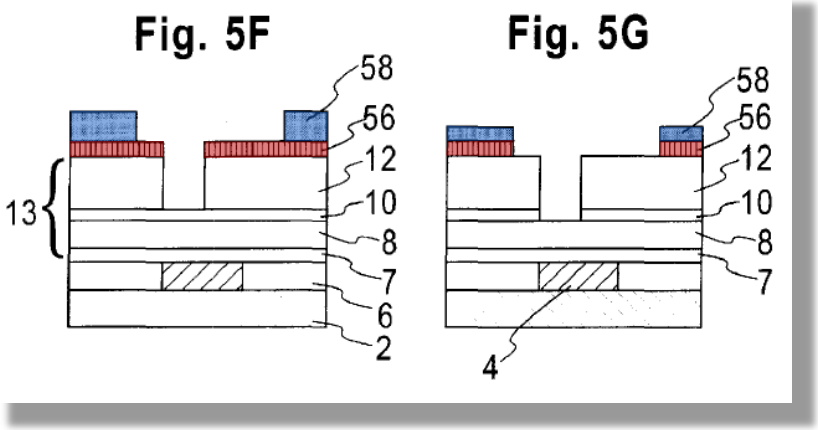
IPR2016-01376, EX2014, at Fig. 2

See, e.g., IPR2016-01376, EX2009, at ¶155; IPR2016-01376, EX2014, at 2, Fig. 2; IPR2016-01376, Paper 26, at 24–27.

Patent Owner Misinterprets Grill's Figures 5F and 5G

FIG. **5A** shows the structure of FIG. **1B** after application of lower hard mask layer **56** and upper hard mask layer **58**. Hard mask layers **56** and **58** are preferably formed from different materials which have different etch properties from each other and from the dielectric underlayers **12** and **8**. For example, lower hard mask layer **56** might be formed from Si3N4 and upper hard mask layer **58** might be formed from SiO2. Other suitable hard mask materials may include

IPR2016-01376, EX1005, at 7:30–38

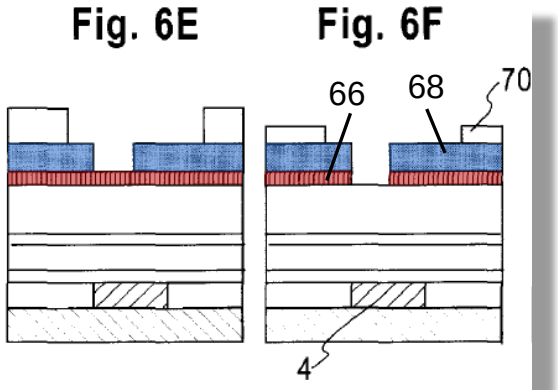


IPR2016-01376, EX1005, at FIGS. 5F, 5G

FIG. **6A** shows the structure of FIG. **1B** after application of lower hard mask layer **66**, middle hard mask layer **68**, and upper hard mask layer **70**. hard mask layers **66**, **68**, and **70** are preferably formed from materials having different etch properties than dielectric underlayers **12** and **8**. Hard mask layers **66** and **70** may be formed from the same material, but preferably one different from that of hard mask layer **68**. For example, lower hard mask layer **66** might be formed from a 20 nm thickness of Si3N4, middle hard mask layer **68** might be formed from a 50 nm thickness of SiO2, and upper hard mask layer **70** might be formed from a 40 nm thickness of Si3N4. Other suitable hard mask materials may include

IPR2016-01376, EX1005, at 8:20–32

No Thinning of Layer 68

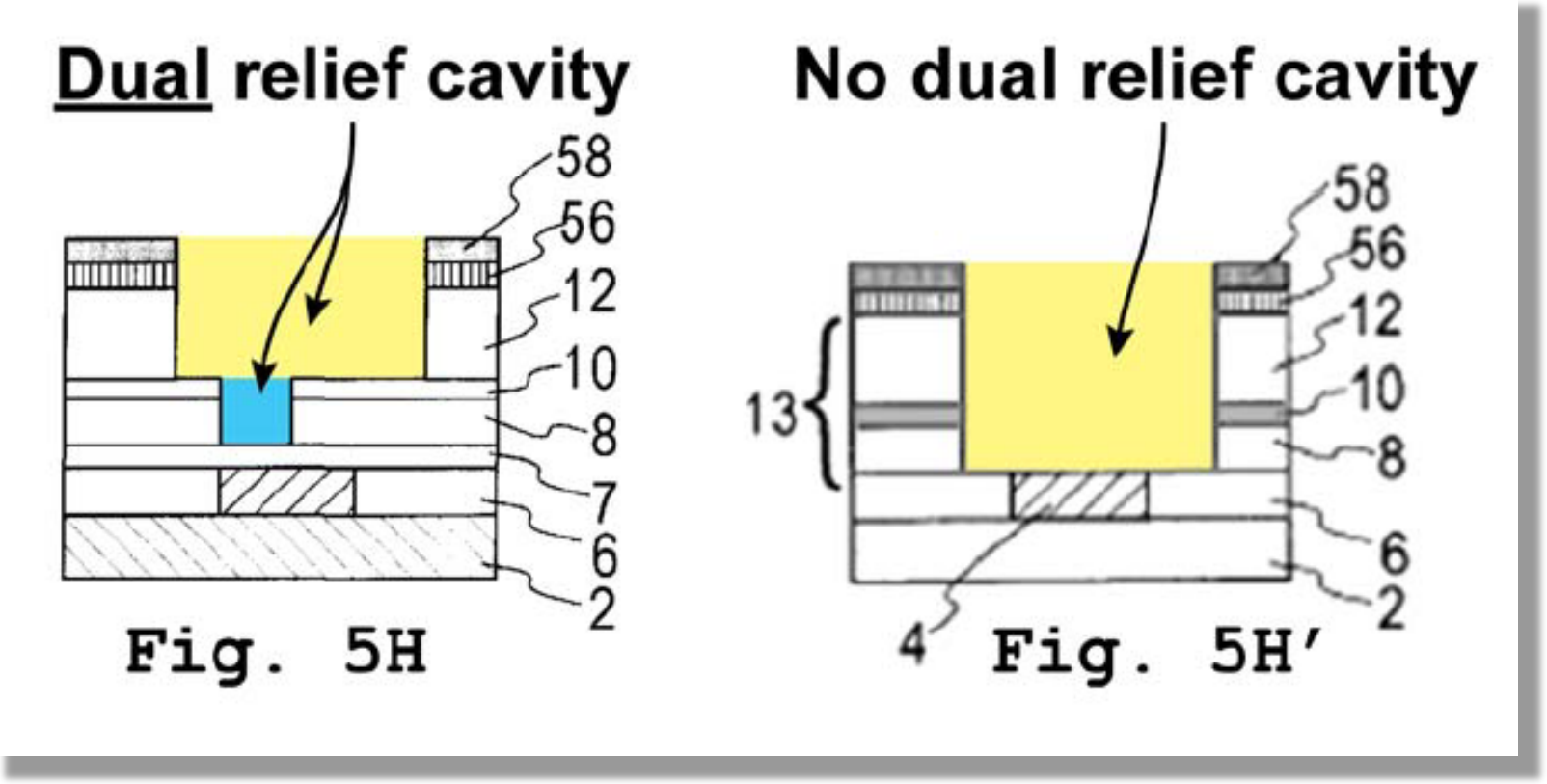


IPR2016-01376, EX1005, at FIGS. 6E, 6F

See, e.g., IPR2016-01376, Paper 26, at 26; IPR2016-01376, EX1005, at 7:30–38, 8:20–32, FIGS. 5F, 5G, 6E, 6F.

Grill-Aoyama Does Not Defeat Grill's Purpose

Patent Owner's Argument

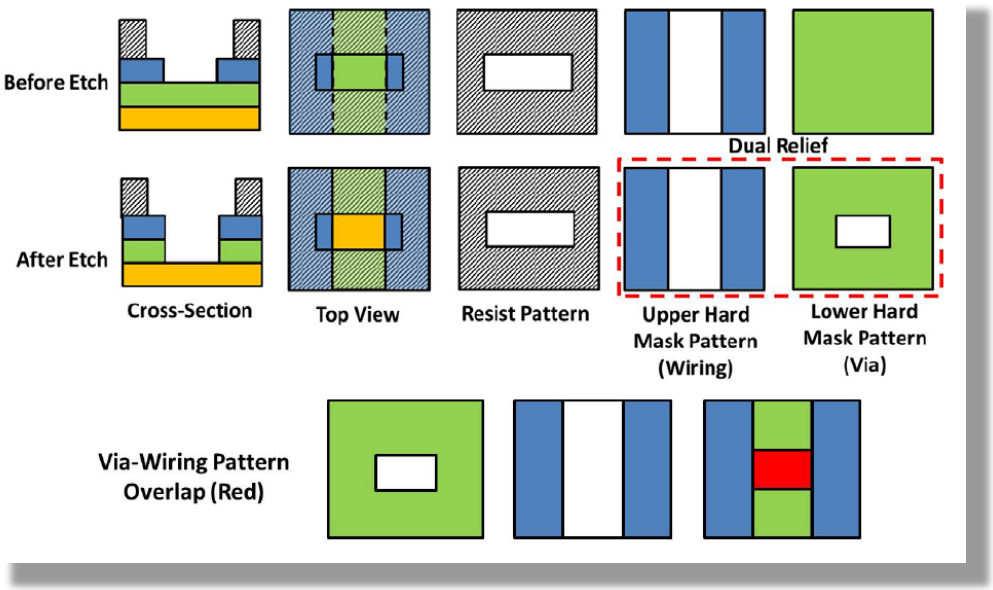


IPR2016-01376, Paper 19, at 52

*Patent Owner never provided any technical reason why this distinction would matter.

See, e.g., IPR2016-01376, Paper 19, at 50–54.

Patent Owner Ignores the Third Dimension



IPR2016-01376, Paper 26, at 24

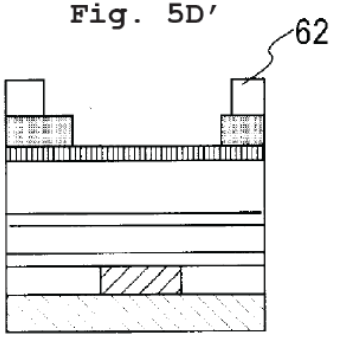
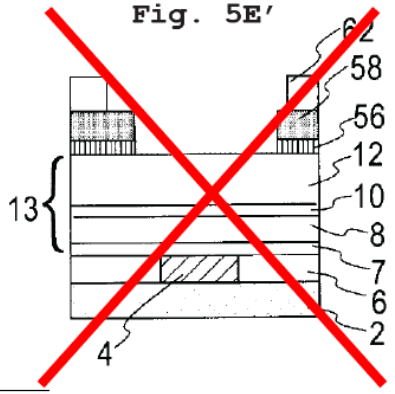
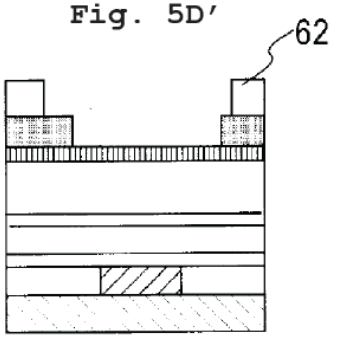
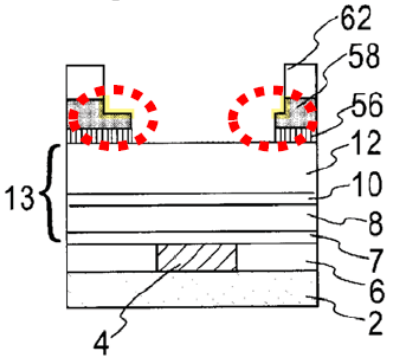
FIGS. **5**A–**5**E show a first preferred embodiment of a method for forming a dual pattern hard mask comprising a first layer of a first material with a first pattern, and a second layer of a second material with a second pattern; FIGS. **5**F–**5**H show how this dual pattern hard mask may be used to fabricate a dual relief cavity for use in a Dual Damascene process. For purposes of illustration, one of said first and second patterns will be a via level pattern, and the other of said first and second patterns will be a wiring level pattern. However, this combination of via and wiring level patterns should be viewed as a special case of the general category of dual relief patterns in which all features of a smaller area (via) pattern substantially overlap with the features of a larger area (wiring) pattern.

IPR2016-01376, EX1005, at 7:16–30

See, e.g., IPR2016-01376, Paper 26, at 23–24; IPR2016-01376, EX1005, at 7:16–30.

Grill-Aoyama Does Not Defeat Grill's Principles of Operation

Patent Owner's Argument

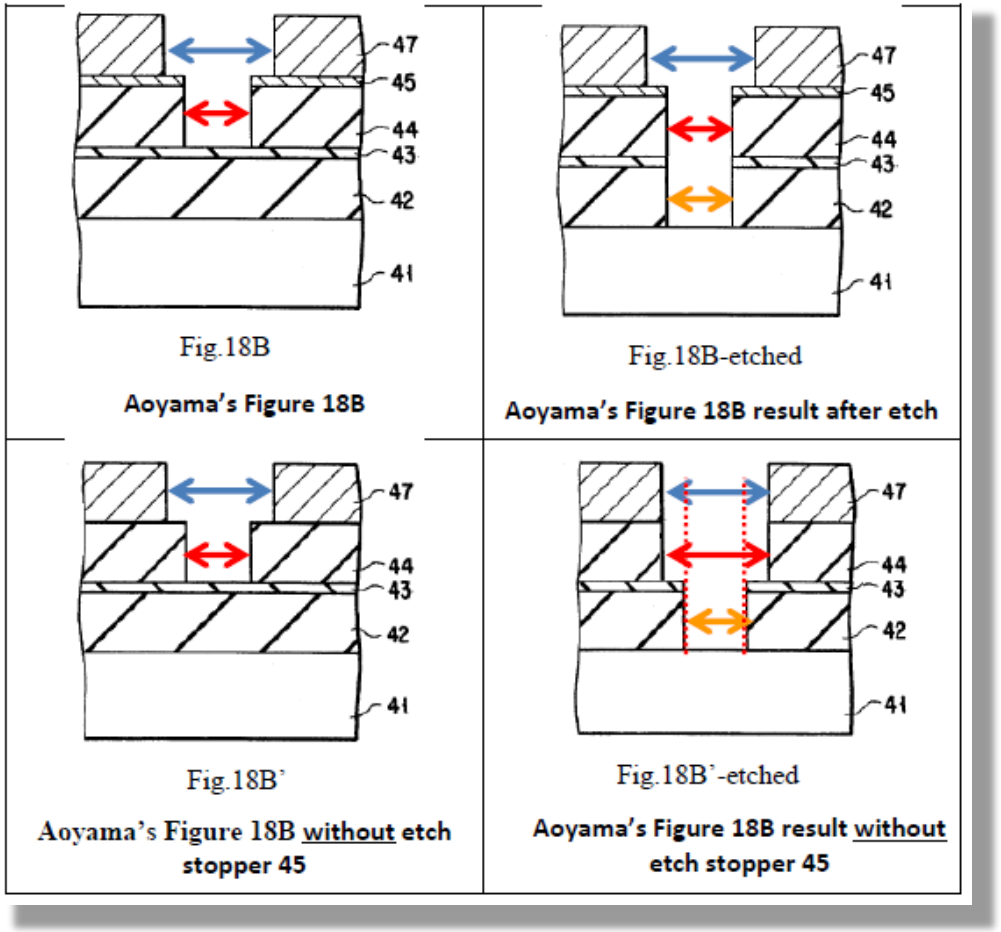
	Before Etch of layer 56	After Etch of layer 56
Petitioner's Inaccurate Illustrations	Fig. 5D′ 	Fig. 5E′ 
Damage to Exposed portions of Grill's Hard Mask layer 58	Fig. 5D′ 	Fig. 5E′-notch 

IPR2016-01376, Paper 19, at 60

See, e.g., IPR2016-01376, Paper 19, at 54–64.

Aoyama Does Not Teach Away From Grill-Aoyama

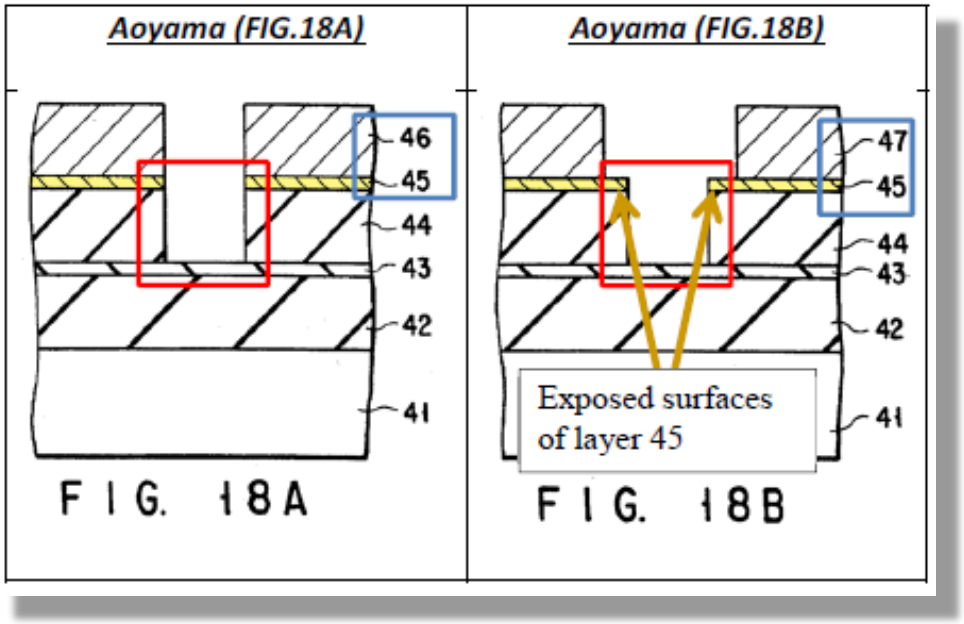
Patent Owner's Argument



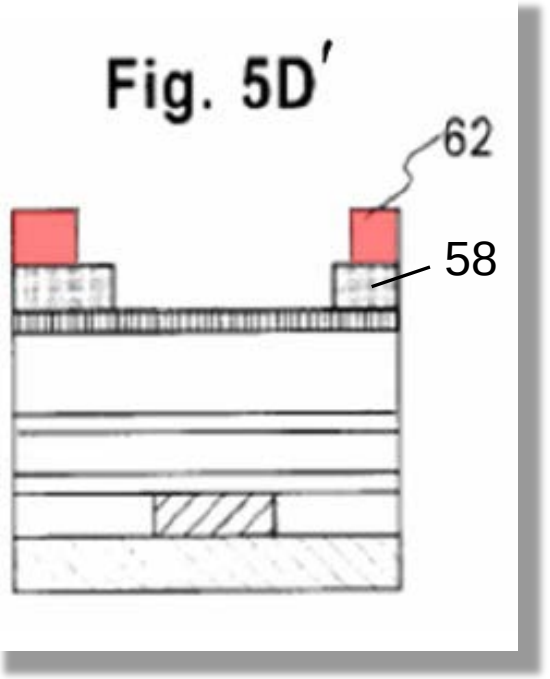
IPR2016-01376, Paper 19, at 66

See, e.g., IPR2016-01376, Paper 19, at 65–71.

Grill-Aoyama Has an Equivalent Layer



IPR2016-01376, Paper 19, at 69



IPR2016-01376, Paper 2, at 62

See, e.g., IPR2016-01376, Paper 19, at 65–71; IPR2016-01376, Paper 2, at 62; IPR2016-01376, Paper 26, at 27.

Grill Does Not Teach Away From Grill-Aoyama

Patent Owner's Argument

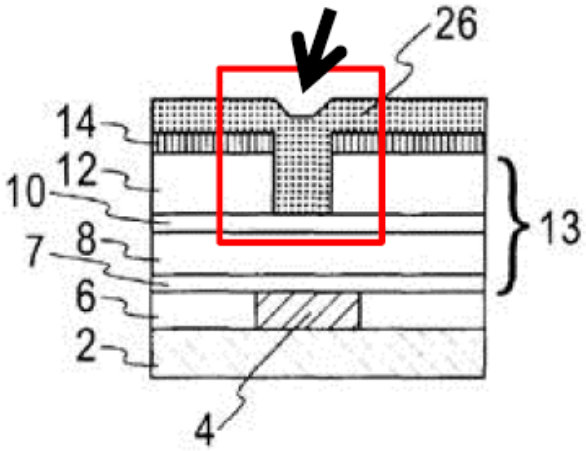
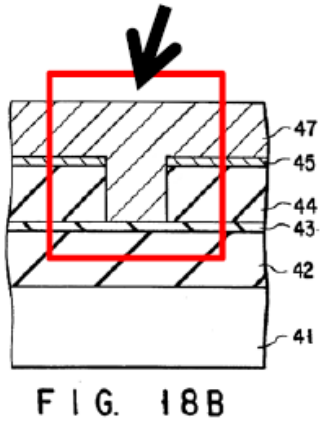
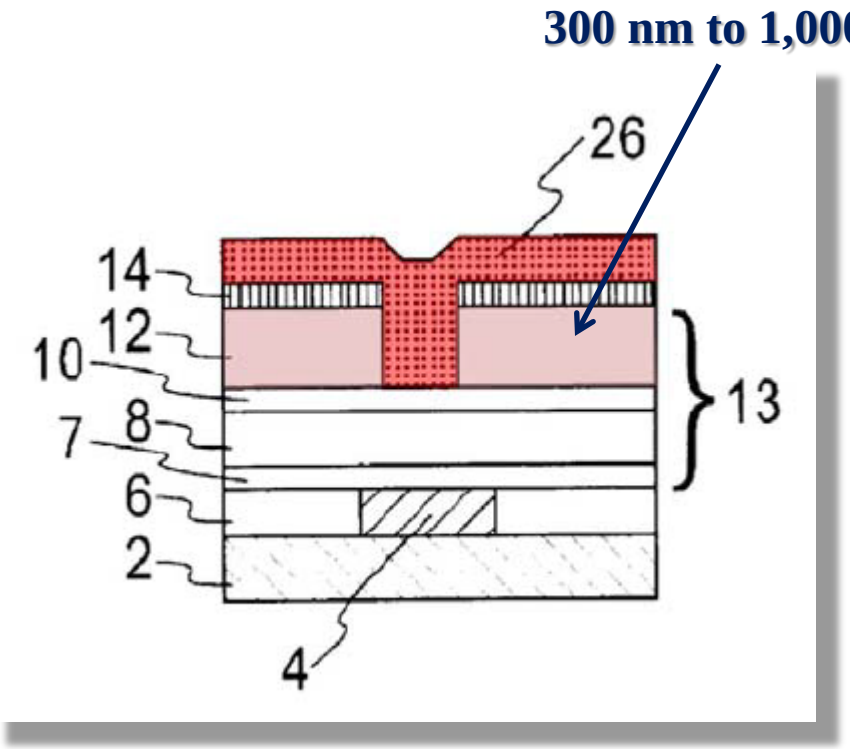
Grill (FIG.2A)	*Aoyama (FIG.18B-modified)*
	

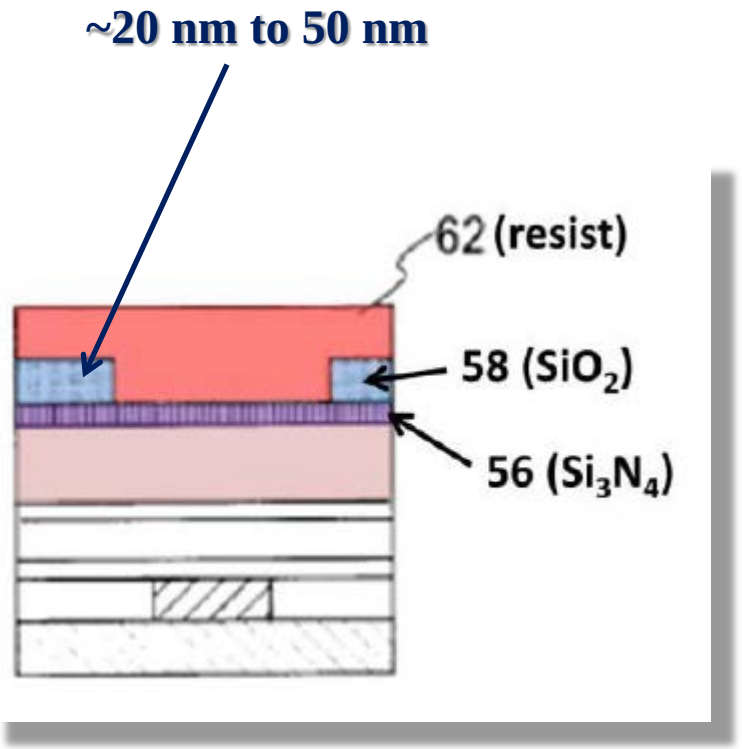
FIG. 18B

See, e.g., IPR2016-01376, Paper 19, at 71–73.

Grill Does Not Teach Away From Grill-Aoyama



IPR2016-01376, Paper 26, at 29



IPR2016-01376, Paper 26, at 30

- **Comparing the lithography over a 300 nm to 1,000 nm step against a 20 nm to 50 nm step is inappropriate. The resist is about 1,000 nm to 2,000 nm thick.**
- **Accommodating a small 20 nm to 50 nm step would have been trivial.**

See, e.g., IPR2016-01376, Paper 19, at 71–73; IPR2016-01376, Paper 26, at 28–31; IPR2016-01376, EX1049, at ¶¶73–74.

The ’696 Patent is in Agreement

Accommodating such a small step in the *Grill-Aoyama* combination would not have been problematic, as the ’696 patent confirms. In the Modified Example of Embodiment 5, photoresist 560 includes a 50 nm photoresist step due to layer 559, but it describes no photolithography or exposure requirements for patterning layer 560 with via patterns wider than the wiring groove. EX1001, 25:9-11, 25:26-36, Fig. 27(b) (below with highlights). This suggests a POSITA would not have viewed this small step as an obstacle. *See* EX1049, ¶¶73-74.

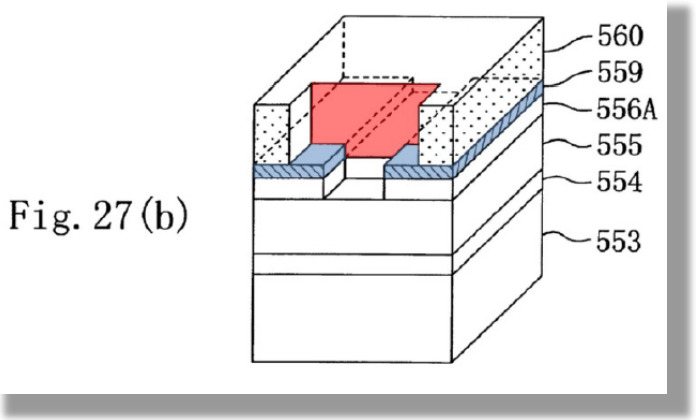
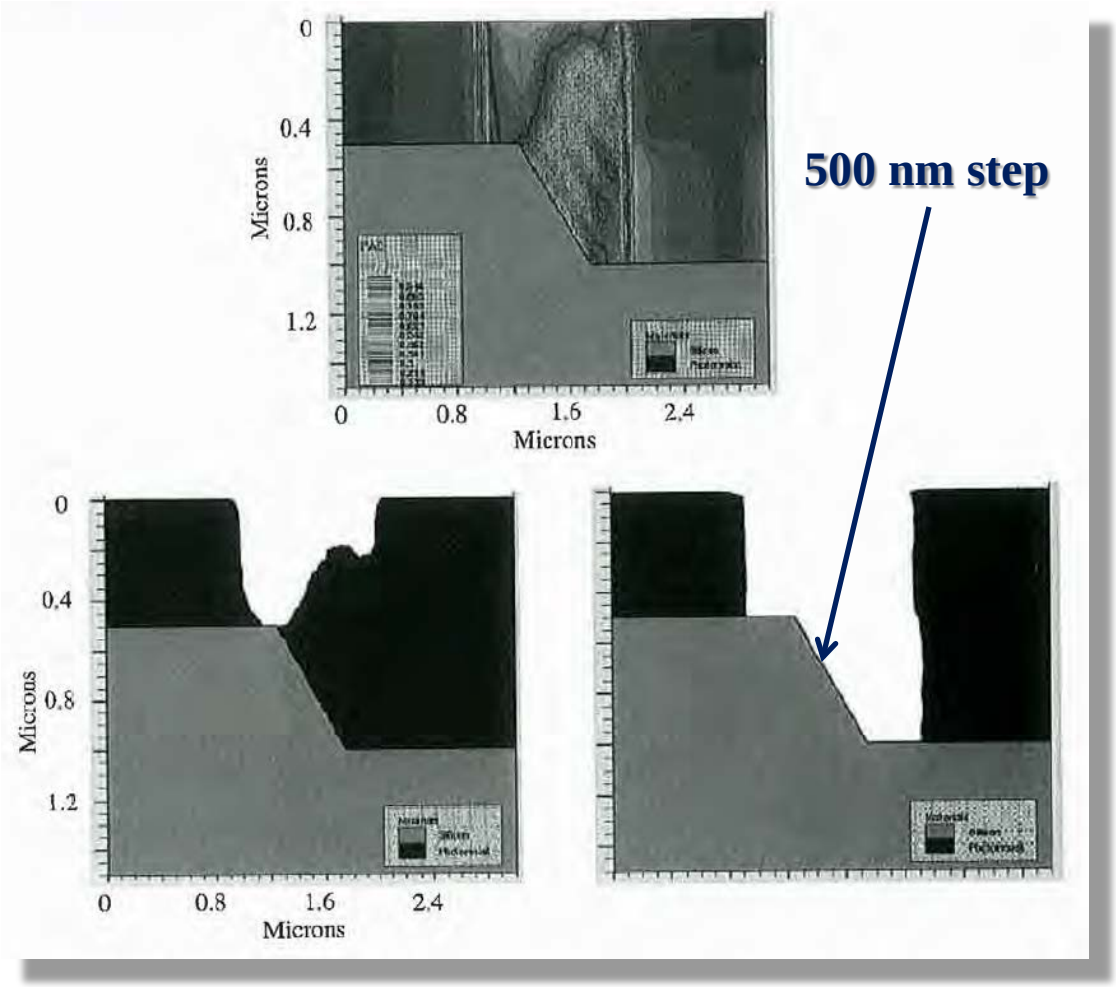


Fig. 27 (b)

IPR2016-01376, Paper 26, at 30–31

See, e.g., IPR2016-01376, Paper 26, at 30–31; IPR2016-01376, EX1001, at 24:60–25:11, 25:36–65, Fig. 27(b).

Accommodating Much Larger Steps Was Routine



IPR2016-01376, EX1030, at 22

See, e.g., IPR2016-01376, EX1030, at 22.

TSMC'S REPLY IS PROPER

Propriety of Petitioner's Reply

Patent Owner's Alleged "New" Argument (Paper 36, at 1)	Petitioner's Response
Petition lacked priority argument (referring to Grill's 102(e) date) Reply 14:8–22:15; Ex. 1036; Ex. 1037; Ex. 1038; Ex. 1049 ¶¶37-54	No such burden in Petition; responsive to Patent Owner's priority allegations Paper 19, at 18–4; *see also* Petition (Paper 2), at 28–29 n.3; EX1002, at ¶153, App'x B; Paper 9, at 1–3
New priority arguments Reply at 17, 19, 21:4–15; EX1036; EX1037; EX1038; EX1049 ¶¶46–52	No such burden in Petition; responsive to Patent Owner's priority allegations Paper 19, at 18–4; *see also* Petition (Paper 2), at 28–29 n.3; EX1002, at ¶153, App'x B; Paper 9, at 1–3
New combination/success arguments regarding "dual relief" cavity Reply 22:16–23:2; EX1039; EX1040	Responsive to Patent Owner's "dual relief" arguments Paper 19, at 50–54 & n.22
New combination/success arguments regarding Aoyama's carbon etch stopper Reply 22:16–23:2; EX1039; EX1040	Responsive to Patent Owner's carbon etch stopper arguments Paper 19, at 65–71

See, e.g., IPR2016-01376, Paper 36, at 1; IPR2016-01376, Paper 2, at 28–29 n.3; IPR2016-01376, EX1002, at ¶153, App'x B; IPR2016-01376, Paper 9, at 1–3; IPR2016-01376, Paper 19, at 18–47, 50–54 & n.22, 65–71.

CLAIM MAPPING

CLAIMS

Independent Claim 10

[10.1] **10**. A method for forming an interconnection structure, comprising the steps of:

[10.2] a) forming a first insulating film over lower-level metal interconnects;

[10.3] b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

[10.4] c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

[10.5] d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film;

[10.6] e) forming a thin film over the fourth insulating film;

[10.7] f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

EX1001 at 34:1–49.

Independent Claim 10

[10.8] g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

[10.9] h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;

[10.10] i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes;

[10.11] j) dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;

[10.12] k) dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes;

EX1001 at 34:1–49.

Independent Claim 10

[10.13] l) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively; and

[10.14] m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

EX1001 at 34:1–49.

Independent Claim 13

[13.1] **13**. A method for forming an interconnection structure, comprising the steps of:

[13.2] a) forming a first insulating film over lower-level metal interconnects;

[13.3] b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

[13.4] c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

EX1001 at 34:58–36:10.

Independent Claim 13

[13.5] d) forming a thin film over the third insulating film;

[13.6] e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

[13.7] f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

[13.8] g) removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;

[13.9] h) dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;

[13.10] i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes;

EX1001 at 34:58–36:10.

Independent Claim 13

[13.11] j) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and

[13.12] k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

EX1001 at 34:1–49, 34:58–36:10.

Dependent Claims 11, 12, 14, and 15

11. The method of claim **10**, wherein at least one of the first and third insulating films is mainly composed of an organic component.

12. The method of claim **10**, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

14. The method of claim **13**, wherein at least one of the first and third insulating films is mainly composed of an organic component.

15. The method of claim **13**, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

EX1001 at 34:50–57, 36:11–18.

Invalidity of the Challenged Claims

Step [10.1]

[10.1] **10**. A method for forming an interconnection structure, comprising the steps of:

MODIFIED EXAMPLE OF EMBODIMENT 5

Next, a method for forming an interconnection structure according to a modified example of the fifth embodiment will be described with reference to FIGS. **24**(*a*) through **24**(*c*), FIGS. **25**(*a*) through **25**(*c*), FIGS. **26**(*a*) through **26**(*d*), FIGS. **27**(*a*) and **27**(*b*), FIGS. **28**(*a*) and **28**(*b*) and FIGS. **29**(*a*) and **29**(*b*).

'696 patent at 24:53–59

MODIFIED EXAMPLE OF EMBODIMENT 6

Next, a method for forming an interconnection structure according to a modified example of the sixth embodiment will be described with reference to FIGS. **33**(*a*) through **33**(*c*), FIGS. **34**(*a*) through **34**(*c*) and FIGS. **35**(*a*) through **35**(*c*).

'696 patent at 29:62–67

[57] **ABSTRACT**

The present invention relates to lithographic methods for forming a dual relief pattern in a substrate, and the application of such methods to fabricating multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels.

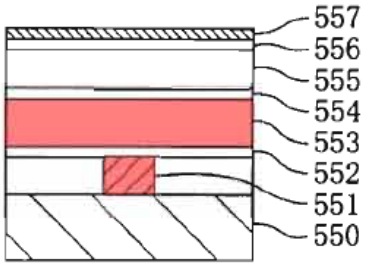
Grill at Abstract

EX1001 at 24:53–59, 29:62–67; EX1005 at Abstract.

Step [10.2]

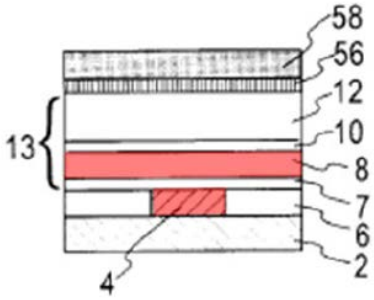
[10.2] a) forming a first insulating film over lower-level metal interconnects;

Fig. 24(a)



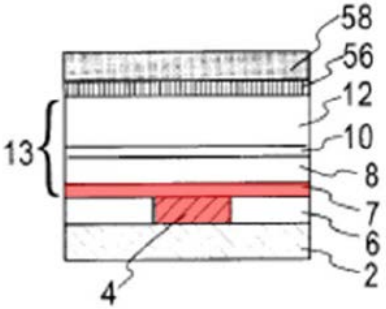
'696 patent at FIG. 24(a)

Fig. 5A



Grill at Fig. 5A (IPR2016-01377)

Fig. 5A



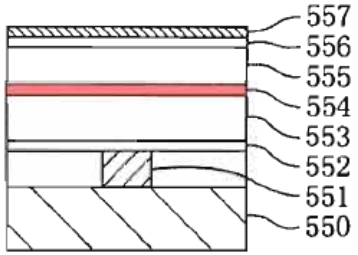
Grill at Fig. 5A (IPR2016-01379)

IPR2016-01377, EX1002 at ¶55; IPR2016-01377, Paper 2, at 44, 60–61; IPR2016-01379, EX1002 at ¶55; IPR2016-01379, Paper 2, at 38, 59–60.

Step [10.3]

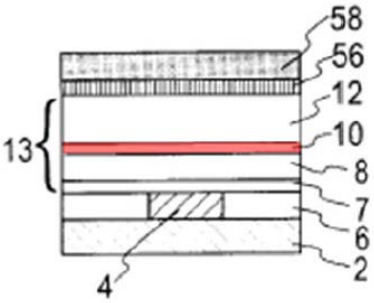
[10.3] b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

Fig. 24(a)



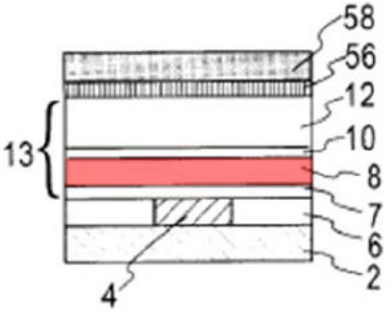
'696 patent at FIG. 24(a)

Fig. 5A



Grill at Fig. 5A (IPR2016-01377)

Fig. 5A



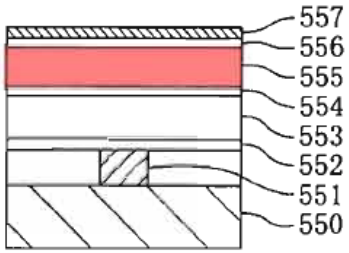
Grill at Fig. 5A (IPR2016-01379)

IPR2016-01377, EX1002 at ¶61; IPR2016-01377, Paper 2, at 45, 60–61; IPR2016-01379, EX1002 at ¶61; IPR2016-01379, Paper 2, at 40, 59–60.

Step [10.4]

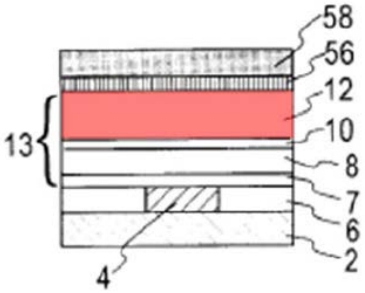
[10.4] c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

Fig. 24(a)



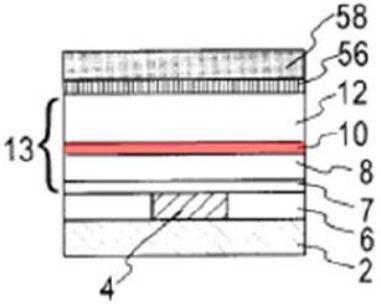
'696 patent at FIG. 24(a)

Fig. 5A



Grill at Fig. 5A (IPR2016-01377)

Fig. 5A



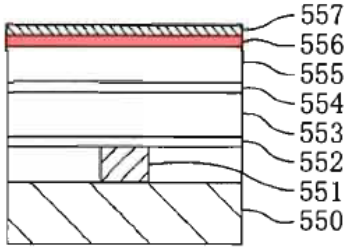
Grill at Fig. 5A (IPR2016-01379)

IPR2016-01377, EX1002 at ¶67; IPR2016-01377, Paper 2, at 46, 60–61; IPR2016-01379, EX1002 at ¶67; IPR2016-01379, Paper 2, at 41, 59–60.

Step [10.5]

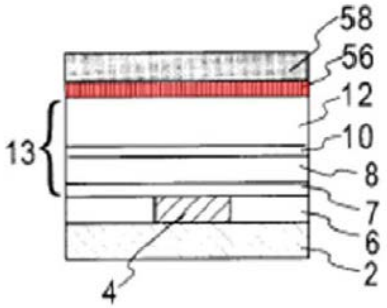
[10.5] d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film;

Fig. 24(a)



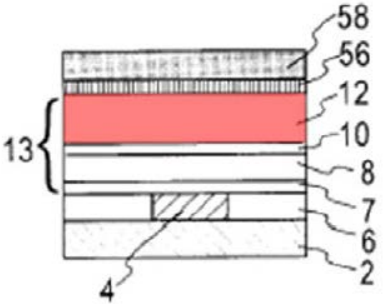
'696 patent at FIG. 24(a)

Fig. 5A



Grill at Fig. 5A (IPR2016-01377)

Fig. 5A



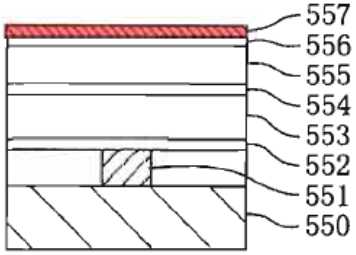
Grill at Fig. 5A (IPR2016-01379)

IPR2016-01377, EX1002 at ¶73; IPR2016-01377, Paper 2, at 48, 60–61; IPR2016-01379, EX1002 at ¶73; IPR2016-01379, Paper 2, at 42, 59–60.

Step [10.6]

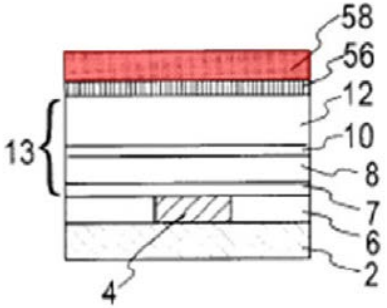
[10.6] e) forming a thin film over the fourth insulating film;

Fig. 24(a)



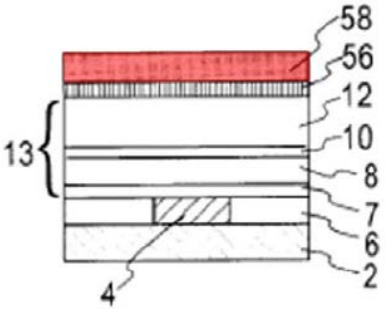
'696 patent at FIG. 24(a)

Fig. 5A



Grill at Fig. 5A (IPR2016-01377)

Fig. 5A



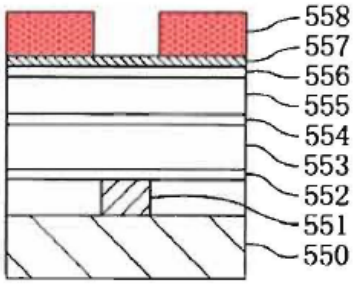
Grill at Fig. 5A (IPR2016-01379)

IPR2016-01377, EX1002 at ¶79; IPR2016-01377, Paper 2, at 48, 60–61; IPR2016-01379, EX1002 at ¶79; IPR2016-01379, Paper 2, at 43, 59–60.

Step [10.7]

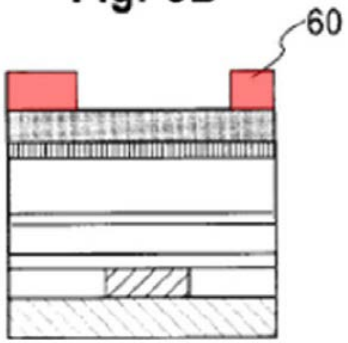
[10.7] f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

Fig. 24(b)



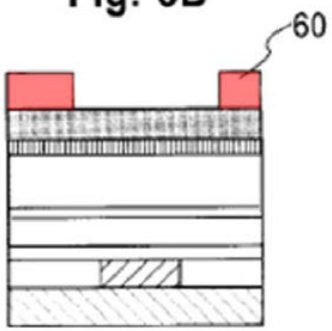
'696 patent at FIG. 24(b)

Fig. 5B



Grill at Fig. 5B (IPR2016-01377)

Fig. 5B



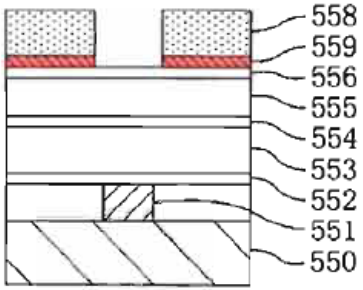
Grill at Fig. 5B (IPR2016-01379)

IPR2016-01377, EX1002 at ¶85; IPR2016-01377, Paper 2, at 61; IPR2016-01379, EX1002 at ¶85; IPR2016-01379, Paper 2, at 61.

Step [10.8]

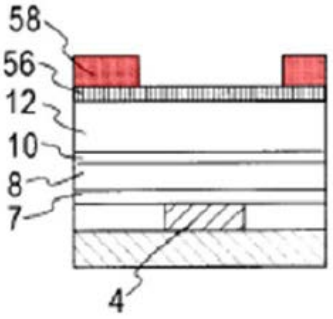
[10.8] g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

Fig. 24(c)



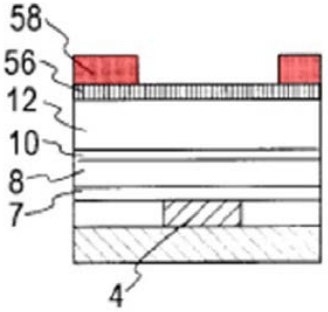
'696 patent at FIG. 24(c)

Fig. 5C



Grill at Fig. 5C (IPR2016-01377)

Fig. 5C



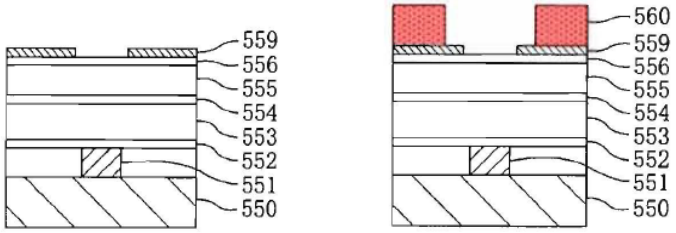
Grill at Fig. 5C (IPR2016-01379)

IPR2016-01377, EX1002 at ¶91; IPR2016-01377, Paper 2, at 62; IPR2016-01379, EX1002 at ¶91; IPR2016-01379, Paper 2, at 61.

Step [10.9]

[10.9]

h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;



'696 patent at FIGS. 25(a), 25(b)

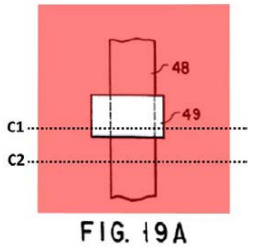
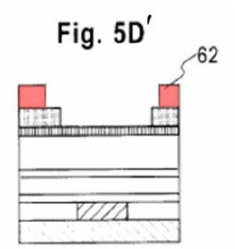
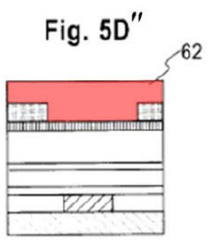


FIG. 19A





Petition at 63 (IPR2016-01377)

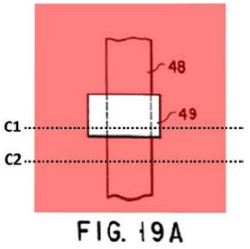
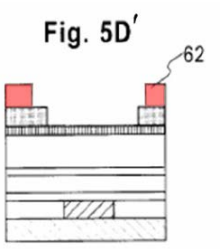
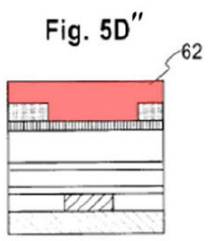


FIG. 19A





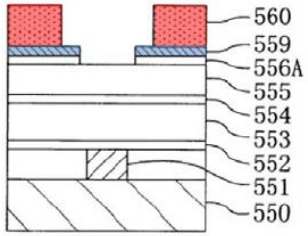
Petition at 63 (IPR2016-01379)

IPR2016-01377, EX1002 at ¶97; IPR2016-01377, Paper 2, at 63; IPR2016-01379, EX1002 at ¶97; IPR2016-01379, Paper 2, at 63.

Step [10.10]

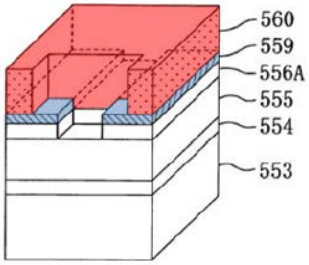
[10.10] i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes;

Fig. 25(c)



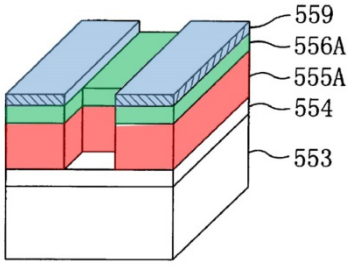
'696 patent at FIG. 25(c)

Fig. 27(b)



'696 patent at FIG. 27(b)

Fig. 28(a)



'696 patent at FIG. 28(a)

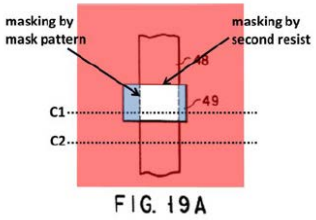


FIG. 19A

Fig. 5E′

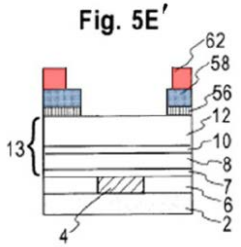
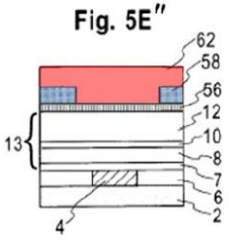


Fig. 5E″



Petition at 65 (IPR2016-01377)

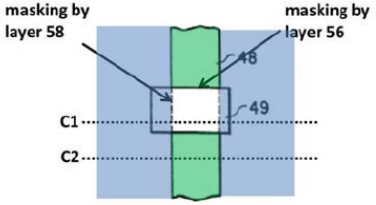


FIG. 19A

Fig. 5F′

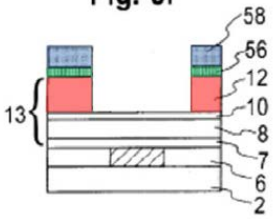
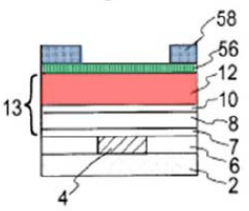


Fig. 5F″



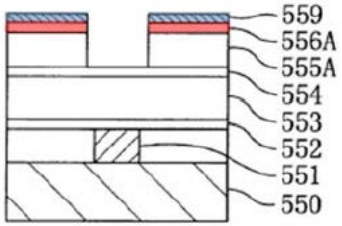
Petition at 65 (IPR2016-01379)

IPR2016-01377, EX1002 at ¶103; IPR2016-01377, Paper 2, at 65–66; IPR2016-01379, EX1002 at ¶103; IPR2016-01379, Paper 2, at 65.

Step [10.11]

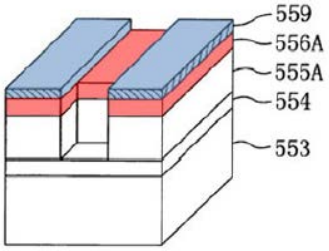
[10.11] j) dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;

Fig. 26(a)



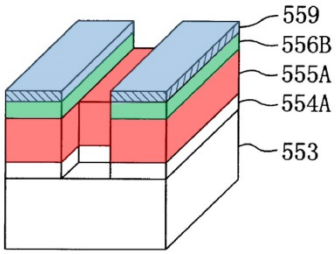
'696 patent at FIG. 26(a)

Fig. 28(a)



'696 patent at FIG. 28(a)

Fig. 28(b)



'696 patent at FIG. 28(b)

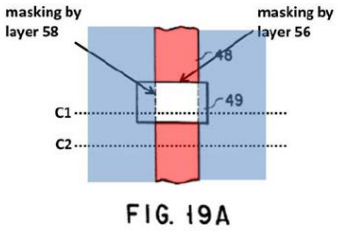


FIG. 19A

Fig. 5F′

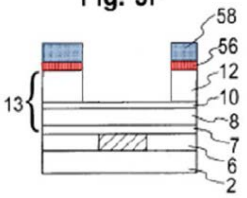
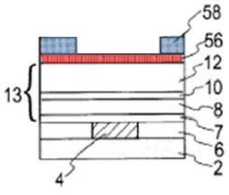


Fig. 5F″



Petition at 67 (IPR2016-01377)

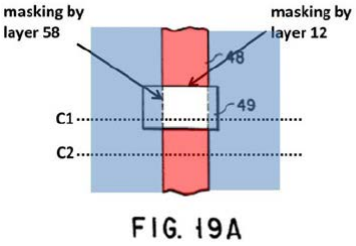


FIG. 19A

Fig. 5G′

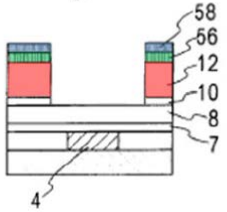
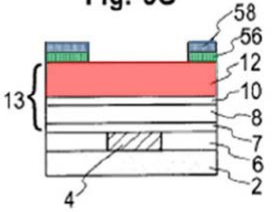


Fig. 5G″



Petition at 67 (IPR2016-01379)

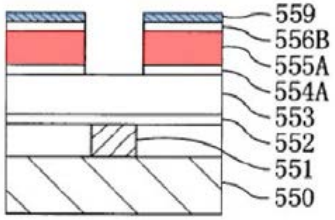
IPR2016-01377, EX1002 at ¶109; IPR2016-01377, Paper 2, at 67; IPR2016-01379, EX1002 at ¶109; IPR2016-01379, Paper 2, at 67.

Step [10.12]

[10.12]

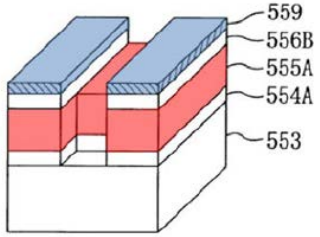
k) dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes;

Fig. 26 (b)



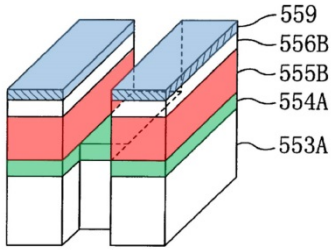
'696 patent at FIG. 26(b)

Fig. 28 (b)



'696 patent at FIG. 28(b)

Fig. 29 (a)



'696 patent at FIG. 29(a)

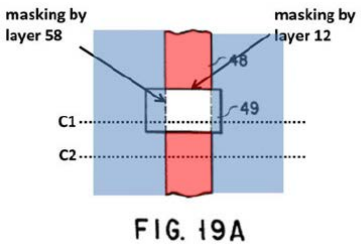


FIG. 19A

Fig. 5G′

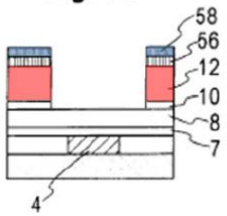
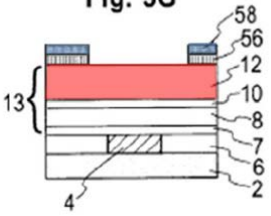


Fig. 5G″



Petition at 69 (IPR2016-01377)

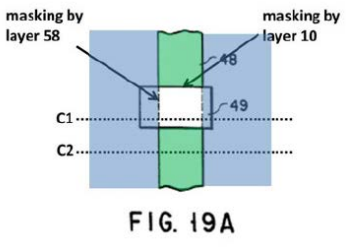


FIG. 19A

Fig. 5H′

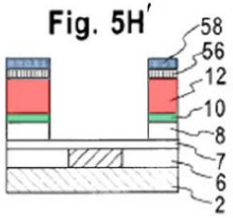
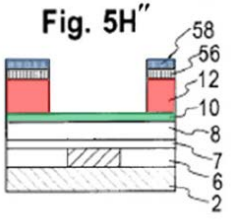


Fig. 5H″



Petition at 70 (IPR2016-01379)

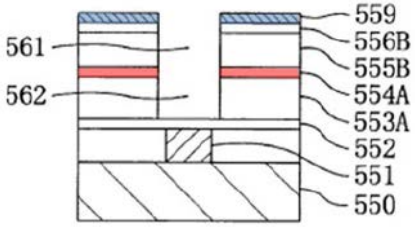
IPR2016-01377, EX1002 at ¶115; IPR2016-01377, Paper 2, at 69; IPR2016-01379, EX1002 at ¶115; IPR2016-01379, Paper 2, at 70.

Step [10.13]

[10.13]

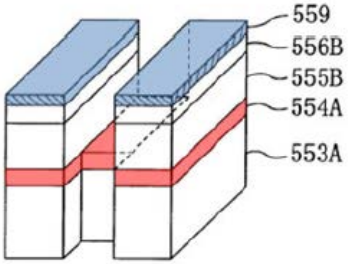
l) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively; and

Fig. 26(c)



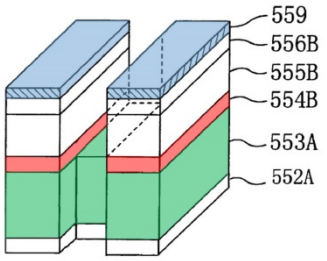
'696 patent at FIG. 26(c)

Fig. 29(a)



'696 patent at FIG. 29(a)

Fig. 29(a)'



'696 patent at FIG. 29(a)'

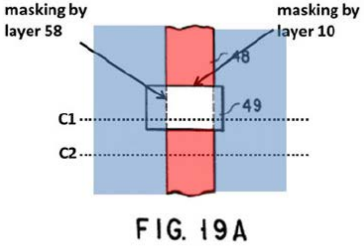


FIG. 19A

Fig. 5H'

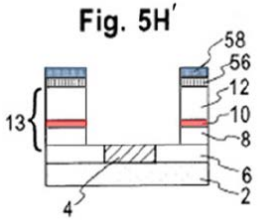
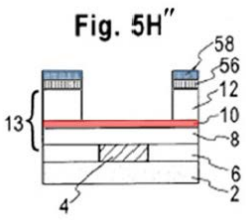


Fig. 5H''



Petition at 71 (IPR2016-01377)

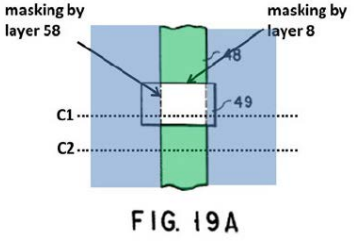


FIG. 19A

Fig. 1J'

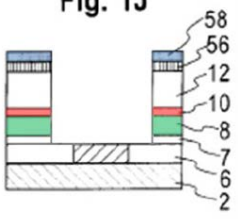
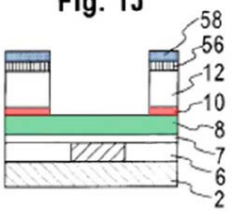


Fig. 1J''



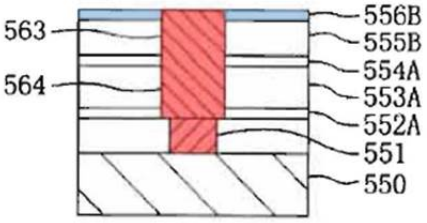
Petition at 73 (IPR2016-01379)

IPR2016-01377, EX1002 at ¶121; IPR2016-01377, Paper 2, at 71; IPR2016-01379, EX1002 at ¶121; IPR2016-01379, Paper 2, at 73.

Step [10.14]

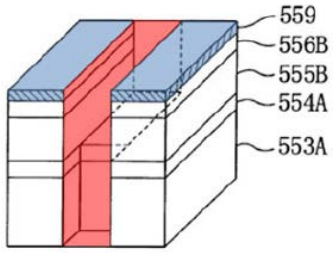
[10.14] m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

Fig. 26(d)



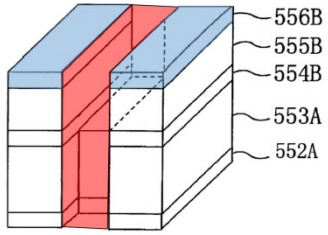
'696 patent at FIG. 26(d)

Fig. 29(a)



'696 patent at FIG. 29(a)

Fig. 29(a)′



'696 patent at FIG. 29(a)'

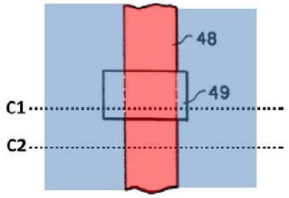


FIG. 19A

Fig. 1L′

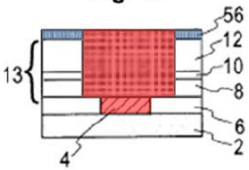
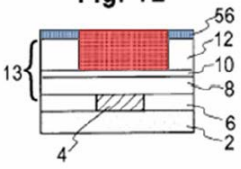


Fig. 1L″



Petition at 72 (IPR2016-01377)

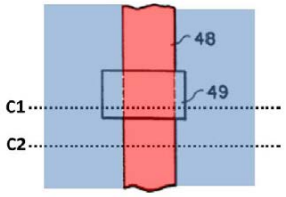


FIG. 19A

Fig. 1L′

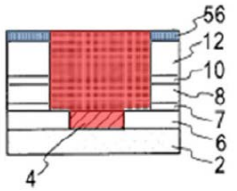
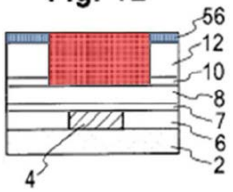


Fig. 1L″



Petition at 75 (IPR2016-01379)

IPR2016-01377, EX1002 at ¶127; IPR2016-01377, Paper 2, at 72–73; IPR2016-01379, EX1002 at ¶127; IPR2016-01379, Paper 2, at 75.

Claim 11

[11.1] **11**. The method of claim **10**, wherein at least one of the first and third insulating films is mainly composed of an organic component.

First, as shown in FIG. **24**(*a*), a silicon nitride film **552** is formed over first metal interconnects **551** formed on a semiconductor substrate **550**. The silicon nitride film **552** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **551** during a subsequent etching process step. Thereafter, a first organic film **553** (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film **552**. Then, a first silicon dioxide film **554** (second insulating film) is formed to be 100 nm thick, for example, on the first organic film **553**. Subsequently, a second organic film **555** (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the first silicon dioxide film **554**. Next, a second silicon dioxide film **556** (fourth insulating film) is deposited to be 200 nm thick, for example, on the second organic film **555**. And a titanium nitride film **557** is deposited to be 50 nm thick, for example, on the second silicon dioxide film **556**.

'696 patent at 24:60–25:11

A layered dielectric stack **13** comprising an optional dielectric passivation/adhesion layer **7**, a via level dielectric **8**, an optional dielectric etch stop layer **10**, and a wiring level dielectric **12** are then applied to produce the structure of FIG. **1B**. Via and wiring dielectrics **8** and **12** might be carbon-based materials such as DLC or fluorinated DLC (FDLC), SiCO or SiCOH compounds, or organic or inorganic polymer dielectrics, and optional dielectric etch stop **10** might be a silicon-containing material such as SiO2, Si3N4, SiOxNy, SiCOH compounds, silicon-containing DLC (SiDLC), etc. The total thickness of layered dielectric stack **13** closely approximates the sum of the via and wiring level thicknesses.

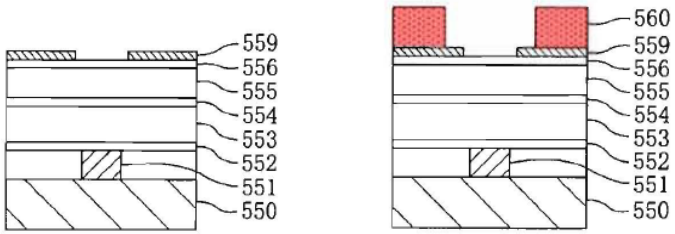
Grill at 4:1–13

IPR2016-01377

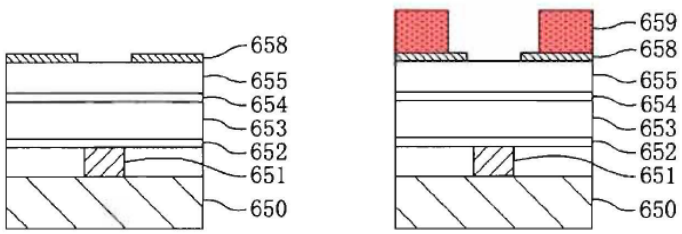
IPR2016-01377, EX1001 at 24:60–25:11; IPR2016-01377, EX1005 at 4:1–13.

Claim 12

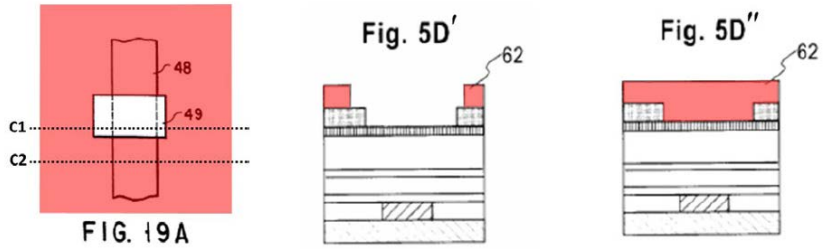
[12.1] **12**. The method of claim **10**, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.



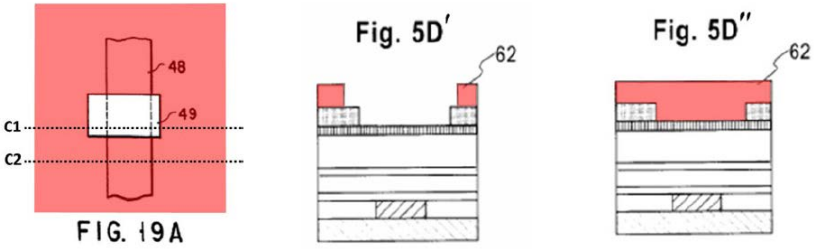
'696 patent at FIGS. 25(a), 25(b)



'696 patent at FIGS. 34(a), 34(b)



Petition at 63 (IPR2016-01377)



Petition at 63 (IPR2016-01379)

IPR2016-01377, EX1002 at ¶97; IPR2016-01377, Paper 2, at 63; IPR2016-01379, EX1002 at ¶97; IPR2016-01379, Paper 2, at 63.

Claim 13

[13.1] 13. A method for forming an interconnection structure, comprising the steps of:

[13.2] a) forming a first insulating film over lower-level metal interconnects;

[13.3] b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

[13.4] c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

[13.5] d) forming a thin film over the third insulating film;

[13.6] e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

[13.7] f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

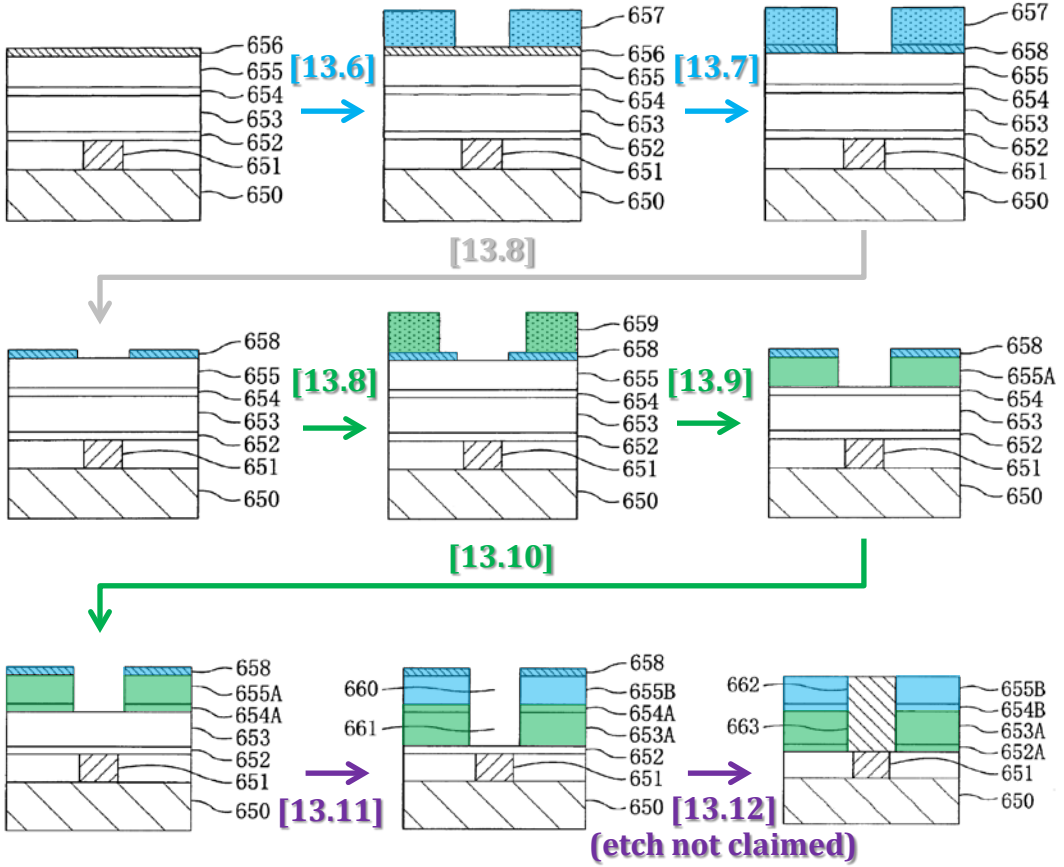
[13.8] g) removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;

[13.9] h) dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;

[13.10] i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes;

[13.11] j) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and

[13.12] k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.



EX1001 at 34:58–36:10, FIGS. 33(a) –35(c).

Step [13.1]

[13.1] **13**. A method for forming an interconnection structure, comprising the steps of:

MODIFIED EXAMPLE OF EMBODIMENT 5

Next, a method for forming an interconnection structure according to a modified example of the fifth embodiment will be described with reference to FIGS. **24**(*a*) through **24**(*c*), FIGS. **25**(*a*) through **25**(*c*), FIGS. **26**(*a*) through **26**(*d*), FIGS. **27**(*a*) and **27**(*b*), FIGS. **28**(*a*) and **28**(*b*) and FIGS. **29**(*a*) and **29**(*b*).

'696 patent at 24:53–59

MODIFIED EXAMPLE OF EMBODIMENT 6

Next, a method for forming an interconnection structure according to a modified example of the sixth embodiment will be described with reference to FIGS. **33**(*a*) through **33**(*c*), FIGS. **34**(*a*) through **34**(*c*) and FIGS. **35**(*a*) through **35**(*c*).

'696 patent at 29:62–67

[57] **ABSTRACT**

The present invention relates to lithographic methods for forming a dual relief pattern in a substrate, and the application of such methods to fabricating multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels.

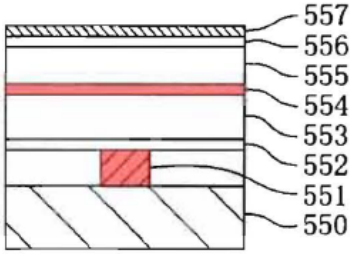
Grill at Abstract

EX1001 at 24:53–59, 29:62–67; EX1005 at Abstract.

Step [13.2]

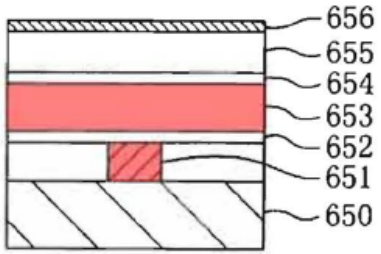
[13.2] a) forming a first insulating film over lower-level metal interconnects;

Fig. 24(a)



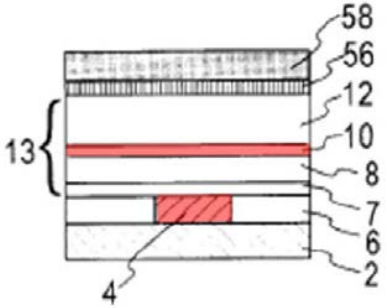
'696 patent at FIG. 24(a)

Fig. 33(a)



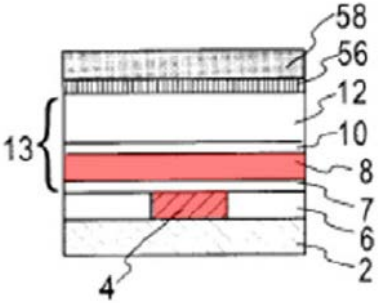
'696 patent at FIG. 33(a)

Fig. 5A



Grill at Fig. 5A (IPR2016-01376)

Fig. 5A



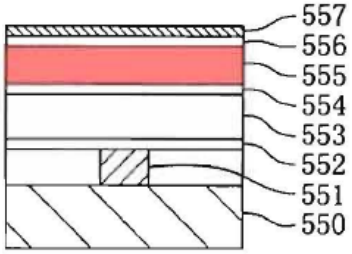
Grill at Fig. 5A (IPR2016-01378)

IPR2016-01376, EX1002 at ¶55; IPR2016-01376, Paper 2, at 38, 57–58; IPR2016-01378, EX1002 at ¶55; IPR2016-01378, Paper 2, at 32, 50–51.

Step [13.3]

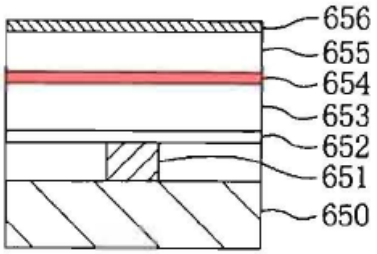
[13.3] b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

Fig. 24(a)



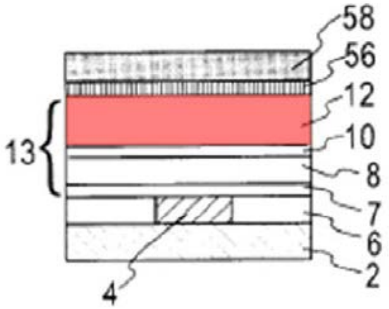
'696 patent at FIG. 24(a)

Fig. 33(a)



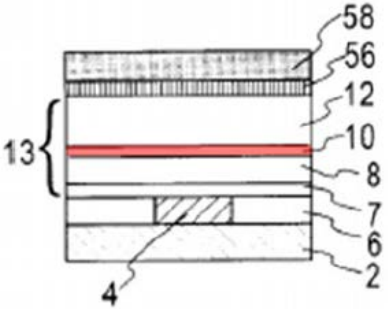
'696 patent at FIG. 33(a)

Fig. 5A



Grill at Fig. 5A (IPR2016-01376)

Fig. 5A



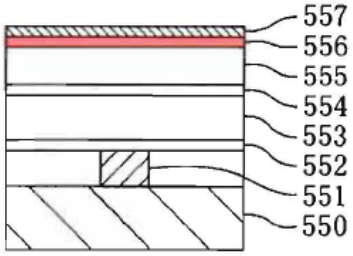
Grill at Fig. 5A (IPR2016-01378)

IPR2016-01376, EX1002 at ¶61; IPR2016-01376, Paper 2, at 39, 57–58; IPR2016-01378, EX1002 at ¶61; IPR2016-01378, Paper 2, at 33, 50–51.

Step [13.4]

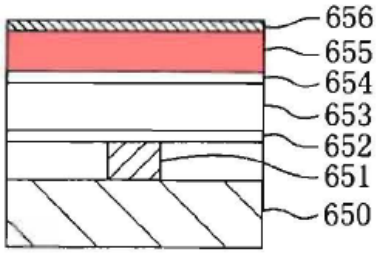
[13.4] c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

Fig. 24(a)



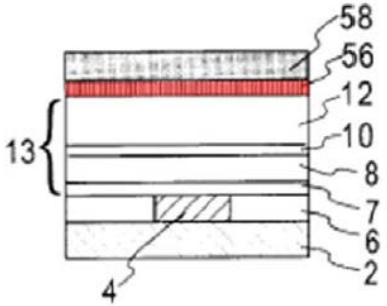
'696 patent at FIG. 24(a)

Fig. 33(a)



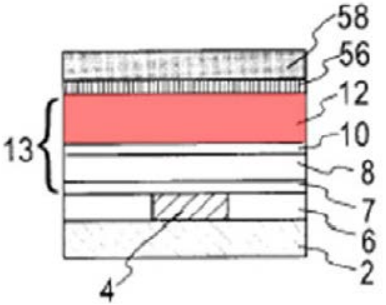
'696 patent at FIG. 33(a)

Fig. 5A



Grill at Fig. 5A (IPR2016-01376)

Fig. 5A



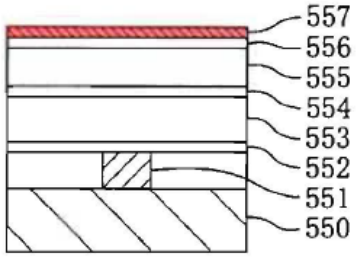
Grill at Fig. 5A (IPR2016-01378)

IPR2016-01376, EX1002 at ¶67; IPR2016-01376, Paper 2, at 40, 57–58; IPR2016-01378, EX1002 at ¶67; IPR2016-01378, Paper 2, at 34, 50–51.

Step [13.5]

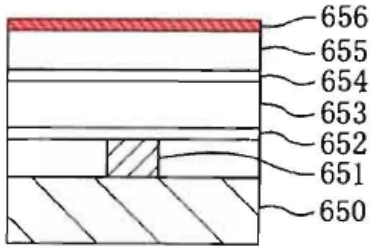
[13.5] d) forming a thin film over the third insulating film;

Fig. 24(a)



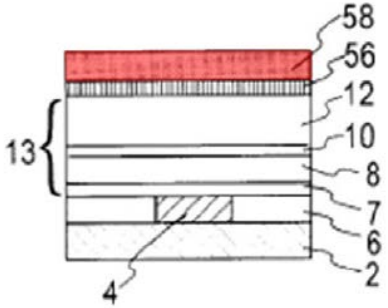
'696 patent at FIG. 24(a)

Fig. 33(a)



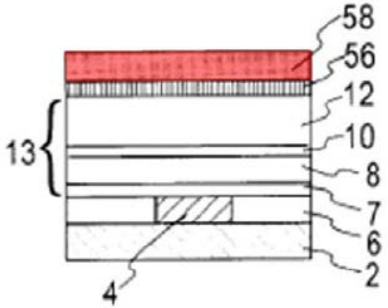
'696 patent at FIG. 33(a)

Fig. 5A



Grill at Fig. 5A (IPR2016-01376)

Fig. 5A



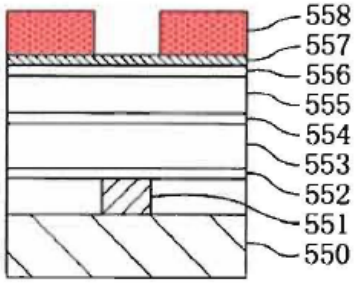
Grill at Fig. 5A (IPR2016-01378)

IPR2016-01376, EX1002 at ¶73; IPR2016-01376, Paper 2, at 41, 57–58; IPR2016-01378, EX1002 at ¶73; IPR2016-01378, Paper 2, at 35, 50–51.

Step [13.6]

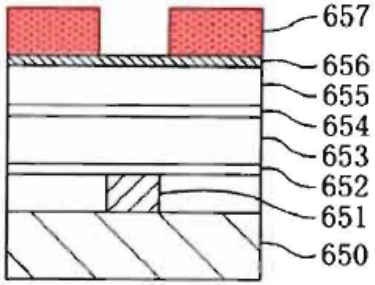
[13.6] e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

Fig. 24(b)



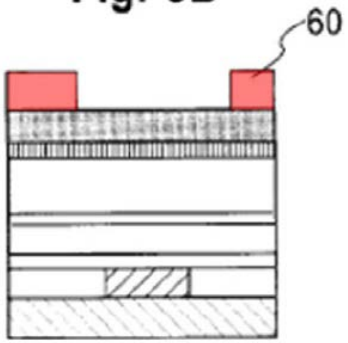
'696 patent at FIG. 24(b)

Fig. 33(b)



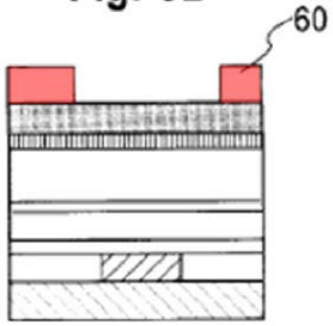
'696 patent at FIG. 33(b)

Fig. 5B



Grill at Fig. 5B (IPR2016-01376)

Fig. 5B



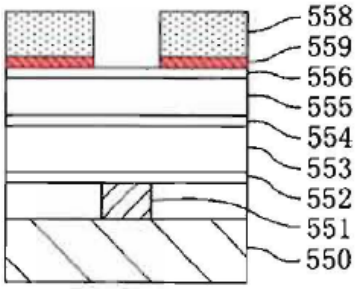
Grill at Fig. 5B (IPR2016-01378)

IPR2016-01376, EX1002 at ¶79; IPR2016-01376, Paper 2, at 58; IPR2016-01378, EX1002 at ¶79; IPR2016-01378, Paper 2, at 51.

Step [13.7]

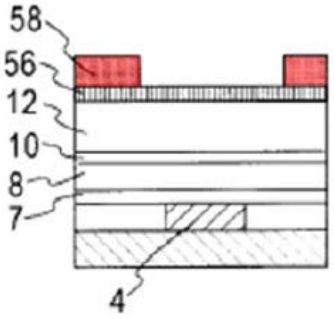
[13.7] f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

Fig. 24(c)



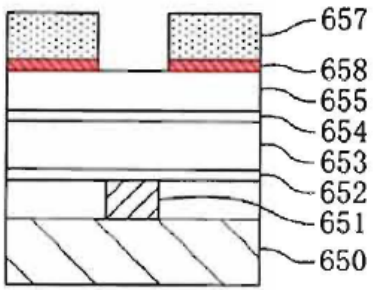
'696 patent at FIG. 24(c)

Fig. 5C



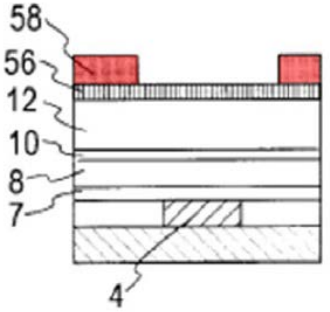
Grill at Fig. 5C (IPR2016-01376)

Fig. 33(c)



'696 patent at FIG. 33(c)

Fig. 5C

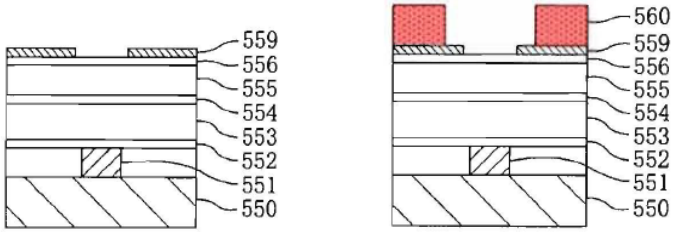


Grill at Fig. 5C (IPR2016-01378)

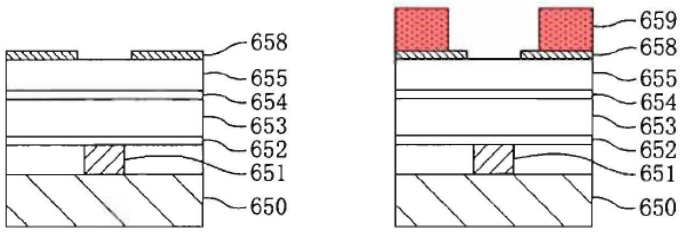
IPR2016-01376, EX1002 at ¶85; IPR2016-01376, Paper 2, at 59; IPR2016-01378, EX1002 at ¶85; IPR2016-01378, Paper 2, at 52.

Step [13.8]

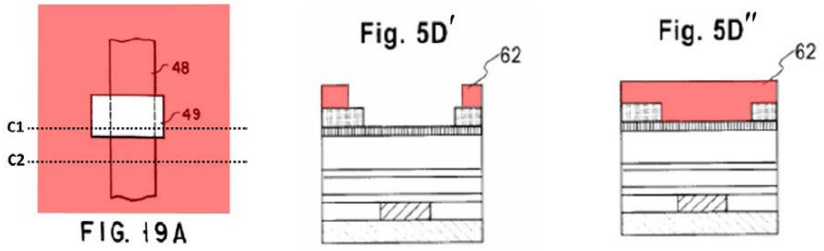
[13.8] g) removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;



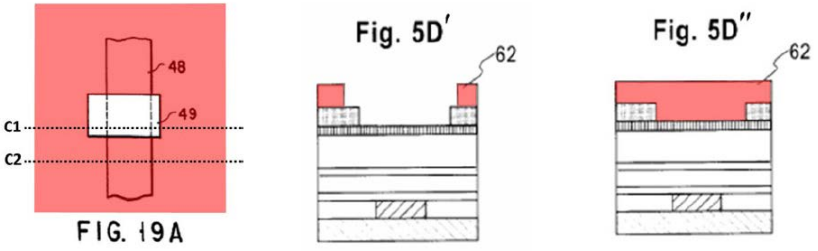
'696 patent at FIGS. 25(a), 25(b)



'696 patent at FIGS. 34(a), 34(b)



Petition at 61 (IPR2016-01376)



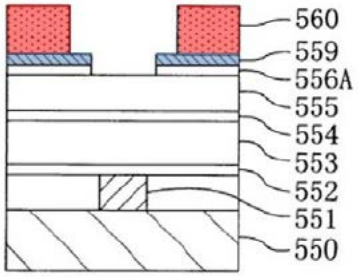
Petition at 53 (IPR2016-01378)

IPR2016-01376, EX1002 at ¶91; IPR2016-01376, Paper 2, at 61; IPR2016-01378, EX1002 at ¶91; IPR2016-01378, Paper 2, at 53.

Step [13.9]

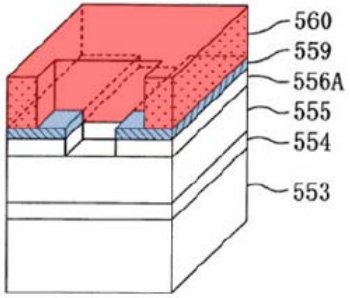
[13.9] h) dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;

Fig. 25(c)



'696 patent at FIG. 25(c)

Fig. 27(b)



'696 patent at FIG. 27(b)

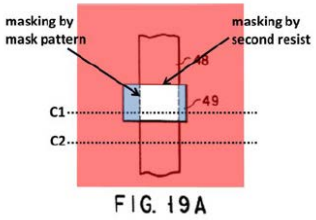
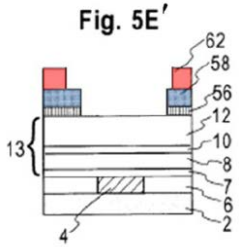
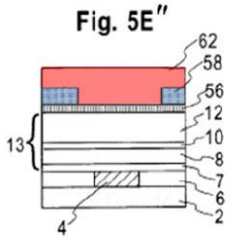


FIG. 19A





Petition at 62 (IPR2016-01376)

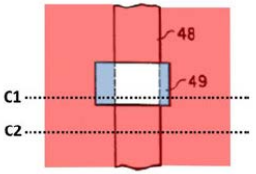
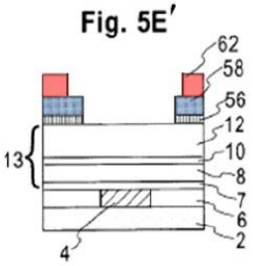
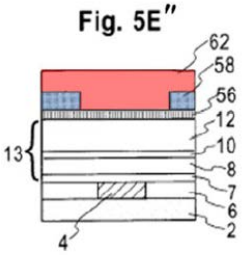


FIG. 19A





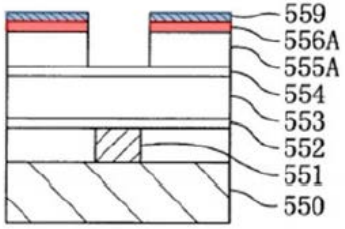
Petition at 55 (IPR2016-01378)

IPR2016-01376, EX1002 at ¶97; IPR2016-01376, Paper 2, at 62–63; IPR2016-01378, EX1002 at ¶97; IPR2016-01378, Paper 2, at 55.

Step [13.10]

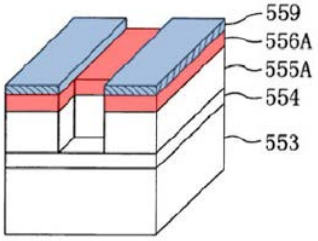
[13.10] i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes;

Fig. 26(a)



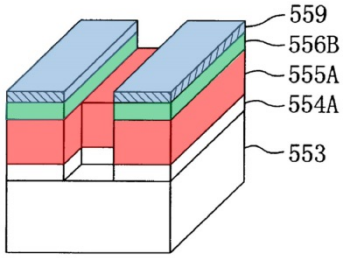
'696 patent at FIG. 26(a)

Fig. 28(a)



'696 patent at FIG. 28(a)

Fig. 28(b)



'696 patent at FIG. 28(b)

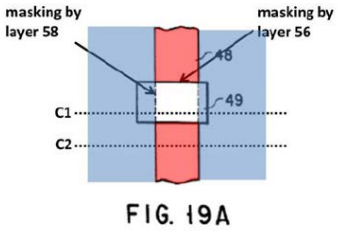


FIG. 19A

Fig. 5F′

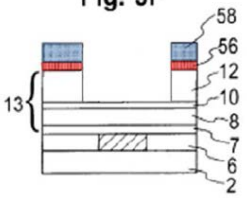
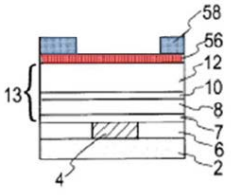


Fig. 5F″



Petition at 64 (IPR2016-01376)

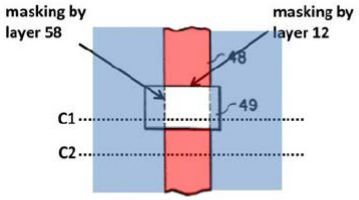


FIG. 19A

Fig. 5G′

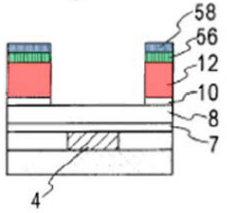
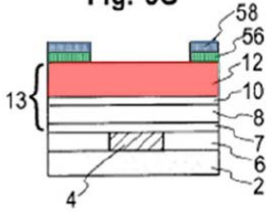


Fig. 5G″



Petition at 58 (IPR2016-01378)

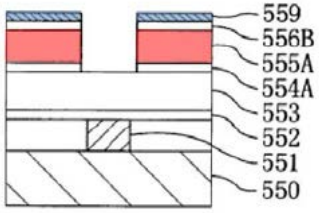
IPR2016-01376, EX1002 at ¶103; IPR2016-01376, Paper 2, at 64–65; IPR2016-01378, EX1002 at ¶103; IPR2016-01378, Paper 2, at 58.

Step [13.11]

[13.11]

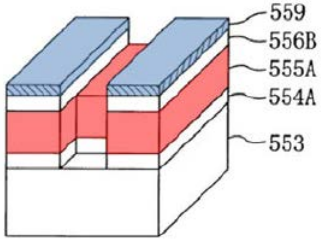
j) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and

Fig. 26 (b)



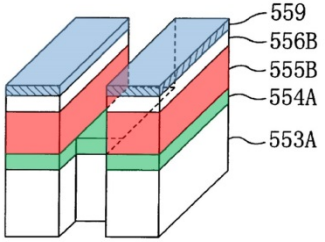
'696 patent at FIG. 26(b)

Fig. 28 (b)



'696 patent at FIG. 28(b)

Fig. 29 (a)



'696 patent at FIG. 29(a)

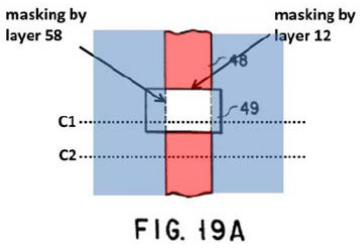


FIG. 19A

Fig. 5G′

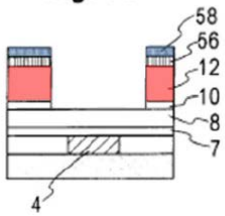
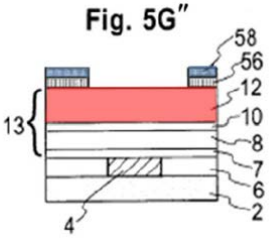


Fig. 5G″



Petition at 66 (IPR2016-01376)

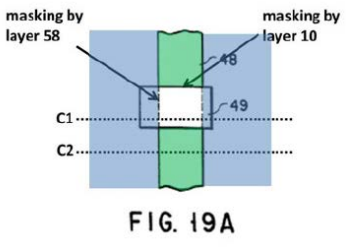


FIG. 19A

Fig. 5H′

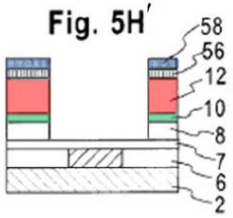
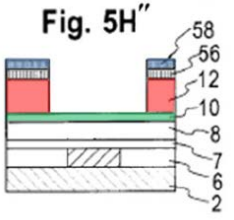


Fig. 5H″



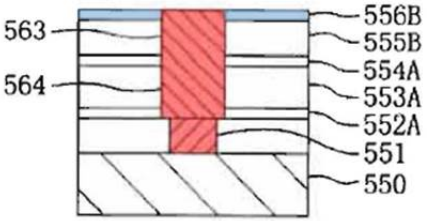
Petition at 60 (IPR2016-01378)

IPR2016-01376, EX1002 at ¶109; IPR2016-01376, Paper 2, at 66–67; IPR2016-01378, EX1002 at ¶109; IPR2016-01378, Paper 2, at 60.

Step [13.12]

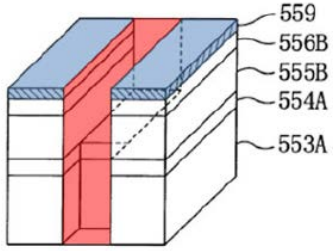
[13.12] k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

Fig. 26(d)



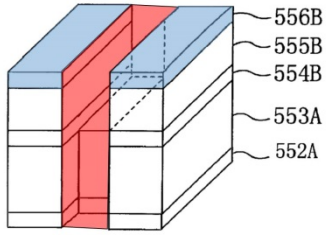
'696 patent at FIG. 26(d)

Fig. 29(a)



'696 patent at FIG. 29(a)

Fig. 29(a)′



'696 patent at FIG. 29(a)'

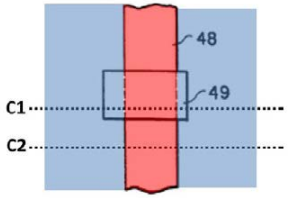


FIG. 19A

Fig. 1L′

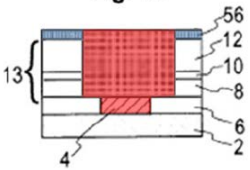
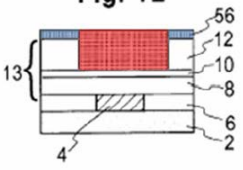


Fig. 1L″



Petition at 69 (IPR2016-01376)

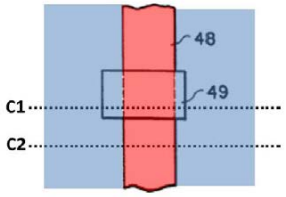


FIG. 19A

Fig. 1L′

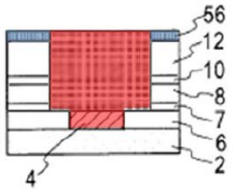
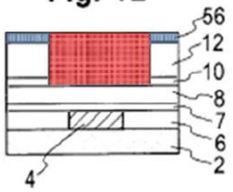


Fig. 1L″



Petition at 62 (IPR2016-01378)

IPR2016-01376, EX1002 at ¶115; IPR2016-01376, Paper 2, at 69–70; IPR2016-01378, EX1002 at ¶115; IPR2016-01378, Paper 2, at 62.

Claim 14

[14.1] **14**. The method of claim **13**, wherein at least one of the first and third insulating films is mainly composed of an organic component.

First, as shown in FIG. **33**(*a*), a silicon nitride film **652** is formed over first metal interconnects **651** formed on a semiconductor substrate **650**. The silicon nitride film **652** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **651** during a subsequent etching process step. Thereafter, a first organic film **653** (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film **652**. Then, a silicon dioxide film **654** (second insulating film) is deposited to be 100 nm thick, for example, on the first organic film **653**. Subsequently, a second organic film **655** (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the silicon dioxide film **654**. And a titanium nitride film **656** (thin film) is deposited to be 50 nm thick, for example, on the second organic film **655**.

'696 patent at 30:1–16

A layered dielectric stack **13** comprising an optional dielectric passivation/adhesion layer **7**, a via level dielectric **8**, an optional dielectric etch stop layer **10**, and a wiring level dielectric **12** are then applied to produce the structure of FIG. 1B. Via and wiring dielectrics **8** and **12** might be carbon-based materials such as DLC or fluorinated DLC (FDLC), SiCO or SiCOH compounds, or organic or inorganic polymer dielectrics, and optional dielectric etch stop **10** might be a silicon-containing material such as SiO2, Si3N4, SiOxNy, SiCOH compounds, silicon-containing DLC (SiDLC), etc. The total thickness of layered dielectric stack **13** closely approximates the sum of the via and wiring level thicknesses.

Grill at 4:1–13

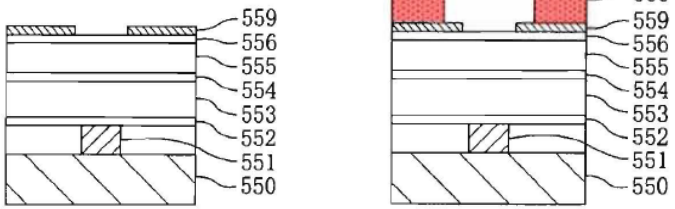
IPR2016-01378

IPR2016-01378, EX1001 at 30:1–16; IPR2016-01378, EX1005 at 4:1–13.

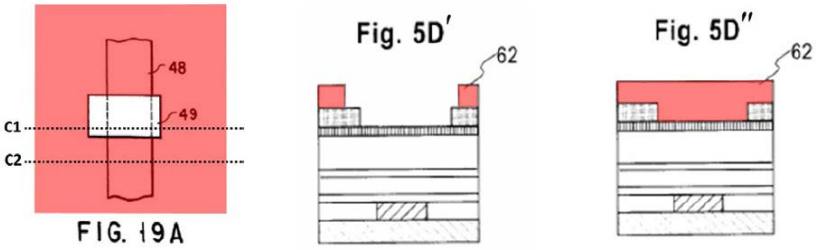
Claim 15

[15.1]

15. The method of claim **13**, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.



'696 patent at FIGS. 25(a), 25(b)



Petition at 61 (IPR2016-01376)

IPR2016-01376

IPR2016-01376, EX1002 at ¶91; IPR2016-01376, Paper 2, at 61.

Independent Claim 10 of the '696 Patent

[10.1] **10**. A method for forming an interconnection structure, comprising the steps of:

[10.2] a) forming a first insulating film over lower-level metal interconnects;

[10.3] b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

[10.4] c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

[10.5] d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film;

[10.6] e) forming a thin film over the fourth insulating film;

[10.7] f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

[10.8] g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

[10.9] h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;

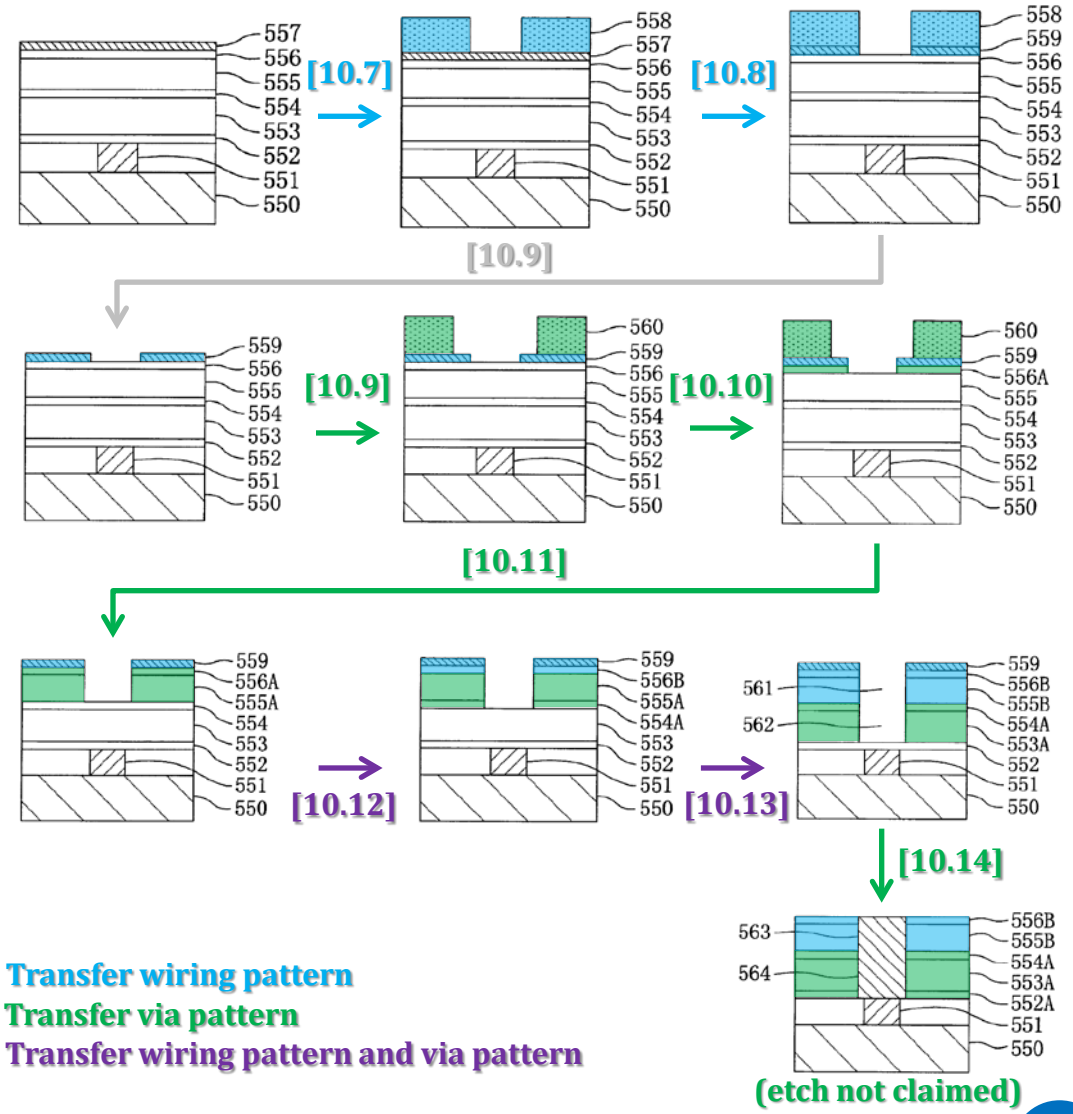
[10.10] i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes;

[10.11] j) dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;

[10.12] k) dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes;

[10.13] l) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively; and

[10.14] m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.



EX1001 at 34:1–49, FIGS. 24(a) –29(b).

Support for Grill's Claim 28

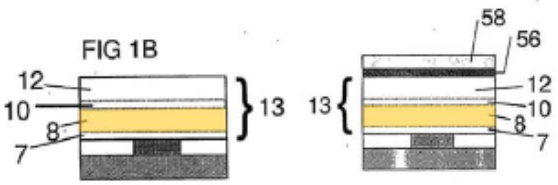
Grill's Provisional Parent Supports Grill's Claim 28

28. A method for forming an interconnect structure on the upper surface of a **substrate** having conductive regions comprising the steps of:	"Figs. 5A-5E show a first preferred embodiment of a method for forming a dual pattern hard mask comprising a first layer of material with a first pattern, and a second layer of material with a second pattern; Figs. 5F-5H show how this dual pattern hard mask may be used to fabricate a dual relief cavity for use in a Dual Damascene process. For purposes of illustration, one of said first and second patterns will be a via level pattern, and the other of said first and second patterns will be a wiring level pattern." EX1048 at 15:3-8.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

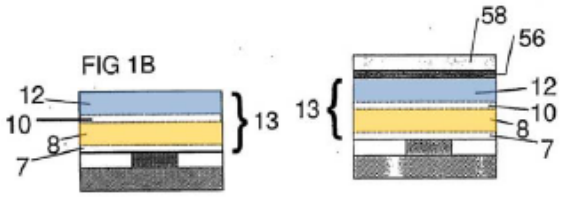
Grill's Provisional Parent Supports Grill's Claim 28

forming over said substrate a first dielectric layer having a thickness corresponding to the thickness of an interconnect via,	FIG 5A FIG 1B  **'628 application at FIGS. 1B, 5A** "The process flow may be exercised on a variety of substrates but is illustrated for the simplified substrate of Fig. 1A which comprises a semiconductor base 2 containing arrays of electrical devices (not shown), conductive via 4, and dielectric passivation layer 6. "A layered dielectric stack 13 comprising an optional dielectric passivation/adhesion layer 7, a via level dielectric 8, an optional dielectric etch stop layer 10, and a wiring level dielectric 12 are then applied to produce the structure of Fig. 1B. Via and wiring dielectrics 8 and 12 might be carbon-based materials such as DLC or fluorinated DLC (FDLC), and optional dielectric etch stop 10 may be materials such as SiO2, Si3N4, silicon-containing DLC (SiDLC), etc. **The total thickness of layered dielectric stack 13 closely approximates the sum of the via and wiring level thickness.**" EX1048 at 12:35-40. *See also* EX1048 at 15:11-12 ("Fig. 5A shows the structure of Fig. 1B after application of lower hard mask layer 56 and upper hard mask layer 58.").

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

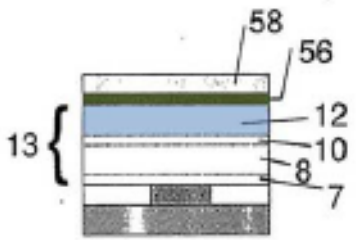
Grill's Provisional Parent Supports Grill's Claim 28

forming over said first dielectric layer a second dielectric layer having a thickness corresponding to the thickness of an interconnect wiring layer,	FIG 5A  **'628 application at FIGS. 1B, 5A** "The process flow may be exercised on a variety of substrates but is illustrated for the simplified substrate of Fig. 1A which comprises a semiconductor base 2 containing arrays of electrical devices (not shown), conductive via 4, and dielectric passivation layer 6. "A layered dielectric stack 13 comprising an optional dielectric passivation/adhesion layer 7, a via level dielectric 8, an optional dielectric etch stop layer 10, and a wiring level dielectric 12 are then applied to produce the structure of Fig. 1B. Via and wiring dielectrics 8 and 12 might be carbon-based materials such as DLC or fluorinated DLC (FDLC), and optional dielectric etch stop 10 may be materials such as SiO2, Si3N4, silicon-containing DLC (SiDLC), etc. **The total thickness of layered dielectric stack 13 closely approximates the sum of the via and wiring level thickness.**" EX1048 at 12:31-40. *See also* EX1048 at 15:11-12 ("Fig. 5A shows the structure of Fig. 1B after application of lower hard mask layer 56 and upper hard mask layer 58.").

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

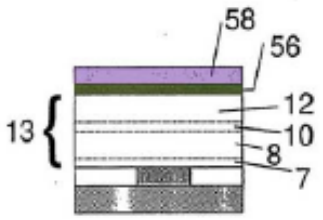
Grill's Provisional Parent Supports Grill's Claim 28

forming a first hard mask layer over said second [dielectric] layer,	FIG 5A  **'628 application at FIG. 5A** "Fig. 5A shows the structure of Fig. 1B after application of lower hard mask layer 56 and upper hard mask layer 58. Hard mask layers 56 and 58 are preferably formed from different materials which have different etch properties from each other and from dielectric underlayers 12 and 8." EX1048 at 15:11-13.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

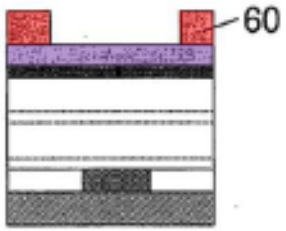
Grill's Provisional Parent Supports Grill's Claim 28

forming a **second hard mask layer** over said **first hard mask layer**, said **second hard mask layer** preferably formed of a material different from said **first hard mask** to permit selective etching of said **second hard mask layer** with respect to said **first hard mask layer**,	FIG 5A  **'628 application at FIG. 5A** "Fig. 5A shows the structure of Fig. 1B after application of **lower hard mask layer 56** and **upper hard mask layer 58**. Hard mask layers 56 and 58 are preferably formed from different materials which have different etch properties from each other and from dielectric underlayers 12 and 8. For example, **lower hard mask layer 56** might be formed from Si3N4 and **upper hard mask layer 58** might be formed from SiO2. . . . . The etching process is preferably selective, for example a selective SiO2 to Si3N4 etch, so that **lower hard mask layer 56** will remain intact during any overetching of **hard mask layer 58**." EX1048 at 15:11-22.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

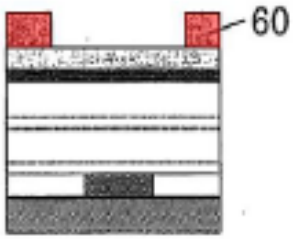
Grill's Provisional Parent Supports Grill's Claim 28

forming a first layer of resist over said second hard mask layer,	FIG 5B  **'628 application at FIG. 5B** "A first resist layer 60, patterned with a first (wiring level) pattern, is formed on layer 58 to form the structure of Fig. 5B." EX1048 at 15:17-18.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

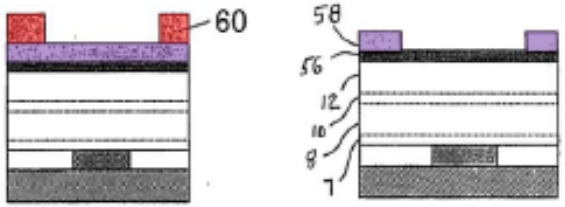
Grill's Provisional Parent Supports Grill's Claim 28

patterning said first layer of resist with a wiring pattern,	FIG 5B  **'628 application at FIG. 5B** **"A first resist layer 60, patterned with a first (wiring level) pattern, is formed on layer 58 to form the structure of Fig. 5B."** EX1048 at 15:17-18.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

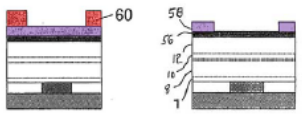
Grill's Provisional Parent Supports Grill's Claim 28

patterning said **second hard mask layer** using said wiring-patterned **first layer of resist** as a mask,	FIG 5B FIG 5C  **'628 application at FIGS. 5B, 5C** "The **pattern of resist layer 60** is transferred into **upper hard mask layer 58** by an etching process to form the structure of Fig. 5C. The etching process is preferably selective, for example a selective SiO2 to Si3N4 etch, so that lower hard mask layer 56 will remain intact during any overetching of **hard mask layer 58**." EX1048 at 15:19-22.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

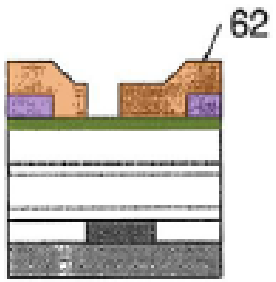
Grill's Provisional Parent Supports Grill's Claim 28

removing said wiring-patterned first layer of resist,	FIG 5B FIG 5C  **'628 application at FIGS. 5B, 5C** Although the *Grill* patent later added a statement that the "[p]atterned resist layer 60 is . . . removed by a process such as ashing or wet chemical etching," a person of ordinary skill in the art would have already understood this to be taught by the '628 application. The '628 application teaches that rework problems are caused when the photoresist and dielectric material have similar etch properties. EX1048 at 11:13-15 ("[D]ifficulties in reworking the second lithography step may occur if the interconnect dielectric and the photoresist stencil used to pattern the hard mask have similar etch characteristics. Such would be the case with an organic photoresist and a carbon-based interconnect dielectric such as DLC."). Accordingly, a person of ordinary skill in the art would have understood that resist rework is not a problem at this stage because the upper hard mask layer 58 and photoresist layer 60 have different etch properties. EX1048 at 15:12-19 ("Hard mask layers 56 and 58 are preferably formed from different materials which have different etch properties from each other and from the dielectric underlayers 12 and 8. . . . If resist layer 60 is misaligned, rework at this stage presents no problem."). A person of ordinary skill in the art thus would have understood that the photoresist layer 60 is removed after hard mask layer 58 is etched. A person of ordinary skill in the art would have understood that the transition between Figures 5B and 5C above occurs by first etching layer 58, and subsequently removing the remaining photoresist layer 60.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

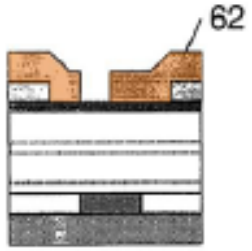
Grill's Provisional Parent Supports Grill's Claim 28

forming a second layer of resist over said first [hard mask layer] and second hard mask layer,	FIG 5D  **'628 application at FIG. 5D** "A second resist layer 62, patterned with a second (via level) pattern, is then formed on the structure of Fig. 5C to produce the structure of Fig. 5D." EX1048 at 15:23-24.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

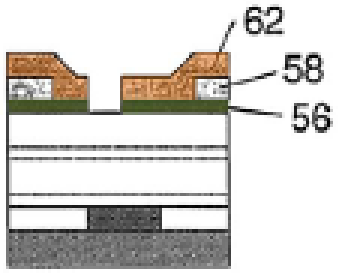
Grill's Provisional Parent Supports Grill's Claim 28

patterning said second layer of resist with a via pattern,	FIG 5D  **'628 application at FIG. 5D** "A second resist layer 62, **patterned with a second (via level) pattern**, is then formed on the structure of Fig. 5C to produce the structure of Fig. 5D." EX1048 at 15:23-24.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

Grill's Provisional Parent Supports Grill's Claim 28

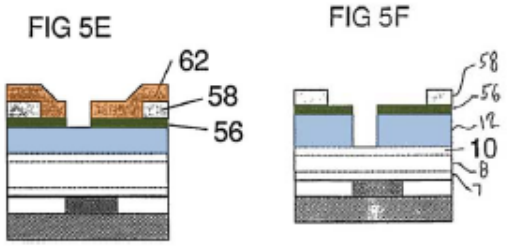
patterning said first hard mask layer using said via-patterned second layer of resist as a mask,	FIG 5E  **'628 application at FIG. 5E** "The pattern of resist layer 62 is then transferred into lower hard mask layer 56." EX1048 at 15:25-26.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

Grill's Provisional Parent Supports Grill's Claim 28

transferring said via pattern in said patterned **first hard mask layer** into said **second dielectric layer**, while concurrently removing said via-patterned **second layer of resist**, and



'628 application at FIGS. 5E, 5F

"The **via level pattern** is then transferred into **dielectric 12** by an etching process such as reactive ion etching, to produce the structure of Fig. 5F." EX1048 at 15:29-30.

Although the *Grill* patent later added a statement that the "[p]atterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12," *Grill* at 7:64–66, a person of ordinary skill in the art would have understood this to be taught by the '628 application.

The '628 application teaches that the "interconnect dielectric and the photoresist stencil used to pattern the hard mask [may] have similar etch characteristics," such as "the case with an organic photoresist and a carbon-based interconnect dielectric such as DLC." EX1048 at 11:12-15. A person of ordinary skill in the art would have understood that etching layer 12 (DLC) under such circumstances concurrently removes layer 62 (photoresist) because the two layers have similar etch properties.

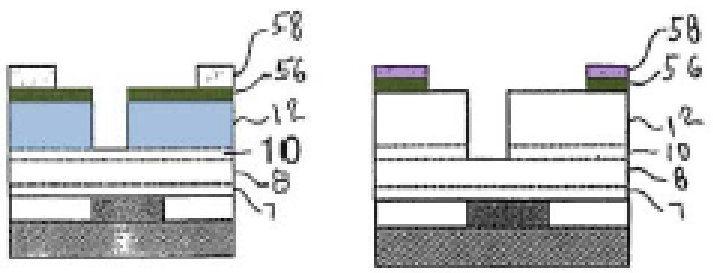
A person of ordinary skill in the art would have further understood that photoresist layer 62 is not removed prior to etching layer 12. Photoresist layer 62 cannot be removed by a dry process before patterning layer 12 because any dry process for removing layer 62 would concurrently etch layer 12, as claim 28 reqires. Again, layers 12 and 62 (photoresist and DLC) have similar etch properties. Similarly, any attempt to strip the photoresist using a wet checmical process before etching layer 12 would cause the problems described with regard to Figures 2C and 2D and damage exposed dielectric layer 12. '682 application at 4, Fig. 2C, 2D.

A person of ordinary skill in the art would have thus understood that the transition between Figures 5E and 5F involves concurrently removing photoresist layer 62 and dielectric layer 12.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

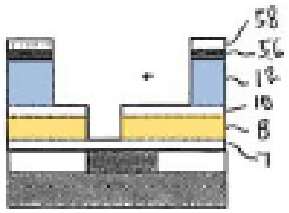
Grill's Provisional Parent Supports Grill's Claim 28

patterning said via-patterned first hard mask layer using said wiring-patterned second hard mask layer as a mask,	FIG 5F FIG 5G  **'628 application at FIG. 5G** "The etching conditions are then changed to removed [sic] exposed portions of lower hard mask layer 56 and optional etch stop 10, to form the structure of Fig. 5G." EX1048 at 15:30-32.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

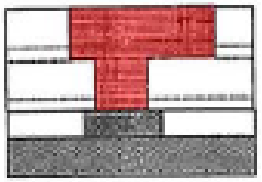
Grill's Provisional Parent Supports Grill's Claim 28

transferring, at least partially concurrently, said via pattern into said first dielectric layer to form via cavities corresponding to said via pattern, and said wiring pattern into said second dielectric layer to form wiring cavities corresponding to said wiring pattern, and	FIG 5H  **'628 application at FIG. 5H** "Dielectrics 8 and 12 are then etched to transfer said **second pattern [wiring level]** into the entire thickness of dielectric 12, and said **first pattern [via level]** into the entire thickness of dielectric 8, as shown in Fig. 5H." EX1048 at 15:32-34.

IPR2016-01376, EX1049, at ¶43

See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

Grill's Provisional Parent Supports Grill's Claim 28

filling said cavities with **conductive material** to make electrical contact with said conductive regions and to form said vias and said wiring pattern.	FIG 1L  **'628 application at FIG. 1L** "The cavity structure may then be completed as shown in FIG. 1J, and, for interconnect applications, filled with **wiring material** as shown in FIGS. 1K to 1L." EX1048 at 15:34-35.

IPR2016-01376, EX1049, at ¶43

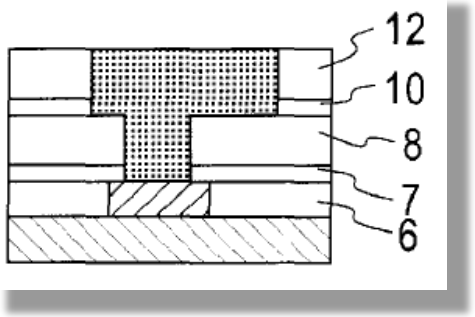
See, e.g., IPR2016-01376, Paper 26, at 15–20; IPR2016-01376, EX1049, at ¶43.

Grill's Optional Layer 7 & The Wetzel Reference

- **Grill Does Not Name Materials for Optional Layer 7**
- **Wetzel Discloses Possible Materials for Layer 7 (e.g., Si_3N_4)**

A layered dielectric stack **13** comprising an optional dielectric passivation/adhesion layer **7**, a via level dielectric **8**, an optional dielectric etch stop layer **10**, and a wiring level dielectric **12** are then applied to produce the structure of FIG. 1B. Via and wiring dielectrics **8** and **12** might be

Grill at 4:1–5



Grill at FIG. 1L

substrate, particularly SiO_2. Further, a passivation layer **16** is provided so as to cover substrate **10**, which includes metal interconnects **12**. Passivation layer **16** functions to protect metal interconnects **12** from damage during later processing steps, and also provides an etch stop function during later processing steps. The passivation layer **16** may be formed of silicon nitride, silicon oxynitride, or composites thereof.

Wetzel at 3:46–52

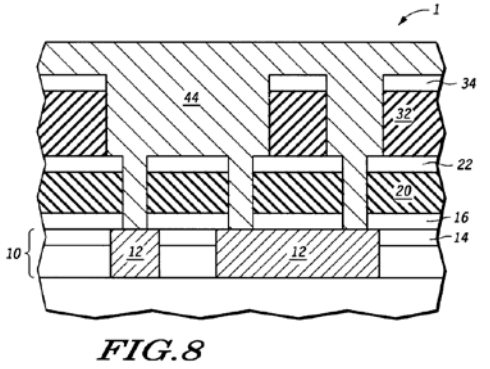


FIG. 8

Wetzel at FIG. 8

See, e.g., Petition, IPR2016-01379, Paper 2, at 79; IPR2016-01379, EX1005, at 4:1–5; IPR2016-01379, EX1019, at 3:46–52, FIG. 8.

Identifying a Priority Document Does Not Shift Burdens

- ***Lucent Techs., Inc. v. Gateway, Inc.***, 543 F.3d 710, 718 (Fed. Cir. 2008)

> [9] [10] Furthermore, we disagree that written descriptive support in the specification is not relevant to determining when the claimed technology was developed. In order to be valid, each patent claim must meet all the statutory requirements, including written description under 35 U.S.C. § 112, first paragraph. Patent claims are awarded priority on a claim-by-claim basis based on the disclosure in the priority applications. *Go Med. Indus. Pty., Ltd. v. Inmed Corp.*, 471 F.3d 1264, 1270 (Fed.Cir.2006); *Augustine Med., Inc. v. Gaymar Indus., Inc.*, 181 F.3d 1291, 1302 (Fed.Cir.1999). When the # 080 patent application was filed as a reissue of the #938 patent, the priority was amended to claim priority as a continuation to an application filed in 1992, which in turn was a CIP of another application that was a continuation ***719** of the #598 application, filed in 1988. Thus, while the # 080 patent (and the #938 patent) shares the same specification as the application filed in 1992, it does not share the same specification as the #598 application. Since the critical date for distinguishing between New Work and Existing Technology is April 1989, it is important to establish whether the claims of the #080 patent are entitled to the priority date of the #598 application (i.e., 1988) or only to the 1992 priority date.

- It is impossible to discern for which claims and on what basis a Patent Owner might allege priority when a patent claims the benefit of priority to an earlier application

See, e.g., IPR2016-01376, Paper 9, at 1–3; IPR2016-01376, Paper 26, at 2–3.

Embodiments of the JP '371 Application

- The Japanese '371 application contains the following:
  - **First Embodiment** (EX1014 at ¶¶0028–0062, FIGS. 1(a)–8(c); EX2012 at 15:7–25:4, FIGS. 1(a)–8(c))
  - **Second Embodiment** (EX1014 at ¶¶0063–0074, FIGS. 9(a)–11(c); EX2012 at 25:5–28:16, FIGS. 9(a)–11(c))
  - **Third Embodiment** (EX1014 at ¶¶0075–0088, FIGS. 12(a)–14(c); EX2012 at 28:17–33:8, FIGS. 12(a)–14(c))
  - **Modified Example of Third Embodiment** (EX1014 at ¶¶0089–0102, FIGS. 15(a)–17(c); EX2012 at 33:9–37:5, FIGS. 15(a)–17(c))
  - **Fourth Embodiment** (EX1014 at ¶¶0104–0115, FIGS. 18(a)–20(c); EX2012 at 37:6–41:4, FIGS. 18(a)–20(c))
  - **Claims 1–9** (EX1014 at 4–5; EX2012 at 3:5–5:19)

See, e.g., IPR2016-01376, Paper 2, at 20–21. Compare also, e.g., IPR2016-01376, EX1001, with IPR2016-01376, EX1014 and IPR2016-01376, EX2012.

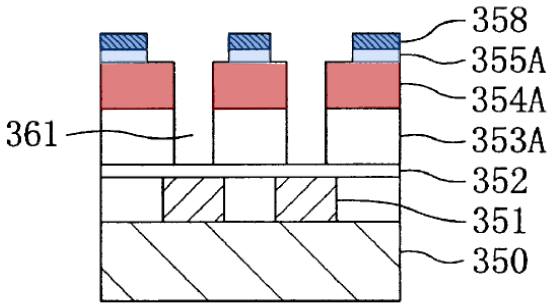
Patent Owner's First Example

Patent Owner's Example 1: Layer 355A

Thereafter, as shown in FIG. **16**(*d*), the patterned organic film **354**A is dry-etched using the mask pattern **358** and the patterned second silicon dioxide film **355**A having the openings for forming wiring grooves as a mask, thereby forming the wiring grooves **362**. In forming the wiring

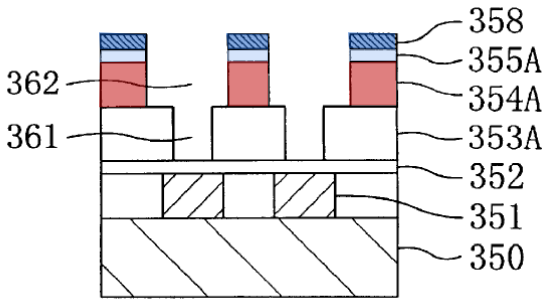
'696 Patent, 19:50–54

Fig. 16(c)



'696 Patent, Fig. 16(c)

Fig. 16(d)

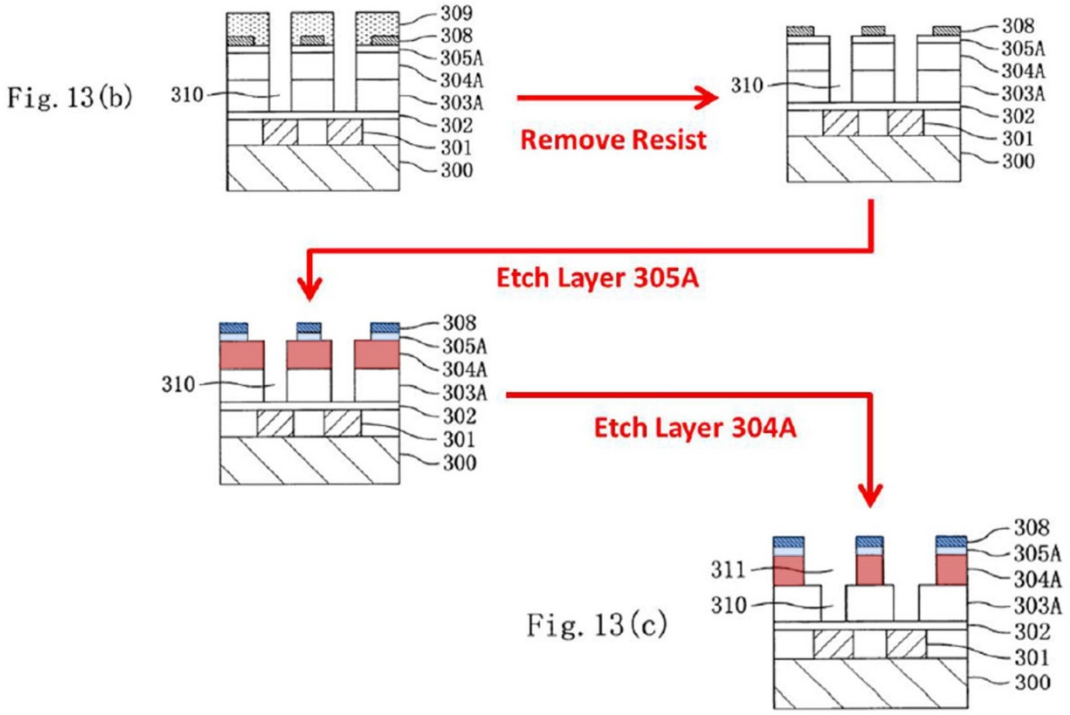


'696 Patent, Fig. 16(d)

See, e.g., IPR2016-01376, EX1001 at 19:40–49, FIGS. 16(c), 16(d); IPR2016-01376, EX1049, at ¶21; IPR2016-01376, Paper 19, at 11–12.

Patent Owner's Second Example

Patent Owner's Example 2: Layer 305A



Next, as shown in FIG. **13**(*c*), the second resist pattern **309** is removed and the patterned second organic-containing silicon dioxide film **305**A is dry-etched using the mask pattern **308** as a mask, thereby forming openings for forming wiring grooves in the patterned second organic-containing silicon dioxide film **305**A. Thereafter, the patterned low-dielectric-constant SOG film **304**A is dry-etched using the mask pattern **308** and the patterned second organic-containing silicon dioxide film **305**A having the openings for wiring grooves as a mask, thereby forming the wiring grooves **311**. In forming the wiring grooves **311**, by selecting

'696 Patent, 17:30–40

IPR2016-01376, EX1049, at ¶21

See, e.g., IPR2016-01376, EX1001 at 17:30–40, FIGS. 13(b), 13(c); IPR2016-01376, EX1049, at ¶21; IPR2016-01376, Paper 19, at 12–13.

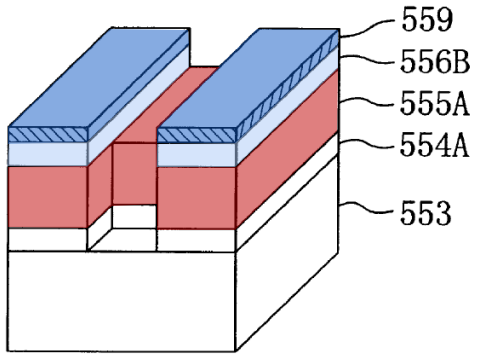
Patent Owner's Third Example

Patent Owner's Example 3: Layer 556B

28(*b*). Then, the patterned second organic film **555**A is dry-etched using the mask pattern **559** and the patterned second silicon dioxide film **556**B as a mask, and the first organic film **553** is dry-etched using the patterned first silicon dioxide film **554**A as a mask, thereby forming a patterned second organic film **555**B having wiring grooves **561** and a patterned first organic film **553**A having contact holes **562** as shown in FIGS. **26**(*c*) and **29**(*a*).

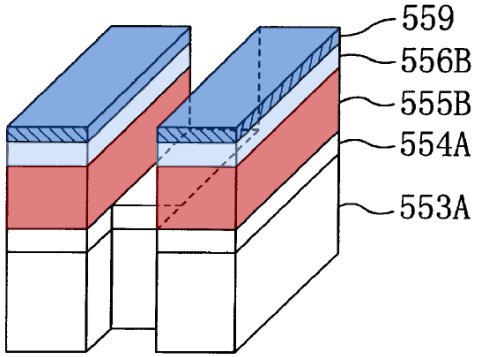
'696 Patent, 26:22–29

Fig. 28(b)



'696 Patent, Fig. 28(b)

Fig. 29(a)



'696 Patent, Fig. 29(a)

See, e.g., IPR2016-01376, EX1001 at 26:22–29, FIGS. 28(b), 29(a); IPR2016-01376, EX1049, at ¶21; IPR2016-01376, Paper 19, at 13–14.

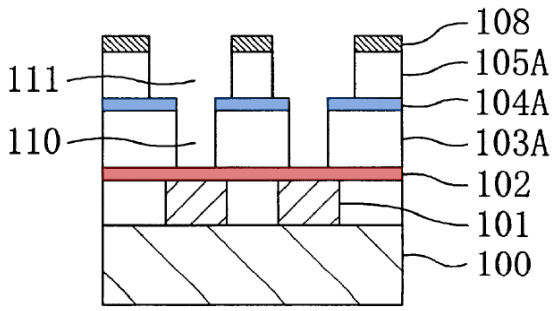
Petitioner's First Example

Petitioner's Example 1: Layer 103A

Subsequently, the silicon nitride film **102** is dry-etched using the patterned organic-containing silicon dioxide film **104A** as a mask, thereby forming a patterned silicon nitride film **102A** and exposing the first metal interconnects **101** within the contact holes **110** as shown in FIG. **3**(*a*).

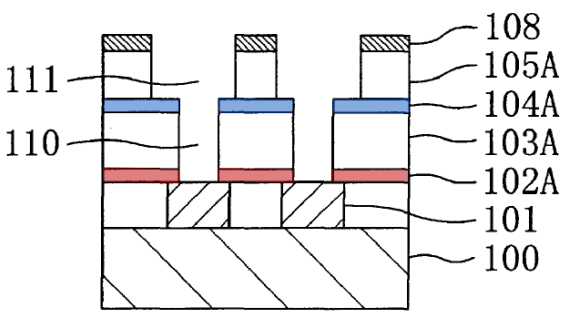
'696 Patent, 11:51–55

Fig. 2(c)



'696 Patent, Fig. 2(c)

Fig. 3(a)



'696 Patent, Fig. 3(a)

See, e.g., IPR2016-01376, EX1001 at 11:51–55, FIGS. 2(c), 3(a); IPR2016-01376, EX1049, at ¶27.

Petitioner's Second Example

Petitioner's Example 2: Layer 103A

Subsequently, the silicon nitride film **102** is dry-etched using the patterned organic-containing silicon dioxide film **104A** as a mask, thereby forming a patterned silicon nitride film **102A** and exposing the first metal interconnects **101** within the contact holes **110** as shown in FIG. **6**(*b*).

'696 Patent, 13:37–41

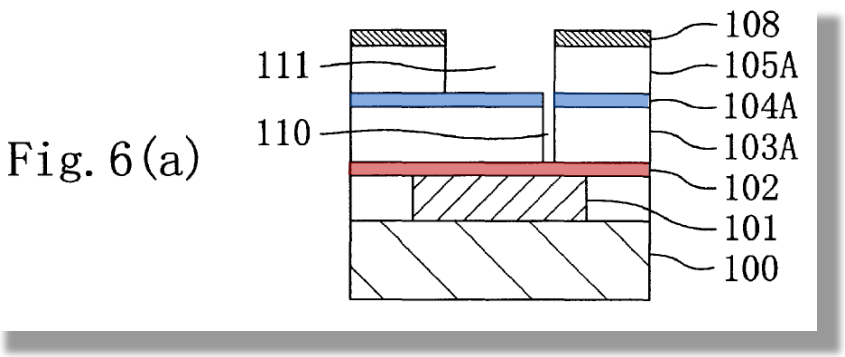


Fig. 6(a)

'696 Patent, Fig. 6(a)

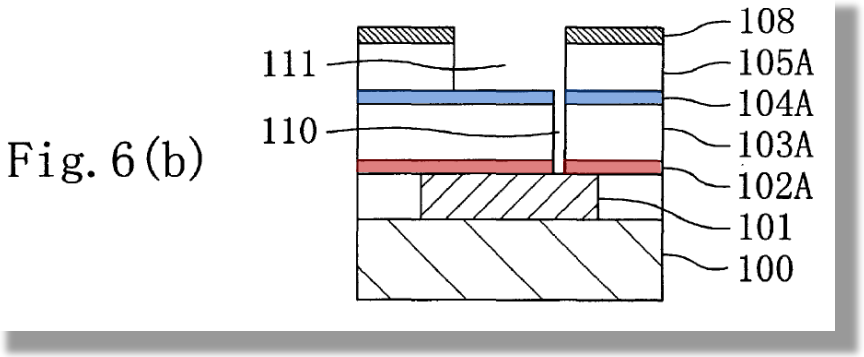


Fig. 6(b)

'696 Patent, Fig. 6(b)

See, e.g., IPR2016-01376, EX1001 at 13:37–41, FIGS. 6(a), 6(b); IPR2016-01376, EX1049, at ¶27.

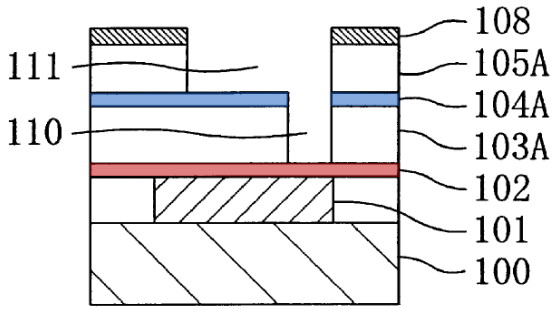
Petitioner's Third Example

Petitioner's Example 3: Layer 103A

Subsequently, the silicon nitride film **102** is dry-etched using the patterned organic-containing silicon dioxide film **104A** as a mask, thereby forming a patterned silicon nitride film **102A** and exposing the first metal interconnects **101** within the contact holes **110** as shown in FIG. **8**(*b*).

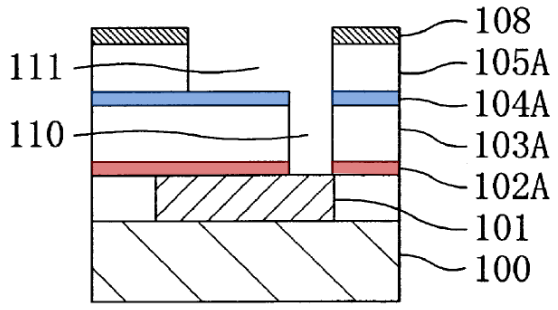
'696 Patent, 14:41–45

Fig. 8(a)



'696 Patent, Fig. 8(a)

Fig. 8(b)



'696 Patent, Fig. 8(b)

See, e.g., IPR2016-01376, EX1001 at 14:41–45, FIGS. 8(a), 8(b); IPR2016-01376, EX1049, at ¶27.

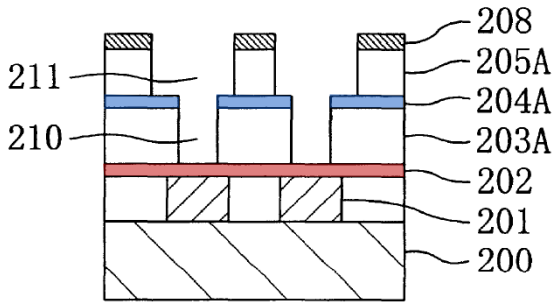
Petitioner's Fourth Example

Petitioner's Example 4: Layer 203A

Subsequently, the silicon nitride film **202** is dry-etched using the patterned organic-containing silicon dioxide film **204**A as a mask, thereby forming a patterned silicon nitride film **202**A and exposing the first metal interconnects **201** within the contact holes **210** as shown in FIG. **11**(*a*).

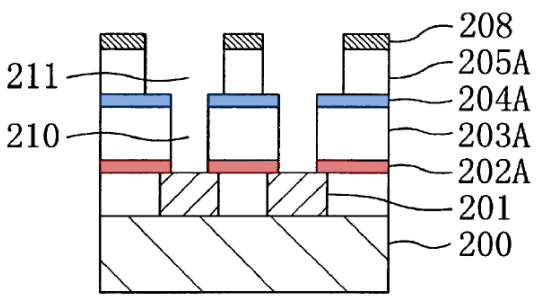
'696 Patent, 16:7–11

Fig. 10(c)



'696 Patent, Fig. 10(c)

Fig. 11(a)



'696 Patent, Fig. 11(a)

See, e.g., IPR2016-01376, EX1001 at 16:7–11, FIGS. 10(c), 11(a); IPR2016-01376, EX1049, at ¶27.

Petitioner's Fifth Example

Petitioner's Example 5: Layers 304A and 305A

Fig. 13(a)

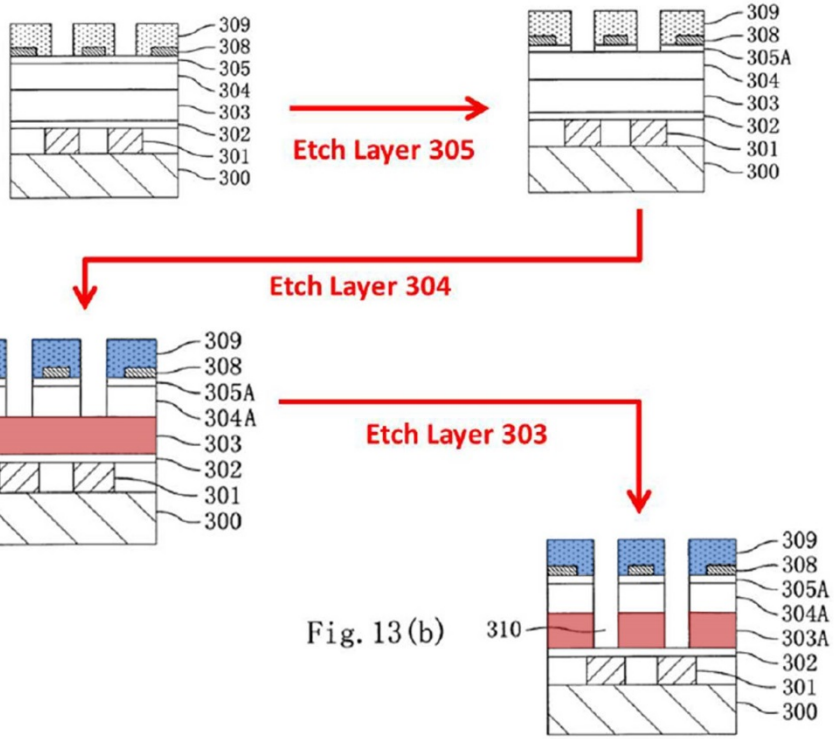


Fig. 13(b)

IPR2016-01376, EX1049, at ¶27

second organic-containing silicon dioxide film **305**. Then, the second organic-containing silicon dioxide film **305**, the low-dielectric-constant SOG film **304** and the first organic-containing silicon dioxide film **303** are sequentially dry-etched using the second resist pattern **309** as a mask. As a result, a patterned second organic-containing silicon dioxide film **305**A, a patterned low-dielectric-constant SOG film **304**A and a patterned first organic-containing silicon dioxide film **303**A having contact holes **310** are formed as shown in FIG. **13**(*b*).

'696 Patent, 17:20–29

See, e.g., IPR2016-01376, EX1001 at 17:20–29, FIGS. 13(a), 13(b); IPR2016-01376, EX1049, at ¶27.

Petitioner's Sixth Example

Petitioner's Example 6: Layer 355A

Fig. 16 (a)

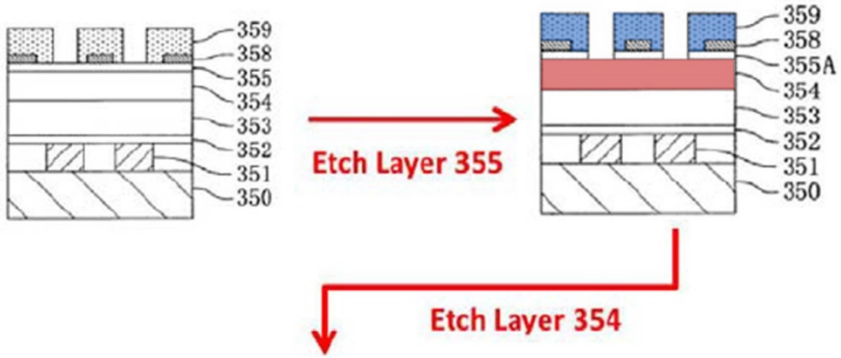


Fig. 16 (b)

IPR2016-01376, EX1049, at ¶27

second silicon dioxide film **355**. Then, the second silicon dioxide film **355** and the organic film **354** are sequentially dry-etched using the second resist pattern **359** as a mask, thereby forming a patterned second silicon dioxide film **355A** and a patterned organic film **354A** having openings **360** for forming contact holes as shown in FIG. **16**(*b*). In this case, the second resist pattern **359** is removed during the step of etching the organic film **354**.

'696 Patent, 19:33–40

the silicon nitride film **352**. Next, an organic film **354** (second insulating film) is deposited to be 400 nm thick, for example, on the first silicon dioxide film **353**. Then, a second

'696 Patent, 19:6–8

See, e.g., IPR2016-01376, EX1001 at 19:6–8, 19:33–40, FIGS. 16(a), 16(b); IPR2016-01376, EX1049, at ¶27.

Petitioner's Seventh Example

Petitioner's Example 7: Layer 405A

Fig. 18(c)

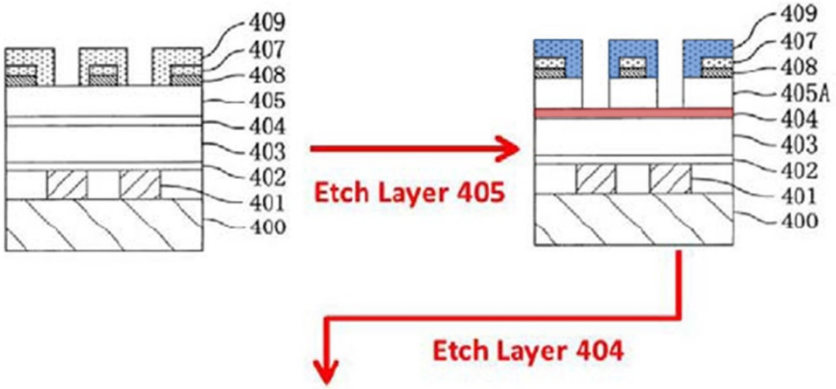
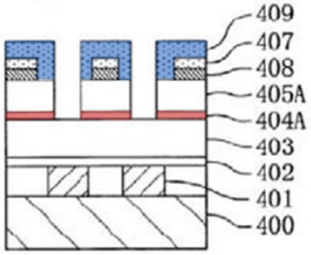


Fig. 19(a)



IPR2016-01376, EX1049, at ¶27

removing the first resist pattern **407**. Then, the second low-dielectric-constant SOG film **405** and the organic-containing silicon dioxide film **404** are sequentially dry-etched using the second resist pattern **409** as a mask, thereby forming a patterned second low-dielectric-constant SOG film **405A** and a patterned organic-containing silicon dioxide film **404A** as shown in FIG. **19**(*a*).

'696 Patent, 21:33–39

See, e.g., IPR2016-01376, EX1001 at 21:33–39, FIGS. 18(c), 19(a); IPR2016-01376, EX1049, at ¶27.

Inconsistency in Specification's Inconsistencies

- In all three Patent Owner examples, the intermediate layer with the flush sidewall has the same ***wiring*** pattern as the mask.
- In all seven Petitioner examples, the intermediate layer with the flush sidewall has the same ***contact hole*** pattern as the mask.

See, e.g., IPR2016-01376, EX1049, at ¶¶ 20–28; IPR2016-01376, Paper 26, at 11–12.

Dr. Glew's ¶70 Does Not Mention Any "Admissions"

Contrary to the additional negative limitation and Petitioner's expert's (Dr. Smith) arguments during his deposition, Petitioner's expert has admitted in prior publications that a "multiple layer resist" having ***flush*** edges can be used to define a "substrate film material" to be etched—*i.e.*, can be used as a mask. EX2018 642-643, 657; EX2010 49:6-50:9; EX2009 ¶¶70-71; *see also* EX2017 574, 592. For

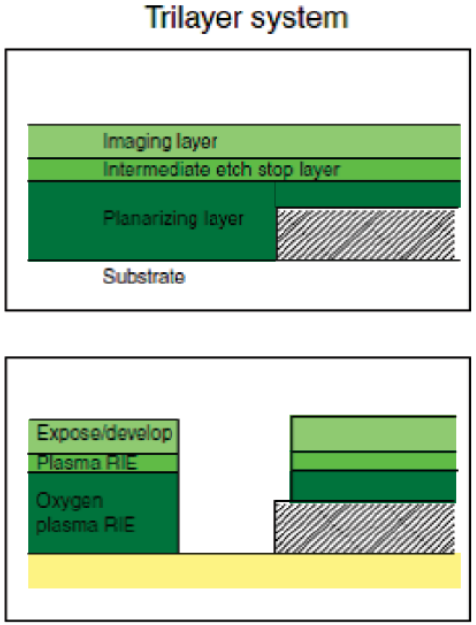
70. I understand that Dr. Smith has asserted during his deposition that passages from the '696 patent that describes using two layers that have flush edges (*e.g.*, layers 358 and 355A) as a mask to etch underlying layer 354A are inconsistent with the other embodiments of the '696 patent. EX2010 45:1-47:8. I disagree. As discussed above, the '696 patent discloses three embodiments that expressly use two layers having flush edges as a mask (the modified third embodiment, third embodiment and modified fifth embodiment). Dr. Smith gives no basis to justify simply ignoring these disclosures by labeling them (incorrectly) as inconsistent.

IPR2016-01376, EX2009, at ¶70

See, e.g., IPR2016-01376, Paper 19, at 17; IPR2016-01376, EX2009, at ¶70.

Dr. Glew's ¶71 Mischaracterizes Dr. Smith's Book

Contrary to the additional negative limitation and Petitioner's expert's (Dr. Smith) arguments during his deposition, Petitioner's expert has admitted in prior publications that a "multiple layer resist" having ***flush*** edges can be used to define a "substrate film material" to be etched—*i.e.*, can be used as a mask. EX2018 642-643, 657; EX2010 49:6-50:9; EX2009 ¶¶70-71; *see also* EX2017 574, 592. For



71. Dr. Smith's testimony is also inconsistent with his own publication which describes using multiple layers in a resist (*e.g.*, a multi-layer resist). Dr. Smith is an author and editor of a book chapter entitled "Multilayer Resist Technology." EX2010 49:6-50:9; EX2018 at 657. As Dr. Smith himself confirmed, his book states that a multilayer resist techniques use "physically distinct layers to separate the imaging function from the etch resistance, planarization and reflection suppression function." EX2010 49:6-50:9; EX2018 at 657. An earlier edition of Dr. Smith's book published in 1998 also includes this passage. EX2017 at 592. As illustrated in Fig. 12.3(c), reproduced below from Smith's book chapter, a multi-layer resist including multiple layers having flush edges (*e.g.*, a planarizing layer, an intermediate etch stop layer, and an imaging layer) is used to define areas for etching a substrate. EX2010 50:10-20, 58:8-59:1; EX2018 at 642-643 ("Three resist layers may be used to allow specific feature shaping…"). This passage is also present in the earlier edition of Dr. Smith's book published in 1998. EX2017 at 574, 592.

IPR2016-01376, EX2009, at ¶71

See, e.g., IPR2016-01376, Paper 19, at 17; IPR2016-01376, EX2009, at ¶71.

Dr. Smith's Testimony Makes No Admissions

Contrary to the additional negative limitation and Petitioner's expert's (Dr. Smith) arguments during his deposition, Petitioner's expert has admitted in prior publications that a "multiple layer resist" having ***flush*** edges can be used to define a "substrate film material" to be etched—*i.e.*, can be used as a mask. EX2018 642-643, 657; EX2010 49:6-50:9; EX2009 ¶¶70-71; *see also* EX2017 574, 592. For

MR. ROSSEN: Okay. All right. I'm going to introduce another document. Can I get you to -- the court reporter to label this as Smith Exhibit 3.

The following was marked for Identification:

SMITH EXH. 3 Chapter 12 of textbook titled Microlithography: Science and Technology

BY MR. ROSSEN:

Q. Are you familiar with this document?

A. I am. This looks like one chapter out of a textbook that I've edited and authored called Microlithography: Science and Technology.

Q. Okay. So this is chapter 12 from the book that you edited, correct?

A. It looks to be some front matter for the book which includes a page describing various -- various other publications by the publisher, a preface to the book itself, a description of the editors, including my coeditor, Dr. Suzuki, a list of contributors to the chapters, a table of contents, and then, yes, it looks like chapter 12 is included.

Q. Okay. And you edited this chapter 12?

A. I co-wrote this chapter and edited it, yes.

IPR2016-01376, EX2010, at 49:6–50:9

See, e.g., IPR2016-01376, Paper 19, at 17; IPR2016-01376, EX2010 at 49:6–50:9.

Patent Owner's Argument for Multi-layer Resists Has No Support

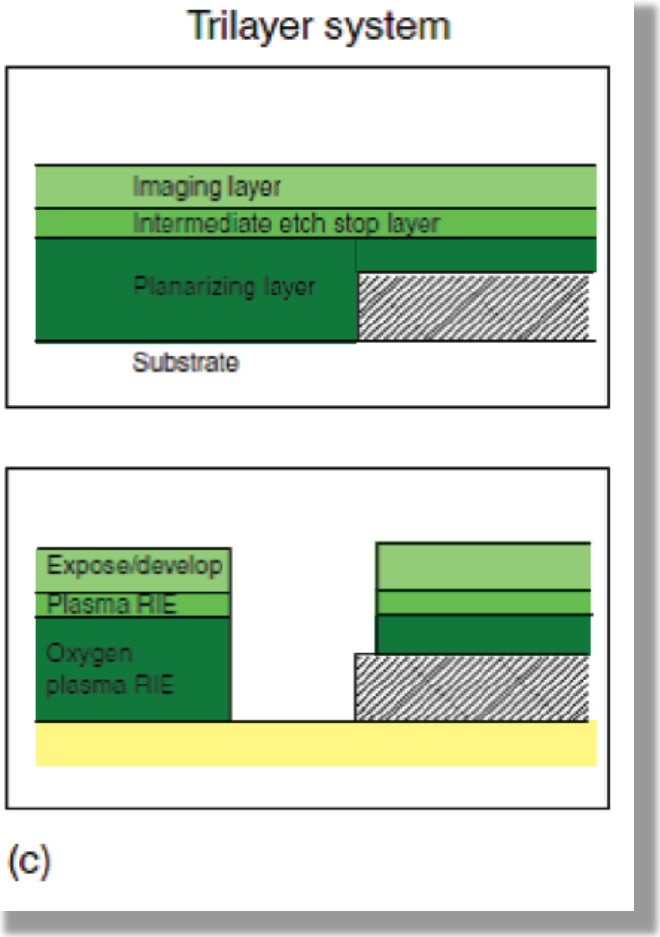
- **Patent Owner relies solely on mischaracterizations of multi-layer resist processes**
- **Patent Owner's position is directly contradicted by the following:**
  - Dr. Smith's testimony
  - The source material cited in Dr. Smith's book to describe the portions Patent Owner relies on
  - Independent textbooks describing multi-layer resist processes
  - Independent patent evidence describing multi-layer resist processes

See, e.g., IPR2016-01376, Paper 26, at 6–7; IPR2016-01376, Paper 41, at 3–5; IPR2016-01376, EX2010, at 60:22–65:8; IPR2016-01376, EX1031, at 41, 70; IPR2016-01376, EX1032, at 14; IPR2016-01376, EX1033, at 3:20–49, FIGS. 1–4; IPR2016-01376, EX1044, at 3–4; IPR2016-01376, EX1045, at 1, 6; IPR2016-01376, EX1046, at 2–3.

Patent Owner's Argument for Multi-layer Resists Has No Support

Contrary to the additional negative limitation and Petitioner's expert's (Dr. Smith) arguments during his deposition, Petitioner's expert has admitted in prior publications that a "multiple layer resist" having ***flush*** edges can be used to define a "substrate film material" to be etched—*i.e.*, can be used as a mask. EX2018 642-643, 657; EX2010 49:6-50:9; EX2009 ¶¶70-71; *see also* EX2017 574, 592. For

IPR2016-01376, Paper 19, at 17



IPR2016-01376, Paper 19, at 18

See, e.g., IPR2016-01376, Paper 19, at 17; IPR2016-01376, EX2018, at 18–19, 33; IPR2016-01376, EX2010, at 49:6–50:9; IPR2016-01376, EX2009, at ¶¶70–71; IPR2016-01376, EX2009, at 61, 79; IPR2016-01376, EX2017, at 60–61, 79.

Patent Owner Mischaracterizes Dr. Smith's Book

Contrary to the additional negative limitation and Petitioner's expert's (Dr. Smith) arguments during his deposition, Petitioner's expert has admitted in prior publications that a "multiple layer resist" having ***flush*** edges can be used to define a "substrate film material" to be etched—*i.e.*, can be used as a mask. EX2018 642-643, 657; EX2010 49:6-50:9; EX2009 ¶¶70-71; *see also* EX2017 574, 592. For

7 SILICON-CONTAINING RESISTS FOR MULTILAYER AND SURFACE IMAGING RESIST APPLICATIONS

Multilayer resist techniques have long been used to ease requirements for resist performance [51–56]. This goal is achieved by using physically distinct layers to separate the imaging function from the etch resistance, planarization, and reflection suppression functions. Trilevel resists have demonstrated enhanced resolution compared with single-layer resist processing. The trade-off for this resolution, however, is additional processing difficulty as the deposition and patterning of three layers must now be simultaneously controlled. Although excellent results have been obtained, the processing complexity has been the major obstacle for the widespread application to production of integrated circuits.

IPR2016-01376, EX2017, at 79 (592)

See, e.g., IPR2016-01376, Paper 19, at 17; IPR2016-01376, EX2017, at 79; IPR2016-01376, Paper 26, at 6–8 & n.2.

Patent Owner Mischaracterizes Dr. Smith's Book

Contrary to the additional negative limitation and Petitioner's expert's (Dr. Smith) arguments during his deposition, Petitioner's expert has admitted in prior publications that a "multiple layer resist" having ***flush*** edges can be used to define a "substrate film material" to be etched—*i.e.*, can be used as a mask. EX2018 642-643, 657; EX2010 49:6-50:9; EX2009 ¶¶70-71; *see also* EX2017 574, 592. For

12.7 Silicon-Containing Resists for Multilayer and Surface Imaging Resist Applications

Multilayer resist techniques have long been used to ease requirements for resist performance [51–56]. This goal is achieved by using physically distinct layers to separate the imaging function from the etch resistance, planarization, and reflection suppression function. Trilevel resists have demonstrated enhanced resolution compared with single-layer resist processing. The trade-off for this resolution, however, is additional processing difficulty as the deposition and patterning of three layers must now be simultaneously controlled. Although excellent results have been obtained, the processing complexity has been the major obstacle for the widespread application to production of integrated circuits.

IPR2016-01376, EX2018, at 33 (657)

See, e.g., IPR2016-01376, Paper 19, at 17; IPR2016-01376, EX2018, at 33; IPR2016-01376, Paper 26, at 6–8 & n.2.

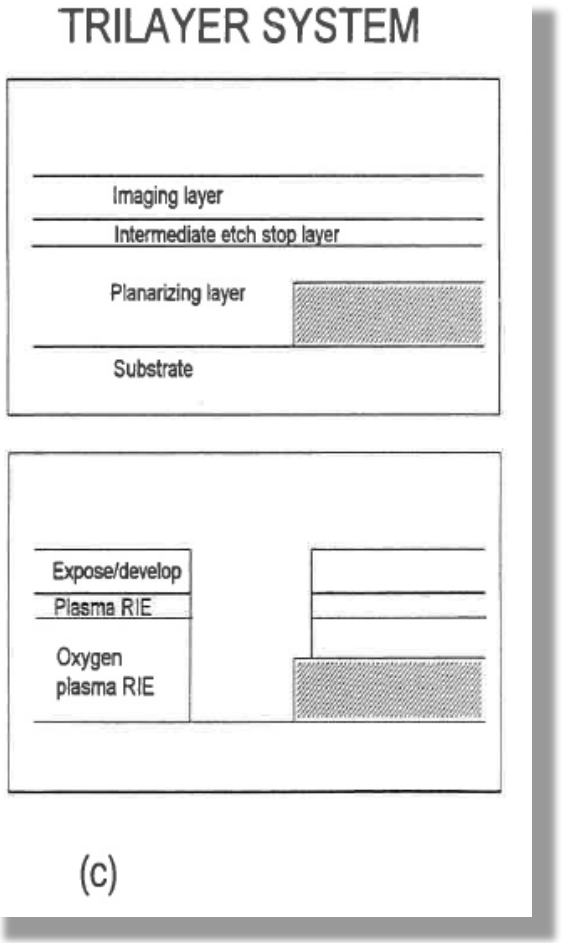
Patent Owner Mischaracterizes Dr. Smith's Book

Contrary to the additional negative limitation and Petitioner's expert's (Dr. Smith) arguments during his deposition, Petitioner's expert has admitted in prior publications that a "multiple layer resist" having ***flush*** edges can be used to define a "substrate film material" to be etched—*i.e.*, can be used as a mask. EX2018 642-643, 657; EX2010 49:6-50:9; EX2009 ¶¶70-71; *see also* EX2017 574, 592. For

3 WET DEVELOPMENT/DRY PATTERN TRANSFER APPROACHES TO MULTILAYERS

Anisotropic pattern transfer can allow significant improvement over the isotropic processing of wet-etched multilayer approaches. Through the use of a plasma reactive ion etch (RIE) pattern transfer process, near anisotropy can be approached, allowing high-aspect ratio, fine feature resolution [12, 13]. The three-layer schemed depicted in Fig. 3 makes use of a polymeric planarizing layer (such as novolac resin or polyimide) and a thin intermediate etch stop layer. This etch stop layer can be a spin-on organosilicon compound (spin on glass), a low-temperature oxide, a silicon oxinitride, or a metallic layer, which provide oxygen etch resistance. A thin resist imaging layer is coated over this etch stop, exposed, and wet developed. Pattern transfer into the intermediate etch-stop layer can be achieved with wet etch or dry plasma techniques with suitable chemistry. Anisotropic pattern transfer through the thick polymeric planarizing layer can be achieved via an oxygen RIE process. Variations on this technique have been used for both optical and electron beam applications [14].

IPR2016-01376, EX2017, at 61 (574)



IPR2016-01376, EX2017, at 60 (573)

See, e.g., IPR2016-01376, Paper 19, at 17; IPR2016-01376, EX2017, at 60–61.

Patent Owner's Argument Has No Support

Other references recognize that "[m]ulti-layer processing techniques" that collectively form a "total patterning layer" for etching were beneficial and "common in semiconductor and computer manufacturing R & D labs." *See, e.g.*, EX2015 260-261; EX2009 ¶¶69, 73; EX2017 574, 592; CBM2012-00002, Pap.66, 64.

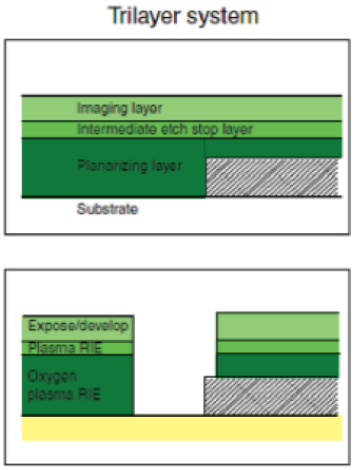
IPR2016-01376, Paper 19, at 18

See, e.g., IPR2016-01376, Paper 19, at 18; IPR2016-01376, EX2015, at 7–8; IPR2016-01376, EX2009, at ¶¶69, 73; IPR2016-01376, EX2017, at 60–61, 79.

Patent Owner Position is Incorrect

- Patent Owner Re-Argued Its Mischaracterizations In Its Reply to Petitioner's Motion to Exclude

EX2018 at 0019, 0033. Dr. Smith depicted (Fig. 3(c) in EX2017 and Fig. 12.3(c) in EX2018 (shown to the right)) these multiple layers, having edges in line and flush with each other, being used collectively to define an area for patterning (used as a mask to pattern) an underlying substrate. EX2017 at 0060; EX2018 at 0018.



Both EX2017 and EX2018 support Patent Owner's construction that an intermediate layer (*e.g.*, intermediate etch stop layer, or planarizing layer) that is in line and flush with an overlying layer (*e.g.*, imaging layer or intermediate etch stop layer, respectively), are used together as a mask to pattern an underlying substrate.

IPR2016-01376, Paper 37, at 6

See generally, e.g., IPR2016-01376, Paper 37, at 1–12.

Patent Owner's Unsupportable Position

- Patent Owner Re-Argued Its Mischaracterizations In Its Reply to Petitioner's Motion to Exclude

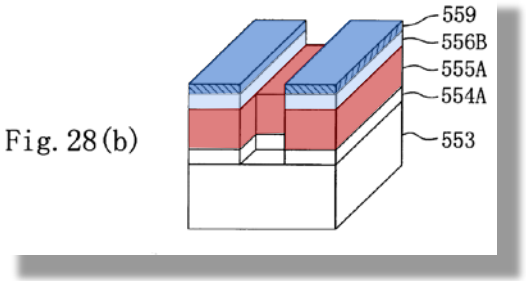
> Similar to EX2017 and EX2018, EX2015 is relevant because it demonstrates that Patent Owner's construction of "using the [designated layer] as a mask" is correct. EX2015 shows that multiple layers of a multi-layer resist process are referred to collectively as a layer used to pattern (used to mask) an underlying substrate. For example, EX2015 states that "[m]ultilayer processing techniques, where layers of radiation sensitive (top), non-photosensitive organic, and/or inorganic materials [are] sandwiched together to become the ***total patterning layer***"—*i.e.*, multiple layers are referred to collectively as a single patterning mask. EX2015 0007.[5]

IPR2016-01376, Paper 37, at 8

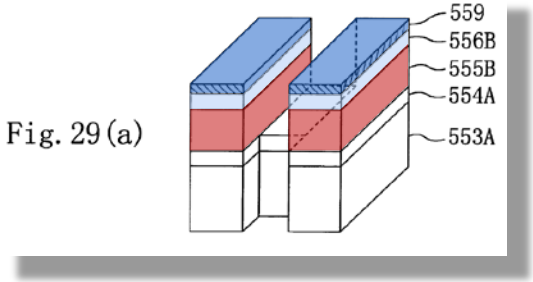
See generally, e.g., IPR2016-01376, Paper 37, at 1–12.

Patent Owner's Examples Are Not Representative

- **The Intermediate Layer in All of Patent Owner's Three Examples Have the *Same Pattern* as the Mask**

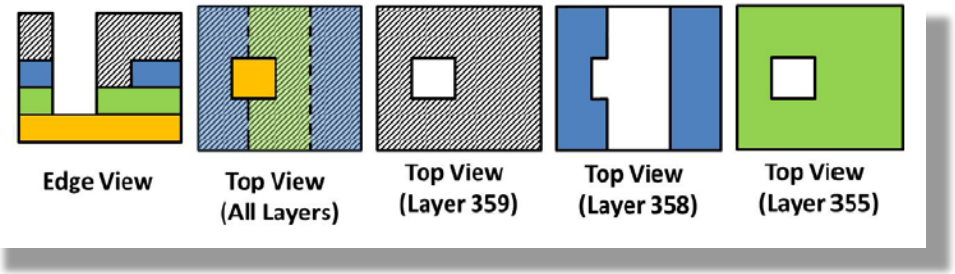


'696 Patent, Fig. 28(b)



'696 Patent, Fig. 29(a)

- **The Intermediate Layer in the Process at Issue Has a Wiring Pattern, Not the Contact Hole Pattern of the Mask**



'696 Patent, Fig. 28(b)

See, e.g., IPR2016-01376, EX1001 at 17:30–40, 19:40–49, 26:22–29, FIGS. 13(b), 13(c), 16(c), 16(d), 28(b), 29(a); IPR2016-01376, EX1049, at ¶32; IPR2016-01376, Paper 19, at 11–14; IPR2016-01376, *Paper 26, at 11.*

The Board's Decision Does Not "Read Out" Any Embodiments

- **A claim need not cover every embodiment**
  - ***TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc.***, 529 F.3d 1364, 1373 (Fed. Cir. 2008) ("Our precedent is replete with examples of subject matter that is included in the specification, but is not claimed.").
  - ***Intamin Ltd. v. Magnetar Techs., Corp.***, 483 F.3d 1328, 1337 (Fed. Cir. 2007) ("[T]his court has acknowledged that a claim need not cover all embodiments. A patentee may draft different claims to cover different embodiments.").
  - ***PSN Illinois, LLC v. Ivoclar Vivadent, Inc.***, 525 F.3d 1159, 1166 (Fed. Cir. 2008) ("[C]ourts must recognize that disclosed embodiments may be within the scope of other allowed but unasserted claims.").

Responsive to IPR2016-01376, Paper 19, at 10–14, for example.

Patent Owner and Its Expert Misunderstand Selectivity

- Patent Owner and its expert mistakenly argued the combination of references would cause the silicon oxide upper hard mask in Grill to etch faster than the silicon nitride lower hard mask in the presence of a silicon nitride etching process.

IPR2016-01376, EX2009, at ¶156

156. Thus, under Petitioner's proposed modification to use Aoyama's wider through hole pattern 62, the upper hard mask 58 would be exposed to a silicon nitride etch process during etching of lower hard mask 56 in step Fig. 5E'. A person of ordinary skill would recognize that because silicon oxide etches at a faster rate than silicon nitride, such exposure of upper hard mask 58 (*e.g.*, composed of silicon oxide) to a dry etch process of lower hard mask 56 (*e.g.*, composed of silicon nitride), as shown in Petitioner's Figure 5D', would degrade the exposed portions of upper hard mask 58. This is confirmed by Figures 5F and 5G of Grill, which illustrate that when etch conditions are set to remove exposed portions of lower hard mask layer 56 and optional etch stop 10 to form the structure of Fig. 5G, the upper hard mask layer 58, despite having a different etch selectivity from lower hard mask layer 56, is substantially thinned. EX1005 Figs.

See, e.g., IPR2016-01376, Paper 26, at 24–27; IPR2016-01376, EX2009, at ¶156.

MOTION TO EXCLUDE

Petitioner's Motion to Exclude

- **Petitioner Moves to Exclude Three Exhibits**
  - Exhibit 2015 (from a 2001 textbook)
  - Exhibit 2018 (from the 2007 version of Dr. Smith's textbook)
  - Exhibit 2019 (from the 2007 version of Dr. Smith's textbook)
- **All Three Exhibits Have Counterparts in the Record that Pre-Date the '696 Patent**
- **Petitioner Seeks Their Exclusion For the Same Reason**
  - To the extent the pre- and post-patent content is the same, it is needlessly cumulative under Fed. R. Evid. 403
  - To the extent the pre- and post-patent content is not the same, the later evidence is "impermissible . . . later knowledge about later art-related facts." *In re Hogan*, 559 F.2d 595, 605 (CCPA 1977).

See, e.g., IPR2016-01376, Paper 30, at 1–2.

Patent Owner's Response to the Motion to Exclude

- **Patent Owner's Response Is an Inappropriate Sur-Reply**
  - Uses 12 pages to respond to a two-page motion
  - Does not address the objections raised in the motion
  - Devoted solely to re-arguing issues of substance
- **Subsection Titles in Patent Owner's Argument Section**
  - A. Exhibits 2015 and 2018 and the proper construction of "using the [designated] layer as a mask"
    - 1. EX2018 belies Petitioner's and its Expert's assertions regarding the meaning of "using the [designated layer] as a mask"
    - 2. EX2015 further demonstrates that Patent Owner's construction is correct
  - B. Exhibit 2019 and Grill's warning against loss of critical dimension control caused by photoresist profiles having widely varied thicknesses

See, e.g., IPR2016-01376, Paper 37, at 1–12.

Petitioner's Reply

- **Petitioner Asks the Board to Strike Patent Owner's Improper Response**
  - The Board should not encourage Patent Owner's Trojan-horse tactics
  - Petitioner is prejudiced because it could not respond to 12 pages of arguments in five pages
- **Petitioner Asks the Board to Exclude Exhibits 2015, 2018, and 2019 for the Reasons Stated in the Motion**

See, e.g., IPR2016-01376, Paper 41, at 1–5.

Effect of Process Conditions

- **Process conditions, such as gas pressure, gas composition, substrate temperature, plasma power, and substrate electrode bias allow the etch profile to be tailored.**

And as we look at Figure 22A and 22B, you can see there is the ability to control side wall profile during the dry etch process depending on the choice of things like pressure, gas, temperature, and power.

Smith Dep. Tr. at 27:8–12

Q Do they travel in a perfectly vertical direction?

A They travel in a vertical direction, again, depending on the design of the process.

One RIE process is not like the other. I'll say it again. The things like power, pressure, temperature, gas flow, those things will -- will influence how directional the ionic species will become.

Smith Dep. Tr. at 35:12–20

See, e.g., IPR2016-01376, EX2040 at 26:20–27:12, 35:12–20.

Overetch Was Routine Under These Circumstances

As mentioned earlier, some overetching is normally part of every etch process. If each layer were of uniform thickness, and the etch were perfectly uniform through time and space, then overetching would theoretically not be needed. The etch time required would be based on the previously determined etch rate or on other endpoint detection methods, to be discussed later. It would not even matter what the etch selectivity over the layer beneath is in that case. However, the thickness of films is not perfectly uniform, and they do not always etch exactly uniformly. So some overetch is always done in manufacturing to ensure that the etch goes to completion everywhere. This is illustrated in Figure 10–4(b). In this figure we again assume that the selectivity with respect to the mask and substrate are infinite and that the etching is purely isotropic. The bias b now increases with time as the overetch continues. The amount of overetching needed, usually measured in terms of time or % time, can be determined by estimating the uncertainties in etch rates and in the nonuniformities of the thicknesses and then calculating the worst case etch time needed. Ten to twenty percent overetches are common. This ensures that while some of the structures may be overetched, none are underetched. We will see later that when the etching is anisotropic, overetching is also required to remove residual film from steps in the topography.

IPR2016-01376, EX1030, at 28

etch selectivity of polysilicon to thin gate oxide of more than 10 : 1 is required. In the case of a contact hole etch, a large amount of overetch time is required because of the different thicknesses of the oxide layers over the polysilicon gate and over the source and drain. Therefore, a high etch selectivity between silicon and oxide is re-

IPR2016-01376, EX1031, at 59

See, e.g., IPR2016-01376, Paper 26 at 13; IPR2016-01376, EX1030, at 28; IPR2016-01376, EX1031, at 59; IPR2016-01376, EX1049, at ¶36.

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), this is to certify that I served a true and correct copy of the **PETITIONER'S DEMONSTRATIVES** by electronic mail, this 8th day of September, 2017, on counsel of record for the Patent Owner as follows:

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Patent Owner has agreed to electronic service.

A true and correct copy of the **PETITIONER'S DEMONSTRATIVES** was also served on September 8, 2017, via email directed to counsel of record for Petitioner GlobalFoundries U.S. Inc. at the following:

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Dated: September 8, 2017

By: */Lisa C. Hines/*
Lisa C. Hines
Litigation Clerk
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