

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX
MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00649
Patent 8,301,833 B1

Before BRYAN F. MOORE, GEORGIANNA W. BRADEN, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc. (“Petitioner”) requests *inter partes* review of claims 1–30 of

U.S. Patent No. 8,301,833 B2 (“the ‘833 Patent,” Ex. 1001) pursuant to 35 U.S.C. §§ 311 *et seq.* Paper 1 (“Pet.”). Netlist, Inc. (“Patent Owner”) filed a preliminary response. Paper 6 (“Prelim. Resp.”). Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.108. Upon consideration of the Petition and Preliminary Response, we conclude the information presented shows there is not a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 1–30 of the ‘833 Patent.

A. *Related Matters*

Petitioner recites the District Court proceedings related to this *inter partes* review. Pet. 2. The Board has twice declined to institute an *inter partes* review of claims 1–30 of the ‘883 Patent. *Sandisk Corporation v. Netlist, Inc.*, Case IPR2014-00994 (PTAB December 16, 2014) (Paper 8) (rehearing denied, Paper 10); *Smart Modular Technologies Inc. v. Netlist, Inc.*, Case IPR2014-01370 (PTAB March 13, 2015) (Paper 13)).

Considering the particular circumstances of this case, we address the merits of the Petition and do not exercise our discretion under 35 U.S.C. § 325(d) (indicating “if another proceeding or matter involving the patent is before the Office, the Director may determine the manner in which the post-grant review or other processing or matter may proceed . . . and may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office”) and/or 35 U.S.C. § 314(a) (authorizing institution of an *inter*

partes review under particular circumstances, but not requiring institution under any circumstances). *See* 37 C.F.R. § 42.108(a) (“the Board may authorize the review to proceed”) (emphasis added); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (explaining that under § 314(a), “the PTO is permitted, but never compelled, to institute an IPR proceeding”). Petitioner was not a party to any of the prior proceedings. In addition, this Petition raises new issues, including asserting obviousness in view of references not at issue in the previous proceedings. Pet. 3.

B. The '833 Patent

The invention in the '833 patent relates to a specific configuration of hybrid memory systems that addresses non-volatile memory backup while running the volatile memory subsystem at lower power, and, therefore, at lower clock speeds. Ex. 1001, 16:29–34. Specifically, the alleged invention of the '833 patent includes circuitry for providing a regular high-speed clock frequency (first clock frequency) during communications between the host and the volatile memory subsystem, and a slower clock frequency during communications between the volatile memory subsystem (using a third clock frequency) and the non-volatile memory subsystem (using a second clock frequency). *Id.* at 21:5–21. Furthermore, the second and third clock frequencies may be substantially equal. *Id.* at 21:23–24.

C. Illustrative Claim

Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

1. A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;

operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem; and

operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

Ex. 1001, 21:6–22.

D. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–30 are unpatentable based on the following grounds:

References	Basis	Claim(s) challenged
Bonella ¹ and Mills ²	§ 103	1–30
Bonella, Mills, and Ashmore ³	§ 103	1–30
Bonella, Mills, Ashmore and Larson ⁴	§ 103	7 and 23
Bonella, Mills, Ashmore and Windows 2000 ⁵	§ 103	8–10, 24–26

¹ US Publication No. 2007/0136523 A1, filed December 8, 2006 (“Bonella,” Ex. 1005). Claims priority to US Provisional No. 11/635,926 filed December 8, 2005.

² US Patent No. 6,026,465, issued February 15, 2000 (“Mills,” Ex. 1007).

³ US Publication No. 2006/0212651 A1, published September 21, 2006 (“Ashmore,” Ex. 1008).

⁴ US Patent No. 6,571,244 B1, issued May 27, 2003 (“Larson,” Ex. 1019).

⁵ MICROSOFT WINDOWS 2000 PROFESSIONAL RESOURCE KIT, lists Feb. 2, 2000 date of publication (“Windows 2000,” Ex. 1021).

Bonella, Mills, Ashmore and Klein ⁶	§ 103	16
Bonella, Mills, Ashmore and Maeda ⁷	§ 103	17

Pet. 3, 14–59.

II. DISCUSSION

A. *Claim Construction*

In an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Consistent with the broadest reasonable construction, claim terms are presumed to have their ordinary and customary meaning as understood by a person of ordinary skill in the art in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

At this juncture of the proceeding, we determine that it is not necessary to provide an express interpretation of any term of the claims.

B. *Asserted Obviousness over Bonella and Mills*

Petitioner contends claims 1–30 are unpatentable under 35 U.S.C. § 103(a) as obvious over Bonella and Mills. Pet. 14–48. Relying on the testimony of Ron Maltiel, Petitioner explains how Bonella and Mills allegedly describe all of the claim limitations. *Id.* (citing Ex. 1003).

⁶ US Patent No. 6,721,860 B2, issued April 3, 2004 (“Klein,” Ex. 1009).

⁷ US Publication No. 2005/0249011 A1, published November 10, 2005 (“Maeda,” Ex. 1013).

1. Bonella (Ex. 1005)

Bonella is directed to a plug-and-play end-user add-in memory module for computers and consumer electronic devices. Ex. 1005 ¶ 2. Bonella discloses a memory module including a volatile memory, a non-volatile memory, and a controller that provides address, data, and control interfaces to the memories and to a host system. *Id.* ¶ 6.

Bonella teaches a “Power Level 5” state that allows for full function, full performance operation. *Id.* ¶ 47. Bonella also teaches a “Power Level 4” state that reduces the power consumption of the memory module by limiting the DRAM performance. *Id.* ¶ 48.

Bonella also teaches that the DRAM write buffer is occasionally backed up to the internal FLASH memory so as to ensure data integrity in case of a power loss. *Id.* ¶ 96. This write buffer flushing can be triggered by a power loss event, which then causes Bonella’s “Power loss algorithm” to be executed:

When the memory module controller detects a power loss event, the data that is flagged as critical is flushed to the FLASH, a flag is set and the memory module then shuts down. At new power on the normal power on sequence is followed and data restored to the DRAM.

Id. ¶ 101.

During the execution of the power loss algorithm, Bonella’s memory relies on backup power such as, for example, Uninterruptible Power Supply (UPS) capacitors. *Id.* ¶ 29.

2. Mills (Ex. 1007)

Mills describes several interfaces for a FLASH memory device, one of which is a synchronous FLASH interface, i.e. “a synchronous flash

interface (SFI) flash memory integrated circuit 600 that incorporates a complete synchronous flash interface in a single flash memory chip.” Ex. 1007, 16:60–63. The synchronous FLASH interface includes a clock input such that all the external operations of the device are synchronized to the rising edge of the clock. *Id.* at 17:10–25.

Mills teaches that this synchronous operation is used for both read operations and write operations: “When SFI is enabled, interlace control 670 and [bank] select logic 674 operate to interlace read (and write) operations between flash bank A 610 and a flash bank B 620” *Id.* at 17:33–39. Because “the device is interleaved internally,” it “creates an average access time for sequential read accesses that is significantly less than the access time of an asynchronous flash device.” *Id.* at 17:1–9.

3. Analysis

Claims 1 and 15 recite generally three limitations (excluding the preamble). We determine that Petitioner has not shown a reasonable likelihood that Bonella teaches the third limitation of claims 1 and 15, i.e. “operating the volatile memory subsystem [operable] at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.” Below, we summarize Petitioner’s position as to the other two limitations of claims 1 and 15 to provide context for the discussion of the third limitation.

In a first limitation, claims 1 and 15 recite “operating the volatile memory subsystem [operable] at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system.” Petitioner argues that Bonella discloses this feature. Pet. 15–19. Petitioner contends

“[o]ne of ordinary skill in the art would understand that Bonella’s DRAM [volatile memory subsystem] is operating at the particular frequency of the clock signal (“CLK”).” *Id.* at 16 (citing Ex. 1005 ¶ 52; Ex. 1003 ¶ 92).

Petitioner also contends, Bonella teaches its memory module has multiple power states, including Power Level 5 [first mode] which “allows for full function, full performance operation” with “no preset restrictions placed on the DRAM” and when “a skilled artisan would understand . . . ‘data is communicated between the volatile memory subsystem and the host system’ during a read from and write to the DRAM write buffer.” Pet. 17–18 (quoting Ex. 1005 ¶ 6, 8–9, 47, Abstract; Ex. 1003 ¶ 98).

In a second limitation, claims 1 and 15 recite “operating the non-volatile memory subsystem [operable] at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem.” Petitioner argues that the combination of Bonella and Mills teach this feature. Pet. 19–24.

Petitioner admits “Bonella does not explicitly disclose “*operating the non-volatile memory subsystem*” (the FLASH memory) “*at a second clock frequency*” during this second mode” Pet. 21. According to Petitioner, Mills discloses a synchronous Flash interface where read and write operations are synchronized to the rising edge of a clock signal provided to the device and operating at a particular frequency (i.e., “*operating [a] non-volatile memory subsystem at a second clock frequency*”).” Pet. 21–22 (citing Ex. 1007, 16:60–63, 17:10–25; Ex. 1003 ¶ 106–107). As explained below, we determine Bonella does not teach operating the volatile memory subsystem [operable] at a third clock frequency when the memory system is

in the second mode of operation, the third clock frequency being less than the first clock frequency, as recited in claims 1 and 15, therefore, we do not decide whether Petitioner has combined Bonella and Mills properly. Below we discuss Petitioner's contentions regarding Bonella that are relevant to the discussion of the third claim limitation.

Petitioner contends Bonella teaches a FLASH memory and associated controller and in the alleged "first mode of operation" Bonella used the DRAM buffer as a write buffer and periodically flushes the write data to the FLASH memory. *Id.* at 20 (citing 1005 ¶ 96; Fig. 1, Ex 1003 ¶¶ 94–97). On the other hand, Petitioner further contends that during a power loss event, the memory module flushes critical data to the FLASH memory—this is Petitioner's alleged "second mode of operation." *Id.* (citing 1005 ¶ 101, Ex 1003 ¶¶ 103).

In a third limitation, claims 1 and 15 recite "operating the volatile memory subsystem [operable] at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Petitioner argues that Bonella discloses this feature. Pet. 23–30. Petitioner contends Bonella discloses modes of operation supported by the system, including a power saving mode [Power Level 4] which saves power in part by reducing the frequency at which the DRAM is operating. Pet. 24–25 (citing Ex 1003 ¶ 116). Table 1, showing the power modes according to Bonella, is reproduced below.

TABLE 1

Partial List of ACPI Power States			
ACPI Power State	Power Source	Power Level (0-5)	Memory Module operational Condition
D0	Line/Battery	5	No operational restrictions, full power
D0	Battery	4	PCIe/DRAM performance reduction, no FLASH restrictions
D0	Battery	3	PCIe/DRAM DRAM wr buffer only, FLASH restrictions
D1	Line/Battery	2	DRAM in standby, FLASH idle
D1	Battery	1	DRAM in standby, FLASH standby
D1	Battery	0	DRAM off, FLASH standby

Table 1 (Ex. 1005, Table 1), above, shows Power Level 4 which operates at a reduced frequency that Petitioner contends is the claimed “third frequency.” Pet. 24–25. According to Petitioner, “A skilled artisan would understand a DRAM operating at a ‘reduced’ frequency in such a power saving mode [Power Level 4] to be operating at a clock frequency lower than the clock frequency at which the DRAM would operate in a normal operating mode, such as Power Level 5 of Bonella.” *Id.* at 25 (citing Ex. 1003 ¶ 118).

Specifically, Petitioner asserts

Bonella’s power flush algorithm (i.e., the “second mode”) would still be triggered during Bonella’s “power saving” mode of operation (i.e., when the DRAM was operating at a “third clock frequency”) if a power loss event occurred. Bonella teaches that the memory module’s backup power source is located within the memory module, Ex. 1005, ¶29, and that the external power source can be a “Line” or “Battery,” even under less than “full power” operation, *id.*, ¶46. One of ordinary skill in the art would understand that Bonella’s memory module, when operating under a “power saving” mode that reduced the DRAM operating frequency (i.e., a “third clock frequency”), could still lose its external power source and be forced to switch to the power loss

algorithm (i.e., the “second mode”). Ex. 1003, ¶119. Bonella thus teaches to one of ordinary skill in the art at least one situation where the ‘*volatile memory subsystem*’ operates ‘*at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency.*’

Pet. 25–26.

Patent Owner asserts that “Bonella does not teach that the alleged VMS [volatile memory system] operates at the alleged ‘third clock frequency’ during the alleged ‘second mode of operation.’” Prelim. Resp. 26. Petitioner asserts the “second mode of operation” is the power loss operation described in paragraph 101 of Bonella (Pet. 20), however, Patent Owner disagrees. *Id.* at 25. Contrary to Petitioner’s position, Patent Owner correctly explains, as a complement to that assertion, that the power source during that alleged “second mode of operation” is the battery uninterruptible power supply (“UPS”) and/or the capacitor (“CAP”) UPS because line and battery power from the alleged “host system” has been lost. *Id.* (citing Ex. 1005 ¶ 33).

Petitioner asserts that the DRAM (the alleged volatile memory system) operates at the alleged “*third clock frequency*” during Power Level 4. Pet. 20. As quoted above, Petitioner asserts “when operating under a ‘power saving’ mode that reduced the DRAM operating frequency (*i.e.*, a “*third clock frequency*”), could still lose its external power source and be forced to switch to the power loss algorithm (*i.e.*, the “*second mode*”).” *Id.* Petitioner does not point to any disclosure in Bonella, however, that indicates what frequency the DRAM is operating at during a power loss. Rather, as Patent Owner explains, the battery associated with Power Level 5 (alleged “first mode of operation”) and Power Level 4 (alleged “second

frequency”) is not the UPS battery so there is no suggestion in Bonella about what frequency the DRAM runs at when powered by the UPS battery. Prelim Resp. 25–26. Thus, we agree with Patent Owner’s assertions that “the Petition fails to show evidence that operating in a ‘power saving’ mode prior to Bonella’s ‘power loss algorithm’ has any effect on the operating frequencies during the ‘power loss algorithm.’” Prelim. Resp. 29–30.

Petitioner does not provide sufficient objective evidence sufficient to support a finding that the DRAM operates at the frequency of Power Level 4 when a power failure occurs during Power Level 4. Additionally, the conclusory statements of Petitioner’s declarant, which are essentially identical to the statements in the Petition, do not explain adequately how the limitation to a “third frequency” is met. Ex. 1003 ¶ 116–120; *see also, e.g., In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) (“[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations.” (citations omitted)); *Velandier v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) (“In giving more weight to prior publications than to subsequent conclusory statements by experts, the Board acted well within [its] discretion.”). For example, statements in the Petition and Maltiel’s declaration do not make clear where Bonella states that during a power loss the DRAM runs at the frequency of the power lever state immediately preceding the power loss, or whether anything in the Bonella reference teaches that alleged fact.

Petitioner also asserts that

[u]sing Bonella’s power reduction technique during the power loss algorithm would also have been the arrangement of old elements (Bonella’s power reduction mode and Bonella’s power

loss algorithm), each performing the same function it had been known to perform, in a way that yields no more than one of ordinary skill in the art would expect from such an arrangement (reducing power consumption during a power loss event, as suggested by Long and Ashmore).

Pet. 29 (citing Ex. 1003 ¶ 126). Petitioner further asserts “[o]ne of ordinary skill in the art would know that Bonella’s backup power supply is not unlimited and therefore would have been motivated to conserve power during such emergency backup operations in order to ensure backup of all unsaved data, or at least as much as possible.” *Id.* at 27 (citing Ex. 1003 ¶ 122). Petitioner has not shown, however, how or why Bonella’s power reduction modes are applicable during a power loss event, given that during a power loss event power is supplied by the UPS, and not the external Line/battery that supplies power under normal operations.

Petitioner asserts that Ashmore supports that contention that running at the frequency associated with Power Level 4 during a power loss would have been obvious because Ashmore “provides a method for reducing battery power consumption during a main power loss to reduce the likelihood of loss of user write-cached data in a write-caching mass storage controller.” Pet. 28 (quoting Ex. 1008 ¶ 9) (emphasis added). Specifically, Petitioner asserts Ashmore “only provide[s] battery power to the critical memory banks, but not to the non-critical memory banks, in order to reduce the amount of battery power consumed during the main power outage.” *Id.* (quoting Ex. 1008 ¶ 9). We are not persuaded by this cited disclosure.

The Ashmore citation relied upon does not state that the operating frequency of the memory bank is adjusted. Petitioner does not point to a motivation to adjust the frequency of the memory banks specifically, simply a general motivation to reduce battery power during power loss. Thus, we

are not persuaded Ashmore supports that contention that running at the frequency associated with Power Level 4 during a power loss would have been obvious.

Petitioner also asserts that Long supports that contention that running at the frequency associated with Power Level 4 during a power loss would have been obvious because Long “‘provide[s] a significantly slower clock signal to the processing circuitry’ *of a memory* ‘while the controller 40 moves data from the volatile-memory storage cache 42 to the flash-based memory vault 44.’” Pet. 28 (quoting Ex. 1011, 4:54–64) (emphasis added). We are not persuaded by this cited disclosure.

The Long citation relied upon does not state that storage cache 42 or FLASH-based memory vault 44 is clocked at a relatively fast clock signal. Petitioner leaves out the part of the quote that states that it is specifically the “‘processing circuitry *of the controller 40*” is run at a lower clock speed. That is, the cited disclosure notes that the processing circuitry of the controller is running at a relatively high clock speed and then is run on a significantly slower clock speed at a later time. This disclosure is silent as to whether storage cache 42 or FLASH-based memory vault 44 is running at the relatively high clock speed along with the controller. Thus, it cannot be determined whether storage cache 42 or FLASH-based memory vault 44 is forced to run at a significantly lower clock speed when the available power is reduced. Thus, we are not persuaded Long supports that contention that running at the frequency associated with Power Level 4 during a power loss would have been obvious.

Accordingly, for the reasons stated above, Petitioner has not shown there is a reasonable likelihood of prevailing in establishing that claims 1

and 15, and claims 2–14 and 16–30 that depend therefrom, would have been obvious over Bonella and Mills.

C. Asserted Obviousness over Bonella, Mills, and Ashmore

Petitioner contends claims 1–30 are unpatentable under 35 U.S.C. § 103(a) as obvious over Bonella, Mills, and Ashmore. Pet. 48–49. As explained above, we determine that Petitioner has not shown a reasonable likelihood that Bonella and Mills renders obvious the “third frequency” limitation of claims 1 and 15, even considering the disclosure of Ashmore. Thus, Petitioner has not shown there is a reasonable likelihood of prevailing in establishing the unpatentability of claims 1–30 of the ‘833 Patent as obvious over Bonella, Mills, and Ashmore.

D. Remaining Asserted Obviousness Grounds

As discussed above in the context of the obviousness analysis with regard to Bonella, Mills, and Ashmore, Petitioner has not shown sufficiently that Bonella, Mills, and/or Ashmore teaches “a volatile memory subsystem” that operates at a “third frequency,” as is required by each of independent claims 1 and 15. Each of Petitioner’s remaining obviousness grounds assumes that either Bonella or Ashmore discloses that limitation. Pet. 50–59. Petitioner bears the burden of proof of showing that limitation for each independent claim. Nonetheless, as shown above, none of the challenges Petitioner relied on to meet claims 1 and 15 shows sufficiently the required “third frequency.”

Thus, upon review of Petitioner’s analysis and supporting evidence and Patent Owner’s response and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it

would prevail with respect to: (1) the ground that claims 7 and 23 are unpatentable over Bonella, Mills, with or without Ashmore, and Larson; (2) the ground that claims 8–10 and 24–26 are unpatentable over Bonella, Mills, with or without Ashmore, and Windows 2000; (3) the ground that claim 16 is unpatentable over Bonella, Mills, with or without Ashmore, and Klein; and (4) the ground that claim 17 is unpatentable over Bonella, Mills, with or without Ashmore, and Maeda.

III. CONCLUSION

The information presented does not show that there is a reasonable likelihood that Petitioner would prevail at trial with respect to at least one claim of the '833 patent, based on any ground presented in the Petition. On this record, we deny the Petition for *inter partes* review of claims 1–30.

IV. ORDER

Accordingly, it is

ORDERED that that the Petition is *denied* as to all challenged claims, and no trial is instituted.

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