



ISSUE

Executive Millennium Report: 1999 Roadmap: Solutions and caveats

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overview

While the 1999 ITRS is a Roadmap for sustaining IC progress, the needed underlying manufacturing capability is based on solutions from equipment and materials suppliers. Addressing the list of potholes, detours, and even "red-flagged" roadblocks in the 1999 ITRS, CEOs and other executives from a broad range of semiconductor equipment and materials suppliers highlight their companies' new solutions and breakthroughs that may make the road passable, and describe ongoing work to tackle remaining problems.

A partial image of the Levitor 2000 single-wafer RTP reactor from ASM International

The International Technology Roadmap for Semiconductors (ITRS) tries to detail future technology in a field where "device linear features have decreased at the rate of 70% every three years ..." and to provide "a reference document for all semiconductor manufacturers." Deep within this document's tabulation of manufacturing metrics, it provides "guidance for suppliers of equipment, materials, and software" and "clear targets for researchers in outer years." While the ICs of the ITRS will come from the likes of Intel, NEC, and STMicroelectronics, innovative process tools to manufacture these ICs will come from such companies as Applied Materials, TEL, and ASM Lithography.



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The most important characteristic of 157nm lithography is that exposure at atmospheric pressure is possible.

Bill Arnold, chief scientist at ASM Lithography (right)

A characteristic of the ITRS 1999 edition is the ominous appearance of its "no known solution" red-boxed specifications, many of them associated with fundamental limitations to scaling of conventional CMOS. These become much like a red brick wall on the Roadmap's transition to technology for 70nm devices in 2008. Curiously, the red boxes have been out there in previous editions, but they are now more clearly in view, and the time and cost of travel will make for an extremely difficult trip.



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Knowing that most of the solutions to ITRS challenges will come from companies within the process industry, Solid State

Technology asked senior executives at semiconductor equipment and materials suppliers to brief us about Roadmap solutions and associated caveats. Additional quotes come directly from the 1999 ITRS (<http://public.itrs.net>).

Lithography

Lithography is the prime example of how the ITRS drills down to its equipment and materials underpinnings. "The growth of the industry has been the direct result of improved lithographic resolution and overlay across increasingly larger fields. Lithography is also a significant economic factor, representing >35% of chip-manufacturing costs and has heavy global interdependence for equipment and materials."

"Achieving a global consensus on an affordable post-optical technology is the grand challenge for lithography. The complexities and magnitude of investments require a new global model for research, development, and commercialization."

Resources and partnerships

Throughout the 1999 ITRS are examples of how the needed specifications for IC manufacturing stretch R&D resources. Steve Robinson, president of Shipley Microelectronics, says "Without consensus on a specific technology for post-193nm lithography, we must stretch and accelerate resources to research resists simultaneously for alternative exposure processes. A major challenge is difficulty attaining frequent access to 157nm and electron projection systems for resist development." (See Table 1.)

He adds, "Also, at the edge of purity and defect targets, we are working at the leading edge of metrology systems available today, but newer, more discerning metrology equipment is needed." The work at Shipley is also an example of the partnerships needed to address ITRS challenges; the company is collaborating with semiconductor manufacturer Samsung Electronics to develop photoresists for 193nm lithography.

CD control

"Development of processes to control minimum feature size to <7nm 3s" is one of five "difficult challenges" that lithography needs to meet just to reach 100nm by 2005 (see Table 2).

Ardy Johnson, VP of FSI's Microlithography Division, notes, "This means that the total contribution, across-wafer and wafer-to-wafer, of the resist process—combined stepper plus track results, but excluding intrafield and mask error—needs to be <6nm by 2002, <4nm by 2005, etc. Here, there are promising results."

As a result of a customer request for data on lithography cell performance for 180nm results, FSI, through hardware and process improvements, has shown better than 3.5nm 3s across-wafer, and 2.6nm wafer-to-wafer, CD control at ASM Lithography's demo lab. This was done with CD matching of <1nm across multiple develop bowls and bake plates, a critical requirement for high-throughput manufacturing.

Table 2. Selected CD control requirements				
Year	1999	2002	2005	2008
Technology node	180nm	130nm	100nm	70nm
MPU gate CD control (nm, 3σ, post etch)	14	9	6	4

Source: 99 ITRS Table 39

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It seems that gains in CD control are coming through resist-processing-system environment control. Eddie Lee, VP of process technology, SVG Track Systems, notes that, for example, managing the evaporation rate of solvent during photoresist spin coating contributes to CD control. Also, controlling the environment above a wafer surface using an enclosed thermal plate technology (e.g., anaerobic conditioning bake step) directly influences resist contrast. "Similar results can be achieved when this method is applied to low-k dielectrics," he says.

Sequence of generations

While the decisions will be applied "long term" on the Roadmap, "narrowing of Roadmap (lithography technology) options for 100-50nm nodes" is another difficult ITRS challenge that drills down to "achieving global consensus among technology developers and chip manufacturers" for the right optical (see "Why optics is forever in lithography," on p. 192) or next-generation (NGL) technique and paying for R&D (see "Entry of 157nm lithography and beyond" on p. 76).

Table 3. Lithography overlay requirements				
Year	1999	2002	2005	2008
Technology node	180nm	130nm	100nm	70nm
Overlay (nm, mean + 3σ)	65	45	35	25

Source: 99 ITRS Table 39, DRAM

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Bill Arnold, chief scientist at ASM Lithography, notes, "Pessimists stress the need for an emergency scenario, claiming that NGL tools will be needed for 70nm, possibly in production in five years. We feel, however, that the limit of optical lithography lies between 70nm and 50nm. It is not inconceivable that we will succeed in producing 35nm devices with lenses and photons."

Arnold's reasoning is that off-axis illumination and optical proximity correction (OPC) on masks is just beginning. Offering a reasonable scenario to the ITRS challenge, he says, "It's most likely that 100nm will come with 193nm ArF laser sources; with phase-shifting masks and very-high-NA lenses, 193nm may be able to address critical layers of the 70nm technology node." Along this route, ASML has reported lithography overlay to at least 25nm with further improvements seen, but the techniques are still proprietary. Arnold will only say, "These involve our new alignment system ATHENA, and improvements in the metrology

Selected PSM requirements				
Year	1999	2002	2005	2008
Technology node (nm)	180	130	100	70
Attenuated PSM transmission uniformity (±% if target)	4	4	4	4
Alternating PSM mean deviation from ±180°		2	2	1

Source: ITRS Table 4

frame and interferometry." (See Table 3.)

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Beyond this, Arnold believes that, compared to NGL techniques, 157nm lithography has highly attractive characteristics. "The most important is that exposure at atmospheric pressure is possible, whereas vacuum is required for all NGL techniques. The greatest challenge in exposure with 157nm radiation is keeping the beam free of oxygen that is not transparent to 157nm." Among the companies directing their efforts toward 157nm technology, ASML (which is also involved with EUV and electron projection lithography programs) and Carl Zeiss plan to complete a concept study by mid-2000 with the resulting first 157nm systems entering production fabs in 2003.

The ITRS has identified three wavelengths beyond 248nm as vital to meeting market requirements well into the next decade and beyond—193nm, 157nm, and 13.5nm. As a result, points out Bob Akins, president and CEO of Cymer Inc., both lithography tool manufacturers and light source providers such as Cymer, are aggressively investing in advanced development programs spanning these wavelengths. Only through this investment in fundamental research and product development will chipmakers meet the design rule targets outlined by the Roadmap. The industry has intensified its search for understanding how the critical wavelength transition points (e.g., 248nm to 193nm, then 193nm to 157nm) must be managed to enable the aggressive ongoing geometry shrink. A collaborative decision-making process, including chipmakers, lithography tool vendors, and leading source suppliers like Cymer, is ongoing.

Role of OPC/PSM

"Optical mask fabrication with resolution enhancement techniques (RETs)," including OPC and phase-shift masks (PSMs), is also on the Roadmap's list of 10 most difficult challenges for lithography. Many see OPC and PSM as keys to the most cost-effective, albeit still expensive, approach to advancing lithography; Motorola, Lucent, and TI are all using PSM for near-100nm production. "Already, prudent application can reliably generate feature sizes $\leq 90\text{nm}$ using 248nm established tools," notes Yao-Ting Wang, CTO at Numerical Technologies.

Already, prudent application can reliably generate feature sizes $\leq 90\text{nm}$ using 248nm established tools.

Yao-Ting Wang, CTO at Numerical Technologies (right)



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But part of the challenge to such maskmaking is "development of the infrastructure for this relatively small market [ITRS]." Wang indicates that RET can address this difficult challenge, but "to realize the full potential, the industry must break down walls between design and manufacturing groups that impede the flow of information through all processes of design, verification, maskmaking and fabrication." This has been done in academia, where engineers at MIT Lincoln Laboratory have fabricated isolated transistor gate patterns with 55nm CDs using double-exposure PSM and a Canon 248nm stepper. (This work did not report on CD control or line-edge roughness.)

The MIT work has shown that the infrastructure required must include seamless vertical integration of all manufacturing stages, including highly accurate, calibrated process models that accurately simulate optical distortions and the mechanical effects of etching and photoresist. It also requires compatibility between various tools used for physical design, maskmaking, inspection, verification, and wafer exposure. In addition, it requires fast, intelligent software algorithms that can efficiently apply OPC and PSM only where necessary so as to minimize complexity and improve yield and productivity.

As the 1999 ITRS recognizes with its more extensive specification of mask requirements (see "Innovations for characterizing phase-shift mask materials" on p. 78), use of OPC and PSM is another part of the infrastructure. "This includes well-designed automated inspection tools using calibrated process models that can differentiate between critical defects and tolerable ones. Integrating such software into mask-inspection systems helps curtail the added complexity that comes with OPC and phase shifting," says Wang. "There must also be a direct software link between physical design and wafer fab so designers can check layouts against silicon. The same process models used for automated mask-inspection tools should also supply the simulation engine behind a silicon-vs.-layout checking tool, to determine where OPC is needed and whether it works when applied."

Wang notes, "Existing maskmaking technology does not limit the ability of our technology solution to meet ITRS demands, because we avoid the 'red boxes' associated with use of nonprinting features (e.g., assist features and scattering bars)." (See Table 4.) "In addition, the use of alternating-aperture phase-shifting (AAPSM) loosens the specifications for CD uniformity on isolated lines; the ITRS supports this (i.e., the 2004 16nm specification for AAPSM on the near-term Roadmap is the same size as the achievable CD uniformity for binary masks in 1999). As for the 2008 red wall predictions, we expect that the introduction of advanced e-beam mask-writing tools, focused ion beam repair tools, and DUV inspection tools will address these issues in time to meet the Roadmap's implementation specifications," Wang says.

Indeed, the ITRS states "Continuous improvements in maskmaking technology (mask writers, inspection, repair, and substrates) are essential to support the technical and manufacturing needs of optical lithography below 180nm." (See "Revolutionary pattern generation" on p. 80.)

Surface preparation

The ITRS states that: "wet chemical cleaning technologies are favored because many inherent properties of aqueous solutions facilitate the removal of metals and particles," but surface preparation, which the ITRS ties closely to defect reduction, is not without its challenges. Many of these are "crosscut" issues involving emerging materials, for example



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higher-k materials that require interface control and copper that, among other things, present special resist-stripping requirements." (See "Dry chemistry alternatives.") "Fundamental changes to surface preparation processes will likely be required." In addition, "in all areas of surface preparation, a balance must be achieved between process and defect performance, cost, and environmental issues." (Metrology is another very significant ITRS "crosscut" technology. See "A partnering approach to metrology" on p. 83.)

Surface cleaning will have to be integrated [to control dielectric layer thickness.]

Daniel G. Queyssac, president and COO of ASM Front-End Business. (right)



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Roger Carolin, CEO, CFM Technology, says, "With aqueous cleans for copper, there are advantages to fully controlled wet-processing environments that include in situ process monitoring, dissolved gas control, and point-of-use chemistry generation—fully integrated wet process sequences or dry-in, dry-out, single-tank processing." For example, dissolved oxygen must be excluded from the rinse water to avoid copper corrosion. In addition, the chemical cleaning process must be performed in a dark environment to avoid light-induced electrochemical reactions that will cause copper to be etched where it is in contact with p-type portions of a transistor structure and redeposited with n-type. "Such a process must be performed using single-pass chemistry to avoid cross-batch contamination due to copper buildup in the cleaning bath," says Carolin. "The process is most effective when megasonic energy can be applied during chemical treatment and during rinse to improve the effectiveness of polymer removal from complex topography, and it should include an integrated IPA dry to avoid watermark defects."

Another aspect of wafer cleaning associated with copper processing involves cleaning wafer backs without affecting front layers prior to lithography to enhance the process latitude necessary to extend optical lithography. Franz Sumnitsch, president and CEO, SEZ, says, "In cooperation with International Sematech, we have developed a copper interconnect process to enhance depth of focus for critical advanced lithography operations. It yields a flatter wafer, free of hot spots, enabling greater process yields at smaller geometries. The key future challenge is 300mm and pre-lithography cleans because with the larger wafer size, there is a greater effect of the hot spot on process yield."

On the environmental, safety, and health side of the ITRS, "reduced chemical use, chemical and water recycling, and alternative process technologies" are required to provide ESH and cost-of-ownership (COO) benefits. Citing just one Roadmap example, "Ozonated water processes show much promise as replacements for sulfuric acid-based resist strips and cleans." (See "Critical cleaning with ozonated water" on p. 84.) Also, additional COO benefits can be realized by footprint reduction, fluid flow optimization through modeling, and in situ sensor-based process control.

Deposition and materials

Integration, cooperation, and good old-fashioned sleeves-rolled-up process development will make the ITRS predictions a reality, according to the executives at companies that will be providing the front-end processing tools and knowledge to make it happen. Low-k dielectrics and copper interconnects will rely most heavily on process integration. Promising new developments such as atomic layer CVD and upgrades to existing processes like RTP will allow advances in several areas.

Low-k dielectrics

Until the recent IBM/Dow Corning announcement (see p. 42), low-k dielectrics didn't make headlines in the mainstream press like counterpart advances in copper interconnect, but they are just as critical for staying on the Roadmap (Table 5). Big players are focusing heavily on low-k materials, with alliances being formed to address the many challenges.

Table 5. Interconnect technology requirements						
Year	1999	2002	2005	2008	2011	2014
Technology node	180nm	130nm	100nm	70nm	50nm	35nm
Number of interconnect levels	6-7	7-8	8-9	9	9-10	10
Barrier/etching thickness (Cu wiring)	1.7nm	1.3nm	1.1nm	0.9	0.8	0.7
MPU interlevel resistor effective dielectric constant	3.5-4.0	2.7-3.0	1.8-2.2	1.5	1.3	1.1
FRAM interlevel resistor effective dielectric constant	4.1	3.0-3.5	2.5-3.0	2.0-2.5	1.7-2.0	1.5-1.8

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Farhad Moghadam, corporate VP and GM of Applied Materials' Dielectric Systems and Modules Product Group, sees integration as the key to progress in low-k dielectrics. "Over the past 12 months, low-k development work has expanded from single-level damascene into multilevel structures. This multilevel integration work has redefined the requirements for a low-k dielectric, proving that materials with thermal-mechanical properties most similar to silicon oxide are optimal because they are simpler to integrate. FSG (k = 3.5) has proven extremely effective for achieving an initial reduction in capacitance with the least integration risk. As the industry moves to smaller geometries, however, materials with a lower k value (<3.0) will become essential."

ASM America, another provider of tools in multiple process areas, also sees integration of process subsets as critical.

According to Daniel G. Queyssac, president and COO of ASM Front-End Businesses, "The dielectric layer thickness for future device generations will be counted in numbers of atomic layers. The control and deposition of these layers will be highly dependent on surface preparation. Surface cleaning will have to be integrated, since it will not be possible to do it outside for controllability."

FSI expects spin-on dielectric (SOD) materials to move us along the Roadmap. Ajit Rode, senior VP and GM of FSI International's spin-on dielectric operations says, "The CALYPSO Low-k dielectric processing system is designed for the SOD marketplace, initially addressing the dielectric requirements at 0.13 μ m, continuing to below the 0.07 μ m technology node. Modular design enables the system to process a wide selection of the SOD materials that will be required to address the multiple technology nodes of the future." With the solutions to the challenges on the Roadmap so undefined, process flexibility is likely to be critical.

Luc Van den hove, VP of Silicon Process Technology at IMEC, sees the same uncertainty. "There is no consensus yet on low-k materials. They are still subject to a lot of materials characterization," he says. "That's why IMEC is doing research on the materials and process steps related to the Cu/low-k modules as they are needed for the 100nm node." IMEC is also working on metrology for the complex structures of low-k dielectrics. "The lowering of the k-value is achieved by the increase of free volume in the matrix material or by adding porosity. Therefore, measurement of the free volume and the characterization of pore distribution, both in size and in shape (open or closed pores), are essential. To do this, IMEC has developed a wafer-level porosimetry tool based on spectroscopic ellipsometry. The technique allows a direct study of the effect of process steps on the dielectric film properties."

Low-k dielectric processing is also an area where CMP work remains. According to Chris Smith, the VP and GM of Applied Materials' CMP Product Group, "Currently, low-k ILD layers typically have a cap that avoids CMP-specific integration issues. As caps are thinned or eliminated, new CMP solutions will be needed to planarize and clean the low-k material after CMP. These solutions will involve both polishing advances and changes in consumables."

Copper interconnects

Integration is identified as the key to success as copper interconnects contribute to Roadmap solutions. (See "Integration is helping to make the road a safer place.") Both Applied Materials and Genus see the barrier and seed layers as a significant challenge for copper interconnects (see Table 5 on p. 84).

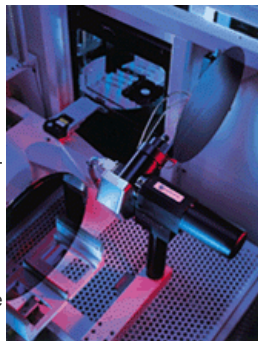
At Applied, Fusen Chen, VP and GM of the Copper/Aluminum Systems and Modules Product Group, expects "a shift from PVD to CVD technology, since CVD enables thinner, more conformal barrier and seed layers. The barrier will likely be the first to transition to CVD, although the choice of material is still unclear—with tungsten nitride, titanium nitride, and tantalum nitride still under evaluation. For the seed layer, the technology transition is expected to be more gradual. Also, integration of the barrier and seed layer within the same system will be critical to ensuring low resistivity and good adhesion of copper to the barrier." The two process sequences being explored are:

the use of a CVD barrier and a CVD seed with CVD fill of vias and electroplating fill of trenches; and
the use of a CVD barrier with a PVD seed and an electroless seed enhancement with electroplating fill.

Integration is vital in the Cu interconnect process area, too, for technical and economic reasons. According to Chen, "To attain a precision process for repeatable gap fill and high yield in electroplating, closed-loop chemical management is essential for process control, as is the integration of key process steps such as bevel cleaning and annealing of copper films. This integration eliminates the batch furnace bottlenecks that inhibit process flow, increases productivity, and minimizes wafer contamination for higher yield."

A 300mm wafer being handled in the front end of a Steag wet bench system. Berkeley Process Control made the wafer transfer twist and rotate mechanism

Genus Inc. also sees PVD barrier and seed layers running out of gas before the 0.10 μ m node due to step coverage concerns. "The step coverage is such that a large fraction of the cross section of the Cu will be used for the barrier, which limits the cross-sectional conductance for high-conductivity Cu," say Tom Seidel and Carl Galewski of Genus. Their solution is PECVD tungsten nitride, compatible with low-k dielectrics. Seidel and Galewski see benefits to other line processes. "In addition to the ability to offer good adhesion to CVD Cu, a key feature of WN barrier technology is the ability to simplify the CMP process. The removal rate of WN and Cu are similar, while TaN and TiN have an 8-10x more difficult removal rate than Cu." An alternative to PECVD will be atomic layer deposition (ALD) barrier technology, which they have demonstrated with TiN and WN. ALD barriers can provide 100% step coverage at low temperatures (<400°C), as well as a range of composition and resistivity.



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Deposition

Incremental improvements in tried-and-true deposition techniques continue to improve the industry's capability, but more than one player sees new ALD processes as critical to keep up with the Roadmap.

Genus agrees with ASM's view (see "Atomic layer CVD for thinner films") that ALD is a necessary technology for meeting the ITRS. Seidel and Galewski said, "Genus recognizes the need for developing thinner films (<100Å) for the semiconductor industry starting in 2000 to support scaling to 0.10 μ m in production for 2003 and beyond. These films must have highly conformal capability with dimensional control at the atomic level. ALD is a key technology for achieving this capability. Genus' ALD roadmap includes multiple dielectric films, Al₂O₃, TiO₂, Ta₂O₅, and ZrO₂."

Atomic layer processes are not the only deposition technologies contributing to Roadmap solutions. CVD and PVD will continue to meet future needs. Bernard Culverhouse, VP, marketing at Trikon Technologies, says, "The new ITRS

expects DRAM makers to stay with subtractive AI technology down to 0.1µm, requiring k values of 3.0 at 0.13µm for 2002 product shipments. Trikon already meets these requirements [with CVD], delivering dielectric materials with k <3 at 0.18µm." Trikon's next-generation ionized PVD module, in advanced development, will address W-plug and Cu metal schemes.

Shallow junction formation

Ion implantation and thermal processing have become sophisticated processes, but more capability can be squeezed from them. Any big developments in shallow junctions are not imminent.

Rapid thermal processing has allowed great strides in processing capability for the last several years. Queyssac, of ASM Front-End Businesses, believes that continued RTP process improvements can keep up with the Roadmap. He describes a new product: "We are perfecting a new proprietary RTP technology that uses gas-bearing principles to hold a wafer a few tenths of a millimeter between the surface of two large refractory-material blocks that are heated to the desired process temperature. Almost 90% of the heat generated is transferred to the wafer. The block material itself has excellent thermal conduction, guaranteeing uniform heating of the wafer. The key intrinsic advantage to the technology is that since the heat transfer is applied through conduction and not radiation, there is no sensitivity to emissivity on either the front or back wafer surfaces. This results in the reduced use of test and setup wafers, which is a significant cost and cycle time reduction factor." This tool, the LEVITOR 4000, also provides very fast cool down—a critical feature to control transient-enhanced diffusion (TED) in ultra-shallow junctions. This targets the ITRS projection of <300ohms/square sheet resistivity at the 30nm technology node.

Eaton Semiconductor anticipates a proliferation of options for junction formation. "It is now clear that reducing the implant energy, annealing time, and dose are of primary importance for achieving the shallowest junctions. Since there are several non-unique combinations of choices for implant and annealing parameters that yield the same junction solutions, it is essential to select solutions that optimize manufacturability and minimize costs," says a chief scientist at Eaton. Still, the technical options are critical for increasingly stringent requirements. These include:

preamorphization of the junction with Ge to enhance junction activation;
the use of heavier, slower-diffusing dopants such as Sb and In for super-steep retrograde (SSR) channels;
the use of non-dopant species (e.g., N and Ar) for altering the gate oxide growth rate, which is needed for producing multiple gate oxide thicknesses on the same wafer as integration increases; and
increased use of "chaining" (using multiple sequential implants) for n-well or p-well formation, which reduces processing steps and results in smaller threshold voltage variations.

Table 6. DRAM stack capacitor films technology requirements						
Year	1999	2002	2005	2008	2011	2014
Technology node	130nm	150nm	100nm	70nm	50nm	35nm
DRAM capacity	1G	3G	3G	24G	64G	192G
Capacitor structure	Cylinder M3	Podestal MIM	Podestal MIM	Podestal MIM	Podestal MIM	Podestal MIM
Capacitor dielectric material	Ta ₂ O ₅	Ti ₂ O ₅	BST	F + BST	***	***
Capacitor dielectric constant	22	50	250	700	1500	1500

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Advanced substrate and isolation technologies are also enabled by ion implantation technology. According to Eaton, "The ITRS has identified high-dose, high-energy buried layers as one of the enhanced substrates that will be used for advanced device fabrication. Buried layer substrates formed by high-energy ion implantation and RTA significantly improve latch-up immunity in aggressively scaled CMOS circuits, and improve the gettering capability (metals and oxygen) of bulk wafers. For 300mm wafers, buried layer substrates will be a low-cost alternative to expensive epitaxial silicon wafers, or an inexpensive performance enhancement to wafers."

Gate materials, high-k dielectrics, and capacitors

The challenges and options for high-k dielectrics and the related gate and capacitor processes are many, and there is still considerable debate about the various solutions. One point of agreement is the need for process integration and cooperation. One technical trend where there seems to be agreement is in the need to shift from silicon-insulator-silicon structures to metal-insulator-metal structures. Much of the current work is focused here.

IMEC's approach is an indication of the magnitude of the task of developing gate dielectrics. Marc Heyns, department director of IMEC's Advanced Surface Preparation, Thin Film, ES&H, and Gate Stack organization, reports, "Currently, there is no consensus on the material that can be used as alternative gate dielectric. Development in such a critical layer in an IC is only possible through large-scale international collaboration. That is why we have set up an Industrial Affiliation Program to develop gate dielectrics and gate electrodes (including metal gates) for sub-100nm devices. Within this program, IMEC wants to develop a manufacturable process for thin films (equivalent oxide thickness [EOT] <1.5nm) with low defect density and accurate thickness control. The gate stack must be integrated in the (n and p) MOS transistor, with the possibility to down-scale the stack to 0.5nm EOT." Their work points to ALCVD as the solution. Heyns adds, "ALCVD results in perfect thickness and uniformity, as well as composition control over large substrates. Therefore, we aim to use this technique to deposit very thin, high-k dielectric layers such as (but not limited to) Al₂O₃, ZrO₂, HfO₂, and their silicates for use as alternative gate dielectrics."



NumeriTech's iN-Phase automated phase-shifting toolset is used to apply phase-shifting structures to an IC design.

NumeriTech's iN-Phase automated phase-shifting toolset is used to apply phase-shifting structures to an IC design.

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Genus also sees an atomic layer process as the answer for high-k dielectrics. It has developed a process for Al₂O₃ that provides atomically uniform films with 100% step coverage on very-high-aspect-ratio features. The company expects to introduce ALD of higher-k dielectric materials (e.g., TiO₂, Ta₂O₅, ZrO₂) later in 2000.

Genus is also working on a migration from tungsten silicides to tungsten for a gate metal material, which addresses the need for lower-resistivity gates. "A tungsten gate process will provide a factor of 8x lower resistivity than WSix, and a factor of 1.7x lower resistivity than silicides made from TiSix or CoSix," say Seidel and Galewski. They add, "Tungsten gates also require a process integration sequence that allows for local oxidation of the gate oxide at the edge of the gate. This ensures gate oxide integrity and high field performance. This process provides a simple integrated process by the thermal conversion of WN to W, with the simultaneous formation of a WSi_n barrier at the polysilicon interface." Lower resistivity, improved gate oxide integrity, and simultaneous barrier formation make this an appealing option.

As in most other process areas, Applied Materials sees integration as a key. The company is developing an integrated approach that combines electrode anneal/nitridation, tantalum oxide deposition, and tantalum oxide anneal in a single system. This is for the capacitor technologies needed as DRAM manufacturers begin implementing high-k tantalum oxide dielectric films in memory cells. Dan Carl, VP and GM of Applied Materials' Capacitor Product Group, sees the need to improve memory capacitance by replacing the silicon electrode of a metal-insulator-silicon (MIS) with a metal electrode such as TiN or Ru, for metal-insulator-metal (MIM) structures. Genus is also working on this evolution to MIM structures. The company, which has developed WN (CVD and PECVD) as the lower electrode in a MIM capacitor, cites the reduction of capacitance due to the elimination of depletion effects in a silicon electrode as one of the greatest opportunities. (See Table 6 on p. 94.)

Etch

Material science expertise and clever process technology appear prominently in the upcoming developments in etch (see "The challenges when etching new materials" on p. 94). These processes, along with lithography, are what drive feature size reduction, so this is the right place to focus significant development effort.

Hitachi Ltd. is addressing challenges in etch processes at the 100nm node and beyond with ultra-high-frequency-electron cyclotron resonance (UHF-ECR) and time modulation (TM) bias technology in their equipment. The system controls plasma uniformity and stability by adopting a semigap plate antenna. The UHF-ECR plasma-etching system controls ions and radicals in the plasma independently for better process control and performance. High productivity has been realized by improvements in the wet-cleaning schedules resulting in reduced operating costs. The TM technology provides advantages for gate materials, producing high selectivity between gate dielectric layers and metal gate electrodes. Application of TM bias also produces better vertical etching while reducing profile defects. Charging damage, known as electron shading effect, which may occur in the manufacture of devices with finer pattern structures, has also been effectively reduced using TM bias.

Akio Yamamoto, senior engineer at Hitachi Ltd., remarks that "Ultra-high-frequency source design and TM bias are just a couple of the innovative technologies we are working on at Hitachi. We are prepared to meet the future advanced etch requirements for our customers as outlined in the ITRS."

"These products deliver both high anisotropy and high selectivity on a level not possible with other etching systems. The TM bias program is designed to be loaded into existing systems by a simple conversion of a conventional RF power source to a new RF power source with TM function with a minor change to the software. The Hitachi UHF-ECR etching



Asyst Technologies' VersaPort 2200 modular 200mm wafer I/O interface.

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system and TM bias will prove useful for processing devices of 100nm geometry and beyond," said Yamamoto.

Culverhouse of Trikon Technologies also sees shifts in processes required to meet Roadmap requirements. "The latest ITRS calls for much smaller features, higher aspect ratios, and more precise profile control as processing moves from reactive ion etch to high-density plasmas (at ~130nm) and the use of hard masks in place of photoresists. Trikon's inductively coupled plasma (ICP) system has been used in dry-develop processes that could replace, or extend, conventional photolithography." Trikon and its partners have provided an existence proof for the technical feasibility of future technology nodes. "Features as small as 25nm have been dry-developed in bilayer resists using Infineon Technologies' CARL methodology and Trikon's developmental work, which was carried out in conjunction with Clariant GmbH, International Sematech, and Infineon," reports Culverhouse. "These features are not required by the ITRS until 2011."

Characterization and defect detection inside trenches and vias with increasingly high aspect ratios are highlighted as major areas of concern in the Roadmap, points out Don Kania, VP and GM for semiconductor products at Veeco Instruments. He reports that the company's atomic force profilers and microscopes have been used to characterize 180nm diameter via features with >13:1 aspect ratios. This suggests a solution for a "yellow box" (solutions being pursued) at 180nm technology. Also, polysilicon features down to 120nm diameter have been measured, changing one of the "red-box" (no known solution) areas for 130nm technology to a yellow. Atomic force tips as small as 70nm can be made reproducibly in useful lengths, Kania reports, and research continues on alternative materials for fine tips, including carbon nanotubes and stiffer materials, such as diamond, which could push the envelope even further into the now-red region.

Inside the factory

Factory integration and management issues are perhaps the most difficult to grasp. The metrics in more specific process areas (linewidth, gate oxide thickness, junction depth, etc.) are easier to understand, and they are a direct outcome of process variables. The quantities used to measure the functioning of a factory (turnaround times, equipment extensibility, scrap reduction, etc.) are definitely the results of factory strategies and technologies, but it is a challenge to quantify cause and effect. For example, how much does software standardization improve the time required to install a new piece of equipment? Here are some ideas on upcoming challenges in areas like this.

Process control

Process control has been the mantra for generations of IC production, but this is still an area where advances are needed. In-line instrumentation is prevalent these days and is a step up from off-line analysis, but another step is needed, according to Dave Fredlake and Terry Turner of Advanced Energy Industries. As they put it, "The end customer must embrace a philosophical shift away from stopping an entire process during an in-line measurement step. The shift must be toward a continuous manufacturing flow that is dependent on processing real-time, wafer-to-wafer data. Imagine the price of a car if the automobile industry still operated this way. Why stop a well-behaved process just to verify that the process is fine?"

In situ measurements exist at some points in the fab, but these are often not very useful. Fredlake and Turner observe, "Current typical usage of in situ measurements does not include reducing the data to forms that give the operator a green light or red light after each wafer. Yet, unless there is a go/no-go signal from in situ instrumentation, the process cannot run continuously. However, with a clear go/no-go signal, the process can be stopped only when absolutely necessary (e.g., to bring the process back within its control limits). Taking it one step further, envision generating a specific list of diagnostic instructions based on up-to-the-minute tool conditions instead of relying only on experience to fix a problem." They see RF in situ sensors as one solution to this challenge. An RF signature can reveal subtle process shifts by looking at V, I, and f of RF power and four harmonic frequencies, for example. This gives 15 components that can be used to develop a detailed polynomial equation that models a process. All of this, though, must result in an easily interpreted output.

"Manufacturing environments have enough problems—learning a new language should not be one of them," say Fredlake and Turner.

The need for real-time process control is echoed throughout the industry. Carl Fiorletta of Adventa Control Technologies states, "As the industry moves forward with smaller features, larger wafers, and more complex processes, we expect to see continued growth in the use of run-to-run and real-time process control in semiconductor manufacturing."

One challenge posed by the ITRS in the area of factory optimization is to "reduce product and operation cost; minimize waste and scrap; and reduce the number of nonproduct wafers." Jon Goldman, president of Jon Goldman Associates, has this view: "If you're sure a piece of production equipment is running properly, why would you use test wafers? Because they are currently the best (only) way to verify that equipment performance is in spec. But there is a better way: implementing comprehensive data capture of all relevant process tool variables, and using this information to develop usable equipment/process models that describe the normal operation. In my opinion, a heavy (and largely ignored) burden falls upon the equipment supplier to help in characterizing data from healthy and poorly performing equipment." This is a large task, but it is the kind of effort required to keep process control progress on the Roadmap.

Metrology challenges

Integrating metrology into a manufacturing tool is a way to monitor or even optimize performance. This requires a new type of business cooperation between process equipment and integrated metrology (IM) manufacturers by creating integration packages (hardware, software and process control methods), and close cooperation in combined sales, service and application support.

An example is the integration of Nova's NovaScan 210 onto Strasbaugh's 6DS-SP CMP polisher in 1995. Following this cooperation, IM tools were integrated on practically all CMP equipment. Recently the NovaScan platform is being

expanded to CVD and photolithography process equipment, believes Moshe Finarov, director of technology for Nova.

The IM concept will migrate to all manufacturing processes in the near future, says Finarov, mainly driven by the transition to 300mm wafers, copper interconnections and fast adaptation of advanced DUV photolithography, all requiring advanced process control.

There are two general trends that can be observed for off-line or stand-alone metrology (SAM). One is the combination of several metrology methods to broaden the application range, and the second is the unification of metrology and inspection equipment being used in different places in the fab.

Different examples of these trends include: combination of ellipsometry and reflectometry in thin film metrology tools, the combination of bright field and dark field scanning methods in microdefect inspection, and the combination of overlay measurements with optical CD control.

Table 7. Material-handling systems technology requirements						
Year	1999	2002	2005	2008	2011	2014
Technology node	180nm	130nm	100nm	70nm	50nm	35nm
Wafer diameter	200 mm	300 mm	300mm	300mm	300mm	450 mm
Transport system types and utilization in factory	Interbay and intrabay	Interbay and intrabay	Some interbay and some integrated	One integrated system	One integrated system	One integrated system
Throughput (moves/hr)	1000	1200	1500	2170	2270	2700
Interbay transport (moves/hr)	150	170	200	N/A	N/A	N/A
Stocker throughput	300	240	300	332	362	350

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Such combinations make SAM tools more powerful, but also cause unprecedented complexity and higher costs. Stand-alone metrology and inspection operations become more and more expensive and often prove a bottleneck of the production pipeline. All this pushes IC manufacturers toward IM dedicated to specific applications.

Integrated metrology is becoming a reality in accordance with the ITRS statement that metrology migrates from stand-alone to in situ and inline metrology solutions. Its potential will be fully used when tool manufacturers start to use the IM data for adjusting the process in real time. This requires investment in such fields as advanced process control—methods and algorithms, communication between process equipment and metrology tools, data transfer between different processes of the fab, and a comprehensive means for data analysis fab-wide, according to Finarov.

Factory management

Applied Materials and other toolmakers are starting to offer "process modules," which are process and inspection systems grouped together to perform particular production sequences. According to Sass Somekh, senior VP, Office of the President, Applied Materials, "Process modules offer chipmakers the potential for lower overall development costs. Having a supplier-developed baseline process sequence that can be customized for specific designs and requirements will save chipmakers both time and money, since they reduce or eliminate the need for each chipmaker to separately develop a new process flow." Somekh even sees a radical change in how equipment and processes are specified. "Chipmakers might even qualify process modules in parallel with their circuit design process, assured that the modules will build their device to a set of known specifications." This would be a significant shift in the current view, in which processes are specified by outputs such as deposition or etch rate.

Table 8. Production equipment technology requirements						
Year	1999	2002	2005	2008	2011	2014
Technology node	180nm	130nm	100nm	70nm	50nm	35nm
Wafer diameter	200mm	300mm	300mm	300mm	300mm	450mm
Relative capital cost		<1.3x of 200mm	<0.85x of previous node	<0.35x of previous node	<0.85x of previous node	<1.3x of 300mm
Relative consumables, gases, chemicals, exhaust, emitters, and utilities		<1.0x of 200mm	10% less than previous node	10% less than previous node	10% less than previous node	10% less than previous node
Relative equipment footprint		<1.0x of 200mm	<0.85x of previous node	<0.35x of previous node	<0.85x of previous node	<1.0x of 300mm
Relative maintenance and spares cost		<1.0x of 200mm	<0.85x of previous node	<0.35x of previous node	<0.85x of previous node	<1.20x of previous node

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Additional approaches to optimizing manufacturing productivity are driven specifically by the shift to 300mm wafers. Mihir Parikh, chairman and CEO of Asyst Technologies, sees the shift taking us across a threshold, requiring new approaches. "One 300mm manufacturing enabler is logistics management of materials in the fab such as wafer cassettes and containers. Logistics associated with current 200mm manufacturing is based on transport automation designed primarily for fab-wide material movement and storage in automated stockers—typically at the end of bays. Equipment loading is

primarily performed by human operators carrying wafer cassettes or containers. Manufacturing with 300mm wafers, which involves greater product weight and value, will result in unacceptable human ergonomic and safety issues. These factors will cause a discontinuity in 300mm manufacturing. Logistics automation will be aimed at equipment productivity through automated equipment loading, requiring the optimization of the equipment-integrated automation with the equipment-loading, logistics, and material-handling systems." (See Table 7 on p. 108.)

Parikh also sees integration as a key to the success of automation. Many of the subsystems (mini-environments, SMIF interfaces, robotics, auto-ID systems, fab connectivity software, etc.) are in widespread use, but their deployment has been haphazard. "IC manufacturing using 300mm wafers will require integrating such subsystems into an optimized system," believes Parikh. "Only then can significantly higher manufacturing productivity be achieved. These productivity improvements can be achieved through reduced wait time before wafers are processed or inspected, improved equipment utilization and productivity, a reduction of contamination and misprocessing, improved product yield and quality, reduced dependency on human operators, improved labor utilization, and reduced human-generated errors." Parikh also sees open architecture solutions as a critical part of true optimization of fab-wide automation.

The latest version of the ITRS brings to mind the same type of issues being faced by the disk drive industry.

Arnold Steinman, CTO of Ion Systems (right)



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In a related issue, standardization is seen to be critical for maximizing factory output. Jack Ghiselli, president of GW Associates, stresses a particular approach to standardization as well. "A methodical approach to implementing standards is missing from the semiconductor industry's arsenal for efficient technology deployment. The industry moves fast and leaders must begin experimenting with possible solutions long before standards have reached an approved and released status. Sometimes, equally valid and appropriate ways of dealing with leading-edge production techniques are developed and become part of an organization's infrastructure. This has been the case with the 300mm transition. Understandably, equipment suppliers are reluctant to commit huge amounts of R&D dollars year after year to implement an automation strategy that may or may not win over the end-user community." Ghiselli sees a solution to this with a "proof-of-concept" strategy, in which standards are verified and validated. "Industry-sponsored support for proof-of-concept standards evaluation would go a long way to usher in cost-effective advances in capital equipment and fab integration strategies, while still leaving plenty of room for innovation and true value-added features," says Ghiselli (see Table 8 on p. 112).

Gas handling

An example of the industry's efforts to meet current and future environmental requirements is Hitachi's catalytic decomposition system. A dual showerhead pre-spray abates 99.9% of TEOS gases in this equipment. Perfluorocompounds (PFCs) are removed by mixing them with water and air, and then heating the mixture to 700°C. A patented catalyst technology breaks down PFCs into CO₂ and HF gas. A post-packed tower removes all HF gas from the effluent, and only CO₂ is released to the facility exhaust. The catalyst cartridges are recycled by Hitachi, and the spent catalyst is reused in steel manufacturing, further reducing the impact on the environment.

Millipore sees an opportunity to address the ITRS factory integration challenge to "control production equipment and factory processes to reduce parametric variation." The company has developed IntelliFlow, a digital mass flow controller with embedded diagnostics. It uses a digital signal processor instead of analog electronics. This flow controller results in improved responsiveness, accuracy, and repeatability. Its dual-range capability eliminates the need for multiple gas lines, which reduces cost and can also reduce parametric variation.

John Sullivan, executive VP of technology at MKS Instruments, foresees a need for chemically engineered precursors for the CVD and ALCVD processes that will be needed at the 100nm node and beyond. The challenges are significant. According to Sullivan, "Conventional CVD requires the simultaneous presence of all reactants in the reaction chamber. ALCVD, on the other hand, introduces the reactants as separate pulses separated by pulses of inert gas. Growth occurs in a monolayer-by-monolayer fashion. For either CVD or ALCVD, suitable precursors are required for the deposition of copper, and for the binary and ternary refractory liners (barrier layers) under consideration such as tantalum and tungsten nitrides and silicides [ITRS, pp. 174-177, Figures 31, 32, and 33]. Many of the precursors being investigated are liquid or solid at room temperature and require novel means of vaporization and delivery into the deposition process chamber." MKS is supporting research on these topics at the Center for Advanced Thin Film Technology at the University at Albany and at the Electronic Materials Program at the Massachusetts Institute of Technology.

One specific requirement called out in the ITRS is already being addressed. The Environment, Safety, & Health section of the ITRS calls for the development of "subatmospheric delivery systems ... for a wider variety of dopant materials." (See ITRS, p. 258.) MKS has developed a pressure-based mass flow controller for this application that is being used with SDS gas delivery systems.

ESD, materials ... no detail too small

The disk drive industry provides a view of the future in one major factory concern—electrostatic discharge (ESD). Arnold Steinman, the chief technology officer of Ion Systems, sees a parallel. "The latest version of the ITRS brings to mind the same type of issues being faced by the disk drive industry, where there was a rapid shift to the use of magneto-resistive (MR) read heads to increase data density. A significant production problem for these devices is their extreme sensitivity to ESD. The current generation of GMR heads is sensitive to ESD events occurring at $\leq 10V$. This means that static control programs often considered optional are now required to achieve acceptable production yields."

Steinman sees comparable concerns in the lithography area. "Unless there is a static control program including ionization in the photolithography area of a wafer fab producing 0.3 μm (or smaller) technology, reticle and product losses will be millions of dollars annually. It is notable that the size of the 5x reticle chrome features at 0.18 μm technology on the wafer is very close to the current feature size of the MR head. These increasingly expensive reticles will become impossible to handle in production without static control." No item in the fab can be ignored in the effort to create an ESD-safe

environment. George Fryburg of Stocker & Yale sees growing demand for lighting products (on microscopes and other equipment) that use ESD-safe materials. A fab manager's job encompasses many such details these days.

There is plenty of research remaining on topics that some in the industry think are "solved." For example, Sunniva Collins, a research metallurgist with Swagelok, has disproved the existence of a significant relationship between manganese and corrosion resistance of standard electropolished tubing materials. ASTM G150, the critical pitting temperature test method, was used in this study, and Collins reports, "Semi's corrosion task force recently voted to adopt ASTM G150 as the basis for functional corrosion testing for this industry."

Entry of 157nm lithography and beyond

From an extensive lithography simulation study to predict the insertion point and extensibility of 157nm optical lithography, IMEC expects that 193nm lithography will be used for the 130nm and 100nm technology nodes and 157nm lithography for 70nm. Electron projection lithography will probably be the technique for 50nm technologies, certainly not before. It is likely, however, that 157nm will be extended to 50nm, assuming a strong industry effort and adequate scaling of k1 process factors, especially for products requiring early market introductions or large-volume applications that need more extensive use of aggressive enhancement techniques. For the 50nm node and beyond, EUV is the most likely candidate, especially for large-volume applications.

Luc Van den hove, VP of silicon process technology, IMEC

Innovations for characterizing phase-shift mask materials

Complete characterization of PSMs requires phase-shift information in addition to thickness, index of refraction (n), and extinction coefficient (k) of the phase-shift materials at the specified wavelength. Transmittance through both the phase-shift material and the substrate must be measured at wavelength. Data must characterize the ideal phase-shift of 180° and 5-10% transmittance.

When the goal is to select an ideal material out of hundreds of possibilities, the time and cost required to perform direct phase-shift measurements are prohibitive. The cost for a dual-beam laser interferometer (the current direct-measurement method) ranges from \$1-2 million depending on the wavelength, taking hours. Even after material selection, and for as long as manufacturing takes place, the fabricator must have access to reliable, fast, and easily implemented testing equipment for process and quality control purposes.



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We have been able to adapt our technology (a method of data collection and analysis that allows the phase-shift, film thickness, and values of n and k to be calculated simultaneously from direct measurements of transmittance and reflectance) to detect nonuniformities in phase shift in both patterned and blanket films with close correlation to directly measured values. This is particularly important because it is crucial for the uniformity of the phase-shift masks to be tightly controlled. Some applications require control of phase shift better than $\pm 1^\circ$ across the entire mask.

The innovation in our technology is the combination of instantaneous collection of highly accurate data points over multiple wavelengths and the simultaneous application of a robust model that allows the phase-shift uniformity of an entire mask to be fully characterized within minutes. Furthermore, this method allows the phase-shift property of any given phase-shift material to be readily determined without the need for creating a step or patterning the mask. This method can be used to perform accurate and precise measurements of thin and ultra-thin films, regardless of whether substrates and interfaces are smooth or rough, or whether there are single or multiple layers, and for a wide range of materials.

Also significant for ITRS requirements, this method has been selected as the technique for characterization of freestanding membranes (typically $\sim 1000\text{\AA}$ SiNx) used for SCALPEL electron beam lithography. Some of the meaningful data we have been able to provide for SCALPEL lithography includes thickness of the SiNx membrane, its values of n and k in the DUV wavelength range (190-300nm), and transmittance through the membrane in the DUV. This information is used to control the process of making the SCALPEL mask and determining its uniformity.

Rahim Foroudhi, CEO, n&k Technology



**The Analyzer 3000
thin-film characterization
system from n&k
Technology.**

*The Analyzer 3000 thin-film
characterization system
from n&k Technology.*

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Revolutionary pattern generation

Some ITRS burdens on maskmaking involve cost and quality. Currently, pattern generators are just barely meeting the 180nm node at the expense of productivity and yield. It is not unusual to hear of 20-30 hr write times and more than \$20,000 for a reticle level. The industry needs a cost-effective, affordable pattern generator that scales its productivity as device complexities and resolution increase; any new pattern generator system must fit the business model of the

photomask industry, which is based on distributed local services.

Our revolutionary approach is based on a massive parallel and wavelength-independent technology, very different from conventional use of one or several beams and wave-dependent refractive optics. We use spatial light modulation technology (SLM) that can image thousands of pixels simultaneously using an array of individually controllable micro-mirrors. This method is fully scalable to device complexity and resolution. The resolution can be increased by increasing the reduction ratio in projection lenses and, when required, can move to a shorter wavelength. The throughput can be maintained by a combination of methods, including an increased number of micro-mirrors in SLM, higher laser flash rates, and an increase of the data-path capacity. The SLM systems can use the same wavelengths and laser sources as steppers, which allows pattern generators to take advantage of the process infrastructure developed for lithography equipment for 248nm, 193nm, and eventually, EUV.



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Bert Jeppsson, president & CEO, Micronic

Dry chemistry alternatives

Most fabs are still using plasma (microwave, ICP, etc.) resist ashing followed by a wet strip-clean using acids or various amine-based commercial solvent formulations. With ITRS environmental and cost issues in mind, however, companies are starting to consider other approaches. For example, for a factory with 10,000 wafer starts using triple metal technology, chemical costs for backend clean only and its disposal can reach more than \$2 million. It is also very difficult to find a wet solvent that can clean post-etch residue effectively without attacking metal or oxide films. The ability to use dry chemistries with at most a subsequent DI water rinse to strip and clean the wafer is very desirable.

Among the many dry-clean technologies (UV, laser, cryogenic, etc.), plasma is the most developed and mature from a basic understanding and manufacturing experience perspective. Unlike simple resist ashing, where a downstream plasma is sufficient, wafer bias is needed to achieve clean wafers for more difficult resist strip and residue clean requirements (e.g., after high-dose implant and plasma etch). As we move along the Roadmap, such requirements will get even more difficult. (With high-density interconnects, for example, there is less tolerance for gate oxide loss during clean and the higher-aspect ratios of vias create challenges for cleaning via bottoms.)

In addition, new chemistry is required for stripping resist from low-k materials. Here, the challenge, especially with organic films, is how to avoid etching low-k materials or changing their properties. Conventional oxygen plasma-based chemistry will not work anymore because oxygen plasma causes a low k film to become more porous, leading to entrapment of subsequently used wet chemicals in the film. We have been working with Sematech and other customers to qualify alternative nonoxidizing and reducing dry chemistries such as NH₃ and H₂ plasmas.

Peter Goebel, COO, Ulvac Technologies

A partnering approach to metrology

As the ITRS notes, in so many areas time-to-market dictates better, faster measurements during development, pilot line, and early production stages to help maturing processes. In addition, new metrology methods must be packaged into cost-effective system designs to help manufacturers achieve a lower cost of ownership and maintain profitability.

For the 100nm-technology node in 2005, barrier layers will be <6nm thick. If a process window of 20% total thickness variation is assumed, then measurement precision must be $\pm 0.012\text{nm}$, beyond current capabilities. Among the many ITRS challenges for metrology, we have made substantial progress in two areas: thickness and density of copper barrier layers and on-product multilayer interconnect stacks composed of a wide range of materials. Using laser-induced sonar, for example, we are already providing repeatability close to 0.012nm and are confident we will be able to meet the precision benchmarks ahead of ITRS dates. Simultaneously but independently produced barrier material density measurement will become increasingly critical because density has been shown to correlate with the barrier's effectiveness in preventing copper diffusion.



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Current film thickness methods, such as x-ray fluorescence, optical reflectivity, ellipsometry, profilometry, and microbalance do not meet the ITRS challenge to provide rapid, spatially resolved multilayer thickness measurements of product wafers. New methods using laser stimulation of acoustic and thermal waves, at this time, require test structures in chip scribe lines. We have demonstrated, however, that our acoustic technology provides the required accurate and repeatable thickness measurements of multilayer interconnect structures, which include a wide variety of materials.

When we introduced picosecond ultrasonics, we knew it was a revolutionary technology that would help enable the development and implementation of copper interconnects. But we also knew we were taking the risk that this technology might not be rapidly assimilated into production. We addressed this by attaching it to a proven production-worthy measurement platform and giving new users an "expert in residence," another kind of partnership that is key to solving ITRS challenges. This approach has had two advantages: it provided rapid applications development on the most important metrology challenges, whose success virtually assured rapid assimilation of the new technology from development straight into production. And our "experts" enabled us to partner with users by sharing nonproprietary knowledge about how tough problems were solved in other fabs, thus eliminating the need to "re-invent." In this sense, we have served as a process control knowledge hub and as a consolidation point for market-relevant guidance for our engineers, allowing them to develop next-generation capabilities faster.

Paul F. McLaughlin, Chairman and CEO, Rudolph Technologies

Critical cleaning with ozonated water

Ozonated water chemistry for critical wafer cleaning is an important part of ITRS demands, both environmental and productive, to reduce chemicals and water consumption. In addition, its use for removal of organic and metal contaminants and the controlled growth of thin oxide layers often results in fewer processing steps, room temperature processing, and smaller-footprint cleaning systems. Recent studies have demonstrated the efficacy of ozone in pre-diffusion and pre-gate critical clean processes.

Conventional methods of introducing ozone into water involve the direct mixing of the gas into water by means of spargers or static mixers. This can result in the formation of bubbles that adhere to hydrophobic wafer surfaces, decreasing cleaning efficiency (e.g., the bubbles block chemical cleaning). Bubbles also tend to attract particles. Bubbles can increase surface roughness in etch processes by altering etch rate where they adhere to the surface.

Such problems can be overcome with a membrane contactor that permits mass transfer of gas into liquids through diffusion, without the dispersion of free gas into the liquid phase; the gas is dissolved into the fluid at the point of contact without the formation of bubbles and at 100% efficiency under appropriate conditions. The important point is that the ozone is dissolved rather than remaining in the gas phase as bubbles.

Our approach uses a compact, modular membrane contactor made of only fully fluorinated materials—a microporous PTFE membrane modified to form a thin, nonporous layer on one side that is gas but not water permeable. This material is inert, non-leaching, and only gas permeable, eliminating wetting problems that can occur with open-pore, hydrophobic membranes. Because the membrane does not wet out over time, ozone transfer rates are maintained at high, consistent levels.



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Steve Chisolm, senior VP, Pall Corp./Microelectronics

Integration is helping to make the road a safer place

To meet the rigors of the accelerating Roadmap, the equipment industry has had to take on more responsibility in the final chipmaking process. Since the semiconductor industry has been bombarded with new technologies, materials, and processes, companies have begun to provide process integration support. This constitutes a guarantee that the complete tool set will work together and help keep chip yield high, thereby allowing companies to control costs and remain competitive. This way of doing business is in contrast to the late '80s and early '90s, an era when the equipment industry would provide chipmakers with individual tools and later a guaranteed process performance, but would leave customers to integrate these processes into the desired process flow.



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Novellus' Damascus Alliance (including Lam Research, Cabot, GaSonics, Novellus, and Speedfam) has been structured to help chipmakers integrate copper material into their manufacturing process. The Alliance members work closely with semiconductor manufacturers to leverage their in-house knowledge of the process to ensure optimal tool performance across the fab. The success is apparent: 10 major chipmakers have already established pilot or production lines for copper interconnect processing.

Novellus' open alliance of equipment makers allows users to select which process works best for their individual manufacturing facilities. The concept of choice is a key value delivered by the Alliance, and it offers multiple choices for each unit process. Overall, IC companies have expressed a preference to using a mix of tools from different vendors to assemble their production lines and therefore, minimize their risk.

The ability to deliver unique products is key to each chipmakers' success. Each requires slightly different technical materials and processes. The job of equipment vendors is to provide them with the tools that enable them to do this with minimal risk, while helping to exercise their own innovation and creativity.

Wilbert van den Hoek, executive VP for integration and advanced development, Novellus Systems Inc.

Atomic layer CVD for thinner films

ALCVD technology has far-reaching potential as an enabling technology for deep-submicron structures. This is a method of depositing a broad spectrum of materials one atomic layer at a time. ALCVD is a catalytic, self-terminating surface reaction. After all reactive bonds have been occupied by the desired material, the material will "grow" no further. This means that the process has a wide tolerance to large variations of process length and temperature in relation to layer thickness. The film's thickness is controlled by the number of ALD cycles made. Since it is a surface reaction, material will "bond" everywhere the precursor and the reactive sites are present, therefore providing exceptional step coverage or

conformality.

Due to its physical attributes, ALCVD provides critical features required by deep-submicron structures—very thin, uniform, and highly conformal layers. In ALCVD processes, the various species react only where they should—on the wafer's surface. This could solve some of the tricky problems presented by new materials, such as barium strontium titanate (BST), and offer new avenues for the use of complex materials. In the ITRS (p. 134, Table 35), BST is listed as the dielectric material for the 100nm and 70nm node for DRAM stack capacitors.



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ALCVD has potential for many types of thin-film applications, including high-k films for gate dielectrics and capacitors (DRAM and decoupling) with Ta₂O₅, Al₂O₃ and ZrO₂; and barrier metal and metal nitrides—TiN, WN, tungsten, TaN, and copper. These applications will be critical for barrier metal and seed layers for copper metallization. Most of those materials are listed as possible barriers for Cu in the ITRS (p. 174, Fig. 31). ALCVD, by depositing very dense film, will allow the use of a larger range of materials and will produce thinner layers compared to conventional CVD. It will also offer a possible solution to the replacement of silicon gates by metal gates for transistors. (We then will be back to the early days of CMOS when metal gates were the technology of choice.) To date, an equivalent oxide thickness (EOT) of 14Å, with leakage currents of $5 \times 10^{-8} \text{ A/cm}^2$, has been demonstrated.

Ernst Granneman, business unit manager, ASM Microchemistry, ASM International

The challenges when etching new materials

In the ITRS, new materials for gate conductors, gate dielectrics, interconnect, decoupling capacitors, and DRAM capacitors and dielectrics are labeled keys to advancing beyond the 180nm process node. The Roadmap states that etching these materials requires entirely new technologies and approaches, better control of deposition in the etch chamber, and optimum chamber-cleaning procedures. (See ITRS '99, pp. 132, 180.)

The high-k materials set, for example, uses constituent elements like platinum, iridium, zirconium, strontium, and lead that have not been seen much before in semiconductor processing. The chemically assisted physical etch, which works best for these new films, simply cannot be optimized in plasma etch systems using a single RF frequency. Increasing RF power to increase ion bombardment makes for too much chemical etch component, chewing up the mask. Decreasing RF power to reduce chemical etching keeps the ion strength too low for effective physical etching.



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We've worked at patenting dual RF frequency plasmas where low-frequency RF power controls ion energy (physical etch) and high-frequency RF power controls ion density (chemical etch), all capacitively coupled to the wafer. This improves process stability (through impedance matching) compared to inductively coupled plasmas. For films like the high-k materials that are difficult to etch, a dual frequency reactor configuration ensures that successful etch processes can be developed for any single film or film stack over a broad range of etch temperatures.

Mike Parodi, president and CEO, Tegal Corp.

Getting fabs under control

No major mature industry, like petrochemicals, pharmaceuticals, or automobiles, relies on final inspection (i.e., ex situ metrology) to control quality and yield as much as the semiconductor industry has traditionally done. Many sensors already exist to help move toward an eventual goal of fab-wide control of processes.

In situ sensor data includes process state information, such as pressure (vacuum gauges), gas analysis (RGAs), and endpoint detection (optical emission spectrometry), as well as new-generation wafer-state information (LES wafer imaging). The accuracy, sensitivity, reliability, and speed of these in situ sensors are all being improved, not just to get better measurements but to help enhance productivity.

The tool itself is another source of data that is often overlooked. Built-in sensors provide data for proper tool operation, and this can be used along with in situ process sensors to supply key information. Fabs also collect masses of data about processes and wafers. These three sources of data need to be combined and analyzed with sophisticated statistical techniques. By looking for correlations across multiple parameters, an analysis engine can detect otherwise unseen relationships.

While the methods of statistical analysis are well known, it takes considerable skill to choose and apply them efficiently to get useful results. If successful, these methods can be equivalent to having a process engineer at each tool. Even better, as engineers are freed up from extensive data analysis, they can focus more on improving processes.

The next step will be to integrate all the data with intelligent software that will provide fab-wide monitoring and eventually, control. At its simplest, this could mean a single screen that, at a glance, would show the status of every tool. More sophisticated applications would compare tools to assist in tool matching and to promote consistent processing while tracking process performance across multiple tools.

We are helping to develop new and better ways to acquire and analyze semiconductor production data as the industry

moves toward reaching the Roadmap's vision of pushing metrology from after-the-fact wafer inspection to true in-process monitoring and control.

James L. Brissenden, president, Leybold Inficon

The future of packaging technology

It is easy to review what has been achieved in the semiconductor industry—more difficult to predict the future. For example, in the early 1980s, AT&T asked McKinsey management consultants to estimate how many cellular phones there would be at the end of the century. The answer came back—about 900,000; this persuaded AT&T to pull out of the market. These days, 900,000 new subscribers join the world's mobile-phone services every three days (The Economist, Sept. 1999)! In AT&T's defense, it was not obvious at that time that dramatic reductions in size and weight could be achieved, changes by and large due to advances in packaging technology. Packaging technologists are about to embark on an even more dizzying ride that will change how we live and work. The rate of change is accelerating, thanks in part, to that unrelenting driver called consumer electronics.

An excellent example of the macro-economic effects of packaging technology comes from the early 1970s when the Swiss mechanical watch industry was a dominant force. The Swiss lost their market to the Japanese digital watch, then regained market share in the 1980s with the Swatch watch, a marketing turnaround of no small measure. Competence in high-volume, tape-automated, bonding-and-display-assembly technology underwrote these market changes.

Packaging technology will play an even more critical role in the next three to five years as technical issues continue to be driven by the commercial market for portable products. Drivers include miniaturization, performance, and producibility. To address these issues, flip chip challenges like underfill and rework will have to be tackled, as will high-density substrate development, wafer-level test and burn-in, and cycle-time/cost reductions. Problems with high-heat flux cooling, especially for high-performance applications, will have to be addressed to meet chip-scale packaging cost, proliferation, and reliability objectives.



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The automotive industry will provide a major push in microelectromechanical systems for sensor applications. Stacked chips and wafer thinning will come to the fore, and copper will predominate for high-performance applications. As wafer-scale packaging gains acceptance, the use of integrated passive devices will be even more critical, as will the movement to integration with front-end processing. These trends will increase the need to coordinate development work with front-end technologists.

As we approach 2015, it is expected there will be broad use of databases for materials and benchmarking. Software enabling the lights-out factory will be a reality and computer-aided design will be most likely done on the Internet with integrated electrical, mechanical, and thermal design tools. Given this, system simulation will be much easier and commonplace. Thanks to powerful desktop PCs and workstations, packaging simulation, as well as electrical, thermal, and mechanical simulations, will be commonplace, and the result will be a significant reduction in package design turnaround time.

Consider this glimpse into the future, made possible by advanced packaging technology. A typical professional will be a walking, wearable terminal with glasses, a briefcase, watch, card, and even shoes that make her smart. From the comfort of her living room, our smart subject will check the process controls and work in process (WIP) in the factory. Between sips of coffee, she will review a customer request and enter some data into an appropriate integrated simulation program off the web. She'll retrieve the design and check that the calculated reliability meets the customer's application. If okay, the design will be sent to the factory where a 50,000-unit run will be completed during the afternoon and shipped that night. Whether we believe these prognostications or not, they are most likely to be the applications that drive us in the next 25 years.

John Jackson, technical director, new business, Semi

Defects, yield, and cost of ownership: The slippery slope of Moore's Law

One of the roles of the 1999 ITRS has been to quantify many of the requirements for keeping the semiconductor industry following Moore's Law of productivity. The random defect targets recently released in the ITRS are based on pre-defined technology nodes using data collected by Sematech member companies on 164 tools, which are divided into 30 generic categories. The ITRS identifies a consensus of conditions for the semiconductor industry to maintain its historical 25-30% increase in productivity/year. One key to maintaining this productivity is not losing ground in areas of historical accomplishment, such as yield improvement.

There is a strong relationship between integrated circuit yield and cost. This is illustrated in Fig. 1, which shows both yield and COO as a function of defect target for a 180nm (linewidth) lithography cell. The 1999 ITRS defect target for this tool is 112 defects/m². This results in a yield of almost 94% and a COO of about \$13.50.

The 1999 ITRS defect target for the lithography cell at 210nm linewidth is 152 defects/m², which also would result in a 94% yield for the wider linewidth. Attempting to manufacture the 180nm linewidth at 152 defects/m², however, lowers the expected yield to 92% and increases the COO to \$14.50. In a 24-mask-level process, this would raise the cost of a completed wafer by at least \$24.00.

Thus, to maintain the same economic productivity requires reducing the defect target from 152 at 210nm to 112 at 180nm. The ITRS Roadmap defect target progression for the lithography cell is shown in Fig. 2. Just maintaining the current tool defect reduction pace to meet the requirements of Moore's Law is a very difficult challenge.

Maintaining equipment yield in wafer fabrication is also a challenge. As shown in Fig. 3, the number of process steps in the Roadmap is expected to increase from 380 in 1999 (180nm) to at least 630 in 2014 (35nm). At this rate, per step equipment yield loss must be cut almost in half, from 28 wafers/100,000 moves to 17 wafers/100,000 moves, just to maintain 90% production yield.

The ITRS Roadmap has grown in complexity. But even with the additional targets for memory and logic circuits, rarely do actual circuit linewidths and areas match the ITRS technology node assumptions. Our company has developed a defect target calculator to help semiconductor suppliers and manufacturers compare the Roadmap targets to their current or planned needs.

The defect target calculator allows users to confidentially enter key parameters for a selected tool and estimate a defect target for a specific chip. The only parameters required are the chip area, minimum linewidth, number of mask levels, and random defect-limited yield requirement. The calculator uses the same scaling method and generic tool categories as the Roadmap to provide specific target estimates. Posting this calculator on the Internet (<http://www.wwk.com>) makes the Roadmap more useful.

Moore's Law provides many challenges to the semiconductor industry. Not the least of these challenges is maintaining the industry's historically significant yield accomplishments.

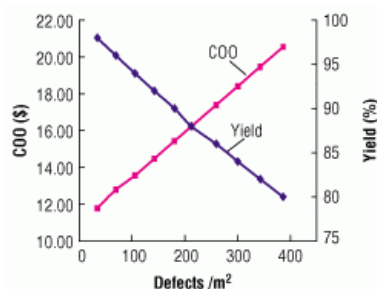


Figure 1. Cost of ownership (COO) and yield vs. lithography defect density.

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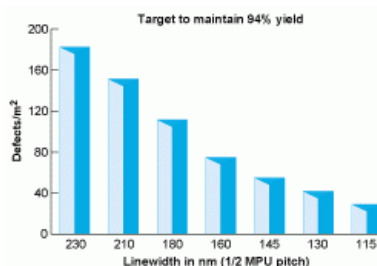


Figure 2. ITRS defect targets.

Figure 2. ITRS defect targets.

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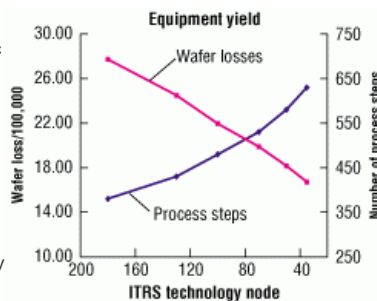


Figure 3. Per step equipment yield required for 90% production yield.

Figure 3. Per step equipment yield required for 90% production yield.

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An evolving view of capital equipment

The role of factory automation and the management of production equipment represent some of the greatest opportunities, as well as challenges, for the semiconductor industry. The 1999 ITRS points us toward many of these opportunities.

Demands for improved cycle time, higher quality within ever-more-demanding wafer processing, and greater equipment flexibility are all factors driving equipment manufacturers and their customers to reevaluate conventional approaches. Here are examples.

Capital costs. Our industry is moving away from outdated cost-of-acquisition models of capital equipment into more useful and insightful ways of evaluating total cost of ownership. In these new models, the impact of equipment costs, as measured in productivity, yield, material costs, and even floor space, are emerging as the true evaluation measures by which to assess capital equipment.



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Equipment footprint. Manufacturing space has always been a premium, but finding new and innovative solutions to maximize production facilities is even more critical when trying to achieve new levels of productivity. Production equipment companies are responding by re-engineering entire equipment platforms to find new ways to improve both space and speed. New innovations in multiprocessing equipment, like combined reflow and cleaning for micro-BGAs, further maximize space usage and set a new standard for the industry.

Consumables. At one time considered a secondary issue, the management and recycling of materials and consumables is now a priority for the semiconductor industry. From ensuring material quality and yield, to using materials like encapsulants more efficiently, to responding to environmental and recycling issues, equipment manufacturers are re-engineering their technologies to maximize the use of consumables.

Maintenance and cost of spares. The ITRS report highlights an area of production efficiency often overlooked—the impact of maintenance costs and manufacturing downtime on per-wafer profitability. Semiconductor companies are seeking equipment partners that can provide global support from advance training and maintenance to 24/7 spare parts programs.

The demand for smaller, faster, and more powerful technologies is challenging all of us to rethink traditional models of equipment acquisition and process management. The innovative solutions we are developing together represent the answer to that challenge.

Rick Berger, president, Speedline Technologies

The view down the Roadmap

The 1999 ITRS cites integration as one of the five difficult challenges for both interconnect and metrology, and we are seeing an analogous change in equipment integration. Individual equipment components, such as pressure sensors, valves, and traps, are merging into subsystems. Component suppliers are transforming into subsystem manufacturers.

By working with equipment manufacturers and fab engineers, for example, MKS has developed subsystems to manage effluent from CVD reactors. These subsystems integrate pressure sensors, valves, heaters, traps, and other specialized components. On the upstream side of the process chamber, many new precursors are being evaluated for use in the CVD of novel materials such as high- and low-k dielectrics, barrier materials, and copper layers. These precursors are increasingly liquids or solids with low vapor pressures, so they pose significant challenges in obtaining consistent and precise delivery to the chamber. Here again we see the instrument and component suppliers building integrated materials delivery subsystems for the tool OEMs that are optimized for the particular precursor and CVD system.



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Another trend is the migration of responsibility for process control from the device manufacturer to the equipment manufacturer — and increasingly to the component and subsystems manufacturer. Component and subsystem manufacturers will play a key role in driving the implementation of new processes and improving current ones.

Some of the continuing challenges include the integration of multiple instruments and sensors with complex process systems. Again, instrument and component companies with broad arrays of process knowledge will be able to provide a variety of integrated technologies. We will see more of these companies' process control "solutions," which will increasingly use digital devices instead of analog instrumentation to better communicate with process tool controllers.

As we travel the Roadmap, we will see more of the gas and vacuum component manufacturers working closely with both the end user and the tool vendor on a global basis to satisfy customer process requirements. These requirements are not just about hardware. They include installation, maintenance, and technical support. The continuing globalization of these services is driving the need for truly global vacuum product suppliers. Those companies that can provide worldwide service capabilities will be preferred.

Peter Younger, president and COO, MKS Instruments Inc.



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