

Welcome !

Thank you for your interest in *the International Technology Roadmap for Semiconductors: 1999 edition*.

We have worked diligently as teams of Technology Working Groups from around the world to assess technology requirements for the semiconductor industry over the next 15 years. The working groups include the technologies of Design; Test and Test Equipment; Process Integration, Devices, and Structures; Front-end Processes; Lithography; Interconnect; Factory Integration; Assembly and Packaging; Environment, Safety, and Health; Defect Reduction; Metrology; and Modeling and Simulation.

For this edition, our focus has been on near term needs for the next six years, and then assessing the longer term issues in the years beyond 2005. We see technical opportunities as well as challenges for all areas as the industry approaches the 100 nm feature size realm and beyond.

As we continue to assess where we are and where we are going, we are once again humbled at the scope of this exercise of "roadmapping" our industry's needs in the areas of research and development. This is an ongoing process as new innovations surface throughout the world, requiring constant review and routine revisions of this information.

This effort is sponsored by the Semiconductor Industry Association (SIA), and with participation from members of the European Electronic Component Association (EECA), the Electronic Industries Association of Japan (EIAJ), the Korea Semiconductor Industry Association (KSIA), and the Taiwan Semiconductor Industry Association (TSIA).

About the *International Technology Roadmap for Semiconductors*

The semiconductor industry consists of a global community of suppliers, researchers, and chip manufacturers. The Semiconductor Industry Association's (SIA) 1994 and 1997 editions of the *National Technology Roadmap for Semiconductors* were very valuable to this world wide industry. The community has responded to the recommendations of the Roadmap for continuing success. It is understood, however, the industry needs for research and development are constantly changing, requiring frequent reviews and new assessments. It is recognized that these assessments that include the entire community leverages our understanding of key challenges we all face as an industry.

As such, the Technology Roadmap for Semiconductors is always in active review. The year 1999 is a formal revision year for the Roadmap. The Technology Working Groups (TWGs) assess the data for technology needs and areas where innovation is encouraged. By consensus these teams update the information. ITRS conferences provide a forum for review by the entire semiconductor community for feedback and input.

Once this feedback is gathered, each TWG issues a formal report. These reports make up the Roadmap. The Roadmap is then reviewed and approved by technical advisory boards from all over the world, prepared for distribution, and made available to the public.

We invite you to participate in this dynamic process by coming to the ITRS Conferences to promote continued success of the industry!

Special thanks to members of the European Electronic Component Association (EECA), the Electronic Industries Association of Japan (EIAJ), the Korea Semiconductor Industry Association (KSIA), and the Taiwan Semiconductor Industry Association (TSIA) for their valued input.

GLOSSARY

KEY OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS (ORTC) TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

TECHNOLOGY NODE (nm)—The ground rules of process governed by the smallest feature printed. The half-pitch of first-level interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. For logic, such as microprocessors (MPUs), gate length is most representative of the leading-edge technology level required for maximum performance. MPU and ASIC logic interconnect half-pitch processing requirements typically lag behind DRAM half-pitch. For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

“MOORE’S LAW”—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a “self-fulfilling” prophecy, “Moore’s Law” has been a consistent macro trend, and key indicator of successful leading-edge semiconductor products and companies, for the past 30 years.

“COST-PER-FUNCTION” MANUFACTURING PRODUCTIVITY IMPROVEMENT DRIVER—In addition to “Moore’s Law”, there is a historically-based “corollary” to the “law,” which suggests that, to be competitive, manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every two years, as suggested by consensus DRAM and MPU models of the 1999 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

“Affordable” Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by **Functions/Chip**. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market “tops-down” needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership (CoO); 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration, Introduction, Sample, Production, Ramp, Peak).

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction, Ramp, Peak, Embedded).

There will be a number of problems in scaling the basic MOSFET structures, particularly for the 100 nm technology node and beyond. The most pressing of these is with the gate stack, the combination of gate dielectric and electrode. The reason for this problem is the thin oxide thickness required for 110 nm and beyond technology generations. For such thin oxides, the gate leakage current due to direct tunneling would become unacceptably large. Use of alternate gate dielectrics with higher relative dielectric constant (κ) than silicon dioxide is the leading projected solution to reduce the gate leakage current to more tolerable levels. However, the time to develop and implement such dielectrics in production is exceedingly short, since the 110 nm node is scheduled for first production by 2004. This is the highest risk problem in the front end. Along with high κ gate dielectrics, dual metal for the gate electrodes is a potential solution to eliminate depletion effects in polysilicon gates and the problem of boron penetration from P^+ polysilicon. Also, metal electrodes sharply reduce the gate resistance and avoid the problem that occurs with silicided polysilicon of increasing sheet resistance for very narrow gates. Ultra-shallow source/drain (S/D) extension junctions will be required, and techniques such as plasma assisted implantation, projection gas immersion laser doping, and ultra-low energy ($< 0.5\text{keV}$) implants are projected solutions for fabricating these junctions. In the deep S/D contact, the requirement of low sheet resistance and contact resistance and shallow junction depth will become increasingly difficult to meet without such innovations as raised S/D or epitaxial Si/Ge. Finally, to maintain the on current and deal with short-channel effects, advanced channel engineering techniques such as highly optimized halo implants and the use of high mobility silicon/germanium epitaxial layers are envisioned. Refer to Figure 13 for the Memory and Logic potential solutions.

Even with innovative scaling solutions as discussed above, it will be quite difficult with technologies at the 100 nm node and beyond to simultaneously meet the requirements for I_{on} , I_{off} , and limited overall chip power dissipation. This is due to the sharp scaling of V_{dd} , while the threshold voltage, V_t , must remain relatively constant to keep I_{off} within tolerable limits. Using multiple V_t s on the chip, or switched V_t through well bias (which requires triple well for bulk CMOS), or dynamic V_t , where the V_t is changed by the gate bias, could alleviate these problems. (Dynamic V_t requires that $V_{dd} \leq 0.6\text{ V}$ to avoid excessive junction leakage due to forward biasing of the source/substrate junction.) Also, SOI technology, with its high-performance at low V_{dd} and its low parasitic capacitance, could be an important solution. Eventually, for the 50 nm node or beyond, such novel structures as dual gate SOI or vertical MOSFETs may be needed. Even further out, novel switching devices such as quantum dot or single electron transistors, are possible solutions. More accurate, comprehensive, and easy to use TCAD and modeling tools are needed to develop and implement the above-mentioned solutions in a cost-effective, timely manner.

For interconnect, as the technology is scaled and the speed increases, the number of metal levels and the density of the wiring increases and reduction of the parasitic resistance and capacitance becomes critical. Copper is being implemented in current technology by some companies because of its relatively low resistivity and its high lifetime against electromigration. Eventually, copper is expected to replace aluminum as the mainstream metallization for ICs. Low dielectric constant (κ) materials are also being implemented for the interlevel and intralevel dielectric to reduce the capacitance, and it is expected that newer materials with lower κ will be utilized for later technology generations. Eventually, “void” structures such as air gap, void-based materials, etc., may be implemented. It is expected that the combination of copper and low κ dielectrics will suffice for many technology generations. In the long run, however, beyond the 50 nm technology node, highly innovative solutions such as optical interconnect, liquid nitrogen cooled conductors, may be utilized to overcome the inherent speed and power limitations of copper and low κ dielectrics.

For DRAMs, improvements in density, cost, speed, and noise immunity with scaling are critical. As with the gate dielectric, high κ dielectrics are expected to be implemented to increase the capacitance of the storage nodes. Also, similar low κ dielectrics to those in logic IC interconnects will be implemented to lower the