



ISSUE

IEDM 1999 focused on CMOS solutions

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It was hard to miss the concentration on CMOS gate oxide technology and system-on-a-chip ICs at this year's IEEE International Electron Devices Meeting (IEDM) in Washington, DC.

The gate oxide emphasis was particularly significant just two weeks after the official release of the 1999 International Technology Roadmap for Semiconductors (ITRS) with its message about the "formidable obstacles to the industry's classical silicon, silicon dioxide, polysilicon scaling approach to continuously improve performance." The 1999 ITRS sees 1.0-1.5nm gate oxides as problematic, possibly beginning with the 100nm technology node in 2005.

Yearly, IEDM reflects the world's best applied research behind microelectronics and gives important clues about where semiconductor manufacturing technology will be three to five years in the future. For IEDM 1999 — the 45th annual event — attendees sat in on 220 invited and contributed technical presentations selected from ~600 abstracts.

Researchers from Lucent Technologies Bell Labs discussed work showing that the reliability of a gate oxide layer is higher when its thickness is more uniform. They determined that 1.6 ± 0.2 nm SiO_2 layers could be used in 50nm transistors operating at 1.2V and 65°C.

In related work, a research team from IBM reported on new data looking at oxide reliability estimates reported at last year's IEDM. With 2.5 ± 0.7 nm-thick oxides, if thickness variations of 0.1nm are not taken into account, projections of oxide failure rates might be off by two orders of magnitude.

The session on high-k gate dielectric process technology — materials with the potential to overcome ITRS limits of scalability related to gate oxides—drew standing-room crowds. Here, significant progress with hafnium oxide (HfO_2), tantalum oxide (Ta_2O_5), and zirconium oxide (ZrO_2) was reported in what seems to be a competitive race among researchers at the University of Texas (UT) in Austin. Morgan Thoma, IEDM publicity chair, noted, " SiO_2 has been the magic material. Now, it's clear that researchers are working their way through the periodic table for a replacement, but there is no known solution yet."

One UT group has used oxygen-modulated dc magnetron sputtering — a process that controls pressure, deposition temperature, and particularly oxygen flow rate — to control HfO_2 interface quality and growth and achieve a physical thickness of ~40-50Å with a gate equivalent oxide thickness (EOT) <13.5Å. This gate, with a dielectric constant of 6-16, was able to maintain a low 4×10^{-4} A/cm² leakage current at +1V. In addition, these researchers reported good thermal stability for HfO_2 , negligible dispersion, and excellent reliability.

Another UT group reported on development work with in-situ rapid thermal processing for CVD Ta₂O₅ with an EOT <15Å. This gate material also exhibited 10⁻⁴ A/cm² leakage current at -1V. The process uses an NH₃-based interface layer that gives a strong resistance to oxygen diffusion during Ta₂O₅ deposition and post-deposition anneal, compared to previously used oxynitride interface layers. In addition, they claim that a novel H₂-O₂ pyrogenic post anneal of the Ta₂O₅ film improves film quality.

A third UT group presented research results with ZrO₃ deposited directly on silicon without an interface layer with DC magnetron-reactive sputtering from a Zr target in an Ar-O₂ ambient, to achieve EOT <13Å and leakage <10⁻² A/cm², with "well-behaved" MOS transistor characteristics.

Yale University researchers reported on their work with titanium oxide (TiO₂) for high-k dielectric applications. They used so-called jet-vapor deposition (JVD), which combines titanium vapor generated by 1 torr DC sputtering in argon and atomic oxygen generated from a microwave discharge sustained by a fast flow of oxygen through a quartz nozzle. At Yale, JVD has been used for TiO₂-Si₃N₄ gate dielectrics with ~1.5nm EOT and leakage current ~100x lower than thermal oxide.

IEDM's high-*k* gate dielectric session ended with a report from Sharp Laboratories of America showing preliminary results using ZrO₃ doped with ~10% aluminum (Al), prepared by co-sputtering Al and Zr targets with a 1:5 power ratio in oxygen and argon at room temperature. Al doping reduces leakage current and increases crystallization temperature of the gate dielectrics. Sharp's team has achieved leakage currents <0.1 A/cm² for a 3nm Zr-Al-O film with effective dielectric constant of 12-18, and has fabricated submicron devices with excellent characteristics.

IEDM 1999 plenary speaker Roel Kramer, chief technology officer at Philips Consumer Electronics, built a strong case that consumer electronics (which includes annual sales of 100 million TV sets) is being led by digital TV and video technologies and is rapidly becoming the major driver for silicon technology. "Here, the solutions will be found in SoCs and silicon will be able to handle the task," said Kramer. Because of this, Kramer sees IC evolution different than that to support PCs, where performance is maximized and additional performance represents significant value for the IC. "In consumer electronics, a specific application is realized so certain functions are mapped onto silicon and additional performance is not useful. The competitiveness of consumer markets also requires more emphasis on cost-effectiveness. We are going to see SoC architectures matched to applications using dedicated cores for a particular task next to DSP and microprocessor cores to achieve higher computational efficiency, compared to general purpose architectures."

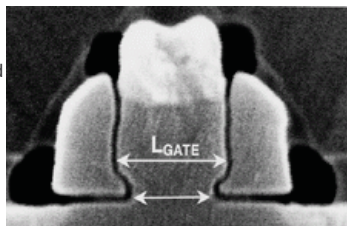
Extending the future of TV to "hypermedia platforms" and consumer decisions being made by "prosumers" (consumers making more knowledgeable decisions), plenary speaker Susumu Kohyama of Toshiba Corp. sees SoC solutions leading to an "approaching big bang in the semiconductor industry. The classic broad range model is no longer valid. Semiconductor manufacturers are going to select from different schemes for vertical and horizontal business integration and perhaps even adopt some unique standalone models," he said.

Looking at the road ahead for microelectronics, Robert H. Dennard confirmed that in line with many of the technology challenges being addressed today, "It seems likely that progress in scaling silicon device technology will slow or even end in the next decade." Dennard is recognized as the inventor of today's one-transistor DRAM memory and with colleagues at IBM developed and defined the concept of silicon scaling in the early 1970s. He was also the recipient of the National Medal of Technology in 1988. "Semiconductor technology will continue to evolve and there is certainly room for unexpected breakthroughs, yet we have to wonder how much there is left to discover," he said. Dennard does not rule out a role for yet unknown contributions from cross-discipline fields, for example magnetics or organics. Also, he does not see silicon-based technology being replaced. Rather, "it will level off at a very high plateau of cost-effectiveness and performance; it won't be easy for any new technology to challenge or replace it and it will continue to provide an excellent base for many new and exciting applications." At the limits of silicon scaling, Dennard foresees a new phase in microelectronics where the emphasis will be on system-level performance using massively parallel technology where, in particular, processor-based technology with memory added will play a major role. "No matter what comes in the future, I believe it will be a very smooth transition. We have to remember that as we evolved over the past 30 years, the path ahead was never very clear," said Dennard.

At one of IEDM's classic "off the record" evening panel discussions, noteworthy experts and clearly more than half of IEDM's attendees bantered with questions about the future of CMOS technology evolution. Asked what will be the smallest dimension gate in mass production, attendees sided with <30nm while the panel consensus was 30nm. Both groups agreed overwhelmingly that cost of manufacturing would be the eventual limiting factor. "While there are tremendous materials issues, application will be achieved as long as there is an economic incentive," said one panel member. What will be the last CMOS substrate? Here, bulk silicon and SOI seemed to be in a toss-up, perhaps both on the same substrate. When queried about alternate device structures, vertical structures (planar CMOS redesigned on its side) ranked high in extending CMOS, followed by eventual use of nano devices.

CMOS transistor may enable 1GHz MPUs

In one of the highlighted papers presented at IEDM 1999, researchers from Intel showed a 100nm gate-length CMOS transistor structure that preformed with an inverter delay of <10psec in a benchmarking oscillator. This enabled 1.06GHz performance in a 16Mb SRAM "learning vehicle" specifically developed for this technology. The significance is that these devices may allow clock frequencies on microprocessors beyond 1GHz. So far, device work with this structure has been achieved with low power consumption, with 1.2-1.5V supply. From a design and process view, Intel's new technology incorporates advanced concepts such as halo implants, steep retrograde wells, ultrathin 2nm gate oxides, cobalt-silicide-clad gates, and a novel notched gate profile that reduces unwanted capacitance. (The SEM image shows the notched polysilicon profile of a fully processed device; Lgate is larger than the polysilicon dimension at the polysilicon-gate oxide interface.)



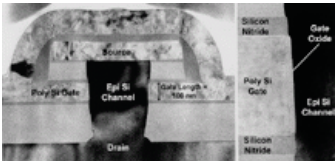
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Ultrasmall gates sans lithography

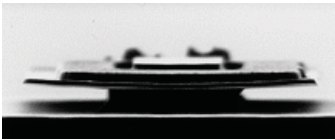
Reporting at IEDM 1999, Bell Lab researchers revealed 200 to 50nm devices fabricated vertically without relying on lithography and etching to define gate sizes. Instead, they used a novel polysilicon deposition technique where the gate length and its variability are controlled simply by controlling the thickness of the deposited film. Shown is (left) a TEM image of a 100nm vertical replacement-gate MOSFET and (right) the channel region revealing the polysilicon gate, two nitride etch stops and offset spacers, and the 60Å gate oxide. The Bell Lab engineers behind this work believe it can be scaled down to sub-30nm lengths.

1999 IEDM speed record

At IEDM 1999, TRW researchers described how they used indium phosphide (InP) to build an HBT transistor, with a novel cantilevered base and undercut collector (see SEM of transistor cross-section) that reduced base-collector capacitance. Operating at 69 GHz, this technology — they claim — was the basis of the fastest static frequency divider ever built in any semiconductor technology.



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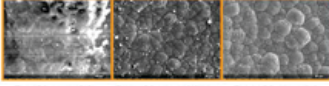
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