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Charge trapping in very thin high-permittivity gate dielectric layers

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The trapping of charge carriers in very thin $\text{SiO}_x/\text{ZrO}_2$ and $\text{SiO}_x/\text{TiO}_2$ gate dielectric stacks during constant gate voltage stress of metal-oxide-semiconductor capacitors has been investigated. The increase of the gate current density observed during the gate voltage stress has been analyzed, taking into account both the buildup of charges in the layer as well as the stress-induced leakage current contribution. From data analysis, the cross section of traps generated during the electrical stress is estimated. It is suggested that these traps are probably ZrOH and TiOH neutral centers that are related to the breaking of bridging O bonds by mobile H^+ protons followed by the trapping of these protons at ZrO or TiO sites. © 2000 American Institute of Physics. [S0003-6951(00)03235-6]

The trapping of charge carriers and the subsequent dielectric breakdown of ultrathin gate dielectric layers is considered as a major reliability issue in very large scale integrated circuits. With respect to this issue, high permittivity dielectrics are currently widely investigated as alternative gate insulating layers in advanced metal-oxide-semiconductor (MOS) devices. As a matter of fact, the scaling down of the SiO_2 layer thickness in such devices is reaching its limit, both from the point of view of gate leakage current limitation¹ as well as intrinsic reliability concerns.^{2,3}

While the wearout and dielectric breakdown of thin SiO_2 layers have been studied for quite a long time,⁴⁻⁸ not much work has been devoted to the charge trapping in high permittivity gate dielectric layers. In this letter, we have investigated the trapping of charge carriers in very thin $\text{SiO}_x/\text{ZrO}_2$ and $\text{SiO}_x/\text{TiO}_2$ gate dielectric stacks deposited by atomic layer chemical vapor deposition during constant gate voltage stress of MOS capacitors. From the analysis of the increased gate current density observed during the electrical stress, the cross sections of electron traps generated in these gate stacks are found to be on the order of 10^{-18} – 10^{-19} cm^2 , suggesting that these traps are neutral centers. We propose that these traps are probably ZrOH and TiOH centers, which could be generated during the breaking of bridging oxygen bonds by mobile H^+ protons and the subsequent trapping of these protons at ZrO and TiO sites.

Zirconium oxide and titanium oxide layers were deposited by atomic layer chemical vapor deposition (ALCVD)^{9,10} on *n*-type Si wafers. The wafers had an ultrathin native SiO_x layer on the order of 1–1.5 nm on top of the Si substrate prior to the deposition of the high permittivity dielectric layer. These latter layers were deposited at a temperature of 300 °C and a pressure of 1 Torr. The precursors used for the deposition of ZrO_2 and TiO_2 were ZrCl_4 and H_2O , and TiCl_4 and H_2O , respectively. The layer thickness, as estimated by

spectroscopic ellipsometry, is $(7.4 \pm 0.1) \text{ nm}$ and $(5.5 \pm 0.1) \text{ nm}$ for the ZrO_2 and TiO_2 layer, respectively. MOS capacitors were defined on the gate dielectric stacks by evaporating gold dots ($5 \times 10^{-3} \text{ cm}^2$ area) through a shadow mask. Current-voltage (*I*–*V*) measurements of the capacitors as well as constant gate voltage stress experiments were performed using a HP 4156A semiconductor parameter analyzer.

The *I*–*V* characteristics of the 7.4 nm ZrO_2 layer recorded after different times of constant gate voltage stress (substrate injection) are shown in Fig. 1. One observes that the gate current in the low voltage region increases with increasing stress time. This behavior is similar to the stress-induced leakage current (SILC) observed in ultrathin SiO_2 layers.¹¹⁻¹³ This SILC contribution has been attributed to trap-assisted tunneling through neutral electron traps generated in the SiO_2 layer during the electrical stress of the capacitor.^{11,14}

The increase of the current density $\Delta J(t) = J(t) - J(0)$ during constant voltage stress of the $\text{SiO}_x/\text{ZrO}_2$ stack is shown in Fig. 2 for different values of the gate voltage stress.

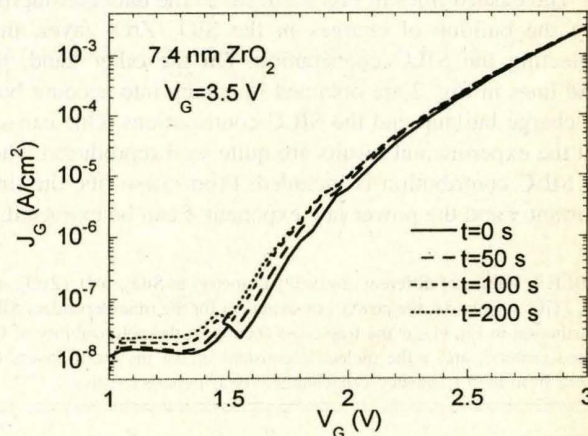


FIG. 1. Current-voltage characteristics of a MOS capacitor with a 7.4 nm ZrO_2 layer recorded after different times of constant gate voltage stress at 3.5 V.

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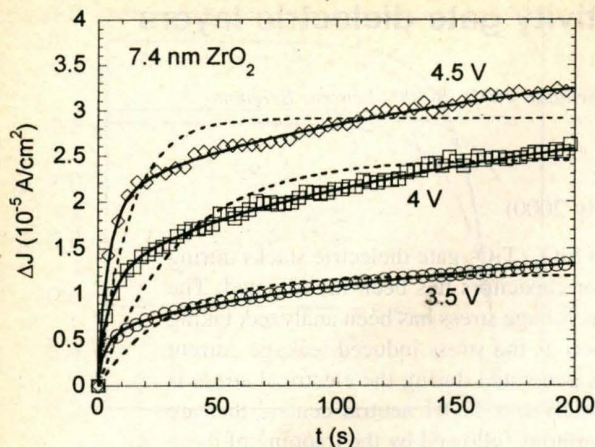


FIG. 2. Time dependence of the current density increase ΔJ observed during constant gate voltage stress of MOS capacitors with a 7.4 nm ZrO_2 layer. Solid lines and dashed lines are fits using Eq. (1).

One observes that the current density increases with time, and that this relative increase is more important as the gate voltage stress is increased.

The time-dependent gate current density can be modeled by the following expression:¹⁵

$$\Delta J(t) = A \left[1 - \exp\left(-\frac{t}{\tau}\right) \right] + \beta(V_G)t^\delta. \quad (1)$$

The first term of Eq. (1) accounts for the buildup of charges in the gate dielectric with a time constant τ given by¹⁶

$$\tau = \frac{q}{\sigma J_G}, \quad (2)$$

where q is the electron charge, σ the trap cross section, and J_G the mean current density injected into the gate dielectric during the electrical stress. On the other hand, the second term of Eq. (1) takes into account the SILC contribution to the gate current which, increases with time according to a power law with an exponent δ (on the order of 0.3–0.5) and is characterized by a voltage-dependent trap generation rate β .^{13,17}

The dashed lines in Fig. 2 are fits to the data considering only the buildup of charges in the $\text{SiO}_x/\text{ZrO}_2$ layer, thus neglecting the SILC contribution. On the other hand, the solid lines in Fig. 2 are obtained by taking into account both the charge buildup and the SILC contributions. One can see that the experimental results are quite well reproduced when the SILC contribution is included. From these fits, the time constant τ and the power law exponent δ can be extracted. It

TABLE I. Values of different physical parameters in SiO_2 , $\text{SiO}_x/\text{ZrO}_2$, and $\text{SiO}_x/\text{TiO}_2$ layers. δ is the power-law exponent for the time-dependent SILC contribution in Eq. (1), σ the trap cross section, α the polarizability of OH related centers^a, and ϵ the dielectric constant of the insulating layers extracted from high frequency capacitance–voltage characteristics.

Sample	δ	σ (cm^2)	α ($\text{\AA}^3$)	ϵ
SiO_2	0.3	1.5×10^{-16}	3.13	3.9
$\text{SiO}_x/\text{ZrO}_2$	0.4	2.0×10^{-18}	5.51	15.3
$\text{SiO}_x/\text{TiO}_2$	0.3	2.3×10^{-19}	5.19	26.2

^aSee Ref. 23.

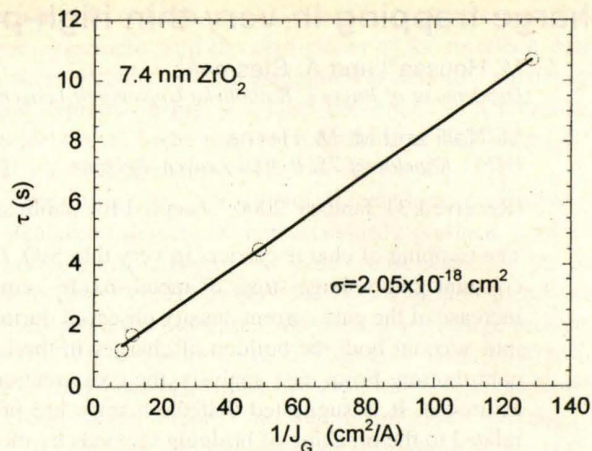


FIG. 3. Time constant τ as a function of the inverse of the current density J_G injected into the gate stack during constant voltage stress experiments performed on a 7.4 nm ZrO_2 layer. The solid line is a fit to the data obtained by using Eq. (2).

should be remarked that the value of δ has been fixed for the different gate voltage stress conditions. The values found for the exponent δ (see Table I) are lying between 0.3 and 0.4 for the $\text{SiO}_x/\text{ZrO}_2$ and $\text{SiO}_x/\text{TiO}_2$, respectively; the value of δ found for a reference thermal SiO_2 layer (2.7 nm thick) is also given in Table I.

The time constant τ extracted from Eq. (1) is shown in Fig. 3 as a function of the inverse of the injected gate current density J_G during the electrical stress of the $\text{SiO}_x/\text{ZrO}_2$ layer (J_G depends on the gate voltage stress V_G). One can see that τ varies almost linearly with $1/J_G$, as predicted by Eq. (2), and the trap cross section σ can be extracted from these data; these cross sections are given in Table I for the $\text{SiO}_x/\text{ZrO}_2$ and $\text{SiO}_x/\text{TiO}_2$ stacks, as well as for the reference thermal SiO_2 layer. Quite small values for σ are found in the high permittivity gate stacks (2.0×10^{-18} – $2.3 \times 10^{-19} \text{ cm}^2$) as compared to $1.5 \times 10^{-16} \text{ cm}^2$ in SiO_2 . These small values for the capture cross section suggest that the traps generated during the electrical stress are neutral centers.¹⁸ In the case of SiO_2 , neutral trapping centers with cross section on the order

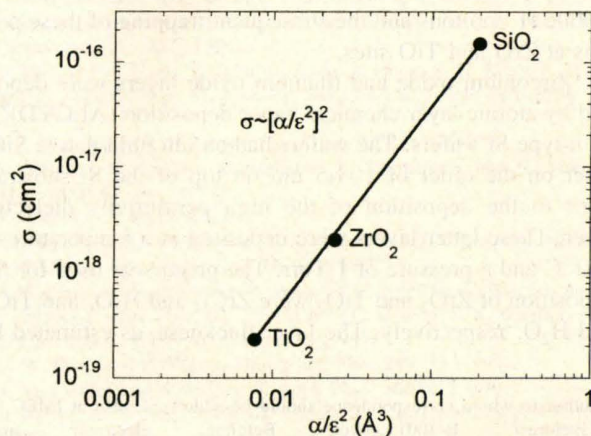


FIG. 4. Trap cross section σ as a function of the ratio (α/ϵ^2) on a log–log scale for SiO_2 , ZrO_2 , and TiO_2 gate layers. The solid line is a fit of Eq. (4) to the data.

of 10^{-16} cm^2 (i.e., values comparable to the one found in this work, see Table I) have been recently attributed^{19,20} to SiOH centers generated during the release of H^+ by hot electron impact ionization at the anode, followed by the breaking of bridging O bonds by these H^+ protons, which are subsequently trapped by the resulting SiO sites.

It is worthwhile to point out that the voltage across the SiO_x layer during the electrical stress of the $\text{SiO}_x/\text{ZrO}_2$ and $\text{SiO}_x/\text{TiO}_2$ stacks was kept below about 1.5 V, such that trap generation in the interfacial SiO_x layer is expected to be extremely small.²¹ Besides, the small values found for the trap cross sections in the high permittivity gate stack suggest that these traps are most probably generated in the ZrO_2 or TiO_2 layers. As a matter of fact, the attractive potential V of a neutral center with polarizability α in a medium of dielectric constant ϵ on a charge carrier is given by¹⁸

$$V(r) = -\frac{\alpha q^2}{2(4\pi\epsilon)^2} \frac{1}{r^4}. \quad (3)$$

Consequently, within the first order Born approximation²² the trap cross section is expected to behave like

$$\sigma \propto \left(\frac{\alpha}{\epsilon^2}\right)^2. \quad (4)$$

The trap cross section σ extracted for the different layers is plotted in Fig. 4 as a function of the ratio α/ϵ^2 on a log-log scale. By analogy with SiO_2 , we assumed that the neutral traps generated during the electrical stress of the ZrO_2 and TiO_2 gate stacks are also induced by the trapping of mobile H^+ , i.e., the values of α used in Fig. 4 are those corresponding to SiOH, ZrOH, and TiOH trapping centers, respectively.²³ It should be pointed out that the presence of H in the gate stacks comes from the use of H_2O as a source during ALCVD of the high permittivity dielectric layer. Besides, time of flight secondary ion mass spectroscopy profiles (not shown here due to the lack of space) revealed that H is uniformly distributed throughout the ZrO_2 and TiO_2 layers.

One can see from Fig. 4 that the trap cross section σ varies like a power law of (α/ϵ^2) , where the power law exponent is found to be 2.06 ± 0.01 . The agreement between the experimental results and Eq. (4) is thus excellent. Consequently, we propose that the neutral traps generated during the electrical stress of the high permittivity gate stacks are ZrOH and TiOH centers resulting from the breaking of

bridging O bonds by mobile H^+ and the subsequent trapping of these protons at ZrO or TiO sites. These results thus suggest that the reliability of the high permittivity gate stacks investigated in this work is related to the hydrogen content in these layers.

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