1 JANUARY 2000 VOLUME 87 NUMBER 1



# JOURNAL OF APPLIED PHYSICS



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# JOURNAL OF APPLIED PHYSICS

CODEN: JAPIAU
ISSN: 0021-8979
URL: http://ojps.aip.org/japo/



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# JOURNAL OF APPLIED PHYSICS


## Volume 87

## January – June 2000





**a publication of the American Institute of Physics**

AIP

JOURNAL OF APPLIED PHYSICS Vol. 87, No. 1, 1 January 2000
CODEN: JAPIAU ISSN: 0021-8979



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**A publication of the American Institute of Physics, Suite 1NO1, 2 Huntington Quadrangle, Melville, NY 11747-4502**

# Hafnium and zirconium silicates for advanced gate dielectrics

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(Received 12 May 1999; accepted for publication 21 September 1999)

Hafnium and zirconium silicate ($HfSi_xO_y$ and $ZrSi_xO_y$, respectively) gate dielectric films with metal contents ranging from ~3 to 30 at. % Hf, or 2 to 27 at. % Zr (±1 at. % for Hf and Zr, respectively, within a given film), have been investigated, and films with ~2–8 at. % Hf or Zr exhibit excellent electrical properties and high thermal stability in *direct contact* with Si. Capacitance–voltage measurements show an equivalent oxide thickness $t_{ox}$ of about 18 Å (21 Å) for a 50 Å $HfSi_xO_y$ (50 Å $ZrSi_xO_y$) film deposited directly on a Si substrate. Current–voltage measurements show for the same films a leakage current of less than $2\times10^{-6}$ A/cm$^2$ at 1.0 V bias. Hysteresis in these films is measured to be less than 10 mV, the breakdown field is measured to be $E_{BD}\sim10$ MV/cm, and the midgap interface state density is estimated to be $D_{it}\sim1-5\times10^{11}$ cm$^{-2}$ eV$^{-1}$. Au electrodes produce excellent electrical properties, while Al electrodes produce very good electrical results, but also react with the silicates, creating a lower $\epsilon$ layer at the metal interface. Transmission electron microscopy (TEM) and x-ray photoelectron spectroscopy indicate that the dielectric films are amorphous silicates, rather than crystalline or phase-separated silicide and oxide structures. TEM shows that these films remain amorphous and stable up to at least 1050 °C in direct contact with Si substrates. © *2000 American Institute of Physics.* [S0021-8979(00)00701-5]

## I. INTRODUCTION

The prospect of replacing silicon dioxide as the gate dielectric material for standard complementary metal oxide semiconductor (CMOS) technology is a formidable task, considering that $SiO_2$ has been used successfully for decades and its properties are understood as well as those of any dielectric. The area of advanced gate dielectrics has gained considerable attention recently because technology roadmaps predict the need for a sub-20 Å Si–oxide gate dielectric for sub-0.13 $\mu$m CMOS. It has been demonstrated that, for both a 15 and a 13 Å gate oxide,[1,2] a transistor intended for high-performance applications can operate with high leakage currents of 1–10 A/cm$^2$ at $V_{DD}$. Transistors intended for low-power use, such as application specific integrated circuits and wireless products, however, require lower leakage currents. There are also significant reliability concerns for $SiO_2$ in this thickness regime, regardless of the transistor application.[3] Some approaches have focused on surface preparation as a way to provide a flatter, more uniform Si interface, and thereby minimize electron channel mobility degradation and gate leakage.[4–6] Growing or depositing sub-15 Å oxides has also been investigated as a potential means for producing high-quality, reproducible, and uniform gate oxides, either for use as the gate dielectric or as the bottom layer of a dielectric stack.[7,8]

Recent efforts on alternate gate dielectrics have been focused on materials structures such as oxynitrides and oxide/nitride stacks, which provide a slightly higher $\epsilon$ value (and are therefore physically thicker) for reduced leakage, improved resistance to boron diffusion, and better reliability characteristics.[9–11] It appears that these approaches with oxide or oxide–nitride combinations will work well down to an equivalent oxide thickness $t_{ox}$ of $t_{ox}\sim15$ Å, but below this, either gate leakage or electron channel mobility degradation effects will most likely prevent further improvements in device performance. As an alternative to oxide/nitride systems, much work has been done on high-$\epsilon$ metal oxides as a means to provide a substantially thicker (physical thickness) dielectric for reduced leakage and improved gate capacitance. Work is ongoing for materials systems such as $Ta_2O_5$,[12–15] $TiO_2$,[16] $SrTiO_3$,[17] $Al_2O_3$,[18] and Zr–Sn–Ti–O,[19] which have $\epsilon$ values ranging from 10 to 80, but these have been employed mainly due to their maturity in memory capacitor and microwave applications, and the resultant semiconductor manufacturing tool development infrastructure. Most of these films, however, are not thermally stable in direct contact with Si. In particular, interfacial reaction has been observed for the cases of $Ta_2O_5$ and $TiO_2$ on Si.[20,21] For this reason, these metal oxides require that both the gate and the channel interfaces be modified to limit the amount of reaction.

Interface engineering schemes have been developed to form oxynitrides and oxide/nitride reaction barriers between the high $\epsilon$ metal oxide material and Si in an attempt to prevent or at least minimize reaction with the underlying Si.[12–16] While these barrier layers have been shown to reduce the extent of reaction between the high-$\epsilon$ dielectric and Si, the increased process complexity for the deposition and control of additional ultrathin dielectric layers, as well as scalability to later technology nodes, is a large concern. Even in the ideal case of completely eliminating interfacial reaction, however, the structure still contains several dielectrics in se-

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ries, where the lowest capacitance layer will dominate the overall capacitance and also set a limit on the minimum achievable $t_{ox}$ value.[22]

It is therefore highly desirable to use an advanced gate dielectric which is stable on Si, *and* which exhibits a Si interface quality comparable to that of $SiO_2$. This would avoid the need for an interfacial layer and at the same time, the high $\epsilon$ value of the material could be fully utilized. Previous work on alternate dielectrics, as discussed below, investigated materials systems such as $ZrO_2$ and $HfO_2$ for the purpose of optical coatings and DRAM applications. Consideration of this work is also useful for gate dielectric applications.

Examination of sputtered $ZrO_2$–$SiO_2$ codeposited, thick (~3000 Å) films has been reported by Russack and co-workers.[23] X-ray diffraction analysis of the films indicated that the films with >10% $SiO_2$ remain amorphous even upon annealing at 500 °C in air for 60 hs. Films with <10% $SiO_2$ exhibited a crystalline $ZrSiO_4$ diffraction pattern under similar annealing conditions. Composition analysis of their films, as deduced by RBS, indicated that the films have a metal:oxygen ratio of 1:2, signifying that they are fully oxidized.

Roberts *et al.* investigated $HfO_2$:$SiO_2$ films also prepared by sputter techniques.[24] They found that Hf–silicate films provided superior performance to sputtered $Ta_2O_5$ films for thin capacitor insulator film thicknesses (100–150 Å range). A preferred stoichiometry of $Hf_4SiO_{10}$ was identified as a result of breakdown measurements and $\epsilon=13$ was reported. It was noted that interfacial $SiO_2$ growth occurs upon subsequent $O_2$ annealing above 800 °C for $Hf_xSiO_{2x+2}$, where $x<2$ or $x>4$. Additionally, investigation of interface engineering using $SiO_2/Hf_4SiO_{10}/Si_3N_4$ insulator stacks provided improved performance compared to similar structures incorporating $Ta_2O_5$.

Balog *et al.*[25] have performed capacitance–voltage ($C$–$V$) measurements on very thick (~3000–4000 Å) polycrystalline $HfO_2$ films in Al/$HfO_2$/Si structures. For films grown (by CVD) at 450 °C in pure $O_2$, a large hysteresis is observed. It was indicated that subsequent anneals in inert ambients, such as in $N_2$ at 800 °C, will lead to a reduction in the observed hysteresis. However, $HfO_2$ films grown at $T \geq 500$ °C result in no observed hysteresis and $D_{it} \sim 1-6 \times 10^{11}/cm^2$. Breakdown fields for these films were reported to be ~1–2 MV/cm and $\epsilon=22-25$ at 1 MHz was reported. Balog *et al.* also found essentially identical results for $ZrO_2$ films in Al/$ZrO_2$/Si structures.[25] The dielectric constant for these films ranged from 17 to 18. However, we note that the reported Si surface preparation procedure most likely resulted in the formation of a native oxide prior to $HfO_2$ and $ZrO_2$ deposition.

Shappir *et al.* examined thinner (300–600 Å) $ZrO_2$ films (deposited by metalorganic CVD at 450 °C) in various MIS structures (with a native oxide on the substrate) that included Al, Mo, and poly-Si gates.[26] For Al gate capacitors, annealing at $T \geq 800$ °C in $N_2$ resulted in a large reduction in leakage current. Interestingly, anneals in $O_2$/HCl at 800 °C resulted in the largest reduction in leakage, although no reduction in the measured dielectric constant (due to potential $SiO_2$ formation) was observed. Breakdown fields of 4 MV/cm were reported for the subsequently annealed films. A large hysteresis was observed in all $C$–$V$ curves, with a shift of ~600 mV for unannealed and $N_2$-annealed samples, and a shift of ~200 mV for $O_2$/HCl-annealed samples. These films were estimated to have $D_{it} \sim 1 \times 10^{12}/cm^2$, which may have been even higher from the polycrystalline $ZrO_2$ were it not for the presence of the native oxide. A dielectric constant at 1 MHz ranging from 14 to 19 was observed ($\epsilon$ decreased with increasing anneal temperature), even with the native oxide present. Leakage currents in these very thick films was reported to be as low as $8 \times 10^{-9}$ A/cm$^2$ at 1.5 MV/cm.

Mo gate devices exhibited similar dielectric constants with a higher (~10x) loss tangent than that for the Al gate structures. Leakage currents were somewhat higher and breakdown was observed at a slightly lower value (~3.7 MV/cm). Since Mo has a larger work function ($\Phi_B = 4.5$ eV) than that of Al ($\Phi_B = 4.3$ eV), Mo is expected to result in a lower tunneling current for gate injection, but apparently reaction at the gate interface altered the tunneling properties. The increase in the leakage current was attributed to MoO or MoN formation during the postdeposition annealing process.

It was found that poly-Si gates produced good performance when the amorphous Si was deposited at 550 °C, followed by a $POCl_3$ doping (885 °C) and drive step (920 °C for 2.5 h), which also served to crystallize the Si electrode. (It was reported that poly-Si deposition at higher temperatures (620 °C) results in the reduction of $ZrO_2$ to form a Zr-rich layer near the poly–Si/$ZrO_2$ interface, leading to very high leakage currents.) Leakage currents were comparable to those observed for the Al or Mo gate structures, but the reported breakdown field was lower than Al, ~3 MV/cm. A dielectric constant of $\epsilon \sim 16$ was measured, again with the presence of a native oxide.

The large hysteresis and other shifts in the $C$–$V$ curves were observed for all of the electrodes and annealing conditions used in this study, which indicates that the shifts probably arise from mobile ion transport in the pure $ZrO_2$ films.[27] All of these studies on $ZrO_2$ and $HfO_2$ indicate crystallization of the metal oxides either during the deposition process or upon moderate postannealing conditions.

An important approach toward predicting and understanding the relative stability of a particular three-component system for device applications can be explained through ternary phase diagrams.[28,29] An analysis of the Gibbs free energies governing the relevant chemical reactions for the Zr–Si–O system leads to the ternary phase diagram shown in Fig. 1. The tie lines in the phase diagram for the Zr–Si–O system,[30] indicate that the metal oxide $ZrO_2$ and the compound silicate $ZrSiO_4$ will both be stable in direct contact with Si up to high temperature. The gray shaded area in Fig. 1 denotes a large field of $ZrSi_xO_y$ compositions which are expected to be stable on Si up to high temperatures. Other $ZrSi_xO_y$ compositions outside of the gray area are also stable on Si, but since it is desirable to prevent any Zr–Si bonding, film compositions within the gray area are preferable. Furthermore, even within the shaded area, compositions with high O levels (closer to $ZrSiO_4$) are preferred because this

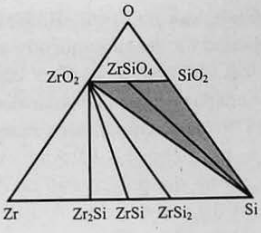



FIG. 1. Ternary phase diagram for the Zr–Si–O system. The tie lines indicate that both $ZrO_2$ and $ZrSiO_4$, as well as $ZrSi_xO_y$ silicates, are stable in direct contact with Si. The gray shaded area indicates a region of $ZrSi_xO_y$ compositions which are expected to be desirable for gate dielectrics. This figure is redrawn from Wang and Mayer (see Ref. 30).

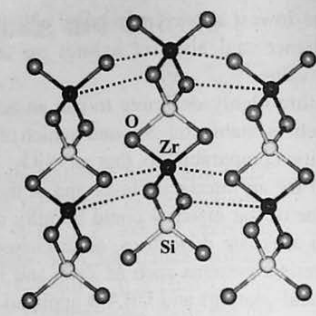



FIG. 2. Atomic model of several chain portions of the crystalline structure for $ZrO_2$–$SiO_2$ (zircon), as described by Blumenthal (see Ref. 36). Black atoms=Zr (or Hf), white atoms=Si, gray atoms=O. Dashed lines represent bonds between Zr (or Hf) atoms of a given chain and O atoms of neighboring chains, which provide a three-dimensional stability to the structure. Similar bonds exist between Zr atoms of a given chain and other O atoms of neighboring chains, but are not shown for clarity.

will be more likely to prevent M–Si bonding (M=Zr or Hf) for silicide phase formation. In fact, the existence of this large phase field of stable $ZrSi_xO_y$ compositions implies yet another potential advantage, in that the level of Zr (or Hf) incorporated into the silicate film could be gradually increased from one technology node to the next. This gradual shift in film composition could provide a continually higher $\epsilon$ value (up to a point), as is needed to meet device performance requirements.

This behavior is expected to be the same for the Hf–Si–O system based on coordination chemistry arguments. Although the thermodynamic information is incomplete for the Hf–Si–O system, the available data suggest that $HfO_2$ and $HfSiO_4$, as well as a large range of $HfSi_xO_y$ compositions, will be stable in direct contact with Si up to high temperatures.[31–33] This thermal stability is extremely important, because it suggests that there is potential to control the dielectric–Si interface. Although some schemes attempt to avoid thermal instabilities of other high-$\epsilon$ materials by using process modifications such as a replacement gate flow,[12] which allows the high-temperature processing to be done before deposition of the final gate dielectric, the continued thermal cycling afterward is sufficient to result in poor electrical properties.[12] It is therefore important to select a materials system in which the desired final state is a stable one.

Both $HfO_2$ and $ZrO_2$ have high dielectric constants and are thermally stable on Si, and therefore are potential gate dielectrics, but there are several concerns associated with these metal oxides. As mentioned previously, these oxides are ionic conductors,[27] as O ions can diffuse through the oxides and leave vacancies behind, which then can act as traps and reliability concerns. Furthermore, both $ZrO_2$ and $HfO_2$ tend to crystallize at low temperatures, leading to polycrystalline films, with high-leakage paths along grain boundaries and nonuniformities in $\epsilon$ value and in film thickness. Low-temperature deposition and processing may be used in an attempt to prevent crystallization, but it is likely that the thermal cycles required in fabricating a transistor would cause the films to crystallize. The heterointerface formed between the $ZrO_2$ or $HfO_2$ and Si may also lead to a large amount of channel electron mobility degradation, which may be manifested only in transistors and not in capacitor structures. A better approach is apparent: use a silicate dielectric from the onset.

Zirconium and hafnium silicates ($ZrSi_xO_y$ and $HfSi_xO_y$, respectively) are also stable in direct contact with Si, and by controllably incorporating a suitably high level of Si *during* deposition, the dielectric–Si interface will act more like the preferable $SiO_2$–Si interface, and the driving force is removed for any reaction between the substrate and the dielectric. The use of $ZrSi_xO_y$ (and therefore $HfSi_xO_y$) should allow for control of the Si interface, which removes the key problem that has limited other high-$\epsilon$ gate dielectric material approaches at the channel interface, and also affords the significant flexibility of continued use of poly Si-based gates. Furthermore, midgap work function metal gate systems have been predicted not to provide a performance improvement worthy of the added process complexity to replace Si-based gates.[34] The $\epsilon$ values of $HfSi_xO_y$ and $ZrSi_xO_y$ are substantially lower than those of pure $HfO_2$ and $ZrO_2$, but this tradeoff for interfacial control will be acceptable as long as the resulting leakage currents are low enough. As a note on the Hf–Si–O system, hafnium suffers the misconception that it is radioactive, but this is not the case.[35]

There has been much less information reported on $HfSi_xO_y$ than on $ZrSi_xO_y$, but the chemical similarities between Hf and Zr allow for comparison between the respective silicate systems. As described by Blumenthal,[36] and Bragg *et al.*,[37] the Bravais lattice for the stoichiometric compound $ZrSiO_4$ (zircon) is body-centered tetragonal, and belongs to point group $D_{4h}$. The crystal is composed of $SiO_4$ tetrahedra interspersed with Zr atoms, but can be considered as parallel chains of $ZrO_2$ and $SiO_2$ structural unit molecules, as shown in Fig. 2. Each Zr and Si atom shares bonds to four O atoms within each chain, and each successive pair of O atoms is oriented in a transverse configuration, forming $ZrO_2$ and $SiO_2$ units. The Si–O bond length is shorter than the Zr–O bond length within a chain (not represented in the figure). Figure 2 shows that each Zr atom also shares bonds with other O atoms in neighboring chains (only two of the four bonds to neighboring chains are shown for each Zr atom, for clarity), providing a three-dimensional stability to the material.

It is important to note that each Zr and Si atom has only O atoms as nearest neighbors. Chemical analysis of homogeneous silicate films is therefore expected to show only Zr–O nearest-neighbor bonding, with a slight effect from Si as a next-nearest neighbor. Although the films presented in this study are amorphous, it is reasonable to assume that for Hf and Zr concentrations less than that of the stoichiometric $MO_2$–$SiO_2$ compound, nearly all bonds will be Zr–O (or Hf–O) and Si–O bonds.

Using coordination chemistry arguments between Hf and Zr, $HfSiO_4$ should have the same structure as $ZrSiO_4$. A value of $\epsilon = 12.6$ for $ZrSiO_4$ is reported by Blumenthal,[36] which is reasonable considering that this structure is comprised of $SiO_2$ ($\epsilon = 3.9$) and $ZrO_2$ ($\epsilon = 25$) components. Similarly, since $HfO_2$ has reported values[25,38] of $\epsilon = 25$–$40$, an $HfSiO_4$ compound is expected to have a range of $\epsilon = 15$–$25$. The exact value of $\epsilon$ will certainly depend strongly on film composition, density, and structure, since amorphous materials, which are used in this study, typically have less lattice polarizability than their crystalline counterparts. Considering all of the desired properties, $HfSi_xO_y$ and $ZrSi_xO_y$ should be excellent materials candidates for advanced gate dielectrics, and indeed some very encouraging results have been previously reported.[39,40]

Finally, the potential use of silicates as a replacement for $SiO_2$ gate dielectrics should not be viewed as a significant departure from the historical progression of dielectrics in CMOS technology. Silicon dioxide has been unimaginably ideal for integrated circuits, because it has been used for decades both as the interlevel dielectric (ILD) between successive metal interconnect levels and as the gate oxide for MOSFETs. Recent technology demands, however, have required that $SiO_2$ in the ILD be modified to create a lower dielectric constant, so that lower RC time delays can be achieved. These changes have been made by simply incorporating H, F, and C into the $SiO_2$ to lower the $\epsilon$ value of the oxide. These modifications, while certainly not trivial, have thus far proved to be manageable and integrable.

Similar demands for higher drive currents and lower leakage have required $SiO_2$ in the gate dielectric to be altered by adding N, both in the form of doping and as a silicon nitride layer on top of $SiO_2$. This process slightly increases the effective dielectric constant, allowing use of a physically thicker film, and thereby achieves a higher drive current with less leakage. With these trends in mind, silicate gate dielectrics should also be viewed as only another modification of $SiO_2$, in this case by "doping" with Zr of Hf, to further improve device performance while remaining compatible with the rest of well-established CMOS processing procedures. In fact, if these silicate films can be used, then by simply increasing the "doping" level of Zr or Hf from one technology node to the next for gradually improved device performance, this same materials system should fulfill the requirements on current roadmaps until the year 2010.

In this study, it is shown that a thin dielectric layer of $HfSi_xO_y$ or $ZrSi_xO_y$ yields a $t_{ox}$ value ranging from 18 to 22 Å with a leakage current density less than $2\times10^{-6}$ A/cm$^2$, while remaining in a glassy, amorphous state in *direct contact* with Si during anneals up to 1050 °C for 20 s. The physical and electrical properties of $HfSi_xO_y$ and $ZrSi_xO_y$ dielectric films are described based on the results of a variety of analysis techniques.

## II. EXPERIMENT

Substrates were 4 in. *n*- and *p*-type Si(100) wafers, both with $\rho = 0.01$–$0.02\,\Omega$ cm. Samples were prepared by etching in a buffered (1%) HF solution for approximately 20 s, leaving an H-terminated surface. Once under vacuum, hydrogen was desorbed by annealing the wafer at 700 °C for 10 min. The silicate films were deposited by two methods. Most silicates were sputter deposited in a system with a base pressure of $5\times10^{-9}$ Torr, with sputter rates of 5–6 Å/min and substrate temperatures ranging from 25 to 600 °C. The substrates were heated radiatively from the back side, with an absolute temperature accuracy of ±20 °C over the temperature range used. Some silicate films were deposited by *e*-beam evaporation in an ultrahigh vacuum (UHV) chamber, with a base pressure of $7\times10^{-11}$ Torr and deposition rates of 2–10 Å/s. Substrate temperature range and heating method were the same as the case for sputtering. Films with high Hf and Zr levels (up to 30 at. %) were achievable by this method, but the electrical properties of these films were typically poor. In this article, therefore, only physical characterization is presented on films deposited by *e*-beam evaporation in the UHV system.

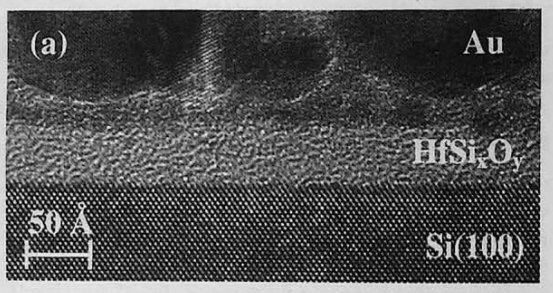
Capacitors were formed using Au and Al *ex situ* thermal evaporation at room temperature, followed by photolithography and wet etching steps to pattern the electrodes. $C$–$V$ measurements were performed in parallel mode on an HP 4284 LCR meter at frequencies up to 1 MHz. Capacitor areas ranged from $10^{-6}$ to $10^{-2}$ cm$^2$, and both capacitance and current scaled linearly with area, indicating uniform, high-quality films.

## III. RESULTS AND DISCUSSION

### A. Physical characterization

Figure 3 shows high-resolution TEM images of a 50 Å $Hf_6Si_{29}O_{65}$ film before and after annealing. Figure 3(a) shows the as-deposited film, which was sputter deposited at a substrate temperature of 500 °C, with an Au cap. The $HfSi_xO_y$–Si interface is seen to be atomically sharp, and the silicate is completely amorphous. Figure 3(b) shows the same film after an anneal at 800 °C for 30 min in a $N_2$ ambient (Au deposited after anneal). The film remains amorphous, the interface remains sharp, and the thickness of the layer shows no visible change after anneal at high temperature, which demonstrates the stability of $HfSi_xO_y$ films in direct contact with Si. Au lattice fringes are visible in both (a) and (b).

Figure 4 shows high-resolution TEM images of a 50 Å $Zr_4Si_{31}O_{65}$ film before and after annealing. Figure 4(a) shows the as-deposited film, which was sputtered at room temperature, with an Al cap. The $ZrSi_xO_y$–Si interface is seen to be atomically sharp, within the region of the TEM image, and the silicate is completely amorphous. It should be noted that all of the samples studied showed similarly sharp interfaces



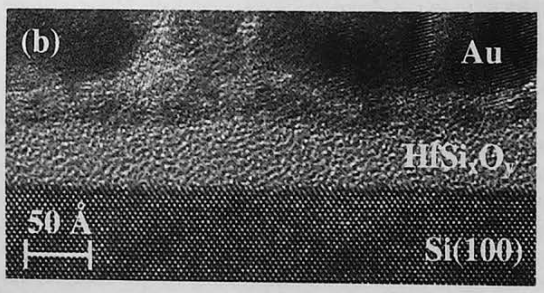
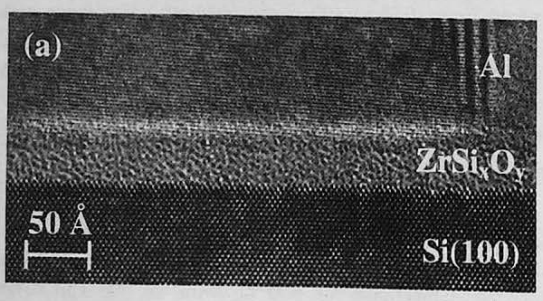




FIG. 3. TEM cross section of a 50 Å $Hf_6Si_{29}O_{65}$ film with an Au cap (a) as-deposited at 500 °C and (b) after annealing at 800 °C for 30 min in $N_2$. The silicate film remains amorphous and stable, with no sign of reaction after the anneal.



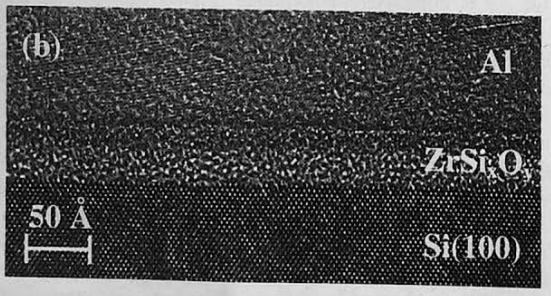
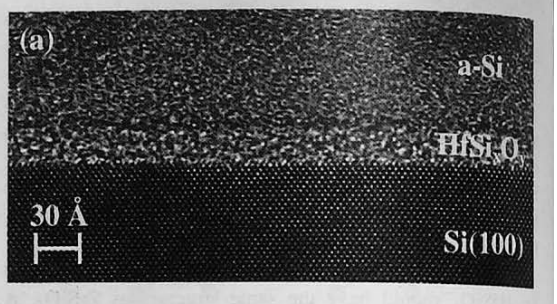




FIG. 4. TEM cross section of a 50 Å $Zr_4Si_{31}O_{65}$ film with an Al cap (a) as-deposited at 500 °C and (b) after annealing at 800 °C for 30 min in $N_2$. The silicate film remains amorphous and stable, but the slight contrast difference at the Al interface indicates possible reaction.



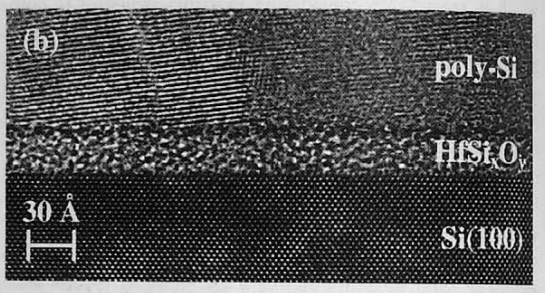




FIG. 5. TEM cross section of a ~30 Å $Hf_7Si_{29}O_{64}$ film with a Si cap (a) as-deposited at 500 °C and (b) after annealing at 1050 °C, for 20 s in $N_2$. The amorphous Si cap crystallized during the anneal, but the film remained amorphous and stable, while maintaining atomically sharp interfaces with both the substrate and the cap layer.

for samples taken from all across the wafers. The termination of the Al lattice fringes on the silicate layer clearly denotes the top interface. Figure 4(b) shows the same film after an anneal at 800 °C for 30 min in a $N_2$ ambient (Al deposited after anneal). As in the case of $Hf_6Si_{29}O_{65}$, the interface remains sharp and the thickness of the layer shows no visible change after anneal at high temperature. There is a slight contrast difference visible in the $Zr_4Si_{31}O_{65}$ layer near the top Al interface in both images. It is possible that this contrast difference arises from some slight reaction of the Al electrode with the $ZrSi_xO_y$ film. Similar contrast is visible for the case of Al on $HfSi_xO_y$ films, but no such contrast differences are visible for Au electrodes on either $HfSi_xO_y$ or $ZrSi_xO_y$ films. Evidence of Al–silicate reaction will be further discussed below in Sec. III B.

Figure 5 shows TEM images of a ~30 Å $Hf_7Si_{29}O_{64}$ film, sputter deposited at 500 °C, with a Si cap, before and after annealing. In Fig. 5(a), an amorphous Si layer has been deposited at 25 °C to provide a capping layer on the silicate. Both interfaces are seen to be atomically sharp, with no signs of reaction, and the silicate film is completely amorphous. Figure 5(b) shows the same film after rapid thermal annealing at 1050 °C for 20 s, which emulates a dopant activation anneal. It can be seen that while the top Si layer has crystallized into poly–Si, the silicate film remains entirely unchanged. The $Hf_7Si_{29}O_{64}$ film is still completely amorphous and is the same thickness as before the anneal, while both Si interfaces have remained atomically sharp. These observations confirm the predictions made by thermodynamics, and indicates that by using silicates, the interface can indeed be

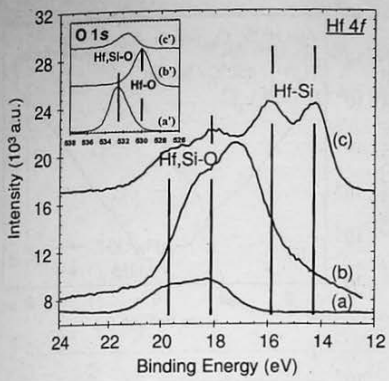



FIG. 6. Hf $4f$ XPS features for: (a) thin $Hf_6Si_{29}O_{65}$ film, (b) thick $HfO_2$ film, and (c) thick O-rich $HfSi_2$ film. No evidence of Hf–Si bond formation is observed for the Hf–silicate film. (Inset) Oxygen $1s$ XPS features for: (a) thin $Hf_6Si_{29}O_{65}$ film, (b) thick $HfO_2$ film, and (c) thick O-rich $HfSi_2$ film. Silicate formation (vs metal–oxide) is confirmed by the O $1s$ feature.

controlled up to the required thermal processing treatments, while the film remains in a glassy phase.

Chemical characterization of various $HfSi_xO_y$ and $ZrSi_xO_y$ films was accomplished by x-ray photoelectron spectroscopy (XPS) utilizing monochromatic and standard Al x-ray sources. Figure 6 shows a comparison of the Hf $4f$ features for: (a) a thin, 53 Å $Hf_6Si_{29}O_{65}$ film to very thick, (b) $HfO_2$, and (c) $HfSi_2$ films. The intensity of (a) is much less than that of (b) and (c) because the $HfO_2$ and $HfSi_2$ films were much thicker than the silicate film. (The $HfSi_2$ film has residual oxygen contamination from the deposition ambient and is thus perhaps more properly described as an "O-rich" $HfSi_2$ film.). It can be seen that curve (a) exhibits features consistent with the formation of Hf–O bonding in the vicinity of Si. No evidence (within detectable limits) of Hf–Si bond formation in the $Hf_6Si_{29}O_{65}$ film is observed, as the Hf $4f$ doublet for Hf–Si bonding, shown in (c), is widely separated from that due to Hf–O bonding (in the vicinity of Si). This lack of Hf–Si bonding is expected in the $HfSi_xO_y$

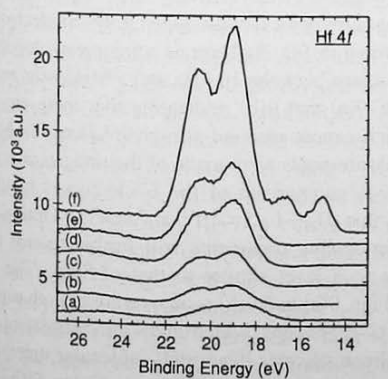



FIG. 7. XPS spectra of the Hf $4f$ region for sputtered and $e$-beam evaporated $HfSi_xO_y$ films. Sputtered $Hf_6Si_{29}O_{65}$ films at: (a) 25 °C; (b) 300 °C; (c) 400 °C; (d) 500 °C; (e) 600 °C; $Hf_{28}Si_{30}O_{42}$ film evaporated at (f) 600 °C. The evaporated film clearly shows peaks for Hf–Si silicide bonding, whereas none of the sputtered films show Hf–Si peaks.

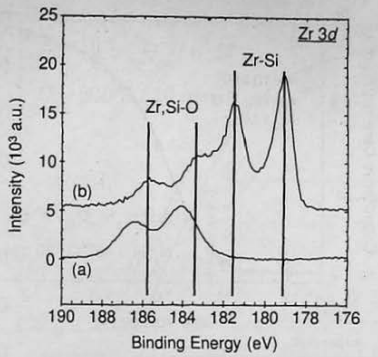



FIG. 8. XPS data with Zr $3d$ features of: (a) a $Zr_5Si_{31}O_{64}$ film and (b) an O-rich $ZrSi_2$ film. No evidence of Zr–Si bond formation is observed for the Zr–silicate film.

films, based on the structural model of $ZrSiO_4$ described earlier, which shows that Zr (or Hf) and Si atoms, respectively, are only bonded to O atoms as nearest neighbors. The data in Fig. 6 are consistent with the formation of a silicate film without phase separation into silicides. Indeed, comparison of the Hf $4f$ features for curves: (a) $Hf_6Si_{29}O_{65}$ and (b) $HfO_2$ films in Fig. 6 confirms that the bonding in (a) is consistent with a silicate rather than a metal oxide. This is also evident by inspection of the O $1s$ features for these samples, shown in the Fig. 6 inset. The observed O $1s$ binding energy of ~532 eV is consistent with a silicate bond rather than a metal–oxide bond (~530 eV).

Figure 7 shows the monochromatic XPS spectra for various $HfSi_xO_y$ films as a function of thickness. These data were charge corrected by aligning the Si substrate spectral feature to 99.5 eV.[41] The Hf $4f$ feature intensity increases with thickness, as expected. Figure 7 shows a comparison of XPS spectra for several $HfSi_xO_y$ films, deposited by both sputtering at temperatures ranging from 25 to 600 °C [curves (a)–(e)] and $e$-beam evaporation at 600 °C [curve (f)]. The evaporated film shows clear peaks associated with Hf–Si bonding, which are not present in the sputtered films. All evaporated silicates showed evidence of silicide bonding, regardless of deposition temperature, whereas none of the sputtered films showed silicide bonding. The silicide bonding may be a result of the specific $e$-beam evaporation conditions used. As mentioned previously, any silicide formation is highly undesirable, and this is in part responsible for the poor electrical properties measured for the evaporated films. Preliminary time-of-flight secondary mass ion spectroscopy analysis (not shown here) also indicates the presence of Hf–Si and Zr–Si fragments for the evaporated films, which is a further indication of silicide bonding.

Similar data were obtained for the $ZrSi_xO_y$ films. Figure 8 presents a comparison of the Zr $3d$ region for: (a) a 160 Å $Zr_5Si_{31}O_{64}$ film to that obtained for (b) an O-rich $ZrSi_2$ film after Ar sputtering. It can again be seen that the film obtained is a silicate with no evidence of Zr–Si bond formation within detectable limits. The expected increase in the Zr intensity as a function of thickness was also observed (not shown).

Rutherford backscattering spectrometry and XPS measurements agreed well, and showed typical Hf film compo-

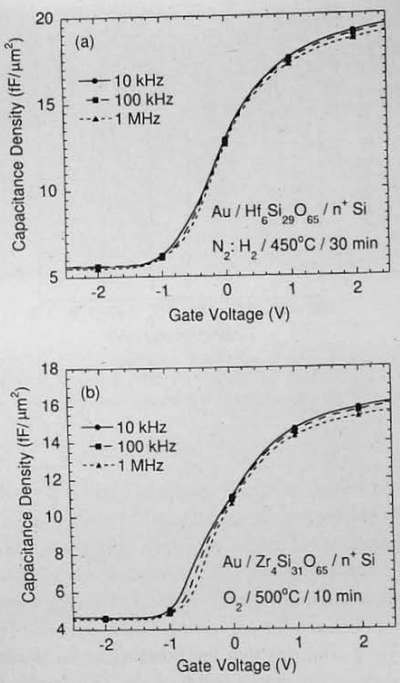



FIG. 9. $C-V$ curves of thin $HfSi_xO_y$ and $ZrSi_xO_y$ films, with Au electrodes ($A=1.76\times10^{-4}$ cm$^2$): (a) 50 Å $Hf_6Si_{29}O_{65}$ film on $n^+$ Si, deposited at 500 °C, and subsequently annealed in forming gas at 450 °C for 30 min. The $C_{max}/A$ value in accumulation yields $t_{ox}=17.8$ Å; (b) 50 Å $Zr_4Si_{31}O_{65}$ film on $n^+$ Si, deposited at 25 °C, and subsequently annealed in $O_2$ at 600 °C for 10 min. The capacitance density in accumulation yields $t_{ox}=20.8$ Å. These films have some dispersion near zero bias which indicates the presence of interface traps.

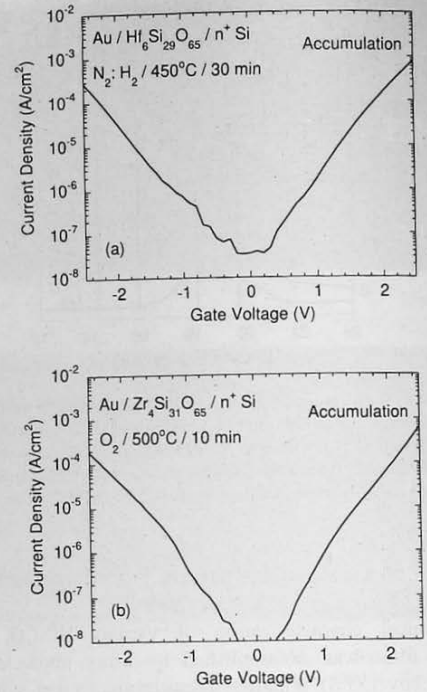



FIG. 10. $I-V$ curves for films shown in Fig. 9: (a) Au/50 Å $Hf_6Si_{29}O_{65}/n^+$ Si. (b) Au/50 Å $Zr_4Si_{31}O_{65}/n^+$ Si. These films show extremely low leakage currents, which are below $2\times10^{-6}$ A/cm$^2$ at 1.0 V in accumulation. The $I-V$ curves are well behaved, and appear nearly symmetrical about zero bias. This suggests nearly equal barrier heights in both polarities.

sitions to be approximately $Hf_6Si_{29}O_{65}$ (±1 at. % for Hf). Depending on deposition conditions, however, the composition ranged down to $Hf_3Si_{30}O_{67}$ or up to $Hf_{30}Si_{10}O_{60}$ (obtained by *e*-beam deposition). Typical Zr films had compositions of $Zr_4Si_{31}O_{65}$ (±1 at. % for Zr), but overall ranged from $Zr_2Si_{32}O_{66}$ to $Zr_{27}Si_{15}O_{58}$ (highest Zr levels obtained by *e*-beam evaporation). Further data accumulation by XPS may allow determination of other physical properties of these silicates, such as the inelastic mean free path for electrons.[42]

### B. Electrical characterization

The $C-V$ characteristics of thin $HfSi_xO_y$ and $ZrSi_xO_y$ films are shown in Fig. 9. A plot of the $C-V$ curves for an Au/50 Å $Hf_6Si_{29}O_{65}/n^+$ Si structure are shown in Fig. 9(a), with an electrode area of $1.76\times10^{-4}$ cm$^2$. The silicate film was deposited directly on Si at 500 °C and postannealed in forming gas (90% $N_2$:10% $H_2$) at 450 °C for 30 min. The largest value of measured capacitance density in accumulation is $C_{max}/A=19.3$ fF/$\mu$m$^2$, which corresponds to $\epsilon\sim11$, or an equivalent oxide thickness of $t_{ox}=17.8$ Å, where $t_{ox}$ is the electrical thickness equivalent for pure $SiO_2$.[43] This is the first reported oxide equivalent below 20 Å for a single layer advanced gate dielectric deposited directly on Si. Figure 9(b) shows the $C-V$ curves for an Au/50 Å $Zr_4Si_{31}O_{65}/n^+$ Si structure, which also has an electrode area of $1.76\times10^{-4}$ cm$^2$. The silicate film was deposited directly on Si at 25 °C and postannealed in $O_2$ at 600 °C for 10 min. The largest value of measured capacitance density in accumulation corresponds to an equivalent oxide thickness of $t_{ox}=20.8$ Å. This is a very promising $t_{ox}$ value, considering that the film was deposited directly on Si.

Figure 9 also demonstrates that the Au electrode, with a work function $\Phi_B=5.3$ eV,[44] creates a flatband condition at zero bias ($V_{fb}\sim0$ V). Au was chosen for its chemical inertness and because of its relatively large $\Phi_B$. Work is underway to measure devices with doped poly–Si electrodes, such as that shown in Fig. 5. There is a frequency dependence of the capacitance between 10 kHz and 1 MHz near zero bias in both Figs. 9(a) and 9(b), indicating that there are interface traps which cannot respond at high frequency. Although no direct measurements were made of the midgap interface state density $D_{it}$, comparison of the $C-V$ curves to ideal ones indicates that $D_{it}\sim1-5\times10^{11}$ cm$^{-2}$ eV$^{-1}$. Optimization of the postprocessing treatments will further reduce the interface traps to a level similar to that of $SiO_2$. The 100 kHz curve in Figs. 9(a) and 9(b) is an overlay of both positive and negative $C-V$ sweeps, which gives a hysteresis of less than 10 mV. Since silicates have $SiO_2$ molecular units, and have similar Si–O bond lengths (1.62 Å) to pure $SiO_2$, it is not surprising that forming gas sinters work well for these materials.

The corresponding current–voltage ($I-V$) characteristics for the films represented in Fig. 9 are shown in Fig. 10.

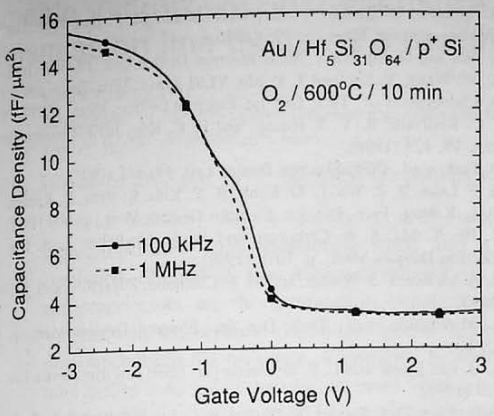



FIG. 11. $C-V$ curves of a 65 Å $Hf_5Si_{31}O_{64}$ film on $p^+$ Si, deposited at 500 °C, followed by anneal in forming gas (90% $N_2$:10% $H_2$) at 450 °C for 30 min, with Au electrodes ($A=1.76\times10^{-4}$ cm$^2$). The capacitance density at $C_{max}$ corresponds to $t_{ox}=21.2$ Å. The dispersion near zero bias indicates interface traps, and $V_{fb}\sim-1$ V, which is expected since $V_{fb}\sim0$ V for a similar on $n^+$ Si, as shown in Fig. 9.

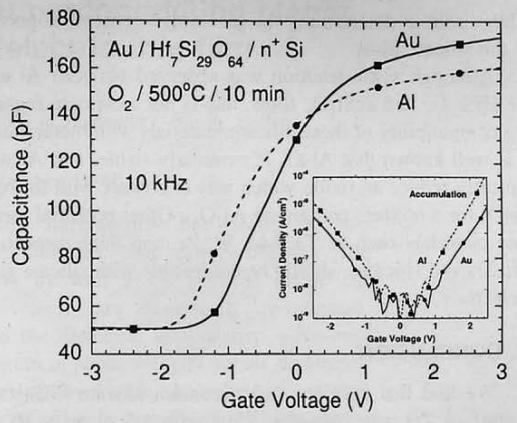



FIG. 12. $C-V$ curves at 10 kHz of a 60 Å $Hf_7Si_{29}O_{64}$ film on $n^+$ Si, deposited at 400 °C followed by an anneal in $O_2$ at 500 °C for 10 min, with Au and Al electrodes of equal area. The lower $C_{max}$ value for the Al electrode indicates reaction between the Al and $HfSi_xO_y$ to form a lower-$\epsilon$ layer. The larger, negative $V_{fb}$ value for the Al curve results from the lower Al $\Phi_B$ value than that of Au, as well as from some $C-V$ stretchout caused by traps in the poor-quality reaction layer. The inset shows the corresponding $I-V$ curves. The higher $\Phi_B$ value for Au results in a lower leakage current compared to Al. The reaction layer with Al may also allow slightly higher leakage. The symmetrical Au $I-V$ curves indicate a flatband condition, whereas the lower Al $\Phi_B$ value results in asymmetrical silicate barrier heights.

Figure 10(a) displays the $I-V$ characteristics for the Au/50 Å $Hf_6Si_{29}O_{65}/n^+$ Si sample shown in Fig. 9(a), with the same Au electrode area. The leakage current density is very low for this film, ranging from $10^{-6}$ to $10^{-5}$ A/cm$^2$ in the bias range from 1.0 to 1.5 V. A pure $SiO_2$ layer of the same electrical ~18 Å thickness[45] has a current density of approximately 1 A/cm$^2$, nearly six orders of magnitude higher leakage current than that for an electrically equivalent $Hf_6Si_{29}O_{65}$ film. Although these results use an Au electrode ($\Phi_B=5.3$ eV) and the leakage characteristics of $SiO_2$ reported in Ref. 45 used an Al electrode ($\Phi_B=4.3$ eV), leakage currents measured on both the $HfSi_xO_y$ and $ZrSi_xO_y$ films showed only a ~2× increase for Al electrodes compared to Au. The order of magnitude comparison of the $SiO_2$ and $HfSi_xO_y$ or $ZrSi_xO_y$ leakage currents is therefore valid. Figure 10(b) shows the $I-V$ plots for the Au/50 Å $Zr_4Si_{31}O_{65}/n^+$ Si sample in Fig. 9(b). The leakage current density is very low, as $J=7\times10^{-7}$ A/cm$^2$ at a bias of 1.0 V. Similar to the $Hf_6Si_{29}O_{65}$ film in Fig. 10(a), the $Zr_4Si_{31}O_{65}$ film in Fig. 10(b) shows an enormous reduction in leakage current over a comparable, electrically equivalent thickness of a pure $SiO_2$ layer.[45] The overall greatly reduced leakage currents measured for both $HfSi_xO_y$ and $ZrSi_xO_y$ result from the physically thicker 50 Å film as well as from the amorphous structure of the film. Devices that were voltage ramped to hard breakdown consistently showed a breakdown field $E_{BD}$ of $E_{BD}>10$ MV/cm. The $I-V$ curves in Figs. 10(a) and 10(b) are also seen to be nearly symmetrical, suggesting that transport under both gate and substrate injection may be limited by very similar activation energies.

Figure 11 shows the $C-V$ curves of a 65 Å $Hf_5Si_{31}O_{64}$ film on $p^+$ Si, deposited at 500 °C, and followed by anneal in forming gas (90% $N_2$:10% $H_2$) at 450 °C for 30 min, with Au electrodes ($A=1.76\times10^{-4}$ cm$^2$). The capacitance density measured in accumulation at $C_{max}$ corresponds to $t_{ox}=21.2$ Å. Since this film is thicker than that shown in Fig. 9(a), the capacitance density is proportionally lower, but both films exhibit $\epsilon\sim11$. It is important to note that this film exhibits $V_{fb}\sim-1$ V on $p^+$ Si, as expected since the film in Fig. 9(a) showed $V_{fb}\sim0$ V on $n^+$ Si. Some dispersion of the capacitance is visible between 100 kHz and 1 MHz, again indicating the presence of interface traps. No postmetal annealing was done in an attempt to further reduce $D_{it}$. The leakage current for this film (not shown) was comparable to that shown in Fig. 10, which is about $10^{-6}$ A/cm$^2$ at a bias voltage of 1 V in accumulation. The data in Fig. 11 demonstrate that these films can be deposited on heavily doped $p^+$ Si wafers with high-quality electrical properties.

Au electrodes consistently showed the best electrical behavior for both $ZrSi_xO_y$ and $HfSi_xO_y$, but Al electrodes were also tested extensively. Reaction between the Al electrodes and the silicate films was nearly always observed, but the resulting electrical properties were still very good. Figure 12 shows the $C-V$ curves at 10 kHz of a 60Å $Hf_7Si_{29}O_{64}$ film on $n^+$ Si, deposited at 400 °C followed by an anneal in $O_2$ at 500 °C for 10 min, with Au and Al electrodes of equal area. The lower $C_{max}$ value for the Al electrode indicates reaction between the Al and $HfSi_xO_y$ to form a lower-$\epsilon$ layer. The reaction layer is seen to reduce the $C_{max}$ value by less than 10% of that for Au, which is still high. The larger, negative $V_{fb}$ value for the Al curve results mainly from the lower Al $\Phi_B$ value compared to that of Au, as well as from some $C-V$ stretchout caused by traps in the lower-$\epsilon$ reaction layer. The inset of Fig. 12 shows the corresponding $I-V$ curves. The higher $\Phi_B$ value for Au results in a lower leakage current compared to Al. The reaction layer with Al may also allow slightly higher leakage. The symmetrical Au $I-V$ curves indicate a flatband condition, whereas the lower Al $\Phi_B$ value results in asymmetrical silicate barrier heights. Substrate temperature and postannealing conditions will play

a large role in determining the resulting electrical properties of the silicate films.

Although some reaction was observed between Al and the $HfSi_xO_y$ and $ZrSi_xO_y$ films, this is not a concern regarding compatibility of these silicate materials with metal gates. It is well known that $Al_2O_3$ is extremely stable, and Al will typically reduce an oxide which it is in contact with to form $Al_2O_3$ (or a mixture containing $Al_2O_3$). Other potential metal gate materials such as Ta, Mo, W, Zr, and their respective nitrides and silicides, should be compatible with silicate gate dielectrics.

## IV. CONCLUSION

We find that hafnium and zirconium silicate ($MSi_xO_y$, M=Hf or Zr) gate dielectric films with ~3–8 at. % Hf or 2–5 at. % Zr exhibit excellent electrical properties and high thermal stability in *direct contact* with Si. $C-V$ measurements show an equivalent oxide thickness $t_{ox}$ less than 18 Å for a 50 Å $Hf_6Si_{29}O_{65}$ film deposited directly on a Si substrate, which yields a dielectric constant $\epsilon \sim 11$. These physically thick, amorphous films maintain extremely low leakage currents. The silicon oxide-like nature of these films appears to help achieve a high-quality interface with Si, high breakdown field strength, and low hysteresis, while still responding to standard forming gas sinters. More work needs to be done, however, in order to better understand the electron transport mechanisms, and to determine how these films behave in transistors with doped poly–Si gates and full processing treatments.

Since these films were limited to low Hf and Zr concentrations by the source target composition and deposition conditions, films which have compositions closer to stoichiometric $MSiO_4$ are expected to exhibit a further increased dielectric constant value while maintaining a low leakage current. Obtaining the $MSiO_4$ stoichiometry should not be necessary, however, especially since it is desirable to maintain an amorphous structure. Any film composition which is somewhat Si rich will be suitable.

## ACKNOWLEDGMENTS

The authors are grateful to M. Howell and R. Beavers for outstanding technical support, to J. Julien for XPS measurements, to M. Douglas for ToF SIMS measurements, and to J. Chervinsky for RBS measurements. Thanks go to S. Tang, B. Brar, S. Summerfelt, and L. Colombo for many useful and interesting discussions.

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