

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GlobalFoundries U.S. Inc.

Petitioner

v.

Godo Kaisha IP Bridge 1

Patent Owner

Patent No. 6,197,696

Filing Date: March 23, 1999

Issue Date: March 6, 2001

Title: METHOD FOR FORMING INTERCONNECTION STRUCTURE

Inter Partes Review No. *To be assigned*

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *ET SEQ.***

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Petition Exhibit 1001:	U.S. Patent No. 6,197,696 to Aoi et al.
Petition Exhibit 1002:	Expert Declaration of Dr. Bruce W. Smith, Ph.D.
Petition Exhibit 1003:	U.S. Patent No. 3,617,824 to Shinoda et al.
Petition Exhibit 1004:	U.S. Patent No. 3,838,442 to Humphreys.
Petition Exhibit 1005:	U.S. Patent No. 6,140,226 to Grill et al.
Petition Exhibit 1006:	U.S. Patent No. 5,635,423 to Huang et al.
Petition Exhibit 1007:	U.S. Patent No. 5,741,626 to Jain et al.
Petition Exhibit 1008:	C. Akrouit et al., "A 480-MHz Microprocessor in a 0.12 μ m L _{eff} CMOS Technology with Copper Interconnects," IEEE J. of Solid-State Circuits, Vol. 33, no. 11 (November 1998).
Petition Exhibit 1009:	J.N. Burghartz et al., "Monolithic Spiral Inductors Fabricated Using a VLSI Cu-Damascene Interconnect Technology and Low-Loss Substrates," International Electron Devices Meeting (December 1996).
Petition Exhibit 1010:	U.S. Patent No. 6,100,184 to Zhao et al.
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Petition Exhibit 1015:	Japanese Patent Application No. 11-075519 to Aoi.
Petition Exhibit 1016:	Certified Translation of Japanese Patent Application No. 11-075519 to Aoi.
Petition Exhibit 1017:	U.S. Provisional Patent Application No. 60/071,628.
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Petition Exhibit 1019:	U.S. Patent No. 5,920,790 to Wetzel et al.

I. Preliminary Statement

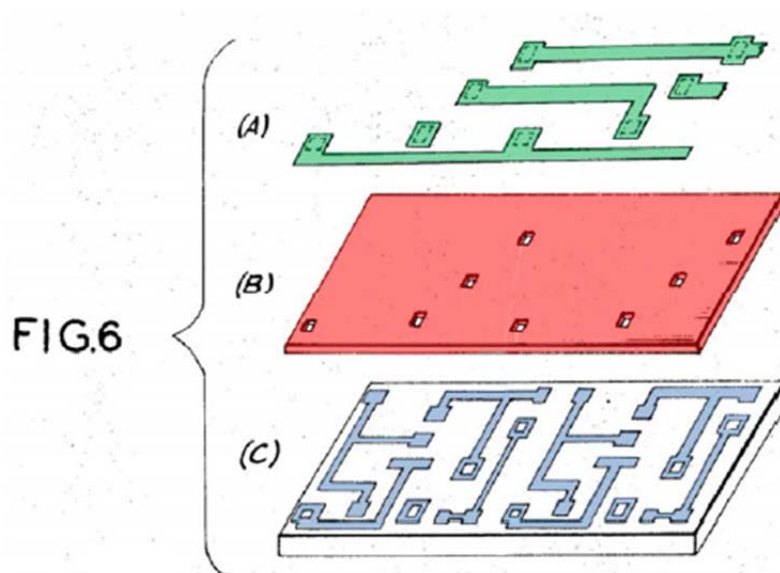
U.S. Patent No. 6,197,696 (Ex. 1001) is directed to methods for forming integrated circuit “interconnects,” which link components in a microchip. In particular, the ’696 patent is directed to common “dual damascene” processes for forming interconnects.

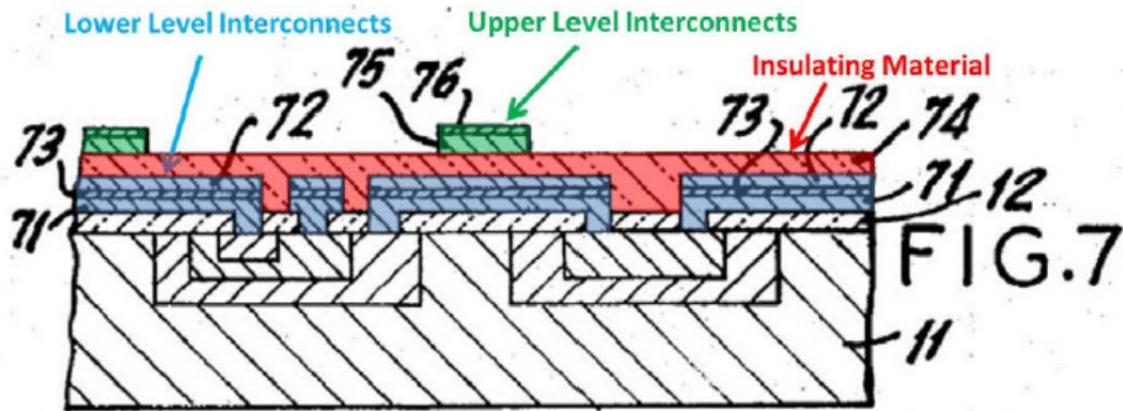
Supported by the Expert Declaration of Bruce Smith, Ph.D., (Ex. 1002), this Petition establishes that challenged claims 10–12 are unpatentable. Rather than defining novel or nonobvious subject matter, the challenged claims recite well-known processes for making well-known structures. Petitioner respectfully requests *inter partes* review under 35 U.S.C. §§311–319 and 37 C.F.R. §42.100 *et seq.*, and cancellation of the challenged claims.

II. Technological Background

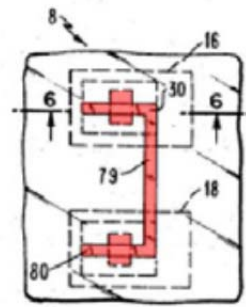
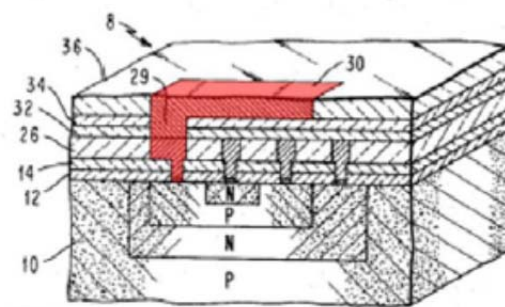
A. Integrated Circuits and Interconnections

Integrated circuits contain millions of discrete semiconductor devices electrically connected by “interconnections,” or “interconnects,” to form circuits. *Shinoda* (Ex. 1003), which dates to 1965, provides an early example. (Ex. 1003, 4:30–73, Figs. 6, 7 (below with highlights and annotations).)





Interconnects typically have “via” portions extending between the planes of adjacent layers to provide electrical connections between those layers. (Ex. 1002, ¶33.) Interconnects also typically have “trench” patterns, which act as wires to define circuits by linking the vias appropriately. These interconnect schemes were common years before the application for the ’696 patent was filed. (*See, e.g.*, Ex. 1004, Abstract, 1:54–2:6, 8:19–54, Figs. 6, 6A (below with highlights), 7, 7A.)



Multiple levels of interconnects are typical. (Ex. 1002, ¶34.) Examples of this type of wiring scheme, which was also common years before the time the application for the ’696 patent was filed, appear below. (Ex. 1008, 1–4, Fig. 2; Ex. 1009, 1–2, Fig. 2; Ex. 1002, ¶34.)

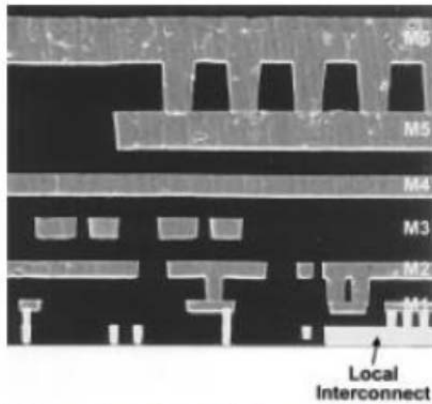


Fig. 2. Scanning electron microscope of six copper metal levels and local interconnect.

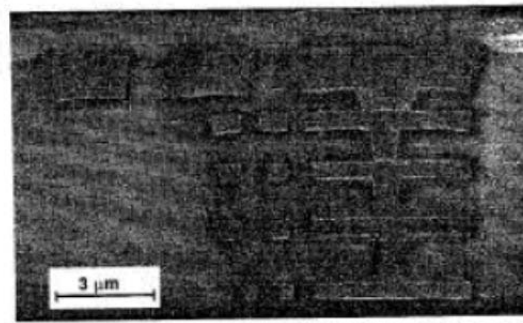
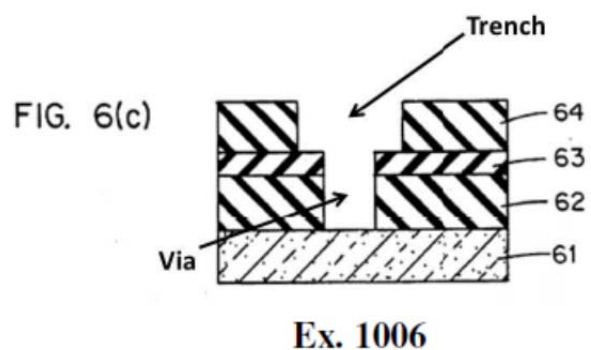
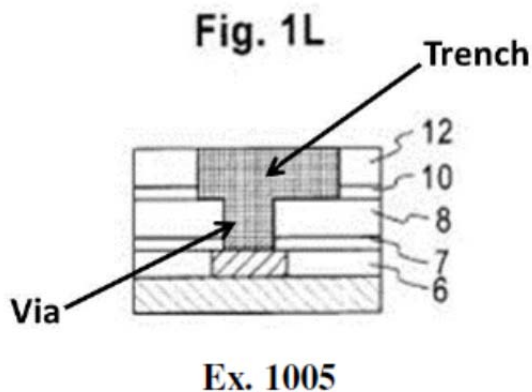
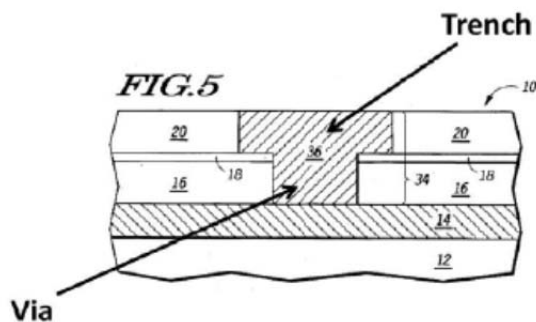


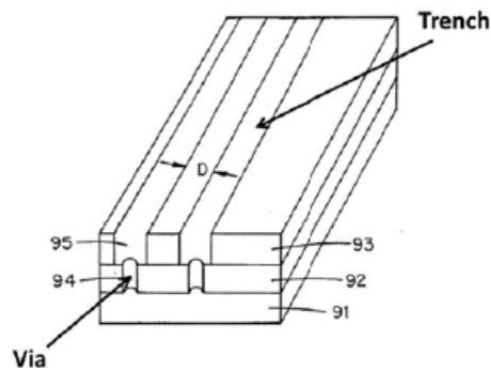
Fig. 2. Cross-sectional SEM of a five-level Cu-damascene interconnect structure with oxide isolation. (Note that the structure is illustrated to demonstrate the VLSI capability of the process; the dimensions of metal layers, vias, and oxide isolation are different from the ones used for the inductor fabrication.)

In a dual damascene process, via and trench structures are formed during the same process. (See Ex. 1009, 1; Ex. 1002, ¶35.) Via and trench patterns are etched into insulating material, then filled with metal and polished flat. (Ex. 1002, ¶35.) Dual damascene processes result in the typical via- trench interconnect structure described above. (Ex. 1005, 1:45–48, 3:33–36; Ex. 1006, Abstract, 2:61–3:2, 3:54–57; Ex. 1007, 2:15–20.) Examples appear below with annotations. (Ex. 1005, Fig. 1L; Ex. 1006, Figs. 6(c), 9; Ex. 1007, Fig. 5.)





Ex. 1007

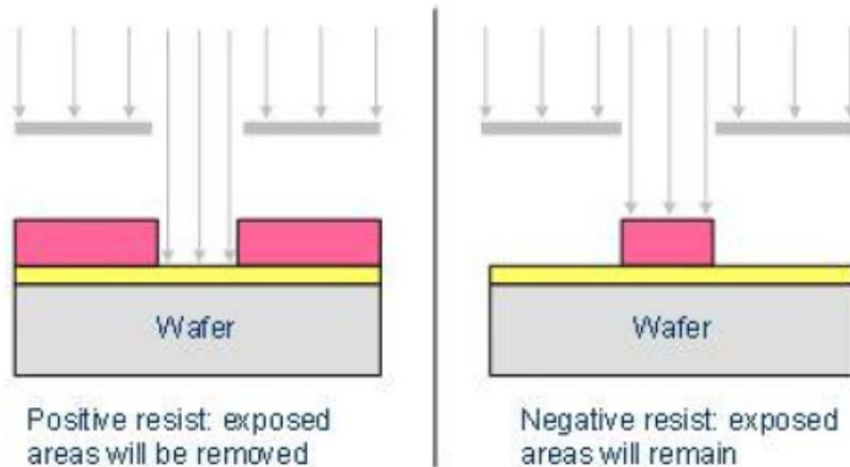


Ex. 1006

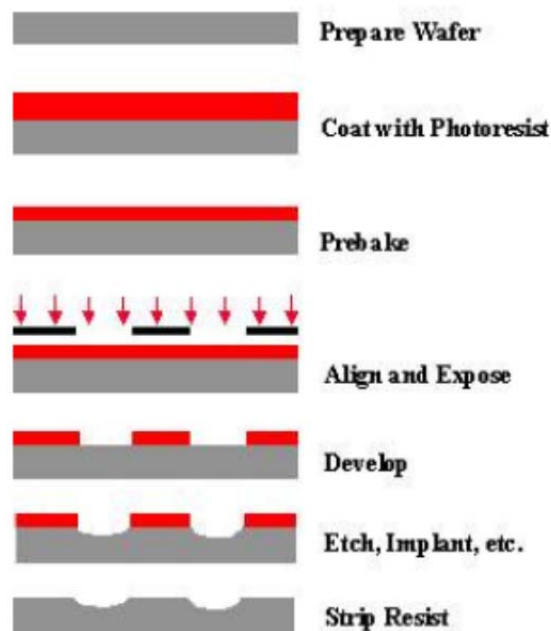
B. Semiconductor Etching and Photolithography

Two processing technologies that can create patterns in a semiconductor wafer are photolithography and etching. In photolithography, a chemical called photoresist coats the surface of the semiconductor wafer. (Ex. 1002, ¶37.) Photoresist changes its molecular structure when illuminated under certain conditions. (*Id.*) A photomask, which is transparent in some regions and opaque in others, contains a pattern that can be transferred to the photoresist. (*Id.*, 138.) After the photomask is aligned to the coated wafer, the photoresist is illuminated through the photomask. (*Id.*) The exposed photoresist is altered by the light, and any photoresist not part of the pattern can be removed with a chemical “developer.” (*Id.*, 139.)

The processed wafer retains the patterned photoresist layer, which can pattern material underneath. (*Id.*) Schematic representations of photolithography appear below. (*Id.*, 140.)



A patterned photoresist layer can serve as a mask during an “etch” process. In etching, the surface of the processed wafer (semiconductor substrate and/or overlying layers) is exposed to corrosive chemicals to remove certain portions. (*Id.*, 142.) After etching, the photoresist may be “stripped” (removed) by another chemical treatment. (*Id.*, 143.) In some cases, the etching process itself may even remove the photoresist. A representation of photolithography and etching appears below.



(*Id.*)

An etch that attacks all exposed materials is called a non-selective etch, whereas an etch that attacks certain material compositions more than others is called a selective etch. (*Id.*, ¶44.) An etch that attacks a material in all directions is called isotropic, whereas an etch that attacks in a preferred direction (often perpendicular to the surface of the wafer) is called anisotropic. (*Id.*, ¶45.) An etch that uses a liquid etching agent is a “wet” etch, whereas an etch that does not use a liquid etching agent (typically using an ionized gas, called a “plasma”) is a “dry” etch. (*Id.*, ¶46.) Dual damascene processes typically use selective, anisotropic, dry etching. (*Id.*, ¶47; *see also, e.g.*, Ex. 1006, 2:61–63; Ex. 1010, 2:44–48; Ex. 1011, 4:9–12.)

III. The '696 Patent

A. Description of the Challenged Claims

This Petition challenges the patentability of claims 10–12 of the '696 patent. Independent claim 10 recites “[a] method for forming an interconnection structure,” and claims 11 and 12 depend from claim 10. (Ex. 1001, 34:1–57.) As illustrated below, claim 10 reads on several embodiments of the '696 patent. (Ex. 1002, ¶¶48–127; *see also* Ex. 1001, 22:47–29:60, Figs. 21(a)–37(b).) The declaration of Dr. Smith also describes the challenged claims and the embodiments of the '696 patent. (*See* Ex. 1002, ¶¶48–139.)

1. step a) of Claim 10

Step a) of claim 10 recites “forming a first insulating film [503, 602] over lower-level metal interconnects [501, 601].”

In the fifth embodiment the claimed first insulating film is “first organic film 503[/553],” located over first metal interconnects 501 [or 551]. (Ex. 1001, 22:52–60, 24:60–25:1, Figs. 21(a), 24(a); Ex. 1002, ¶¶51–52.) In the sixth embodiment the claimed first insulating film is “silicon nitride film 602[/652],” located over first metal interconnects 601 [or 651]. (Ex. 1001, 28:1–9,

30:1–11, Figs. 30(a), 33(a); Ex. 1002, ¶¶53–54.) Examples of step a) from the fifth and sixth embodiments of the '696 patent are shown below with highlights. (Ex. 1001, 22:52–23:24, 28:1–36, Figs. 21(a), 30(a); Ex. 1002, ¶¶50–55.)

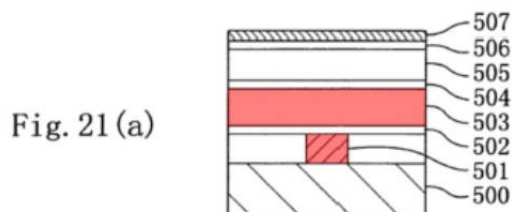


Fig. 21 (a)

Fifth Embodiment

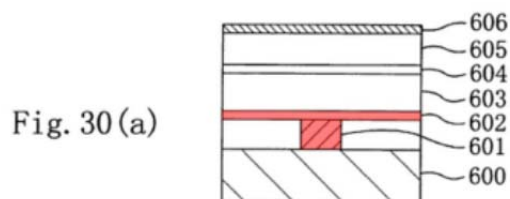


Fig. 30 (a)

Sixth Embodiment

2. step b) of Claim 10

Step b) of claim 10 recites “forming a second insulating film [504, 603], having a different composition than that of the first insulating film, over the first insulating film [503, 602].”

In the fifth embodiment the claimed second insulating film is “first silicon dioxide film 504[554],” with a composition that differs from the first insulating film (first organic film 503 [or 553]). (Ex. 1001, 22:57–62, 24:65–25:3, Figs. 21(a), 24(a); Ex. 1002, ¶¶57–58.) In the sixth embodiment the claimed second insulating film is “first organic film 603[653],” with a composition that differs from the first insulating film (silicon nitride film 602 [or 652]). (Ex. 1001, 28: 1– 9, 30:1–9, Figs. 30(a), 33(a); Ex. 1002, ¶¶59–60.) Examples of step b) from the '696 patent are shown below with highlights. (Ex. 1001, 22:57–62, 28:1–36, Figs. 21(a), 30(a); Ex. 1002, ¶¶56–61.)

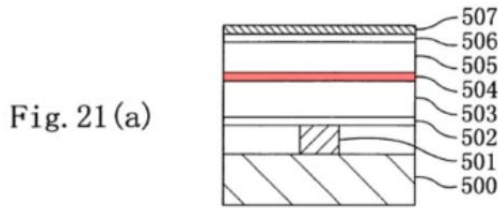


Fig. 21 (a)

Fifth Embodiment

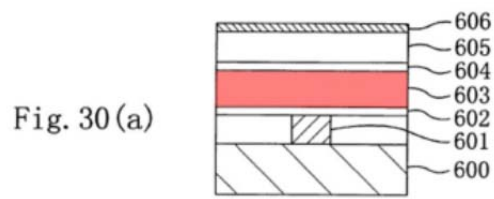


Fig. 30 (a)

Sixth Embodiment

3. step c) of Claim 10

Step c) of claim 10 recites “forming a third insulating film [505, 604], having a different composition than that of the second insulating film, over the second insulating film [504, 603].”

In the fifth embodiment the claimed third insulating film is “second organic film 505[555],” with a composition that differs from the second insulating film (first silicon dioxide film 504 [or 554]). (Ex. 1001, 22:60–64, 25:1–6, Figs. 21(a), 24(a); Ex. 1002, ¶¶63–64.) In the sixth embodiment the claimed third insulating film is “silicon dioxide film 604[654],” with a composition that differs from the second insulating film (first organic film 603 [or 653]). (Ex. 1001, 28: 6–11, 30:6–11, Figs. 30(a), 33(a); Ex. 1002, ¶¶65–66.) Examples of step c) from the ’696 patent are shown below with highlights. (Ex. 1001, 22:60–64, 28:1–36, Figs. 21(a), 30(a); Ex. 1002, ¶¶62–67.)

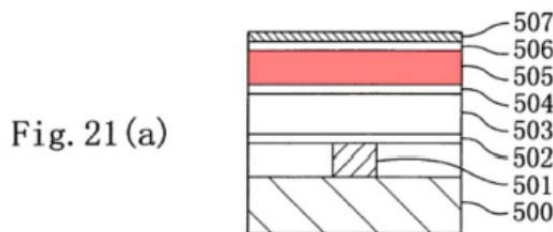


Fig. 21 (a)

Fifth Embodiment

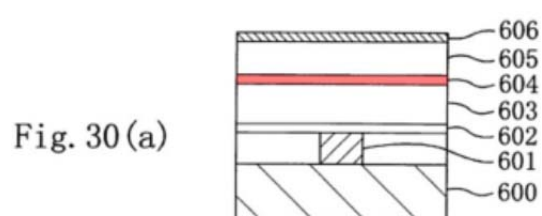


Fig. 30 (a)

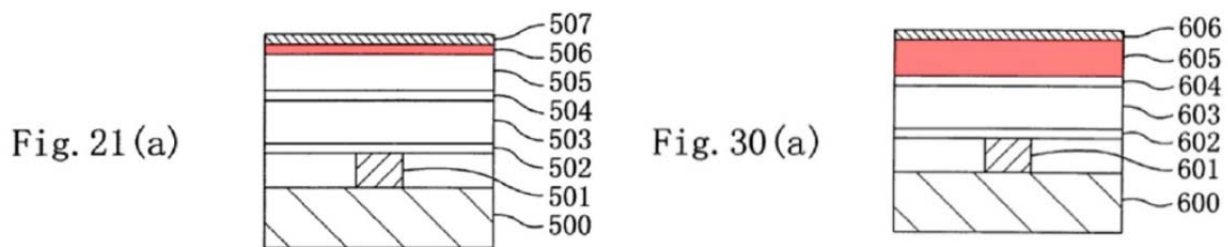
Sixth Embodiment

4. step d) of Claim 10

Step d) of claim 10 recites “forming a fourth insulating film [506, 605], having a different

composition than that of the third insulating film, over the third insulating film [505, 604].”

In the fifth embodiment the claimed fourth insulating film is “second silicon dioxide film 506[/556],” with a composition that differs from the composition of the third insulating film (second organic film 505 [or 555]). (Ex. 1001, 22:62–67, 25:3–9, Figs. 21(a), 24(a); Ex. 1002, ¶¶69–70.) In the sixth embodiment the claimed fourth insulating film is “second organic film 605[/655],” with a composition that differs from the composition of the claimed third insulating film (silicon dioxide film 604 [or 654]). (Ex. 1001, 28: 9–14, 30:9–14, Figs. 30(a), 33(a); Ex. 1002, ¶¶71–72.) Examples of step d) from the ’696 patent are shown below with highlights. (Ex. 1001, 22:62–67, 28:1–36, Figs. 21(a), 30(a); Ex. 1002, ¶¶68–73.)



5. step e) of Claim 10

Step e) of claim 10 recites “forming a thin film [507, 606] over the fourth insulating film [506, 605].”

In the fifth embodiment, “a titanium nitride film 507[/557] (thin film) is deposited to be 50 nm thick.” (Ex. 1001, 23:1–3, 25:9–11, Figs. 21(a), 24(a); Ex. 1002, ¶¶75–76.) In the sixth embodiment, “a titanium nitride film 606[/656] (thin film) is deposited to be 50 nm thick.” (Ex. 1001, 28:14–16, 30:14–16, Figs. 30(a), 33(a); Ex. 1002, ¶¶77–78.) Examples of step e) from the ’696 patent are shown below with highlights. (Ex. 1001, 23:1–3, 28:1–36, Figs. 21(a), 30(a); Ex. 1002, ¶¶74–79.)

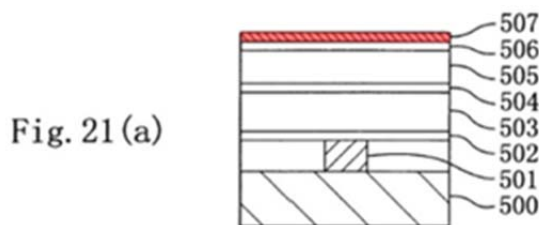


Fig. 21 (a)

Fifth Embodiment

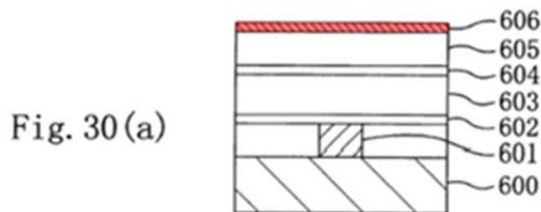


Fig. 30 (a)

Sixth Embodiment

6. step f) of Claim 10

Step f) of claim 10 recites “forming a first resist pattern [508, 607] on the thin film [507, 606], the first resist pattern having openings for forming wiring grooves.”

In the fifth embodiment “a first resist pattern 508[558], having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 507[557].” (Ex. 1001, 23:25–27, 25:19–21, Figs. 21(b), 24(b); Ex. 1002, ¶¶81–82.) In the sixth embodiment “a first resist pattern 607[657], having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 606[656].” (Ex. 1001, 28:37–39, 30:37–39, Figs. 30(b), 33(b); Ex. 1002, ¶¶82–83.) Examples of step f) from the ’696 patent are shown below with highlights. (*Id.*, 23:25–27, 28:37–43, Figs. 21(b), 30(b); Ex. 1002, ¶¶80–85.)

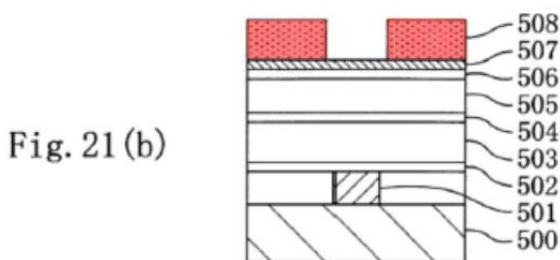


Fig. 21 (b)

Fifth Embodiment

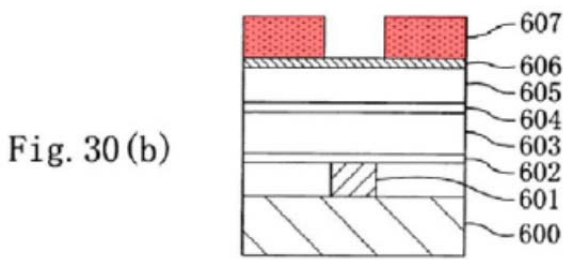


Fig. 30 (b)

Sixth Embodiment

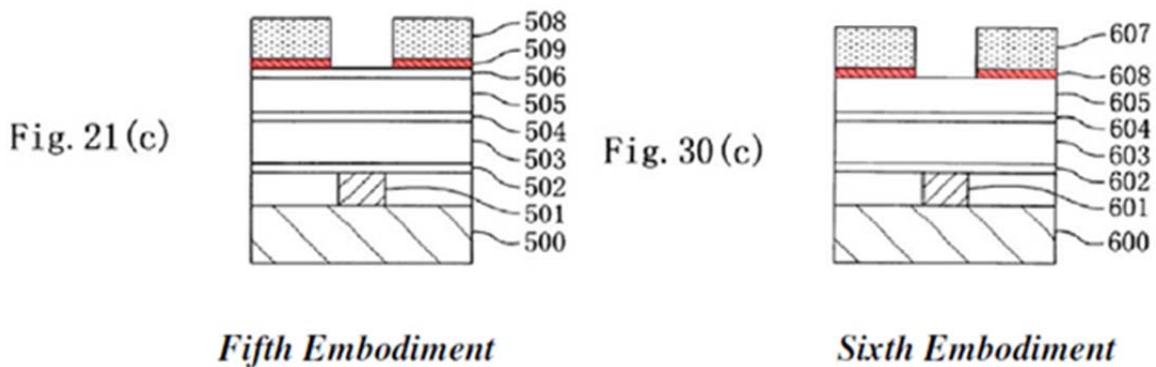
7. step g) of Claim 10

Step g) of claim 10 recites “etching the thin film [507, 606] using the first resist pattern

[508, 607] as a mask, thereby forming a mask pattern [509, 608] out of the thin film to have the openings for forming wiring grooves.”

In the fifth embodiment “the titanium nitride film 507[557] is dry-etched using the first resist pattern 508[558] as a mask, thereby forming a mask pattern 509[559], having openings for forming wiring grooves, out of the titanium nitride film 507[557].” (Ex. 1001, 23:27–32, 25:21–25, Figs. 21(c), 24(c); ex. 1002, ¶¶87–88.) In the sixth embodiment “the titanium nitride film 606[656] is dry-etched using the first resist pattern 607[657] as a mask, thereby forming a mask pattern 608[658], having openings for forming wiring grooves, out of the titanium nitride film 606[656].” (Ex. 1001, 28:39–43, 30:39–43, Figs. 30(c), 33(c); Ex. 1002, ¶¶89–90.)

Examples of step g) from the '696 patent are shown below with highlights. (Ex. 1001, 23:27–32, 28:37–43, Figs. 21(c), 30(c); Ex. 1002, ¶¶86–91.)



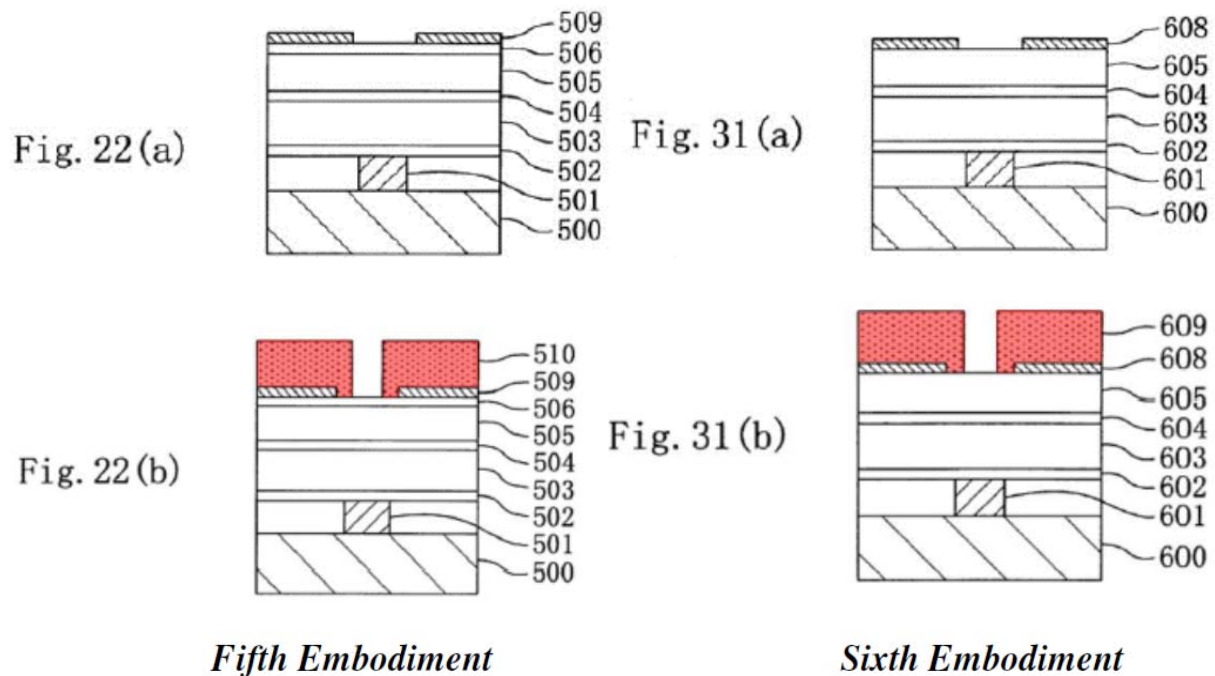
8. step h) of Claim 10

Step h) of claim 10 recites “removing the first resist pattern [508, 607] and then forming a second resist pattern [510, 609] on the fourth insulating film [506, 605] and the mask pattern [509, 608], the second resist pattern having openings for forming contact holes.”

In the fifth embodiment, “the first resist pattern 508[558] is removed.” (Ex. 1001, 23:33–34, 25:26–27, Figs. 22(a), 25(a).) “Then, as shown in FIG. 22(b)[FIG. 25(b)], a second resist pattern 510[560], having openings for forming contact holes, is formed by lithography on

the mask pattern 509[559].” (*Id.*, 23:40–42, 25:27–35, Figs. 22(b), 25(b); Ex. 1002, ¶¶93–94.)

In the sixth embodiment, “the first resist pattern 607[657] is removed.” (Ex. 1001, 28:44–46, 30:44–46, Figs. 31(a), 34(a).) “Then, as shown in FIG. 31(b)[FIG. 34(b)], a second resist pattern 609[659], having openings for forming contact holes, is formed by lithography on the mask pattern 608[658].” (*Id.*, 28:49–51, 30:49–57, Figs. 31(b), 34(b); Ex. 1002, ¶¶95–96.) Examples of step h) from the ’696 patent are shown below with highlights. (Ex. 1001, 23:33–42, 28:44–51, Figs. 22(a), 22(b), 31(a), 31(b); Ex. 1002, ¶¶92–97.)



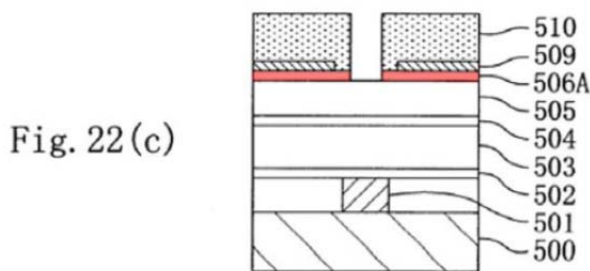
9. step i) of Claim 10

Step i) of claim 10 recites “dry-etching the fourth insulating film [506, 605] using the second resist pattern [510, 609] and the mask pattern [509, 608] as a mask, thereby patterning the fourth insulating film [506, 605] to have the openings for forming contact holes.”

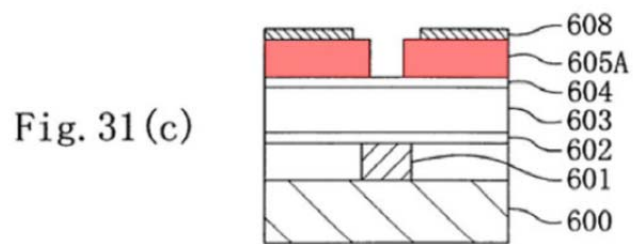
In the fifth embodiment, “the second silicon dioxide film 506[556] is dry-etched using the second resist pattern 510[560] and the mask pattern 509[559] as a mask, thereby forming a

patterned second silicon dioxide film 506A[/556A] having openings for forming contact holes.”

(Ex. 1001, 23:42–46, 25:36–41, Figs. 22(c), 25(c); Ex. 1002, ¶¶99–100.) In the sixth embodiment, “the second organic film 605[/655] is dry-etched using the second resist pattern 609[/659] and the mask pattern 608[/658] as a mask, thereby forming a patterned second organic film 605A[/655A] having openings for forming contact holes.” (Ex. 1001, 28:51–55, 30:58–62, Figs. 31(c), 34(c); Ex. 1002, ¶¶101–02.) Examples of step i) from the ’696 patent are shown below with highlights. (Ex. 1001, 23:42–46, 28:51–55, Figs. 22(c), 31(c); Ex. 1002, ¶¶98–103.)



Fifth Embodiment



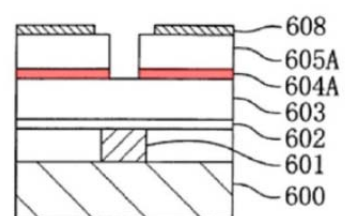
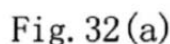
Sixth Embodiment

10. step i) of Claim 10

Step j) of claim 10 recites “dry-etching the third insulating film [505, 604] using the patterned fourth insulating film [506A, 605A] as a mask, thereby patterning the third insulating film [505A, 604A] to have the openings for forming contact holes.”

In the fifth embodiment, “the second organic film 505[/555] is dry-etched using the patterned second silicon dioxide film 506A[/556A] as a mask, thereby forming a patterned second organic film 505A[/555A] having openings for forming contact holes.” (Ex. 1001, 23:47–51, 25:66–26:3, Figs. 23(a), 26(a); Ex. 1002, ¶¶105–06.) In the sixth embodiment, “the silicon dioxide film 604[/654] is dry-etched using the patterned second organic film 605A[/655A] as a mask, thereby forming a patterned silicon dioxide film 604A[/654A] having openings for

Examples of step j) from the '696 patent are shown below with highlights. (Ex. 1001, 23:47–51, 29:1–5, Figs. 23(a), 32(a); Ex. 1002, ¶¶104–09.)

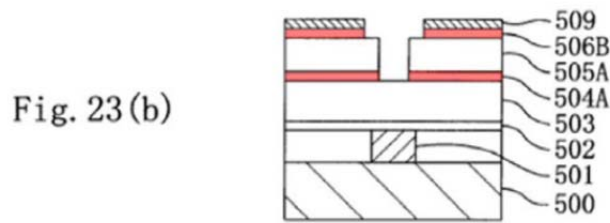


Sixth Embodiment

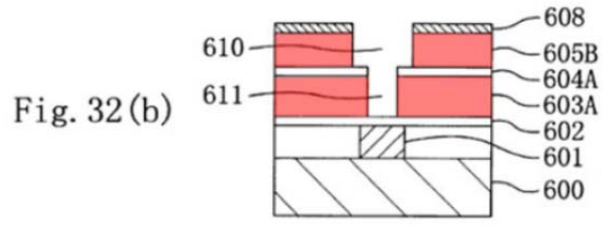
Step k) of claim 10 recites “dry-etching the patterned fourth insulating film [506A, 605A] and the second insulating film [504, 603] using the mask pattern [608] and the patterned third insulating film [505A, 604A] as respective masks, thereby forming wiring grooves [511, 610] in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes [512, 611].”

In the fifth embodiment, “the patterned second silicon dioxide film 506A[/556A] and the first silicon dioxide film 504[/554] are dry-etched using the mask pattern 509[/559] and the patterned second organic film 505A[/555A] as respective masks, thereby forming a patterned second silicon dioxide film 506B[/556B] having [openings for forming] wiring grooves and a patterned first silicon dioxide film 504A[/554A] having openings for forming contact holes as shown in FIG. 23(b)/[FIGS. 26(b) and 28(b)].” (Ex. 1001, 23:66–24:6, 26:15–22, Figs. 23(b), 26(b), 28(b); Ex. 1002, ¶¶111–12.) In the sixth embodiment, “the patterned second organic film 605A[/655A] and the first organic film 603[/653] are dry-etched using the mask pattern 608[/658] and the patterned silicon dioxide film 604A[/654A] as respective masks, thereby

forming a patterned second organic film 605B[/655B] having wiring grooves 610[/660] and a patterned first organic film 603A[/653A] having contact holes 611[/661].” (Ex. 1001, 29:6–12, 31:12–18, Figs. 32(b), 35(b); Ex. 1002, ¶¶113–14.) Examples of step k) from the ’696 patent are shown below with highlights. (Ex. 1001, 23:66–24:6, 29:6–12, Figs. 23(b), 32(b); Ex. 1002, ¶¶110–15.)



Fifth Embodiment



Sixth Embodiment

12. step l) of Claim 10

Step l) of claim 10 recites “dry-etching the patterned third insulating film [505A, 604A] and the first insulating film [503, 602] using the mask pattern [509, 608] and the patterned second insulating film [504A, 603A] as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively.”

In the fifth embodiment, “the patterned second organic film 505A[/555A] and the first organic film 503[/553] are dry-etched using the mask pattern 509[/559] and the patterned first silicon dioxide film 504A[/554A] as respective masks, thereby forming a patterned second organic film 505B[/555B] having wiring grooves 511[/561] and a patterned first organic film 503A[/553A] having contact holes 512[/562].” (Ex. 1001, 24:7–13, 26:22–29, Figs. 23(c), 26(c), 29(a); Ex. 1002, ¶¶117–18.) In the sixth embodiment, “patterned silicon dioxide film 604A[/654A] and the silicon nitride film 602[/652] are dry-etched using the mask pattern 608[/658] and the patterned first organic film 603A[/653A] as respective masks, thereby forming a patterned silicon dioxide film

604B[/654B] having wiring grooves (see FIG. 32(c)/[FIG. 35(c)]) and a patterned silicon nitride film 602A[/652A] having the contact holes (see FIG. 32(c)/[FIG. 35(c)]), and exposing the first metal interconnects 601[/651] within the contact holes 611[/661].” (Ex. 1001, 29:13–20, 31:19–26, Figs. 32(c), 35(c); Ex. 1002, ¶¶119–20.) Examples of step l) from the ’696 patent are shown below with highlights. (Ex. 1001, 24:7–13, 29:13–20, Figs. 23(c), 32(c); Ex. 1002, ¶¶116–21.)

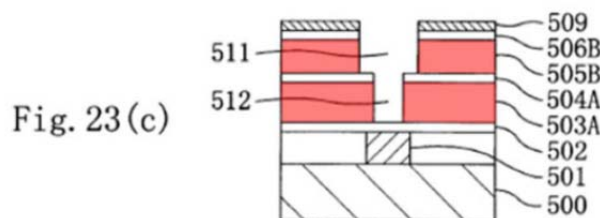


Fig. 23(c)

Fifth Embodiment

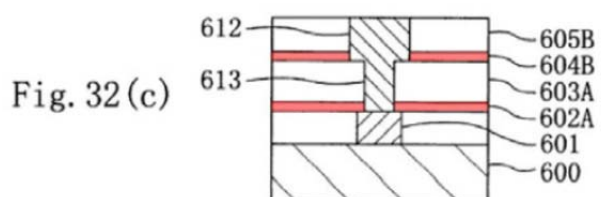


Fig. 32(c)

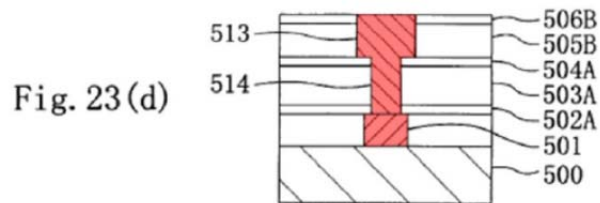
Sixth Embodiment

13. step m) of Claim 10

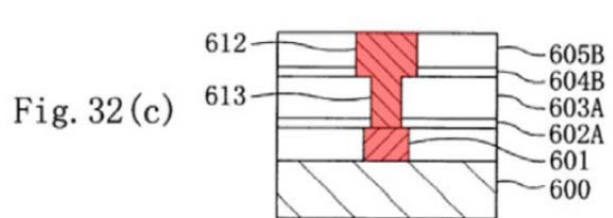
Step m) of claim 10 recites “filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects [513, 612] and contacts [514, 613] connecting the lower- and upper-level metal interconnects together.”

In the fifth embodiment, “a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 512[/562] and the wiring grooves 511[/561].” (Ex. 1001, 24:22–24, 26:38–41, Figs. 23(c), 26(c).) “As a result, second metal interconnects 513[/563] and contacts 514[/564], connecting the first and second metal interconnects 501[/551] and 513[/563] together, are formed.” (*Id.*, 24:33–35, 26:44–47, Figs. 23(d), 26(d); Ex. 1002, ¶¶123–24.) In the sixth embodiment, “a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 611[/661] and the wiring grooves 610[/660].” (Ex. 1001, 29:24–26, 31:30–32, Figs. 32(c), 35(c).) “As a result, second metal interconnects 612[/662] and contacts 613[/663], connecting the first and second metal interconnects 601[/651] and 612[/662]

together, are formed.” (*Id.*, 29:35–39, 31:41–44; Ex. 1002, ¶¶125–26.) Examples of step m) from the ’696 patent are shown below with highlights. (Ex. 1001, 24:22–35, 29:24–39, Fig. 32(c); Ex. 1002, ¶¶122–27.)



Fifth Embodiment



Sixth Embodiment

14. Dependent Claims 11 and 12

Claims 11 depends from claim 10 and further recites that “at least one of the first and third insulating films is mainly composed of an organic component.” (*See* Ex. 1001, 22:52–23:24, 24:60–25:11, 28:1–36, 30:1–16, Figs. 21(a), 24(a), 30(a), 33(a); Ex. 1002, ¶¶128–33.)

Claim 12 depends from claim 10 and further recites “wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.” (*See* Ex. 1001, 23:40–42, 25:26–65, 26:12–60, 28:49–51, 30:52–56, 31:49–32:6, Figs. 22(b), 25(b), 31(b), 34(b), 27(b), 36, 37(a); Ex. 1002, ¶¶134–39.)

B. Examination of the ’696 Patent

The application for the ’696 patent was filed March 23, 1999, and claims foreign priority to Japanese Patent Application No. 10-079371, filed March 26, 1998.

The original application for the ’696 patent included 15 claims. (Ex. 1012, 150–58.) The Examiner issued a first-action Notice of Allowability, accompanied by a statement of reasons for

allowance, stating simply, “Prior art lacks the steps of forming an interconnection structure as recited in the claims.” (*Id.*, 352–53.) The ’696 patent issued March 6, 2001, with all 15 original claims.

C. The Challenged Claims Are Not Entitled to the Benefit of Foreign Priority

The ’696 patent claims priority to Japanese Patent Application No. 10-079371 (Ex. 1013; Ex. 1014) (“the ’371 application”), filed March 26, 1998, but the challenged claims are not entitled to such priority. Patent Owner bears the burden of proving entitlement to the benefit of foreign priority, *Fiers v. Revel*, 984 F.2d 1164, 1169 (Fed. Cir. 1993); *Core Survival, Inc. v. S&S Precision, LLC*, PGR2015-00022, Paper 8, at 7–10 (Feb. 19, 2016), but Patent Owner cannot meet its burden here. Moreover, “genuine issue[s] of material fact . . . will be viewed in the light most favorable to the petitioner.” 37 C.F.R. §42.108.

As explained in section III.A, the challenged claims are directed to the fifth, modified fifth, sixth, and modified sixth embodiments of the ’696 patent (“new embodiments”). (Ex. 1002, ¶¶48–139.) The ’371 application, however, describes only the first through fourth embodiments of the ’696 patent. (*Compare* Ex. 1014, ¶¶0028–0115, Figs. 1(a)–20(c), *with* Ex. 1001, 10:22–22:44, Figs. 1(a)–20(c); *see also* Ex. 1002, ¶141.)

The ’371 application does not disclose the new embodiments, to which the challenged claims are directed. (*Compare generally* Ex. 1014, *with* Ex. 1001, 22:46–32:9, Figs. 21(a)–37(b); *see also* Ex. 1002, ¶¶140–42.) It also does not include Figures 21(a)–37(b) or claims 10–15, which relate to the new embodiments. (*See* Ex. 1014, [Claim 1]–[Claim 9], [Figure 1]–[Figure 20].) The descriptions, figures, and claims relevant to the subject matter challenged in this petition were added in Japanese Patent Application No. 11-075519 (Ex. 1015; Ex. 1016), filed March 9, 1999, and the application for the ’696 patent, filed March 23, 1999. (*See* Ex. 1016,

[Claim 9]–[Claim 15], ¶¶0124–0201; Ex. 1012, 125–49, 154–58.)

None of the embodiments described in the ’371 application disclose all of the steps recited in claims 10.¹ The challenged claims are not entitled to the benefit of foreign priority. *See, e.g., In re Ziegler*, 992 F.2d 1197, 1200 (Fed. Cir. 1993).

1. The first, second, and fourth embodiments of the ’371 application do not disclose step h) of claim 10

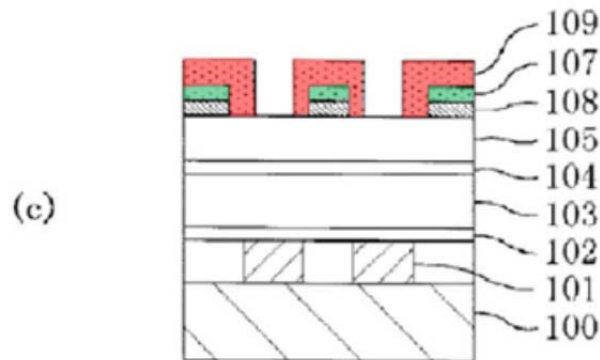
Step h) of claim 10 recites, “removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes.”

The first, second, and fourth embodiments do not teach “removing the first resist pattern” before “forming a second resist pattern.” Accordingly, none of these embodiments disclose claim 10. (*See* Ex. 1002, ¶¶144–46.)

The description of the first embodiment of the ’371 application states, “[T]he second resist pattern 109 is formed without removing the first resist pattern 107.” (Ex. 1014, ¶0043; *see also* ¶¶0050, 0056, Figs. 1(c), 5(a), 7(a).) The description of the second embodiment similarly states that “a second resist pattern 209, having openings for the formation of contact holes is formed by lithography on the second organic film 205 without removing the first resist pattern 207.” (*Id.*, ¶0068; *see also* Fig. 9(c).) The description of the fourth embodiment states that “a second resist pattern 409 having openings for the formation of contact holes is formed by lithography on the second low-dielectric-constant SOG film 405 without removing the first resist pattern 407.” (*Id.*, ¶0107; *see also* Fig. 18(c).)

¹ The examples contained herein are illustrative, not limiting. Again, Patent Owner must establish priority.

Figure 1(c) of the '371 patent application, shown below with highlights, demonstrates the formation of the second resist pattern (red) without removing the first resist pattern (green). (See also Ex. 1014, Figs. 5(a), 7(a), 9(c), 18(c).)



2. The third, variant of the third, and fourth embodiments do not disclose step i) of claim 10

Step i) of claim 10 recites “dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes.”

The third, variant of the third, and fourth embodiments of the '371 application do not disclose “dry-etching the fourth insulating film using . . . the mask pattern as a mask.” These description of the embodiments only disclose the second resist pattern as a mask during this step. (See Ex. 1002, ¶¶147–54.)

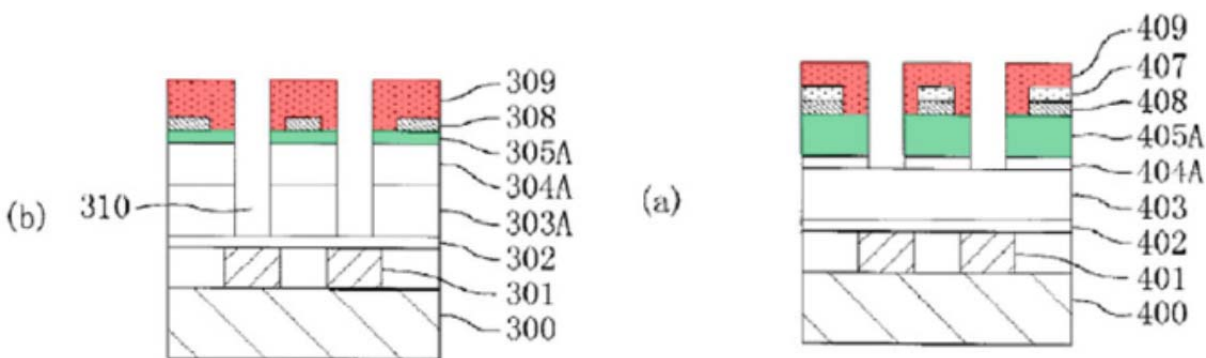
To map the third embodiment to claim 10, the fourth insulating film must be layer 305, as it is the fourth of only five layers over the lower level interconnects (301). But the third embodiment of the '371 application states, “[T]he second organic constituent-incorporated silicon dioxide film 305, the low-dielectric-constant SOG film 304 and the first organic constituent-incorporated silicon dioxide film 303 are sequentially dry-etched using the second resist pattern 309 as a mask.” (*Id.*, ¶0079; see also, Fig. 13(b).) Pattern 308 is not disclosed as a

mask for this step. (Ex. 1002, ¶¶148–49.)

To map the variant of the third embodiment to claim 10, the fourth insulating film must be layer 355, as it is the fourth of only five layers over the lower level interconnects (351). But the variant of the third embodiment states, “[T]he second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask.” (*Id.*, ¶0093; *see also* Fig. 16(b).) Pattern 358 is not disclosed as a mask for this etch step. (Ex. 1002, ¶¶150–51.)

To map the fourth embodiment to claim 10, the fourth insulating film must be layer 405, as it is the fourth of only five layers over the lower level interconnects (401). But the fourth embodiment states, “[T]he second low-dielectric-constant SOG film 405 and the organic constituent-incorporated silicon dioxide film 404 are sequentially dry-etched using the second resist pattern 409 as a mask.” (*Id.*, ¶0107; *see also* Fig. 19(a).) Pattern 408 is not disclosed as a mask for this etch step. (Ex. 1002, ¶¶152–53.)

Figures 13(b) and 19(a) of the ’371 patent application illustrate this point and are shown below on the left and right, respectively, with highlights. (*See also id.*, Fig. 16(b).)



3. The third, variant of the third, and fourth embodiments do not disclose step j) of claim 10

Step j) of claim 10 recites, “dry-etching the third insulating film using the patterned

fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

The third, variant of the third, and fourth embodiments of the ’371 application do not disclose “dry-etching the third insulating film using the patterned fourth insulating film as a mask.” These embodiments disclose using the second resist pattern as a mask when etching the third insulating film. (*See* Ex. 1002, ¶¶155–57.)

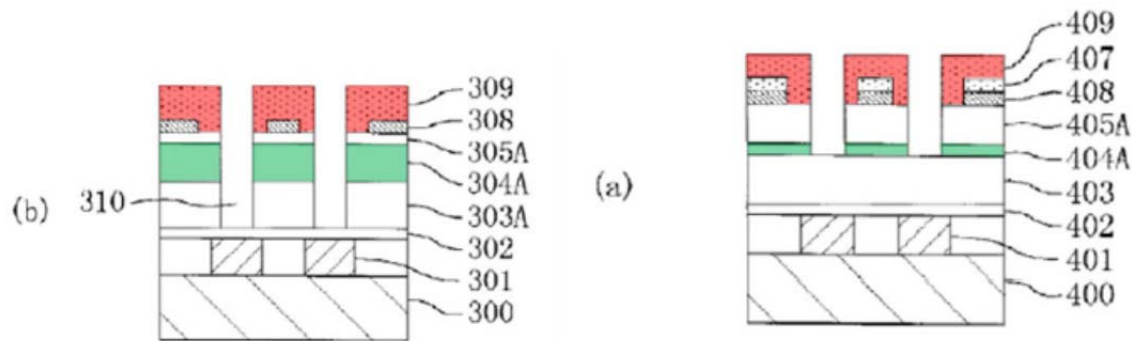
To map the third embodiment to claim 10, the third insulating film must be layer 304, because it is the third of only five layers over the lower level interconnects (301). For the third embodiment, the ’371 application states, “[T]he second organic constituent-incorporated silicon dioxide film 305, the low-dielectric-constant SOG film 304 and the first organic constituent-incorporated silicon dioxide film 303 are sequentially dry-etched using the second resist pattern 309 as a mask.” (*Id.*, ¶0079; *see also*, Fig. 13(b).) The patterned fourth insulating film (layer 305) is not disclosed as a mask during this etch step. (Ex. 1002, ¶157.)

To map the variant of the third embodiment to claim 10, the third insulating film must be layer 354, as it is the third of only five layers over the lower level interconnects (351). But the variant of the third embodiment states, “[T]he second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask.” (*Id.*, ¶0093; *see also* Fig. 16(b).) The patterned fourth insulating film (layer 355) is not disclosed as a mask during this etch step. (Ex. 1002, ¶157.)

To map the fourth embodiment to claim 10, the third insulating film must be layer 404, as it is the third of only five layers over the lower level interconnects (401). But the fourth embodiment states, “[T]he second low-dielectric-constant SOG film 405 and the organic constituent-incorporated silicon dioxide film 404 are sequentially dry-etched using the second

resist pattern 409 as a mask.” (*Id.*, ¶0107; *see also* Fig. 19(a).) The patterned fourth insulating film (layer 405) is not disclosed as a mask during this etch step. (Ex. 1002, ¶156.)

Figures 13(b) and 19(a) of the ’371 patent application illustrate this point and are shown below on the left and right, respectively, with highlights. (*See also id.*, Fig. 16(b).)



4. No embodiments of the ’371 application disclose step l) of claim 10

Step l) of claim 10 recites, “dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively.”

None of the embodiments of the ’371 application disclose this step. (*See* Ex. 1002, ¶¶158–65.) In the first embodiment, the first insulating film (layer 102) is etched using the patterned third insulating film (patterned layer 104A) as a mask. (Ex. 1014, ¶0038, Fig. 3(a).) Similarly, in the second embodiment the first insulating film (layer 202) is etched using the patterned third insulating film (patterned layer 204A) as a mask. (*Id.*, ¶0071, Fig. 11(a).) In the third embodiment, the third insulating film (layer 304) is etched using second resist pattern 309 as a mask. (*Id.*, ¶0079, Fig. 13(b).) In the variant of the third embodiment, the third insulating film (layer 354) is etched using second resist pattern 359 as a mask. (*Id.*, ¶0093, Fig. 16(b).) In the fourth embodiment, the first insulating film (layer 402) is etched using the patterned third

insulating film (patterned layer 404A) as a mask. (*Id.*, ¶0110, Fig. 20(a).) In all of these embodiments, the first and third insulating films are etched in different steps. (*Id.*, ¶¶0036, 0038, 0070, 0071, 0079, 0082, 0093, 0097, 0107, 110, Figs. 2(b), 3(a), 10(b), 11(a), 13(b), 14(a), 16(b), 17(a), 19(a), 20(a).)

IV. Statement of Precise Relief Requested for Each Claim Challenged

A. Claims for Which Review is Requested

Petitioner requests review under 35 U.S.C. §311 of claims 10–12 and the cancellation of those claims as unpatentable.

B. Statutory Grounds of Challenge

Claims 10–12 are unpatentable under 35 U.S.C. §103.

C. Level of Ordinary Skill

A person of ordinary skill in the art (“POSITA”) would possess (1) the equivalent of a Master of Science degree from an accredited institution in electrical engineering, materials science, physics, or the equivalent; (2) a working knowledge of semiconductor processing technologies for integrated circuits; and (3) at least two years of experience in related semiconductor processing analysis, design, and development. (Ex. 1002, ¶167.) Additional graduate education could substitute for professional experience, and significant work experience could substitute for formal education. (*Id.*)

D. Claim Construction

Claim terms are given their ordinary and accustomed meaning as understood by a POSITA. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). A claim in an unexpired patent in post-grant review receives the “broadest reasonable construction in light of the specification of the patent in which it appears.” 37 C.F.R. §42.100(b). The broadest reasonable construction should apply to all claims of the ’696 patent.

V. Claims 10–12 of the '696 Patent Are Unpatentable Over the Prior Art

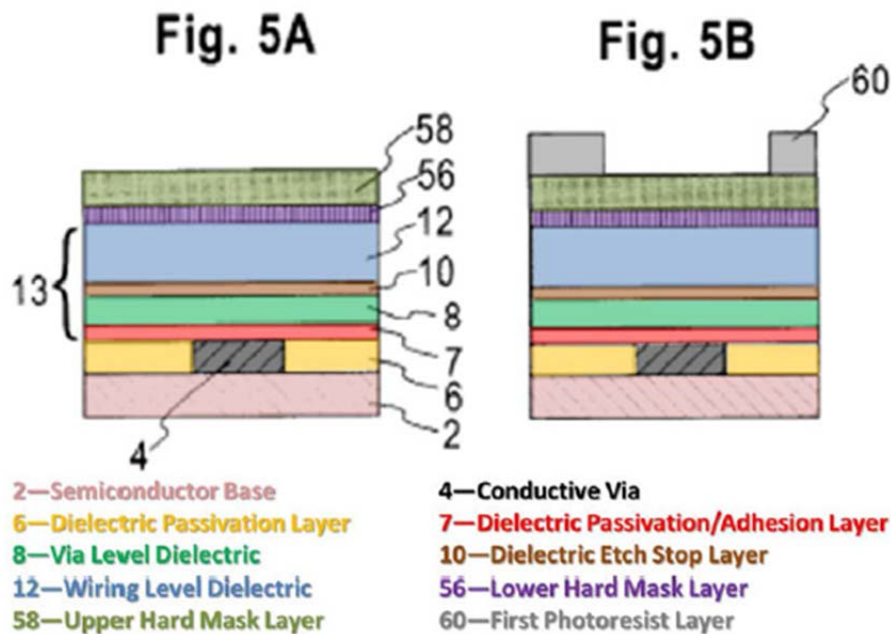
A. Disclosures of the Prior Art

1. *Grill* (U.S. Patent No. 6,140,226)

Grill was filed July 30, 1998, and claims priority to U.S. Provisional Patent Application No. 60/071,628 (Ex. 1017, “'628 application”), filed January 16, 1998. Due to its filing date, *Grill* is prior art to the '696 patent under §102(e). Because of the '628 application, *Grill* is prior art under §102(e) even if the challenged claims were entitled to the benefit of foreign priority.² *Grill* was neither considered nor cited during prosecution.

² Petitioner need not do anything more at this stage to meet its initial burden of production to demonstrate *Grill* is prior art under §102(e). See *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1379–80 (Fed. Cir. 2015); *Ariosa Diagnostics, Inc. v. Illumina, Inc.*, IPR2014-01093, Paper 69 at 10, 12–13 (Jan. 7, 2016). IPB bears the burden of production to show the challenged claims are entitled to a priority date before July 30, 1998. *Dynamic Drinkware*, 800 F.3d. at 1380; IPR2014-01093, Paper 69 at 14. If IPB could do so, the burden of production shifts to Petitioner, *Dynamic Drinkware*, 800 F.3d. at 1380; IPR2014-01093, Paper 69 at 14–15, who would be permitted to establish that *Grill* antedates the earliest priority date of the '696 patent because of the '628 application. Although Petitioner need not show *Grill* is supported by the '628 application unless Patent Owner shows the challenged claims antedate *Grill*, Dr. Smith provides a provisional claim chart in his declaration, showing support for *Grill*'s claim 28 in the '628 application. (See also Ex. 1002, ¶¶5, 179.) The disclosures of the '628 application that demonstrate the unpatentability of the challenged claims are at pages 10–14, 16, and 17 and Figures 5A–5H, 1J–1L of Exhibit 1017. (Ex. 1002, ¶179.)

Grill discloses “methods to fabricat[e] multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels.” (Ex. 1005, Abstract; *see also* 7:16–30.) This Petition focuses on the embodiment of *Grill* described at 4:60-5:8 and 7:16–8:8 and minor variations. The structure of Fig. 5A is formed first, followed by patterning a first photoresist layer [60], as Figure 5B shows. (*Id.*, 7:30–44.) This photolithography defines the shape of trench. (Ex. 1002, ¶171.)



An etch transfers the photoresist pattern [60] into the upper hard mask layer [58], as Figure 5C shows. (Ex. 1005, 7:45–50.) The first layer of photoresist [60] is removed, and a second layer of photoresist [62] is patterned to define what will become the via level of the interconnection, as Figure 5D shows. (*Id.*, 7:51–55; Ex. 1002, ¶172.)

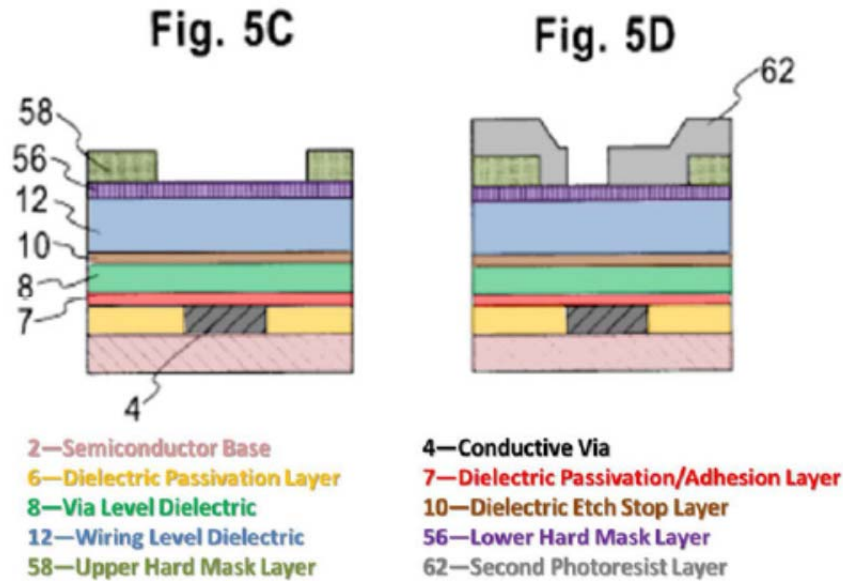
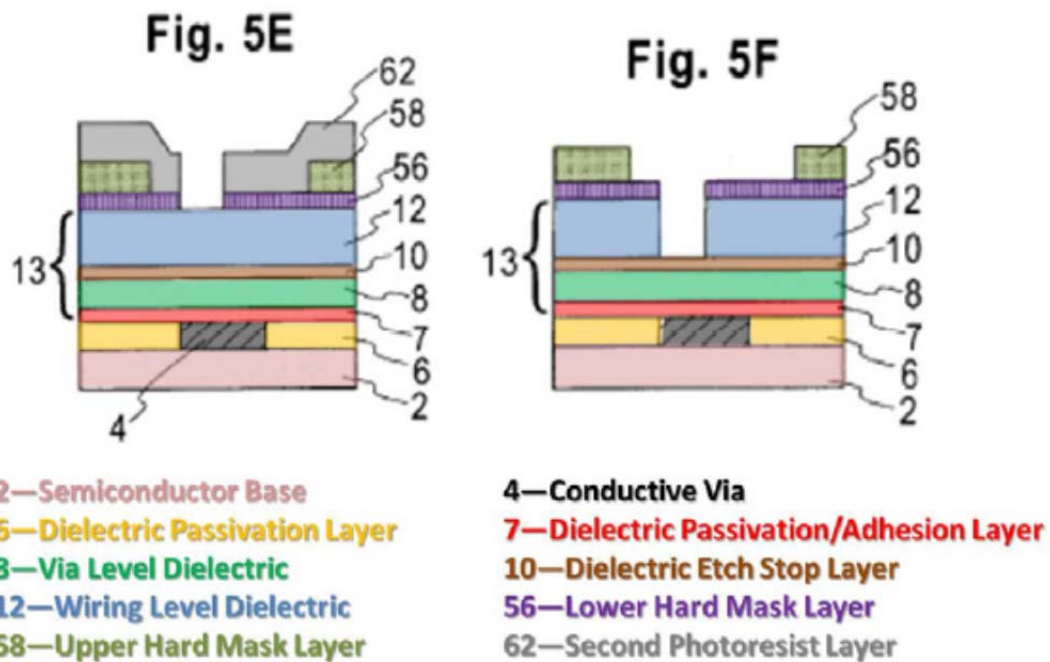


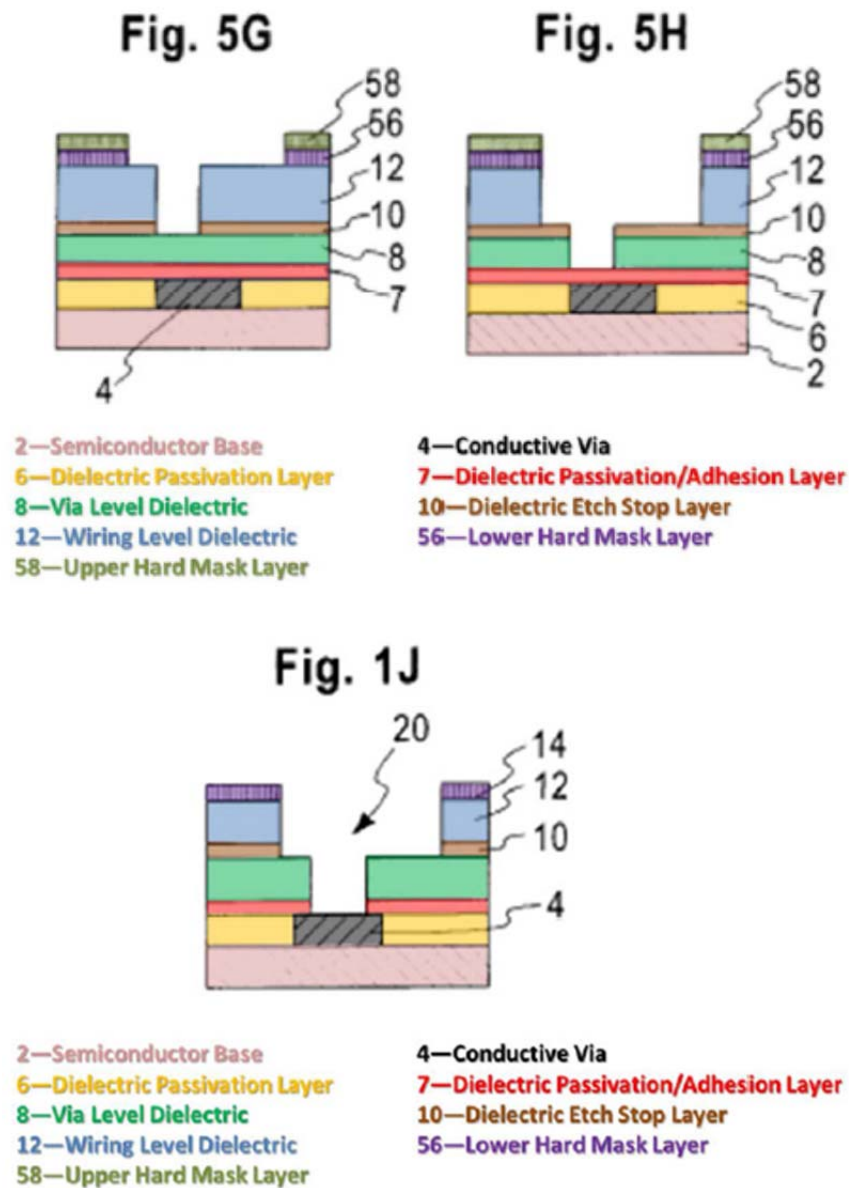
Figure 5E shows the next step of etching to transfer the photoresist pattern [62] into the lower hard mask layer [56]. (Ex. 1005, 7:57–61.) This pattern is transferred into layer [12] by another etch, which also removes the second photoresist layer [62] (as in Figure 5F).

(*Id.*, 7:62-66; Ex. 1002, ¶173.)



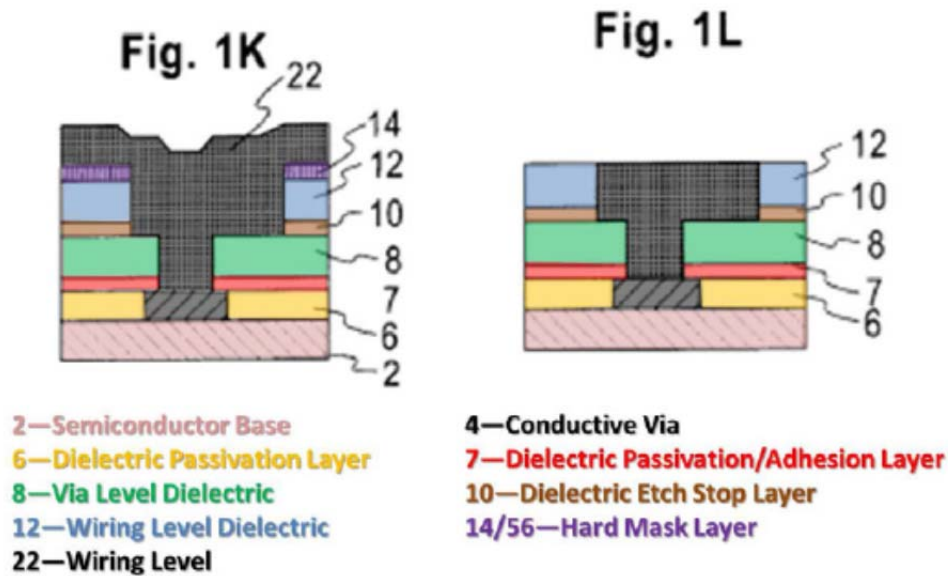
Another etch removes the exposed portions of the lower hard mask [56] and etch stop

[10], as Figure 5G shows. (Ex. 1005, 7:67–8:2.) A further etch removes the exposed portions of dielectric layers 8 and 12, as FIG. 5H shows. (*Id.*, 8:2–5.) A final etch removes the exposed portions of optional dielectric layer 7, and also removes the exposed portions of etch stop [10] to form the dual-relief cavity of Fig. 1J. (*Id.*, 4:61–64, 8:5–8; Ex. 1002, ¶174.)

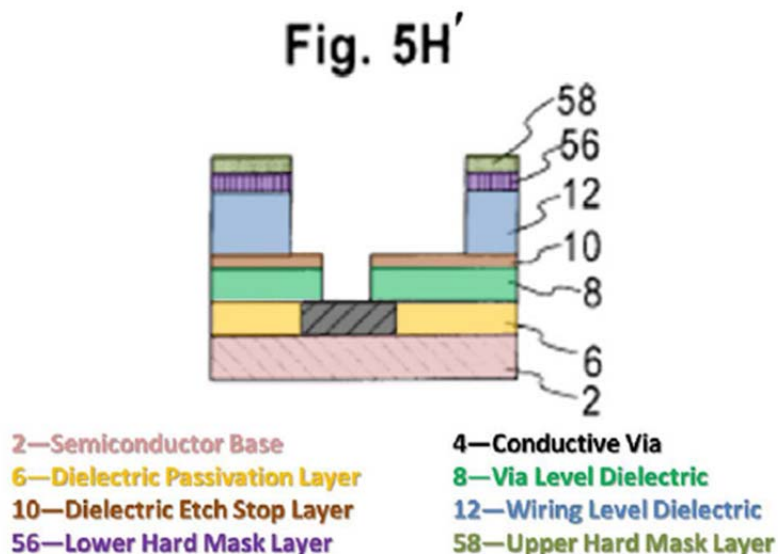


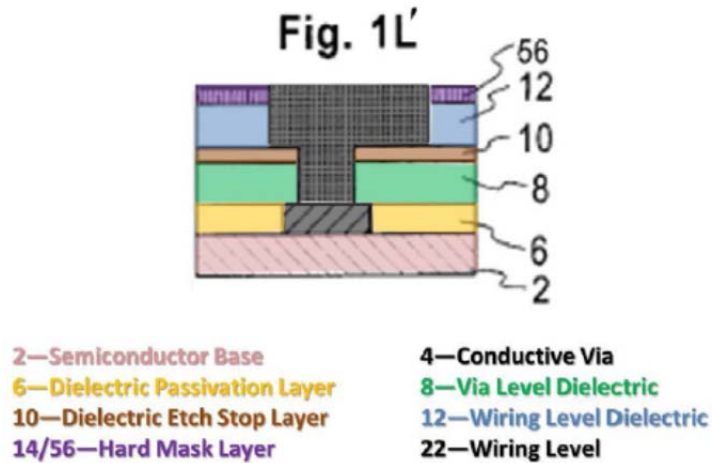
The cavity is filled with conductive material [22], as Figure 1K shows, and planarized by a chemical-mechanical polishing (CMP) process, as Figure 1L shows. (Ex. 1005, 4:64–5:8, 8:5–8.) Hard mask 14, which is analogous to lower hard mask 56 and upper hard mask 58

(compare Ex. 1001, 4:24–29, Figs., 1C, 1I, with Ex. 1005, 7:30–42, Figs. 5A, 5H), may remain in the final structure. (Ex. 1005, 5:5–8; Ex. 1002, ¶175.)



Although this is the only illustration of the described embodiment, other variations are disclosed. For example, *Grill* teaches that passivation/adhesion layer [7] is optional, and so is etch stop [10]. (*Id.*, 4:1–5, 4:61–63.) Modified Figures 5H' and 1L' below illustrate how a POSITA would understand the alternative embodiment in which optional layer 7 is absent. (Ex. 1002, ¶¶176–78.)

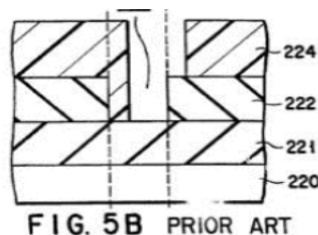
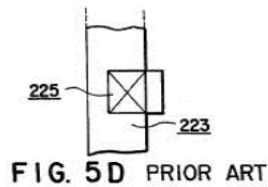




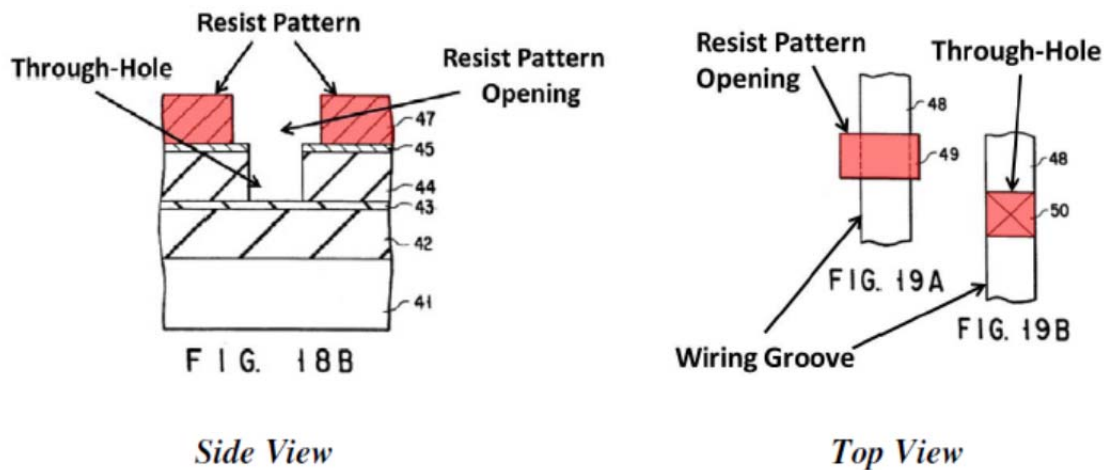
2. *Aoyama* (U.S. Patent No. 5,592,024)

Aoyama (Ex. 1018) teaches a damascene process in which the opening in the via resist pattern is wider than the wiring groove. (Ex. 1018, 15:48–51, 16:3–5, Figs. 18A–18C, 19A–19B.) *Aoyama* was filed October 28, 1994, and issued January 7, 1997, so it qualifies as prior art under §102(b). *Aoyama* was neither considered nor cited during prosecution.

Aoyama explains a problem in which misalignment of the photomask when forming the through-hole (via) can cause it to be smaller than desired and the wiring groove to be wider than desired at the through-hole. (*Id.*, 3:18–21, 3:29–32, Figs. 5B, 5D (shown below).) This increases contact resistance, degrades reliability, and hinders increased integration density. (*Id.*, 3:33–38, 6:7–14.)

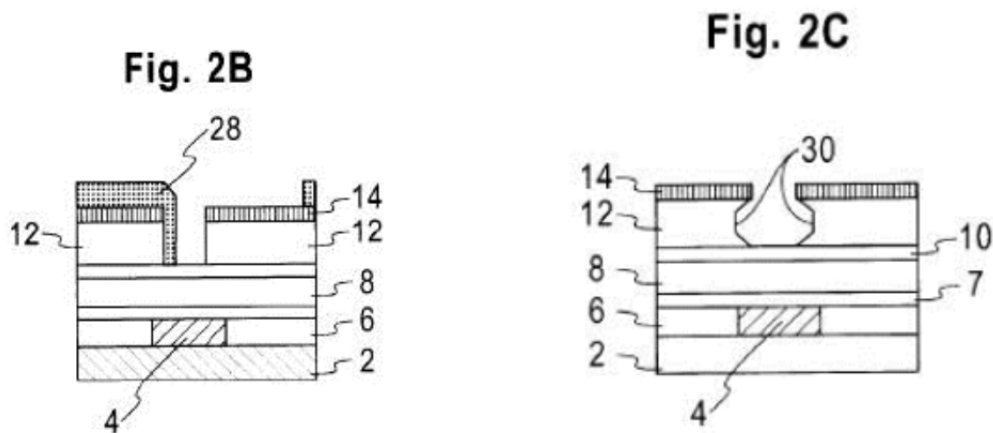


Aoyama resolves this problem using a resist pattern with a through-hole wider than the wiring groove. (*Id.*, 16:3–5, Figs. 18B, 19A (each below with annotations and highlights).) Even when misaligned, a through-hole having the same width as the wiring groove is formed. (*Id.*, 16:14–16, Fig. 19B (below with annotations and highlights).)



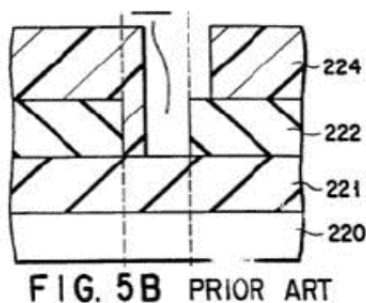
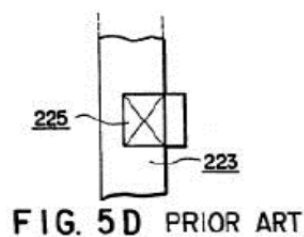
3. A POSITA would have combined teachings of *Grill* and *Aoyama*

A POSITA would have found it obvious to combine certain teachings of *Grill* and *Aoyama*. (Ex. 1002, ¶¶183–91.) One problem *Grill* addresses is the problem of “lithographic rework” because of photolithographic misalignment occurs between via and wiring patterns. (Ex. 1005, 2:26–38.) Organic and other low-k materials may have similar etch characteristics to photoresist, so stripping a misaligned photoresist pattern for rework may not only remove the photoresist but also damage the underlying dielectric. (*Id.*, 2:26–32.) As Figures 2B and 2C of *Grill* show below, stripping misaligned photoresist 28 can damage inter-layer dielectric 12 and make it difficult to control the size of the via pattern. (*Id.*, 5:13–33.)

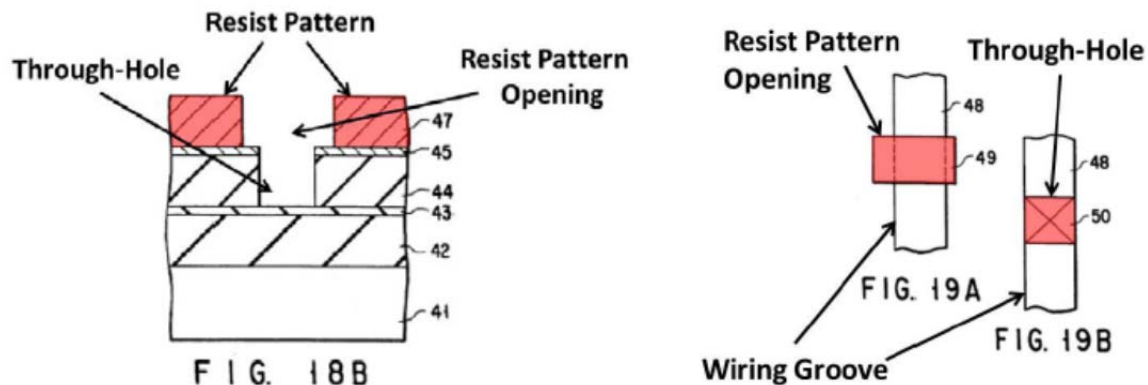


Grill discloses a solution using two hard masks on top of the wiring-level dielectric. (*Id.*, 2:64–3:6, Fig. 5A.) Lithographic alignment for both via and wiring levels is completed and transferred into thin films on the surface of the device before the underlying dielectrics are ever exposed. (*Id.*, 2:64–3:1, Figs. 5A–5E.)

Aoyama solves a related problem. *Aoyama* explains that misalignment of the photomask during via formation can cause the via dimensions to be too small and the wiring dimensions to be too large. (Ex. 1018, 3:18–21, 3:29–32, Figs. 5B, 5D (shown below).) This increases contact resistance, degrades reliability, and hinders higher integration densities. (*Id.*, 3:33–38, 6:7–14.)



To solve this problem, *Aoyama* discloses a resist pattern with a via opening wider than the wiring groove. (*Id.*, 16:3–5, Figs. 18B, 19A (below with highlights).) This added width increases misalignment tolerance since the width of the via is defined by the wiring groove. (*Id.*, 16:14–16.) A via having the same width as the wiring groove is formed even when misaligned. (*Id.*, 16:14–16, Fig. 19B (below with highlights and annotations).)



Aoyama does not eliminate the possibility of misaligned photomasks. (Ex. 1002, ¶187.) A wider via opening in the photomask increases misalignment tolerance but does not guarantee alignment. (*Id.*) The misalignment in Figure 5D above is possible even with the wider pattern in Figure 19A. (*Id.*)

A POSITA would have appreciated that *Grill*'s and *Aoyama*'s solutions complement one another. (Ex. 1002, ¶188.) When misalignment occurs, *Grill*'s structure permits rework without damaging the underlying dielectrics. (Ex. 1005, 2:26–38; Ex. 1002, ¶188.) *Aoyama*'s wider via pattern reduces instances of misalignment, preventing the time-consuming, inefficient, and costly process of photolithographic rework. (Ex. 1002, ¶188.)

A POSITA would have further found it obvious to combine *Grill*'s two hard masks with *Aoyama*'s widened through-hole pattern without modifying the *Grill* process. (Ex. 1002, ¶189.) Nothing about the width of the via pattern in *Aoyama* affects the dual-hard mask structure of

Grill, and nothing about the dual-hard mask structure of *Grill* affects the width of the via pattern in *Aoyama*. (*Id.*)

A POSITA would have understood that the combination of *Aoyama* and *Grill* predictably reduces instances of misalignment and permits lithographic rework when misalignment occurs. (Ex. 1002, ¶190.) This combination therefore avoids increased contact resistance, degradation of reliability, and damage to the inter-layer dielectrics from misalignment, and facilitates higher integration density. (Ex. 1005, 2:26–38, 2:64–3:6, 5:13–33; Ex. 1018, 3:33–38, 6:7–14; Ex. 1002, ¶190.)

The combination of *Grill* and *Aoyama* is merely a combination of familiar elements according to known methods to yield predictable results; use of known techniques to improve similar devices, methods, or products in the same way; and application of known techniques to known devices, methods, or products ready for improvement to yield predictable results. (*See, e.g.*, Ex. 1005, 2:26–38, 2:64–3:6, 5:13–33; Ex. 1018, 3:33–38, 6:7–14; Ex. 1002, ¶191.)

B. *Grill* Renders Claims 10 and 11 Obvious

The arguments that follow in this section are based on *Grill*'s disclosure that dielectric passivation/adhesion layer [7] is optional. (Ex. 1005, 4:1–5, 4:61–63.) A POSITA would have understood that the expressly disclosed embodiment of *Grill* at 4:60–5:8 and 7:16–8:8, without optional layer [7], renders claims 10 and 11 obvious.³ *See, e.g., Upsher-Smith Labs., Inc. v. PamLab L.L.C.*, 412 F.3d 1319, 1322 (Fed. Cir. 2005) (“‘[O]ptional inclusion’ of antioxidants teaches vitamin supplement compositions that both do and do not contain antioxidants.”). In

³ Because this ground of unpatentability relies on what a POSITA would have understood about a variant *Grill* suggests but does not describe in detail (embodiment without optional layer [7]), Petitioner presents this ground as a single-reference obviousness argument.

fact, *Grill* is virtually identical to the fifth embodiment of the '696 patent.

1. Claim 10 is obvious in view of *Grill*

a. [10.1] *Grill* discloses the preamble of claim 10

The preamble of claim 10 recites, “A method for forming an interconnection structure.” *Grill*, titled “Dual Damascene Processing for Semiconductor Chip Interconnects,” discloses “methods to fabricat[e] multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels.” (Ex. 1005, Abstract; *see also* 1:12–15, 7:16–30, Fig. 1L; *see also* Ex. 1001, Abstract, Fig. 3(c).)

b. [10.2] *Grill* discloses “forming a first insulating film”

Claim 10 recites “forming a first insulating film over lower-level metal interconnects.” *Grill* discloses “via level dielectric 8,” which “might be carbon-based materials such as DLC or fluorinated DLC (FDLC), SiCO or SiCOH compounds, or organic or inorganic polymer dielectrics.” (Ex. 1005, 4:1–13.) A POSITA would have understood that via level dielectric [8] is an insulating film. (Ex. 1002, ¶196.) Further, *Grill* discloses a “conductive via 4,” which is “formed in the interlevel dielectric to provide interlevel contacts between the wiring traces.” (Ex. 1005, 1:25–27, 3:60–67, Fig. 5A.)

A POSITA would have understood that via level dielectric [8] is over the conductive via [4]. (Ex. 1002, ¶197.) *Grill*’s Figure 5A and Figure 21(a) from the fifth embodiment of the '696 patent appear below. (*See also* Ex. 1001, 22:57–60; Ex. 1002, ¶¶195–98.)

Fig. 5A

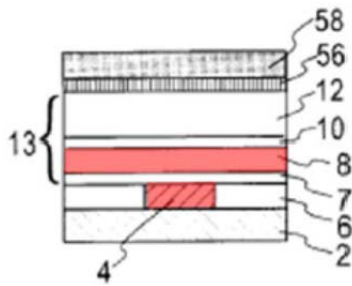
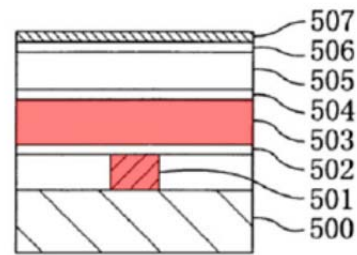


Fig. 21 (a)



c. [10.3] *Grill* discloses “forming a second insulating film”

Claim 10 recites “forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film.” *Grill* discloses “dielectric etch stop layer 10,” which “might be a silicon-containing material such as SiO₂, Si₃N₄, SiO_xN_y, SiCOH compounds, silicon-containing DLC (SiDLC), etc.” (Ex. 1005, 4:1–13, Fig. 5A.) Additionally, *Grill* teaches that via level dielectric [8] “might be carbon-based materials such as DLC or fluorinated DLC (FDLC), SiCO or SiCOH compounds, or organic or inorganic polymer dielectrics.” (*Id.*) Based on this disclosure, a POSITA would have understood that the disclosed etch stop [10] is an insulating film with a composition that differs from via level dielectric [8]. (Ex. 1002, ¶¶200–01.)

A POSITA would have understood that etch stop [10] is over via level dielectric [8]. (Ex. 1002, ¶201.) *Grill*’s Figure 5A and Figure 21(a) from the fifth embodiment of the ’696 patent appear below. (See Ex. 1001, 22:60–62; Ex. 1002, ¶¶199–202.)

Fig. 5A

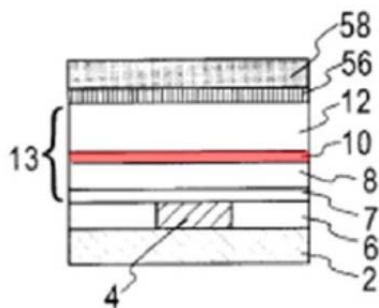
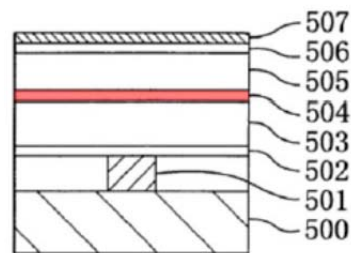


Fig. 21(a)



d. [10.4] *Grill* discloses “forming a third insulating film”

Claim 10 recites “forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film.” *Grill* discloses “wiring level dielectric 12,” which “might be carbon-based materials such as DLC or fluorinated DLC (FDLC), SiCO or SiCOH compounds, or organic or inorganic polymer dielectrics.” (Ex. 1005, 4:1–13, Fig. 5A.) *Grill* teaches that etch stop [10] “might be a silicon-containing material such as SiO₂, Si₃N₄, SiO_xN_y, SiCOH compounds, silicon-containing DLC (SiDLC), etc.” (*Id.*) Based on this disclosure, a POSITA would have understood that the disclosed wiring level dielectric [12] is an insulating film with a composition that differs from etch stop [10]. (Ex. 1002, ¶¶204-05.)

A POSITA would have understood the wiring level dielectric [12] is over etch stop [10]. (Ex. 1002, ¶205.) *Grill*’s Figure 5A and Figure 21(a) from the fifth embodiment of the ’696 patent appear below. (*See also* Ex. 1001, 22:62–65; Ex. 1002, ¶¶203–06.)

Fig. 5A

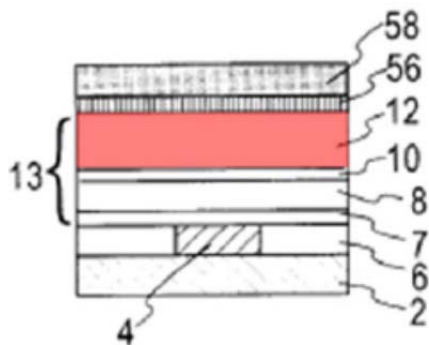
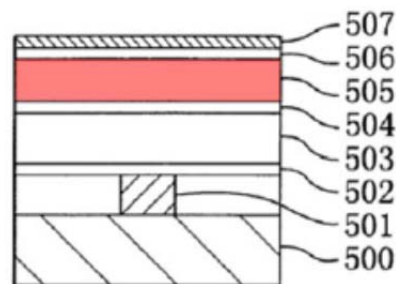


Fig. 21 (a)



e. [10.5] *Grill* discloses “forming a fourth insulating film”

Claim 10 recites “forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film.” *Grill* discloses “lower hard mask layer 56,” which is “preferably formed from different materials which have different etch properties from . . . the dielectric underlayer[] 12.” (Ex. 1005, 7:31–35.) “[S]uitable hard mask materials may include SiO₂-based materials, other oxides, nitrides other than Si₃N₄, carbon-based dielectrics, SiC-based dielectrics, polycrystalline silicon, amorphous hydrogenated silicon, and metals.” (*Id.*, 7:38–42.) *Grill* teaches that “wiring level dielectric 12 . . . might be carbon-based materials such as DLC or fluorinated DLC (FDLC), SiCO or SiCOH compounds, or organic or inorganic polymer dielectrics.” (*Id.*, 4:1–13.) A POSITA would have understood that the disclosed lower hard mask layer [56] is an insulating film with a composition that differs from the wiring level dielectric [12]. (Ex. 1002, ¶208.)

A POSITA also would have understood that the lower hard mask layer [56] is over the etch wiring level dielectric [12]. (Ex. 1002, ¶209.) *Grill*’s Figure 5A and Figure 21(a) from the fifth embodiment of the ’696 patent appear below. (*See also* Ex. 1001, 22:66–23:1; Ex. 1002, ¶¶207–10.)

Fig. 5A

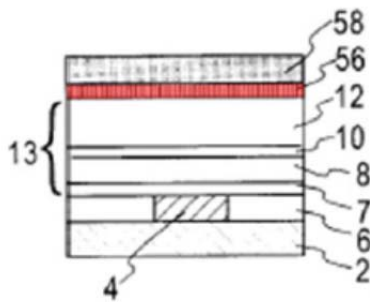
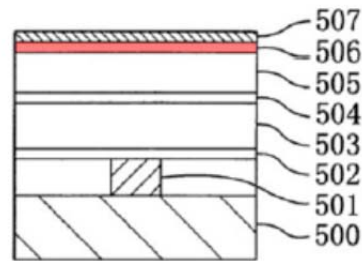


Fig. 21(a)



f. [10.6] *Grill* discloses “forming a thin film”

Claim 10 recites “forming a thin film over the fourth insulating film.” *Grill* discloses “upper hard mask layer 58.” (Ex. 1005, 7:31–35.) *Grill* explains that the upper hard mask layer “might be formed from a 40 nm thickness.” (*Id.*, 8:29–31.) A POSITA would have understood that the upper hard mask layer [58] is a thin film over the lower hard mask layer [56]. (Ex. 1002, ¶¶212–13.) *Grill*’s Figure 5C and Figure 21(a) from the fifth embodiment of the ’696 patent appear below. (See also Ex. 1001, 23:1–3; Ex. 1002, ¶¶211–14.)

Fig. 5A

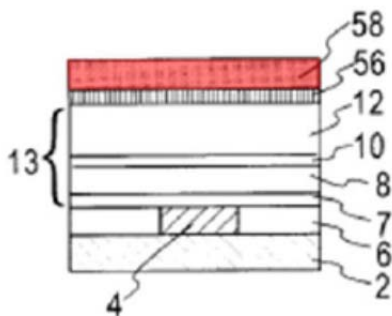
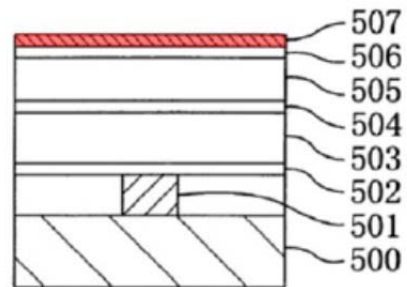


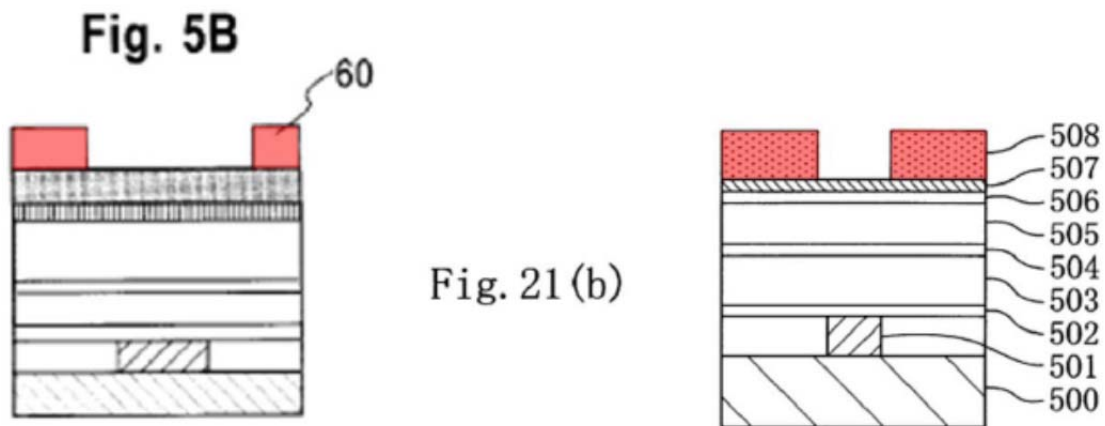
Fig. 21(a)



g. [10.7] *Grill* discloses “forming a first resist pattern”

Claim 10 recites “forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves.” *Grill* states that “[a] first resist layer 60, patterned with a first (wiring level) pattern, is formed on layer 58.” (Ex. 1005, 7:42–44.) A

POSITA would have understood that the first resist layer [60] is on the upper hard mask layer, [58] and its opening corresponds to a wiring groove. (Ex. 1002, ¶215.) *Grill*'s Figure 5B and Figure 21(b) from the fifth embodiment of the '696 patent appear below. (*See also* Ex. 1001, 23:25–27; Ex. 1002, ¶¶214–16.)



h. [10.8] *Grill* discloses “etching the thin film”

Claim 10 recites “etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves.” *Grill* states, “The pattern of resist layer 60 [the wiring level pattern] is transferred into upper hard mask layer 58 by an etching process.” (Ex. 1005, 7:42–47.) A POSITA would have understood that the resist layer [60] masks the upper hard mask [58] and that the width of the openings in upper hard mask [58] correspond to wiring grooves. (Ex. 1002, ¶218.) *Grill*'s Figure 5C and Figure 22(a) from the fifth embodiment of the '696 patent appear below to illustrate this. (*See also* Ex. 1001, 23:27–32, Fig. 21(c); Ex. 1002, ¶¶217–19.)

Fig. 5C

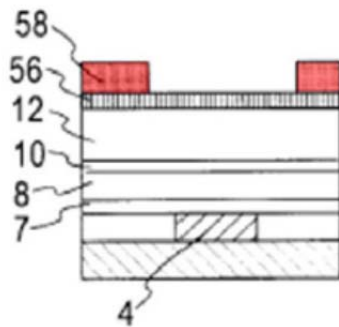
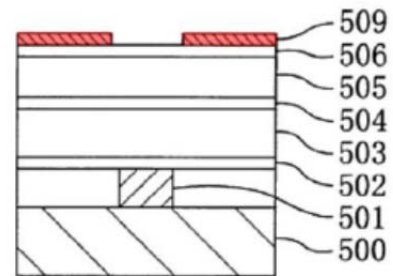


Fig. 22(a)



- i. **[10.9] Grill discloses “removing the first resist pattern and then forming a second resist pattern”**

Claim 10 recites “removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes.” *Grill* states, “Patterned resist layer 60 is then removed by a process such as ashing or wet chemical etching, and a second resist layer 62, patterned with a second (via level) pattern, is then formed on the structure.” (Ex. 1005, 7:51–55, Figs. 5B, 5C, 5D.) A POSITA would have understood that the second resist layer [62] is formed on both the lower hard mask layer [56] and the mask pattern [58]. (*Id.*) *Grill*’s Figure 5D and Figure 22(b) from the fifth embodiment of the ’696 patent appear below to illustrate this. (*See also* Ex. 1001, 23:33–42; Ex. 1002, ¶¶220–22.)

Fig. 5D

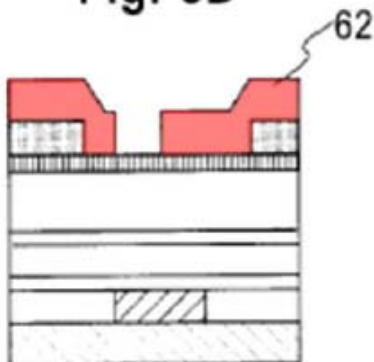
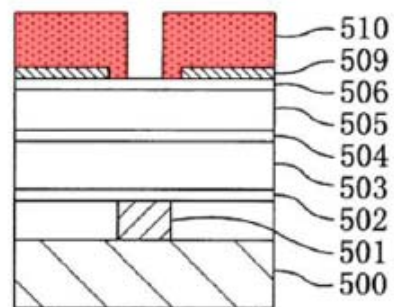


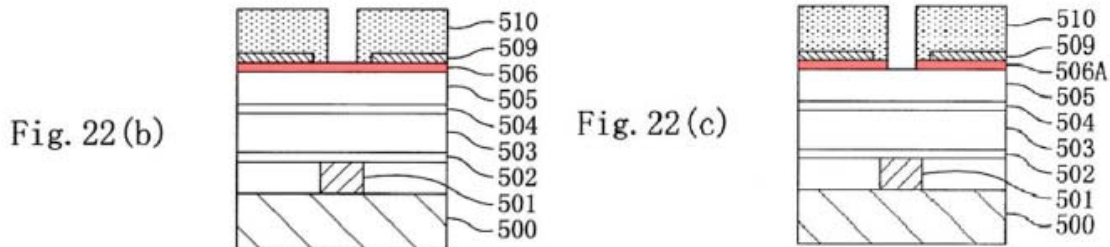
Fig. 22(b)



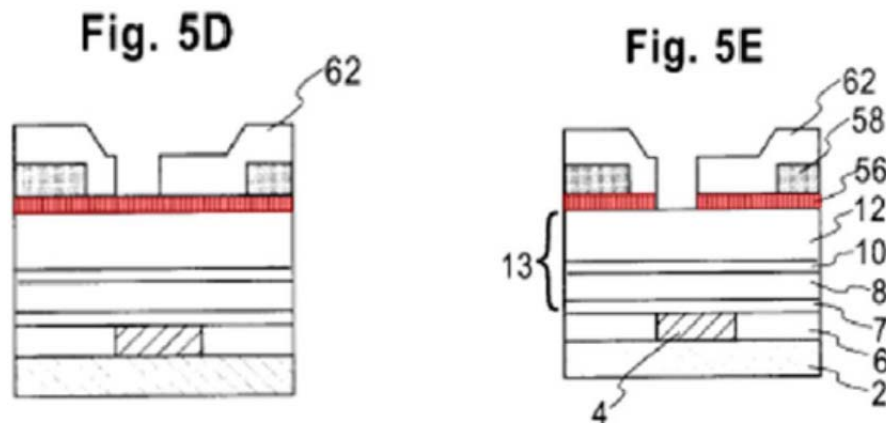
j. [10.10] Grill discloses “dry-etching the fourth insulating film”

Claim 10 recites “dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes.”

The '696 patent explains, “the second silicon dioxide film 506 is dry-etched using the second resist pattern 510 and the mask pattern 509 as a mask, thereby forming a patterned second silicon dioxide film 506A having openings for forming contact holes as shown in FIG. 22(c).” (Ex. 1001, 23:42–46.) Figures 22(b) and 22(c) of the '696 patent illustrate this below.



Grill discloses the same thing, as highlighted Figures 5D and 5E show below. (*Compare* Ex. 1001, 23:40–46, Figs. 22(b), 22(c), *with* Ex. 1005, 7:57–61, Figs. 5D, 5E.)



Grill states, “The pattern of resist layer 62 [i.e., the via level pattern] is then transferred into lower hard mask layer 56.” (Ex. 1005, 7:57–61, Fig. 5E.) As Figures 5D and 5E show above, and based on the description of the '696 patent, a POSITA would have understood that

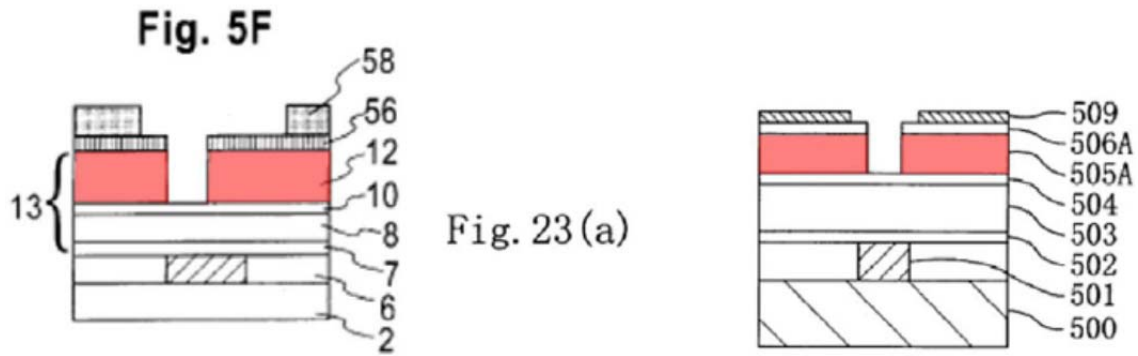
the resist layer [62] and the upper hard mask [58] mask lower hard mask [56] during etching in the manner described by the '696 patent. (Ex. 1002, ¶¶223–27.)

A POSITA would have further understood that the lower hard mask layer [56] has openings for forming contact holes because it contains the via level pattern of the second resist layer 62. (Ex. 1005, 7:51–55; Ex. 1002, ¶225.) Additionally, a POSITA would have understood that dry etching transfers the second resist pattern [62] into the lower hard mask layer [56]. (Ex. 1002, ¶226.) Layer 56 may be Si_3N_4 (Ex. 1005, 7:34–37), and the etch in Figures 5D and 5E is anisotropic to preserve the dimensions of the via level pattern (Ex. 1002, ¶226). A POSITA would have understood that anisotropic etches of Si_3N_4 are dry etches. (*Id.*)

k. [10.11] *Grill* discloses “dry-etching the third insulating film”

Claim 10 recites “dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.” *Grill* states, “The via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching.” (Ex. 1005, 7:62–63.) As Figure 5F shows below,⁴ a POSITA would have understood that the wiring level dielectric [12] has openings for forming contact holes. (Ex. 1002, ¶229.) Figure 23(a) from the fifth embodiment of the '696 patent also appears below. (*See also* Ex. 1001, 23:47–51; Ex. 1002, ¶¶228–30.)

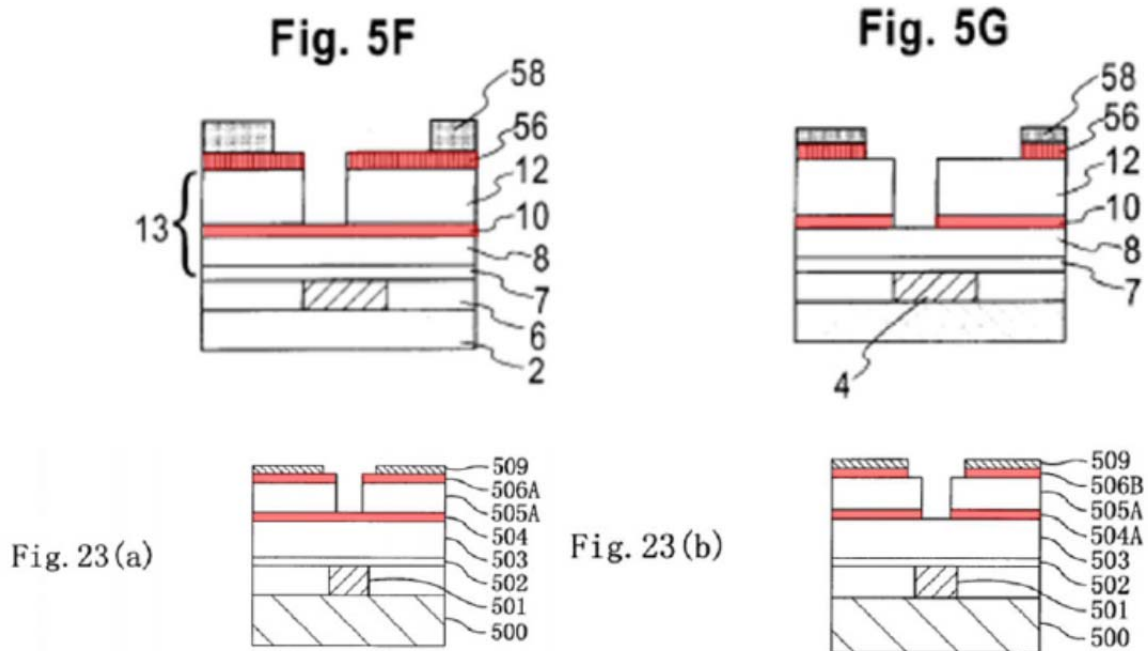
⁴ “Patterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12.” (Ex. 1005, 7:64–66; Ex. 1002, ¶229 & n.3.) A POSITA would have understood that lower hard mask [56] acts as a mask as second resist [62] is removed during the etching process. (Ex. 1002, ¶229.) The fifth, modified fifth, sixth, and modified sixth embodiments of the '696 patent teach the same. (Ex. 1001, 23:47–59, 25:66–26:14, 28:49–61, 30:58–31:6, Figs. 23(a), 26(a), 31(c), 34(c).)



1. [10.12] *Grill* discloses “dry-etching the patterned fourth insulating film and the second insulating film”

Claim 10 recites “dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes.” *Grill* states, “The etching conditions are then changed to removed [sic] exposed portions of lower hard mask layer 56 and optional etch stop 10.” (Ex. 1005, 7:67–8:2, Fig. 5G.) A POSITA would have understood that this is a dry etch for similar reasons explained in section V.B.1.j. (Ex. 1002, ¶233.)

As Figures 5F and 5G show below, a POSITA would have understood that upper hard mask [58] masks lower hard mask [56] during the etch, and wiring level dielectric [12] masks etch stop [10]. (Ex. 1002, ¶232.) The width of the hole in the lower hard mask [56] corresponds to the wiring groove, and the width of the hole in etch stop [10] corresponds to the width of the contact hole. (*Id.*) Figures 23(a) and 23(b) from the fifth embodiment of the ’696 patent show the same. (*See also* Ex. 1001, 23:66–24:6; Ex. 1002, ¶¶231–34.)



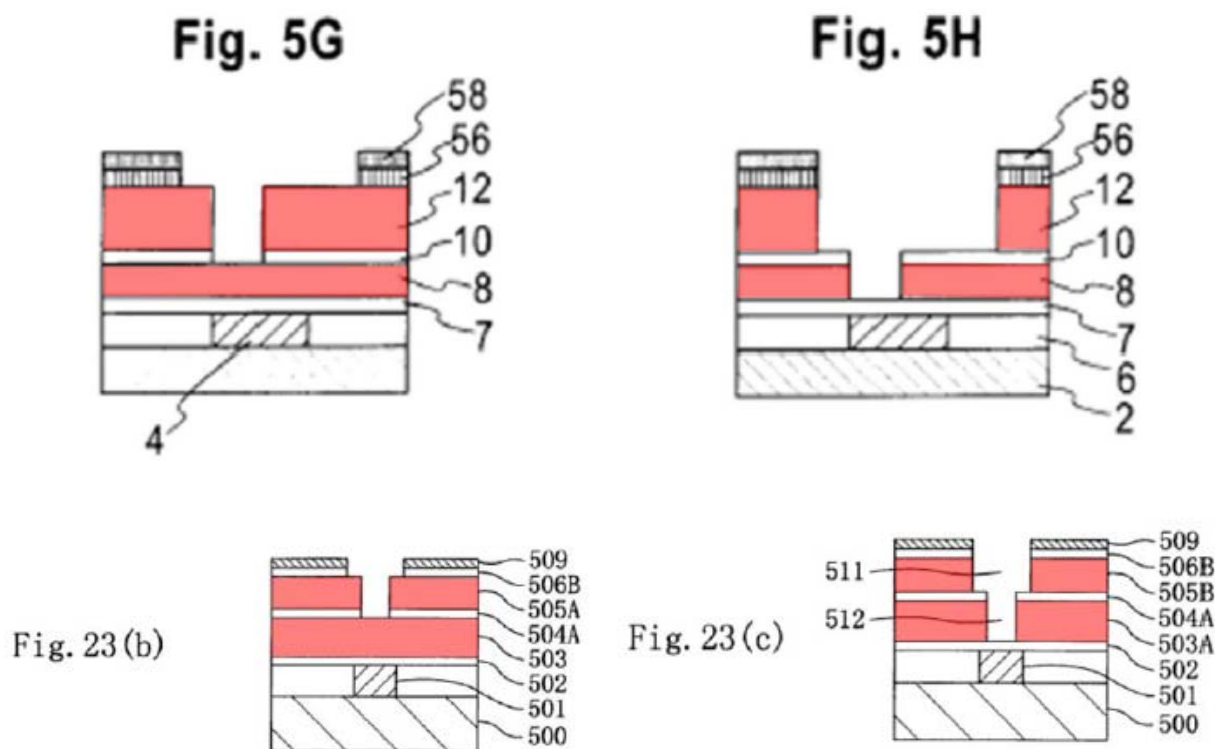
m. [10.13] *Grill* discloses “dry-etching the patterned third insulating film and the first insulating film”

Claim 10 recites “dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively.” *Grill* states, “Dielectrics 8 and 12 are then etched to transfer said second pattern into the entire thickness of dielectric 12, and said first pattern into the entire thickness of dielectric 8, as shown in FIG. 5H.” (Ex. 1005, 8:2–5, Fig. 5H.) As Figures 5G and 5H show below, a POSITA would have understood that upper hard mask [58] masks wiring level dielectric [12] during the etch, and etch stop [10] masks via level dielectric [8]. (Ex. 1002, ¶236.) Additionally, a POSITA would have understood that this is a dry etch for similar reasons explained in section V.B.1.j. (Ex. 1002, ¶237.)

The width of the hole in the wiring level dielectric [12] corresponds to the wiring groove, and the width of the hole in via level dielectric [8] corresponds to the width of the contact hole.

(*Id.*) Figures 23(b) and 23(c) from the fifth embodiment of the '696 patent also appear below.

(*See also* Ex. 1001, 24:7–13; Ex. 1002, ¶¶235–38.)



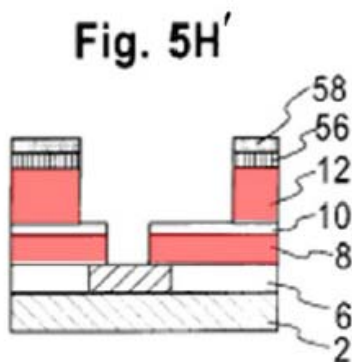
n. [10.14] *Grill* discloses “filling in the wiring grooves”

Claim 10 recites “filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.” A POSITA would have understood that, when not using optional layer [7], the conductive via [4] is exposed after progressing to the step Figure 5H⁵ shown below. (Ex. 1002, ¶240.) Because the conductive via [4] is already exposed when optional layer [7] is not used, a POSITA also would have understood that the additional step in Figure 1J of *Grill* is unnecessary and likely harmful. (*Id.*) The wiring level pattern would not be

⁵ Figure 5H' is identical to Figure 5H of *Grill*, except optional layer 7 has not been used.

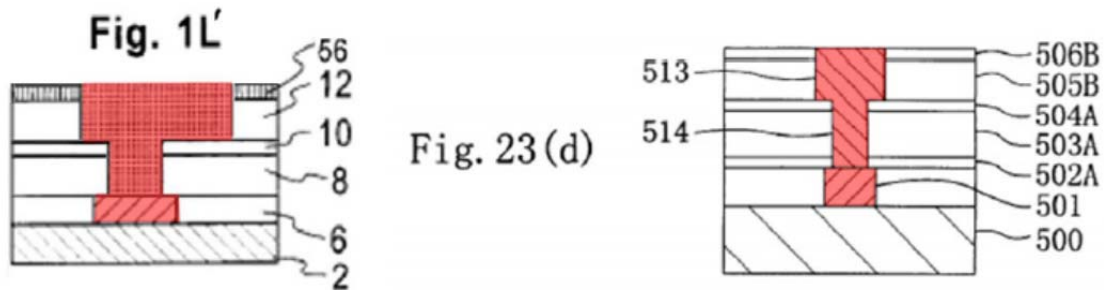
(*See* Ex. 1005, 4:1–2, 4:61–63.)

transferred into etch stop [10].⁶ (*Id.*)



Regarding the claimed step of filling the wiring grooves, *Grill* states, “Cavity 20 is . . . overfilled with conductive wiring material 22, by a process such as physical vapor deposition, chemical vapor deposition, solution deposition, or plating.” (Ex. 1005, 4:64–5:2, Fig. 1K.) The conductive wiring material [22] is planarized by CMP to be approximately even with the top surface of dielectric 12 or remaining hard mask. (*Id.*, 5:2–8, Fig. 1L.) As Figure 1L' shows below, a POSITA would have understood that, when layer [7] is not used, metal fills contact holes in via level dielectric [8] and etch stop [10], as well as wiring grooves in wiring level dielectric [12] and lower hard mask [56]. (Ex. 1002, ¶241.) Figure 23(d) from the fifth embodiment of the '696 patent also appears below. (*See also* Ex. 1001, 24:22–24; Ex. 1002, ¶¶239–42.)

⁶ Even if the optional passivation/adhesion layer [7] is used, a POSITA would have understood that in many cases it is desirable not to etch the etch stop [10] as the passivation/adhesion layer [7] is etched, by using a selective etch. (*See, e.g.*, Ex. 1010, 6:25–29, 6:62–7:2, 7:15–18, 7:55–65, Fig. 10; Ex. 1002, ¶240 & n.5.)



2. Claim 11 is obvious in view of *Grill*

Claim 11 depends from claim 10 (*see* §V.B.1) and further recites that “at least one of the first and third insulating films is mainly composed of an organic component.” As explained in section V.B.1, *Grill* discloses claim 10. *Grill* also discloses claim 11. (Ex. 1002, ¶¶243–47.) *Grill* states that “wiring dielectrics 8 and 12 might be carbon-based materials such as . . . organic or inorganic polymer dielectrics.” (Ex. 1005, 4:1–13.) A POSITA would have understood that these teachings are not affected by the presence or absence of optional passivation/adhesion layer [7]. (Ex. 1002, ¶246.) Thus, *Grill* teaches that via level dielectric [8] and wiring level dielectric [12] may be mainly composed of an organic component. (*Id.*)

C. The *Grill-Aoyama* Combination Renders Claims 10–12 Obvious

As explained in section V.A.3, a POSITA would have been motivated to combine certain teachings of *Grill* and *Aoyama*, and the *Grill-Aoyama* combination is virtually identical to the modified fifth embodiment of the ’696 patent, which claims 10–12 cover. Again, the analysis reflects *Grill*’s disclosure that the dielectric passivation/adhesion layer [7] is optional. (Ex. 1005, 4:1–5, 4:61–63.)

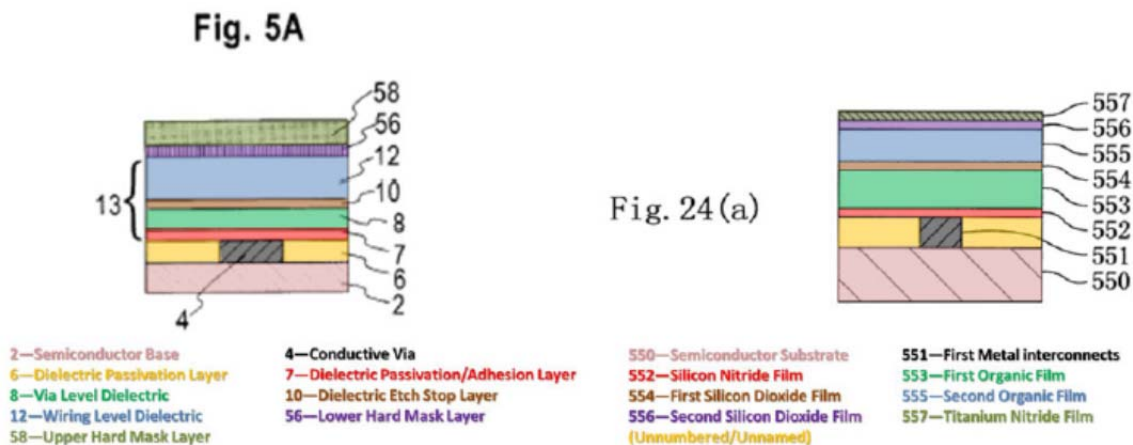
1. Claim 10 is obvious in view of the *Grill-Aoyama* combination

a. [10.1] *Grill* discloses the preamble of claim 10

The preamble of claim 10 recites “[a] method for forming an interconnection structure.” As discussed in section V.B.1.a, *Grill* discloses this feature.

b. [10.2]–[10.6] *Grill* discloses forming first, second, third, and fourth insulating films, and a thin film

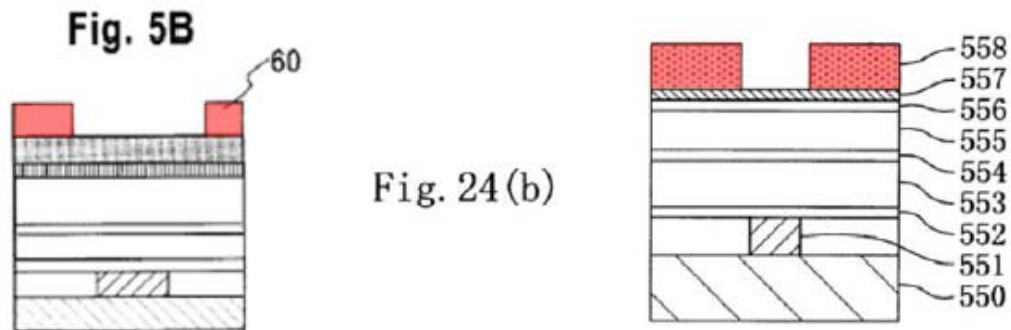
As discussed in sections V.B.1.b through V.B.1.f, *Grill* discloses the claimed steps of forming first, second, third, and fourth insulating films, and forming a thin film. Figure 5A of *Grill* and Figure 24(a) from the modified fifth embodiment of the '696 patent are shown below with annotations and highlights. The first insulating film corresponds to *Grill*'s layer 8 (and the '696 patent's layer 553). The second insulating film corresponds to *Grill*'s layer 10 (and the '696 patent's layer 554). The third insulating film corresponds to *Grill*'s layer 12 (and the '696 patent's layer 555). The fourth insulating film corresponds to *Grill*'s layer 56 (and the '696 patent's layer 556). The thin film corresponds to *Grill*'s layer 58 (and the '696 patent's layer 557). (Compare Ex. 1005, 3:60–4:13, 7:30–42, with, Ex. 1001, 24:60–25:11; see also Ex. 1002, ¶¶250–51.)



c. [10.7] *Grill* discloses “forming a first resist pattern”

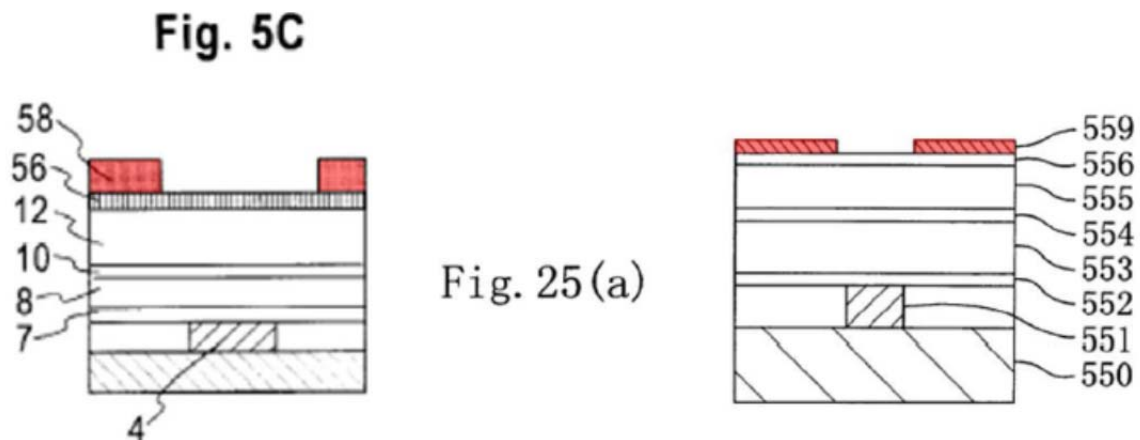
Claim 10 recites “forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves.” As discussed in section V.B.1.g, *Grill* discloses this feature. Figure 5B of *Grill* and Figure 24(b) from the modified fifth embodiment of the '696 patent appear below with highlights. The first resist pattern corresponds to *Grill*'s layer 60

(and the '696 patent's layer 558). (*Compare* Ex. 1005, 7:42–44, *with*, Ex. 1001, 25:19–21; *see also* Ex. 1002, ¶¶252–53.)



d. [10.8] *Grill* discloses “etching the thin film”

Claim 10 recites “etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves.” As discussed in section V.B.1.h, *Grill* discloses this feature. Figure 5C of *Grill* and Figure 25(a) from the modified fifth embodiment of the '696 patent appear below with highlights. The mask pattern corresponds to *Grill*'s patterned layer 58 (and the '696 patent's layer 559). (*Compare* Ex. 1005, 7:45–50, *with*, Ex. 1001, 25:21–25; *see also* Ex. 1002, ¶¶254–55.)

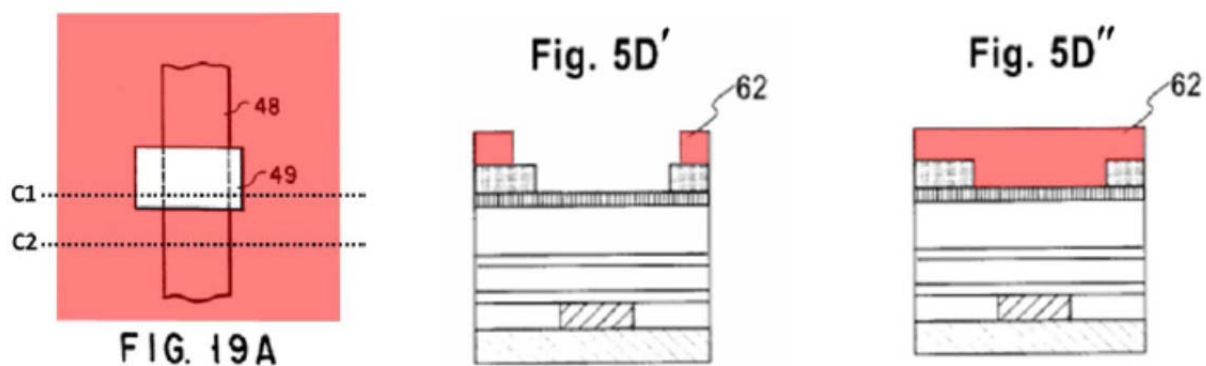


e. [10.9] The *Grill-Aoyama* combination discloses “removing the first resist pattern and then forming a second resist pattern”

Claim 10 recites “removing the first resist pattern and then forming a second resist

pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes.” The *Grill-Aoyama* combination discloses this. (Ex. 1002, ¶¶257–61.) *Grill* states, “Patterned resist layer 60 is then removed by a process such as ashing or wet chemical etching, and a second resist layer 62, patterned with a second (via level) pattern, is then formed on the structure.” (Ex. 1005, 7:51–55, Figs. 5B, 5C, 5D.)

A POSITA would have understood that second resist layer 62 is formed on the fourth insulating film [56] and the mask pattern [58]. (Ex. 1002, ¶258.) The shape of *Aoyama*’s through-hole, viewed from above, is shown in Figure 19A below. The areas colored red in Figure 19A indicate that photoresist is in the areas other than the through-hole location. (Ex. 1002, ¶259.) Two dashed lines have been added to indicate cross-sections C1 and C2. Element 48 is a trench. (Ex. 1018, 16:18–21.) Cross-section C1 of the *Grill-Aoyama* combination appear below in Figure 5D’. (Ex. 1002, ¶259.) Cross-section C2 of the *Grill-Aoyama* combination appear below in Figure 5D”. (*Id.*) The Figures below show that the second resist pattern is on the fourth insulating film [56] and the mask pattern [58]. (*Id.*)



Figures 25(b) and 27(b) from the modified fifth embodiment of the ’696 patent also appear below with highlights. (*See also* Ex. 1001, Fig. 37(a).) The ’696 patent states, “a second resist pattern 560, having openings for forming contact holes, is formed by lithography on the mask pattern 559 as shown in FIG. 25(b).” (Ex. 1001, 25:27–35.)

Fig. 25 (b)

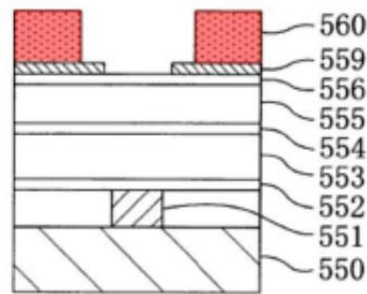
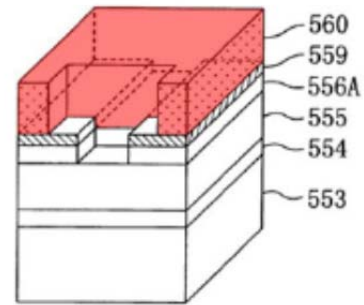


Fig. 27 (b)

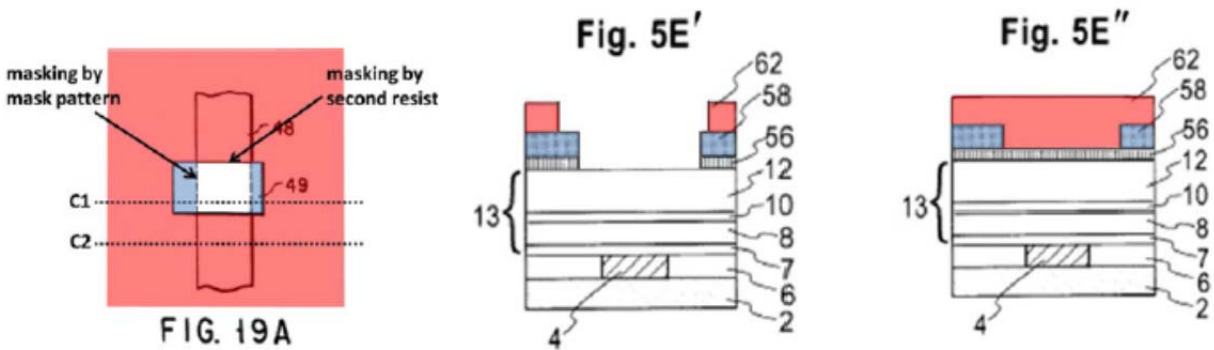


f. [10.10] The *Grill-Aoyama* combination discloses “dry-etching the fourth insulating film”

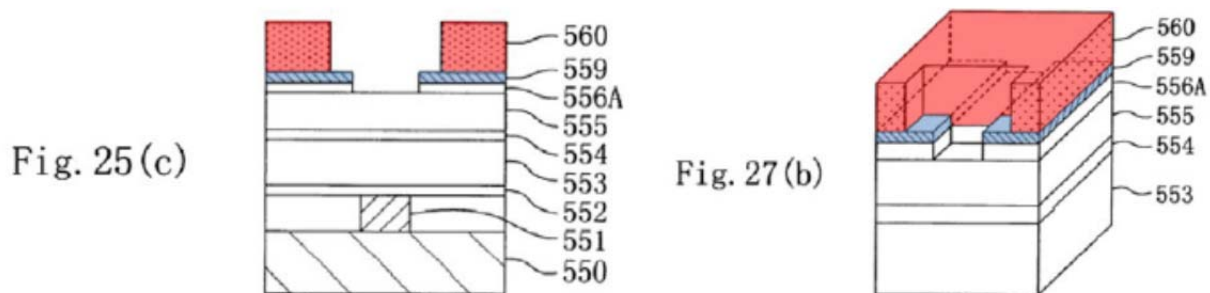
Claim 10 recites “dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes.”

Grill states, “The pattern of resist layer 62 [via level pattern] is then transferred into lower hard mask layer 56.” (Ex. 1005, 7:57–61, Fig. 5E.) As explained in section V.B.1.j, a POSITA would have understood that the lower hard mask layer [56] has openings for forming contact holes because it contains the via pattern of resist layer 62. (Ex. 1005, 7:51–55; Ex. 1002, ¶263.) As section V.B.1.j also explains, a POSITA would have understood that dry etching transfers the second resist pattern [62] into the lower hard mask layer [56]. (Ex. 1002, ¶263.)

A POSITA would have understood that second resist pattern [62] and mask pattern [58] both mask the fourth insulating film [56] during this etch. (Ex. 1002, ¶264.) The shape of *Aoyama*’s through-hole, viewed from above, is Figure 19A shows below. The red areas indicate photoresist [62], and the blue areas indicate the mask pattern [58]. Cross-section C1 of the *Grill-Aoyama* combination is shown in Figure 5E’. (Ex. 1002, ¶265.) Cross-section C2 of the *Grill-Aoyama* combination is shown in Figure 5E”. (*Id.*) The Figures below show masking by the mask pattern [58] and second resist layer [62]. (*See also* Ex. 1002, ¶¶262–67.)



Figures 25(c) and 27(b) from the modified fifth embodiment of the '696 patent also appear below with highlights. (See also Ex. 1001, Fig. 37(a).) The '696 patent states, "the second silicon dioxide film 556 is dry-etched using the second resist pattern 560 and the mask pattern 559 as a mask, thereby forming a patterned second silicon dioxide film 556A having openings for forming contact holes." (Ex. 1001, 25:36–41.)



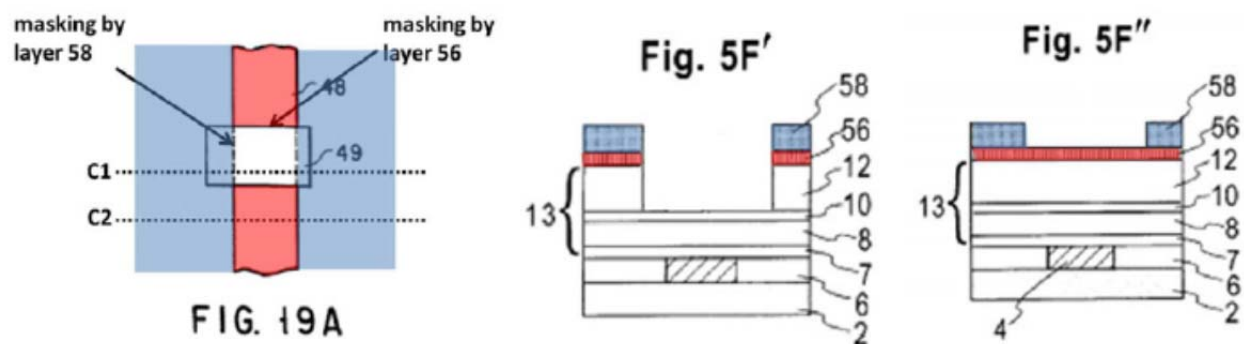
g. [10.11] The *Grill-Aoyama* combination discloses “dry-etching the third insulating film”

Claim 10 recites “dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

Grill states that “[t]he via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching.” (Ex. 1005, 7:62–63, Fig. 5F.) A POSITA would have understood that the patterned third insulating film [56] acts as a mask during this etch. (Ex. 1002,

¶269.) Additionally, a POSITA would have understood that a reactive ion etch is a dry etch.
(*Id.*)

The top surface of *Aoyama*'s structure, viewed from above, appears in Figure 19A below. The resist pattern [62] is removed during the etch of dielectric layer 12, exposing the mask pattern [58] and patterned fourth insulating film [56]. (Ex. 1005, 7:64–66, Figs. 5E, 5F.) The red areas of Figure 19A indicate the patterned fourth insulating film [56], and the blue areas indicate the mask pattern [58]. Cross-section C1 of the *Grill-Aoyama* combination is shown in Figure 5F'. (Ex. 1002, ¶270.) Cross-section C2 of the *Grill-Aoyama* combination appears in Figure 5F''. (*Id.*) The Figures below show masking by the patterned fourth insulating film [56] and the mask pattern [58]. (See also Ex. 1002, ¶¶268–72.)



Figures 26(a) and 28(a) from the modified fifth embodiment of the '696 patent are also shown below with color highlights. (See also Ex. 1001, Fig. 37(a).) The '696 patent states, “the second organic film 555 is dry-etched using the patterned second silicon dioxide film 556A as a mask, thereby forming a patterned second organic film 555A having openings for forming contact holes.” (Ex. 1001, 25:66–26:3.)

Fig. 26 (a)

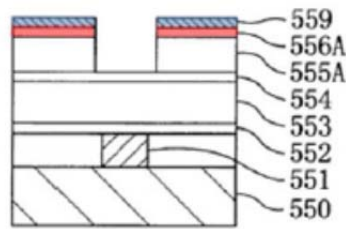
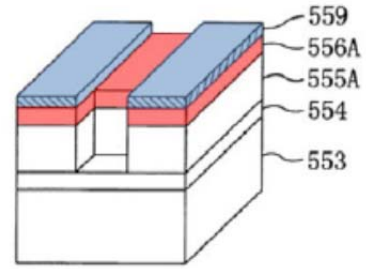


Fig. 28 (a)

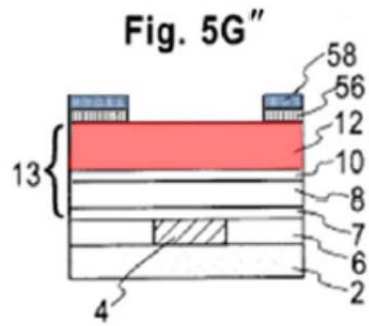
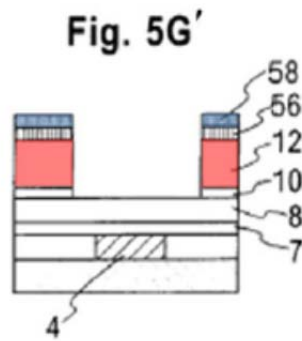
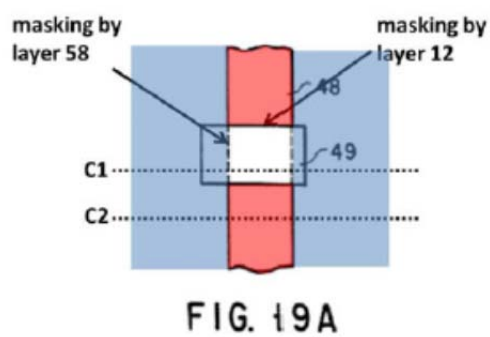


h. [10.12] The *Grill-Aoyama* combination discloses “dry-etching the patterned fourth insulating film and the second insulating film”

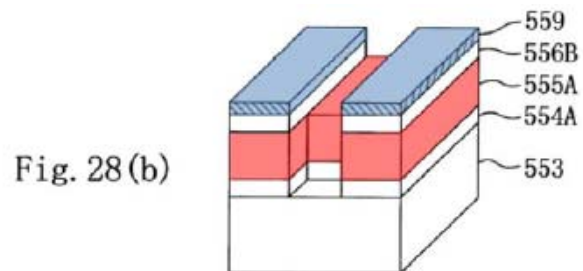
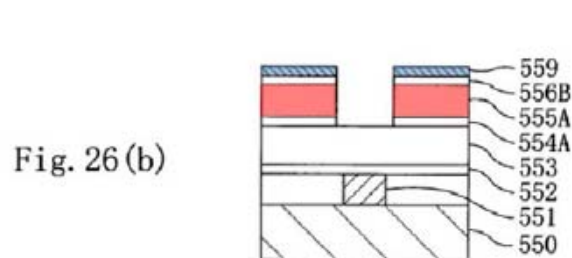
Claim 10 recites “dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes.”

Grill states, “The etching conditions are then changed to removed [sic] exposed portions of lower hard mask layer 56 and optional etch stop 10.” (Ex. 1005, 7:67–8:2, Fig. 5G.) A POSITA would have understood that in the *Grill-Aoyama* combination upper hard mask [58] masks lower hard mask [56] in the wiring groove, and the wiring level dielectric [12] masks etch stop [10] in the contact hole. (Ex. 1002, ¶274.) Additionally, a POSITA would have understood that this etch is a dry etch for similar reasons explained in section V.B.1.j. (*Id.*)

The top surface of *Aoyama*’s structure, viewed from above, appears in Figure 19A below. The red areas of Figure 19A indicate the patterned third insulating film [12], and the blue areas indicate the mask pattern [58]. Cross-section C1 of the *Grill-Aoyama* combination appear in Figure 5G’. (Ex. 1002, ¶275.) Cross-section C2 of the *Grill-Aoyama* combination appear in Figure 5G”. (*Id.*) The Figures below show masking by the patterned third insulating film [12] and the mask pattern [58]. (*See also* Ex. 1002, ¶¶273–77.)



Figures 26(b) and 28(b) from the modified fifth embodiment of the '696 patent also appear below with highlights. (See also Ex. 1001, Fig. 37(a).) The '696 patent states, “the patterned second silicon dioxide film 556A and the first silicon dioxide film 554 are dry-etched using the mask pattern 559 and the patterned second organic film 555A as respective masks, thereby forming a patterned second silicon dioxide film 556B having openings for forming wiring grooves and a patterned first silicon dioxide film 554A having openings for forming contact holes.” (Ex. 1001, 26:15–22.)

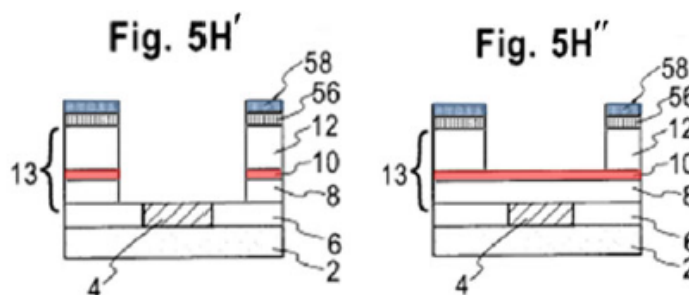
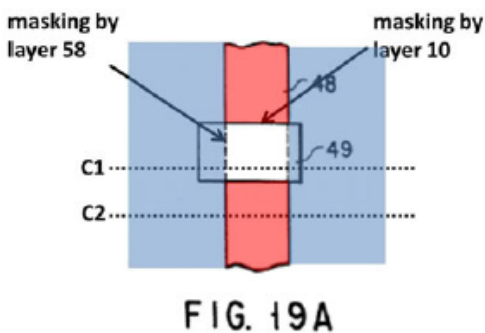


- i. **[10.13] The *Grill-Aoyama* combination discloses “dry-etching the patterned third insulating film and the first insulating film”**

Claim 10 recites “dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively.”

Grill states, “Dielectrics 8 and 12 are then etched to transfer said second pattern into the entire thickness of dielectric 12, and said first pattern into the entire thickness of dielectric 8, as shown in FIG. 5H.” (Ex. 1005, 8:2–5, Fig. 5H.) A POSITA would have understood that upper hard mask [58] masks wiring level dielectric [12], and etch stop [10] masks via level dielectric [8]. (Ex. 1002, ¶279.) Additionally, a POSITA would have understood that this etch is a dry etch for similar reasons explained in section V.B.1.j. (*Id.*)

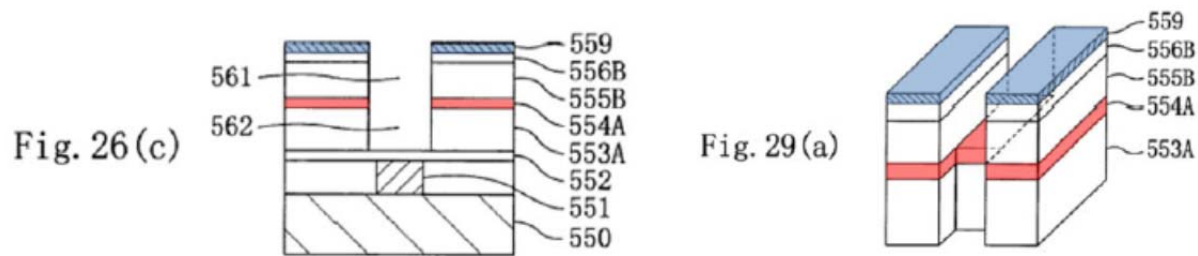
The top surface of *Aoyama*’s structure, viewed from above, is shown in Figure 19A below. The red areas of Figure 19A indicate the patterned second insulating film [10], and the blue areas indicate the mask pattern [58]. Cross-section C1 of the *Grill-Aoyama* combination appears in Figure 5H’. (Ex. 1002, ¶280.) Cross-section C2 of the *Grill-Aoyama* combination appears in Figure 5H”. (*Id.*) The Figures below show masking during the etch by the patterned second insulating film [10] and the mask pattern [58]. (*See also* Ex. 1002, ¶¶278–83.)



Figures 5H’ and 5H” above are illustrated without optional layer [7]. As explained in section V.B.1.n, a POSITA would have understood that the additional step in Figure 1J of *Grill* is unnecessary and likely harmful. (*Id.*, ¶281.) The wiring level pattern, therefore, would not be transferred into etch stop [10]. (*Id.*)

Figures 26(c) and 29(a) from the modified fifth embodiment of the ’696 patent also appear below with highlights. (*See also* Ex. 1001, Fig. 37(a).) The ’696 patent states, “the

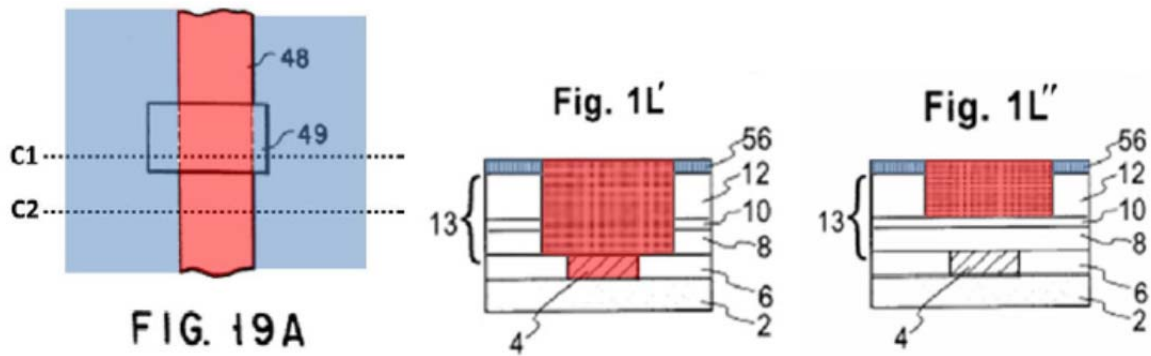
patterned second organic film 555A is dry-etched using the mask pattern 559 and the patterned second silicon dioxide film 556B as a mask, and the first organic film 553 is dry-etched using the patterned first silicon dioxide film 554A as a mask, thereby forming a patterned second organic film 555B having wiring grooves 561 and a patterned first organic film 553A having contact holes 562.” (Ex. 1001, 26:22–29.)



j. [10.14] *Grill* discloses “filling in the wiring grooves”

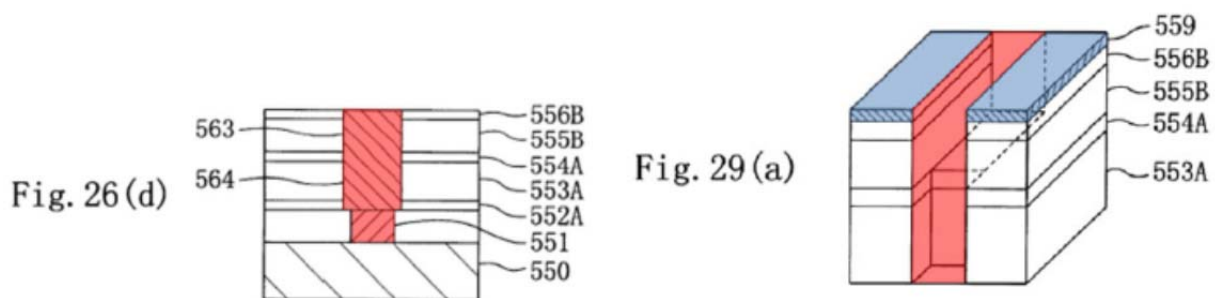
Claim 10 recites “filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.” *Grill* states that “[c]avity 20 is . . . overfilled with conductive wiring material 22, by a process such as physical vapor deposition, chemical vapor deposition, solution deposition, or plating.” (Ex. 1005, 4:64–5:2, Fig. 1K.) The conductive wiring material [22] is planarized by CMP to be approximately even with the top surface of dielectric 12 or remaining hard mask. (*Id.*, 5:2–8, Fig. 1L.)

The top surface of *Aoyama*’s structure, viewed from above, appears in Figure 19A below. The red areas of Figure 19A indicate the metallized regions, and the blue areas indicate the patterned fourth insulating film [56]. Cross-section C1 of the *Grill-Aoyama* combination is shown in Figure 1L’. (Ex. 1002, ¶286.) Cross-section C2 of the *Grill-Aoyama* combination is shown in Figure 1L”. (*Id.*) Optional layer [7] has not been used.



As Figures 1L' and 1L'' show, a POSITA would have understood that, when layer [7] is not used, metal fills the contact holes in etch stop [10] and wiring level dielectric [8] and fills the wiring grooves in lower hard mask [56] and wiring level dielectric [12]. (Ex. 1002, ¶287; *see also supra* §§III.A.13, V.B.1.n.)

Figures 26(d) and 29(a) from the modified fifth embodiment of the '696 patent also appear below. The '696 patent states, “a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 562 and the wiring grooves 561.” (Ex. 1001, 26:38–41.) “As a result, second metal interconnects 563 and contacts 564, connecting the first and second metal interconnects 551 and 563 together, are formed.” (*Id.*, 26:44–47.)



2. Claim 11 is obvious in view of the *Grill-Aoyama* combination

Claim 11 depends from claim 10 (*see* §V.C.1) and further recites that “at least one of the first and third insulating films is mainly composed of an organic component.” As explained in section V.C.1, a POSITA would have understood that the *Grill-Aoyama* combination discloses

each limitation of claim 10. As explained in section V.B.2, a POSITA would have understood that *Grill* discloses the additional feature recited by claim 11. A POSITA would have understood that this disclosure would remain unaffected by the combining it with the relevant teachings of *Aoyama* and regardless of whether layer [7] of *Grill* is used. (Ex. 1002, ¶¶290–93; *see also supra* §V.A.3.)

3. Claim 12 is obvious in view of the *Grill-Aoyama* combination

Claim 12 depends from claim 10 (*see* §V.C.1) and further recites that “a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.” As explained in section V.C.1, a POSITA would have understood that the *Grill-Aoyama* combination discloses each limitation of claim 10.

The '696 patent discusses this feature with reference to Figures 25(b), 25(c), 27(b), 34(b), 36, and 37(a), all shown below with highlights. (*See* Ex. 1001, 25:26–65, 30:49–57, 31:49–67.) The '696 patent explains that “even if the openings of the second resist pattern 560 for forming contact holes have misaligned with the openings of the mask pattern 559 for forming wiring grooves, the openings of the patterned second silicon dioxide film 556A for forming contact holes can be formed to be self-aligned with the openings of the mask pattern 559 for forming wiring grooves.” (*Id.*, 25:46–52.) In addition, “the contacts 564 can connect the first and second metal interconnects 551 and 563 together with a lot more certainty.” (*Id.*, 25:63–65; *see also* 25:42–65, 27:12–60, 31:49–67, Fig. 37(b).)

Fig. 25 (b)

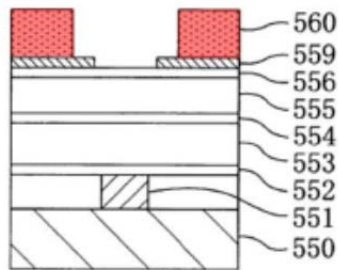


Fig. 25 (c)

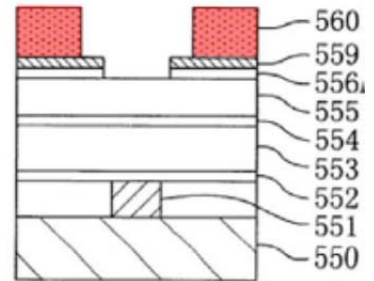


Fig. 27 (b)

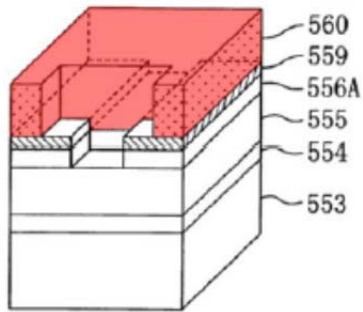


Fig. 34 (b)

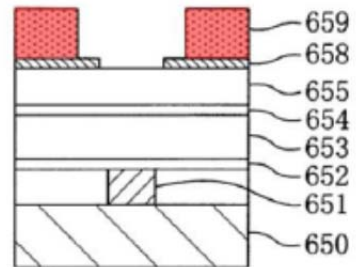


Fig. 36

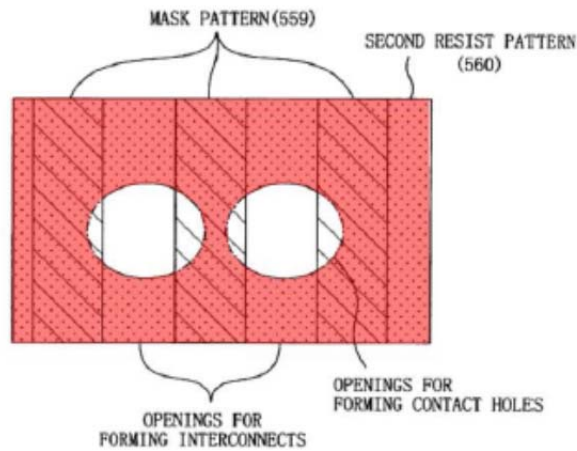
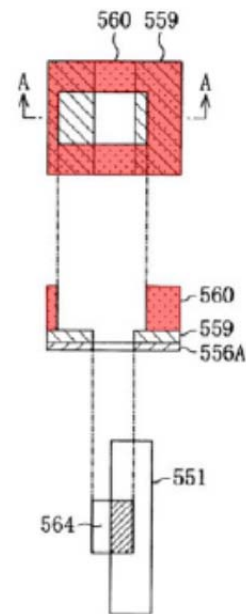
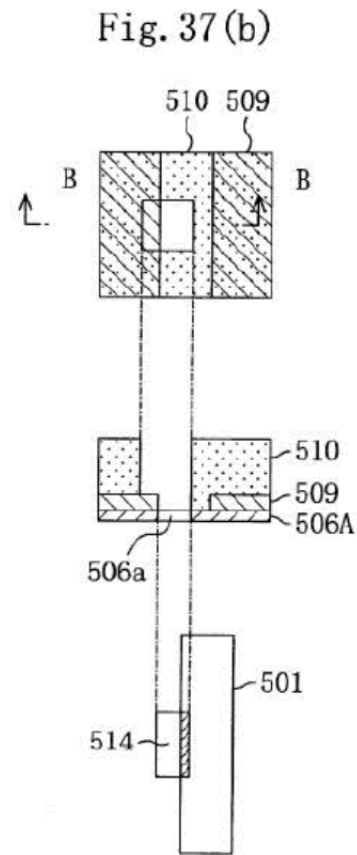
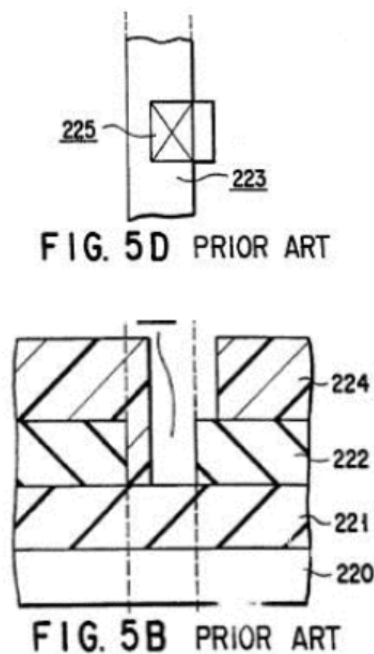


Fig. 37 (a)



Aoyama discloses the same solution to the same problem. *Aoyama* states that misalignment of the photomask during through-hole (via) formation can cause the through-hole

to be smaller than desired and the wiring groove wider than desired at the location of the through-hole. (Ex. 1018, 3:18–21, 3:29–32.) This increases contact resistance, degrades reliability, and makes it difficult to achieve a higher integration density. (*Id.*, 3:33–38, 6:7–14.) The problem is illustrated below by Figures 5B and 5D of *Aoyama*. Figure 37(b) of the '696 patent also appear below for comparison. (See also Ex. 1001, 27:31–51.)



Aoyama resolves this problem using a resist pattern with a through-hole wider than the wiring groove. (*Id.*, 16:3–5, Figs. 18B, 19A.) Even when misaligned, a through-hole having the same width as the wiring groove forms. (*Id.*, 16:14–16, Fig. 19B.) Figures 18B, 19A, and 19B, shown below with highlights, illustrate *Aoyama*'s solution. (See also *id.*, 3:6–38, 6:7–13, 15:48–16:30.) Figure 25(c) and a portion of Figure 37(a) of the '696 patent also appear below with highlighting for comparison. (See also Ex. 1001, 25:42–65, 27:12–60, 31:49–60.)

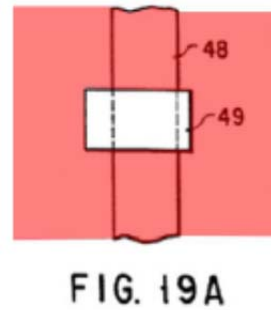
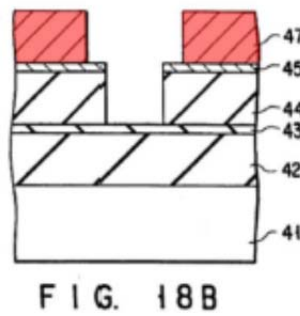
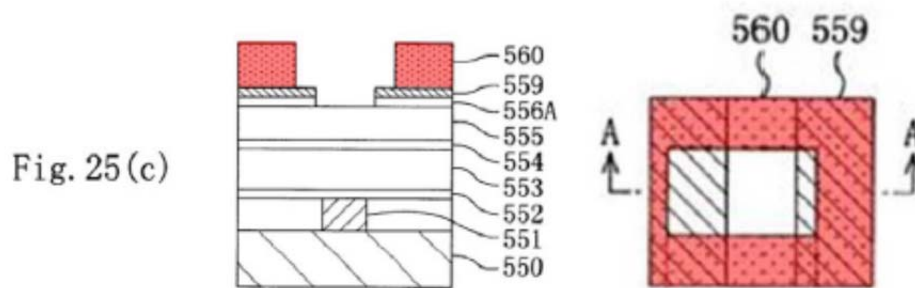


Fig. 37(a)



A POSITA would have understood that these disclosures would remain unaffected by the combining them with the relevant teachings of *Grill* and regardless of whether layer [7] of *Grill* is used. (Ex. 1002, ¶¶294–300; *see also supra* §V.A.3.)

D. Alternative Combinations for Claim 11

If the Board determines Patent Owner is entitled to foreign priority (which, as explained in section III.C, it is not), and in the event the Board determines that the '628 application's "carbon-based dielectrics" do not encompass organic components, Petitioner proposes two contingent grounds of unpatentability for claim 11. Claim 11 would then be obvious in view of (1) the combination of *Grill* (as limited by the '628 application) and *Wetzel* and (2) the combination of *Grill* (as limited by the '628 application), *Aoyama*, and *Wetzel*.

1. Disclosure of *Wetzel* (U.S. Patent No. 5,920,790)

Wetzel (Ex. 1019) teaches a damascene process for forming multilevel metal interconnects in semiconductor devices. (Ex. 1019, Abstract, 1:7–10, Figs. 1–9.) *Wetzel* was filed August 29, 1997, and issued July 6, 1999, so it qualifies as prior art under §102(e). *Wetzel* was neither considered nor cited during prosecution.

Wetzel discloses organic low-k materials as inter-level dielectrics in a damascene process for forming multilevel metal interconnects. *Wetzel* explains, “The via ILD layer 20 is preferably formed of low-k organic materials,” including “polyimides, polyarylethers, PTFEs, polyquinolines, polyphenylquinoxalines, parylenes, and polynaphthalenes” and “benzocyclobutenes, fluorinated amorphous carbons, and polyimides.” (*Id.*, 4:2–12.) *Wetzel* further discloses “a second dielectric layer, trench ILD layer 32,” that “is formed of similar materials” as ILD layer 20. (*Id.*, 4:33–44.) These layers are shown below in highlighted Figure 6.

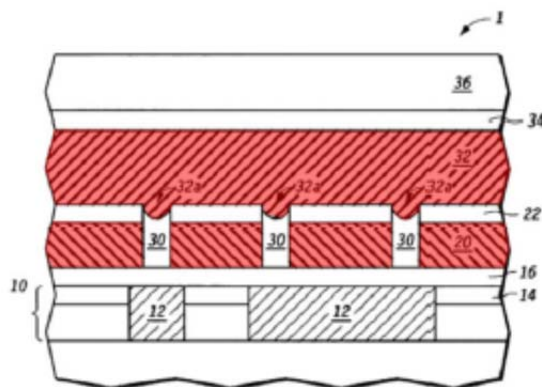


FIG. 6

2. A POSITA would have combined teachings of *Wetzel* with teachings of *Grill*

The '628 application explains that traditional interconnects exhibit signal propagation delays due to large RC time constants. (Ex. 1017, 10.) The '628 application teaches “using interlevel and intralevel dielectrics with lower dielectric constants.” (*Id.*) If the Board determines

the '628 application's "carbon-based dielectrics" do not encompass organic components (*but compare id.*, 10–13, 16, 17, *with* Ex. 1005, 2:30–32, 4:5–8, 7:35–42, 8:26–35; *see also* Ex. 1002, ¶303), a POSITA would have understood that *Wetzel*'s organic components are combinable with the structures in the '628 application. (Ex. 1002, ¶303.) The '628 application teaches diamond-like carbon (DLC) and fluorinated diamond-like carbon (FDLC), for example. (Ex. 1017, 10, 12.) *Wetzel* likewise discloses "fluorinated amorphous carbons," which a POSITA would have understood includes FDLC. (Ex. 1019, 4:8–10; Ex. 1002, ¶303.) *Wetzel* discloses organic low-k materials as substitutes for "fluorinated amorphous carbons" as interlevel and intralayer dielectrics. (Ex. 1019, 4:2–12.)

A POSITA would have understood that using interlevel dielectric materials disclosed by comparable references, such as *Wetzel*, would have been nothing more than a simple substitution of one known element (DLC or FDLC) for another (a low-k organic dielectric) to obtain predictable results. (Ex. 1002, ¶304.) A POSITA thus would have been motivated to use *Wetzel*'s "low-k organic materials" with *Grill*'s teaching of "interlevel and intralevel dielectrics with lower dielectric constants" to achieve predictable results (a reduction in the RC time constant because of lower capacitance). (*Id.*)

3. A POSITA would have combined teachings of *Wetzel* with teachings of *Grill* and *Aoyama*

As explained in the previous section, a POSITA would have been motivated to combine certain teachings of the '628 application and *Wetzel*. As explained in section V.A.3, a POSITA also would have been motivated to combine certain teachings of *Grill* and *Aoyama*. The teachings of *Aoyama* regarding the size of the aperture in the via-defining mask pattern have no bearing on the material choice for the interlevel and intralayer dielectric layers. (Ex. 1002, ¶305.) Conversely, the teachings of *Wetzel* regarding the material choice for the interlevel and

intralayer dielectric layers have no bearing on the size of the aperture in the via-defining mask pattern. (*Id.*) A POSITA would have combined the teachings of *Grill* (as limited by the '628 application), *Aoyama*, and *Wetzel* for the same reasons set forth in sections V.A.3 and V.D.2. (*Id.*)

4. Claim 11 is obvious in view of the *Grill-Wetzel* combination

Claim 11 depends from claim 10 (*see* §V.B.1) and further recites that “at least one of the first and third insulating films is mainly composed of an organic component.” As explained in sections V.B.1.a through V.B.1.n, *Grill* discloses each element of claim 10. (*See also* Ex. 1002, ¶¶179, 306.) To the extent the '628 application is determined not to include it, *Wetzel* discloses the additional feature of claim 11. (Ex. 1002, ¶307.) *Wetzel* states that “[t]he via ILD layer 20 is preferably formed of low-k organic materials, such as thermoplastics or thermosetting plastics” and that “trench ILD layer 32 . . . is formed of similar materials.” (Ex. 1019, 4:2–12, 4:41–44.) A POSITA would have understood that these teachings are not affected by combination with the '628 application's teachings or by the presence or absence of optional layer [7]. (Ex. 1002, ¶307.) Thus, the *Grill-Wetzel* combination discloses that via level dielectric [8] and wiring level dielectric [12] may be mainly composed of an organic component. (*Id.*)

5. Claim 11 is obvious in view of the *Grill-Aoyama-Wetzel* combination

Claim 11 depends from claim 10 (*see* §V.C.1) and further recites that “at least one of the first and third insulating films is mainly composed of an organic component.” As explained in section V.C.1, a POSITA would have understood that the *Grill-Aoyama* combination (as limited by the '628 application) discloses each limitation of claim 10. (*See also* Ex. 1002, ¶¶179, 308.) As explained in section V.D.4, a POSITA would have understood that the contingent *Grill-Wetzel* combination (as limited by the '628 application) discloses the additional feature recited

by claim 11. A POSITA would have understood that this disclosure would remain unaffected by further combining the contingent *Grill-Wetzel* combination with the relevant teachings of *Aoyama*. (Ex. 1002, ¶308; *see also supra* §V.D.3.)

VI. Mandatory Notices Under 37 C.F.R. §42.8

A. Real Parties-In-Interest

The real party in interest is GlobalFoundries U.S. Inc. (“Global”).

B. Related Matters

This petition includes the same grounds and exhibits against the ’696 patent as asserted in IPR2016-01377, filed by Taiwan Semiconductor Manufacturing Company Limited (“TSMC”), which was instituted on January 18, 2017.

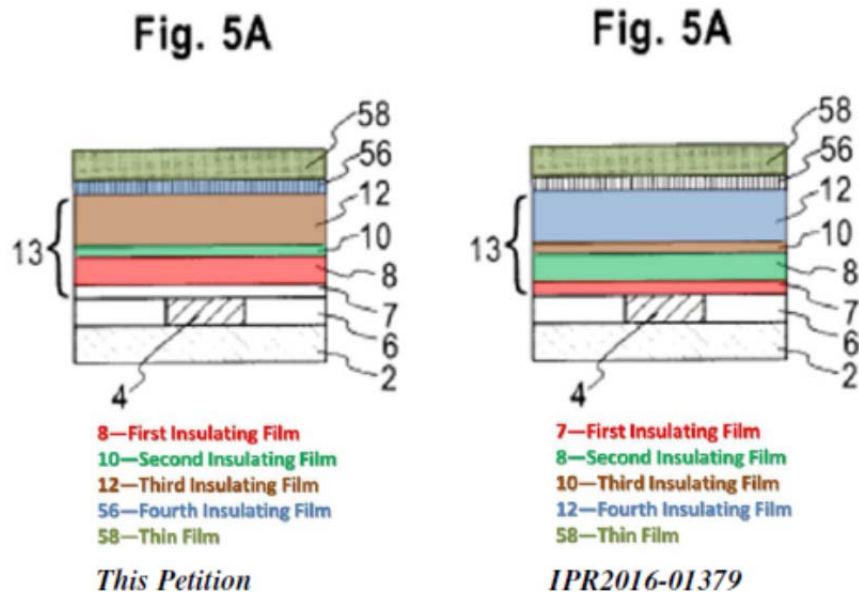
TSMC concurrently filed, with IPR2016-01377, related *inter partes* petitions IPR2016-01376, IPR2016-01378, and IPR2016-01379 challenging several claims of the ’696 patent. IPR2016-01377, IPR2016-01376, IPR2016-01378, and IPR2016-01379 each were instituted on January 18, 2017.

The Petitioner is concurrently filing *inter partes* petitions that have the same ground and exhibits as asserted in IPR2016-01376, IPR2016-01378, and IPR2016-01379.

None of the grounds proposed in these related petitions is redundant. Neither of IPR2016-01376 and IPR2016-01378 challenges any of claims 10, 11, and 12. Like the present Petition, IPR2016-01379 challenges claims 10 and 12 based on the *Grill* and *Aoyama* references, but it does not challenge claim 11 and the proposed grounds further rely on the *Wetzel* reference. And in the present Petition, *Grill* is submitted for single-reference obviousness under §103, whereas in IPR2016-01379 *Grill* is submitted only in obviousness combinations under §103.

Notably, the present Petition and IPR2016-01379 map the layers of the *Grill* reference to the challenged claims in a considerably different manner, such that the substantive basis and

supporting arguments for the petitions materially differ. This is shown in the Figures below.



Patent Owner Godo Kaisha IP Bridge 1 filed a recent lawsuit asserting infringement of the '696 patent. In Case No. 2:16-cv-00134-JRG-RSP (E.D. Tex. Feb. 14, 2016), Patent Owner has sued Avago Technologies Ltd., Avago Technologies US, Inc., Broadcom Corporation, Broadcom Limited, and LSI Corporation. Petitioner is not aware of any other related matters involving the '696 patent.

C. Lead and Back-Up Counsel

Lead Counsel: Christopher P. Carroll (Reg. No. 55,776; Tel. (617) 979-9342; christopher.carroll@whitecase.com), attorney at White & Case LLP, 75 State St, Boston, MA 02109-1814.

Back-Up Counsel: Shamita Etienne-Cummings (Reg. No. 46,072, Tel. (202) 626-3695; setienne@whitecase.com), attorney at White & Case LLP, 701 Thirteenth St NW, Washington, DC 20005-3807.

D. Service Information

Global consents to service by e-mail at the following addresses:

christopher.carroll@whitecase.com, setienne@whitecase.com.

VII. Certification Under 37 C.F.R. §42.24(d)

This Petition complies with 37 C.F.R. §42.24. As calculated by the “Word Count” feature of Microsoft Word 2010, it contains 13,602 words, excluding the words contained in the following: Table of Contents, Table of Authorities, List of Exhibits, Mandatory Notices Under 37 C.F.R. §42.8, Certification Under §42.24(d), and Certificate of Service.

VIII. Payment of Fees

The required fees are submitted electronically in accordance with 37 C.F.R. §§42.103(a) and 42.15(a). If any additional fees are due during this proceeding, the Office is authorized to charge such fees to Deposit Account No. 50-3672.

IX. Time for Filing Petition

This Petition is being filed within one month after the date that institution of IPR2016-01377 was granted on January 18, 2017. 37 C.F.R. §42.122(b).

X. Grounds for Standing

Under 37 C.F.R. §42.104(a), Petitioner certifies that the ’696 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the ’696 patent to challenge the claims on the grounds identified in this Petition.

XI. Conclusion

For the reasons set forth above, the challenged claims are unpatentable. Trial should be instituted and the claims should be cancelled.

Respectfully submitted,

Dated: February 13, 2017

By: /Christopher P. Carroll/
Christopher P. Carroll, Reg. No. 55,776

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Petition for Inter Partes Review, the associated Power of Attorney, and Exhibits 1001 through 1019 were served on February 13, 2017, by express mail at the following address of record for the '696 patent and an address known to the petitioner as likely to effect service:

Address of Record

Attn: Gerald J. Ferguson, Jr.
SIXBEY, FRIEDMAN, LEEDOM &
FERGUSON, P.C.
8180 Greensboro Drive, Suite 800
McLean, VA 22102

Address Likely to Effect Service

Attn: Andrew N. Thomases
Ropes & Gray LLP
1900 University Avenue, 6th Floor
East Palo Alto, CA 94303-2284

Address of Courtesy Copies

Attn: E. Robert Yoches
Finnegan, Henderson, Farabow, Garrett &
Dunner LLP
901 New York Avenue, NW Washington DC
20001-4413

/Christopher P. Carroll/
Christopher P. Carroll
WHITE & CASE LLP
75 State St
Boston, MA 02109-1814
Telephone: (617) 979-9342
Facsimile: (617) 439-6702