

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Taiwan Semiconductor Manufacturing Company, Ltd.

Petitioner

v.

Godo Kaisha IP Bridge 1

Patent Owner

Patent No. 6,197,696

Filing Date: March 23, 1999

Issue Date: March 6, 2001

Title: METHOD FOR FORMING INTERCONNECTION STRUCTURE

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*Inter Partes* Review No. IPR2016-01376

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**DECLARATION OF DR. BRUCE W. SMITH, PH.D.  
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF UNITED  
STATES PATENT NO. 6,197,696**

## **TABLE OF CONTENTS**

I.	Introduction .....	1
II.	Summary of Opinions .....	1
III.	Background and Qualifications .....	2
	A. Background.....	2
	B. Previous Expert Witness Experience.....	3
	C. Compensation .....	3
IV.	Materials Reviewed .....	4
V.	Legal Standards .....	6
	A. Anticipation .....	7
	B. Obviousness.....	8
VI.	Technological Background.....	12
	A. Integrated Circuits and Interconnections .....	12
	B. Semiconductor Etching and Photolithography .....	16
VII.	The '696 Patent.....	19
	A. Description of the Challenged Claims .....	19
	1. Claim 13 .....	19
	2. Claim 15 .....	43
	B. Japanese Patent Application No. 10-079371 does not disclose many elements of claims 13 and 15 .....	46
VIII.	Level of Ordinary Skill in the Art .....	53
IX.	Claim Construction .....	54
X.	Analysis .....	54

A.	<i>Grill</i> (U.S. Patent No. 6,140,226).....	55
B.	<i>Aoyama</i> (U.S. Patent No. 5,592,024) .....	61
C.	The combination of <i>Grill</i> and <i>Aoyama</i> .....	63
D.	<i>Grill</i> and Claim 13 .....	67
E.	The combination of <i>Grill</i> and <i>Aoyama</i> and Claim 13 .....	87
F.	The combination of <i>Grill</i> and <i>Aoyama</i> and Claim 15 .....	103

I, Dr. Bruce W. Smith, Ph.D., declare as follows:

## **I. Introduction**

1. My name is Dr. Bruce W. Smith. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company, Ltd. (“TSMC” or “Petitioner”) in connection with a petition for *inter partes* review of U.S. Patent No. 6,197,696 (“the ’696 patent”).

2. I have been retained as a technical expert by TSMC to study and provide my opinions on the technology in and the validity of claims 13 and 15 in the ’696 patent (“the Challenged Claims”). I have also been asked to provide my opinions as to whether certain related applications provide support for the Challenged Claims and whether a certain prior art reference is supported by the disclosures of its provisional application.

## **II. Summary of Opinions**

3. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the broadest reasonable interpretation of the claims in light of the specification, it is my opinion that the Challenged Claims of the ’696 patent are obvious over the prior art references discussed below.

4. Based on my experience, knowledge of the art at the relevant time, and the broadest reasonable interpretation of the claims in light of the specification,

it is further my opinion that the Challenged Claims do not have support in Japanese application JP 10-079371, to which the '696 patent claims the benefit of priority.

5. Based on my experience, knowledge of the art at the relevant time, and the broadest reasonable interpretation of the claims in light of the specification, it is further my opinion that at least claim 28 of the *Grill* reference (U.S. Patent No. 6,140,226) is supported by U.S. Provisional Patent Application No. 60-071,628, to which the *Grill* reference claims the benefit of priority.

### **III. Background and Qualifications**

#### **A. Background**

6. I have over 30 years of research, academic, industry, and consulting engineering experience in IC (integrated circuit) processing, semiconductor device materials, microelectronics, and microlithography. I have expertise in semiconductor IC processes and fabrication, microlithography, and deposition and etch processes.

7. I am a professor of Microelectronic Engineering and the Director of the Ph.D. program in Microsystems Engineering at the Rochester Institute of Technology (RIT).

8. I am a Fellow of the Institute of Electrical and Electronics Engineers (IEEE), a Fellow of the International Society for Optical Engineering (SPIE), and a Fellow of the Optical Society of America (OSA). I have received numerous

awards including the IEEE Technology Innovation Award, the RIT Trustees Scholarship Award, the SPIE Research Mentoring Award, the RIT Creators Award, and the Rush Henrietta Outstanding Alumni Award, among others, and have been inducted into RIT's Innovator Hall of Fame.

9. I have published over 200 technical papers, articles, textbooks, and textbook chapters, and I hold 27 patents. My patented technologies have been licensed both nationally and internationally.

10. Additional details about my employment history, fields of expertise, and publications are further included in my curriculum vitae, attached as Appendix A.

**B. Previous Expert Witness Experience**

11. I have served as an expert witness since the mid 1990's. In the last ten years or so, I have testified at the International Trade Commission twice and district court three times. In addition, I have been deposed over twenty times on patents related to semiconductor device fabrication. Several of these have been IPR cases. Additional details about my litigation consulting experience are further included in my curriculum vitae, attached as Appendix A.

**C. Compensation**

12. I am being compensated for services provided in this matter at my usual and customary rate of \$525 per hour plus travel expenses. My compensation

is not conditioned on the conclusions I reach as a result of my analysis or on the outcome of this matter, and in no way affects the substance of my statements in this declaration.

13. I have no financial interest in Petitioner TSMC or any of its subsidiaries. I also have no financial interest in Patent Owner Godo Kaisha IP Bridge 1. I do not have any financial interest in the '696 patent and have not had any contact with any of the named inventor of the '696 patent, Nobuo Aoi.

#### **IV. Materials Reviewed**

14. In forming my opinions, I have reviewed the following references:

- The '696 patent (which I understand is Exhibit 1001 to TSMC's petition);
- U.S. Patent No. 3,617,824 ("*Shinoda*," which I understand is Exhibit 1003 to TSMC's petition);
- U.S. Patent No. 3,838,442 ("*Humphreys*," which I understand is Exhibit 1004 to TSMC's petition);
- U.S. Patent No. 6,140,226 ("*Grill*," which I understand is Exhibit 1005 to TSMC's petition);
- U.S. Patent No. 5,635,423 ("*Huang*," which I understand is Exhibit 1006 to TSMC's petition);

- U.S. Patent No. 5,741,626 (“*Jain*,” which I understand is Exhibit 1007 to TSMC’s petition);
- C. Akrou et al., “A 480-MHz Microprocessor in a  $0.12\mu\text{m}$   $L_{\text{eff}}$  CMOS Technology with Copper Interconnects,” IEEE J. of Solid-State Circuits, Vol. 33, no. 11 (November 1998) (“*Akrou*,” which I understand is Exhibit 1008 to TSMC’s petition);
- J.N. Burghartz et al., “Monolithic Spiral Inductors Fabricated Using a VLSI Cu-Damascene Interconnect Technology and Low-Loss Substrates,” International Electron Devices Meeting (December 1996) (“*Burghartz*,” which I understand is Exhibit 1009 to TSMC’s petition);
- U.S. Patent No. 6,100,184 (“*Zhao*,” which I have been told is Exhibit 1010 to TSMC’s petition);
- U.S. Patent No. 6,103,616 (“*Yu*,” which I have been told is Exhibit 1011 to TSMC’s petition);
- File History of U.S. Patent No. 6,197,696 to Aoi et al. (which I have been told is Exhibit 1012 to TSMC’s petition)
- Japanese Patent Application No. 10-079371 to Aoi (“the ’371 application,” which I have been told is Exhibit 1013 to TSMC’s petition);



- Certified Translation of Japanese Patent Application No. 10-079371 to Aoi (“the ’371 application,” which I have been told is Exhibit 1014 to TSMC’s petition);
- Japanese Patent Application No. 11-075519 to Aoi (which I have been told is Exhibit 1015 to TSMC’s petition);
- Certified Translation of Japanese Patent Application No. 11-075519 to Aoi (“the ’519 application,” which I have been told is Exhibit 1016 to TSMC’s petition);
- U.S. Provisional Patent Application No. 60/071,628 (which I have been told is Exhibit 1017 to TSMC’s petition); and
- U.S. Patent No. 5,592,024 to Aoyama et al. (“*Aoyama*,” which I have been told is Exhibit 1018 to TSMC’s petition).

## **V. Legal Standards**

15. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the ’696 patent are patentable, I have been told that I am obliged to follow existing law. I have been told the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §§ 102 and 103.

16. I also understand that, in an *inter partes* review proceeding, patent claims may be deemed unpatentable if it is shown by preponderance of the

evidence that they were anticipated and/or rendered obvious by one or more prior art patents or publications.

17. Further, I have been told that, in an *inter partes* review proceeding, patent claims cannot claim the benefit of priority to a domestic or a foreign application, if the domestic or the foreign application does not adequately describe or enable those claims.

**A. Anticipation**

18. I have been told that for a claim to be anticipated under § 102, every limitation of the claimed invention must be found in a single prior art reference.

19. I have been told that a claim is unpatentable as anticipated under § 102(a) if the claimed invention was “known or used by others in this country, or patented or described in a printed publication in this or another country, before the invention thereof by the applicant for patent.”

20. I have been told that a claim is unpatentable as anticipated under § 102(b) if the claimed invention was “patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States.”

21. I have been told that a claim is unpatentable as anticipated under § 102(e) if “the invention was described in (1) an application for patent, published

under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.”

**B. Obviousness**

22. I have been told that under 35 U.S.C. § 103(a), “[a] patent may not be obtained although the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.”

23. When considering the issues of obviousness, I have been told that I am to do the following:

- a. Determine the scope and content of the prior art;
- b. Ascertain the differences between the prior art and the claims at issue;

- c. Resolve the level of ordinary skill in the pertinent art; and
- d. Consider evidence of secondary indicia of non-obviousness (if available).

24. I have been told that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of alleged invention, which I have assumed is shortly before the '696 patent was filed.

25. I have been told that obviousness is a determination of law based on underlying determinations of fact. I have been told that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and secondary considerations of non-obviousness.

26. I have been told that any assertion of secondary indicia must be accompanied by a nexus between the merits of the invention and the evidence offered.

27. I have been told that a reference may be combined with other references to disclose each element of the invention under § 103. I have been told that a reference may also be combined with the knowledge of a person of ordinary skill in the art and that this knowledge may be used to combine multiple references. I have also been told that a person of ordinary skill in the art is presumed to know the relevant prior art. I have been told that the obviousness

analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

28. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been told that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

29. I have been told that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I have been told that the inferences and creative steps a person of ordinary skill in the art would employ are also relevant to the determination of obviousness.

30. I have been told that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been told that if a person of ordinary skill in the art can implement a predictable variation and would see the benefit of doing so, that variation is likely to be obvious. I have been told that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been told that, when

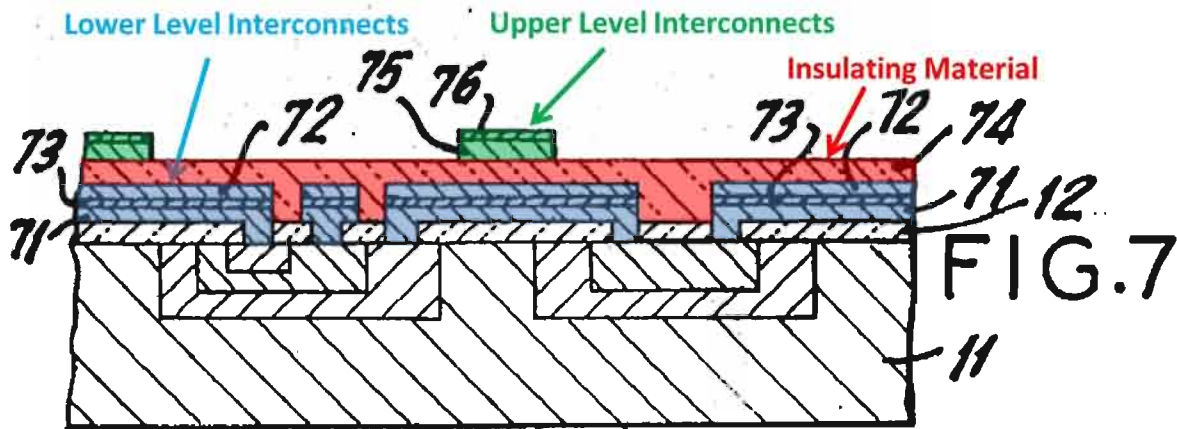
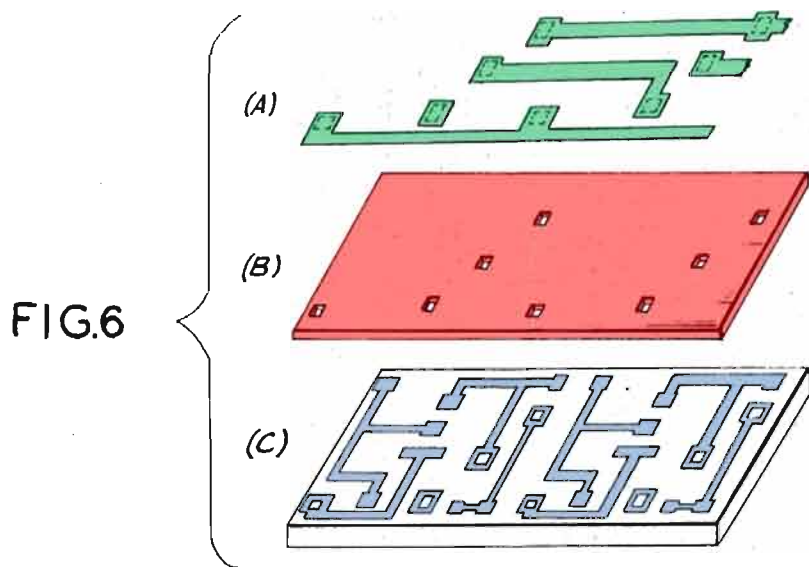
there is a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art has good reason to pursue those known options.

31. I have been told that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been told that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

## **VI. Technological Background**

### **A. Integrated Circuits and Interconnections**

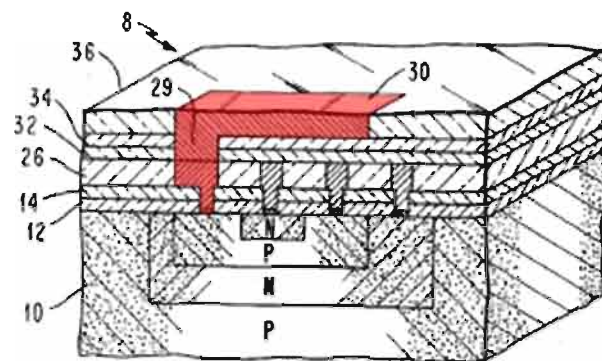
32. Integrated circuits contain millions of discrete semiconductor devices. These discrete devices are electrically connected to one another by “interconnections,” or “interconnects,” to form circuits. U.S. Patent No. 3,617,824, from 1965, provides an early example of interconnects. (*Shinoda* at 4:30–73, Figs. 6, 7.) For example, Figures 6 and 7 of *Shinoda* (below) shows interconnects (in blue and green) in an integrated circuit.



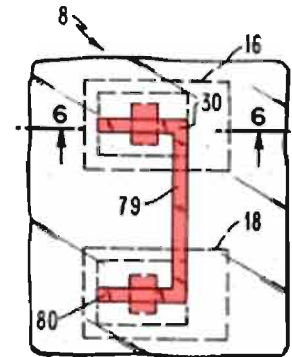
33. Interconnects having a “via” and “trench” portions were very common years before the application for the '696 patent was filed. “Vias” provide an electrical connection path between device levels by extending between the planes of one or more adjacent layers. When filled with a conductive material, these vias provide the electrical contact between conductive layers and are often also referred to as contact holes. When filled with a conductive material, the “trenches” are the



wires that link the filled vias (or contacts) to form circuits. Figures 6 and 6A of U.S. Patent No. 3,838,442 show this structure. (*Humphreys* at Abstract, 1:54–2:6, 8:19–54, Figs. 6, 6A, 7, 7A.)



**FIG. 6**



**FIG. 6A**

34. Multiple levels of interconnects are typically used to form various circuits within a microchip. The vias are vertical metal patterns that link each interconnect level together. The trenches are coplanar with the semiconductor substrate and connect the circuit elements. These trenches define each metallization level in an integrated circuit. This type of multi-level wiring scheme was common in semiconductor processing years before the time the application for the '696 patent was filed. Examples appear below. (*Akrout* at Fig. 2; *Burghartz* at Fig. 2.) The via-trench structures are readily apparent.

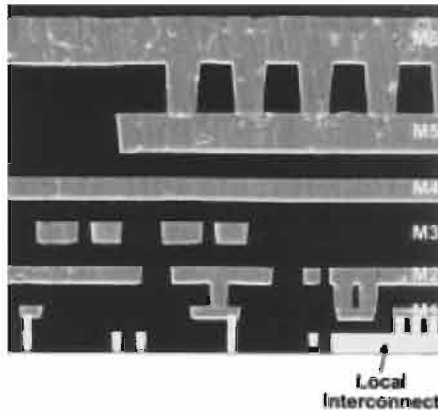


Fig. 2 Scanning electron microscope of six copper metal levels and local interconnect.

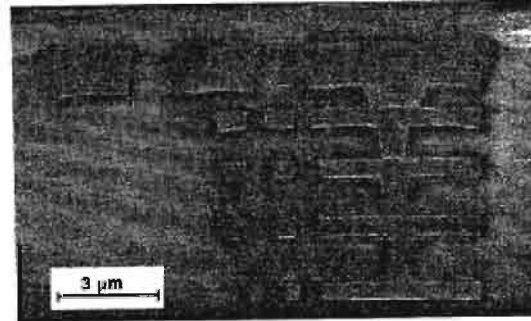
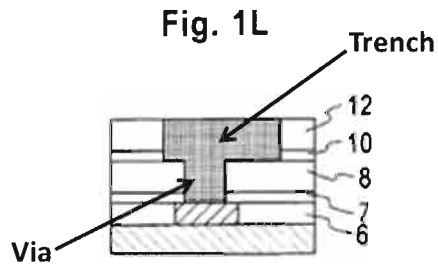


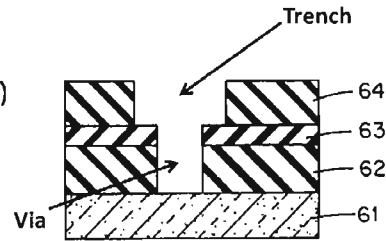
Fig. 2 Cross-sectional SEM of a five-level Cu-damascene interconnect structure with oxide isolation. (Note that the structure is illustrated to demonstrate the VLSI capability of the process; the dimensions of metal layers, vias, and oxide isolation are different from the ones used for the inductor fabrication.)

35. One way to make this type of interconnect structure is a damascene process. In a damascene process, the via and trench patterns are etched into an insulating material, and those patterns are filled with metal. Excess metal is removed by a chemical-mechanical polish (CMP) treatment. In a single damascene process, the via and trench levels are formed independently through two separate damascene processes. In a dual damascene process, the vias and trenches are formed in the same process. Like other metallization processes, the resulting structure formed in a dual damascene process is characterized by via portions for contacting each discrete device and trenches for linking the vias. (*Grill* at 1:45–48, 3:33–36; *Huang* at Abstract, 2:61–3:2, 3:54–57; *Jain* at 2:15–20.) Examples of the dual-damascene structure appear below with annotations. (*Grill* at Fig. 1L; *Huang* at Figs. 6(c), 9; *Jain* at Fig. 5.)



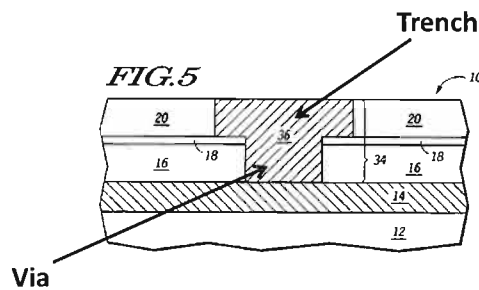
*Grill*

FIG. 6(c)

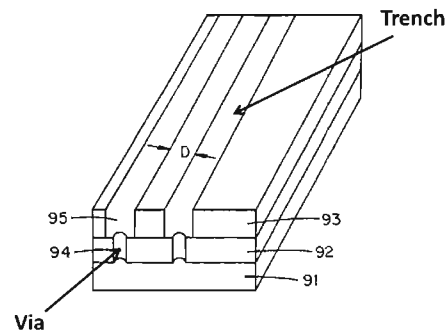


*Huang*

FIG. 9



*Jain*



*Huang*

## B. Semiconductor Etching and Photolithography

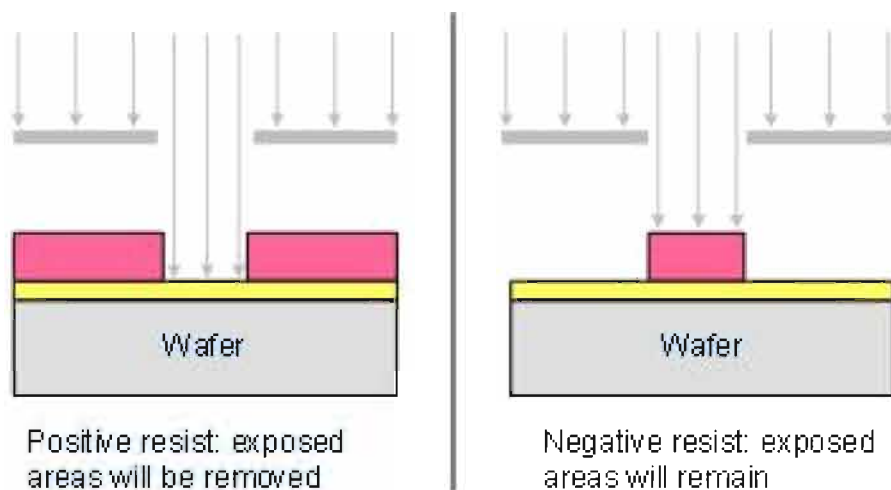
36. One semiconductor processing technology that can create patterns in a semiconductor wafer is called photolithography.

37. In photolithography, a chemical called a “photoresist” uniformly coats the surface of the processed semiconductor wafer. Photoresist is sensitive to light and will change its molecular structure when illuminated under the right conditions.

38. A photomask, which is transparent in some regions and opaque in others, contains a pattern that is meant to be transferred to the processed wafer through the photoresist. After the photomask is aligned, the photoresist is illuminated through the photomask. The exposed photoresist is altered by the light.

39. Any photoresist that is not part of the pattern can be removed with a chemical called a “developer.” The processed wafer retains the patterned photoresist layer, which can be used to help pattern material beneath the photoresist.

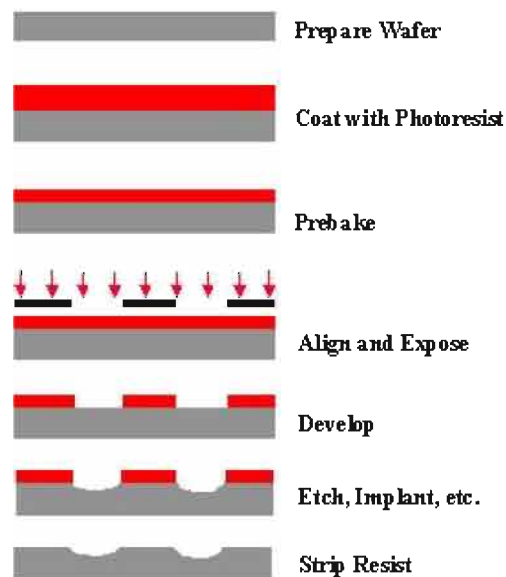
40. A schematic representation of two photolithography processes appear below. In a “negative” photoresist process, the exposed portions of the photoresist remain on the processed wafer. In a “positive” photoresist process, the illuminated portions of the photoresist are removed from the processed wafer.



41. Another semiconductor processing technology that can create patterns in a semiconductor wafer is called etching. Etching usually complements photolithography.

42. A patterned photoresist layer can serve as a “mask” during an etch process. In an etch process, surfaces of the processed wafer (semiconductor substrate and/or overlying layers) are exposed to corrosive chemicals to remove certain portions of the processed wafer.

43. After etching, the photoresist may be “stripped” (i.e., removed) from the wafer by another chemical treatment. In some processes, the photoresist may also be removed during etching. The following diagram shows photolithography and etching.



44. An etch that attacks all exposed materials is called a non-selective etch. An etch that attacks certain material compositions more than others is called

a selective etch. The ratio of etch rates between two materials is known as “selectivity.” (*Wang* at 6:1–11.)

45. An etch that attacks a material in all directions is called isotropic. An etch that attacks a material in a preferred direction (most commonly perpendicular to the surface of the wafer) is called anisotropic.

46. An etch that uses a liquid etching agent is called a “wet” etch. An etch that does not use a liquid (typically an ionized gas, called a “plasma,” instead) is called a “dry” etch.

47. In dual damascene processes, selective anisotropic dry etching is typically used. (*Huang* at 2:61–63; *Zhao* at 2:45–48; *Yu* at 4:9–12.) This preserves the critical dimensions (i.e., the sizing) of the vias and trenches and ensures that the correct layers are etched during each step of the process.

## **VII. The ’696 Patent**

### **A. Description of the Challenged Claims**

#### **1. Claim 13**

48. A person of ordinary skill in the art would have understood that claim 13 reads on the fifth and sixth embodiments, including the modified fifth and sixth embodiments, of the ’696 patent. (’696 patent at 22:47–29:60, Figs. 21(a)–37(b).) Below I describe the steps of claim 13 of the ’696 patent with reference to the fifth and sixth embodiments of the ’696 patent (including their modified counterparts).

49. The preamble of claim 13 recites “[a] method for forming an interconnection structure.” The ’696 patent, titled “Method of Forming Interconnection Structure,” states that “[t]he present invention relates to a method for forming an interconnection structure in a semiconductor integrated circuit.” (’696 patent at Title, Abstract, 1:6–8.)

50. Step a) of claim 13 recites “forming a first insulating film [504, 554, 603, 653] over lower-level metal interconnects [501, 551, 601, 651].”

51. In my opinion, a person of ordinary skill in the art would have understood that in the fifth embodiment the claimed first insulating film is first silicon dioxide film 504, which is located over lower-level interconnects 501. (’696 patent at 22:52–62.) A person of ordinary skill in the art would have understood that silicon dioxide is an insulating film.

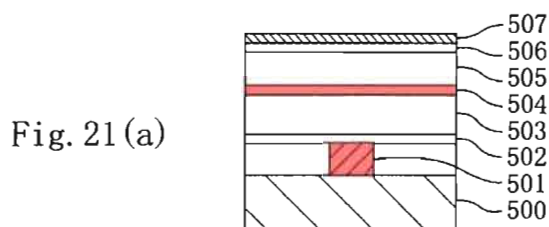
52. In my opinion, a person of ordinary skill in the art would have understood that in the modified fifth embodiment the claimed first insulating film is first silicon dioxide film 554, which is over lower-level interconnects 551. (’696 patent at 24:60–25:3.) A person of ordinary skill in the art would have understood that silicon dioxide is an insulating film.

53. In my opinion, a person of ordinary skill in the art would have understood that in the sixth embodiment the claimed first insulating film is first

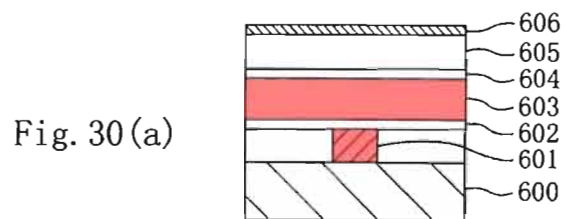
organic film 603, which is an “insulating film” and located over lower-level interconnects 601. (’696 patent at 28:1–9.)

54. In my opinion, a person of ordinary skill in the art would have understood that in the modified sixth embodiment the claimed first insulating film is first organic film 653, which is an “insulating film” and located over lower-level interconnects 651. (’696 patent at 30:1–11.)

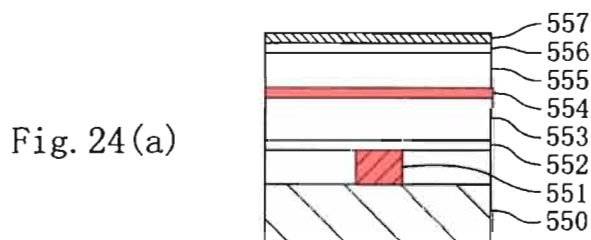
55. Figures 21(a), 24(a), 30(a), and 33(a) from the ’696 patent showing step a) appear below. (’696 patent at 22:52–23:24, 24:60–25:11, 28:1–36, 30:1–16, Figs. 21(a), 24(a), 30(a), 33(a).)



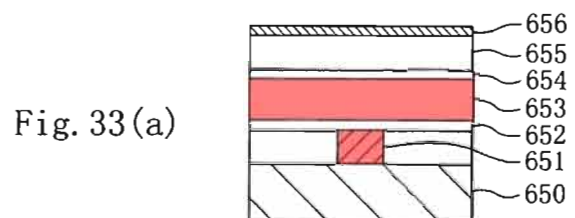
***Fifth Embodiment***



***Sixth Embodiment***



***Modified Fifth Embodiment***



***Modified Sixth Embodiment***



56. Step b) of claim 13 recites “forming a second insulating film [505, 555, 604, 654], having a different composition than that of the first insulating film, over the first insulating film [504, 554, 603, 653].”

57. In my opinion, a person of ordinary skill in the art would have understood that in the fifth embodiment the claimed second insulating film is “second organic film 505,” which is an “insulating film” and has a composition that differs from the composition of the claimed first insulating film (first silicon dioxide film 504). (’696 patent at 22:60–64.) A person of ordinary skill in the art would have understood that silicon dioxide is not organic. A person of ordinary skill in the art also would have understood that second organic film 505 is located over first silicon dioxide film 504.

58. In my opinion, a person of ordinary skill in the art would have understood that in the modified fifth embodiment the claimed second insulating film is “second organic film 555,” which is an “insulating film” and has a composition that differs from the composition of the claimed first insulating film (first silicon dioxide film 554). (’696 patent at 25:1–6.) A person of ordinary skill in the art would have understood that silicon dioxide is not organic. A person of ordinary skill in the art also would have understood that second organic film 555 is located over first silicon dioxide film 554.

59. In my opinion, a person of ordinary skill in the art would have understood that in the sixth embodiment the claimed second insulating film is “silicon dioxide film 604,” which has a composition that differs from the composition of the claimed first insulating film (first organic film 603). (’696 patent at 28: 6–11.) A person of ordinary skill in the art would have understood that silicon dioxide is an insulating film and that it is not organic. A person of ordinary skill in the art also would have understood that silicon dioxide film 604 is located over first organic film 603.

60. In my opinion, a person of ordinary skill in the art would have understood that in the modified sixth embodiment the claimed second insulating film is “silicon dioxide film 654,” which has a composition that differs from the composition of the claimed first insulating film (first organic film 653). (’696 patent at 30:6–11.) A person of ordinary skill in the art would have understood that silicon dioxide is an insulating film and that it is not organic. A person of ordinary skill in the art also would have understood that silicon dioxide film 654 is located over first organic film 653.

61. Figures 22(a), 24(a), 30(a), and 33(a) from the ’696 patent showing step b) appear below. (’696 patent at 22:52–23:24, 24:60–25:11, 28:1–36, 30:1–16, Figs. 21(a), 24(a), 30(a), 33(a).)

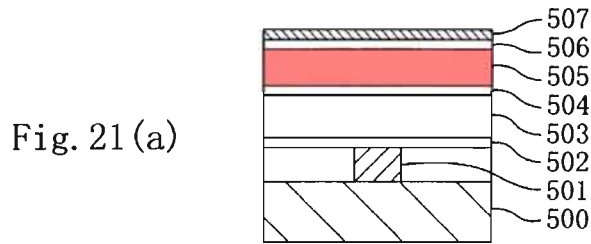


Fig. 21(a)

***Fifth Embodiment***

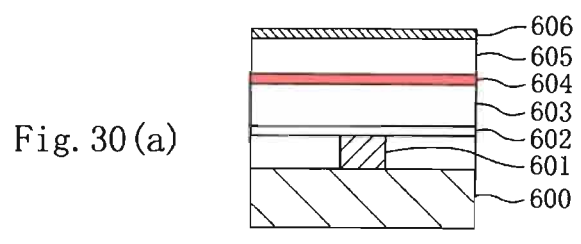


Fig. 30(a)

***Sixth Embodiment***

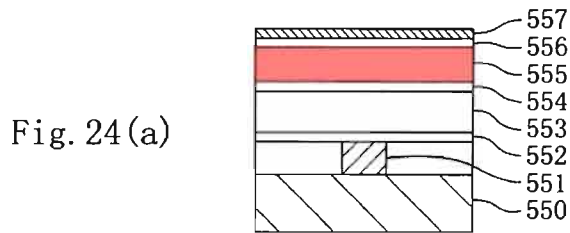


Fig. 24(a)

***Modified Fifth Embodiment***

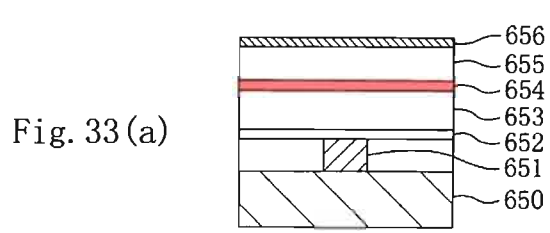


Fig. 33(a)

***Modified Sixth Embodiment***

62. Step c) of claim 13 recites “forming a third insulating film [506, 556, 605, 655], having a different composition than that of the second insulating film, over the second insulating film [505, 555, 604, 654].”

63. In my opinion, a person of ordinary skill in the art would have understood that in the fifth embodiment the claimed third insulating film is “second silicon dioxide film 506,” which has a composition that differs from the composition of the claimed second insulating film (second organic film 505). (’696 patent at 22:62–67.) A person of ordinary skill in the art would have understood that silicon dioxide is an insulating film and that it is not organic. A person of ordinary skill in the art also would have understood that second silicon dioxide film 506 is located over second organic film 505.

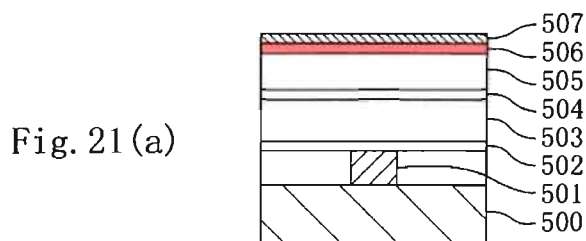
64. In my opinion, a person of ordinary skill in the art would have understood that in the modified fifth embodiment the claimed third insulating film is “second silicon dioxide film 556,” which has a composition that differs from the composition of the claimed second insulating film (second organic film 555). (’696 patent at 25:3–9.) A person of ordinary skill in the art would have understood that silicon dioxide is an insulating film and that it is not organic. A person of ordinary skill in the art also would have understood that second silicon dioxide film 556 is located over second organic film 555.

65. In my opinion, a person of ordinary skill in the art would have understood that in the sixth embodiment the claimed third insulating film is “second organic film 605,” which is an “insulating film” and has a composition that differs from the composition of the claimed second insulating film (silicon dioxide film 604). (’696 patent at 28: 9–13.) A person of ordinary skill in the art would have understood that silicon dioxide is not organic. A person of ordinary skill in the art also would have understood that second organic film 605 is located over silicon dioxide film 604.

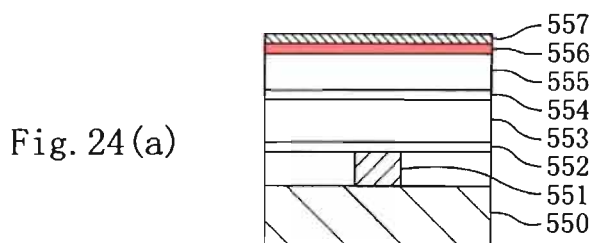
66. In my opinion, a person of ordinary skill in the art would have understood that in the modified sixth embodiment the claimed third insulating film is “second organic film 655,” which is an “insulating film” and has a composition that differs from the composition of the claimed second insulating film (silicon

dioxide film 654). ('696 patent at 30:9–14.) A person of ordinary skill in the art would have understood that silicon dioxide is not organic. A person of ordinary skill in the art also would have understood that second organic film 655 is located over silicon dioxide film 654.

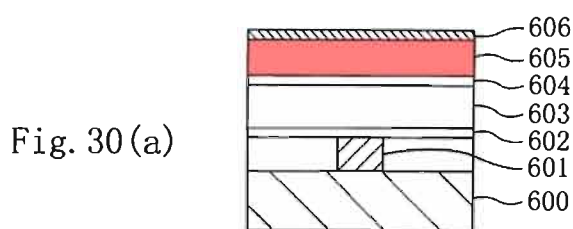
67. Figures 21(a), 24(a), 30(a), and 33(a) from the '696 patent showing step c) appear below. ('696 patent at 22:52–23:24, 24:60–25:11, 28:1–36, 30:1–16, Figs. 21(a), 24(a), 30(a), 33(a).)



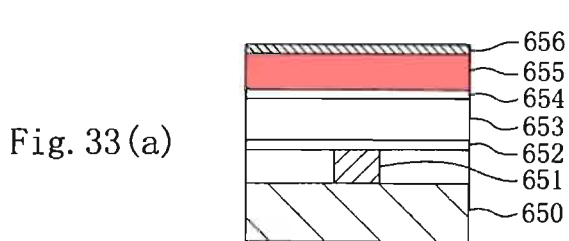
***Fifth Embodiment***



***Modified Fifth Embodiment***



***Sixth Embodiment***



***Modified Sixth Embodiment***

68. Step d) of claim 13 recites “forming a thin film [507, 557, 606, 656] over the third insulating film [506, 556, 605, 655].”

69. I believe that a person of ordinary skill in the art would have understood that in the fifth embodiment, “a titanium nitride film 507 (thin film) is

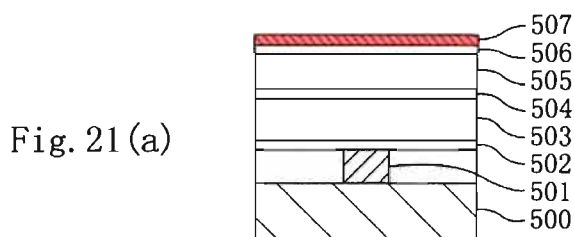
deposited to be 50 nm thick.” (’696 patent at 23:1–3.) A person of ordinary skill in the art would have understood that titanium nitride film 507 is located over the claimed third insulating film (second silicon dioxide film 506).

70. I believe that a person of ordinary skill in the art would have understood that in the modified fifth embodiment, “a titanium nitride film 557 is deposited to be 50 nm thick.” (’696 patent at 25:9–11.) A person of ordinary skill in the art would have understood that titanium nitride film 557 is located over the claimed third insulating film (second silicon dioxide film 556).

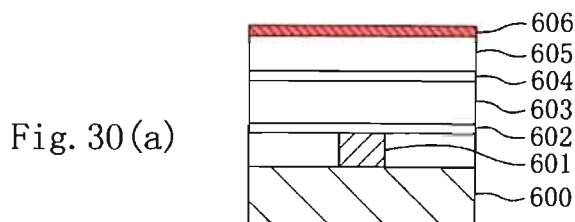
71. I believe that a person of ordinary skill in the art would have understood that in the sixth embodiment, “a titanium nitride film 606 (thin film) is deposited to be 50 nm thick.” (’696 patent at 28:14–16.) A person of ordinary skill in the art would have understood that titanium nitride film 606 is located over the claimed third insulating film (second organic film 605).

72. I believe that a person of ordinary skill in the art would have understood that in the modified sixth embodiment, “a titanium nitride film 656 (thin film) is deposited to be 50 nm thick.” (’696 patent at 30:14–16.) A person of ordinary skill in the art would have understood that titanium nitride film 656 is located over the claimed third insulating film (second organic film 655).

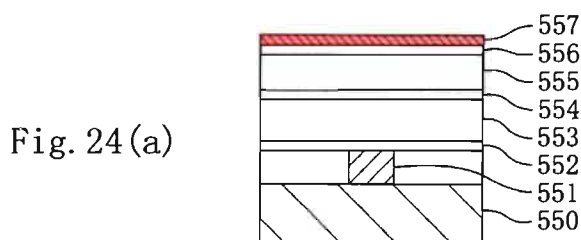
73. Figures 21(a), 24(a), 30(a), and 33(a) from the '696 patent showing step d) appear below. ('696 patent at 22:52–23:24, 24:60–25:11, 28:1–36, 30:1–16, Figs. 21(a), 24(a), 30(a), 33(a).)



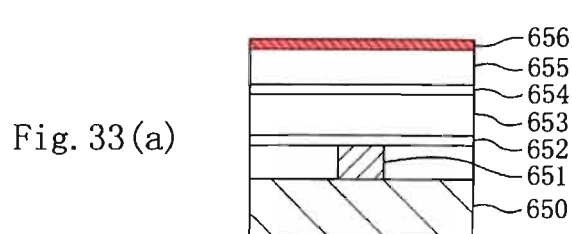
***Fifth Embodiment***



***Sixth Embodiment***



***Modified Fifth Embodiment***



***Modified Sixth Embodiment***

74. Step e) of claim 13 recites “forming a first resist pattern [508, 558, 607, 657] on the thin film [507, 557, 606, 656], the first resist pattern having openings for forming wiring grooves.”

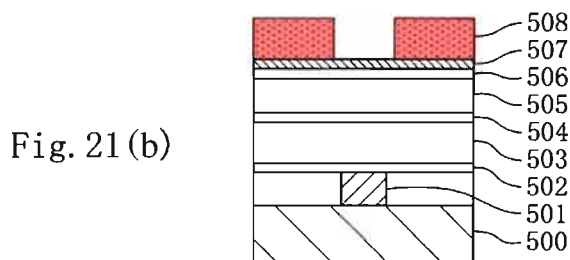
75. I believe that a person of ordinary skill in the art would have understood that in the fifth embodiment, “a first resist pattern 508, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 507.” ('696 patent at 23:25–27.)

76. I believe that a person of ordinary skill in the art would have understood that in the modified fifth embodiment, “a first resist pattern 558, having openings for forming wiring grooves, is formed on the titanium nitride film 557.” (’696 patent at 25:19–21.)

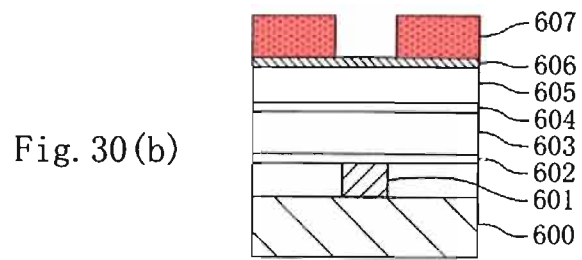
77. I believe that a person of ordinary skill in the art would have further understood that in the sixth embodiment, “a first resist pattern 607, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 606.” (’696 patent at 28:37–39.)

78. I believe that a person of ordinary skill in the art would have further understood that in the modified sixth embodiment, “a first resist pattern 657, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 656.” (’696 patent at 30:37–39.)

79. Figures 21(b), 24(b), 30(b), and 33(b) of the ’696 patent showing step e) appear below. (’696 patent at 23:25–32, 25:19–25, 28:37–43, 30:37–43, Figs. 21(b), 24(b), 30(b), 33(b).)



***Fifth Embodiment***



***Sixth Embodiment***



Fig. 24 (b)

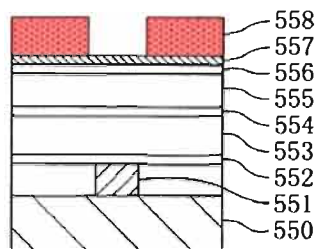
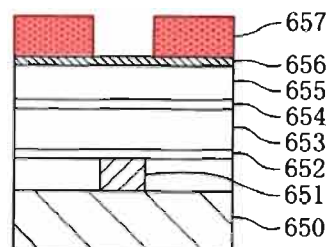


Fig. 33 (b)



### *Modified Fifth Embodiment*

### *Modified Sixth Embodiment*

80. Step f) of claim 13 recites “etching the thin film [507, 557, 606, 656] using the first resist pattern [508, 558, 607, 657] as a mask, thereby forming a mask pattern [509, 559, 608, 658] out of the thin film to have the openings for forming wiring grooves.”

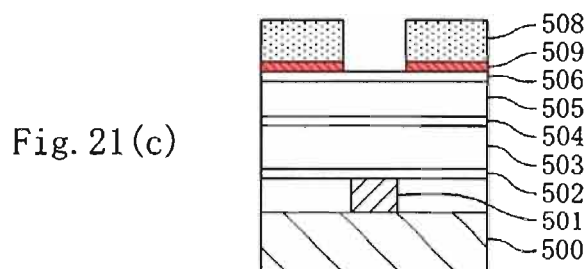
81. I believe that a person of ordinary skill in the art would have understood that in the fifth embodiment, “the titanium nitride film 507 is dry-etched using the first resist pattern 508 as a mask, thereby forming a mask pattern 509, having openings for forming wiring grooves, out of the titanium nitride film 507.” (’696 patent at 23:27–32.)

82. I believe that a person of ordinary skill in the art would have understood that in the modified fifth embodiment, “the titanium nitride film 557 is dry-etched using the first resist pattern 558 as a mask, thereby forming a mask pattern 559, having openings for forming wiring grooves, out of the titanium nitride film 557.” (’696 patent at 25:21–25.)

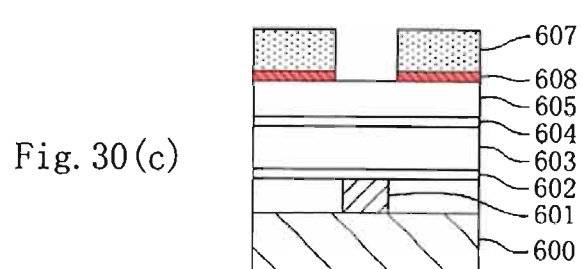
83. I believe that a person of ordinary skill in the art would have understood that in the sixth embodiment, “the titanium nitride film 606 is dry-etched using the first resist pattern 607 as a mask, thereby forming a mask pattern 608, having openings for forming wiring grooves, out of the titanium nitride film 606.” (’696 patent at 28:39–43.)

84. I believe that a person of ordinary skill in the art would have understood that in the modified sixth embodiment, “the titanium nitride film 656 is dry-etched using the first resist pattern 657 as a mask, thereby forming a mask pattern 658, having openings for forming wiring grooves, out of the titanium nitride film 656.” (’696 patent at 30:39–43.)

85. Figures 21(c), 24(c), 30(c), and 33(c) of the ’696 patent showing step f) appear below. (’696 patent at 23:25–32, 25:19–25, 28:37–43, 30:36–43, Figs. 21(c), 24(c), 30(c), 33(c).)



*Fifth Embodiment*



*Sixth Embodiment*

Fig. 24(c)

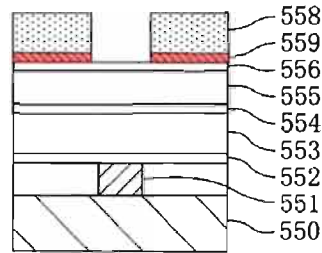
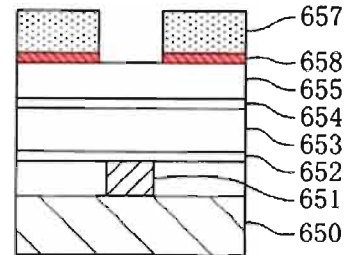


Fig. 33(c)



***Modified Fifth Embodiment***

***Modified Sixth Embodiment***

86. Step g) of claim 13 recites “removing the first resist pattern [508, 558, 607, 657] and then forming a second resist pattern [510, 560, 609, 659] on the third insulating film [506, 556, 605, 655] and the mask pattern [509, 559, 608, 658], the second resist pattern having openings for forming contact holes.”

87. I believe a person of ordinary skill in the art would have understood that in the fifth embodiment, “the first resist pattern 508 is removed.” (’696 patent at 23:33–34.) “Then, as shown in FIG. 22(b), a second resist pattern 510, having openings for forming contact holes, is formed by lithography on the mask pattern 509.” (’696 patent at 23:40–42.)

88. I believe a person of ordinary skill in the art would have understood that in the modified fifth embodiment, “the first resist pattern 558 is removed.” (’696 patent at 25:26–27.) “Then, a second resist pattern 560, having openings for forming contact holes, is formed by lithography on the mask pattern 559 as shown in FIG. 25(b).” (’696 patent at 25:27–35.)

89. I believe a person of ordinary skill in the art would have understood that in the sixth embodiment “the first resist pattern 607 is removed.” (’696 patent at 28:44–46.) “Then, as shown in FIG. 31(b), a second resist pattern 609, having openings for forming contact holes, is formed by lithography on the mask pattern 608.” (’696 patent at 28:49–51.)

90. I believe a person of ordinary skill in the art would have understood that in the modified sixth embodiment “the first resist pattern 657 is removed.” (’696 patent at 30:44–46.) “Then, as shown in FIG. 34(b), a second resist pattern 659, having openings for forming contact holes, is formed by lithography on the mask pattern 658.” (’696 patent at 30:49–57.)

91. Figures 22(a), 22(b), 25(a), 25(b), 31(a), 31(b), 34(a), and 34(b) showing step g) appear below. (’696 patent at 23:33–42, 25:26–35, 28:44–51, 30:44–57, Figs. 22(a), 22(b), 25(a), 25(b), 31(a), 31(b), 34(a), 34(b).)

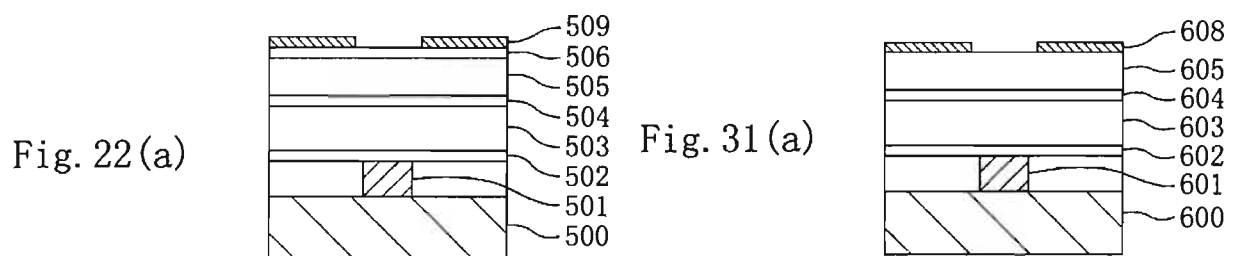


Fig. 22(b)

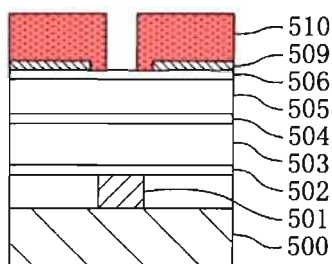
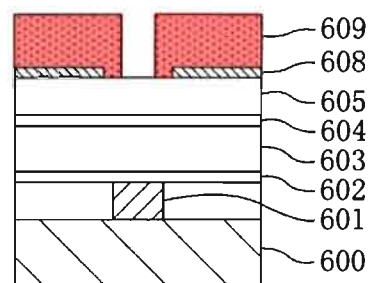


Fig. 31(b)



***Fifth Embodiment***

***Sixth Embodiment***

Fig. 25(a)

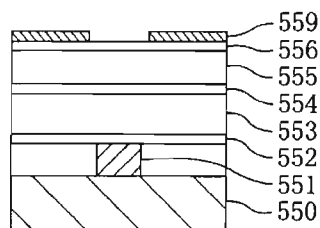


Fig. 34(a)

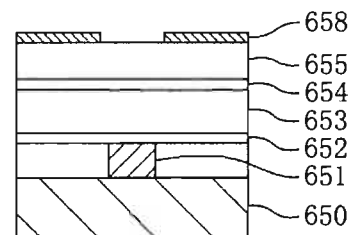


Fig. 25(b)

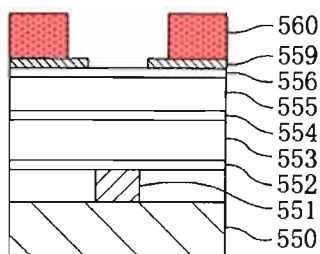
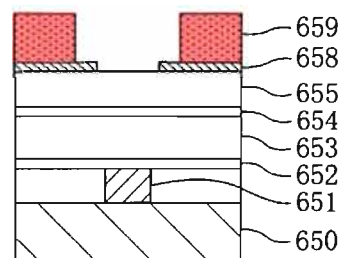


Fig. 34(b)



***Modified Fifth Embodiment***

***Modified Sixth Embodiment***

92. Step h) of claim 13 recites “dry-etching the third insulating film [506, 556, 605, 655] using the second resist pattern [510, 560, 609, 659] and the mask pattern [509, 559, 608, 658] as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

93. I believe a person of ordinary skill in the art would have understood that regarding the fifth embodiment, the '696 patent states, “the second silicon

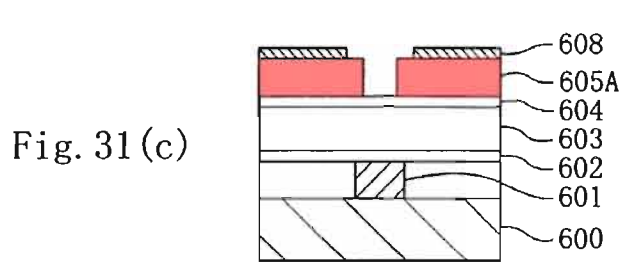
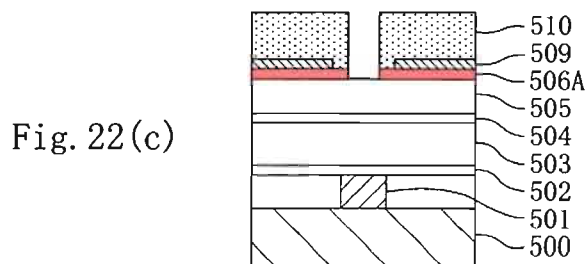
dioxide film 506 is dry-etched using the second resist pattern 510 and the mask pattern 509 as a mask, thereby forming a patterned second silicon dioxide film 506A having openings for forming contact holes as shown in FIG. 22(c).” (’696 patent at 23:42–46.)

94. I believe a person of ordinary skill in the art would have understood that in the modified fifth embodiment, “the second silicon dioxide film 556 is dry-etched using the second resist pattern 560 and the mask pattern 559 as a mask, thereby forming a patterned second silicon dioxide film 556A having openings for forming contact holes as shown in FIGS. 25(c) and 27(b).” (’696 patent at 25:36–41.)

95. I believe a person of ordinary skill in the art would have understood that in the sixth embodiment, “the second organic film 605 is dry-etched using the second resist pattern 609 and the mask pattern 608 as a mask, thereby forming a patterned second organic film 605A having openings for forming contact holes as shown in FIG. 31(c).” (’696 patent at 28:51–55.)

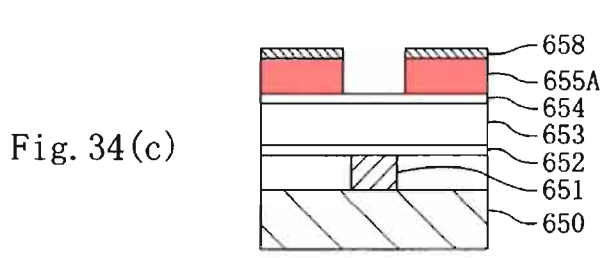
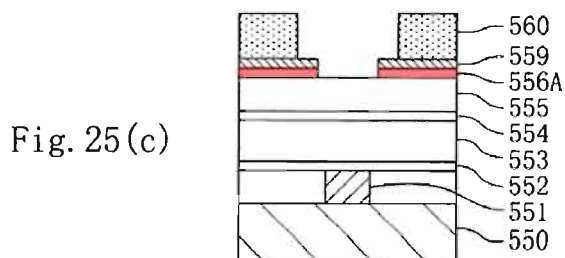
96. I believe a person of ordinary skill in the art would have understood that in the modified sixth embodiment, “the second organic film 655 is dry-etched using the second resist pattern 659 and the mask pattern 658 as a mask, thereby forming a patterned second organic film 655A having openings for forming contact holes as shown in FIG. 34(c).” (’696 patent at 30:58–62.)

97. Figures 22(c), 25(c), 27(b), 31(c), and 34(c) from the '696 patent showing step h) appear below. ('696 patent at 23:42–46, 25:36–41, 28:51–55, 30:58–31:6, Figs. 22(c), 25(c), 27(b), 31(c), 34(c).)



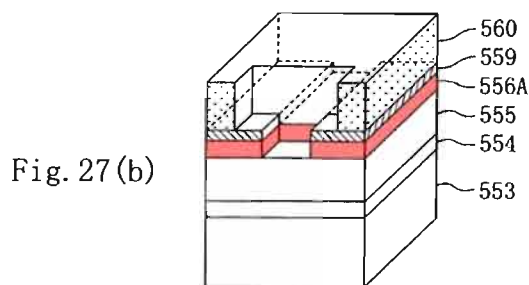
*Fifth Embodiment*

*Sixth Embodiment*



*Modified Fifth Embodiment*

*Modified Sixth Embodiment*



*Modified Fifth Embodiment*

98. Step i) of claim 13 recites “dry-etching the second insulating film [505, 555, 604, 654] using the patterned third insulating film [506A, 556A, 605A,

655A] as a mask, thereby patterning the second insulating film to have the openings for forming contact holes.”

99. I believe a person of ordinary skill in the art would have understood that in the fifth embodiment, “the second organic film 505 is dry-etched using the patterned second silicon dioxide film 506A as a mask, thereby forming a patterned second organic film 505A having openings for forming contact holes as shown in FIG. 23(a).” (’696 patent at 23:47–51.)

100. I believe a person of ordinary skill in the art would have understood that in the modified fifth embodiment, “the second organic film 555 is dry-etched using the patterned second silicon dioxide film 556A as a mask, thereby forming a patterned second organic film 555A having openings for forming contact holes as shown in FIGS. 26(a) and 28(a).” (’696 patent at 25:66–26:3.)

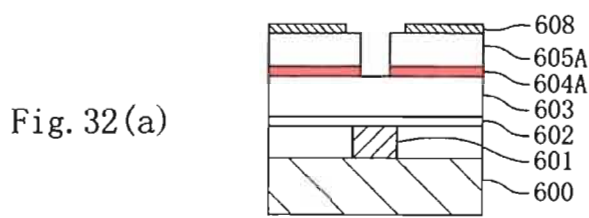
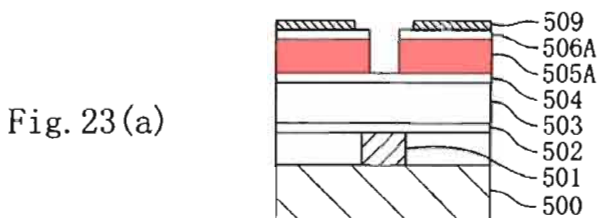
101. I believe a person of ordinary skill in the art would have understood that in the sixth embodiment, “the silicon dioxide film 604 is dry-etched using the patterned second organic film 605A as a mask, thereby forming a patterned silicon dioxide film 604A having openings for forming contact holes as shown in FIG. 32(a).” (’696 patent at 29:1–5.)

102. I believe a person of ordinary skill in the art would have understood that in the modified sixth embodiment, “the silicon dioxide film 654 is dry-etched using the patterned second organic film 655A as a mask, thereby forming a



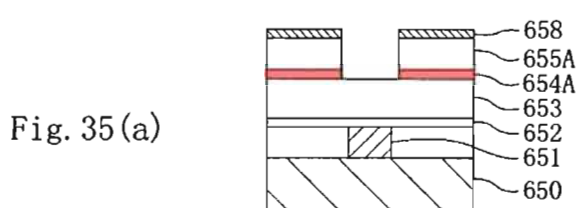
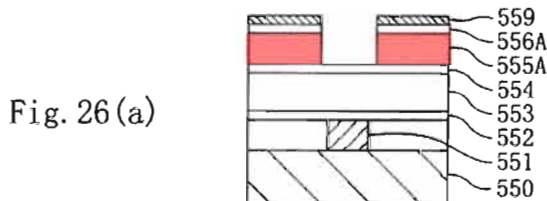
patterned silicon dioxide film 654A having openings for forming contact holes as shown in FIG. 35(a).” (’696 patent at 31:7–11.)

103. Figures 23(a), 26(a), 28(a), 32(a), and 35(a) from the ’696 patent showing step i) appear below. (’696 patent at 23:47–51, 25:66–26:14, 29:1–5, 31:7–11, Figs. 23(a), 26(a), 28(a), 32(a), 35(a).)



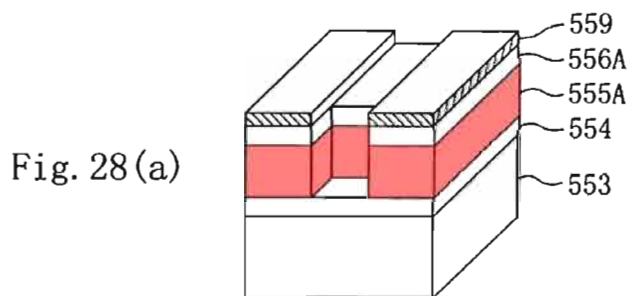
*Fifth Embodiment*

*Sixth Embodiment*



*Modified Fifth Embodiment*

*Modified Sixth Embodiment*



*Modified Fifth Embodiment*

104. Step j) of claim 13 recites “dry-etching the patterned third insulating film [506A, 556A, 605A, 655A] and the first insulating film [504, 554, 603, 653] using the mask pattern [509, 559, 608, 658] and the patterned second insulating film [505A, 555A, 604A, 654A] as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively.”

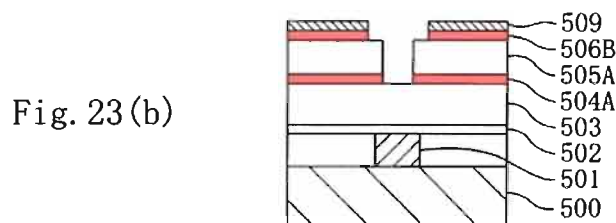
105. I believe a person of ordinary skill in the art would have understood that in the fifth embodiment, “the patterned second silicon dioxide film 506A and the first silicon dioxide film 504 are dry-etched using the mask pattern 509 and the patterned second organic film 505A as respective masks, thereby forming a patterned second silicon dioxide film 506B having openings for forming wiring grooves and a patterned first silicon dioxide film 504A having openings for forming contact holes as shown in FIG. 23(b).” (’696 patent at 23:66–24:6.)

106. I believe a person of ordinary skill in the art would have understood that in the modified fifth embodiment, “the patterned second silicon dioxide film 556A and the first silicon dioxide film 554 are dry-etched using the mask pattern 559 and the patterned second organic film 555A as respective masks, thereby forming a patterned second silicon dioxide film 556B having wiring grooves and a patterned first silicon dioxide film 554A having openings for forming contact holes as shown in FIGS. 26(b) and 28(b).” (’696 patent at 26:15–22.)

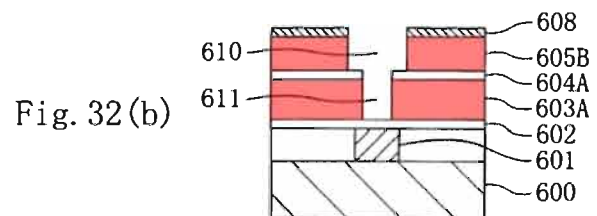
107. I believe a person of ordinary skill in the art would have understood that in the sixth embodiment, “the patterned second organic film 605A and the first organic film 603 are dry-etched using the mask pattern 608 and the patterned silicon dioxide film 604A as respective masks, thereby forming a patterned second organic film 605B having wiring grooves 610 and a patterned first organic film 603A having contact holes 611 as shown in FIG. 32(b).” (’696 patent at 29:6–12.)

108. I believe a person of ordinary skill in the art would have understood that in the modified sixth embodiment, “the patterned second organic film 655A and the first organic film 653 are dry-etched using the mask pattern 658 and the patterned silicon dioxide film 654A as respective masks, thereby forming a patterned second organic film 655B having wiring grooves 660 and a patterned first organic film 653A having contact holes 661 as shown in FIG. 35(b).” (’696 patent at 31:12–18.)

109. Figures 23(b), 26(b), 28(b), 32(b), and 35(b) from the ’696 patent showing step j) appear below. (’696 patent at 23:66–24:6, 26:15–29, 29:6–12, 31:12–18, Figs. 23(b), 26(b), 28(b), 32(b), 35(b).)



*Fifth Embodiment*



*Sixth Embodiment*

Fig. 26 (b)

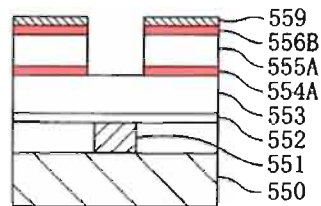
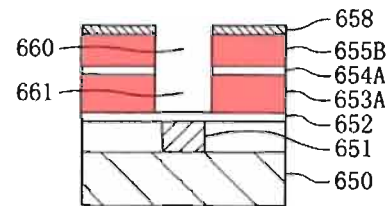


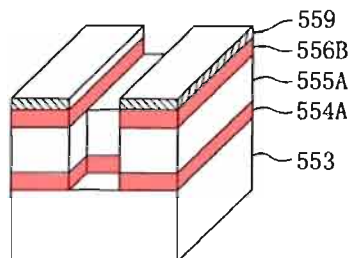
Fig. 35 (b)



***Modified Fifth Embodiment***

***Modified Sixth Embodiment***

Fig. 28 (b)



***Modified Fifth Embodiment***

110. Step k) of claim 13 recites “filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects [513, 563, 612, 662] and contacts [514, 564, 613, 663] connecting the lower- and upper-level metal interconnects together.”

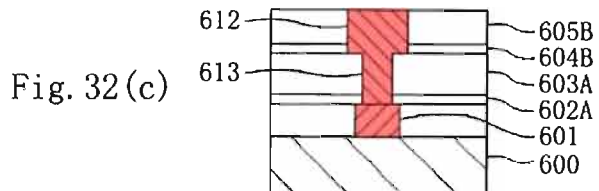
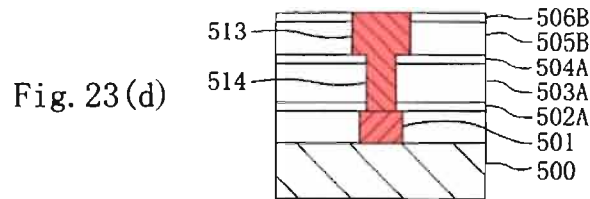
111. I believe a person of ordinary skill in the art would have understood that in the fifth embodiment, “a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 512 and the wiring grooves 511.” (’696 patent at 24:22–24.) “As a result, second metal interconnects 513 and contacts 514, connecting the first and second metal interconnects 501 and 513 together, are formed.” (’696 patent at 24:33–35, Fig. 23(d).)

112. I believe a person of ordinary skill in the art would have understood that in the modified fifth embodiment, “a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 562 and the wiring grooves 561.” (’696 patent at 26:38–41.) “As a result, second metal interconnects 563 and contacts 564, connecting the first and second metal interconnects 551 and 563 together, are formed.” (’696 patent at 26:44–47, Fig. 26(d).)

113. I believe a person of ordinary skill in the art would have understood that in the sixth embodiment, “a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 611 and the wiring grooves 610.” (’696 patent at 29:24–26.) “As a result, second metal interconnects 612 and contacts 613, connecting the first and second metal interconnects 601 and 612 together, are formed.” (’696 patent at 29:35–38, Fig. 32(c).)

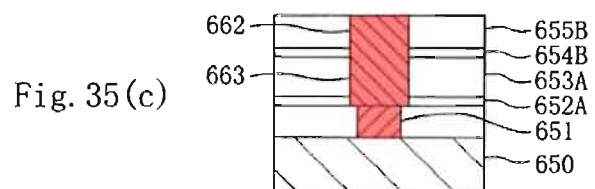
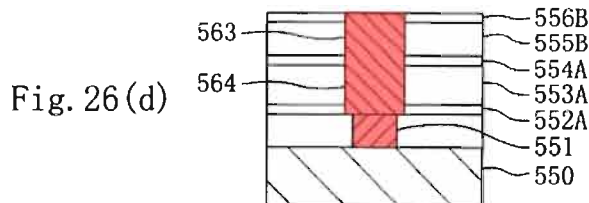
114. I believe a person of ordinary skill in the art would have understood that in the modified sixth embodiment, “a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 661 and the wiring grooves 660.” (’696 patent at 31:30–32.) “As a result, second metal interconnects 662 and contacts 663, connecting the first and second metal interconnects 651 and 662 together, are formed.” (’696 patent at 31:41–44, Fig. 35(c).)

115. Figures 23(d), 26(d), 32(c), and 35(c) from the '696 patent showing step k) appear below. ('696 patent at 24:22–24, 26:30–47, 29:24–39, 31:19–44, Figs. 23(d), 26(d), 32(c), 35(c).)



***Fifth Embodiment***

***Sixth Embodiment***



***Modified Fifth Embodiment***

***Modified Sixth Embodiment***

## 2. Claim 15

116. Claim 15 depends from claim 13 and further recites that “a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.”

117. I believe a person of ordinary skill in the art would have understood that in the fifth embodiment, “as shown in FIG. 22(b), second resist pattern 510, having openings for forming contact holes, is formed by lithography on the mask

pattern 509.” (’696 patent at 23:40–42, Fig. 22(b).) A person of ordinary skill in the art would have understood that the opening in the second resist pattern 510 is the designed size of the contact holes. A person of ordinary skill in the art would have understood that Figure 22(b) shows the width of this designed size of the contact holes to be smaller than the width of the wiring groove in mask pattern 509.

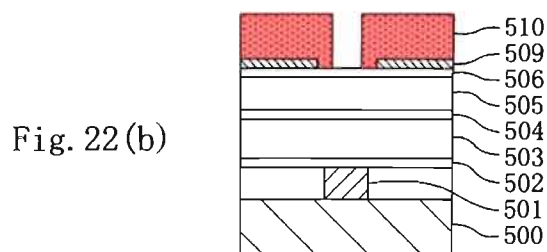
118. I believe a person of ordinary skill in the art would have understood that in the modified fifth embodiment, “the sizes of the openings of the second resist pattern 560 for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to wiring grooves for forming second metal interconnects.” (’696 patent at 25:42–46, 25:26–65, 26:12–60, Figs. 25(b), 27(b), 36, 37(a).)

119. I believe a person of ordinary skill in the art would have understood that in the sixth embodiment, “as shown in FIG. 31(b), second resist pattern 609, having openings for forming contact holes, is formed by lithography on the mask pattern 608.” (’696 patent at 28:49–51, Fig. 31(b).) A person of ordinary skill in the art would have understood that the opening in the second resist pattern 609 is the designed size of the contact holes. A person of ordinary skill in the art would have understood that Figure 31(b) shows the width of this designed size of the

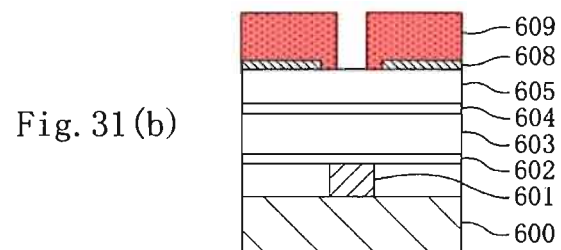
contact holes to be smaller than the width of the wiring groove in mask pattern 609.

120. I believe a person of ordinary skill in the art would have understood that in the modified sixth embodiment, “the sizes of the openings of the second resist pattern 659 for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to the wiring grooves for forming second metal interconnects.” (’696 patent at 30:52–56, 31:49–32:6, Figs. 34(b), 27(b), 36, 37(a).)

121. I therefore believe that a person of ordinary skill in the art would have understood that claim 15 reads on the modified fifth and modified sixth embodiments of the ’696 patent, but not the fifth or sixth embodiments. Figures 22(b), 25(b), 31(b), 34(b), and 27(b) from the ’696 patent showing claim 15 appear below. (’696 patent at 23:40–42, 25:26–65, 26:12–60, 28:49–51, 30:52–56, 31:49–32:6, Figs. 22(b), 25(b), 31(b), 34(b), 27(b), 36, 37(a).)



*Fifth Embodiment*



*Sixth Embodiment*



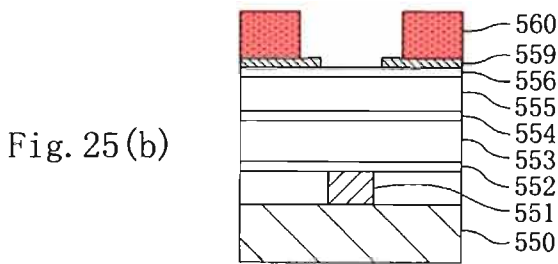
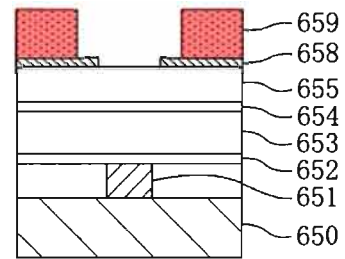


Fig. 25(b)

Fig. 34(b)



*Modified Fifth Embodiment*

*Modified Sixth Embodiment*

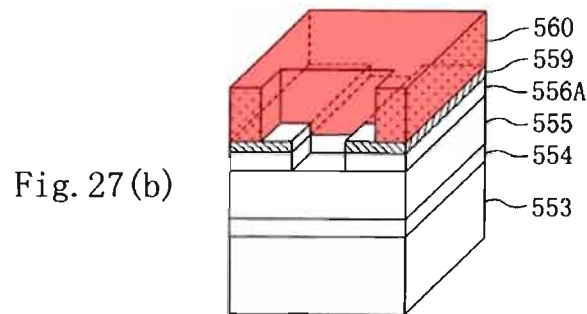


Fig. 27(b)

*Modified Fifth Embodiment*

**B. Japanese Patent Application No. 10-079371 does not disclose many elements of claims 13 and 15**

122. In my opinion, a person of ordinary skill in the art would not have understood the '371 application to disclose all of the limitations of the challenged claims.

123. In my opinion, the '371 application only describes the first, second, third, modified third, and fourth embodiments of the '696 patent. (Compare '371 application at ¶¶0028–0062, Figs. 1(a)–8(c), with '696 patent at 10:22–14:56, Figs. 1(a)–8(c); compare '371 application at ¶¶0063–0074, Figs. 9(a)–11(c), with '696 patent at 14:58–16:38, Figs. 9(a)–11(c); compare '371 application at ¶¶0075–0088,

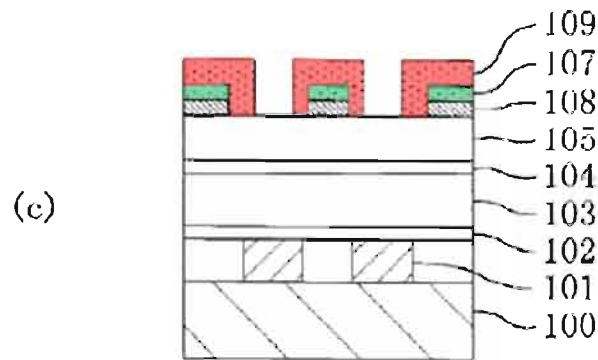
Figs. 12(a)–14(c), with '696 patent at 16:39–18:58, Figs. 12(a)–14(c); compare '371 application at ¶¶0089–0102, Figs. 15(a)–17(c), with '696 patent at 18:59–20:49, Figs. 15(a)–17(c); compare '371 application at ¶¶0103–0115, Figs. 18(a)–20(c), with '696 patent at 20:51–22:44, Figs. 18(a)–20(c).)

124. The '371 application does not include Figures 21(a)–37(b) or claims 13 and 15, which relate to the fifth, modified fifth, sixth, and modified sixth embodiments of the '696 patent. ('371 application at [Claim 1]–[Claim 9], [Figure 1]–[Figure 20].) As explained above, these claims are directed to the fifth, modified fifth, sixth, and modified sixth embodiments of the '696 patent. In my opinion, these claims do not cover any of the first, second, third, variant of the third, and fourth embodiments of the '371 application. The related descriptions, figures, and claims directed to the fifth, modified fifth, sixth, and modified sixth embodiments were newly added in Japanese Patent Application No. 11-075519 (“the '519 application”) and the application for the '696 patent. (Compare '519 application at [Claim 9]–[Claim 15], ¶¶0124–0201; File History of the '696 patent at 125–49, 154–58.)

125. In my opinion, a person of ordinary skill in the art would have understood that the first, second, and fourth embodiments of the '371 application do not disclose step g) of claim 13.

126. Step g) of claim 13 recites, “removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes.”

127. In my opinion, person of ordinary skill in the art would have understood that the first, second, and fourth embodiments of the '371 application do not disclose “removing the first resist pattern and then forming a second resist pattern.” The '371 application states the opposite. It explicitly states that “the second resist pattern 109 is formed without removing the first resist pattern 107.” ('371 application at ¶0043, Fig. 1(c); '696 patent at 11:13–16, Fig. 1(c).) The same is equally true of the other variations of the first embodiment and the second and fourth embodiments. ('371 application at ¶¶0050, 0056, 0068, 0107, Figs. 5(a), 7(a), 9(c), 18(c); '696 patent at 13:5–8, 13:60–63, 15:38–41, 21:30–33, Figs. 5(a), 7(a), 9(c), 18(c).) Figure 1(c) of the '371 application, which, in my opinion, a person of ordinary skill in the art would have understood shows the formation of the second resist pattern (red) without removing the first resist pattern (green), appears below. Figures 5(a), 7(a), 9(c), and 18(c) of the '371 application show the same.



128. In my opinion, a person of ordinary skill in the art would have understood that the third, variant of the third, and fourth embodiments of the '371 application do not disclose step h) of claim 13.

129. Step h) of claim 13 recites “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

130. In my view, to map the third embodiment of the '371 application to claim 13, the third insulating film would have to be either layer 304 or layer 305. Otherwise, the claimed layer stacking sequence would not be possible.

131. The third embodiment of the '371 application states that “the second organic constituent-incorporated silicon dioxide film 305, the low-dielectric-constant SOG film 304 and the first organic constituent-incorporated silicon dioxide film 303 are sequentially dry-etched using the second resist pattern 309 as a mask.” ('371 application at ¶0079, Fig. 13(b).) Thus, in my opinion, the mask pattern 308 is not disclosed as a mask for this step.

132. In my view, to map the variant of the third embodiment of the '371 application to claim 13, the third insulating film would also have to be layer 355. Otherwise, a person of ordinary skill in the art would have understood that step j) of claim 13 would not be met.

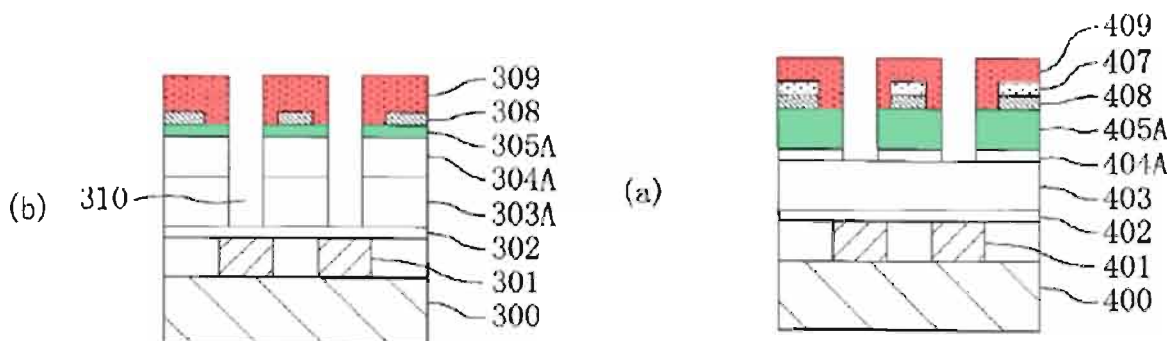
133. The variant of the third embodiment of the '371 application states that “the second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask.” ('371 application at ¶0093, Fig. 16(b).) In my opinion, the mask pattern 358 is not disclosed as a mask for this step.

134. In my view, to map the fourth embodiment of the '371 application to claim 13, the third insulating film would also have to be layer 405. Otherwise, a person of ordinary skill in the art would have understood that step j) of claim 13 would not be met.

135. The fourth embodiment of the '371 application states that “the second low-dielectric-constant SOG film 405 and the organic constituent-incorporated silicon dioxide film 404 are sequentially dry-etched using the second resist pattern 409 as a mask.” ('371 application at ¶0107, Fig. 19(a).) In my opinion, the mask pattern 408 is not disclosed as a mask for this step.

136. Accordingly, in my opinion, a person of ordinary skill in the art would have understood that the third, variant of the third, and fourth embodiments of the

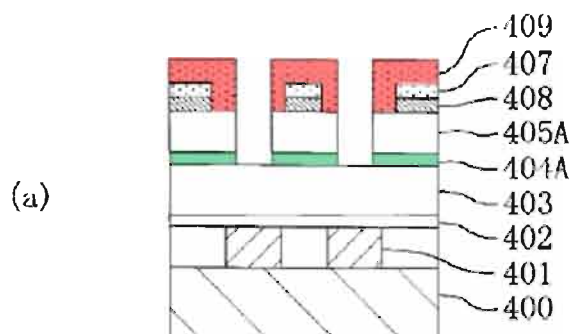
'371 application do not disclose step i) of claim 13. This is shown below in Figures 13(b) and 19(a) of the '371 application.



137. Step i) of claim 13 similarly recites, “dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes.”

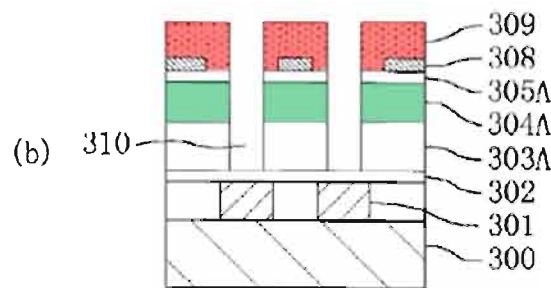
138. In my opinion, a person of ordinary skill in the art would have understood that the fourth embodiment fails to teach “dry-etching the second insulating film using the patterned third insulating film as a mask.” In the fourth embodiment of the '371 application, the second insulating film [404] is etched using the second resist pattern [409] as a mask, as shown in Fig. 19(a), reproduced below. ('371 application at ¶0107, Fig. 19(a).) The '371 application states that “the second low-dielectric-constant SOG film 405 and the organic constituent-incorporated silicon dioxide film 404 are sequentially dry-etched using the second resist pattern 409 as a mask.” ('371 application at ¶0107, Fig. 19(a).) In my

opinion, patterned second low-dielectric-constant SOG 405A is not disclosed as a mask for this step.



139. In my opinion, a person of ordinary skill in the art would have understood that the third and variant of the third embodiments also fail to disclose all the limitations of claim 13. Like the fourth embodiment, they do not disclose at least “dry-etching the second insulating film using the patterned third insulating film as a mask.” In my opinion, both the third and variant of the third embodiments etch the second insulating film [304, 354] using the second resist pattern [309, 359] as a mask, as shown in Fig. 13(b) below. In the third embodiment of the ’371 application, “[T]he second organic constituent-incorporated silicon dioxide film 305, the low-dielectric-constant SOG film 304 and the first organic constituent-incorporated silicon dioxide film 303 are sequentially dry-etched using the second resist pattern 309 as a mask.” (’371 application at ¶0079, Fig. 13(b).) In the variant of the third embodiment, “[T]he second silicon dioxide film 355 and the organic film 354 are sequentially dry-

etched using the second resist pattern 359 as a mask.” (’371 application at ¶0093, Fig. 16(b).) In my opinion, the patterned second organic constituent-incorporated silicon dioxide film 305A is not disclosed as a mask during this etch step. (’371 application at ¶0079.) Additionally, it is my opinion that the patterned second silicon dioxide film 355A is not disclosed as a mask during this etch step. (’371 application at ¶0093.)



140. Because of these deficiencies at least, it is my opinion that a person of ordinary skill in the art would not have found the ’371 application to adequately describe the Challenged Claims.

### **VIII. Level of Ordinary Skill in the Art**

141. In determining the qualifications of a person of ordinary skill in the art, I have been told that factors to consider in determining the level of ordinary skill in the art may include type of problems encountered in the art, solutions to those problems in the art, speed with which innovations are made in the art, the sophistication of the technology and the educational level of active workers in the field. The field of semiconductors and interconnects is fast-moving and the



technology is very sophisticated, so based on my experience in this field when the '696 application was filed, such a person would have had (1) the equivalent of a Master of Science degree from an accredited institution in electrical engineering, materials science, physics, or the equivalent; (2) a working knowledge of semiconductor processing technologies for integrated circuits; and (3) at least two years of experience in related semiconductor processing analysis, design, and development. Additional graduate education could substitute for professional experience, and significant work experience could substitute for formal education.

#### **IX. Claim Construction**

142. I have been told that in district court, claim terms are given their ordinary and accustomed meaning as understood by a person of ordinary skill in the art as of the applicable priority date. I have also been told that a claim in an unexpired patent in *inter partes* review generally receives the “broadest reasonable construction in light of the specification of the patent in which it appears.” I have used these guidelines in explaining how a person of ordinary skill in the art would interpret any contested claims.

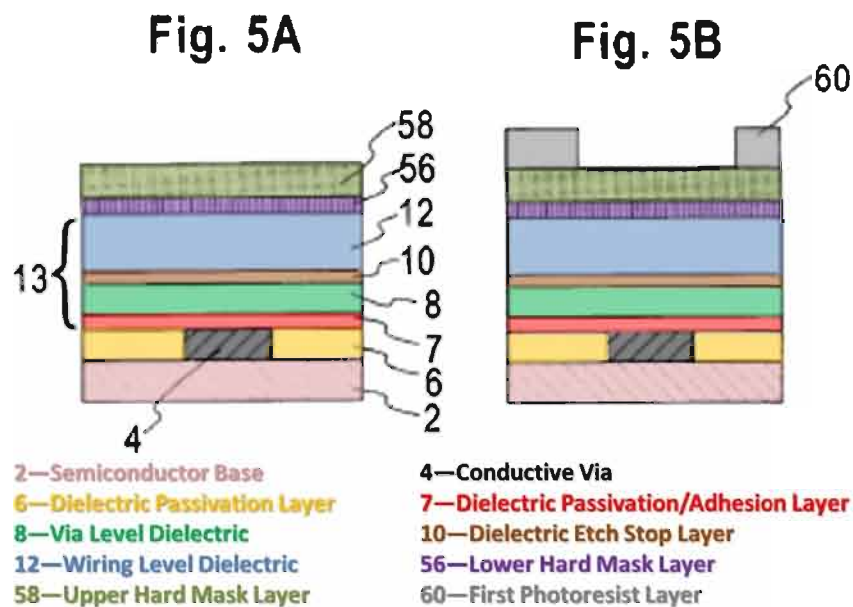
#### **X. Analysis**

143. Based on my personal experience at the time and my review of the prior art, it is my opinion that the methods claimed by the '696 patent were known in the art.

**A. Grill (U.S. Patent No. 6,140,226)**

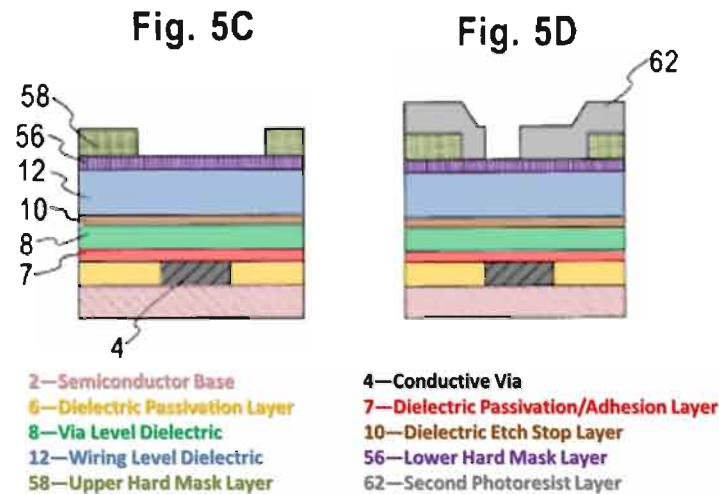
144. *Grill* discloses “methods to fabricat[e] multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels.” (*Grill* at Abstract, 7:16–30.).

145. In one embodiment, the structure of Fig. 5A is formed first, followed by patterning a first photoresist layer [60], as shown in Fig. 5B. (*Grill* at 7:30–44.) As a person of ordinary skill in the art would have understood, this photolithography defines what will become the wiring (i.e., trench) level of the interconnection.

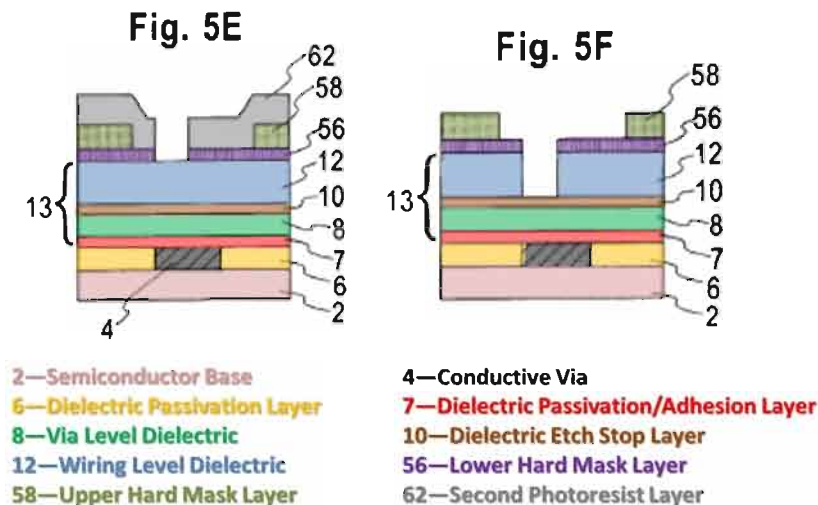


146. Next, an etch transfers the photoresist pattern [60] into the upper hard mask layer [58], as shown in Fig. 5C. (*Grill* at 7:45–50.) The first layer of

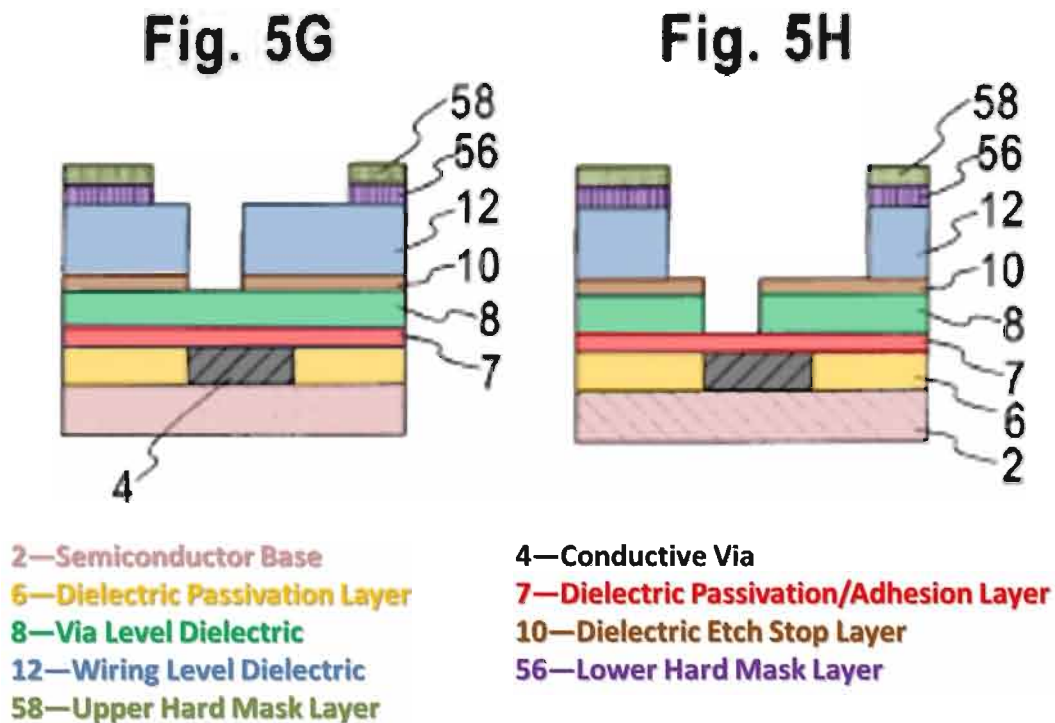
photoresist [60] is then removed, and a second layer of photoresist [62] is patterned to define what will become the via (i.e., contact) level of the interconnection, as shown in Fig. 5D. (*Grill* at 7:51–55.)



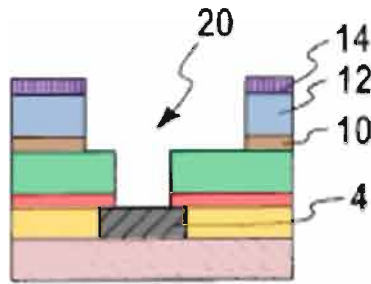
147. As shown in Figure 5E, the next step is an etch to transfer the photoresist pattern [62] into the lower hard mask layer [56]. (*Grill* at 7:57–61.) This pattern is then transferred into layer [12] by another etch, which also removes the second photoresist layer [62] (as shown in Fig. 5F). (*Grill* at 7:62–66.)



148. Another etch is then performed to remove the exposed portions of both the lower hard mask [56] and etch stop layer [10], as shown in Figure 5G. (*Grill* at 7:67–8:2.) A further etch removes the exposed portions of dielectric layers 8 and 12, as shown in FIG. 5H. (*Grill* at 8:2–5.) A final etch removes the exposed portions of dielectric layer 7, which may also remove the exposed portions of the etch stop [10] to form the dual-relief cavity of Fig. 1J. (*Grill* at 4:61–64, 8:5–8.)



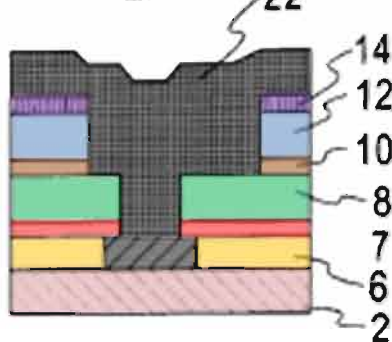
**Fig. 1J**



- |                                |   |
|--------------------------------|---|
| 2—Semiconductor Base           | 4—Conductive Via                        |
| 6—Dielectric Passivation Layer | 7—Dielectric Passivation/Adhesion Layer |
| 8—Via Level Dielectric         | 10—Dielectric Etch Stop Layer           |
| 12—Wiring Level Dielectric     | 56—Lower Hard Mask Layer                |
| 58—Upper Hard Mask Layer       |   |

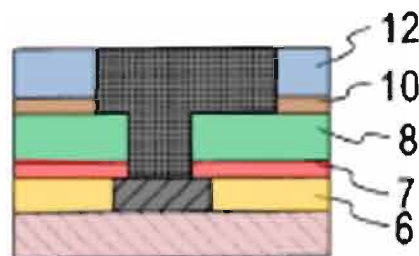
149. The cavity is filled with conductive material [22], as shown in Fig. 1K, and planarized by a chemical-mechanical polishing (CMP) process, as shown in Figure 1L. (*Grill* at 4:64–5:8, 8:5–8.) Hard mask 14 (which is analogous to lower hard mask 56 and upper hard mask 58) may remain in the final structure even though not shown in Figure 1L. (*Grill* at 5:5–8.)

**Fig. 1K**



- |                                |
|--------------------------------|
| 2—Semiconductor Base           |
| 6—Dielectric Passivation Layer |
| 8—Via Level Dielectric         |
| 12—Wiring Level Dielectric     |
| 22—Wiring Level                |

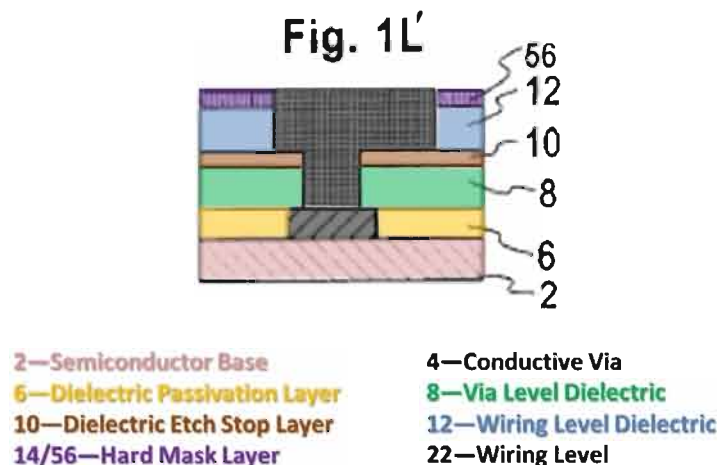
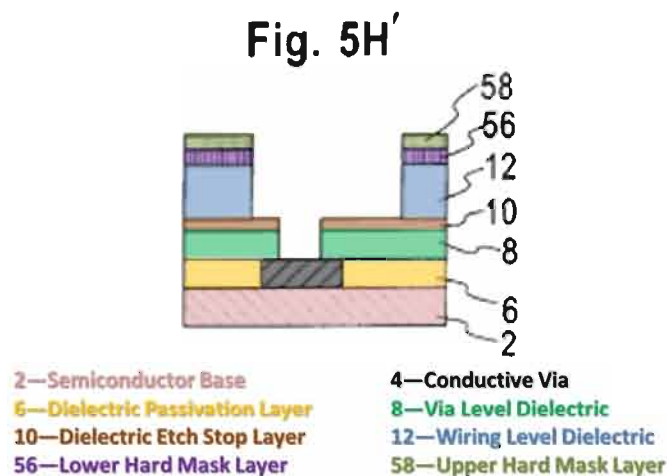
**Fig. 1L**



- |   |
|---|
| 4—Conductive Via                        |
| 7—Dielectric Passivation/Adhesion Layer |
| 10—Dielectric Etch Stop Layer           |
| 14/56—Hard Mask Layer                   |

150. This is the only illustration of the described embodiment. *Grill* also states that layer 7 is optional, as is etch stop layer 10. (*Grill* at 4:1–5, 4:61–63.)

Modified Figures 5H' and 1L'<sup>1</sup> below illustrate how I believe a person of ordinary skill in the art would understand the alternative embodiment in which optional layer 7 is not used.



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<sup>1</sup> The prime or apostrophe in a figure number means it is one that is modified slightly from the corresponding patent.

151. In this alternative embodiment without optional layer 7, the etching step of Figure 1J (*Grill* at 4:61–64) is unnecessary because the conductive via is opened during the etch step of Figure 5H'. A person of ordinary skill in the art would have understood that etch stop 10 is a very thin layer that does not contribute significantly to the RC time constant (the product of the circuit line resistance and capacitance) of the resulting circuit interconnect if it is left in place. Thus, there is no need to etch layer 10 for purposes to reduce the RC time constant of the interconnect. Furthermore, a person of ordinary skill in the art would have understood that etching etch stop layer 10 with the conductive via exposed could damage the underlying conductive via. Accordingly, a person of ordinary skill in the art would have known that it was preferable not to perform the etch step of Figure 1J when optional layer 7 is not present.<sup>2</sup>

152. Additionally, a hard mask layer is shown in Figure 1L' above, which *Grill* teaches is an option. (*Grill* at 5:5–8.) A person of ordinary skill in the art would have understood that this allows the hard mask to serve as an etch stop during CMP, thereby protecting the trench level low-k dielectric layer.

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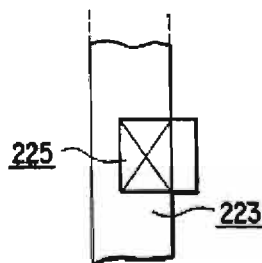
<sup>2</sup> Alternatively, even if the optional passivation/adhesion layer [7] is used, a person of ordinary skill in the art would have understood that in many cases it is desirable not to etch the etch stop layer [10] when the passivation/adhesion layer [7] is etched. (*Zhao*, 6:25–29, 6:62–7:2, 7:15–18, 7:55–65, Fig. 10.)

153. It is also my opinion that at least claim 28 of *Grill* is supported by its provisional application, U.S. Provisional Patent Application No. 60/071,628, as detailed in Appendix B. The disclosures of the '628 application that demonstrate the unpatentability of the challenged claims are at pages 1–4, 6, and 7 and Figures 5A–5H, 1J–1L of the '628 application.

**B. *Aoyama* (U.S. Patent No. 5,592,024)**

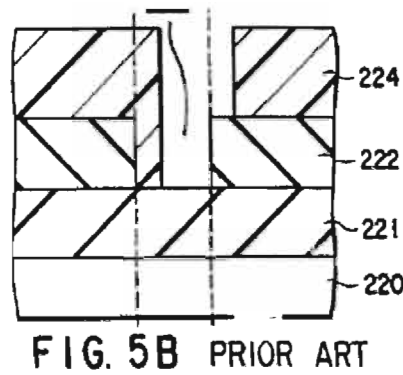
154. *Aoyama* discloses a damascene interconnect formation process in which the opening in the via resist pattern is wider than the wiring groove. (*Aoyama* at 15:48–51, 16:3–5, Figs. 18A–18C, 19A–19B.)

155. *Aoyama* explains a problem relating to photomask misalignment. If the photomask is misaligned when defining the photoresist layer to have the “through-hole” (via) pattern, the via can be smaller than desired and the wiring groove to be wider than desired (at the location of the via). (*Aoyama* at 3:18–21, 3:29–32, Figs. 5B, 5D (shown below).) This leads to an increase in contact resistance, degradation in reliability, and problems for increasing integration density. (*Aoyama* at 3:33–38, 6:7–14.)

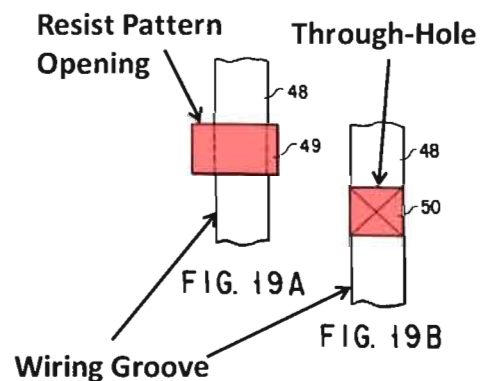
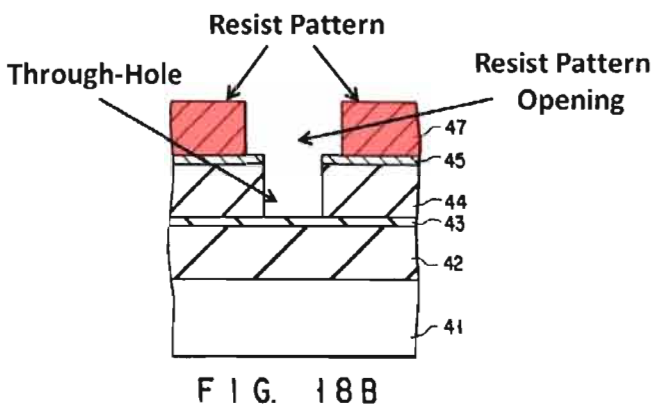


**FIG. 5D PRIOR ART**





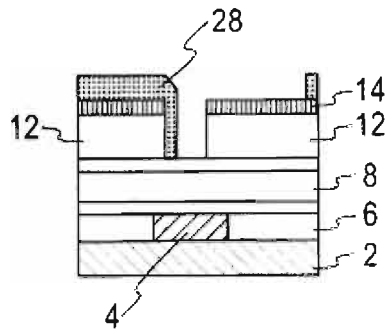
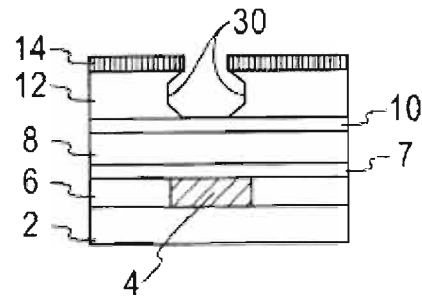
156. *Aoyama* teaches a solution to this problem. *Aoyama* teaches a via resist pattern with a through-hole wider than the wiring groove. (*Aoyama* at 16:3–5, Figs. 18B, 19A (each shown below).) The width of the wiring groove, not the opening in the via level photoresist, then defines the width of the via. (*Aoyama* at Figs. 19A, 19B.) That way, even when some misalignment occurs, the via will have the correct width, as defined by the wiring groove. (*Aoyama* at 16:14–16, Figs. 18B, 19B (shown below).)



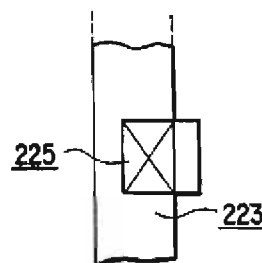
**C. The combination of *Grill* and *Aoyama***

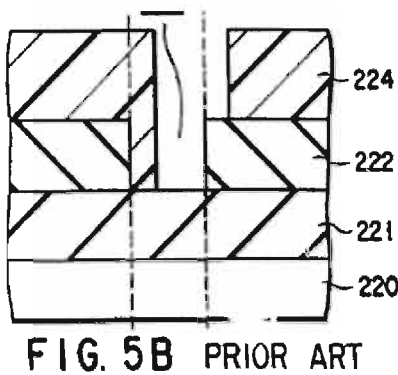
157. In my opinion, the combination of *Grill* and *Aoyama* is very similar to the modified fifth embodiment of the '696 patent. I believe that a person of ordinary skill in the art would have understood that the disclosed embodiment of *Grill* at 4:60–5:8 and 7:16–8:8, without optional layer 7, when combined with the certain teachings of *Aoyama*, meets every limitation of claims 13 and 15 and renders them obvious.

158. *Grill* addresses the problem of “lithographic rework” when the via and wiring patterns are misaligned due photolithography errors. (*Grill* at 2:26–38.) People of ordinary skill in the art understood that organic and other low-k dielectric materials may have similar etch characteristics to photoresist such that stripping a photoresist pattern might damage the underlying dielectric. (*Grill* at 2:26–32.) *Grill* discloses a solution to this problem of using two hard masks on top of the wiring-level dielectric. (*Grill* at 2:64–3:6, Fig. 5A.) This ensures alignment of both via and wiring levels is completed and transferred into the thin films on the surface of the device before the underlying inter-level dielectrics are ever uncovered. (*Grill* at 2:64–3:1.) Figures 2B and 2C of *Grill* below show how stripping misaligned photoresist 28 can damage inter-layer dielectric 12 and make it difficult to control the via dimension. (*Grill* at 5:13–33.)

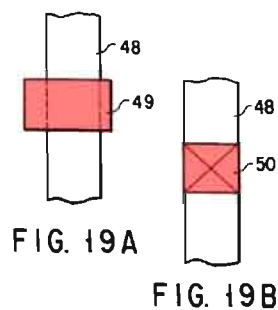
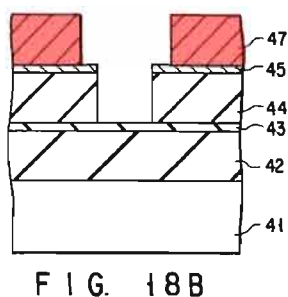
**Fig. 2B****Fig. 2C**

159. *Aoyama* solves a related misalignment problem. People of ordinary skill in the art understood that misalignment of the photomask during via formation can cause the via dimensions to be too small and the wiring dimensions to be too large if the edge of the via pattern overlaps the patterned wiring groove. (*Aoyama* at 3:18–21, 3:29–32.) This is shown in Figures 5B and 5D of *Aoyama* below. (Compare *Aoyama* at Fig. 5B with *Grill* at Fig. 2B.) People of ordinary skill in the art also understood that such misalignment leads to an increase in contact resistance, degradation in reliability, and difficulty in achieving higher integration density. (*Aoyama* at 3:33–38, 6:7–14.)

**FIG. 5D PRIOR ART**



160. *Aoyama* discloses a solution to this misalignment problem. *Aoyama* discloses using a via opening that is wider than the wiring groove. (*Aoyama* at 16:3–5, Figs. 18B, 19A (each shown below).) The added width to the via pattern increases misalignment tolerance, because the width of the via is defined by the width of the wiring groove, not the via pattern. (*Aoyama* at 16:14–16.) Therefore, a via having the same width as the wiring groove is formed even when misaligned. (*Aoyama* at 16:14–16, Figs. 18B, 19B (shown below).)



161. A person of ordinary skill in the art would have understood that *Aoyama* does not completely eliminate the possibility of a misaligned photomask. For example, a wider via opening in the photomask provides increased misalignment tolerance, but it does not guarantee proper alignment. The

misalignment in *Aoyama*'s Figure 5D is still possible even with the wider pattern shown in Figure 19A. The difference is that a greater degree of misalignment is required before the problem occurs. A person of ordinary skill in the art would have understood that the misalignment error explained in *Aoyama* would occur with less frequency but that it could still occur.

162. A person of ordinary skill in the art would have appreciated that *Grill*'s and *Aoyama*'s solutions complement one another in addressing the problem of misalignment in semiconductor damascene processes. When misalignment occurs, *Grill*'s structure enables rework without fear of damaging any of the inter-level dielectrics. (*Grill* at 2:26–38.) Moreover, the wider via pattern of *Aoyama* reduces instances of misalignment, which reduces the need for *Grill*'s rework. Accordingly, a person of ordinary skill in the art would have understood that the combination of *Grill* and *Aoyama* reduces instances of misalignment and permits rework when misalignment occurs.

163. A person of ordinary skill in the art also would have found it obvious that combining *Grill*'s two hard masks with *Aoyama*'s widened via pattern would not require modification of the *Grill* process. A person of ordinary skill in the art also would have understood that nothing about the width of the via pattern in *Aoyama* affects the dual-hard mask structure of *Grill*, and nothing about the dual-hard mask structure of *Grill* affects the width of the via pattern in *Aoyama*. The

via-level mask pattern and the dual hard mask structure are independent but easily and obviously combinable.

164. Again, a person of ordinary skill in the art would have understood that the combination of *Aoyama* and *Grill* predictably reduces instances of misalignment and permits lithographic rework when misalignment does occur. A person of ordinary skill in the art would have understood that combination of *Grill* and *Aoyama* therefore avoids the problems of increased contact resistance, degraded reliability, and damaged inter-layer dielectrics, and lower integration density. (*Grill* at 2:26–38, 2:64–3:6, 5:13–33; *Aoyama* at 3:33–38, 6:7–14.)

165. In my opinion, the combination of *Grill* and *Aoyama* is a combination of familiar elements according to known methods to yield predictable results. It is also my opinion that the combination of *Grill* and *Aoyama* constitutes the use of known techniques to improve similar devices, methods, or products in the same way. It is also my opinion that the combination of *Grill* and *Aoyama* constitutes an application of known techniques to known devices, methods, or products ready for improvement to yield predictable results.

**D. *Grill* and Claim 13**

166. The preamble of claim 13 recites “[a] method for forming an interconnection structure.”

167. *Grill* is titled “Dual Damascene Processing for Semiconductor Chip Interconnects.” It discloses “methods to fabricat[e] multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels.” (*Grill* at Abstract, 1:12–15, 7:16–30, Fig. 1L; ’696 patent at Abstract, Fig. 3(c).)

168. In view of these disclosures, I believe that a person of ordinary skill in the art would have understood that *Grill* discloses “[a] method for forming an interconnection structure.”

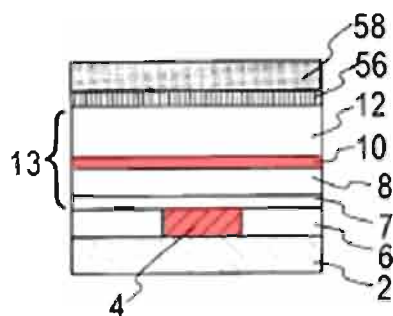
169. Claim 13 recites “forming a first insulating film over lower-level metal interconnects.”

170. *Grill* discloses “dielectric etch stop layer 10,” which “might be a silicon-containing material such as SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, SiO<sub>x</sub>N<sub>y</sub>, SiCOH compounds, silicon-containing DLC (SiDLC), etc.” (*Grill* at 4:1–13.) Based on this disclosure, I believe a person of ordinary skill in the art would have understood that the disclosed etch stop layer [10] is an insulating film. A person of ordinary skill in the art would have understood that all of these dielectric materials are electrical insulators.

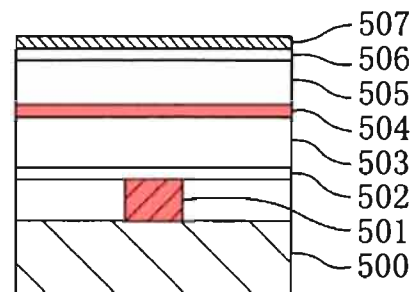
171. Further, *Grill* discloses a “conductive via 4,” which is “formed in the interlevel dielectric to provide interlevel contacts between the wiring traces.”

(*Grill* at 1:25–27, 3:60–67, Fig. 5A.) As shown by Figure 5A below, I believe a person of ordinary skill in the art would have understood that the etch stop [10] is located over the conductive via [4]. (*Grill* at Fig. 5A.) Figure 21(a) from the fifth embodiment of the '696 patent is shown below for comparison.

**Fig. 5A**



**Fig. 21 (a)**



172. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that *Grill* discloses “forming a first insulating film over lower-level metal interconnects.”

173. Claim 13 recites “forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film.”

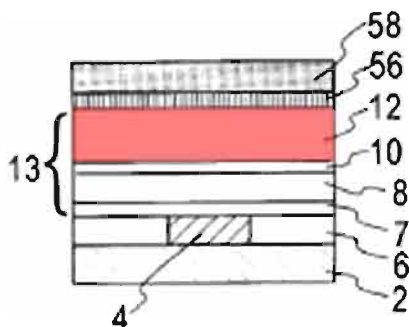
174. *Grill* discloses “via level dielectric 8,” which “might be carbon-based materials such as DLC or fluorinated DLC (FDLC), SiCO or SiCOH compounds, or organic or inorganic polymer dielectrics.” (*Grill* at 4:1–13.) Based on this disclosure, I believe a person of ordinary skill in the art would have understood that the disclosed via level dielectric [8] is an insulating film. A person of ordinary



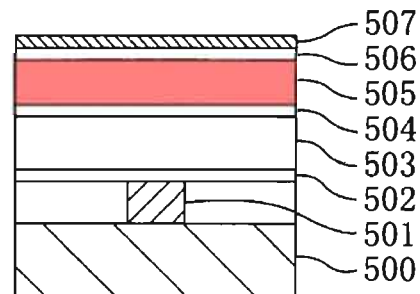
skill in the art would have understood that all of these dielectric materials are electrical insulators.

175. *Grill* also teaches that the etch stop [10] “might be a silicon-containing material such as SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, SiO<sub>x</sub>N<sub>y</sub>, SiCOH compounds, silicon-containing DLC (SiDLC), etc.” *Grill* therefore teaches a wiring level dielectric 12 and etch stop 10 having different compositions (e.g., FDLC and SiO<sub>x</sub>N<sub>y</sub>, respectively). (*Grill* at 4:1–13.) As shown in Figure 5A below, I believe a person of ordinary skill in the art would have understood that the wiring level dielectric [12] is located over the etch stop [10]. (*Grill* at Fig. 5A.) Figure 21(a) from the fifth embodiment of the ’696 patent is shown below for comparison.

**Fig. 5A**



**Fig. 21(a)**



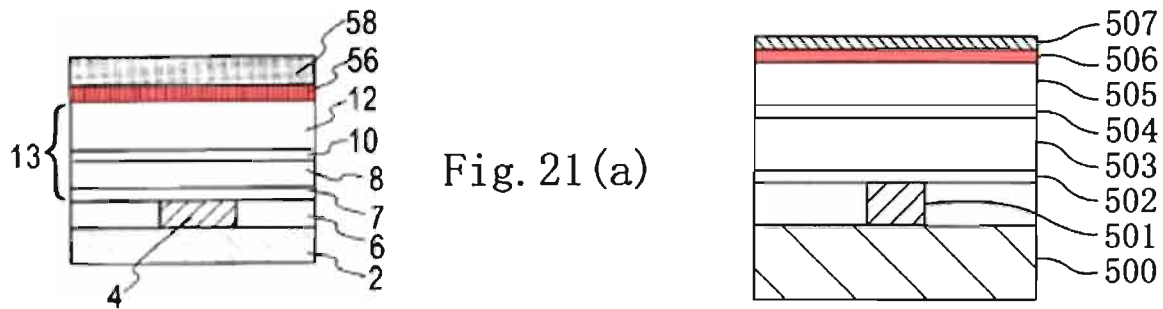
176. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that *Grill* discloses “forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film.”

177. Claim 13 recites “forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film,” which *Grill* teaches.

178. *Grill* discloses “lower hard mask layer 56,” which is “preferably formed from different materials which have different etch properties from . . . the dielectric underlayer[] 12.” (*Grill* at 7:31–35, 4:1–13, 7:38–42.) “[S]uitable hard mask materials may include SiO<sub>2</sub>-based materials, other oxides, nitrides other than Si<sub>3</sub>N<sub>4</sub>, carbon-based dielectrics, SiC-based dielectrics, polycrystalline silicon, amorphous hydrogenated silicon, and metals.” (*Grill* at 7:38–42.) Based on these disclosures, I believe a person of ordinary skill in the art would have understood that the lower hard mask layer [56] is an insulating film having a different composition than the wiring level dielectric [12]. A person of ordinary skill in the art would have understood that many of these materials are electrical insulators.

179. As shown in *Grill*’s Figure 5A below, a person of ordinary skill in the art would have understood that the lower hard mask layer [56] is located over the wiring level dielectric [12]. (*Grill* at, Fig. 5A.) Figure 21(a) from the fifth embodiment of the ’696 patent is shown below for comparison.

**Fig. 5A**



180. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that *Grill* discloses “forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film.”

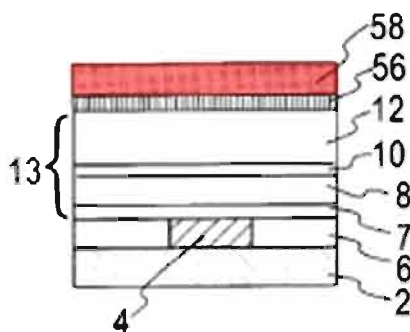
181. Claim 13 recites “forming a thin film over the third insulating film.”

182. *Grill* discloses “upper hard mask layer 58,” which “might be formed from SiO<sub>2</sub>.” (*Grill* at 7:31–35.) “Other suitable hard mask materials may include SiO<sub>2</sub>-based materials, other oxides, nitrides other than Si<sub>3</sub>N<sub>4</sub>, carbon-based dielectrics, SiC-based dielectrics, polycrystalline silicon, amorphous hydrogenated silicon, and metals.” (*Grill* at 7:38–42.) In one example, *Grill* states that the upper hard mask layer “might be formed from a 40 nm thickness of Si<sub>3</sub>N<sub>4</sub>.” (*Grill* at 8:29–31.) I believe a person of ordinary skill in the art would have understood that the upper hard mask layer [58] is a thin film.

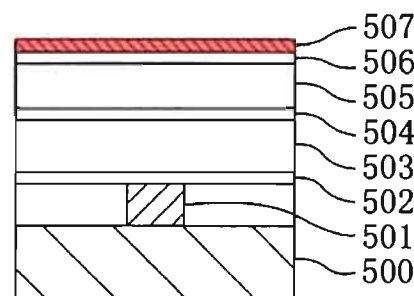
183. As shown in *Grill*’s Figure 5A below, I believe a person of ordinary skill in the art would have understood that the upper hard mask layer [58] is

located over the lower hard mask layer [56]. (*Grill* at Fig. 5A.) Figure 21(a) from the fifth embodiment of the '696 patent is shown below for comparison.

**Fig. 5A**

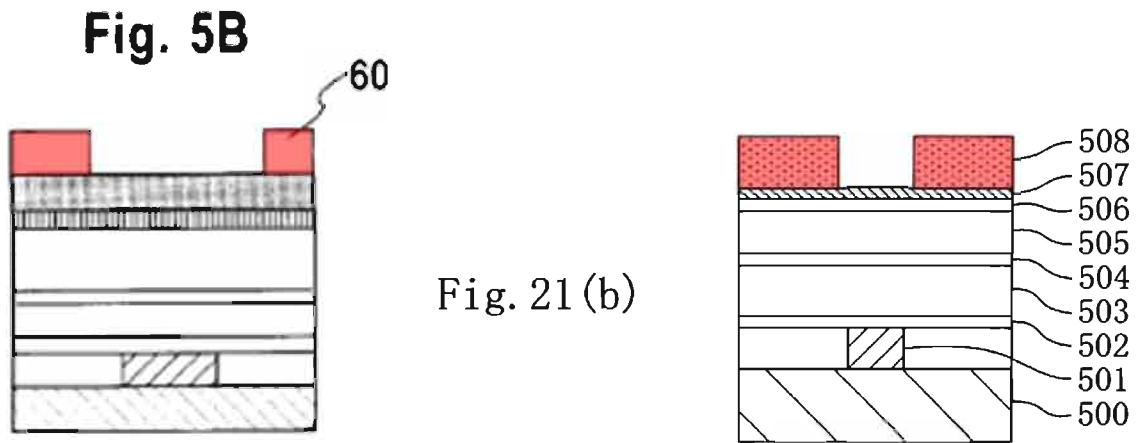


**Fig. 21 (a)**



184. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that *Grill* discloses “forming a thin film over the third insulating film.”

185. Claim 13 recites “forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves.” *Grill* states, “A first resist layer 60, patterned with a first (wiring level) pattern, is formed on layer 58.” (*Grill* at 7:42–44, Fig. 5B.) This is shown in *Grill*’s Figure 5B below. I believe a person of ordinary skill in the art would have understood the first resist layer [60] is located on the upper hard mask layer [58], and its opening corresponds to a wiring groove (i.e., *Grill*’s “wiring level” pattern). Figure 21(b) from the fifth embodiment of the '696 patent is shown below for comparison.

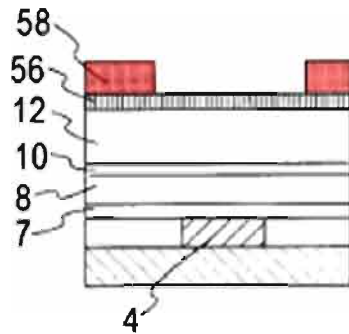


186. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that *Grill* discloses “forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves.”

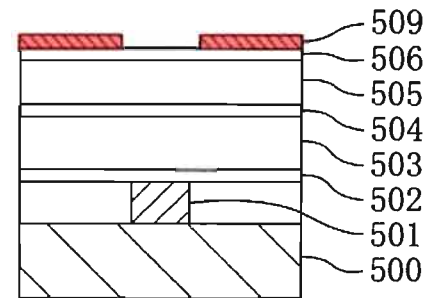
187. Claim 13 recites “etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves.”

188. *Grill* states that “[t]he pattern of resist layer 60 [i.e., the wiring level pattern] is transferred into upper hard mask layer 58 by an etching process.” (*Grill* at 7:42–47, Fig. 5C.) *Grill*’s Figure 5C below shows this. A person of ordinary skill in the art would have understood that the resist layer [60] masks the upper level hard mask [58] and that the aperture of the openings in upper level hard mask [58] correspond to the wiring grooves (i.e., *Grill*’s “wiring level” pattern). Figure 22(a) from the fifth embodiment of the ’696 patent is shown below for comparison.

**Fig. 5C**



**Fig. 22(a)**

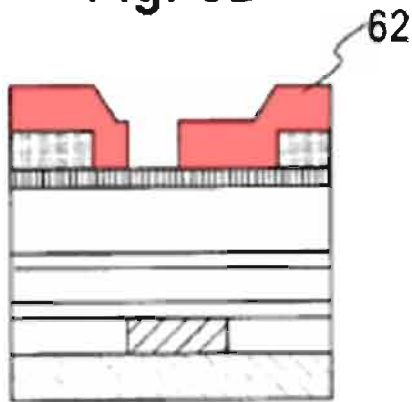


189. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that *Grill* discloses “etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves.”

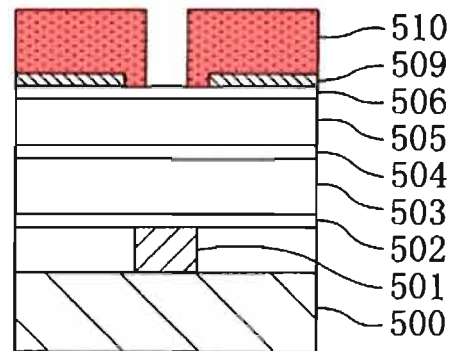
190. Claim 13 recites “removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes.”

191. *Grill* states that “[p]atterned resist layer 60 is then removed by a process such as ashing or wet chemical etching, and a second resist layer 62, patterned with a second (via level) pattern, is then formed on the structure.” (*Grill* at 7:51–55, Fig. 5D.) *Grill*’s Figure 5D shows this below. I believe a person of ordinary skill in the art would have understood that the second resist layer [62] is formed on both the lower hard mask layer [56] and the mask pattern [58]. (*Grill* at 7:51–55, Fig. 5D) Figure 22(b) from the fifth embodiment of the ’696 patent is shown below for comparison.

**Fig. 5D**



**Fig. 22 (b)**

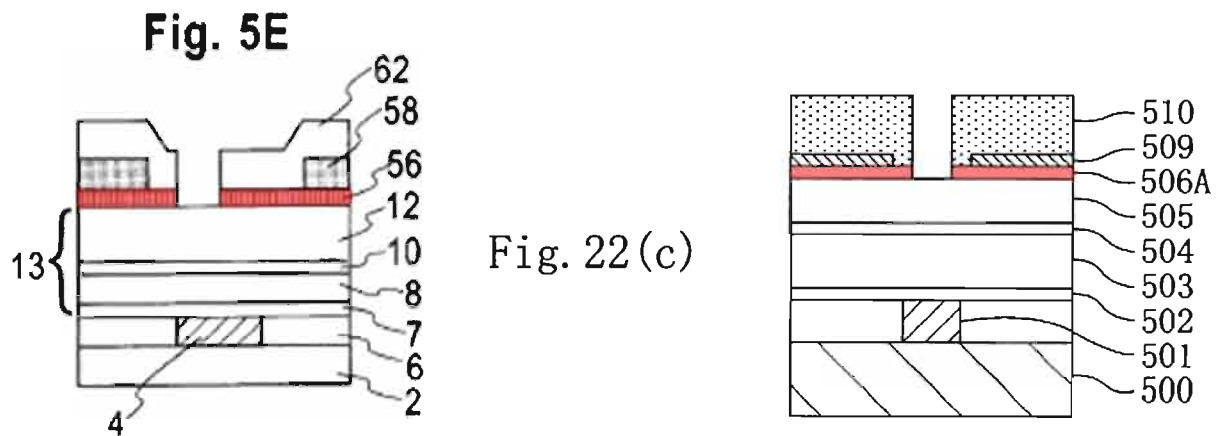


192. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that *Grill* discloses “removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes.”

193. Claim 13 recites “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

194. *Grill* states, “The pattern of resist layer 62 [i.e., the via level pattern] is then transferred into lower hard mask layer 56.” (*Grill* at 7:57–61, Fig. 5E.) *Grill*’s Figure 5E below shows this. Based on the description in the ’696 patent, I believe a person of ordinary skill in the art would have understood that the resist layer [62] and the upper level hard mask [58] mask the lower hard mask [56] during etching in the manner described in the ’696 patent. Figure 5E of *Grill* is shown below to illustrate this disclosure. *Grill*’s disclosure is identical to the fifth

embodiment of the '696 patent in this regard, which states that “the second silicon dioxide film 506 is dry-etched using the second resist pattern 510 and the mask pattern 509 as a mask, thereby forming a patterned second silicon dioxide film 506A having openings for forming contact holes as shown in FIG. 22(c).” ('696 patent at 23:42–46.) Figure 22(c) from the fifth embodiment of the '696 patent is also shown below for comparison.



195. I also believe that a person of ordinary skill in the art would have understood that the lower hard mask layer [56] has openings for forming contact holes (since it is the via level pattern).

196. Additionally, a person of ordinary skill in the art would have understood that the second resist pattern [62] is transferred into the lower hard mask layer [56] by dry etching. Layer 56 may be  $\text{Si}_3\text{N}_4$ , for example (*Grill* at 7:34–37), and the etch shown in Figures 5D and 5E is anisotropic to preserve the dimensions of the via level pattern (avoiding the problem of Figure 2C, for



example). The silicon nitride film here is not a single-crystal material. It is typically amorphous, meaning that it has no crystalline order. Anisotropic wet etches work by exploiting chemical differences along different directions of a crystal lattice. When no such directionality exists in a material, the wet etch is isotropic. Dry etches, however, tend to be highly directional regardless of the etchant. Thus, a person of ordinary skill in the art would have understood that an anisotropic etch of silicon nitride, as shown in Figures 5D and 5E of *Grill*, would have been a dry etch.

197. Based on these disclosures and the knowledge possessed by a person of ordinary skill in the art, I believe a person of ordinary skill in the art would have understood that *Grill* discloses “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

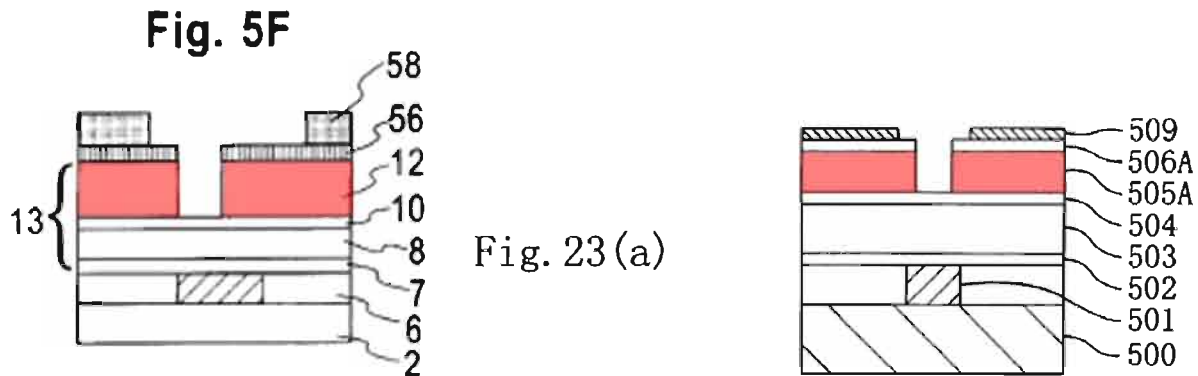
198. Claim 13 recites “dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes.”

199. *Grill* states that “[t]he via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching.” (*Grill* at 7:62–63, Fig. 5F.) A person of ordinary skill in the art would have understood that reactive ion etching (RIE) is a dry etch. “Patterned second resist layer 62 is absent from

FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12.”<sup>3</sup> (*Grill* at 7:64–66.) Lower hard mask [56] acts as a mask as the second resist pattern [62] is removed during the etch process. The fifth, modified fifth, sixth, and modified sixth embodiments of the ’696 patent use the same process. (’696 patent at 23:47–59, 25:66–26:14, 28:49–61, 30:58–31:6, Figs. 23(a), 26(a), 31(c), 34(c).) As shown in *Grill*’s Figure 5F below, I believe a person of ordinary skill in the art would have understood that the wiring level dielectric [12] has openings for forming contact holes (i.e., via level pattern). Figure 23(a) from the fifth embodiment of the ’696 patent is shown below for comparison.

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<sup>3</sup> Even without this express teaching that the resist pattern [62] is typically removed by the etching process used to pattern dielectric 12, I believe that a person of ordinary skill in the art would have understood this to be true. For example, *Grill* teaches that the “interconnect dielectric and the photoresist stencil used to pattern the hard mask [may] have similar etch characteristics,” such as “the case with an organic photoresist and a carbon-based interconnect dielectric such as DLC.” (*Grill* at 2:26–32.)



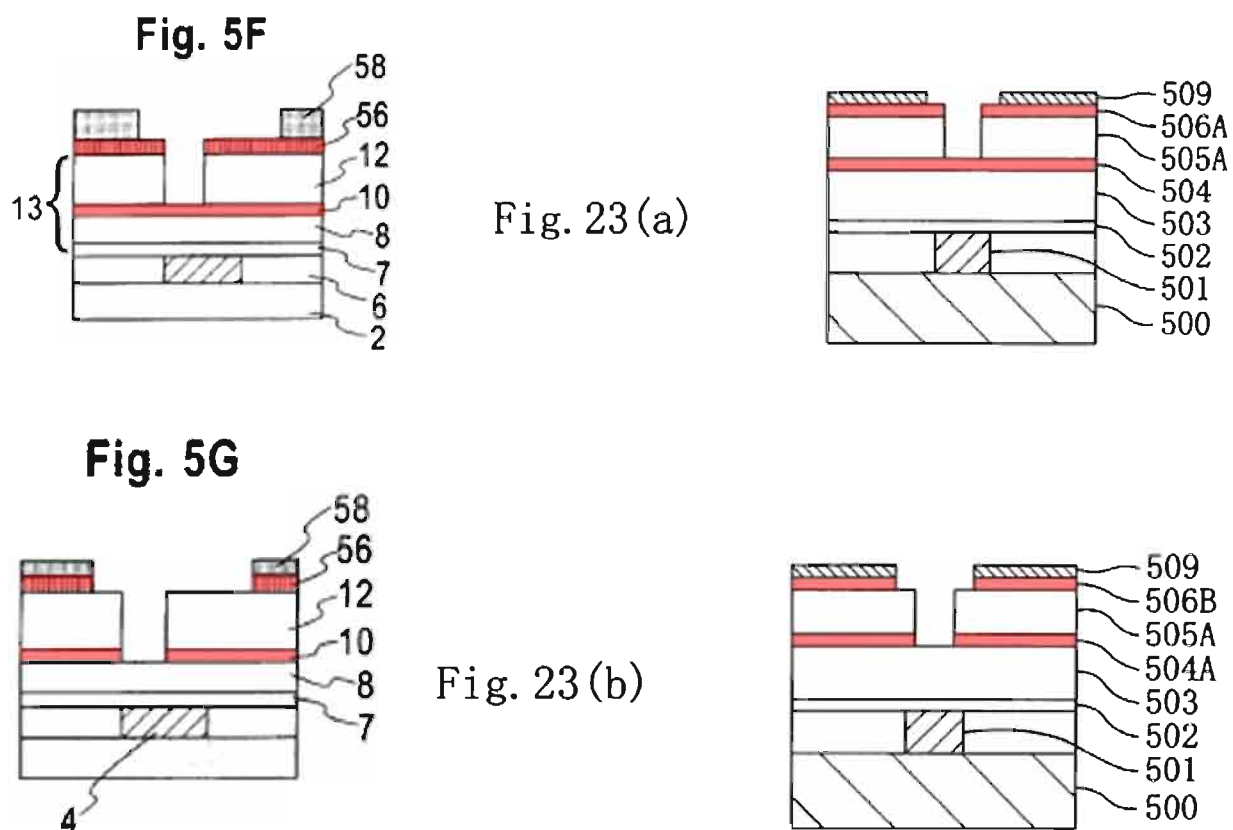
200. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that *Grill* discloses “dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes.”

201. Claim 13 recites “dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively.”

202. *Grill* states that “[t]he etching conditions are then changed to removed [sic] exposed portions of lower hard mask layer 56 and optional etch stop 10.”

(*Grill* at 7:67–8:2, Fig. 5G.) *Grill*’s Figures 5F and 5G below show this. I believe a person of ordinary skill in the art would have understood that the lower hard mask [56] is masked by the upper level hard mask [58] during the etch, and the etch stop [10] is masked by the wiring level dielectric [12]. Figures 23(a) and 23(b) from the fifth embodiment of the ’696 patent are shown below for

comparison. The '696 patent states that “the patterned second silicon dioxide film 506A and the first silicon dioxide film 504 are dry-etched using the mask pattern 509 and the patterned second organic film 505A as respective masks, thereby forming a patterned second silicon dioxide film 506B having openings for forming wiring grooves and a patterned first silicon dioxide film 504A having openings for forming contact holes as shown in FIG. 23(b).” ('696 patent at 23:66–24:6.)



203. These Figures further clarify to a person of ordinary skill in the art that the aperture of the hole in the lower hard mask [56] corresponds to the wiring groove, and the aperture of the hole in the etch stop [10] corresponds to the aperture of the contact hole. This is also confirmed by comparison with '696

patent at 23:66–24:6. In my view, a contact hole in the '696 patent is part of the final opening that extends from the lower-level metal interconnect to the upper-level metal interconnect. The same logic applies to wiring grooves and openings for forming wiring grooves. The '696 patent distinguishes contact hole patterns and wiring groove patterns by using the labels “A” and “B,” respectively, to designate contact hole patterns and wiring groove patterns in patterned layers. The patterns marked “A” in the final structure are contact holes, and the patterns marked “B” in the final structure are wiring grooves. ('696 patent at, for example, Figs. 23(d), 26(d), 29(a), 32(c), 35(c).) Some openings for forming contact holes are removed altogether before the final structure. ('696 patent at 23:40–42, 25:27–29, 28:49–51, 30:49–51, Figs. 22(b), 25(b), 27(b), 31(b), 34(b).) Others become wiring grooves in the final structure. ('696 patent at 23:42–46, 25:66–26:3, 28:51–55, 30:58–62, Figs. 23(a), 26(a), 28(b), 31(c), 34(c).) Some, such as patterns 504A and 554A, remain in the final structure and therefore become contact holes. ('696 patent at Figs. 23(b), 23(d), 26(b), 26(d), 28(b), 29(a).) The aperture in layer 10 of *Grill* is the same as these layers, and remains a contact hole in the final structure, as explained below.

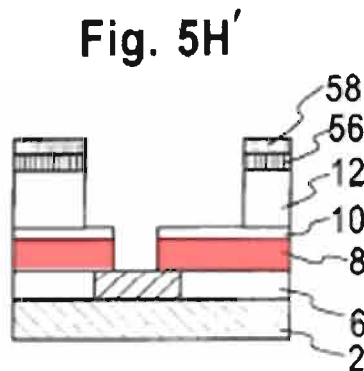
204. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that *Grill* discloses “dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned

second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively.”

205. Claim 13 recites “filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together,” which *Grill* renders obvious.

206. I believe a person of ordinary skill in the art would have understood that, before performing this claim step, an additional etch is required to remove the layer immediately above the conductive via [4] to expose the conductive via [4]. (*Grill* at 8:2–8, Fig. 5H.) The fifth and sixth embodiments of the ’696 patent each teach an additional, unclaimed step as well. In describing the fifth embodiment, the ’696 patent states that, after forming contact holes in the first insulating film, “silicon nitride film 502 is dry-etched using the patterned first silicon dioxide film 504A as a mask, thereby forming a patterned first silicon nitride film 502A (see FIG. 23(d)) and exposing the first metal interconnects 501 within the contact holes 512.” (’696 patent at 24:14–18.) In describing the sixth embodiment, the ’696 patent states that “the patterned silicon dioxide film 604A and the silicon nitride film 602 are dry-etched using the mask pattern 608 and the patterned first organic film 603A as respective masks, thereby forming a patterned silicon dioxide film

604B having wiring grooves (see FIG. 32(c)) and a patterned silicon nitride film 602A having the contact holes (see FIG. 32(c)), and exposing the first metal interconnects 601 within the contact holes 611.” (’696 patent at 29:13–20, Fig. 23(c), Fig. 32(b).) The unclaimed intermediary etch of *Grill*, as I believe a person of ordinary skill in the art would have understood it, is depicted in Fig. 5H’.<sup>4</sup>



207. A person of ordinary skill in the art would have understood that in *Grill*’s embodiment that does not have optional layer 7, the conductive via [4] is exposed after progressing to the step shown in Fig. 5H’. Because the conductive via [4] is already exposed, I believe a person of ordinary skill in the art would have

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<sup>4</sup> Figure 5H’ is a depiction of the *Grill* embodiment that omits optional layer 7. It depicts what a person of ordinary skill in the art would have understood regarding *Grill*’s alternative embodiment without optional layer 7.

also understood that the additional step in Fig. 1J of *Grill* is unnecessary.<sup>5</sup> As I stated above, a person of ordinary skill in the art would have understood that etch stop 10 is a very thin layer that does not contribute significantly to the RC time constant of the interconnect. Thus, there is no real need to etch layer 10 to reduce the RC constant of the interconnect. Furthermore, a person of ordinary skill in the art would have understood that etching etch stop layer 10 with the conductive via exposed could damage the conductive via and reduce the conductivity of the interconnect. Accordingly, a person of ordinary skill in the art would have known that it is preferable not to perform the etch step of Figure 1J when optional layer 7 is not present.

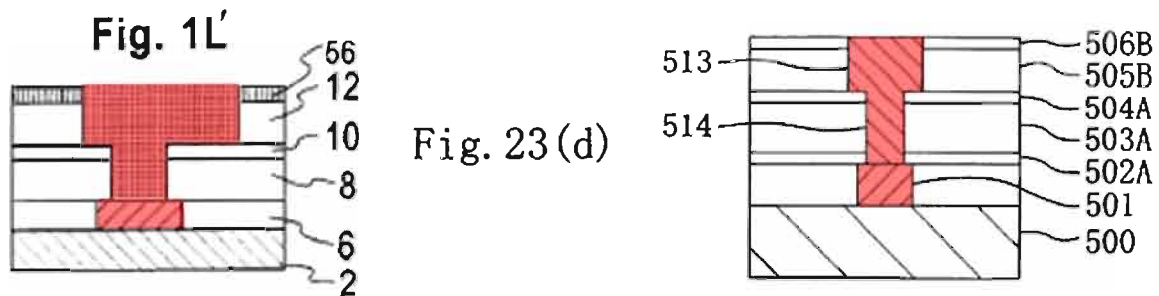
208. *Grill* states that “[c]avity 20 is . . . overfilled with conductive wiring material 22, by a process such as physical vapor deposition, chemical vapor deposition, solution deposition, or plating.” (*Grill* at 4:64–5:2, Fig. 1K.) Then, the conductive wiring material [22] is planarized by CMP to be approximately even with the top surface of dielectric 12 or remaining hard mask. (*Grill* at 5:2–8, Fig.

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<sup>5</sup> Alternatively, even if the optional passivation/adhesion layer [7] is used, a person of ordinary skill in the art would have understood that in many cases it is desirable not to etch the etch stop layer [10] when the passivation/adhesion layer [7] is etched, by using a selective etch. (*Zhao*, 6:25–29, 6:62–7:2, 7:15–18, 7:55–65, Fig. 10.)



1L.) Figure 1L'<sup>6</sup> shows this. I believe a person of ordinary skill in the art would have understood that, if layer 7 were removed, metal would fill the contact holes in the etch stop layer [10] and the via level dielectric [8] and fill the wiring grooves in the lower hard mask [56] and the wiring level dielectric [12]. Figure 23(d) from the fifth embodiment of the '696 patent is shown below for comparison.



209. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that *Grill* would have rendered obvious to a person of ordinary skill in the art the step of “filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.”

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<sup>6</sup> Figure 1L' is a depiction of the *Grill* embodiment that omits optional layer 7. It depicts what a person of ordinary skill in the art would have understood regarding *Grill*'s alternative embodiment without optional layer 7.

**E. The combination of *Grill* and *Aoyama* and Claim 13**

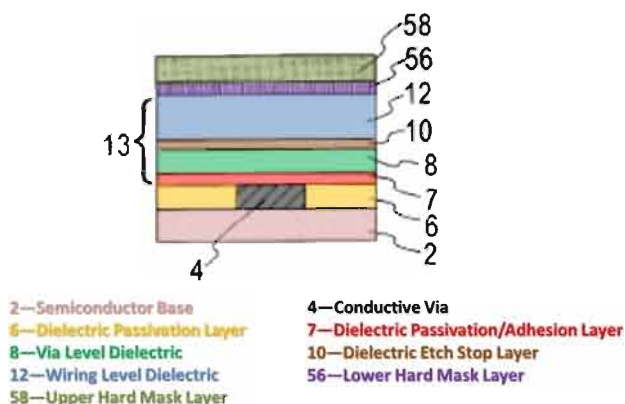
210. The preamble of claim 13 recites “[a] method for forming an interconnection structure.”

211. As discussed above, it is my opinion that *Grill* discloses a method for forming an interconnection structure.

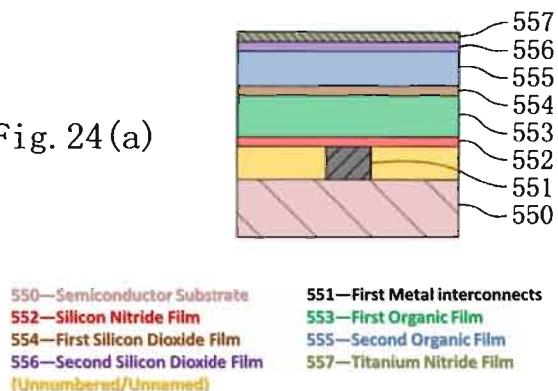
212. Claim 13 recites “forming a first insulating film over lower-level metal interconnects; forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; [and] forming a thin film over the third insulating film.”

213. As discussed above, *Grill* discloses these features. Figure 5A of *Grill* and Figure 24(a) from the modified fifth embodiment of the ’696 patent are reproduced below for comparison. The first insulating film corresponds to *Grill*’s layer 10 and the ’696 patent’s layer 554. The second insulating film corresponds to *Grill*’s layer 12 and the ’696 patent’s layer 555. The third insulating film corresponds to *Grill*’s layer 56 and the ’696 patent’s layer 556. The thin film corresponds to *Grill*’s layer 58 and the ’696 patent’s layer 557. (*Grill* at 3:60–4:13, 7:30–42; ’696 patent at 24:60–25:11.)

**Fig. 5A**



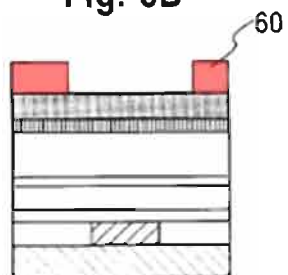
**Fig. 24(a)**



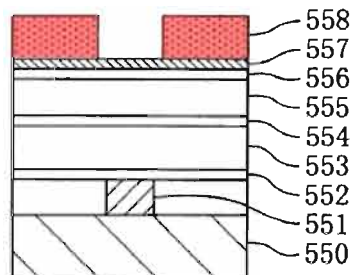
214. Claim 13 recites “forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves.”

215. As discussed above, *Grill* discloses this feature. Figure 5B of *Grill* and Figure 24(b) from the modified fifth embodiment of the '696 patent are shown below for comparison. The first resist pattern corresponds to *Grill*'s layer 60 and the '696 patent's layer 558. (*Grill* at 7:42–44; '696 patent at 25:19–21.)

**Fig. 5B**

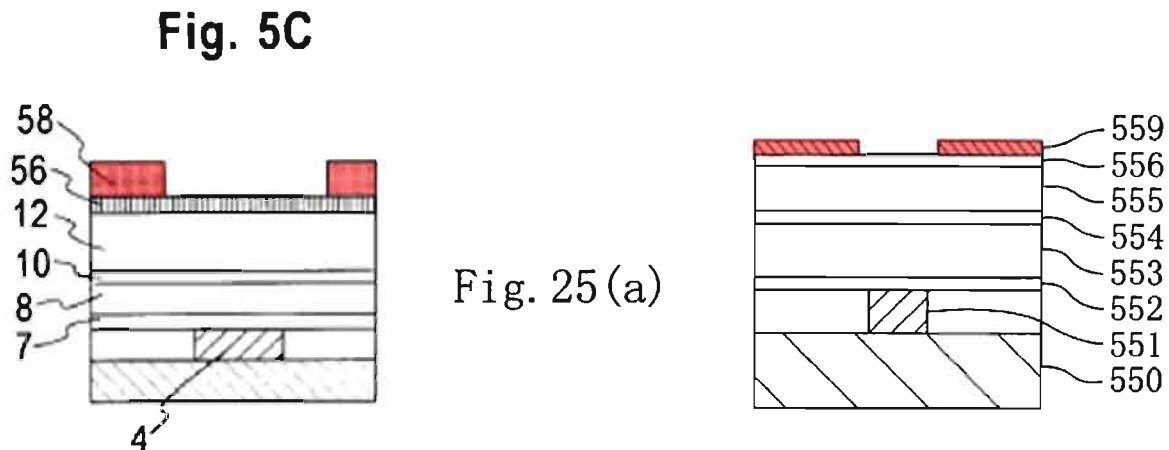


**Fig. 24(b)**



216. Claim 13 recites “etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves.”

217. As discussed above, *Grill* discloses this feature. Figure 5C of *Grill* and Figure 25(a) from the modified fifth embodiment of the '696 patent are shown below for comparison. The mask pattern corresponds to *Grill*'s patterned layer 58 and the '696 patent's layer 559. (*Grill* at 7:45–50; '696 patent at 25:21–25.)



218. Claim 13 recites “removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes.”

219. A person of ordinary skill in the art would have understood that the combination of *Grill* and *Aoyama* discloses this feature.

220. *Grill* states that “[p]atterned resist layer 60 is then removed by a process such as ashing or wet chemical etching, and a second resist layer 62, patterned with a second (via level) pattern, is then formed on the structure.” (*Grill* at 7:51–55, Fig. 5D.) A person of ordinary skill in the art would have understood that second resist layer [62] is formed on the lower hard mask [56] and the mask

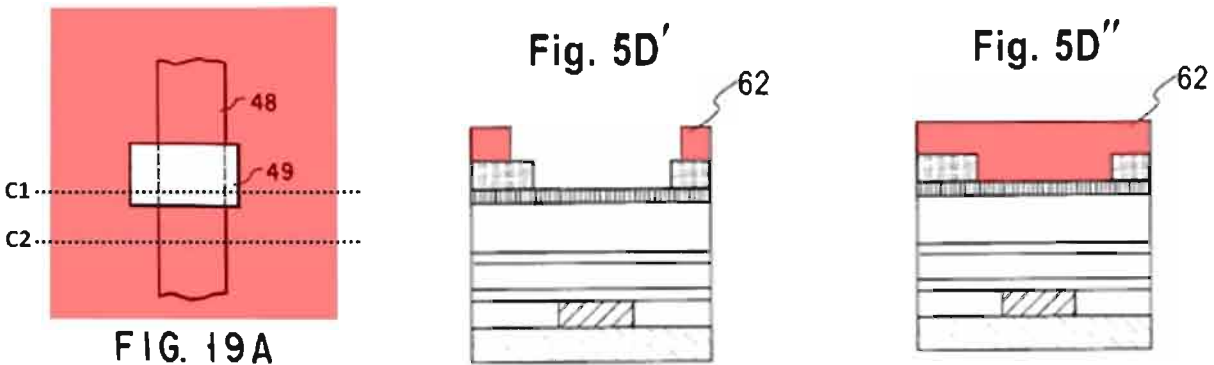
pattern [58] in the *Grill-Aoyama* combination. To understand this, a person of ordinary skill in the art would have known to look beyond the cross-sections shown in *Grill* and considered the three-dimensional structure as a whole.

221. The shape of *Aoyama*'s through-hole (i.e., via), as viewed looking down from above, is shown in Figure 19A below. The areas colored red in Figure 19A indicate that photoresist is located in the areas other than the through-hole location. A person of ordinary skill in the art would have understood that this is how the photomask and photoresist works in *Grill*. The photoresist in the via areas is removed to permit etching the via into the device structure. Two dashed lines have been added to Figure 19A below to indicate cross-sections C1 and C2.

Element 48 is a trench. (*Aoyama* at 16:18–21.) A person of ordinary skill in the art would have understood that cross-section C1 of the *Grill-Aoyama* combination is shown below in Figure 5D'.<sup>7</sup> A person of ordinary skill in the art would have understood that cross-section C2 of the *Grill-Aoyama* combination is shown below in Figure 5D''. A person of ordinary skill in the art would have understood that the Figures below show that the second resist pattern is on both the lower hard mask [56] and the mask pattern [58].

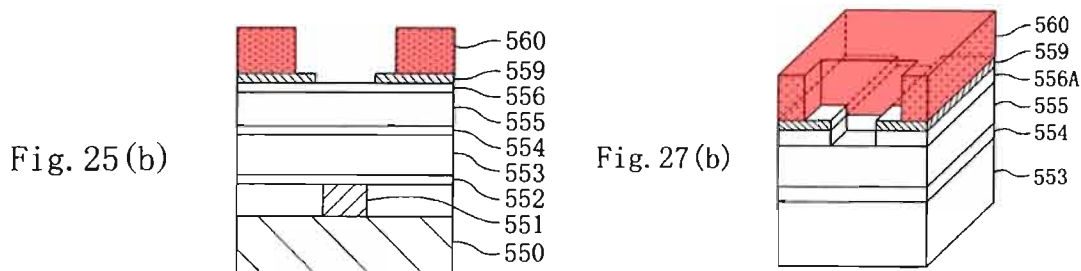
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<sup>7</sup> The prime in a figure number indicates that it has been modified from the original *Grill* figure.



222. Figures 25(b) and 27(b) from the modified fifth embodiment of the '696 patent are shown below for comparison. ('696 patent at Fig. 37(a).)

According to the '696 patent, "a second resist pattern 560, having openings for forming contact holes, is formed by lithography on the mask pattern 559 as shown in FIG. 25(b)." ('696 patent at 25:27–35.)



223. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that the *Grill-Aoyama* combination discloses "removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes."

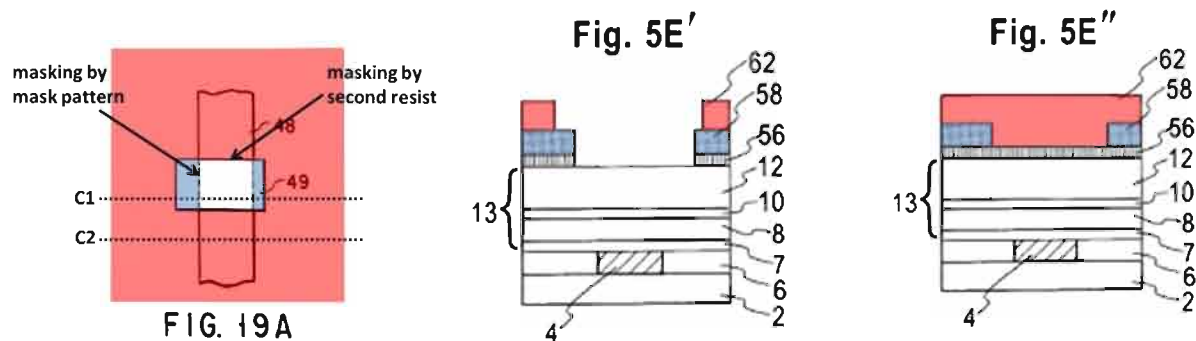
224. Claim 13 recites “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

225. *Grill* states that “[t]he pattern of resist layer 62 [the via level pattern] is then transferred into lower hard mask layer 56.” (*Grill* at 7:57–61, Fig. 5E.) As explained above, a person of ordinary skill in the art would have understood that the lower hard mask layer [56] has openings for forming contact holes because it contains the via level pattern of the second resist layer [62]. (*Grill* at 7:51–55.) As I also explain above, a person of ordinary skill in the art would have understood that the second resist pattern [62] is transferred into the lower hard mask layer [56] by dry etching, as opposed to wet etching, because it is an anisotropic etch of a non-single-crystal or amorphous material. Anisotropic wet etches work by exploiting chemical differences along different directions of a crystal lattice. When no such directionality exists in a material, the wet etch is isotropic. Dry etches, however, tend to be highly directional regardless of the etchant. Thus, a person of ordinary skill in the art would have understood that an anisotropic etch of a non-single-crystal or amorphous material would have been a dry etch.

226. I believe that a person of ordinary skill in the art would have understood that the lower hard mask [56] is etched using both the second resist pattern [62] and the mask pattern [58] as a mask. Again, a person of ordinary skill

in the art would have understood that a three-dimensional perspective of *Grill* is needed.

227. The shape of *Aoyama's* via opening, viewed from above, is shown in Figure 19A below. A person of ordinary skill in the art would have understood that the red areas indicate photoresist [62] and that the blue areas indicate the mask pattern [58]. A person of ordinary skill in the art would have understood that cross-section C1 of the *Grill-Aoyama* combination is shown below in Figure 5E'. A person of ordinary skill in the art would have understood that cross-section C2 of the *Grill-Aoyama* combination is shown below in Figure 5E''. A person of ordinary skill in the art would have understood the Figures below show masking during the etch by both the mask pattern [58] and second resist layer [62].

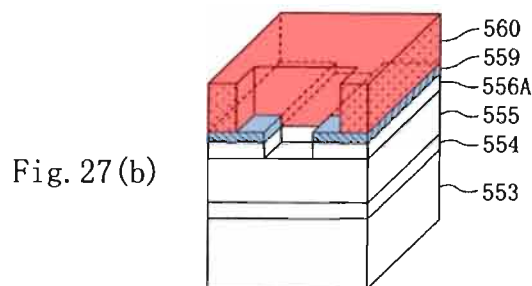
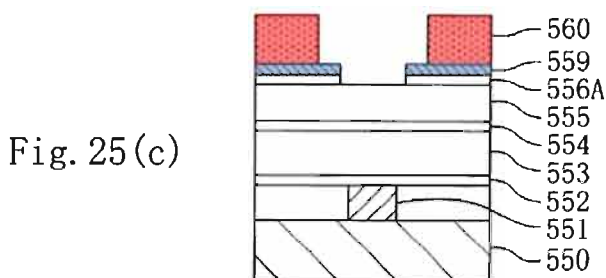


228. Figures 25(c) and 27(b) from the modified fifth embodiment of the '696 patent are shown below with color highlights for comparison. According to the '696 patent, "the second silicon dioxide film 556 is dry-etched using the second resist pattern 560 and the mask pattern 559 as a mask, thereby forming a patterned



second silicon dioxide film 556A having openings for forming contact holes.”

(’696 patent at 25:36–41.)

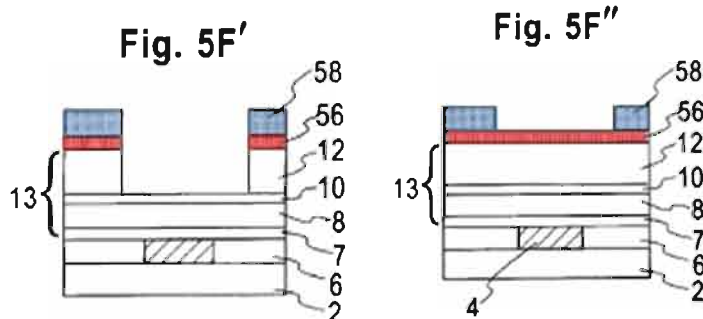
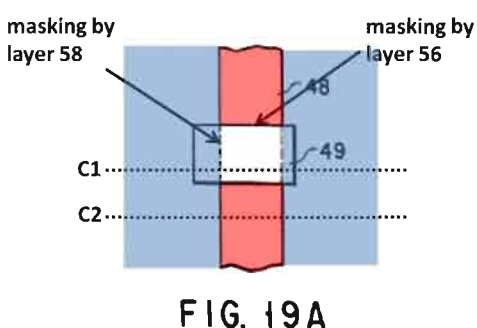


229. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that the *Grill-Aoyama* combination discloses “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

230. Claim 13 recites “dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes.”

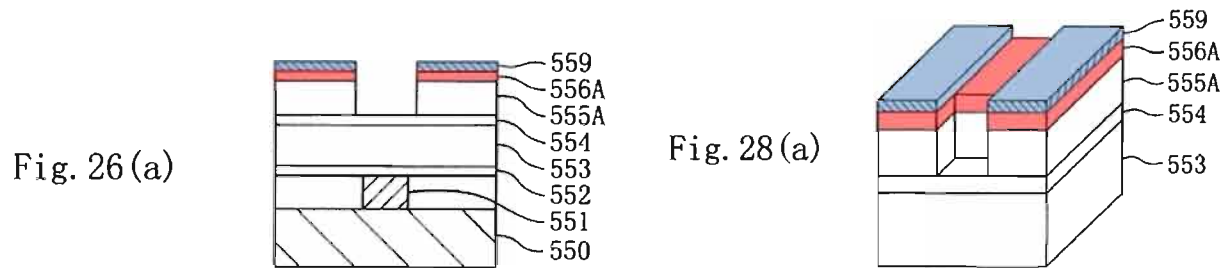
231. *Grill* states that “[t]he via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching.” (*Grill* at 7:62–63, Fig. 5F.) I believe a person of ordinary skill in the art would have understood that the patterned lower hard mask [56] acts as a mask during this etch in the *Grill-Aoyama* combination. A person of ordinary skill in the art would have understood that a reactive ion etch is a dry etching process.

232. The top surface of *Aoyama*'s structure, as viewed looking down on it, is shown in Figure 19A below. A person of ordinary skill in the art would have understood that the resist pattern [62] is removed during the etch of dielectric layer 12, exposing the mask pattern [58] and patterned lower hard mask [56]. (*Grill* at 7:64–66.) A person of ordinary skill in the art would have understood that the red areas of Figure 19A indicate the patterned lower hard mask [56] and that the blue areas indicate the mask pattern [58]. A person of ordinary skill in the art would have understood that cross-section C1 of the *Grill-Aoyama* combination is shown below in Figure 5F'. A person of ordinary skill in the art would have understood that cross-section C2 of the *Grill-Aoyama* combination is shown below in Figure 5F''. A person of ordinary skill in the art would have understood that the Figures below show masking during the etch by the patterned lower hard mask [56], as well as by the mask pattern [58].



233. Figures 26(a) and 28(a) from the modified fifth embodiment of the '696 patent are shown below for comparison. According to the '696 patent, "the second organic film 555 is dry-etched using the patterned second silicon dioxide

film 556A as a mask, thereby forming a patterned second organic film 555A having openings for forming contact holes.” (’696 patent at 25:66–26:3.)



234. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that the *Grill-Aoyama* combination discloses “dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes.”

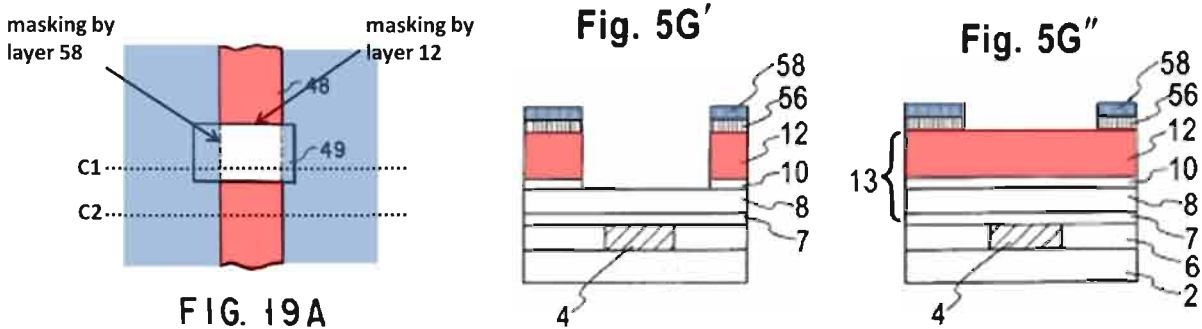
235. Claim 13 recites “dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively.”

236. *Grill* states that “[t]he etching conditions are then changed to removed [sic] exposed portions of lower hard mask layer 56 and optional etch stop 10.” (*Grill* at 7:67–8:2, Fig. 5G.) Understanding the three-dimensional nature of the *Grill* structure, I believe a person of ordinary skill in the art would have understood that in the *Grill-Aoyama* combination the lower hard mask [56] is masked in the

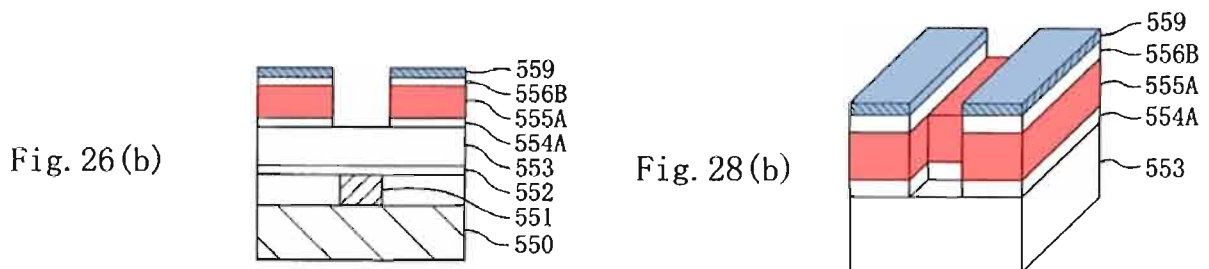
wiring groove by the upper level hard mask [58] during the etch, and the etch stop [10] is masked in the contact hole by the wiring level dielectric [12]. As I explain above, the aperture in etch stop [10], like patterns 504A and 554A in the '696 patent, is a contact hole. Additionally, I believe a person of ordinary skill in the art would have understood that this etch is a dry etch because it is an anisotropic etch of a non-single-crystal or amorphous material. Anisotropic wet etches work by exploiting chemical differences along different directions of a crystal lattice. When no such directionality exists in a material, the wet etch is isotropic. Dry etches, however, tend to be highly directional regardless of the etchant. Thus, a person of ordinary skill in the art would have understood that an anisotropic etch of a non-single-crystal or amorphous material would have been a dry etch.

237. The top surface of *Aoyama*'s structure, as viewed looking down on it, is shown in Figure 19A below. A person of ordinary skill in the art would have understood that the red areas of Figure 19A indicate the patterned second insulating film [12] and that the blue areas indicate the mask pattern [58]. A person of ordinary skill in the art would have understood that cross-section C1 of the *Grill-Aoyama* combination is shown below in Figure 5G'. A person of ordinary skill in the art would have understood that cross-section C2 of the *Grill-Aoyama* combination is shown below in Figure 5G''. A person of ordinary skill in the art would have understood that the Figures below show masking during the

etch by the patterned second insulating film [12], as well as by the mask pattern [58].



238. Figures 26(b) and 28(b) from the modified fifth embodiment of the '696 patent are shown below for comparison. According to the '696 patent, "the patterned second silicon dioxide film 556A and the first silicon dioxide film 554 are dry-etched using the mask pattern 559 and the patterned second organic film 555A as respective masks, thereby forming a patterned second silicon dioxide film 556B having openings for forming wiring grooves and a patterned first silicon dioxide film 554A having openings for forming contact holes." ('696 patent at 26:15–22.)



239. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that the *Grill-Aoyama* combination discloses “dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively.”

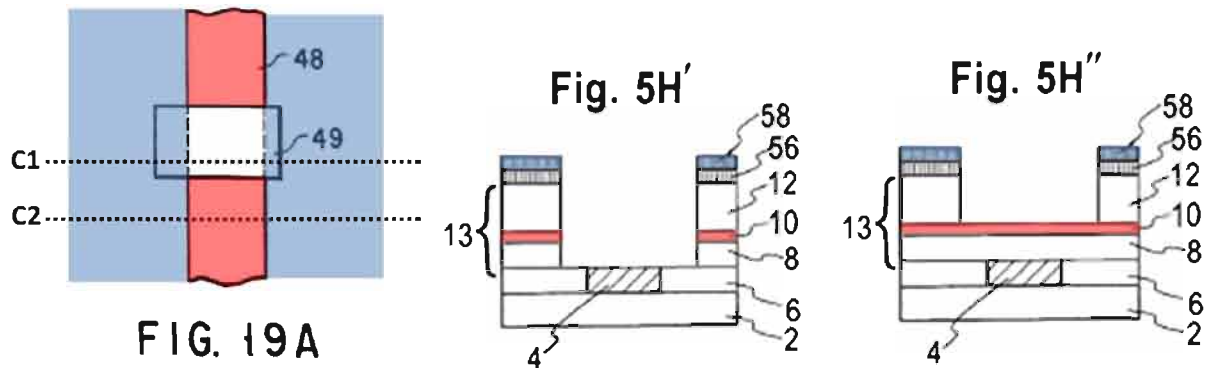
240. Claim 13 recites “filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.”

241. A person of ordinary skill in the art would have understood that before performing this claim step an additional etch is required to remove the layer immediately above the conductive via [4] to expose the conductive via [4]. (*Grill* at 8:2–8.) As explained above, the ’696 patent expressly teaches this additional etch step. (’696 patent at 24:14–18, 29:13–20, Fig. 23(c), Fig. 32(b)). I have been told that prior art that discloses all of the claimed steps of claim 13 invalidates claim 13 regardless of the presence any additional steps. I believe a person of ordinary skill in the art would have understood the unclaimed etch of the *Grill-Aoyama* combination as depicted in Figures 19A, 5H’, and 5H’’.<sup>8</sup> A person of

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<sup>8</sup> Figures 5H’ and 5H’’ are a depiction of the *Grill-Aoyama* combination using the *Grill* embodiment that omits optional layer 7. It shows what I believe a

ordinary skill in the art would have understood that Figures 5H' and 5H'' depict the respective cross-sections C1 and C2 of Figure 19A.



242. I believe a person of ordinary skill in the art would have understood that the conductive via [4] is exposed after the step shown above. Because the conductive via [4] is already exposed, I believe a person of ordinary skill in the art would have also understood that the additional step in Figure 1J of *Grill* is unnecessary. As I explain above, the additional etch step may also be harmful because the etchant could damage the exposed conductive via. I therefore believe that a person of ordinary skill in the art would have understood that the wiring level pattern would not be transferred into etch step 10.

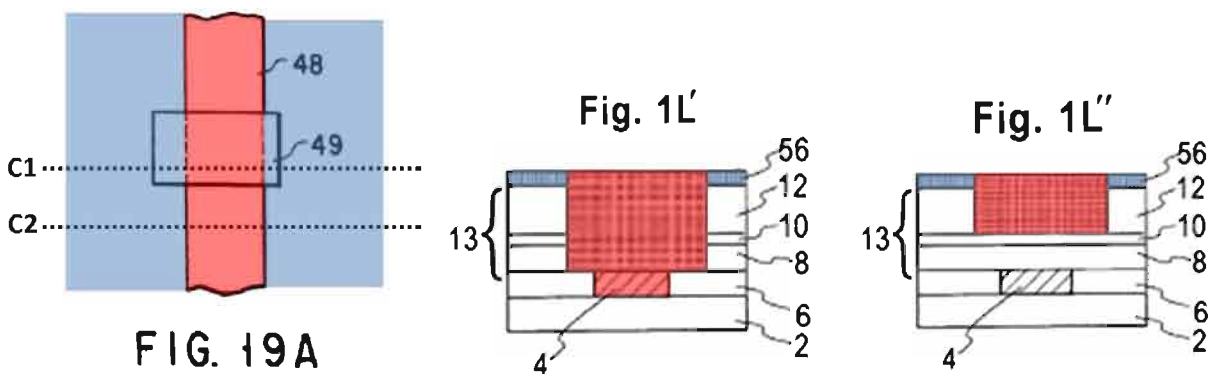
243. With regard to the claim step of filling the wiring grooves, *Grill* states that “[c]avity 20 is . . . overfilled with conductive wiring material 22, by a process

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person of ordinary skill in the art would have understood regarding *Grill*'s alternative embodiment without optional layer 7, as it is combined with *Aoyama*.

such as physical vapor deposition, chemical vapor deposition, solution deposition, or plating.” (*Grill* at 4:64–5:2, Fig. 1K.) Then, the conductive wiring material [22] is planarized by CMP to be approximately even with the top surface of dielectric 12 or remaining hard mask. (*Grill* at 5:2–8, Fig. 1L.)

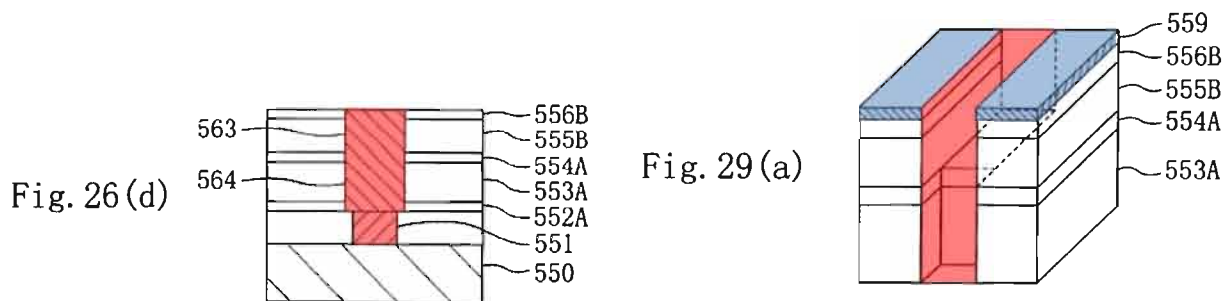
244. The top surface of *Aoyama*’s structure, as viewed looking down on it, is shown in Figure 19A below. A person of ordinary skill in the art would have understood that the red areas of Figure 19A indicate the metallized regions and that the blue areas indicate the patterned lower hard mask [56]. A person of ordinary skill in the art would have understood that cross-section C1 of the *Grill-Aoyama* combination is shown below in Figure 1L’. A person of ordinary skill in the art would have understood that cross-section C2 of the *Grill-Aoyama* combination is shown below in Figure 1L’’. Figure 1L’ is a depiction of the *Grill* embodiment that omits optional layer 7 depicting what I believe a person of ordinary skill in the art would have understood regarding *Grill*’s alternative embodiment without optional layer 7.





245. I believe a person of ordinary skill in the art would have understood that, if layer 7 were removed, metal would fill the contact holes in the etch stop layer [10] and via level dielectric [8] and fill the wiring grooves in the lower hard mask [56] and the wiring level dielectric [12], as shown in Figures 1L' and 1L".

246. Figures 26(d) and 29(a) from the modified fifth embodiment of the '696 patent are shown below for comparison. According to the '696 patent, "a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 562 and the wiring grooves 561." ('696 patent at 26:38–41.) "As a result, second metal interconnects 563 and contacts 564, connecting the first and second metal interconnects 551 and 563 together, are formed." ('696 patent at 26:44–47.)



247. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that the *Grill-Aoyama* combination discloses "filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together."

**F. The combination of *Grill and Aoyama* and Claim 15**

248. Claim 15 depends from claim 13 and further recites that “a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.”

249. The '696 patent discusses this feature with reference to Figures 25(b), 25(c), 27(b), 34(b), 36, and 37(a), all shown below. ('696 patent at 25:26–65, 30:49–57, 31:49–67.) The '696 patent explains that “even if the openings of the second resist pattern 560 for forming contact holes have misaligned with the openings of the mask pattern 559 for forming wiring grooves, the openings of the patterned second silicon dioxide film 556A for forming contact holes can be formed to be self-aligned with the openings of the mask pattern 559 for forming wiring grooves.” ('696 patent at 25:46–52.) Also, “the contacts 564 can connect the first and second metal interconnects 551 and 563 together with a lot more certainty.” ('696 patent at 25:63–65, 25:42–65, 27:12–60, 31:49–67, Fig. 37(b).)

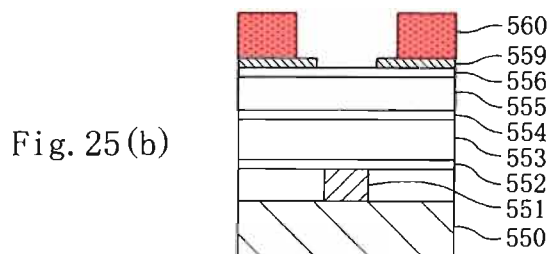
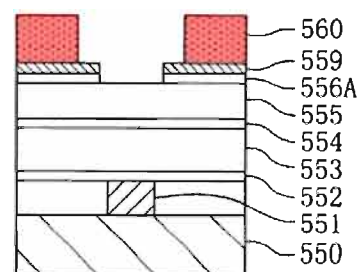


Fig. 25(c)



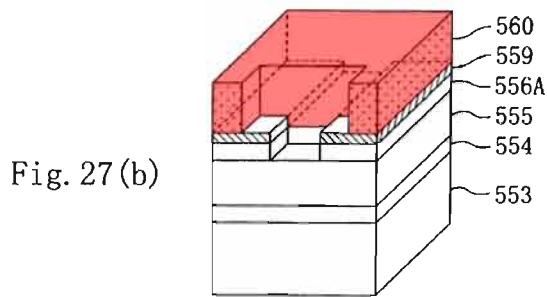


Fig. 27(b)

Fig. 34(b)

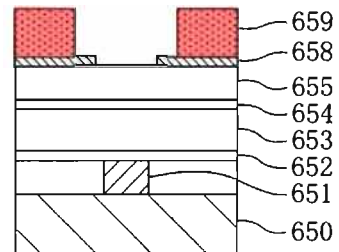
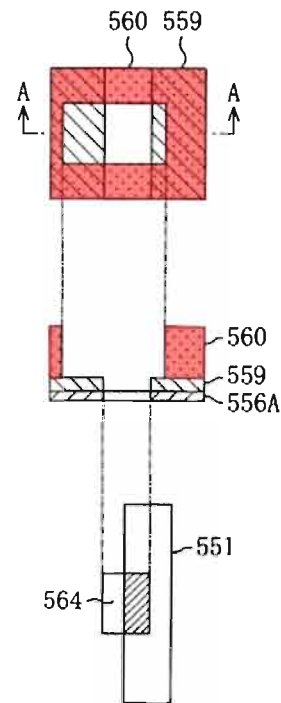
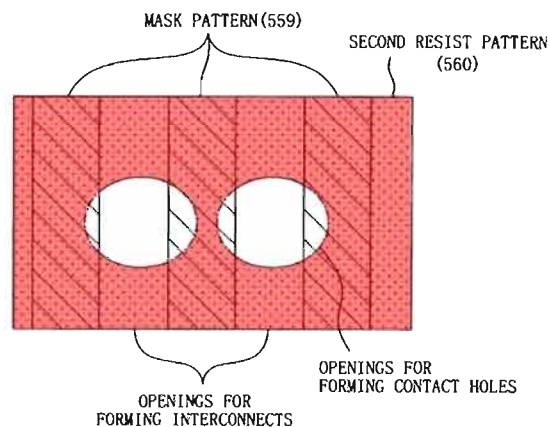


Fig. 37(a)

Fig. 36



250. A person of ordinary skill in the art would have understood that *Aoyama* discloses the same solution to address the same problem. *Aoyama* states that misalignment of the photomask during through-hole (i.e., via) formation can cause the through-hole to be too small and the wiring groove too wide (at the location of the through-hole). (*Aoyama* at 3:18–21, 3:29–32.) This leads to an increase in contact resistance, degradation in reliability, and difficulty in achieving



below, illustrate *Aoyama*'s solution. (Refer also to *Aoyama* at 3:6–38, 6:7–13, 15:48–16:30.) Figure 25(c) and a portion of Figure 37(a) of the '696 patent are also reproduced below for comparison. ('696 patent at 25:42–65, 27:12–60, 31:49–60.)

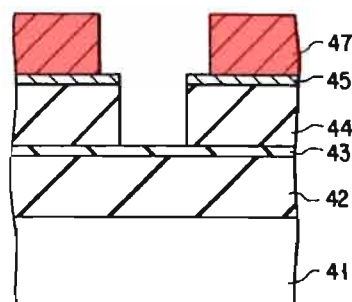


FIG. 18B

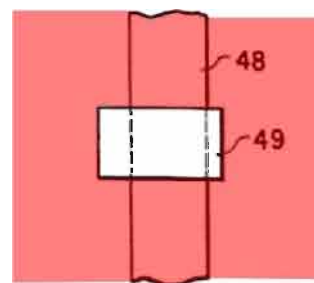
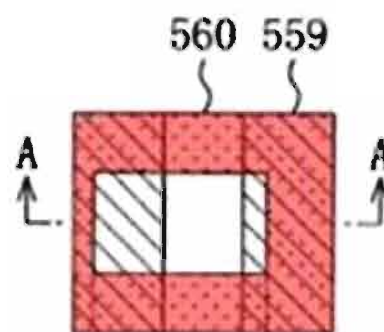
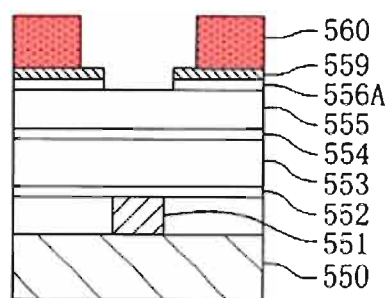


FIG. 19A

Fig. 37(a)

Fig. 25(c)



252. I believe a person of ordinary skill in the art would have understood that these disclosures would remain unaffected by the combining them with the relevant teachings of *Grill* and regardless of whether layer 7 of *Grill* is used.

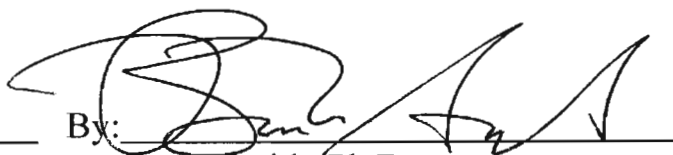
253. Based on these disclosures, I believe a person of ordinary skill in the art would have understood that the *Grill-Aoyama* combination discloses that “a

size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.”

254. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

255. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 11th day of July 2016, in Rochester, New York.

Dated: 7/11/2016 By:   
Dr. Bruce Smith, Ph.D.

# Appendix A

## SUMMARY

Bruce Smith has over 30 years of research, academic, industry, and consulting engineering experience in IC (integrated circuit) processing, semiconductor device materials, microelectronics, microlithography, and LCD-TFT (thin film transistor) technology. He is a professor of Microelectronic Engineering and the Director of the Ph.D. program in Microsystems Engineering at the Rochester Institute of Technology. His industry experience includes manufacturing and R&D and he has worked with companies in the US, Europe, and Asia. Professor Smith is a Fellow of the IEEE, a Fellow of the OSA, a Fellow of SPIE, and a member of AVS, ASEE, and SID. He is the recipient of RIT's Trustees Scholarship Award, a SPIE Research Mentoring Award, RIT's Creators Award, and the Rush Henrietta Outstanding Alumni Award, among others, and has been inducted into RIT's Innovator Hall of Fame. Professor Smith has over 200 publications including technical papers, articles, textbooks, and textbook chapters. He holds 27 patents and has licensed his technology both nationally and internationally.

Prof. Smith has expertise and is able to serve as an expert witness in semiconductor IC processes and fabrication, microlithography, deposition and etch processes, and TFT/LCD flat panel technology.

## PROFESSIONAL EXPERIENCE

- Rochester Institute of Technology, Professor, Kate Gleason College of Engineering, 1988-present  
Director and Professor, Microsystems Engineering Ph.D. Program, 2008-present  
Intel Professor of Research and Technology, Microelectronic Engineering, 2000-2007  
Associate Dean of Graduate Programs, Kate Gleason College of Engineering, 2001-2004  
Director, Center for Nanolithography Research, 2004-present  
Professor, Microelectronic Engineering Department, 1988-2008
- IMEC (Interuniversity Microelectronics Center), Leuven, Belgium, Visiting Professor, 2008
- Lithographic Technology Corp / Amphibian Systems, President, 1998-present
- IMEC (Interuniversity Microelectronics Center), Leuven, Belgium, Visiting Professor, 2001
- International SEMATECH, Austin Texas, Visiting Scholar, 1997
- Rutherford Appleton Laboratories, Oxford, U.K., Visiting Scientist, 1995
- Digital Equipment Corp., Hudson, Mass., Advanced Development Center, 1986-1988
- Gould AMI Semiconductor, Santa Clara, Calif., Process Development Group, 1983-1986

## EDUCATION

- B.S., M.S. Rochester Institute of Technology, College of Science, Imaging Science, Thesis: "Optically Transparent Heat Mirror Thin-Films of ZnS-Ag-ZnS," 1988.
- Ph.D., Rochester Institute of Technology, Center for Imaging Science, Thesis: "Excimer Laser Semiconductor Microlithography at 193nm," 1994.

## LITIGATION SUPPORT EXPERIENCE

- |          |           |   |
|----------|-----------|---|
| Date:    | 2014-     | Weil, Gotshal & Manges LLP  |
| Case:    |           | DSS Technology Management, Inc. vs. <u>Samsung Electronics Co. Ltd.</u> |
| Project: |           | Inter partes review petition  |
| Field:   |           | Multiple patterning for integrated circuit processing                   |
| Date:    | 2013-2015 | Ropes and Gray LLP  |
| Case:    |           | <u>Spansion LLC</u> v. Macronix America Co., Ltd. et al                 |
| Project: |           | ITC patent infringement case – Testifying Expert                        |
| Field:   |           | Flash memory chip method and processes                                  |



Date:	2013 –2014	McKenna Long & Aldridge LLP
Case:		<u>Eidos Display, LLC v. AU Optronics Corp. et al</u> (AU, Chi Mei Innolux, Chunghwa, Hannstar, and Hannspree)
Project:		Patent Infringement (USDC, E. Texas) – Testifying Expert
Field:		This film transistor (TFT) processing for LCD flat panel devices
Date:	2013-2014	Mintz, Levin, Cohn, Ferris, Glovsky, and Pepeo PC
Case:		<u>Graphics Properties Holdings, Inc. v. Panasonic Corp. of North America et al</u> (Toshiba, Barnes and Noble, Google, Hewlett-Packard, Lenova, and ZTE) – Testifying Expert
Project:		Patent infringement (Delaware Federal District)
Field:		Wide angle LCD display devices and backlighting
Date:	2012 –	Bunsow, DeMory, Smith, & Allison LLP
Case:		<u>NXP B.V. v. Research in Motion Ltd. et. al.</u> (TriQuint, SanDisk, Hynix, and Qualcomm)
Project:		Patent Infringement (USDC, FLA Middle District), IPR (USPTO) – Testifying Expert
Field:		Dummy pattern fill for integrated circuit fabrication
Date:	2011 –2012	Mintz, Levin, Cohn, Ferris, Glovsky, and Pepeo PC
Case:		<u>Graphics Properties Holdings v. Respondents</u> (RIM, HTC, LG, Apple, Samsung, and Sony)
Project:		ITC Patent Infringement – Testifying Expert
Field:		LCD stack configuration for display devices
Date:	2011	O’Melveny and Meyers
Case:		<u>Samsung Electronics Co. Ltd. v. AU Optronics Corp. et al</u> (Acer, BenQ, and SANYO)
Project:		ITC Patent infringement
Field:		Flat panel (LCD) display device manufacturing processes
Date:	2010-2011	McDermott Will & Emery
Case:		<u>Spansion Inc. v. Samsung Electronics Co</u>
Project:		ITC patent infringement case – Testifying Expert
Field:		Contact hole processes for flash memory chips
Date:	2011-	Keker and Van Nest LLP
Case:		STC UNM v. <u>Intel Corp.</u>
Project:		Patent infringement (USDC, New Mexico) – Testifying Expert
Field:		Lithography techniques and integrated circuit products
Date:	2010-	Irell & Manella LLP
Case:		Patent re-examination
Project:		USPTO re-examination and hearing – Testifying Expert
Field:		Flat panel LCD illumination devices
Date:	2010	Keker and Van Nest LLP
Case:		STC UNM v. <u>Taiwan Semiconductor Manufacturing Co.</u>
Project:		ITC patent infringement
Field:		Lithography techniques and integrated circuit products
Date:	2010-2011	McDermott Will & Emery
Case:		<u>Spansion LLC v. Samsung Electronics Co.</u> (and counter-claim)
Project:		Patent infringement case (USDC, E.D. Va. District) – Testifying Expert
Field:		Flash memory device processes
Date:	2010-2011	Irell & Manella LLP
Case:		<u>Chi Mei Innolux v. Sony Corporation</u>
Project:		ITC patent infringement case
Field:		LCD flat panel patterned electrodes
Date:	2010-2011	Ropes and Gray LLP

	Case:	Samsung Electronics Co. v. <u>Spansion Japan Ltd.</u>
	Project:	ITC patent infringement case
	Field:	Lithography and etch processing for flash memory products
Date:	2010	Sidley Austin LLP
	Case:	<u>Agere Systems Inc. and LSI Corp.</u> v. Xilinx, Inc.
	Project:	Patent infringement (S.D. N.Y.)
	Field:	Metallization of integrated circuits
Date:	2010	McDermott Will & Emery
	Case:	Samsung Electronics Co. v. <u>Spansion LLC and Spansion Inc.</u>
	Project:	ITC patent infringement case
	Field:	Lithography and etch processing for flash memory products
Date:	2010	Standley Law Group LLP
	Case:	<u>American Panel</u> v. Vertex
	Project:	Patent infringement arbitration
	Field:	Flat panel display technology
Date:	2009-2011	Irell & Manella LLP
	Case:	Apel dyn Corp. v. <u>Chi Mei Optoelectronics Corp.</u> et al (AU, Samsung, Sharp, and Sony)
	Project:	Patent infringement (USDC, Delaware) – Testifying Expert
	Field:	LCD flat panel response time
Date:	2009-10	Fish and Richardson P.C.
	Case:	<u>Semiconductor Energy Laboratory Co. Ltd.</u> v. Eastman Kodak
	Project:	Patent interference case (USPTO)
	Field:	Organic light emitting diode (OLED) display devices
Date:	2009	Steptoe and Johnson, LLP
	Case:	Qimonda AG v. <u>Seagate Technology</u>
	Project:	ITC patent infringement case - Testifying Expert
	Field:	Polysilicon and amorphous silicon technology; silicon-oxi-nitride anti-reflection coating deposition technology
Date:	2009	Fish and Richardson P.C.
	Case:	Sharp Corp. v. <u>Samsung Electronics Co. Ltd.</u>
	Project:	Patent infringement, (E.D. Tx.)
	Field:	Liquid crystal display polarizers and electro static discharge (ESD) technology
Date:	2008	Steptoe and Johnson, LLP
	Case:	Neumark-Rothschild v. <u>Toshiba Corp.</u>
	Project:	ITC patent infringement case
	Field:	Wide bandgap (II-VI and III-V) semiconductor materials processing for short-wavelength LEDs and laser diodes
Date:	2006 –2012	Wolf Block Schorr and Solis-Cohen, LLP
		Bernstein Litowitz Berger & Grossmann LLP
	Case:	<u>Anvik Corp.</u> v. Nikon Corp., et al (Toshiba, Samsung, LG Electronics, Sharp, LG, Chi Mei, AU, AFPD, Panasonic, IPS, and Hitachi, )
	Project:	Patent infringement (USDC, S. NY District) – Testifying Expert
	Field:	Lithography method for LCD flat panel manufacturing
Date:	2007-08	Ropes & Gray, LLP
	Case:	Akrion Inc., v. <u>Solid State Equipment Corp.</u>
	Project:	Patent infringement
	Field:	Silicon wafer cleaning and preparation
Date:	2007-08	Fish and Richardson P.C.

Case:	Renesas Technology v. <u>Samsung Electronics</u>
Project:	ITC patent infringement case – Testifying Expert
Field:	Thin film and diffractive elements for photomask mask light blocking
Date:	2005-06
Case:	Vinson & Elkins, LLP <u>Advanced Micro Devices</u> v. Oki Electronics
Project:	Patent infringement (USDC, N. CA District) – Testifying Expert
Field:	Silicon wafer preparation and coating
Date:	2004-05
Case:	Irell & Manella, LLP Ultratech Stepper, Inc. v. <u>ASM Lithography, Inc.</u>
Project:	Patent infringement (USDC, N. CA District) – Testifying Expert
Field:	Optical microlithography scanning
Date:	1997-03
Case:	Ward Norris Heller & Reidy, LLP – Testifying Expert IBM Fishkill, NY and Essex, VT, including Union Carbide Corp., Eastman Kodak, J. T. Baker Chemical, KTI, Shipley, Ashland Oil, E. I. DuPont de Nemours and Industri-Chem, suppliers of solvents for the IBM cleanroom operations
Field:	Multi-state litigation, allegations regarding various chemicals used in the manufacturing of semiconductor devices
Date:	1997-03
Cases:	Ward Norris Heller & Reidy, LLP – Testifying Expert Kasowitz Benson Torres & Friedman, LLP Steptoe & Johnson, LLP San Jose IBM Workers Litigation v. Shipley Company San Jose IBM Workers Litigation v. American Hoechst Corporation San Jose IBM Workers Litigation v. Ashland Chemical Company, Union Carbide Corporation, Fischer Scientific Company, and Eastman Kodak Company Rubio v. IBM et al.
Field:	Allegations regarding various chemicals used in an manufacturing of semiconductor devices

## SERVICE

### Professional Associations

Fellow, SPIE International Society for Optical Engineering  
Fellow, Optical Society of America (OSA)  
Senior Member, Institute of Electrical and Electronics Engineers (IEEE)  
Member, American Vacuum Society (AVS)  
Member, American Society for Engineering Education (ASEE)  
Member, Society for Information Display (SID)

### External Service

2014-2018 SPIE Microlithography Symposium Co-Chairman  
2012-2014 OSA Awards Committee  
1997-2014 SPIE Optical Microlithography, Program Committee  
2010-2014 EIPBN Program Committee  
2003-2014 SPIE Zernike Award Committee  
2009-2010 Councilor, Optical Society of America (OSA), Rochester Section  
2008-2009 Program Chairman, International Symposium on Immersion Lithography Extensions  
2004-2005 Conference Chairman, SPIE Optical Microlithography Conference  
1997-2002 EIPBN Program Committee  
1997-1998 SPIE/ISMA Singapore Program Committee  
1995-1997 Chairman, OSA Lithography / Patterning Technical Working Group  
1990-1996 Faculty Advisor, SPIE Student Chapter

### Honors and Awards

2014	IEEE Technology Innovation Award
2014	RIT College of Engineering Research and Publication Awards
2013	RIT Innovation Hall of Fame
2012	Fellow, Optical Society of America
2011	SPIE Research Mentor Award
2008	Visiting Professor, IMEC Micro and Nanoelectronics Research Center
2007	Trustees Excellence in Scholarship and Teaching Award, Rochester Institute of Technology
2007	Fellow, SPIE International Society for Optical Engineering
2007	Rush Henrietta Outstanding Alumni Award
2005	Million Dollar Principle Investigator Award, Rochester Institute of Technology
2005	Patenting Productivity Award, Rochester Institute of Technology
2002	Intellectual Property Productivity Award, Rochester Institute of Technology
2001	Visiting Professor, IMEC Micro and Nanoelectronics Research Center
2000	Intel Professor of Research and Technology, Intel Corp.
1999	RIT Creators Award, Rochester Institute of Technology
1997	Visiting Scholar, International Sematech
1993	Texas Instruments, Douglas Harvey Award
1991	Texas Instruments, Douglas Harvey Award

### Editorial Review

Editorial review of IEEE, JVAC, JM3, and SPIE, journals.

## PATENTS

1. 8,852,850 Method of photolithography using a fluid and a system thereof
2. 7,768,648 Method for aberration evaluation in a projection system
3. 7,345,735 Apparatus for aberration detection and measurement
4. 7,233,887 Method of photomask correction and its optimization using localized frequency analysis
5. 7,170,588 Reduction Smith-Talbot interferometer prism for micropatterning
6. 7,136,143 Method for aberration detection and measurement
7. 7,092,073 Method of illuminating a photomask using chevron illumination
8. 6,934,010 Optical proximity correction method utilizing gray bars as sub-resolution assist features
9. 6,881,523 Optical proximity correction method utilizing ruled ladder bars as sub-resolution assist features
10. 6,846,595 Method of improving photomask geometry
11. 6,835,505 Mask for projection photolithography at or below about 160 nm and a method thereof
12. 6,791,667 Illumination device for projection system and method for fabricating
13. 6,788,388 Illumination device for projection system and method for fabricating
14. 6,556,361 Projection imaging system with a non-circular aperture and a method thereof
15. 6,541,750 Modification of a projection imaging system with a non-circular aperture and a method thereof
16. 6,525,806 Apparatus and method of image enhancement through spatial filtering
17. 6,480,263 Apparatus and method for phase shift photomasking
18. 6,466,304 Illumination device for projection system and method for fabricating
19. 6,395,433 Photomask for projection lithography at or below about 160 nm and a method thereof
20. 6,388,736 Imaging method using phase boundary masking with modified illumination
21. 6,368,755 Masks for use in optical lithography below 180 nm
22. 6,309,780 Attenuated phase shift mask and a method for making the mask
23. 5,939,227 Multi-layered attenuated phase shift mask and a method for making the mask
24. JP2010079303 Method of improving photomask geometry
25. JP2006079117 Optical proximity correction method utilizing gray bar as sub-resolution assist feature
26. EP1240557 Imaging method using phase boundary masking with modified illumination

## SELECTED PUBLICATIONS

1. "The saga of sigma: influences of illumination throughout optical generations," BW Smith - SPIE Advanced Lithography, 2014.
2. "Optical Projection Lithography," B.W. Smith, Nanolithography: The Art of Fabricating Nanoelectronic and Nanophotonic Devices and Systems, Woodhead Publishing, 2014.

3. "Feasibility of compensating for EUV field edge effects through OPC," C Maloney, J Word, GL Fenger, A Niroomand, BW Smith, SPIE Advanced Lithography, 2014.
4. "Optimization of image-based aberration metrology for EUV lithography," Z Levinson, G Fenger, A Burbine, AR Schepis, BW Smith, SPIE Advanced Lithography, 2014.
5. "Study of angular effects for optical systems into the EUV," A Burbine, Z Levinson, A Schepis, BW Smith, SPIE Advanced Lithography, 2014.
6. "Alternative method for variable aspect ratio vias using a vortex mask," AR Schepis, Z Levinson, A Burbine, BW Smith - SPIE Advanced Lithography, 2014.
7. "Extreme ultraviolet lithography resist-based aberration metrology," Germain L. Fenger; Lei Sun; Sudharshanan Raghunathan; Obert R. Wood; Bruce W. Smith, J. Micro/Nanolith. MEMS MOEMS. 12 (4), 2013.
8. "The Impact of Pupil Plane Filtering on Mask Roughness Transfer," Burak Baylav, Chris Maloney, Zac Levinson, Joost Bekaert, Alessandro Vaglio Pret, and Bruce W. Smith, J. Vac. Sci. Technol. B 31, 06F801, 2013.
9. "Modeling the effects of pupil-manipulated spherical aberration in optical nanolithography", M. K. Sears, B.W. Smith, J. Micro/Nanolith. MEMS MOEMS. 12(1), 2013.
10. "Scanning interference evanescent wave lithography for sub-22-nm generations," P. Xie, B. W. Smith, J. Micro/Nanolithography, MEMS, and MOEMS. 12(1), 2013.
11. "Lens wavefront compensation for 3D photomask effects in subwavelength optical lithography," M.K. Sears, J. Bekaert, B.W. Smith, Applied Optics 52 (3), 314-322, 2013.
12. "Line edge roughness (LER) mitigation studies specific to interference-like lithography,": B Baylav, A Estroff, P Xie, BW Smith, Proc. SPIE 8683, Optical Microlithography XXVI, 86831Y, 2013
13. "Pupil wavefront manipulation to compensate for mask topography effects in optical nanolithography," MK Sears, BW Smith, Proc. SPIE 8683, Optical Microlithography XXVI, 86830G, 2013.
14. "EUVL resist-based aberration metrology," Germain L. Fenger ; Sudharshanan Raghunathan ; Lei Sun ; Obert R. Wood ; Bruce W. Smith, Proc. SPIE 8679, Extreme Ultraviolet (EUV) Lithography IV, 86790P, 2013.
15. "Tuning Metamaterials for Applications at DUV Wavelengths," A. Estroff, B.W. Smith, Intl. Journal of Optics, 2012.
16. "Aqueous developable dual switching photoresists for nanolithography", L. Chen, Y.K. Goh, H.H. Cheng, B.W. Smith, P. Xie, W. Montgomery, A.K. Whittaker, I. Blakey, Journal of Polymer Science Part A: Polymer Chemistry 1, 2012.
17. "The saga of lambda: spectral influences throughout lithography generations," B.W. Smith, Proc. SPIE 8325, 2012.
18. "Pupil wavefront manipulation for optical nanolithography," Monica Kempell Sears, Joost Bekaert, and Bruce W. Smith, Proc. SPIE 8326, 2012.
19. "Longer wavelength EUV lithography (LW-EUVL)," Christopher W. Maloney and Bruce W. Smith, Proc. SPIE 8322, 2012.
20. "Scanning interference evanescent wave lithography for sub-22 nm generations," Peng Xie and Bruce W. Smith, Proc. SPIE 8326, 2012.
21. "3D mask modeling for EUV lithography," Julien Mailfert, Christian Zuniga, Vicky Philipsen, Konstantinos Adam, Michael Lam, James Word, Eric Hendrickx, Geert Vandenberghe, and Bruce Smith, Proc. SPIE 8322, 2012.
22. "Aqueous Developable Dual Switching Photoresists for Nanolithography," Lan Chen, Yong Keng Goh, Han Hao Cheng, Bruce W. Smith, Peng Xie, Warren Montgomery, Andrew K. Whittaker, Idriss Blakey, Journal of Polymer Science Part A: Polymer Chemistry, 2012.
23. "Lithography beyond the IC", B.W. Smith, Proc. SPIE, v 7973-01, 2011.
24. "PAG-free chain scissioning resists for 193-nm immersion lithography that can be developed by aqueous base," I. Blakey, L. Chen, Y. K. Goh, A. Dorgelo, P. Xie, N. Lafferty, B. Smith, P. Zimmerman, M.W. Montgomery, A. Whittaker, Proc. SPIE, v 7972-86, 2011.
25. "Development of an inorganic nanoparticle photoresist for EUV, e-beam, and 193-nm lithography," M. Kryszak, M. Trikeriotis, E. Schwarz, N. Lafferty, P. Xie, B.W. Smith, P. Zimmerman, M.W. Montgomery, E. Giannelis, C. Ober, Proc. SPIE v 7972-48, 2011.

26. "Extending SMO into the pupil plane," M. Kempsell Sears, B.W. Smith, Proc. SPIE v 7973-46, 2011.
27. "Projection lithography below  $\lambda/7$  through deep-ultraviolet evanescent optical imaging," P. Xie and B. W. Smith, J. Vac. Sci. Technol. B 28, 2010.
28. "Photo-patternable inorganic hardmask," Alan Telecky, Peng Xie, Jason Stowers, Andrew Grenville, Bruce Smith, and Douglas A. Keszler, J. Vac. Sci. Technol. B 28, 2010.
29. "Alternatives to Chemical Amplification for 193 nm Lithography," Baylav, B.; Meng Zhao; Ran Yin; Peng Xie; Scholz, C.; Smith, B.; Smith, T.; Zimmerman, P. Source: Proceedings of the SPIE - The International Society for Optical Engineering, v 7639, 2010.
30. "Non-chemically amplified resists for 193-nm immersion lithography: influence of absorbance on performance," Lan Chen; Yong-Keng Goh; Lawrie, K.; Smith, B.; Montgomery, W.; Zimmerman, P.A.; Blakey, I.; Whittaker, A.K., Proceedings of the SPIE - The International Society for Optical Engineering, v 7639, 2010
31. "Metamaterials for enhancement of DUV lithography," Estroff, A.; Lafferty, N.V.; Peng Xie; Smith, B.W., Proceedings of the SPIE - The International Society for Optical Engineering, v 7640, 2010.
32. "Achieving Interferometric Double Patterning through Wafer Rotation," Peng; Lafferty, N.V.; Smith, B.W. , Proceedings of the SPIE - The International Society for Optical Engineering, v 7640, 2010.
33. "Development of an inorganic photoresist for DUV, EUV, and electron beam imaging," Trikeriotis, M.; Woo Jin Bae; Schwartz, E.; Krysak, M.; Lafferty, N.; Peng Xie; Smith, B.; Zimmerman, P.; Ober, C.K.; Giannelis, E.P., Proceedings of the SPIE - The International Society for Optical Engineering, v 7639, 2010.
34. "Analysis of higher order pitch division for sub-32 nm lithography," Peng Xie; Smith, B.W. , Proceedings of the SPIE - The International Society for Optical Engineering, v 7274, 2009.
35. "Alternative optical technologies: more than curiosities?," Smith, B.W., Proceedings of the SPIE - The International Society for Optical Engineering, v 7274, 2009
36. "Inverse lithography for 45-nm-node contact holes at 1.35 numerical aperture Kempself, M.L.; Hendrickx, E.; Trichtkov, A.; Sakajiri, K.; Yasui, K.; Yoshitake, S.; Granik, Yu.; Vandenberghe, G.; Smith, B.W., Journal of Microlithography, Microfabrication, and Microsystems, v 8, n 4, Oct. 2009.
37. "EUV resist requirements: absorbance and acid yield," Gronheid, R.; Fonseca, C.; Leeson, M.J.; Adams, J.R.; Strahan, J.R.; Willson, C.G.; Smith, B.W., Proceedings of the SPIE - The International Society for Optical Engineering, v 7273, 2009
38. "Design and analysis of a compact EUV interferometric lithography system," B.W. Smith, J. Micro/Nanolith. MEMS MOEMS, Vol. 8, 021207, 2009.
39. "Enhancement of hyper-NA imaging through selective TM polarization," B.W. Smith, J. Zhou, P. Xie, J. Vac. Soc. B: Microelectronics and Nanometer Structures, Volume 26 (6) 2008.
40. "Photomask image enhancement using grating generated surface waves," N. Lafferty, A. Estroff, A. Bourov. B.W. Smith, J. Vac. Soc. B: Microelectronics and Nanometer Structures, Volume 26 (6) 2008.
41. "Applications of TM polarized illumination," Bruce Smith, Jianming Zhou, and Peng Xie, Proc. SPIE 6924, 2008.
42. "Quantum state control interference lithography and trim double patterning for 32-16 nm nodes," Robert D. Frankel, Bruce W. Smith, and Andrew Estroff , Proc. SPIE 6520, 2007.
43. "Snell or Fresnel – The influence of material index on hyper NA lithography," B. W. Smith, J. Zhou, Proc. SPIE 6520, 2007.
44. "Immersion Lithography with Numerical Apertures above 2.0 using High Index Optical Materials," J. Zhou, N. Lafferty, B. W. Smith, J. H. Burnett, Proc. SPIE 6520, 2007.
45. "On the quality of measured optical aberration coefficients using phase wheel monitor," L. Zavyalova, A. Robinson, A. Bourov, N. Lafferty, B. W. Smith, Proc. SPIE 6520, 2007.
46. "Mask Enhancement Using and Evanescent Wave Effect," N. Lafferty, J. Zhou, B. W. Smith, Proc. SPIE 6520, 2007.
47. "Evanescent wave imaging in optical lithography," Bruce W Smith, Yongfa Fan, Jianming Zhou, Neal Lafferty, Andrew Estroff, Proc. SPIE Optical Microlithography XIX, 6154, 2006.

48. "Effects of beam pointing instability on two-beam interferometric lithography," Yongfa Fan, Anatoly Bourov, Michael Slocum, Bruce W Smith, Proc. SPIE Optical Microlithography XIX, 6154, 2006.
49. "Resist process window characterization for the 45-nm node using an interferometric immersion microstepper," Anatoly Bourov, Stewart A Robertson, Bruce W Smith, Michael A Slocum, Emil C Piscani, Proc. SPIE Advances in Resist Technology and Processing XXIII, 6153, 2006.
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51. "Three-dimensional imaging of 30-nm nanospheres using immersion interferometric lithography," Jianming Zhou, Yongfa Fan, Bruce W Smith, Proc. Optical Microlithography XIX, 6154, 2006.
52. "Experimental measurement of photoresist modulation curves," Anatoly Bourov, Stewart A Robertson, Bruce W Smith, Michael Slocum, Emil C Piscani, Proc. Optical Microlithography XIX, 6154, 2006.
53. "Practical approach to full-field wavefront aberration measurement using phase wheel targets," Lena V Zavyalova, Bruce W Smith, Anatoly Bourov, Gary Zhang, Venugopal Vellanki, Patrick Reynolds, Donis G Flagello, Proc. Optical Microlithography XIX, 6154, 2006.
54. "High NA 193nm Immersion Lithography for 32nm Half-Pitch Imaging" J. Zhou, Y. Fan, A. Bourov, B.W. Smith, Appl. Opt., 2006.
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58. "Air bubble-induced light-scattering effect on image quality in 193 nm immersion lithography," Yongfa Fan, Neal Lafferty, Anatoly Bourov, Lena Zavyalova, Bruce W. Smith , Appl. Opt., Vol. 44 Issue 19 , 3904, 2005.
59. "Photoresist Modulation Curves," A. Bourov, Y. Fan, F. C. Cropanese, B. W. Smith, Proc. SPIE Optical Microlithography, vol. 5754, 2005.
60. "Automated Aberration Extraction using Phase Wheel Targets," L. Zavyalova, A. Bourov, B.W. Smith, Proc. SPIE Optical Microlithography, vol. 5754, 2005.
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## INVITED PRESENTATIONS

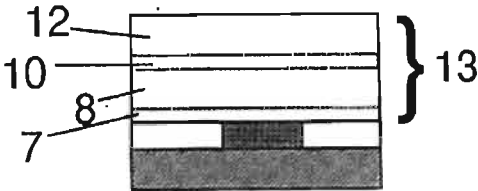
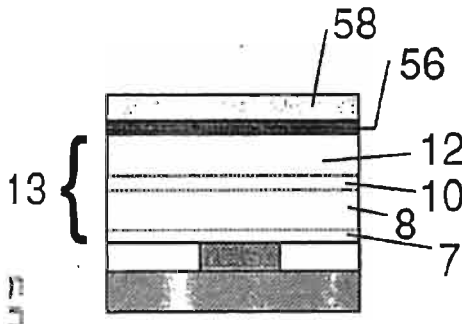
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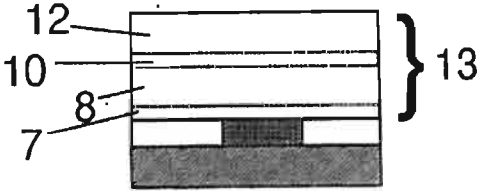
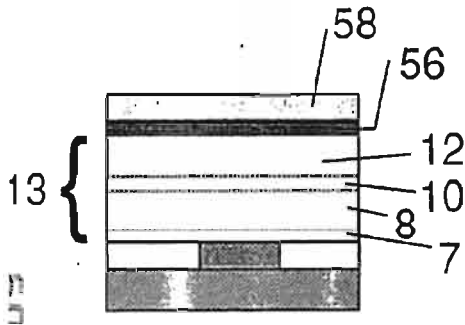
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# Appendix B

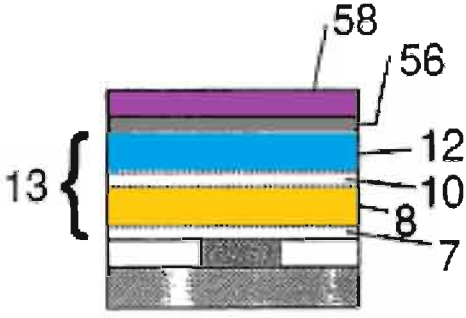
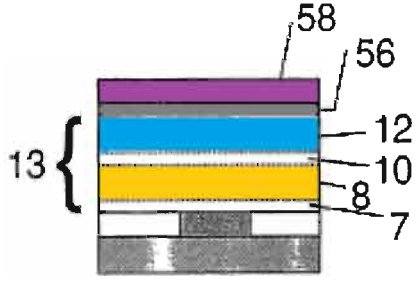
## APPENDIX B

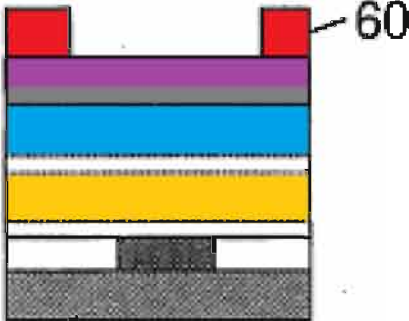
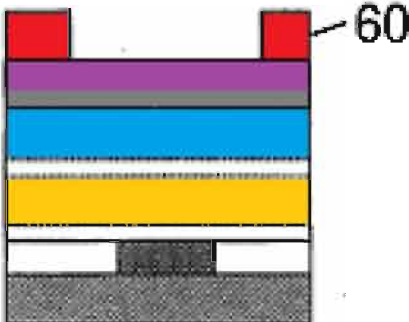
<i>Grill Claim 28 Element</i>	<b>Disclosure of U.S. Provisional Application 60/071,628 (“’628 application”)</b>
28. A method for forming an interconnect structure on the upper surface of a substrate having conductive regions comprising the steps of:	“Figs. 5A - 5E show a first preferred embodiment of a method for forming a dual pattern hard mask comprising a first layer of material with a first pattern, and a second layer of material with a second pattern; Figs. 5F - 5H show how this dual pattern hard mask may be used to fabricate a dual relief cavity for use in a Dual Damascene process. For purposes of illustration, one of said first and second patterns will be a via level pattern, and the other of said first and second patterns will be a wiring level pattern.” ’628 application at 6.
forming over said substrate a <b>first dielectric layer</b> having a thickness corresponding to the thickness of an interconnect via,	<p>“The process flow may be exercised on a variety of substrates but is illustrated for the simplified substrate of Fig. 1A which comprises a semiconductor base 2 containing arrays of electrical devices (not shown) conductive via , and dielectric passivation layer 6.</p> <p>“A layered dielectric stack 13 comprising an optional dielectric passivation/adhesion layer 7, a via level dielectric 8, an optional dielectric etch stop layer 10, and a wiring level dielectric 12 are then applied to produce the structure of Fig. 1B. Via and wiring dielectrics 8 and 12 might be carbon-based materials such as DLC or fluorinated DLC (FDLC), and optional dielectric etch stop 10 may be materials such as SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, silicon-containing DLC (SiDLC), etc. The total thickness of layered dielectric stack 13 closely approximates the sum of the via and wiring level thickness.” ’628 application at 3.</p>

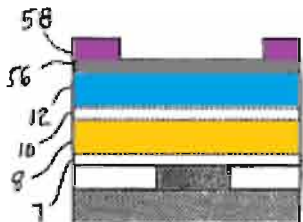
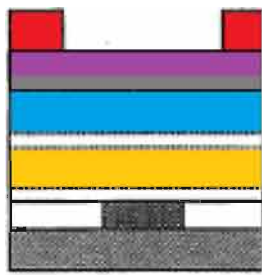
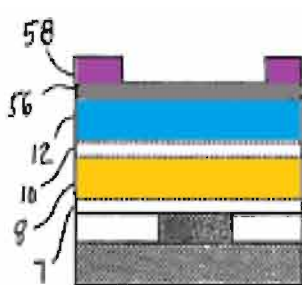
Grill Claim 28 Element	Disclosure of U.S. Provisional Application 60/071,628 (“’628 application”)
	<p data-bbox="911 279 1040 317">FIG 1B</p>  <p data-bbox="651 575 1057 613">’628 application at Fig. 1B.</p> <p data-bbox="927 657 1057 695">FIG 5A</p>  <p data-bbox="651 1073 1393 1234">’628 application at Fig. 5A; <i>see also</i> ’628 application at 6 (“Fig. 5A shows the structure of Fig. 1B after application of lower hard mask layer 56 and upper hard mask layer 58”.)</p>
<p data-bbox="220 1276 607 1528">forming over said <b>first dielectric layer</b> a <b>second dielectric layer</b> having a thickness corresponding to the thickness of an interconnect wiring layer,</p>	<p data-bbox="651 1276 1377 1528">“The process flow may be exercised on a variety of substrates but is illustrated for the simplified substrate of Fig. 1A which comprises a semiconductor base 2 containing arrays of electrical devices (not shown) conductive via , and dielectric passivation layer 6.</p> <p data-bbox="651 1549 1386 1881">“A layered dielectric stack 13 comprising an optional dielectric passivation/adhesion layer 7, a via level dielectric 8, an optional dielectric etch stop layer 10, and a wiring level dielectric 12 are then applied to produce the structure of Fig. 1B. Via and wiring dielectrics 8 and 12 might be carbon-based materials such as DLC or fluorinated DLC (FDLC), and optional dielectric</p>

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	<p data-bbox="646 254 1398 464">etch stop 10 may be materials such as SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, silicon-containing DLC (SiDLC), etc. The total thickness of layered dielectric stack 13 closely approximates the sum of the via and wiring level thickness.” ’628 application at 3.</p> <div data-bbox="781 506 1256 751"> <p data-bbox="911 506 1040 548">FIG 1B</p>  </div> <p data-bbox="646 806 1057 848">’628 application at Fig. 1B.</p> <div data-bbox="781 884 1243 1283"> <p data-bbox="927 884 1057 926">FIG 5A</p>  </div> <p data-bbox="646 1297 1398 1472">’628 application at Fig. 5A; <i>see also</i> ’628 application at 6 (“Fig. 5A shows the structure of Fig. 1B after application of lower hard mask layer 56 and upper hard mask layer 58”.)</p>
<p data-bbox="219 1507 623 1633">forming a first hard mask layer over said <a href="#">second [dielectric] layer</a>,</p>	<p data-bbox="646 1507 1398 1801">“Fig. 5A shows the structure of Fig. 1B after application of lower hard mask layer 56 and upper hard mask layer 58. Hard mask layers 56 and 58 are preferably formed from different materials which have different etch properties from each other and from dielectric underlayers 12 and 8.” ’628 application at 6.</p>

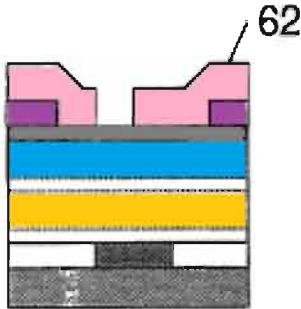
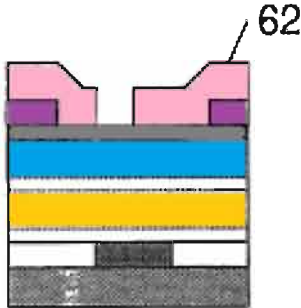


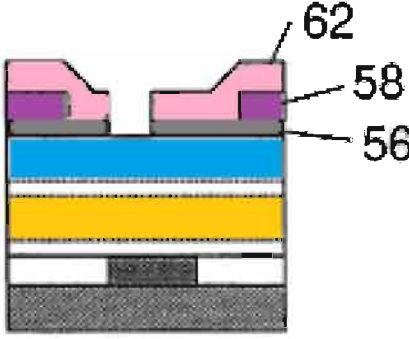
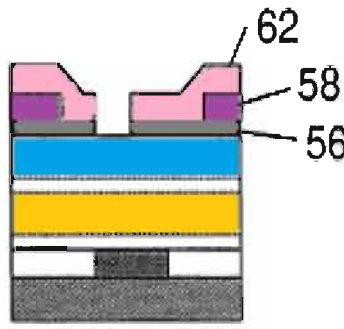
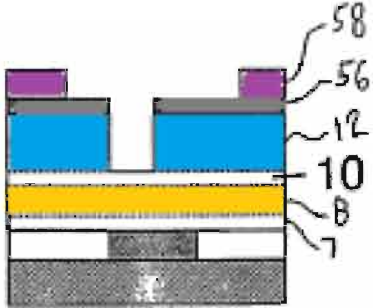
Grill Claim 28 Element	Disclosure of U.S. Provisional Application 60/071,628 (“’628 application”)
	<p style="text-align: center;">FIG 5A</p> 
<p>forming a <b>second hard mask layer</b> over said first hard mask layer, said <b>second hard mask layer</b> preferably formed of a material different from said first hard mask to permit selective etching of said <b>second hard mask layer</b> with respect to said first hard mask layer,</p>	<p>“Fig. 5A shows the structure of Fig. 1B after application of lower hard mask layer 56 and upper hard mask layer 58. Hard mask layers 56 and 58 are preferably formed from different materials which have different etch properties from each other and from dielectric underlayers 12 and 8. For example, lower hard mask layer 56 might be formed from Si<sub>3</sub>N<sub>4</sub> and upper hard mask layer 58 might be formed from SiO<sub>2</sub>. . . . The etching process is preferably selective, for example a selective SiO<sub>2</sub> to Si<sub>3</sub>N<sub>4</sub> etch, so that lower hard mask layer 56 will remain intact during any overetching of hard mask layer 58.” ’628 application at 6.</p> <p style="text-align: center;">FIG 5A</p> 
<p>forming a <b>first layer of resist</b> over said <b>second hard mask layer</b>,</p>	<p>“A first resist layer 60, patterned with a first (wiring level) pattern, is formed on layer 58 to form the structure of Fig. 5B.” ’628 application at 6.</p>

<i>Grill Claim 28 Element</i>	Disclosure of U.S. Provisional Application 60/071,628 (“’628 application”)
	<p style="text-align: center;">FIG 5B</p>  <p>’628 application at Fig. 5B.</p>
<p>patterning said <b>first layer of resist</b> with a wiring pattern,</p>	<p>“A first resist layer 60, patterned with a first (wiring level) pattern, is formed on layer 58 to form the structure of Fig. 5B.” ’628 application at 6.</p> <p style="text-align: center;">FIG 5B</p>  <p>’628 application at Fig. 5B.</p>
<p>patterning said <b>second hard mask layer</b> using said wiring-patterned <b>first</b></p>	<p>“The pattern of resist layer 60 is transferred into upper hard mask layer 58 by an etching process to form the structure of Fig. 5C. The etching process</p>

<b>Grill Claim 28 Element</b>	<b>Disclosure of U.S. Provisional Application 60/071,628 (“’628 application”)</b>
<p>layer of resist as a mask,</p>	<p>is preferably selective, for example a selective SiO<sub>2</sub> to Si<sub>3</sub>N<sub>4</sub> etch, so that lower hard mask layer 56 will remain intact during any overetching of hard mask layer 58.” ’628 application at 6.</p> <p style="text-align: center;">FIG 5C</p>  <p>’628 application at Fig. 5C.</p>
<p>removing said wiring-patterned first layer of resist,</p>	<div style="display: flex; justify-content: space-around; align-items: flex-start;"> <div style="text-align: center;"> <p>FIG 5B</p>  </div> <div style="text-align: center;"> <p>FIG 5C</p>  </div> </div> <p>’628 application at Figs. 5B, 5C.</p> <p>“Hard mask layers 56 and 58 are preferably formed from different materials which have different etch properties from each other and from the dielectric underlayers 12 and 8. For example, lower hard mask layer 56 might be formed from Si<sub>3</sub>N<sub>4</sub> and upper hard mask layer 58 might be formed from SiO<sub>2</sub>. Other suitable hard mask materials may include SiO<sub>2</sub>-based materials, other oxides, nitrides other than Si<sub>3</sub>N<sub>4</sub>, carbon-based dielectrics, and polycrystalline silicon, and</p>

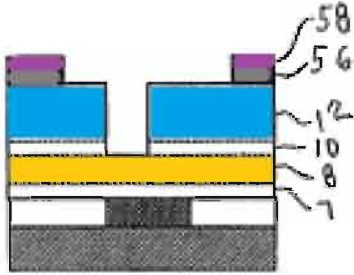
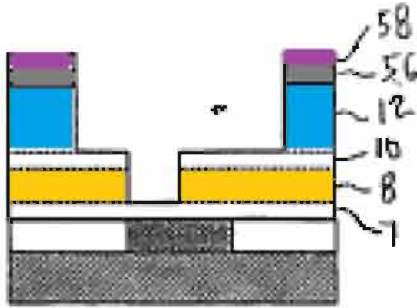
<i>Grill</i> Claim 28 Element	Disclosure of U.S. Provisional Application 60/071,628 (“’628 application”)
	<p>amorphous hydrogenated silicon. . . . If resist layer 60 is misaligned, rework at this stage presents no problem.” ’628 application at 6.</p> <p>Although the non-provisional application for the <i>Grill</i> patent later adds a statement that the “[p]atterned resist layer 60 is . . . removed by a process such as ashing or wet chemical etching,” a person of ordinary skill in the art would have already understood this to be part of the ’628 application’s disclosures.</p> <p>The ’628 application teaches that rework problems are caused when the photoresist and dielectric material have similar etch properties. ’628 application at 2. Accordingly, a person of ordinary skill in the art would have understood that resist rework is not a problem at this stage because the upper hard mask layer 58 and photoresist layer 60 have different etch properties. A person of ordinary skill in the art thus would have understood that the photoresist layer 60 is not removed when upper hard mask layer 58 is etched. A person of ordinary skill in the art would have understood that the transition between Figures 5B and 5C above is only possible by first etching layer 58, then subsequently removing the photoresist layer 60.</p>
forming a <b>second layer of resist</b> over said first and <b>second</b> hard mask layer,	<p>“A second resist layer 62, patterned with a second (via level) pattern, is then formed on the structure of Fig. 5C to produce the structure of Fig. 5D.” ’628 application at 6.</p>

<i>Grill Claim 28 Element</i>	Disclosure of U.S. Provisional Application 60/071,628 (“’628 application”)
	<p data-bbox="906 254 1036 296">FIG 5D</p>  <p data-bbox="651 646 1057 688">’628 application at Fig. 5D.</p>
<p data-bbox="224 722 586 848">patterning said second layer of resist with a via pattern,</p>	<p data-bbox="651 722 1393 890">“A second resist layer 62, patterned with a second (via level) pattern, is then formed on the structure of Fig. 5C to produce the structure of Fig. 5D.” ’628 application at 6.</p> <p data-bbox="906 911 1036 953">FIG 5D</p>  <p data-bbox="651 1304 1057 1346">’628 application at Fig. 5D.</p>
<p data-bbox="224 1436 613 1604">patterning said first hard mask layer using said via-patterned second layer of resist as a mask,</p>	<p data-bbox="651 1436 1377 1562">“The pattern of resist layer 62 is then transferred into lower hard mask layer 56.” ’628 application at 6.</p>

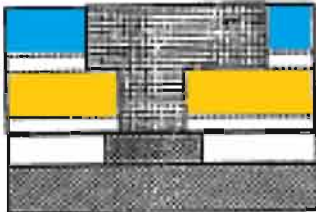
Grill Claim 28 Element	Disclosure of U.S. Provisional Application 60/071,628 (“’628 application”)
	<p style="text-align: center;"><b>FIG 5E</b></p>  <p>’628 application at Fig. 5E.</p>
<p>transferring said via pattern in said patterned first hard mask layer into said second dielectric layer, while concurrently removing said via-patterned second layer of resist, and</p>	<p>“The via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching, to produce the structure of Fig. 5F.” ’628 application at 6.</p> <div style="display: flex; justify-content: space-around; align-items: flex-start;"> <div style="text-align: center;"> <p><b>FIG 5E</b></p>  </div> <div style="text-align: center;"> <p><b>FIG 5F</b></p>  </div> </div> <p>’628 application at Figs. 5E, 5F.</p> <p>Although the non-provisional application for the ’696 patent added a statement that the “[p]atterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12,” <i>Grill</i> at 7:64–66, a person of ordinary skill in the art would have already understood this to be part of the ’628 application’s disclosures.</p> <p>The ’628 application teaches that the</p>



<i>Grill Claim 28 Element</i>	<b>Disclosure of U.S. Provisional Application 60/071,628 (“’628 application”)</b>
	<p>“interconnect dielectric and the photoresist stencil used to pattern the hard mask [may] have similar etch characteristics,” such as “the case with an organic photoresist and a carbon-based interconnect dielectric such as DLC.” ’628 application at 2. A person of ordinary skill in the art would have understood that etching layer 12 under such circumstances concurrently etches layer 58 because the two layers have similar etch properties.</p> <p>A person of ordinary skill in the art would have further understood that the photoresist layer 62 is not removed prior to etching layer 12. If a dry etch is performed to ash the photoresist layer 62, the process would concurrently etch layer 12, as claim 28 requires. On the other hand, if the photoresist is stripped with a wet chemical treatment before etching layer 12, the problems described with regard to Figures 2C result. ’682 application at 4, Figs. 2C, 2D. This would damage the exposed interlayer dielectric layer 12 and make it difficult to control the via dimension.</p> <p>A person of ordinary skill in the art would have thus understood that the transition between Figures 5E and 5F above is only possible by concurrently etching photoresist layer 62 and dielectric layer 12.</p>
<p>patterning said via-patterned first hard mask layer using said wiring-patterned second hard mask layer as a mask,</p>	<p>“The etching conditions are then changed to removed [sic] exposed portions of lower hard mask layer 56 and optional etch stop 10, to form the structure of Fig. 5G.” ’628 application at 6.</p>

Grill Claim 28 Element	Disclosure of U.S. Provisional Application 60/071,628 (“’628 application”)
	<p style="text-align: center;"><b>FIG 5G</b></p>  <p>’628 application at Fig. 5G.</p>
<p>transferring, at least partially concurrently, said via pattern into said <b>first dielectric layer</b> to form via cavities corresponding to said via pattern, and said wiring pattern into said <b>second dielectric layer</b> to form wiring cavities corresponding to said wiring pattern, and</p>	<p>“Dielectrics 8 and 12 are then etched to transfer said second pattern [via level] into the entire thickness of dielectric 12, and said first pattern [wiring level] into the entire thickness of dielectric 8, as shown in Fig. 5H.” ’628 application at 6.</p> <p style="text-align: center;"><b>FIG 5H</b></p>  <p>’628 application at Fig. 5H.</p>
<p>filling said cavities with conductive material to make electrical contact with said conductive regions and to form said vias and said wiring</p>	<p>“The cavity structure may then be completed as shown in FIG. 1J, and, for interconnect applications, filled with wiring material as shown in FIGS. 1K to 1L.” ’628 application at 6.</p>



<i>Grill Claim 28 Element</i>	Disclosure of U.S. Provisional Application 60/071,628 (“’628 application”)
pattern.	<p data-bbox="894 262 1052 310">FIG 1L</p>  <p data-bbox="651 646 1052 688">’628 application at Fig. 1L.</p>