

## CERTIFICATION OF TRANSLATION

The undersigned, Richard Patner, whose address is 26357 Lexington Drive, Bonita Springs, FL 34135, United States of America, declares and states as follows:

I am well acquainted with the English and Japanese languages; I have in the past translated numerous Japanese documents of legal and/or technical content into English.

I have been requested to translate into English the attached Japanese Patent No. 10-079371 titled "**Method of forming wiring structure**."

To a copy of this Japanese document I therefore attach an English translation and my Certification of Translation.

I hereby certify that the attached English translation of Japanese Patent No. 10-079371 titled "**Method of forming wiring structure**" is, to the best of my knowledge and ability, an accurate translation.

And I declare further that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that false statements and the like are punishable by fine and imprisonment, or both, under Section 1001 of Title 18 of the United States Code.



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[Title of Invention] Method of forming wiring structure

[Scope of Patent Claims]

[Claim 1] A method of forming a wiring structure comprising 11 steps:

a first step of forming a first insulating film over lower-level metal wiring,

a second step of forming a second insulating film having a different structure from that of said first insulating film over the aforementioned first insulating film,

a third step of forming a third insulating film having a different structure from that of said second insulating film over the aforementioned second insulating film,

a fourth step of forming a conducting film over the aforementioned third insulating film,

a fifth step of forming a first resist pattern having an opening for the formation of wiring over the aforementioned conducting film,

a sixth step of forming a mask pattern from the aforementioned conducting film with an opening for the formation of wiring by etching the aforementioned conducting film using the aforementioned first resist pattern as a mask,

a seventh step of forming a second resist pattern with an opening for the formation of contact holes over the aforementioned third insulating film,

an eighth step of patterning the aforementioned third insulating film so as to form an opening for the formation of contact holes in said third insulating film by dry etching the aforementioned third insulating film using the first resist pattern or the second resist pattern under etching conditions such that the pattern with the higher etching rate is used while the pattern with the lower etching rate is used in etching of the aforementioned second insulating film, and by removing the entire first resist pattern and second resist pattern or leaving the lower portion,

a ninth step of patterning the aforementioned second insulating film so as to form an opening for the formation of contact holes in said second insulating film by dry etching, using the aforementioned third insulating film that had been patterned as a mask, of the aforementioned second insulating film under etching conditions such that the etching rate of the aforementioned second insulating film is higher while the etching rate of the aforementioned first insulating film and the third insulating film is lower,

a tenth step of forming wiring grooves in the aforementioned third insulating film and of forming contact holes in the aforementioned first insulating film by dry etching using the aforementioned mask pattern for the aforementioned third insulating film as a mask and by dry etching using the aforementioned second insulating film that had been patterned for the aforementioned first insulating film as a mask under etching conditions such that the etching rate of the aforementioned first insulating film and the third insulating film is higher while the etching rate of the mask pattern and of the second insulating film is lower,

and an eleventh step of forming contacts that connect the upper-level metal wiring and the aforementioned lower-level metal wiring with the aforementioned upper-level metal wiring by packing metal film in the aforementioned wiring grooves and contact holes.

[Claim 2] The method of forming a wiring structure of Claim 1 in which a step of forming adhesion layers comprising metal film in the section of the aforementioned third insulating film exposed in the aforementioned wiring grooves and in the section of the aforementioned first insulating film exposed in the aforementioned contact holes is inserted between the aforementioned tenth step and the aforementioned eleventh step.

[Claim 3] The method of forming a wiring structure of Claim 1 in which the principal constituents of the aforementioned third insulating film are organic constituents.

[Claim 4] The method of forming a wiring structure of Claim 3 in which the aforementioned third step also includes the step of forming the aforementioned third insulating film by the CVD method using reactive gas that contains perfluorodecalin.

[Claim 5] The method of forming a wiring structure of Claim 3 in which the principal constituents of the aforementioned first insulating film are organic constituents.

[Claim 6] The method of forming a wiring structure of Claim 5 in which a step of forming an adhesion layer by plasma treatment using reactive gas containing nitrogen in the section of the aforementioned third insulating film exposed in the aforementioned wiring grooves and in the section of the aforementioned first insulating film exposed in the aforementioned contact holes is further included between the aforementioned tenth step and the aforementioned eleventh

step.

[Claim 7] The method of forming a wiring structure of Claim 3 in which the aforementioned first step includes a step of forming the aforementioned third insulating film by the CVD method using reactive gas that contains perfluorodecalin.

[Claim 8] A method of forming a wiring structure comprising 12 steps:

a first step of forming a first insulating film over lower-level metal wiring,

a second step of forming a second insulating film having a different structure from that of said first insulating film over the aforementioned first insulating film,

a third step of forming a third insulating film having a different structure from that of said second insulating film over the aforementioned second insulating film,

a fourth step of forming a conducting film over the aforementioned third insulating film,

a fifth step of forming a first resist pattern having an opening for the formation of wiring over the aforementioned conducting film,

a sixth step of forming a mask pattern from the aforementioned conducting film with an opening for the formation of wiring by etching the aforementioned conducting film using the aforementioned first resist pattern as a mask,

a seventh step of forming a second resist pattern with an opening for the formation of contact holes over the aforementioned third insulating film,

an eighth step of patterning the aforementioned third insulating film so as to form an opening for the formation of contact holes in said third insulating film by dry etching the aforementioned third insulating film using the aforementioned first resist pattern or the second resist pattern as the mask under etching conditions such that the aforementioned third insulating film has a higher etching rate while the second insulating film has a lower etching rate relative to the first resist pattern and the second resist pattern,

a ninth step of patterning the aforementioned second insulating film so as to form an opening for the formation of contact holes in said second insulating film by dry etching the aforementioned second insulating film using the aforementioned first resist pattern or the second resist pattern as the mask under etching conditions such that the aforementioned second insulating film has a higher etching rate while the first insulating film and third insulating film have lower etching rates relative to the first resist pattern and the second resist pattern,

a tenth step of removing the aforementioned first resist pattern and the aforementioned second resist pattern,

an eleventh step of forming wiring grooves in the aforementioned third insulating film and of forming contact holes in the aforementioned first insulating film by dry etching of the aforementioned third insulating film using the aforementioned mask pattern as a mask and by dry etching of the aforementioned first insulating film using the aforementioned patterned second insulating film as a mask under etching conditions such that the etching rate of the aforementioned first insulating film and the third insulating film is higher while the etching rate of the aforementioned mask pattern and of the second insulating film is lower,

and a twelfth step of forming contacts that connect the upper-level metal wiring and the aforementioned lower-level metal wiring with the aforementioned upper-level metal wiring by packing metal film in the aforementioned wiring grooves and contact holes.

[Claim 9] The method of forming a wiring structure of Claim 8 in which the aforementioned third insulating film is a low-dielectric-constant SOG film with a siloxane framework.

#### **[Detailed Description of the Invention]**

**[0001]**

#### **[Technical Field of Invention]**

The present invention concerns a method of forming a wiring structure in semiconductor integrated circuit devices.

**[0002]**

#### **[Related Art]**

Accompanying higher integration of semiconductor integrated circuits, expansion of the wiring delay times attributable to increase in the interwiring capacitance, which is parasitic capacitance between metal wiring, has blocked higher performance of semiconductor integrated circuits. The wiring delay time is known as the so-called RC delay, which is proportional to the product of the metal wiring resistance and the interwiring capacitance.

**[0003]**

Accordingly, the resistance of the metal wiring must be reduced or the inter-wiring capacitance must be reduced in order to reduce the wiring delay time.

**[0004]**

Thus, IBM and Motorola have reported semiconductor integrated circuit devices that use copper instead of aluminum alloy as material for wiring in order to reduce the wiring resistance. Copper material has a specific resistance about two-thirds as high as that of an aluminum alloy material. Accordingly, in accordance with simple calculation, the wiring

delay involved with the use of a copper material for wiring material can be about two-thirds of that involved with the use of an aluminum alloy material therefor. That is to say, the operating speed can be increased by about 1.5 times.

**[0005]**

However, there is a concern that even the use of copper in metal wiring would not be able to catch up with the drastically increasing integration of semiconductor integrated circuits. Also, the specific resistance of copper as wiring material is just a little bit higher than, but almost equal to, that of gold or silver. Accordingly, even if gold or silver is used instead of copper as a metal wiring material, the wiring resistance would be reduced only slightly.

**[0006]**

Under these circumstances, not only reducing wiring resistance but also suppressing inter-wiring capacitance are essential in further increasing the number of devices that can be integrated within a single semiconductor integrated circuit. In addition, the relative dielectric constant of an interlevel insulating film must be reduced to suppress the inter-wiring capacitance. A silicon dioxide film has heretofore been used as a typical material for an interlevel insulating film. However, the relative dielectric constant of a silicon dioxide film is about 4 to 4.5. Thus, it would be difficult to apply a silicon dioxide film to a semiconductor integrated circuit that has a higher degree of integration.

**[0007]**

In order to solve such problems, fluorine-doped silicon dioxide film, low-dielectric-constant SOG film, and organic polymer film have been proposed as alternate interlevel insulating films with smaller relative dielectric constants than that of silicon dioxide film.

**[0008]**

#### **[Problems Solved by the Invention]**

The relative dielectric constant of a fluorine-doped silicon dioxide film is about 3.3 to 3.7, which is about 20 percent lower than that of a conventional silicon dioxide film. However, a fluorine-doped silicon dioxide film is highly hygroscopic and easily absorbs water in the air, resulting in various problems in practice. For example, when the fluorine-doped silicon dioxide film absorbs water, SiOH groups having a high relative dielectric constant are introduced into the film. As a result, the relative dielectric constant of the fluorine-doped silicon dioxide film adversely increases or the SiOH groups react with the water during a heat treatment to release H<sub>2</sub>O gas. In addition, fluorine free radicals contained in the fluorine-doped silicon dioxide film segregate near the surface thereof during a heat treatment and react with Ti contained in a TiN layer formed thereon as an adhesion layer to form a TiF film, which easily peels off.

**[0009]**

An HSQ (hydrogen silsesquioxane film, composed of Si, O and H atoms in which the number of H atoms is about two-thirds that of O atoms) is a low-dielectric-constant SOG film that has been examined. However, HSQ film releases a larger amount of water than a conventional silicon dioxide film. Accordingly, since it is difficult to form buried wiring in the HSQ film, a patterned metal film must be formed as metal wiring on HSQ film.

**[0010]**

Also, since the HSQ film cannot adhere strongly to metal wiring, a CVD oxide film should be formed between the metal wiring and the HSQ film to improve the adhesion therebetween. However, in such a case, the problem of greater interwiring capacitance compared to the case of using HSQ film alone arises because the interwiring capacitance essentially becomes the serial capacitance of HSQ film and CVD oxide film because of the presence of CVD oxide film that has great specific interwiring inductive capacitance.

**[0011]**

An organic polymer film as well as the low-dielectric constant SOG film similarly cannot adhere strongly to metal wiring. Accordingly, a CVD oxide film must be formed as an adhesion layer between the metal wiring and the organic polymer film as well.

**[0012]**

Moreover, the problem arises of the inability to use the conventional resist process because an organic polymer film would be damaged when removing a resist pattern by ashing since the etching rate of an organic polymer film is virtually equal to the ashing rate when ashing a resist pattern using an oxygen plasma. Thus, a method of etching resist film has been proposed in which a CVD oxide film is formed over an organic polymer film, followed by the formation of a resist film over said CVD oxide film so that said CVD oxide film would act as an etching stopper,

**[0013]**

However, during the step of forming the CVD oxide film over the organic polymer film, the surface of the organic polymer film is exposed to a reactive gas containing oxygen, as a result of which the organic polymer film reacts with oxygen to take in polar groups such as carbonyl groups and ketone groups. As a result, the problem arises of increase in the relative dielectric constant of the organic polymer film.

**[0014]**

Also, in forming embedded copper wiring in the organic polymer film, a TiN adhesion layer, for example, should be formed around wiring grooves formed in the organic polymer film because the organic polymer film cannot adhere strongly to the metal wiring. However, since the TiN film has high resistance, the effective cross-sectional area of the metal wiring decreases. Consequently, the intended effect attainable by the use of the copper lines, i.e., reduction in resistance, would be lost.

**[0015]**

In light of the aforementioned circumstances, an objective of the present invention is to enable the formation of an interlevel insulating film having a low relative dielectric constant while using the conventional resist process.

**[0016]**

**[Means of Solving the Problems]**

The first method of forming a wiring structure pursuant to the present invention comprises 11 steps: a first step of forming a first insulating film over lower-level metal wiring, a second step of forming a second insulating film having a different structure from that of said first insulating film over the first insulating film, a third step of forming a third insulating film having a different structure from that of said second insulating film over the second insulating film, a fourth step of forming a conducting film over the third insulating film, a fifth step of forming a first resist pattern having an opening for the formation of wiring over the conducting film, a sixth step of forming a mask pattern from the aforementioned conducting film with an opening for the formation of wiring by etching the conducting film using the first resist pattern as a mask, a seventh step of forming a second resist pattern with an opening for the formation of contact holes over the third insulating film, an eighth step of patterning the third insulating film so as to form an opening for the formation of contact holes in said third insulating film by dry etching the third insulating film using the first resist pattern or the second resist pattern under etching conditions such that the pattern with the higher etching rate is used while the pattern with the lower etching rate is used in etching of the second insulating film, and by removing the entire first resist pattern and second resist pattern or leaving the lower portion, a ninth step of patterning the second insulating film so as to form an opening for the formation of contact holes in said second insulating film by dry etching, using the third insulating film that had been patterned as a mask, of the second insulating film under etching conditions such that the etching rate of the second insulating film is higher while the etching rate of the first insulating film and the third insulating film is lower, a tenth step of forming wiring grooves in the third insulating film and of forming contact holes in the first insulating film by dry etching using the mask pattern for the third insulation as a mask and by dry etching using the second insulating film that had been patterned for the first insulating film as a mask under etching conditions such that the etching rate of the first insulating film and the third insulating film is higher while the etching rate of the mask pattern and of the second insulating film is lower, and an eleventh step of forming contacts that connect the upper-level metal wiring and the lower-level metal wiring with the upper-level metal wiring by packing metal film in the wiring grooves and contact holes.

**[0017]**

In the eighth step of forming the first wiring structure, the third insulating film is patterned by dry etching using the first resist pattern or the second resist pattern under etching conditions such that the pattern with the higher etching rate is used while the pattern with the lower etching rate is used in etching of the second insulating film, and both the first resist pattern and the second resist pattern are then removed, as a result of which the step of removing the first resist pattern and the second resist pattern by ashing with oxygen plasma is obviated.

**[0018]**

In addition, the second insulating film can be used as an etching stopper in the tenth step when forming wiring grooves by dry etching using the mask pattern for the third insulating film as a mask because the structures of the second insulating film and of the third insulating film differ.

**[0019]**

The inclusion in the first method of forming a wiring structure of a step between the tenth step and the eleventh step in which an adhesion layer comprising metal film is formed in the section of the third insulating film exposed in the wiring grooves and in the section of the first insulating film exposed in the contact holes would be desirable.

**[0020]**

Setting the principal constituents of the third insulating film to be organic constituents would be desirable in the first method of forming a wiring structure.

**[0021]**

In this case, the inclusion of a third step of forming the third insulating film by the CVD method using reactive gas that contains perfluorodecalin would be desirable.

**[0022]**

Setting the principal constituents of the first insulating film to be organic constituents in this case would be desirable.

**[0023]**

The further inclusion between the tenth step and the eleventh step of a step of forming an adhesion layer by plasma treatment using reactive gas containing nitrogen in the section of the third insulating film exposed in the wiring grooves and in the section of the first insulating film exposed in the contact holes would be desirable.

**[0024]**

When the principal constituent of the first insulating film is an organic constituent, the inclusion in the first step of a step of forming the third insulating film by the CVD method using reactive gas that contains perfluorodecalin would be desirable.

**[0025]**

The second method of forming a wiring structure pursuant to the present invention comprises 12 steps: a first step of forming a first insulating film over lower-level metal wiring, a second step of forming a second insulating film having a different structure from that of said first insulating film over the first insulating film, a third step of forming a third insulating film having a different structure from that of said second insulating film over the second insulating film, a fourth step of forming a conducting film over the third insulating film, a fifth step of forming a first resist pattern having an opening for the formation of wiring over the conducting film, a sixth step of forming a mask pattern from the conducting film with an opening for the formation of wiring by etching the conducting film using the first resist pattern as a mask, a seventh step of forming a second resist pattern with an opening for the formation of contact holes over the third insulating film, an eighth step of patterning the third insulating film so as to form an opening for the formation of contact holes in said third insulating film by dry etching the third insulating film using the first resist pattern or the second resist pattern as the mask under etching conditions such that the third insulating film has a higher etching rate while the second insulating film has a lower etching rate relative to the first resist pattern and the second resist pattern, a ninth step of patterning the second insulating film so as to form an opening for the formation of contact holes in said second insulating film by dry etching the second insulating film using the first resist pattern or the second resist pattern as the mask under etching conditions such that the second insulating film has a higher etching rate while the first insulating film and third insulating film have lower etching rates relative to the first resist pattern and the second resist pattern, a tenth step of removing the first resist pattern and the second resist pattern, an eleventh step of forming wiring grooves in the third insulating film and of forming contact holes in the first insulating film by dry etching of the third insulating film using the mask pattern as a mask and by dry etching of the first insulating film using the patterned second insulating film as a mask under etching conditions such that the etching rate of the first insulating film and the third insulating film is higher while the etching rate of the mask pattern and of the second insulating film is lower, and a twelfth step of forming contacts that connect the upper-level metal wiring and the lower-level metal wiring with the upper-level metal wiring by packing metal film in the wiring grooves and contact holes.

**[0026]**

Even if a damaged layer is formed in the section exposed in an opening for the formation of contact holes in the second insulating film of the first insulating film and the third insulating film in the tenth step of removing the first resist pattern and the second resist pattern in the second method of forming a wiring structure, a damaged layer formed in the first insulating film and the third insulating film is reliably removed since wiring grooves are formed in the third insulating film and since contact holes are formed in the first insulating film by dry etching using a mask pattern for the third insulating film as a mask and by dry etching using a second insulating film that had been patterned for the first insulating film as a mask under etching conditions such that the etching rate is higher for the first insulating film and the third insulating film as well as etching conditions such that the etching rate of the mask pattern and the second insulating film is lower.

**[0027]**

The third insulating film in the second method of forming a wiring structure preferably would be a low-dielectric-constant SOG film with a siloxane framework.

**[0028]****[Description of the Preferred Embodiments]**

(First Embodiment)

The method of forming a wiring structure pursuant to the first embodiment of the present invention is explained below with reference to Figure 1 (a) to (c), Figure 2 (a) to (c) and Figure 3 (a) to (c).

**[0029]**

First, as shown in Figure 1(a), a silicon nitride film 102 is formed over a first metal wiring 101 formed on a semiconductor substrate 100. The silicon nitride film 102 is formed to be 50 nm thick, for example, and to protect the first metal wiring 101 during a subsequent etching process step. Thereafter, a first organic film 103 whose principal constituent is an organic constituent and that has a film thickness of 1  $\mu\text{m}$ , for example, is deposited on said silicon



nitride film 102. Then, an organic constituent-incorporated silicon oxide film 104 with film thickness of 50 nm that contains organic constituents in silicon oxide is deposited on the first organic film 103. Then, a second organic film 105 with a film thickness of 400 nm whose principal constituent is organic constituent is deposited on said organic constituent-incorporated silicon oxide film 104. Subsequently, a titanium nitride film 106 having a film thickness of 50 nm, for example, is deposited on said second organic film 105.

**[0030]**

There is no specific limitation on the method of depositing the first and second organic films 103 and 105. For example, the plasma CVD method using reactive gas whose principal constituent is perfluorodecalin may be used. Furthermore, hydrocarbon films or hydrocarbon films containing fluorine formed by the plasma CVD method, the application method or by the thermal CVD method may be used as the first and second organic films 103 and 105.

**[0031]**

Moreover, the first organic film 103 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin and organic silanes such as hexamethyl disiloxane, arylalkoxy silane or alkylalkoxy silane. In such cases, an organic/inorganic hybrid film can be obtained.

**[0032]**

Similarly, there is no specific limitation on the method of deposition of the organic constituent-incorporated silicon oxide film 104. For instance, the film 104 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. In such a case, an organic constituent-incorporated silicon oxide film 104 with a structure in which a phenyl group bonded to a silicon atom is incorporated into silicon dioxide can be obtained.

**[0033]**

Next, as shown in Figure 1 (b), a first resist pattern 107 having openings for the formation of wiring grooves is formed by lithography on the titanium nitride film 106. Thereafter, the titanium nitride film 106 is dry-etched using the first resist pattern 107 as a mask, thereby forming a mask pattern 108 out of the titanium nitride film 106 as shown in Figure 1 (c).

**[0034]**

Subsequently, a second resist pattern 109 with openings for forming contact holes is formed by lithography on the second organic film 105 without removing the first resist pattern 107. Then, the second organic film 105 is dry-etched, thereby forming a patterned second organic film 105A having the openings for the formation of contact holes as shown in Figure 2 (a). In this case, since the second organic film 105 and the first and second resist patterns 107 and 109 are all mainly composed of organic constituents, the second organic film 105 is etched at substantially the same rate as that of the first and second resist patterns 107 and 109. Thus, when the second organic film 105 is dry-etched, the first and second resist patterns 107 and 109 are also removed simultaneously.

**[0035]**

It should be noted that the second resist pattern 109 may be left in the course of dry-etching the second organic film 105.

This is because the residual second resist pattern 109 would be removed during a subsequent step of forming wiring grooves 111 in the patterned second organic film 105A (consult Figure 2(c)).

**[0036]**

Then, the organic constituent-incorporated silicon oxide film 104 is dry-etched using the patterned second organic film 105A as a mask, thereby forming a patterned organic constituent-incorporated silicon oxide film 104A having the openings for the formation of contact holes as shown in Figure 2(b). In this dry etching step, etching of the patterned second organic film 105A can be prevented by selecting etching conditions such that the organic constituent-incorporated silicon oxide film 104 is etched at a rate higher than that of the patterned second organic film 105A.

**[0037]**

Next, the patterned second organic film 105A is dry-etched using the mask pattern 108 as a mask, thereby forming the wiring grooves 111 in the patterned second organic film 105A as shown in Figure 2(c). At the same time, the first organic film 103 is also dry-etched using the patterned organic constituent-incorporated silicon oxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact holes.

**[0038]**

Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic constituent-incorporated silicon oxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal wiring 101 in the contact holes 110 as shown in Figure 3(a).

**[0039]**

Then, as shown in Figure 3(b), an adhesion layer 112 made of titanium nitride is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film 113 is deposited over the entire surface of the substrate to completely fill in the contact holes 110 and the wiring grooves 111.

There is no specific limitation on the structure of the metal film 113. Permissible examples include copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof. Also, there is no specific limitation on the method of depositing the metal film 113. For instance, plating, CVD or sputtering may be employed.

**[0040]**

Finally, as shown in Figure 3(c), portions of the adhesion layer 112, the metal film 113 and the mask pattern 108, which are deposited on the patterned second organic film 105A, are removed by the CMP technique, for example. As a result, the second metal wiring 114 consisting of metal film 113 as well as the contact 115 consisting of metal film 113 that connects the first and second metal wirings 101 and 114 are formed.

**[0041]**

Multilevel wiring structure may be formed by carrying out the same procedures as those mentioned above on the second metal wiring 114.

**[0042]**

In the first embodiment, the organic constituent-incorporated silicon oxide film 104 is formed by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Accordingly, the film 104 has a structure in which a phenyl group (organic group) bonded to a silicon atom is introduced into silicon dioxide. Thus, the film 104 can be processed as well as a conventional CVD oxide film and the relative dielectric constant of the film 104 is as low as that of the conventional CVD oxide film. In addition, the film 104 can adhere strongly to organic film, oxide film and metal film.

**[0043]**

After the mask pattern 108 has been formed out of the titanium nitride film 106, the second resist pattern 109 is formed without removing the first resist pattern 107, and the first and second resist patterns 107 and 109 are removed by dry etching the second organic film 105. Thus, it is no longer necessary to ash and remove the first and second resist patterns 107 and 109 with oxygen plasma. That is to say, it is possible to prevent the second organic film 105 from being damaged during the step of ashing and removing a resist pattern. Accordingly, although the second organic film 105 with a low relative dielectric constant is used as an interlevel insulating film, an ordinary resist application process is applicable to this embodiment.

**[0044]**

Moreover, the wiring grooves 111 are formed by dry-etching the patterned second organic film 105A using the mask pattern 108 as a mask and using the patterned organic constituent-incorporated silicon oxide film 104A as an etching stopper. Accordingly, the depth of the wiring grooves 111 matches the thickness of the second organic film 105. That is to say, the depth of the wiring grooves 111 can be defined by self-alignment.

**[0045]**

Hereinafter, problems caused by the misalignment of the second resist pattern 109 with the first resist pattern 107 and the measured taken to solve the problems will be described.

**[0046]**

First, the problems that are caused if the second resist pattern 109 has misaligned are described with reference to Figures 4(a) through 4(c), Figures 5(a) through 5(c) and Figures 6(a) through 6(c).

**[0047]**

As in the first embodiment, a silicon nitride film 102 is first formed to be 50 nm thick, for example, over first metal wiring 101 formed on a semiconductor substrate 100 as shown in Figure 4(a). Thereafter, a first organic film 103, whose principal constituent is an organic constituent, is formed to be 1  $\mu$ m thick, for example, on the silicon nitride film 102.

**[0048]**

Next, an organic constituent-incorporated silicon oxide film 104 containing an organic constituent in silicon dioxide is formed to be 50 nm thick, for example, on the first organic film 103. Then, a second organic film 105 mainly composed of an organic constituent is formed to be 400 nm thick, for example, on the organic constituent-incorporated silicon oxide film 104. Subsequently, a titanium nitride film 106 is deposited to a thickness of 50 nm on the second organic film 105, for example.

**[0049]**

Next, as shown in Figure 4(b), a first resist pattern 107 having openings for the formation of wiring grooves is formed on the titanium nitride film 106. Thereafter, the titanium nitride film 106 is dry-etched using the first resist pattern 107 as a mask, thereby forming a mask pattern 108 out of the titanium nitride film 106 as shown in Figure 4(c).

**[0050]**

Subsequently, a second resist pattern 109 having openings for the formation of contact holes is formed on the second organic film 105 without removing the first resist pattern 107. As can be seen by comparing Figures 5(a) and 1(c), the second resist pattern 109 has misaligned with the first resist pattern 107.

**[0051]**

Then, the second organic film 105 is dry-etched to form a patterned second organic film 105A having the openings for the formation of contact holes as shown in Figure 5(b). As in the first embodiment, since the second organic film 105 and the first and second resist patterns 107 and 109 are all mainly composed of organic constituents, the first and second resist patterns 107 and 109 are removed simultaneously with the dry-etching of the second organic film 105. In this case, since the second resist pattern 109 has misaligned with the first resist pattern 107, the diameter of the openings for the formation of contact holes, which are provided in the second organic film 105A, is smaller than desired.

**[0052]**

Then, the organic constituent-incorporated silicon oxide film 104 is dry-etched using the patterned second organic film 105A as a mask, thereby forming a patterned organic constituent-incorporated silicon oxide film 104A having the openings for the formation of contact holes as shown in Figure 5(c).

**[0053]**

Next, the patterned second organic film 105A is dry-etched using the mask pattern 108 as a mask, thereby forming the wiring grooves 111 in the patterned second organic film 105A as shown in Figure 6(a). At the same time, the first organic film 103 is also dry-etched using the patterned organic constituent-incorporated silicon oxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact holes 110 as shown in Figure 6(a). Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic constituent-incorporated silicon oxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal wiring 101 within the contact holes 110 as shown in Figure 6(b).

**[0054]**

Then, an adhesion layer 112 made of titanium nitride is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer 112, the metal film and the mask pattern 108 that are deposited on the patterned second organic film 105A are removed by the CMP technique, for example. As a result, the second metal wiring 114 is formed, as shown in Figure 6(c), but since the diameter of the contact holes 110 is smaller than desired, the contact holes 110 cannot be completely filled in with the metal film, and the first and second metal wiring 101 and 112 cannot be connected to each other, resulting in a contact failure.

**[0055]**

Next, the measures that should be taken to solve the problems caused by the misalignment of the second resist pattern 109 will be described with reference to Figures 7(a) through 7(c) and Figures 8(a) through 8(c).

**[0056]**

First, a second resist pattern 109 having openings for the formation of contact holes is formed through the same process steps as those described with reference to Figures 4(a) through 4(c) and Figure 5(a). In this case as well, the second resist pattern 109 has also misaligned with the first resist pattern 107 (consult Figure 5(a)).

**[0057]**

Thus, as shown in Figure 7(a), the first resist pattern 107 and the mask pattern 108 are dry-etched using the second resist pattern 109 as a mask. In this manner, portions of the first resist pattern 107 not overlapping with the second resist pattern 109 are removed and the openings of the mask pattern 108 are expanded to the size that includes the openings for the formation of wiring grooves or the openings for the formation of contact holes. By so doing, the openings in the second resist pattern 109 for the formation of contact holes can be transferred to the first resist pattern 107 and to the mask pattern 108.

**[0058]**

Then, the second organic film 105 is dry-etched, thereby forming a patterned second organic film 105A having the openings for the formation of contact holes as shown in Figure 7(b). In this case as well, since the principal constituent of the second organic film 105 and the first and second resist patterns 107 and 109 is primarily organic constituents, the first and second resist patterns 107 and 109 are removed simultaneously with the dry-etching of the second organic film 105.

**[0059]**

Then, the organic constituent-incorporated silicon dioxide film 104 is dry-etched using the patterned second organic film 105A as a mask, thereby forming a patterned organic constituent-incorporated silicon dioxide film 104A having the openings for the formation of contact holes as shown in Figure 7(c).

**[0060]**

As described above, the second resist pattern 109 has misaligned with the first resist pattern 107. However, in this case, the pattern for the openings of the second resist pattern for the formation of contact holes 109 has been successfully transferred to the first resist pattern 107 and the mask pattern 108. Thus, the diameter of the openings for the formation of contact holes, which have been formed in the patterned second organic film 105A and the patterned organic

constituent-incorporated silicon dioxide film 104A, is a predetermined size.

**[0061]**

Next, the patterned second organic film 105A is dry-etched using the mask pattern 108 as a mask, thereby forming the wiring grooves 111 in the patterned second organic film 105A as shown in Figure 8(a). At the same time, the first organic film 103 is also dry-etched using the patterned organic constituent-incorporated silicon dioxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact holes 110 as shown in Figure 8(a). Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic constituent-incorporated silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal wiring 101 within the contact holes 110 as shown in Figure 8(b).

**[0062]**

Then, an adhesion layer 112 made of titanium nitride is deposited to a thickness of 50 nm, for example, on the wall faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer 112, the metal film and the mask pattern 108 that are deposited on the patterned second organic film 105A are removed by the CMP technique, for example. As a result, second metal wiring 114 and contacts 115 are formed out of the titanium nitride film 112 and the metal film as shown in Figure 8(c).

**[0063]**

(Second Embodiment)

The method of forming a wiring structure pursuant to the second embodiment of the present invention is explained below with reference to Figures 9(a) through 9(c), Figures 10(a) through 10(c) and Figures 11(a) through 11(c).

**[0064]**

First, as shown in Figure 9(a), a silicon nitride film 202 is formed to be 50 nm thick, for example, over first metal wiring 201 formed on a semiconductor substrate 200. Thereafter, a first organic film 203 mainly composed of an organic constituent, is formed to be 1  $\mu\text{m}$  thick, for example, on the silicon nitride film 202. Next, an organic constituent-incorporated silicon dioxide film 204 containing an organic constituent in silicon dioxide is formed to be 50 nm thick, for example, on the first organic film 203. Then, a second organic film 205 mainly composed of an organic constituent is formed to be 400 nm thick, for example, on the organic constituent-incorporated silicon dioxide film 204. Finally, a titanium nitride film 206 is deposited to a thickness of 50 nm, for example, on the second organic film.

**[0065]**

There is no specific limitation on method of depositing the first and second organic films 203 and 205. For example, these films 203 and 205 may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. In addition, hydrocarbon films or fluorine-containing hydrocarbon films formed by plasma CVD, coating or thermal CVD may be used as the first and second organic films 203 and 205.

**[0066]**

Similarly, there is no specific limitation on the method of depositing the organic constituent-incorporated silicon dioxide film 204. For instance, the film 204 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

**[0067]**

Next, as shown in Figure 9(b), a first resist pattern 207 having openings for the formation of wiring grooves is formed by lithography on the titanium nitride film 206. Thereafter, the titanium nitride film 206 is dry-etched using the first resist pattern 207 as a mask, thereby forming a mask pattern 208 out of the titanium nitride film 206 as shown in Figure 9(c).

**[0068]**

Subsequently, a second resist pattern 209, having openings for the formation of contact holes is formed by lithography on the second organic film 205 without removing the first resist pattern 207. Then, the second organic film 205 is dry-etched, thereby forming a patterned second organic film 205A having the openings for the formation of contact holes as shown in Figure 10(a). In this case, since the main constituents of the second organic film 205 and the first and second resist patterns 207 and 209 are organic, the second organic film 205 is etched at a rate substantially equal to that of the first and second resist patterns 207 and 209. Consequently, the first and second resist patterns 207 and 209 are removed by dry etching the second organic film 205.

**[0069]**

If there is a concern that the second resist pattern 209 has been misaligned with the first resist pattern 207, then the first resist pattern 207 and the mask pattern 208 would be dry-etched using the second resist pattern 209 as a mask. In this manner, parts of the first resist pattern 207 not overlapping the second resist pattern 209 are removed and the openings of the mask pattern 208 are expanded to the size that includes the openings for the formation of wiring grooves or the openings for the formation of contact holes, as described in the first embodiment.

**[0070]**

Then, the organic constituent-incorporated silicon dioxide film 204 is dry-etched using the patterned second organic film 205A as a mask, thereby forming a patterned organic constituent-incorporated silicon dioxide film 204A having the openings for the formation of contact holes as shown in Figure 10(b). Next, the patterned second organic film 205A is dry-etched using the mask pattern 208 as a mask, thereby forming the wiring grooves 211 in the patterned second organic film 205A as shown in Figure 10(c). At the same time, the first organic film 203 is also dry-etched using the patterned organic constituent-incorporated silicon dioxide film 204A as a mask, thereby forming a patterned first organic film 203A having the contact holes 210 as also shown in Figure 10(c).

**[0071]**

Subsequently, the silicon nitride film 202 is dry-etched using the patterned organic constituent-incorporated silicon dioxide film 203A [sic] as a mask, thereby forming a patterned silicon nitride film 202A and exposing the first metal wiring 201 within the contact holes 210 as shown in Figure 11(a).

**[0072]**

Then, the patterned first and second organic films 203A and 205A are subjected to plasma processing using ammonium gas. As a result, as shown in Figure 11(b), adhesion layers 212, including amino and amide groups, are deposited on the wall faces of the patterned first organic film 203A exposed inside the contact holes 210 and on the wall faces of the patterned second organic film 205A exposed inside the wiring grooves 211. Thereafter, a metal film 213 is deposited over the entire surface of the substrate to completely fill in the contact holes 210 and the wiring grooves 211. There is no specific limitation on the composition of the metal film 213 in this embodiment, in which copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, there is no specific limitation on the method of depositing the metal film 213. For instance, plating, CVD or sputtering may be employed.

**[0073]**

Finally, as shown in Figure 11(c), portions of the metal film 213 and the mask pattern 208 that are deposited on the patterned second organic film 205A are removed by the CMP technique, for example. As a result, second metal wiring 214 and contacts 215 are formed out of the metal film 213.

**[0074]**

A multilevel wiring structure may be formed on the second metal wiring 214 through the same process steps as those described above.

**[0075]**

(Third Embodiment)

The method of forming a wiring structure pursuant to the third embodiment of the present invention is explained below with reference to Figures 12(a) through 12(c), Figures 13(a) through 13(c) and Figures 14(a) through 14(c).

**[0076]**

First, as shown in Figure 12(a), a silicon nitride film 302 is formed over first metal wiring 301 formed on a semiconductor substrate 300. The silicon nitride film 302 is formed to be 50 nm thick, for example, and to protect the first metal wiring 301 during a subsequent etching process step. Thereafter, a first organic constituent-incorporated silicon dioxide film 303 containing an organic constituent in silicon dioxide is formed to be 1  $\mu\text{m}$  thick, for example, on the silicon nitride film 302. Next, a low-dielectric-constant SOG film 304 having a siloxane framework is deposited to be 400 nm thick, for example, on the first organic constituent-incorporated silicon dioxide film 303. Then, a second organic constituent-incorporated silicon dioxide film 305 containing an organic constituent in silicon dioxide is deposited to a thickness of 50 nm, for example, on the low-dielectric-constant SOG film 304. Finally, a titanium nitride film 306 is formed to a thickness of 50 nm, for example, on the second organic constituent-incorporated silicon dioxide film 305.

**[0077]**

There is no specific limitation on the methods of depositing the first and second organic constituent-incorporated silicon dioxide films 303 and 305. For example, these films 303 and 305 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. In addition, an HSQ film may be used as the low-dielectric-constant SOG film 304 with a siloxane framework.

**[0078]**

Next, as shown in Figure 12(b), a first resist pattern 307 having openings for the formation of wiring grooves is formed by lithography on the titanium nitride film 306. Thereafter, the titanium nitride film 306 is dry-etched using the first resist pattern 307 as a mask, thereby forming a mask pattern 308 out of the titanium nitride film 306 as shown in Figure 12(c).

**[0079]**

Subsequently, as shown in Figure 13(a), the first resist pattern 307 is removed and then a second resist pattern 309

having openings for the formation of contact holes is formed on the second organic constituent-incorporated silicon dioxide film 305. Then, the second organic constituent-incorporated silicon dioxide film 305, the low-dielectric-constant SOG film 304 and the first organic constituent-incorporated silicon dioxide film 303 are sequentially dry-etched using the second resist pattern 309 as a mask. As a result, a patterned second organic constituent-incorporated silicon dioxide film 305A, a patterned low-dielectric-constant SOG film 304A and a patterned first organic constituent-incorporated silicon dioxide film 303A having contact holes 310 are formed as shown in Figure 13(b).

**[0080]**

Next, as shown in Figure 13(c), the second resist pattern 309 is removed and the patterned second organic constituent-incorporated silicon dioxide film 305A is dry-etched using the mask pattern 308 as a mask, thereby forming openings for the formation of wiring grooves in the patterned second organic constituent-incorporated silicon dioxide film 305A. Thereafter, the patterned low-dielectric-constant SOG film 304A is dry-etched using the mask pattern 308 and the patterned second organic constituent-incorporated silicon dioxide film 305A having the openings for wiring grooves as a mask, thereby forming the wiring grooves 311. In forming the wiring grooves 311, by selecting the etching conditions such that the first organic constituent-incorporated silicon dioxide film 303A is etched at a rate sufficiently lower than that of the low-dielectric-constant SOG film 304A, sufficient selectivity can be secured for the patterned first organic constituent-incorporated silicon dioxide film 303A. Accordingly, the depth of the wiring grooves 311 can be unequivocally determined by the sum of the thicknesses of the second organic constituent-incorporated silicon dioxide film 305 and the low-dielectric-constant SOG film 304.

**[0081]**

If there is a concern that the second resist pattern 309 has been misaligned with the first resist pattern 307, then the mask pattern 308 should be dry-etched using the second resist pattern 309 as a mask before the second organic constituent-incorporated silicon dioxide film 305 is dry-etched using the second resist pattern 309 as a mask. That is to say, if the mask pattern 308 is exposed to the openings of the second resist pattern 309 for the formation of contact holes because of the misalignment of the second resist pattern 309 with the first resist pattern 307, then the mask pattern 308 is dry-etched using the second resist pattern 309 as a mask. In this manner, the openings of the mask pattern 308 are expanded to include the openings for the formation of wiring grooves and contact holes.

**[0082]**

Subsequently, the silicon nitride film 302 is dry-etched using the patterned first organic constituent-incorporated silicon dioxide film 303A as a mask, thereby forming a patterned silicon nitride film 302A and exposing the first metal wiring 301 within the contact holes 310 as shown in Figure 14(a).

**[0083]**

Then, as shown in Figure 14(b), an adhesion layer 312 made of titanium nitride is deposited to a thickness of 50 nm, for example, on the wall faces of the contact holes 310 and the wiring grooves 311. Thereafter, a metal film 313 is deposited over the entire surface of the substrate to completely fill in the contact holes 310 and the wiring grooves 311. There is no specific limitation on the composition of the metal film 313 in this embodiment, in which copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, there is no specific limitation on the method of depositing the metal film 313. For instance, plating, CVD or sputtering may be employed.

**[0084]**

Finally, as shown in Figure 14(c), portions of the adhesion layer 312, the metal film 313 and the mask pattern 308 that are deposited on the patterned second organic constituent-incorporated silicon dioxide film 305A are removed by the CMP technique, for example. As a result, second metal wiring 314 and contacts 315 connecting the first and second metal wiring 301 and 314 are formed out of the metal film 313.

**[0085]**

A multilevel wiring structure may be formed on the second metal wiring 314 through the same process steps as those described above.

**[0086]**

In the third embodiment, when the first resist pattern 307 is ashed and removed with oxygen plasma, the low-dielectric-constant SOG film 304 is not exposed to the oxygen plasma because the second organic constituent-incorporated silicon dioxide film 305 exists on the low-dielectric-constant SOG film 304.

**[0087]**

Also, in this embodiment, after the second organic constituent-incorporated silicon dioxide film 305, the low-dielectric-constant SOG film 304 and the first organic constituent-incorporated silicon dioxide film 303 have been sequentially dry-etched using the second resist pattern 309 as a mask, the second resist pattern 309 is ashed and removed with oxygen plasma. Accordingly, the regions of the patterned low-dielectric-constant SOG film 304A that are exposed in the openings for the formation of contact holes are exposed to oxygen plasma and damaged. However, the damaged

layer formed in the patterned low-dielectric-constant SOG film 304A is removed when the wiring grooves 311 are formed in the patterned low-dielectric-constant SOG film 304A and thus has no harmful effects on subsequent process steps.

**[0088]**

Accordingly, the low-dielectric-constant SOG film 304 may be made of a material degradable with oxygen plasma. For example, if an HSQ film is exposed to oxygen plasma, the SiCH bonds thereof are oxidized and the content of water as well as the relative dielectric constant thereof both increase to impair the reliability and performance of the device. However, in the third embodiment, the patterned low-dielectric-constant SOG film 304A in which the wiring grooves 311 have already been formed is not affected by oxygen plasma. Thus, even if an HSQ film is used as an interlevel insulating film, deterioration in reliability and performance of the device can be avoided.

**[0089]**

(Variant of Third Embodiment)

Next, a method for the formation of a wiring structure based on a modified example of the third embodiment of the present invention is described with reference to Figures 15(a) through 15(c), Figures 16(a) through 16(c) and Figures 17(a) through 17(c).

**[0090]**

First, as shown in Figure 15(a), a silicon nitride film 352 is formed over first metal wiring 351 formed on a semiconductor substrate 350. The silicon nitride film 352 is formed to be 50 nm thick, for example, and to protect the first metal wiring 351 during a subsequent etching process step. Thereafter, a first silicon dioxide film 353 is formed to be 1  $\mu\text{m}$  thick, for example, on the silicon nitride film 352. Next, an organic film 354 is deposited to be 400 nm thick, for example, on the first silicon dioxide film 353. Then, a second silicon dioxide film 355 is formed to be 50 nm thick, for example, on the organic film 354. And a titanium nitride film 356 is formed to be 50 nm thick, for example, on the second silicon dioxide film 355.

**[0091]**

There is no specific limitation on the methods of depositing the first and second silicon dioxide films 353 and 355. For example, these films may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

**[0092]**

Next, as shown in Figure 15(b), a first resist pattern 357 having openings for the formation of wiring grooves is formed by lithography on the titanium nitride film 356. Thereafter, the titanium nitride film 356 is dry-etched using the first resist pattern 357 as a mask, thereby forming a mask pattern 358 out of the titanium nitride film 356 as shown in Figure 15(c).

**[0093]**

Subsequently, as shown in Figure 16(a), the first resist pattern 357 is removed and then a second resist pattern 359 having openings for the formation of contact holes is formed on the second silicon dioxide film 355. Then, the second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask, thereby forming a patterned second silicon dioxide film 355A and a patterned organic film 354A having openings 360 for the formation of contact holes as shown in Figure 16(b). In this case, the second resist pattern 359 is removed during the step of etching the organic film 354.

**[0094]**

Next, as shown in Figure 16(c), the first silicon dioxide film 353 is dry-etched using the patterned second silicon dioxide film 355A and the patterned organic film 354A as masks, thereby forming a patterned first silicon dioxide film 353A having contact holes 361. In this etching process step, the mask pattern 358 is transferred to the patterned second silicon dioxide film 355A. Accordingly, openings for the formation of wiring grooves are formed in the patterned second silicon dioxide film 355A.

**[0095]**

Thereafter, as shown in Figure 16(d), the patterned organic film 354A is dry-etched using the mask pattern 358 and the patterned second silicon dioxide film 355A having the openings for the formation of wiring grooves as masks, thereby forming the wiring grooves 362. In forming the wiring grooves 362, by selecting etching conditions such that the first silicon dioxide film 353A is etched at a rate sufficiently lower than that of the organic film 354A, sufficient selectivity can be secured for the patterned first silicon dioxide film 353A. Accordingly, the depth of the wiring grooves 362 can be unequivocally determined by the sum of the thicknesses of the second silicon dioxide film 355 and the organic film 354.

**[0096]**

If there is a concern that the second resist pattern 359 has been misaligned with the first resist pattern 357, then the mask

pattern 358 should be dry-etched using the second resist pattern 359 as a mask before the second silicon dioxide film 355 is dry-etched using the second resist pattern 359 as a mask. That is to say, if the mask pattern 358 is exposed to the openings of the second resist pattern 359 for the formation of contact holes because of the misalignment of the second resist pattern 359 with the first resist pattern 357, then the mask pattern 358 is dry-etched using the second resist pattern 359 as a mask. In this manner, the openings of the mask pattern 358 are expanded to include the openings for the formation of wiring grooves and contact holes.

**[0097]**

Subsequently, the silicon nitride film 352 is dry-etched using the patterned first silicon dioxide film 353A as a mask, thereby forming a patterned silicon nitride film 352A and exposing the first metal wiring 351 within the contact holes 361 as shown in Figure 17(a).

**[0098]**

Then, as shown in Figure 17(b), an adhesion layer 363 made of titanium nitride is deposited to a thickness of 50 nm, for example, on the wall faces of the contact holes 361 and the wiring grooves 362. Thereafter, a metal film 364 is deposited over the entire surface of the substrate to completely fill in the contact holes 361 and the wiring grooves 362. There is no specific limitation on the composition of the metal film 364 in this embodiment, in which copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 364 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

**[0099]**

Finally, as shown in Figure 17(c), portions of the adhesion layer 363, the metal film 364 and the mask pattern 358 that are deposited on the patterned second silicon dioxide film 355A are removed by the CMP technique, for example. As a result, second metal wiring 365 and contacts 366, connecting the first and second metal wiring 351 and 365, are formed out of the metal film 364.

**[0100]**

A multilevel wiring structure may be formed on the second metal wiring 365 through the same process steps as those described above.

**[0101]**

In this variant of the third embodiment, the organic film 354 is not exposed to the oxygen plasma when the first resist pattern 357 is ashed and removed by oxygen plasma because the second silicon dioxide film 355 exists on the organic film 354.

**[0102]**

Also, the second resist pattern 359 is removed when the second silicon dioxide film 355 and the organic film 354 are dry-etched using the second resist pattern 359 as a mask. Accordingly, the organic film 354 is not exposed to oxygen plasma since there is no need to ash and remove the second resist pattern 359 with oxygen plasma.

**[0103]**

(Fourth Embodiment)

The method of forming a wiring structure pursuant to the fourth embodiment of the present invention is explained below with reference to Figures 18(a) through 18(c), Figures 19(a) through 19(c) and Figures 20(a) through 20(c).

**[0104]**

First, as shown in Figure 18(a), a silicon nitride film 402 is formed over first metal wiring 401 formed on a semiconductor substrate 400. The silicon nitride film 402 is formed to be 50 nm thick, for example, and to protect the first metal wiring 401 during a subsequent etching process step. Thereafter, a first low-dielectric-constant SOG film 403 having a siloxane framework is formed to be 1  $\mu\text{m}$  thick, for example, on the silicon nitride film 402. Next, an organic constituent-incorporated silicon dioxide film 404 containing an organic constituent in silicon dioxide is deposited to be 50 nm thick, for example, on the first low-dielectric-constant SOG film 403. Then, a second low-dielectric-constant SOG film 405 having a siloxane framework is formed to be 400 nm thick, for example, on the organic constituent-incorporated silicon dioxide film 404. Then, a titanium nitride film 406 is formed to be 50 nm thick, for example, on the second low-dielectric-constant SOG film 405.

**[0105]**

The first and second low-dielectric-constant SOG films 403 and 405 may be HSQ films, for example. There is no specific limitation on the methods of depositing the organic constituent-incorporated silicon dioxide film 404. For example, these films 303 and 305 may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. By so doing, an organic constituent-incorporated silicon dioxide film 404 having a structure in which a phenyl group bonded to a silicon atom is introduced into silicon dioxide can be obtained.

**[0106]**

Next, as shown in Figure 18(b), a first resist pattern 407 having openings for the formation of wiring grooves is formed



by lithography on the titanium nitride film 406. Thereafter, the titanium nitride film 406 is dry-etched using the first resist pattern 407 as a mask, thereby forming a mask pattern 408 out of the titanium nitride film 406 as shown in Figure 18(c).

**[0107]**

Subsequently, a second resist pattern 409 having openings for the formation of contact holes is formed by lithography on the second low-dielectric-constant SOG film 405 without removing the first resist pattern 407. Then, the second low-dielectric-constant SOG film 405 and the organic constituent-incorporated silicon dioxide film 404 are sequentially dry-etched using the second resist pattern 409 as a mask, thereby forming a patterned second low-dielectric-constant SOG film 405A and a patterned organic constituent-incorporated silicon dioxide film 404A as shown in Figure 19(a).

**[0108]**

Next, the first and second resist patterns 407 and 409 are ashed and removed with oxygen plasma. As a result, a damaged layer 410 is formed in portions of the patterned second low-dielectric-constant SOG film 405A and the first low-dielectric-constant SOG film 403 that are exposed to the openings for the formation of contact holes, as shown in Figure 19(b).

**[0109]**

Then, the patterned second low-dielectric-constant SOG film 405A is dry-etched using the mask pattern 408 as a mask, thereby forming wiring grooves 412 in the patterned second low-dielectric-constant SOG film 405A. At the same time, the first low-dielectric-constant SOG film 403 is dry-etched using the patterned organic constituent-incorporated silicon dioxide film 404A as a mask, thereby forming a patterned first low-dielectric-constant SOG film 403A having contact holes 411, as shown in Figure 19(c). By performing this dry-etching process step, the damaged layer 410 can be removed from the patterned second low-dielectric-constant SOG films 405A and the first low-dielectric-constant SOG film 403.

**[0110]**

Subsequently, the silicon nitride film 402 is dry-etched using the patterned organic constituent-incorporated silicon dioxide film 404A as a mask, thereby forming a patterned silicon nitride film 402A and exposing the first metal wiring 401 within the contact holes 411 as shown in Figure 20(a).

**[0111]**

Then, as shown in Figure 20(b), an adhesion layer 413 made of titanium nitride is deposited to a thickness of 50 nm, for example, on the wall faces of the contact holes 411 and the wiring grooves 412. Thereafter, a metal film 414 is deposited over the entire surface of the substrate to completely fill in the contact holes 411 and the wiring grooves 412. There is no specific limitation on the composition of the metal film 414 in this embodiment, in which copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, there is no specific limitation on the method of depositing the metal film 414. For instance, plating, CVD or sputtering may be employed.

**[0112]**

Finally, as shown in Figure 20(c), portions of the adhesion layer 413, the metal film 414 and the mask pattern 408 that are deposited on the patterned second low-dielectric-constant SOG film 405A are removed by the CMP technique, for example. As a result, second metal wiring 415 and contacts 416 connecting the first and second metal wiring 401 and 415 are formed out of the metal film 414.

**[0113]**

A multilevel wiring structure may be formed on the second metal wiring 114 [sic, should be 415?] through the same process steps as those described above.

**[0114]**

In the fourth embodiment, when the first and second resist patterns 407 and 409 are ashed and removed with oxygen plasma, a damaged layer 410 is formed in the first low-dielectric-constant SOG film 403 and the patterned second low-dielectric-constant SOG film 405A. However, the damaged layer 410 can be removed when the contact holes 411 and the wiring grooves 412 are formed.

**[0115]**

Accordingly, the first and second low-dielectric-constant SOG films 403 and 405 may be made of a material degradable with oxygen plasma. For example, if an HSQ film is exposed to oxygen plasma, SiCH bonds thereof are oxidized and the content of water and the relative dielectric constant thereof both increase to impair the reliability and performance of the device. However, according to the fourth embodiment, the patterned first low-dielectric-constant SOG film 403A in which the contact holes 411 have already been formed and the patterned second low-dielectric-constant SOG film 405A in which the wiring grooves 412 have already been formed are not affected by oxygen plasma. Thus, even if an HSQ film is used as an interlevel insulating film, the deterioration in reliability and performance of the device can be avoided.

**[0116]**

**[Effects of Invention]**

The step of removing a first resist pattern and a second resist pattern by ashing using an oxygen plasma is rendered unnecessary in the first method of forming a wiring structure, which enables the third insulating film to avoid being damaged when removing the resist patterns through ashing. Consequently, an insulating film having a low relative dielectric constant, which would sustain damage due to oxygen plasma, can be used as a third insulating film, as a result of which an interlevel insulating film having a low relative dielectric constant could be formed while using a conventional resist process.

**[0117]**

Moreover, the depth of the wiring grooves can be defined by self-alignment since the depth of the wiring grooves can be matched to the film thickness of the third insulating film since the second insulating film can be used as an etching stopper when forming wiring grooves by dry etching the third insulating film in the tenth step using the mask pattern as the mask.

**[0118]**

The provision of a step of forming an adhesion layer comprising metal film in the section of exposure to wiring grooves in the third insulating film and in the section exposed to contact holes in the first insulating film between the tenth step and the eleventh step in the first method of forming a wiring structure ensures adhesion between the upper-level metal wiring and the third insulating film as well as adhesion between contacts and the first insulating film.

**[0119]**

The etching conditions such that the pattern with the higher etching rate is used in etching of the third insulating film using the first resist pattern or the second resist pattern while the pattern with the lower etching rate is used in etching of the second insulating film in the eighth step can be reliably realized by setting the principal constituent of the third insulating film to be organic constituents in the first method of forming a wiring structure.

**[0120]**

A third insulating film in which the principal constituents are organic constituents and that has a low relative dielectric constant can be reliably realized by including the step of forming the third insulating film by the CVD method using reactive gas that contains perfluorodecalin.

**[0121]**

Etching conditions such that the etching rate of the second insulating film is higher while the etching rate of the first insulating film and the third insulating film is lower in the ninth step and etching conditions such that the etching rate of the first insulating film and the third insulating film is higher while the etching rate of the mask pattern and of the second insulating film is lower in the tenth step can be reliably realized by setting the principal constituent of the first insulating film to be organic constituents in this case,

**[0122]**

Adhesion between upper-level metal wiring and contacts as well as between first and third insulating films in which the principal constituents are organic constituents can be reliably realized by providing a step of forming an adhesion layer by plasma treatment of the section exposed to wiring grooves in the third insulating film and plasma treatment of the section exposed to contact holes in the first insulating film using reactive gas containing nitrogen, said additional step being added between the tenth step and the eleventh step, when the principal constituents of the first insulating film and of the second insulating film are organic constituents.

**[0123]**

A first insulating film in which the principal constituents are organic constituents that has a low relative dielectric constant can be reliably realized by including a first step in which a first insulating film is formed by the CVD method using reactive gas containing perfluorodecalin when the principal constituents of the first insulating film are organic constituents.

**[0124]**

Even if a damaged layer is formed in the section exposed in an opening for the formation of contact holes in the second insulating film of the first insulating film and the third insulating film in the tenth step of removing the first resist pattern and the second resist pattern in the second method of forming a wiring structure, since said damaged layer can be reliably removed in the eleventh step, insulating films having a low relative dielectric constant can be used as the first and third insulating films even though they would be damaged by oxygen plasma, as a result of which an interlevel insulating film having a low relative dielectric constant can be formed while using a conventional resist process.

**[0125]**

An interlevel insulating film having a low relative dielectric constant can be formed while using a conventional resist process when the third insulating film in the second method of forming a wiring structure is a low-dielectric-constant SOG film with a siloxane framework.

### **[Brief Description of Drawings]**

[Figure 1]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the first embodiment of the present invention.

[Figure 2]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the first embodiment of the present invention.

[Figure 3]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the first embodiment of the present invention.

[Figure 4]

(a) to (c) are cross-sectional views explaining the problems when the second resist pattern has misaligned in the method of forming a wiring structure pursuant to the first embodiment of the present invention.

[Figure 5]

(a) to (c) are cross-sectional views explaining the problems when the second resist pattern has misaligned in the method of forming a wiring structure pursuant to the first embodiment of the present invention.

[Figure 6]

(a) to (c) are cross-sectional views explaining the problems when the second resist pattern has misaligned in the method of forming a wiring structure pursuant to the first embodiment of the present invention.

[Figure 7]

(a) to (c) are cross-sectional views explaining resolutions when the second resist pattern has misaligned in the method of forming a wiring structure pursuant to the first embodiment of the present invention.

[Figure 8]

(a) to (c) are cross-sectional views explaining resolutions when the second resist pattern has misaligned in the method of forming a wiring structure pursuant to the first embodiment of the present invention.

[Figure 9]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the second embodiment of the present invention.

[Figure 10]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the second embodiment of the present invention.

[Figure 11]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the second embodiment of the present invention.

[Figure 12]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the third embodiment of the present invention.

[Figure 13]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the third embodiment of the present invention.

[Figure 14]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the third embodiment of the present invention.

[Figure 15]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to a variant of the third embodiment of the present invention.

[Figure 16]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to a variant of the third embodiment of the present invention.

[Figure 17]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to a variant of the third embodiment of the present invention.

[Figure 18]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the fourth embodiment of the present invention.

[Figure 19]

(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the fourth embodiment of the present invention.

[Figure 20]

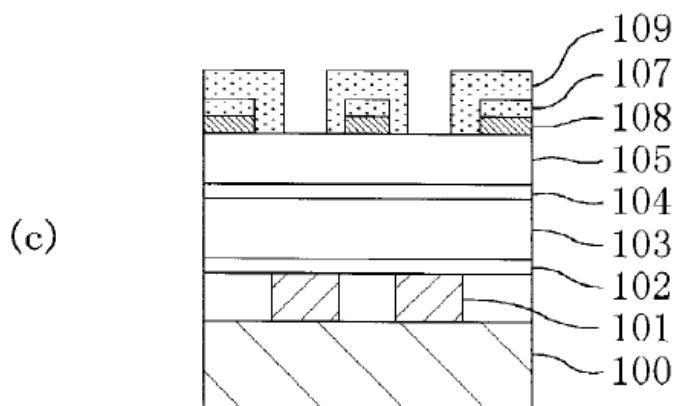
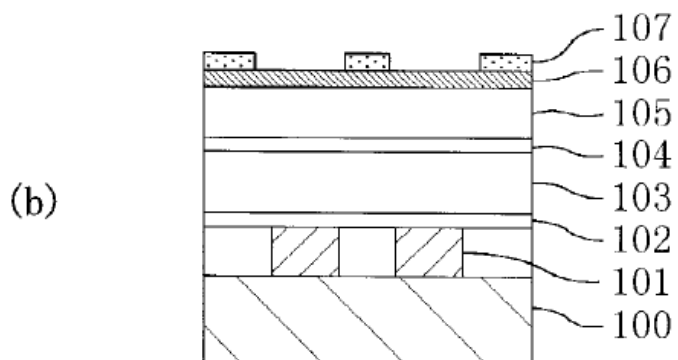
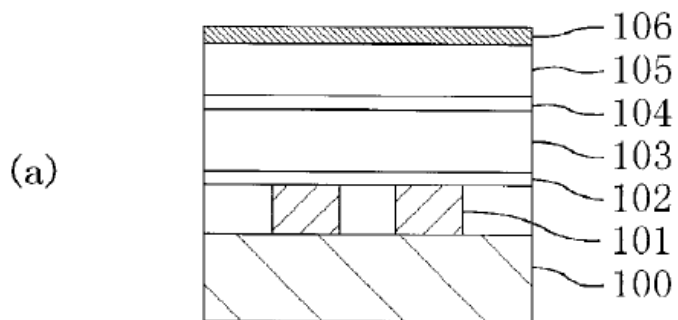
(a) to (c) are cross-sectional views illustrating the method of forming a wiring structure pursuant to the fourth embodiment of the present invention.

**[Explanation of Notations]**

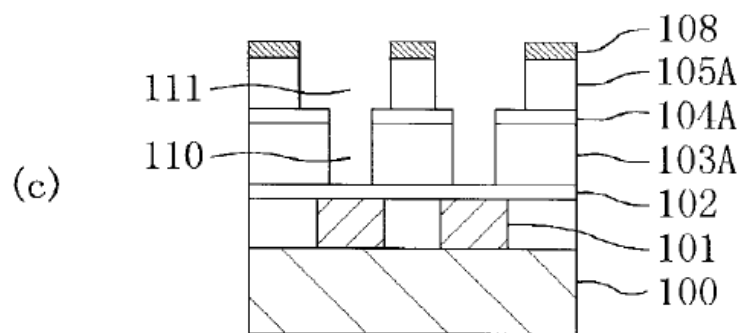
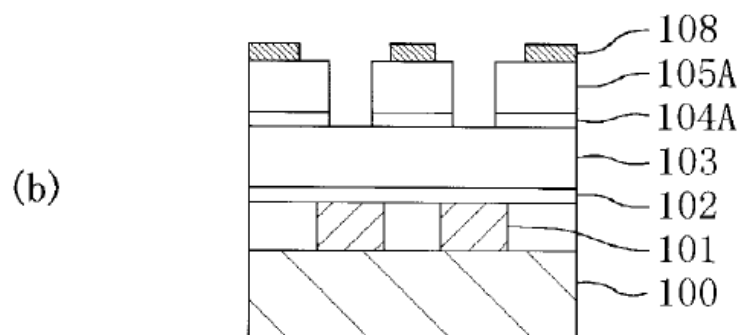
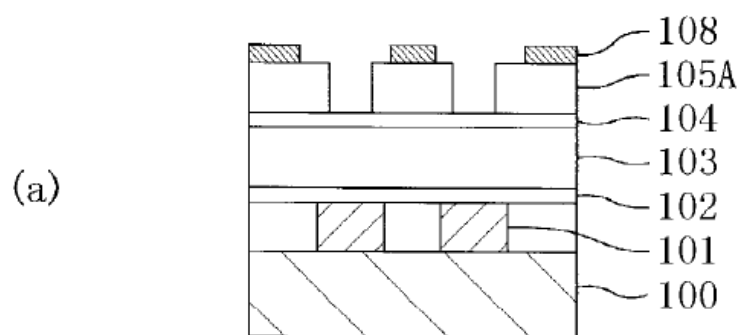
100 semiconductor substrate  
101 first metal wiring  
102 silicon nitride film  
102A patterned silicon nitride film  
103 first organic film  
103A patterned first organic film  
104 organic constituent-incorporated silicon oxide film  
104A patterned organic constituent-incorporated silicon oxide film  
105 second organic film  
105A patterned second organic film  
106 titanium nitride film  
107 first resist pattern  
108 mask pattern  
109 second resist pattern  
110 contact holes  
112 adhesion layer  
113 metal film  
114 second metal wiring  
115 contacts  
200 semiconductor substrate  
201 first metal wiring  
202 silicon nitride film  
202A patterned silicon nitride film  
203 first organic film  
203A patterned first organic film  
204 organic constituent-incorporated silicon dioxide film  
204A patterned organic constituent-incorporated silicon dioxide film  
205 second organic film  
205A patterned second organic film  
206 titanium nitride film  
207 first resist pattern  
208 mask pattern  
209 second resist pattern  
210 contact holes  
211 wiring grooves  
212 adhesion layers  
213 metal film  
214 second metal wiring  
215 contacts  
300 semiconductor substrate  
301 first metal wiring  
302 silicon nitride film  
302A patterned silicon nitride film  
303 first organic constituent-incorporated silicon dioxide film  
303A patterned first organic constituent-incorporated silicon dioxide film  
304 low-dielectric-constant SOG film  
305 second organic constituent-incorporated silicon dioxide film  
305A patterned second organic constituent-incorporated silicon dioxide film

306 titanium nitride film  
307 first resist pattern  
308 mask pattern  
309 second resist pattern  
310 contact holes  
312 adhesion layer  
313 metal film  
314 second metal wiring  
315 contacts  
350 semiconductor substrate  
351 first metal wiring  
352 silicon nitride film  
352A patterned silicon nitride film  
353 first silicon dioxide film  
353A patterned first silicon dioxide film  
354 organic film  
355 second silicon dioxide film  
355A patterned second silicon dioxide film  
356 titanium nitride film  
357 first resist pattern  
358 mask pattern  
359 second resist pattern  
360 openings  
361 contact holes  
362 wiring grooves  
363 adhesion layer  
364 metal film  
365 second metal wiring  
366 contacts  
400 semiconductor substrate  
401 first metal wiring  
402 silicon nitride film  
402A patterned silicon nitride film  
403 first low-dielectric-constant SOG film  
403A patterned first low-dielectric-constant SOG film  
404 organic constituent-incorporated silicon dioxide film  
404A patterned organic constituent-incorporated silicon dioxide film  
405 second low-dielectric-constant SOG film  
405A patterned second low-dielectric-constant SOG film  
406 titanium nitride film  
407 first resist pattern  
408 mask pattern  
409 second resist pattern  
410 damaged layer  
411 contact holes  
412 wiring grooves  
413 adhesion layer  
414 metal film  
415 second metal wiring  
416 contacts

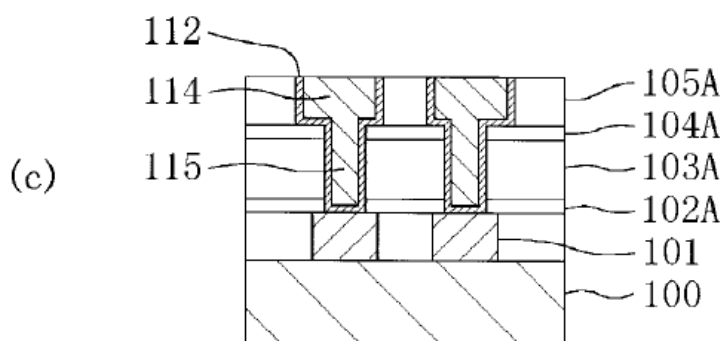
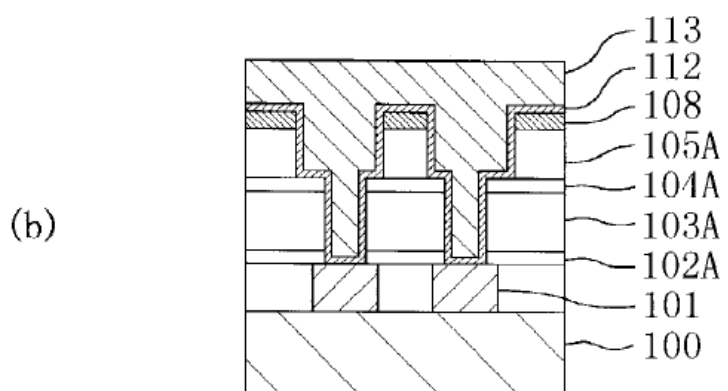
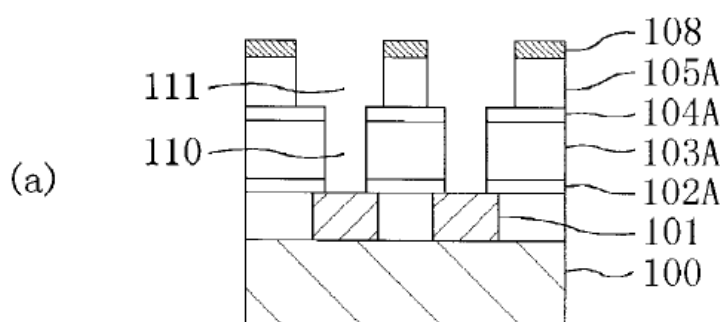
[Name of Document] Diagrams  
[Figure 1]



[Figure 2]

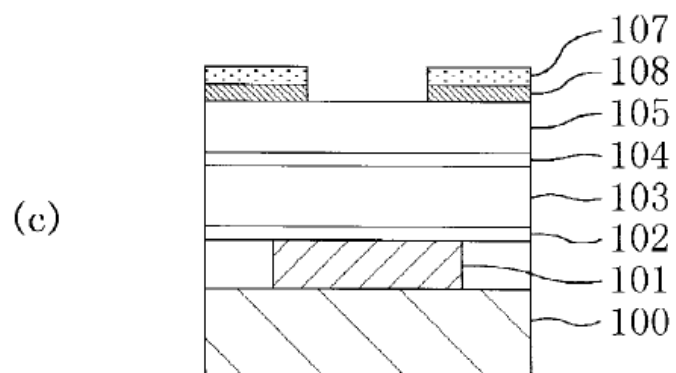
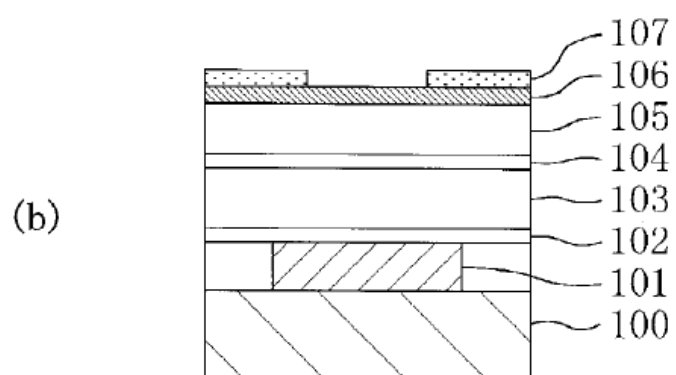
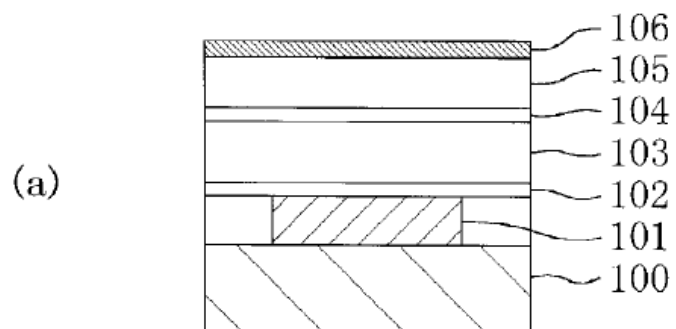


[Figure 3]

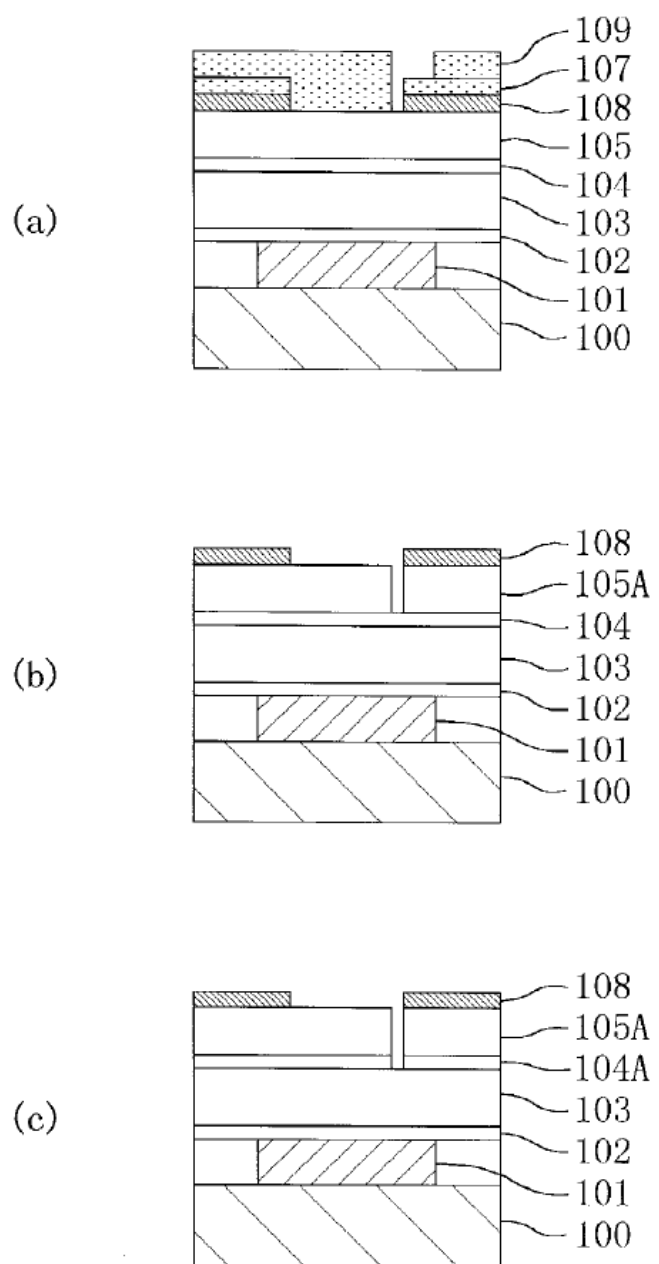




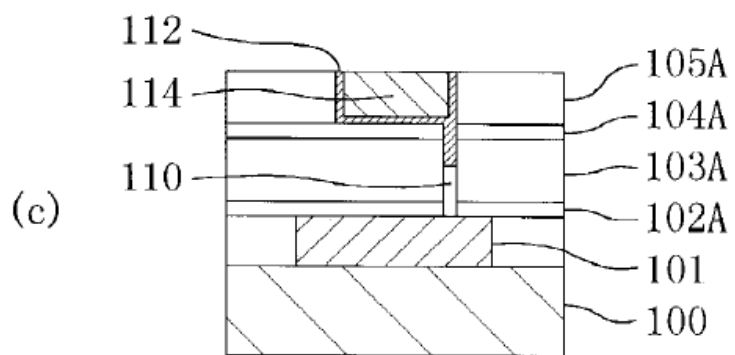
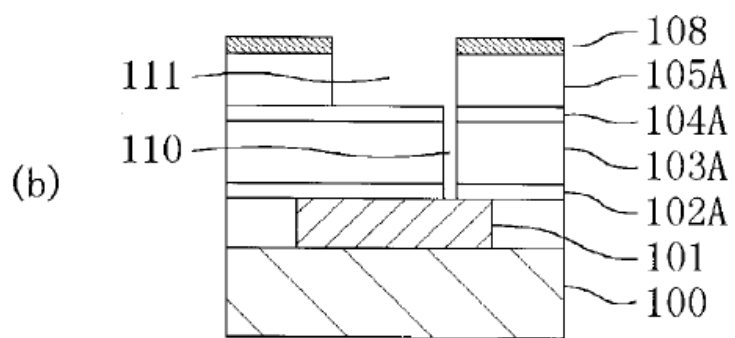
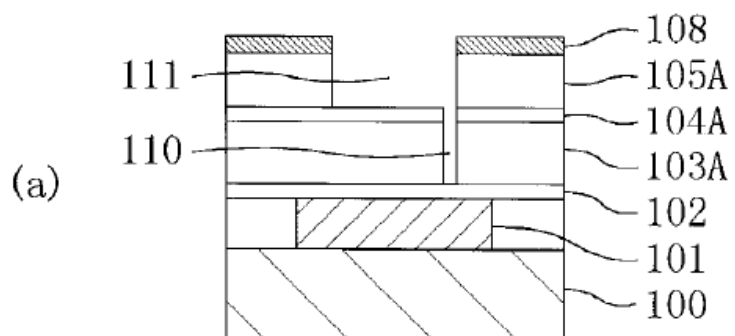
[Figure 4]



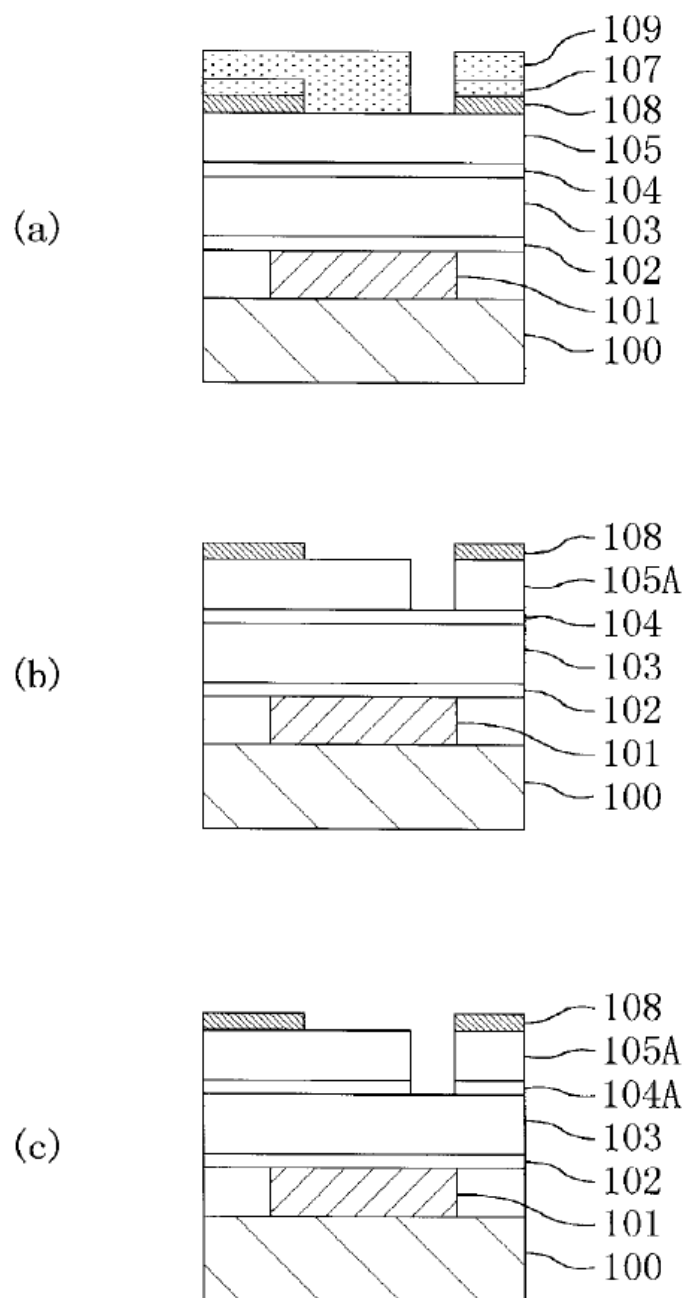
[Figure 5]



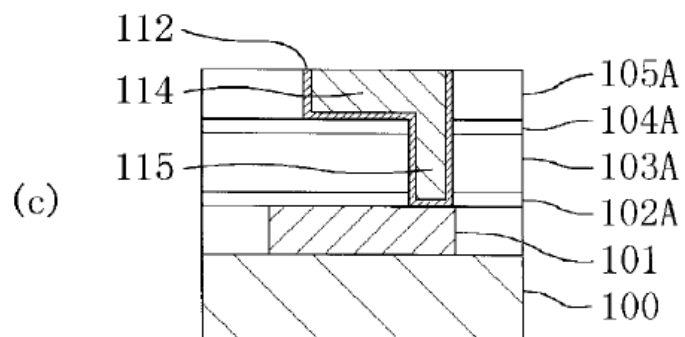
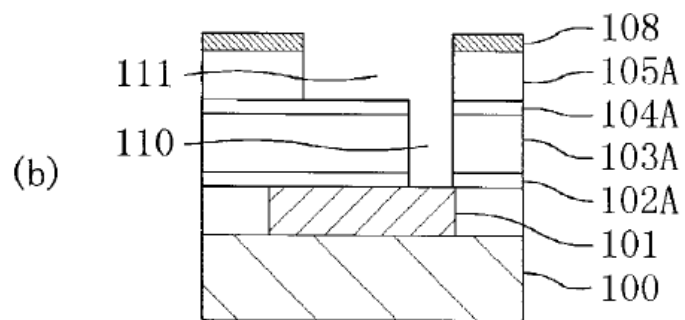
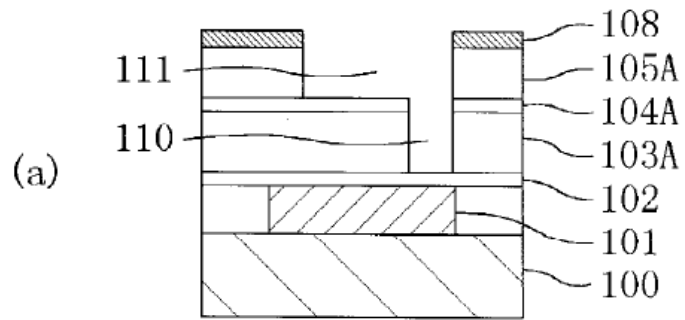
[Figure 6]



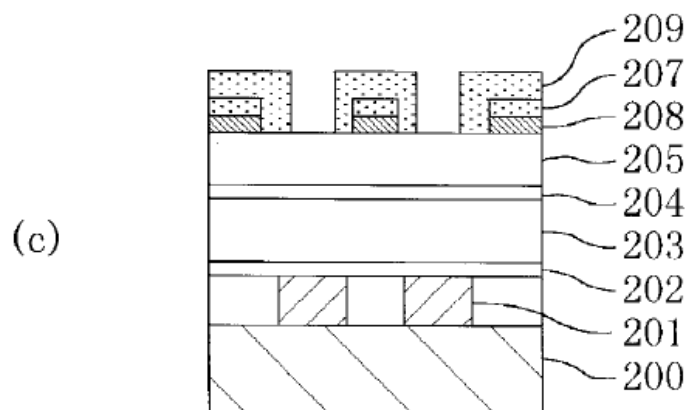
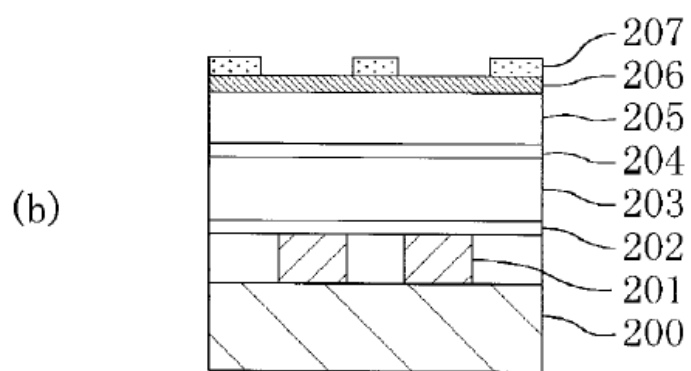
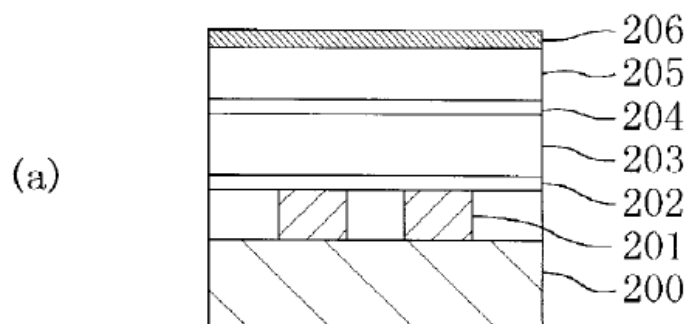
[Figure 7]



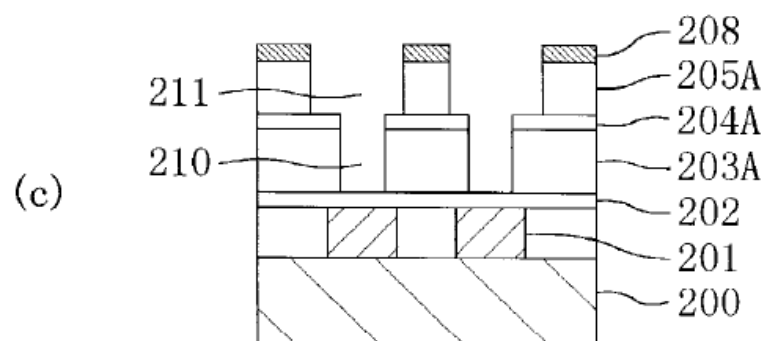
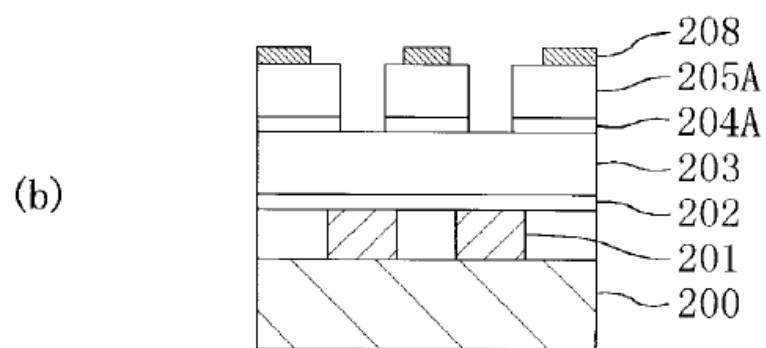
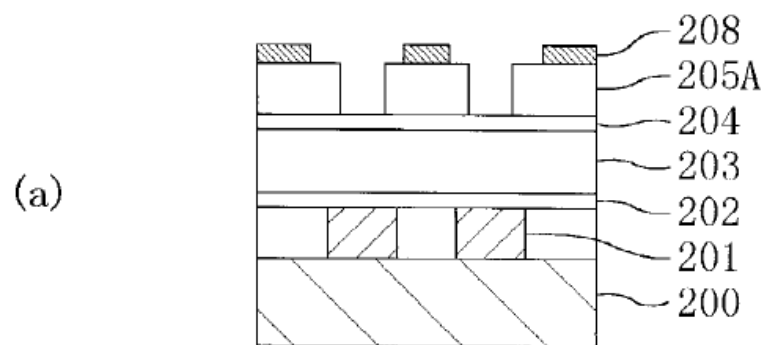
[Figure 8]



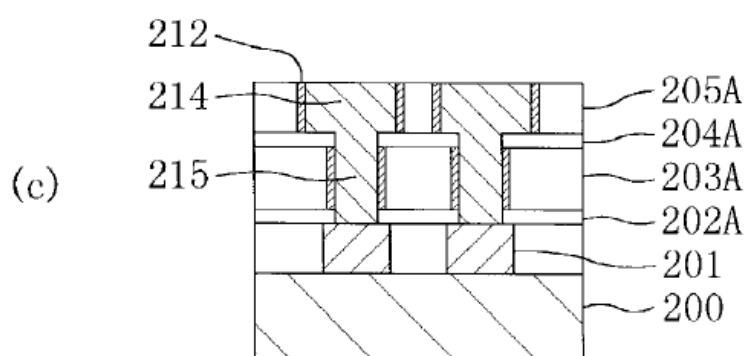
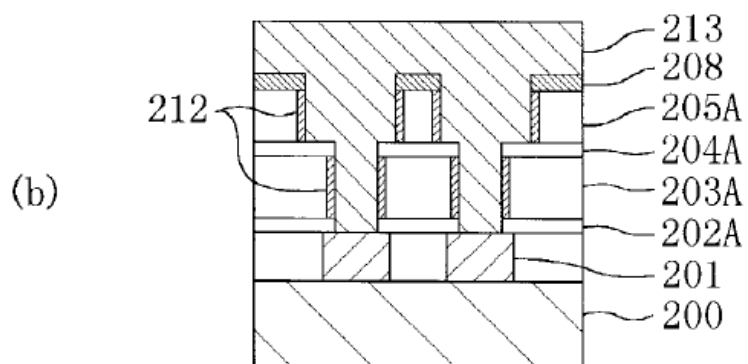
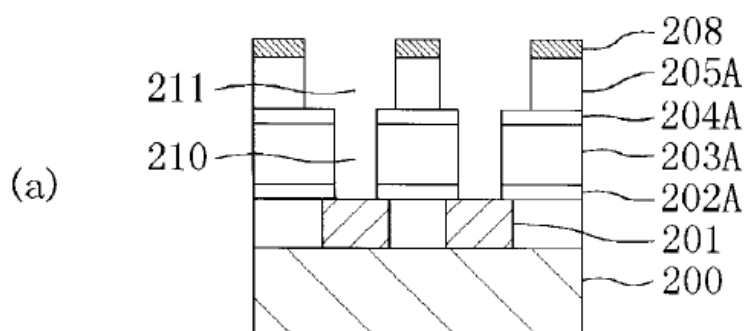
[Figure 9]



[Figure 10]

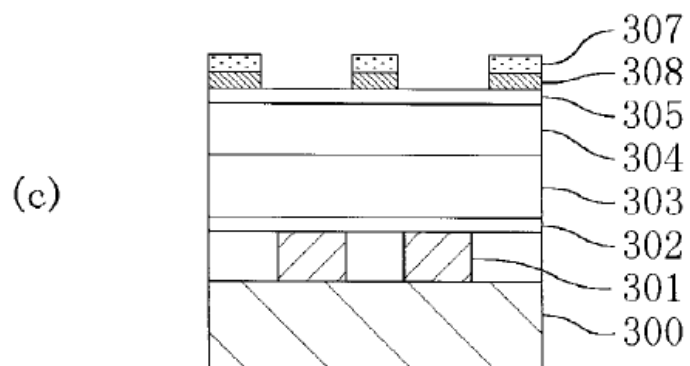
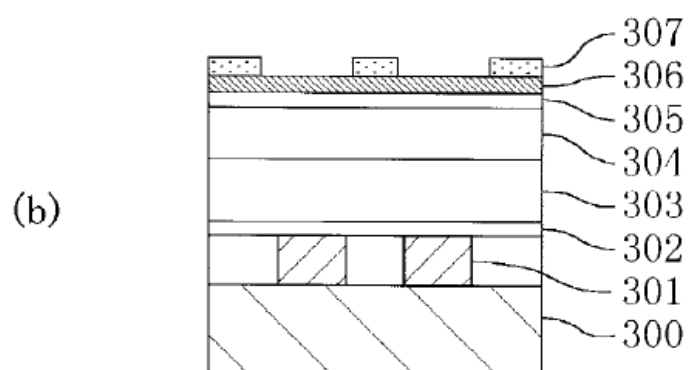
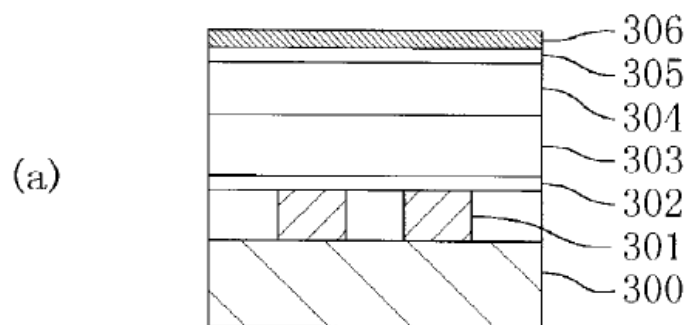


[Figure 11]

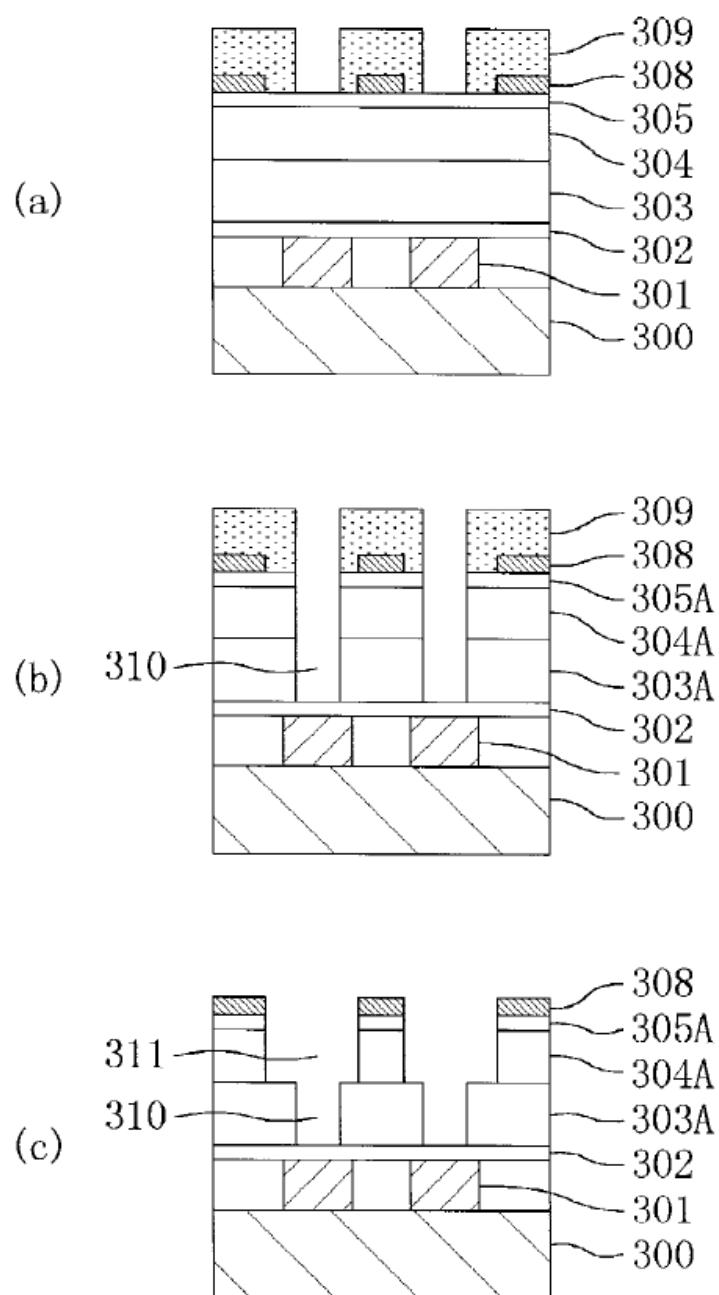




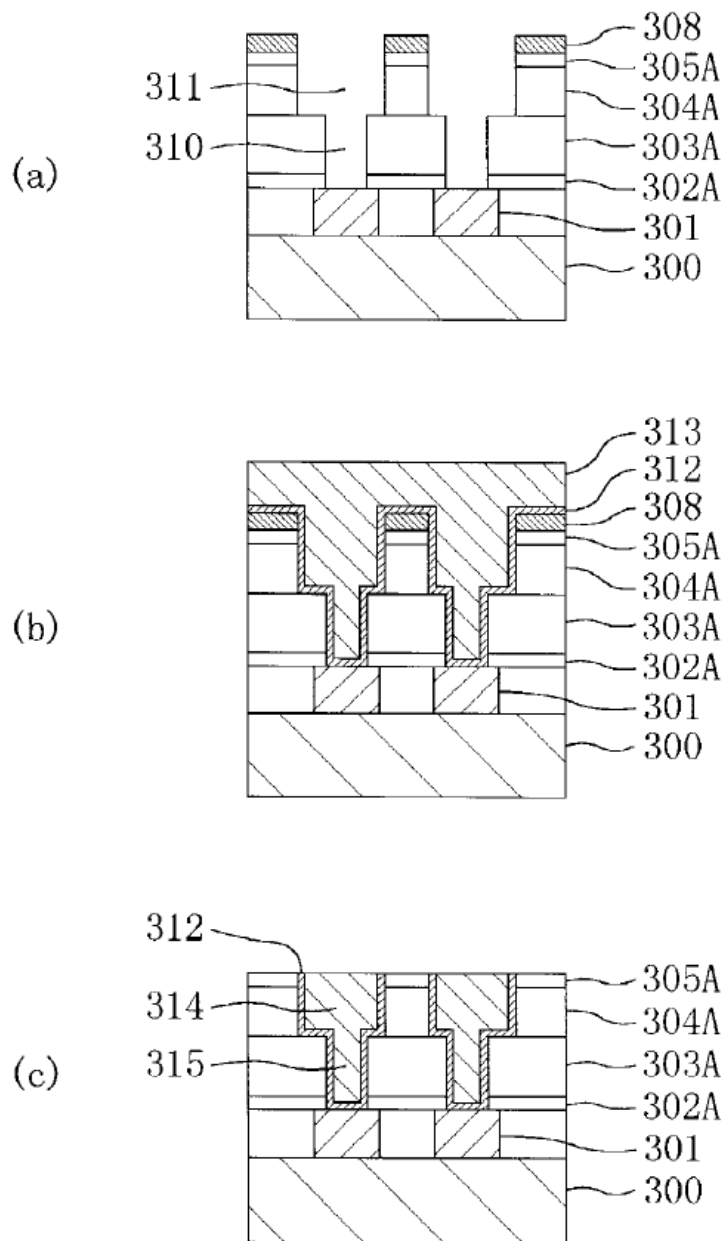
[Figure 12]



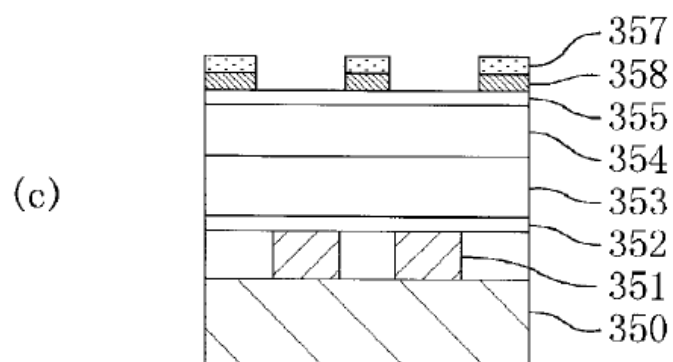
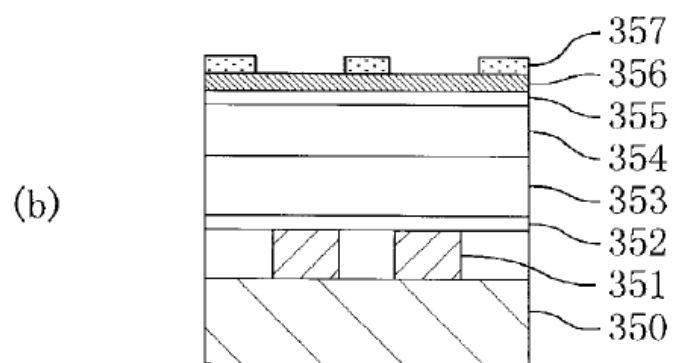
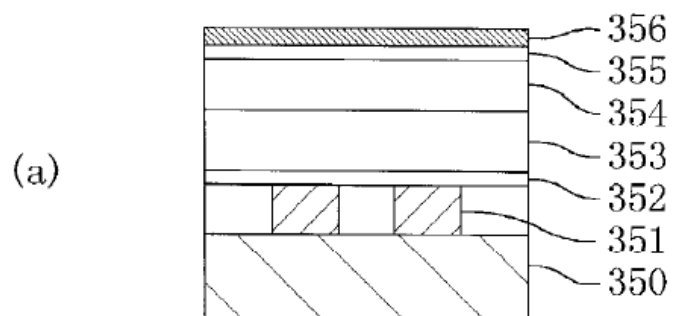
[Figure 13]



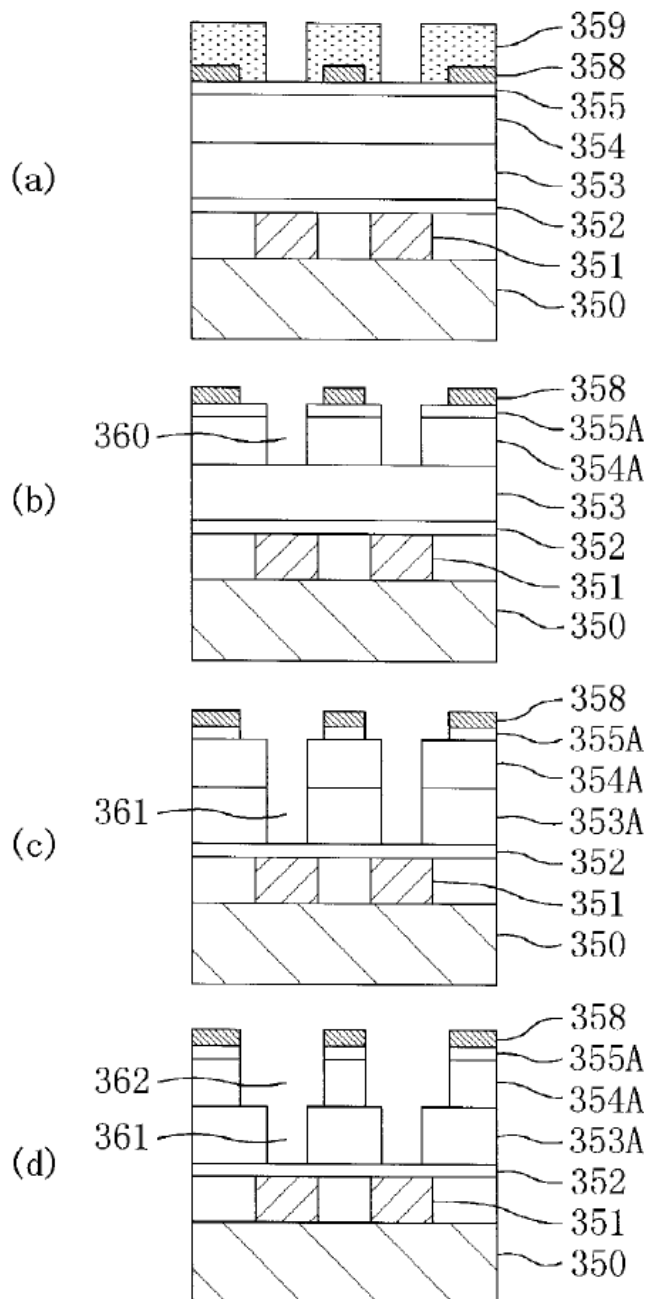
[Figure 14]



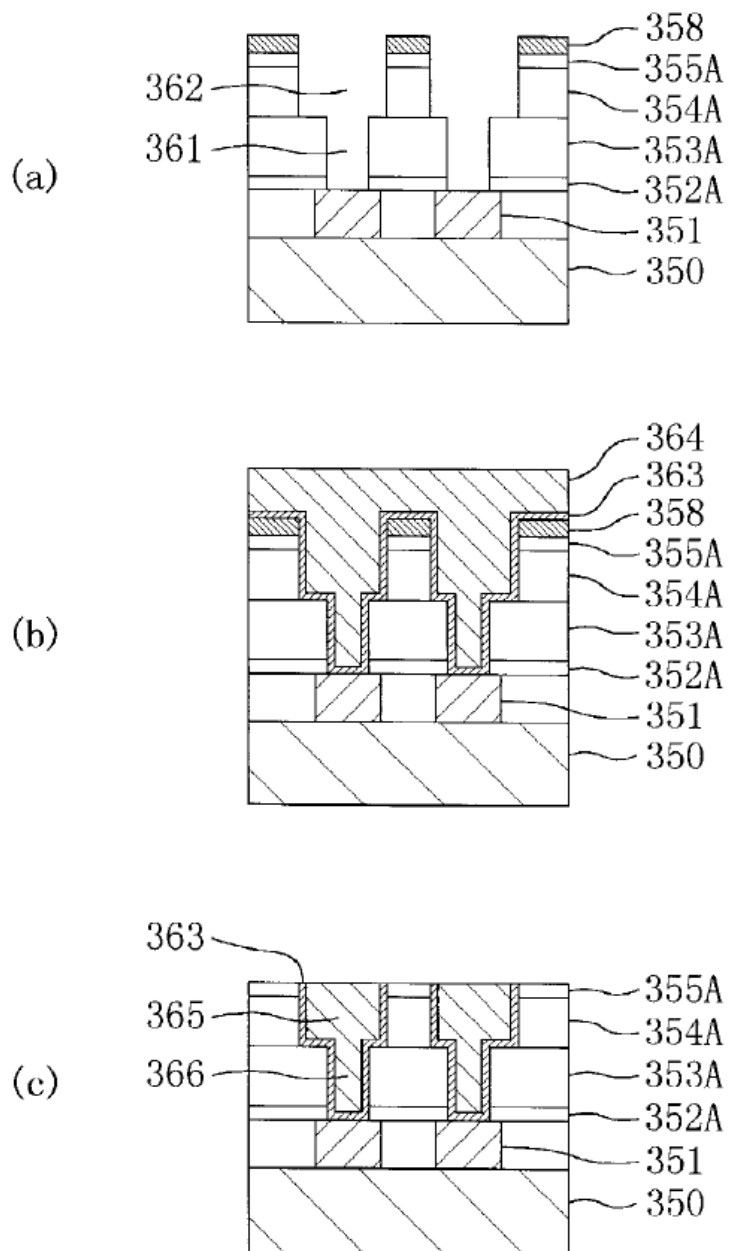
[Figure 15]



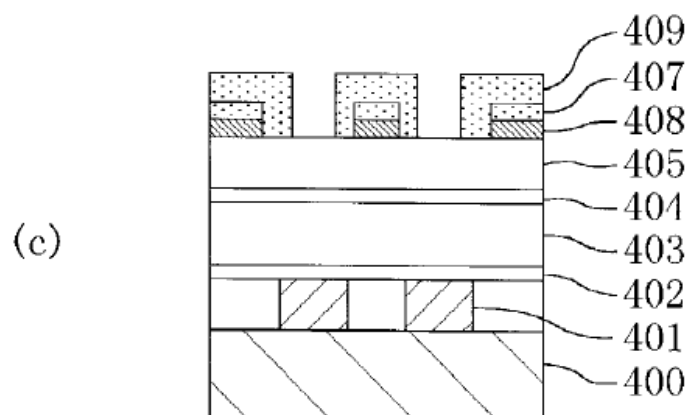
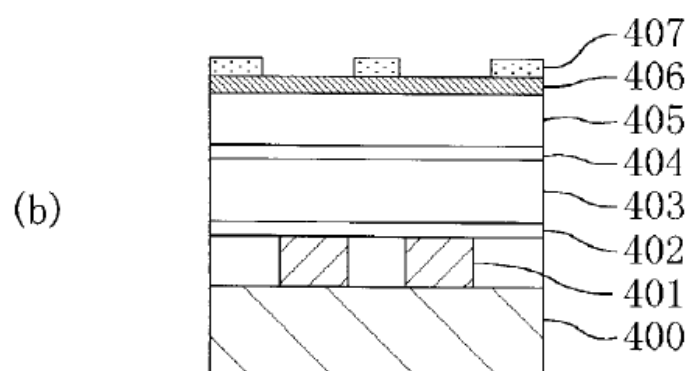
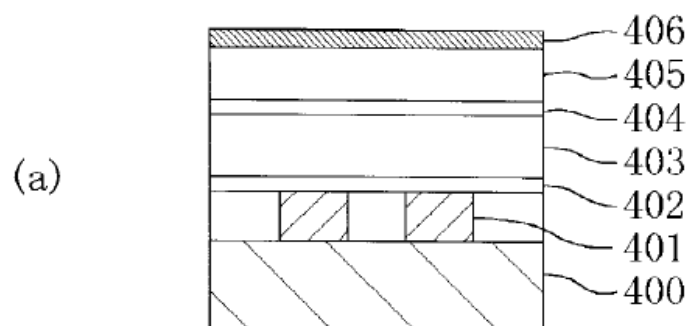
[Figure 16]



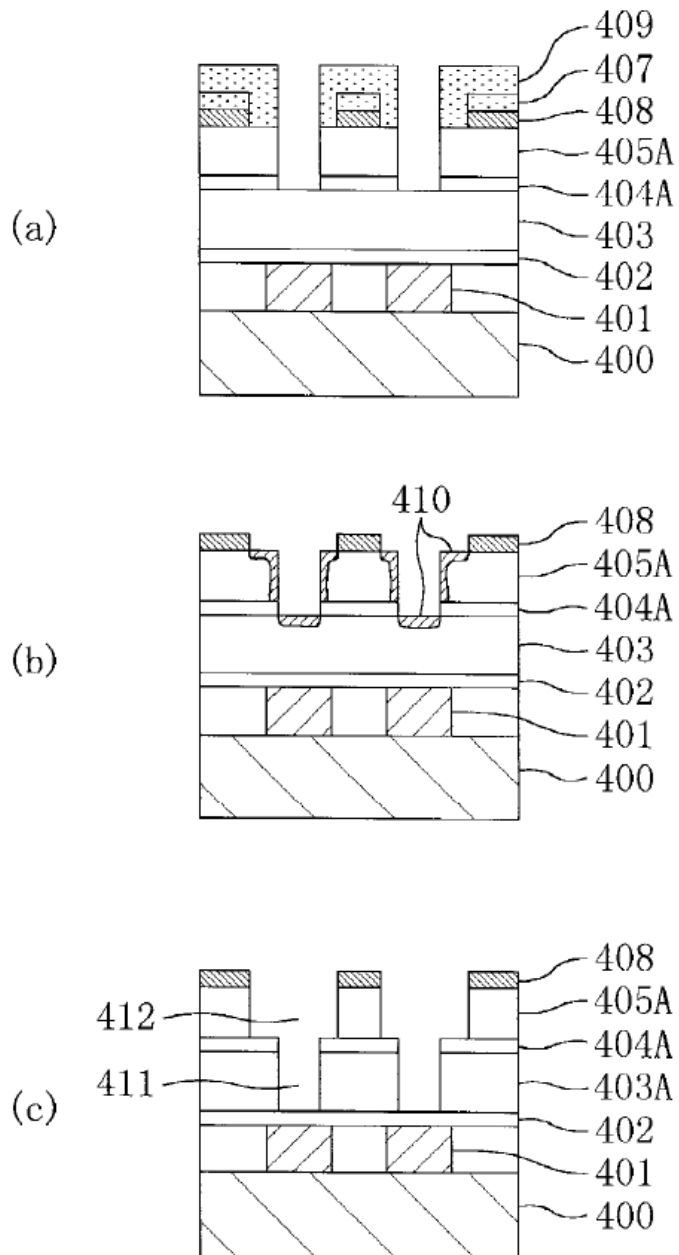
[Figure 17]



[Figure 18]

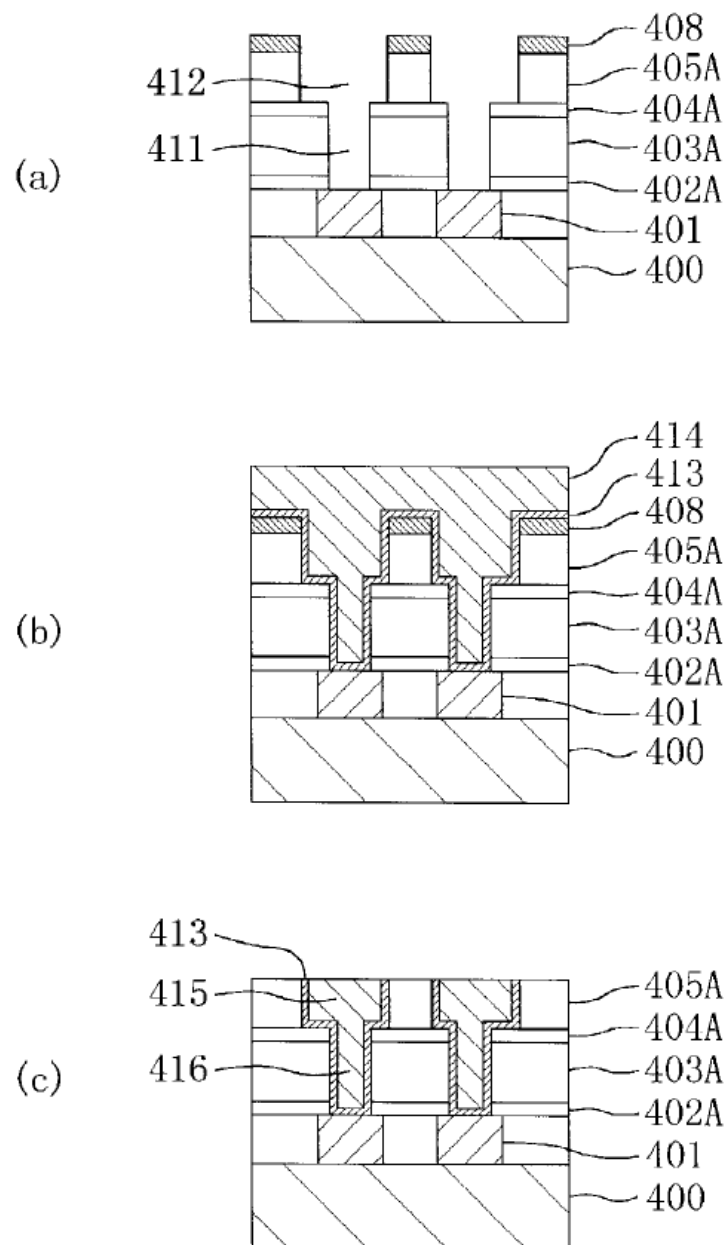


[Figure 19]





[Figure 20]



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[Name of Document] Abstract  
[Abstract]

[Subject] To enable the formation of an interlevel insulating film having a low relative dielectric constant using a conventional resist process.

[Means of Resolution] A silicon nitride film 102, first organic film 103, organic constituent-incorporated silicon oxide film 104, second organic film 105 and titanium nitride film 106 are sequentially deposited on a first metal wiring 101 over a semiconductor substrate 100, followed by formation of a mask pattern 108 by etching the titanium nitride film 106 using the first resist pattern 107 formed on the titanium nitride film 106 as a mask. Then, a second resist pattern is formed over the second organic film 105. The second organic film 105 is etched using the second resist pattern 109 as a mask, after which the second organic film 105 is patterned and both the first and second resist patterns 107 and 109 are removed. The second organic film 105 is etched using the mask pattern 108 as a mask to form wiring grooves and the first organic film 103 is etched using the patterned organic constituent-incorporated silicon oxide film 104 as a mask to form contact holes.

[Selected Diagrams] Figure 1

[Document Name] Ex officio correction data  
[Patent] 10-079371

[Drafting date]  
[Coordinator Code] 6175 Page: 1/1

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[Name of Document] Ex officio correction data  
[Corrected Document] Patent Application  
<Certification Information - Additional Information>  
[Patent Applicant]

[Identification number] 00005821  
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