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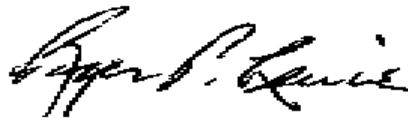
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I hereby certify that the Japanese translation of the
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JP Hei. 11 [1999] – 075519 Part I

is true, and that all statements of information and belief
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SINCERELY,

A handwritten signature in black ink, appearing to read "Roger P. Lewis". The signature is fluid and cursive, with the first name "Roger" being more prominent.

ROGER P. LEWIS

Date: June 30, 2016

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【Name of Item】 Abstract 1

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【Document Name】 Specifications

【Name of Invention】 Formation Method of Wiring Structure

【Scope of the Patent Claims】

【Claim 1】 A formation method of wiring structure that is characterized by the following:

Process 1, by which a 1st insulating film is formed over the lower layer of metal wiring, and Process 2, by which a 2nd insulating film that differs in composition from the afore described 1st insulating film is formed over this 1st insulating film, and

Process 3, by which a 3rd insulating film that differs in composition from the afore described 2nd insulating film is formed over this 2nd insulating film, and

Process 4, by which a thin film is formed over the afore described 3rd insulating film, and

Process 5, by which a 1st resist pattern that has opening(s) for forming wiring is formed over the afore described thin film, and

Process 6, by which etching is performed vis-à-vis the afore described thin film whilst using the afore described 1st resist pattern as a mask, thus forming from the afore described thin film a mask pattern that has opening(s) for forming wiring, and

Process 7, by which a 2nd resist pattern that has opening(s) for contact hole formation is formed over the afore described 3rd insulating film, and

Process 8, by which dry etching is performed vis-à-vis the afore described 3rd insulating film so that the etching conditions for the etching rate for the afore described 3rd insulating film vis-à-vis the 1st resist pattern and the 2nd resist pattern is high whilst the etching rate vis-à-vis the afore described 2nd insulating film is low, so that together with pattern formation on the afore described 3rd insulating film of opening(s) for contact hole formation on this 3rd insulating film, and the total or partial removal of the afore described 1st resist pattern and the 2nd resist pattern, and

Process 9, by which the etching conditions are such that the etching rate vis-à-vis the afore described 2nd insulating film is high, the etching rate vis-à-vis the 3rd insulating film is low, the patterning is in such a way as to form on the afore described 2nd insulating film contact hole formation opening(s) on this 2nd insulating film, with, as a mask, the afore described 3rd insulating film that has been patterned vis-à-vis the afore described 2nd insulating, and

Process 11, by which, under etching [...]

[...] conditions such that the etching rate vis-à-vis the afore described 1st insulating film and 3rd insulating film is high whilst the etching rate vis-à-vis the afore described mask pattern and 2nd insulating pattern is low, are conducted dry etching vis-à-vis the afore described 3rd insulating film as the afore described mask pattern and also conducting dry etching vis-à-vis the afore described 1st insulating pattern as the patterned afore described 2nd insulating film, resulting in the formation of the wiring groove(s) in the afore described 3rd insulating film together with the contact hole(s) in the afore described 1st insulating film, and

Process 11, by which the filling of the afore described wiring groove(s) and contact hole(s) with a metal film so as to form the contact that connects the upper level metal wiring & the afore described lower level metal wiring and the afore described lower level metal wiring & the afore described upper level metal wiring.

【Claim 2】 The formation method of wiring structure of Claim 1 that is characterized by the fact that it is further equipped with a process between the afore described Process 10 and Process 11 of the formation of an adhesive layer consisting of a metal film that is formed in the exposed portion(s) of the afore described wiring groove(s) in the afore describe 3rd insulating film and the exposed portion(s) of the afore described contact hole(s) of the afore described 1st insulating film.

【Claim 3】 The formation method of wiring structure described in Claim 1 that is characterized by the fact that the afore described 3rd insulating film is mainly composed of organic component(s).

【Claim 4】 The formation method of wiring structure described in Claim 3 that is characterized by the fact it includes the formation of the afore described 3rd insulating film by means of the CVD method wherein a perfluorodecalin containing reactive gas is used.

【Claim 5】 The formation method of wiring structure described in Claim 3 that is characterized by the fact that the afore described 1st insulating film is mainly composed of organic component(s).

【Claim 6】 The formation method of wiring structure of Claim 5 that is characterized by the fact that it is further equipped with a process between the afore described Process 10 and Process 11 of the formation of an adhesive layer by the plasma processing wherein nitrogen-containing reactive gas(es) is/are used on the exposed portion(s) of the afore described wiring groove(s) in the afore describe 3rd insulating film and the exposed portion(s) of the afore described contact hole(s) of the afore described 1st insulating film.

【Claim 7】 The formation method of wiring structure described in Claim 3 that is characterized by the fact it includes the formation of the afore described 1st insulating film by means of the CVD method wherein a perfluorodecalin containing reactive gas is used.

【Claim 8】 A formation method of wiring structure that is characterized by the following:
Process 1, by which a 1st insulating film is formed over the lower layer of metal wiring, and [...]

[...] Process 2, by which a 2nd insulating film that differs in composition from the afore described 1st insulating film is formed over this 1st insulating film, and

Process 3, by which a 3rd insulating film that differs in composition from the afore described 2nd insulating film is formed over this 2nd insulating film, and

Process 4, by which a thin film is formed over the afore described 3rd insulating film, and

Process 5, by which a 1st resist pattern that has opening(s) for forming wiring is formed over the afore described thin film, and

Process 6, by which etching is performed vis-à-vis the afore described thin film whilst using the afore described 1st register pattern as a mask, thus forming from the afore described thin film a mask pattern that has opening(s) for forming wiring, and

Process 7, by which a 2nd resist pattern that has opening(s) for contact hole formation is formed over the afore described 3rd insulating film, and

Process 8, by which etching conditions are such that the etching rate is high vis-à-vis the afore described 3rd insulating film whilst the etching rate is low for the etching vis-à-vis the afore described 2nd insulating film and the 1st resist pattern & the 2nd resist pattern is low, and dry etching is performed vis-à-vis the afore described 3rd insulating film, whilst using the afore described 1st resist pattern and the 2nd resist pattern as a mask, thus patterning so as to form in the afore described 3rd insulating film the opening portion(s) for the contact hole formation of this 3rd insulating film.

Process 9, by which etching conditions are such that the etching rate is high vis-à-vis the afore described 2nd insulating film whilst the etching rate is low for the etching vis-à-vis the afore described 1st insulating film, the 3rd insulating film, the 1st resist pattern and the 2nd resist pattern, the patterning is in such a way as to form on the afore described 2nd insulating film the contact hole opening portion(s) on this 2nd insulation fil, by means of performing dry etching with the afore described 1st resist pattern and the 2nd resist pattern vis-à-vis the afore described insulating film, and

Process 10, by which the afore described 1st resist pattern and the 2nd resist pattern are removed, and

Process 11, by which etching conditions are such that the etching rate is high vis-à-vis the afore described 3rd insulating film and 1st insulating film whilst the etching rate is low for the etching vis-à-vis the afore described mask pattern and the 2nd insulating film, the 3rd insulating film, the 1st resist pattern and the 2nd resist pattern, by means of performing dry etching vis-à-vis the afore described 3rd insulating film with the afore described mask pattern as a mask, and together with performing dry etching vis-à-vis the afore described 1st insulating film with the afore described patterned 2nd [...]

[...] insulating film as a mask in such a way as to form on the afore described wiring groove(s) of the afore described 3rd insulating film as well as the contact hole(s) of the afore described 1st insulating film, and

Process 12, by which the filling of the afore described wiring groove(s) and contact hole(s) with a metal film so as to form the contact that connects the upper level metal wiring & the afore described lower level metal wiring and the afore described lower level metal wiring & the afore described upper level metal wiring.

【Claim 9】 The formation method of wiring structure described in Claim 8 that is characterized by the fact that afore described 3rd insulating film is mainly a low dielectric constant SOG film that has a siloxane skeleton.

【Claim 10】 A formation method of wiring structure that is characterized by the following:

Process 1, by which a 1st insulating film is formed over the lower layer of metal wiring, and

Process 2, by which a 2nd insulating film that differs in composition from the afore described 1st insulating film is formed over this 1st insulating film, and

Process 3, by which a 3rd insulating film that differs in composition from the afore described 2nd insulating film is formed over this 2nd insulating film, and

Process 4, by which a 4th insulating film that differs in composition from the 3^d insulating film is formed over the afore described 3rd insulating film, and

Process 5, by which a thin film is formed over the afore described 4th insulating film, and

Process 6, by which is formed on the afore described 4th insulating film a 1st resist pattern that has wiring formation opening portion(s), and

Process 7, by which etching is performed vis-à-vis the afore described thin film with the afore described 1st resist pattern as a mask, to form from the afore described thin film a mask pattern that has wiring formation opening portion(s), and

Process 8, by which, after removing the 1st resist pattern, the 2nd resist pattern on the afore described 4th insulating film is formed such that a 2nd resist pattern that has wiring formation opening portion(s), and

Process 9, by which dry etching is performed vis-à-vis the afore described 4th insulating film with the afore described 2nd resist pattern and a mask pattern are used as a mask so as to form patterning on the afore described 4th insulating film such that this 4th insulating film has wiring formation opening portion(s), and

Process 10, by which dry etching is performed, with the patterned afore described 4th insulating film as a mask, vis-à-vis the afore described 3rd insulating film in a way so as to form on the afore described 3rd insulating film control hole formation opening portion(s) of this 3rd insulating film, and

Process 11, by which dry etching is performed, with the afore described mask pattern as a mask, vis-à-vis the patterned afore described 4th insulating film together with dry etching, with the patterned afore described 3rd insulating film as a mask, vis-à-vis the afore described 2nd insulating film so as to form the wiring groove(s) of the patterned afore described 4th insulating film together with the patterning of the afore described 2nd insulating film so that contact hole formation opening portion(s) is/are formed on this 2nd insulating film, and

Process 12, by which dry etching is performed, with the afore described mask pattern as a mask, vis-à-vis the patterned afore described 3rd insulating film together with dry etching, with the patterned afore described 2nd insulating film as a mask, vis-à-vis the afore described 1st insulating film so as to form the wiring groove(s) of the patterned afore described 4th insulating film together with the patterning of the afore described 2nd insulating film so that contact hole(s) is/are formed on afore described 1st insulating film, and

Process 13, by which the filling of the afore described wiring groove(s) and contact hole(s) with a metal film so as to form the contact that connects the upper level metal wiring & the afore described lower level metal wiring and the afore described lower level metal wiring & the afore described upper level metal wiring.

【Claim 11】 The formation method of wiring structure described in Claim 10 that is characterized by the fact that at least 1 of the afore described 2nd insulating film and the 3rd insulating film is such that the main composition component is organic, and

【Claim 12】 The formation method of wiring structure described in Claim 11 that is characterized by the fact that the dimensions of the contact hole formation opening portion(s) are, vis-à-vis the dimensions of the contact hole(s), larger in the vertical direction vis-à-vis the direction in which the afore described upper level of the metal wiring extends.

【Claim 13】 A formation method of wiring structure that is characterized by the following:

Process 1, by which a 1st insulating film is formed over the lower layer of metal wiring, and

Process 2, by which a 2nd insulating film that differs in composition from the afore described 1st insulating film is formed over this 1st insulating film, and

Process 3, by which a 3rd insulating film that differs in composition from the afore described 2nd insulating film is formed over this 2nd insulating film, and

Process 4, by which a thin film is formed over the afore described 4th insulating film, and

Process 5, by which is formed on the afore described 4th insulating film a 1st resist pattern that has wiring formation opening portion(s), and

Process 6, by which etching is performed vis-à-vis the afore described thin film with the afore described 1st resist pattern as a mask, to form from the afore described thin film a mask pattern that has wiring formation opening portion(s), and

Process 7, by which, after removing the 1st resist pattern, the 3rd resist pattern on the afore described 4th insulating film is formed such that a 2nd resist pattern that has wiring formation opening portion(s), and

Process 8, by which dry etching is performed vis-à-vis the afore described 3rd insulating film with the afore described 3rd resist pattern and a mask pattern are used as a mask so as to form patterning on the afore described 3rd insulating film such that this 4th insulating film has wiring formation opening portion(s), and

Process 9, by which dry etching is performed, with the patterned afore described 3rd insulating film as a mask, vis-à-vis the afore described 2nd insulating film in a way so as to form on the afore described 2nd insulating film control hole formation opening portion(s) of this 2nd insulating film, and

Process 10, by which dry etching is performed, with the afore described mask pattern as a mask, vis-à-vis the patterned afore described 3rd insulating film together with dry etching, with the patterned afore described 1st insulating film as a mask, vis-à-vis the afore described 2nd insulating film so as to form the wiring groove(s) of the patterned afore described 3rd insulating film together with the patterning of the afore described 1st insulating film so that contact hole formation opening portion(s) is/are formed on afore described 1st insulating film, and

Process 11, by which the filling of the afore described wiring groove(s) and contact hole(s) with a metal film so as to form the contact that connects the upper level metal wiring & the afore described lower level metal wiring and the afore described lower level metal wiring & the afore described upper level metal wiring.

【Claim 14】 The formation method of wiring structure described in Claim 10 that is characterized by the fact that at least 1 of the afore described 2nd insulating film and the 3rd insulating film is such that the main composition component is organic, and

【Claim 15】 The formation method of wiring structure described in Claim 13 tht is characterized by the fact that the dimensions of the contact hole formation opening portion(s) are, vis-à-vis the dimensions of the contact hole(s), larger in the vertical direction vis-à-vis the direction in which the afore described upper level of the metal wiring extends.

【Detailed Explanation of the Invention】

【0001】

The present invention relates to a formation method of wiring structure in semi-conductor integrated circuit devices.

【Technical Field of the Invention】

【0002】

【Prior Art】

With the progression of integration on semi-conductor integrated circuits, he increase in wiring delay time, for which the increase in wiring capacity, which is the parasitic capacitance amongst the metal wires, has interfered with improving the performance of semi-conductor integrated circuits. This wiring delay time is what is called RC delay, and it is proportional to product of the resistance of the metal wiring and the line-to-line capacitance.

【0003】

Thus, in order to reduce the wiring delay time it is necessary to make the metal wiring resistance smaller or to reduce the line-to-line capacitance.

【0004】

With that, IBM Corporation and Motorola, Inc. have reported on semi-conductor integrated circuit devices wherein copper is used as the material for the wiring instead of aluminum alloys for the purpose of reducing the wiring resistance. Because copper materials have specific resistance that is two-thirds that of aluminum allow materials, when copper materials are used as wiring materials, it is possible to actualize a high speed that is 1.5 times as compared with when aluminum alloy materials are used because simple calculation shows that the wiring delay time is reduced by two-thirds.

【0005】

However, there is the concern that as the integration of semi-conductor circuits proceeds, even with the use of copper wiring wherein copper is used, there may be limitations in terms of speed. Also, when copper is used as wiring material, because the specific resistance of copper is the next smallest as compared to gold or silver so that even if gold or silver were to be used for metal wiring instead of copper, the [...]

[...] decrease in wiring resistance would only be slight.

【0006】

Because of this, suppressing the line-to-line capacitance as well as reducing the wiring resistance are important, and to reduce the line-to-line capacitance it is necessary to reduce the relative dielectric constant of the inter-level insulating films. Heretofore, silicon dioxide films have been used for inter-level insulating films but the relative dielectric constant is about 4 to 4.5, and there are difficulties in using them for inter-level integrating films in the more and more integrated semi-conductor integrated circuits.

【0007】

With that, the use of such as fluorine-doped silicon dioxide films, low dielectric constant SOG films and organic polymer films, which have smaller relative dielectric constants as compared to silicon dioxide films have been proposed.

【0008】

【Problems the Invention Seeks to Resolve】

【0009】

Although the relative dielectric constant of fluorine-doped silicon dioxide films is about 3.3 to 3.7, which is about 20% lower than that of conventional silicon dioxide films, fluorine-doped silicon dioxide films are highly hygroscopic and readily absorb moisture from the atmosphere, and this results in numerous problems such as the adverse increase in the relative dielectric constant of fluorine-doped silicon dioxide films and the reaction of SiOH groups with water during thermal treatment resulting in the release of H₂O gases, the segregation of the fluorine free radicals contained within fluorine-doped silicon dioxide films near the surface thereof during thermal treatment and the reaction and the reaction of SiOH groups with water during thermal treatment, so that the segregated fluorine reacts with the Ti and such of the TiN film that serves as an adhesive level forming a TiF film that tends to peel; there are numerous practical problems related to the use of fluorine-doped silicon dioxide films.

【0009】

HSQ (hydrogen silsesquioxane: composed of Si, O and H atoms, and which contains about two-thirds the number of O atoms as H atoms) have been considered but HSQ films release a larger quantity of moisture when compared with conventional silicon dioxide films, and as such it is difficult to process and when forming a metal wiring on HSQ films, it is necessary to use patterned metal wiring for the metal film.

【0010】

Furthermore, because HSQ films have low adhesion vis-à-vis the metal wiring, it is necessary to form a CVD film between the metal wiring and the HSQ film in order to form a CVD oxide film as an adhesion layer. However, when a CVD oxide film is formed on the metal wiring, there is a CVD oxide film with a large relative dielectric capacitance between metal wiring so that the actual line-to-line capacitance is equal to the serial capacitance formed by the HSQ film and the CVD film because of the presence of a CVD oxide film that has a high dielectric constant resulting in a line-to-line capacitance that is larger than when HSOQfilm alone is used.

【0011】

Because, like low dielectric constant SOG films, organic polymer films do not adhere strongly to the metal wiring, it is necessary to form a CVD oxide film as an adhesion layer between the metal wiring.

【0012】

Furthermore, the etch rate used for etching organic polymer films is approximately equal to the ash rate at which the resist pattern is ashed with oxygen plasma so that there is the problem that it is not possible to use the usual resist application process in such situations since organic polymer films are likely to be damaged during the ashing and the resist pattern removal. Thus forming a CVD oxide film on an organic film and forming a resist film on the CVD oxide film and then etching the resist film using the CVD oxide film as an etch stopper (protective film) have been proposed.

【0013】

However, when a CVD film is formed on an organic polymer film, the surface of the organic polymer film is exposed to oxygen containing reactive gases so that the organic polymer film reacts with the oxygen to take in polar groups such as carbonyl groups and ketone groups, and as a result, there is the problem of a disadvantageous increase in the relative dielectric constant of the organic polymer film.

【0014】

Also, when the filled-in wiring wherein copper is filled into the organic polymer film, because organic polymer films do not adhere well to the metal wiring, there is the need to form an adhesion layer in the wiring depressions that are formed in the organic polymer film by means of something like an adhesion layer made of TiN, etc. but because the resistance of a TiN film is high, there is the problem of the effective cross sectional area of the metal wiring is decreased, thus negating the low resistance merits of using metal wiring with copper.

【0015】

In consideration of the afore description, the objective has been a method for the formation of inter-layer films with low dielectric constant whilst using conventional resist processing.

【0016】

【Means for Resolving the Issues】

The 1st method for the formation of wiring structure in accordance with the present invention includes as the 1st process of the formation of a 1st insulating film over the lower-level metal wiring, the 2nd process of the formation of a 2nd insulating film wherein the composition differs from that of the 1st insulating film, the 3rd process of the formation on the 1st insulating film of a 3rd insulating film wherein the composition differs from that of the 2nd insulating film, the 4th process of the formation of a thin film on the 3rd insulating film, the 5th process of the formation on the thin film of a 1st resist pattern wherein there is a plurality of openings for the formation of wiring grooves, the 6th process of the etching of the thin film with the use of the 1st resist pattern as a mask thus forming a mask pattern out of the thin film so that there are openings for the formation of the wiring grooves, the 7th process of the formation on the 3rd insulating film of a 2nd resist pattern wherein there is a plurality of openings for the formation of contact holes, the 8th process of dry etching the 3rd insulating film under conditions such that the 3rd insulating film and 1st resist pattern & the 2nd resist pattern re etched at high rate whilst the 2nd insulating film is etched at a low rate so that the 3rd insulating film is patterned so as to have openings for the formation of contact holes, and the total or partial removal of the lower parts of the 1st resist pattern & the 2nd resist pattern, the 9th process of dry etching using the mask pattern and the patterned 2nd insulating film as the respective masks the 3rd insulating film & the 1st insulating film under conditions such that the 1st insulating film & the 3rd insulating film are etched at a high rate and the mask pattern & the 2nd insulating film are etched at a low rate so as to respectively form wiring grooves and contact holes in the 3rd insulating film & the 1st insulating film, the 10th process of dry etching the 3rd insulating film & the 1st insulating film using the mask pattern & the patterned 2nd insulating film as the respective masks under conditions [...]

[...] such that the 1st insulating film & the 3rd insulating film are etched at a high rate and the mask pattern & the 2nd insulating film are etched at a low rate so as to respectively form the wiring grooves and the contact holes in the 3rd insulating film & the 1st insulating film, and the 11th process of filling the wiring grooves and the contact holes with a metal film in order to form upper-level metal wiring and contacts that connect the lower-level metal wiring and the upper-level metal wiring.

【0017】

In the 1st method of the method for the formation of the wiring structure, the 3rd insulating film is dry etched under conditions such that the 3rd insulating film and the 1st resist pattern & the 2nd resist pattern are etched a high rate whilst the 2nd insulating film is etched at a low rate so that the patterning of the 3rd insulating film and the removal of the 1st resist pattern & the 2nd resist pattern as described in Process 8 so that it not necessary to perform the ashing process and the process of removing the 1st resist pattern & the 2nd resist pattern using oxygen plasma, which in turn means that because it is possible to prevent the 3rd insulating from being damaged during the ashing and the resist pattern removal, a low dielectric constant insulating film that would otherwise be readily damaged by oxygen plasma may be used for the 3rd insulating film; thus it is possible to use a low dielectric constant film for the inter-level insulating film for the formation with the use of n ordinal resist application process.

【0018】

Also, the 2nd insulating film can be used as an etching stopper during the course of the wiring groove formation by the dry etching of the 3rd insulating film using the mask pattern as a mask in Process 10 so that the depth of each of the wiring grooves can be equalized with the thickness of the 3rd insulating film.

【0019】

In the 1st method for the formation of the wiring structure, it is preferable to further equip Process 10 and Process 11 a method for the formation of adhesion layer that is made of a metal film in the portion of the wiring grooves of the 3rd insulating film that is exposed and the portion of the contact holes of the 1st insulating film that is exposed.

【0020】

In 1st method for the formation of the wiring structure, it is preferable for the 3rd insulating film to be one in which an organic component is the main component.

【0021】

In this case, it is preferable to have included in Process 3 a process whereby the 3rd insulating film is formed by the CVD method wherein a reactive gas that contains perfluorodecalin.

【0022】

Also, in this case, it is preferable for the 1st insulating film to be one in which an organic component is the main component.

【0023】

In the case that the 1st insulating film is one in which an organic component is the main component, it is further preferable for there to be between Process 10 and Process 11 a process for the formation of an adhesive layer from a plasma processing wherein a reactive gas that includes nitrogen is used for the portions of the wiring grooves of the 3rd insulating film that are exposed and the contact holes of the 1st insulating film that are exposed.

【0024】

In the case that the 1st insulating film is one in which an organic component is the main component, it is preferable that the 1st Process of the formation of the 1st insulating film be by the CVD method wherein a reactive gas that contains perfluorodecalin.

【0025】

The 2st method for the formation of wiring structure in accordance with the present invention includes as the 1st process of the formation of a 1st insulating film over the lower-level metal wiring, the 2nd process of the formation of a 2nd insulating film wherein the composition differs from that of the 1st insulating film, the 3rd process of the formation on the 1st insulating film of a 3rd insulating film wherein the composition differs from that of the 2nd insulating film, the 4th process of the formation of a thin film on the 3rd insulating film, the 5th process of the formation on the thin film of a 1st resist pattern wherein there is a plurality of openings for the formation of wiring grooves, the 6th process of the etching of the thin film with the use of the 1st resist pattern as a mask thus forming a mask pattern out of the thin film so that there are openings for the formation of the wiring grooves, the 7th process of the formation on the 3rd insulating film of a 2nd resist pattern wherein there is a plurality of openings for the formation of contact holes, the 8th process wherein the etching rate conditions for the etching vis-à-vis the 3rd insulating film is at a high rate and the etching vis-à-vis the 2nd insulation film, the 1st resist pattern & the 2nd resist pattern is at a low rate, and the patterning is conducted so as to form in the 3rd insulating film the contact holes of this 3rd insulating film by performing the dry etching vis-à-vis the 3rd insulating film with the 1st resist pattern & the 2nd resist pattern as a mask, the 9th process wherein the etching rate conditions for the etching vis-à-vis the 2nd insulating film is at a high rate and the etching vis-à-vis the 2nd resist pattern is at a low rate, and the patterning is conducted so as to form in the 3rd insulating film the contact hole formation opening portions of this 3rd insulating film by performing the dry etching vis-à-vis the 1st resist pattern & the 2nd resist [...]

[...] pattern as a mask, the 10th process of removing the resist patterns of the 1st insulation film & the 3rd insulation film, the 11th process wherein the etching rate conditions for the etching vis-à-vis the 1st insulating film & the 3rd insulating film is at a high rate and the etching vis-à-vis the mask pattern and the 2nd insulation film is at a low rate, and by the dry etching performed with the mask pattern as a mask vis-à-vis the 3rd insulating film as well as the dry etching performed mask pattern vis-à-vis 2nd insulating film the contact holes are formed in the 1st insulating film as well as the wiring grooves of the 3rd insulating film, and the 12th process of filling the wiring grooves and the contact holes with a metal film in order to form upper-level metal wiring and contacts that connect the lower-level metal wiring and the upper-level metal wiring.

【0026】

In the 2nd method for the formation of the wiring structure, even if a damaged layer is formed in the 1st insulating film & the 3rd insulating film that are exposed within the openings for the formation of the contact holes in the 2nd insulating film during the 10th process wherein the 1st resist pattern & the 2nd resist pattern are removed, the damaged layer is certain to be removed in the following 11th process wherein the 3rd insulating film & the 1st insulating film are dry etched using the mask pattern and the patterned 2nd insulating film as the masks under conditions such that the 1st insulating film & the 3rd insulating film are etched at a high rate whilst the mask pattern & the 2nd insulating film are etched at a low rate in order to form the wiring grooves and the contact holes in the 3rd insulating film & the 1st insulating film.

【0027】

In the 2nd method for the formation of the wiring structure it is preferable for the 3rd insulation film to be a low dielectric constant SOG film that has a siloxane skeleton.

【0028】

The 3rd method for the formation of the wiring structure includes [...]

[..] the 1st process by which the 1st insulating film is formed over the lower-level metal wiring, the 2nd process by which the 2nd insulating film that has a composition that differs from the composition of the 1st insulating film, the 3rd process by which a 3rd insulating film that has a composition that differs from the composition of the 2nd insulating film is formed over the 2nd insulating film, the 4th process by which a 4th insulating film that has a composition that differs from the composition of the 3rd insulating film is formed over the 3rd insulating film, the 5th process by which a thin film is formed over the 4th insulation film, the 6th process by which a 1st resist pattern such that the 1st resist pattern has openings for the formation of wiring grooves is formed on the thin film, the 7th process by which the thin film is etched using the 1st resist pattern as a mask so as to form a mask pattern from the thin film wherein there are formed openings for the formation of the wiring grooves, the 8th process by which the 1st resist pattern is removed and the 2nd resist pattern is formed on the 4th insulating film and the mask pattern, with the 2nd resist pattern having openings for the formation of the contact holes, the 9th process by which dry etching of the 4th insulation film is performed using the 2nd resist pattern & the mask pattern as a mask, thus patterning the 4th insulating film so that it has openings for the formation of the contact holes, the 10th process by which dry etching of the 3rd insulating film is performed using the patterned 4th insulating film as a mask, thus patterning the 3rd insulating film so that it has openings for the formation of the contact holes, the 11th process by the dry etching of the patterned 4th insulating film and the 2nd insulating film is performed using respectively the mask pattern and the patterned 3rd insulating film as 2nd insulating the masks, thus forming the wiring grooves in the patterned 4th insulating film and the patterning of the 3rd insulating film so that it has openings for the formation of the wiring grooves, the 12th process by which the patterned 3rd insulating film & the 1st insulating film are dry etched using respectively the mask pattern & the patterned 2nd insulating film as the mask, thus forming respectively the wiring grooves and the contact holes in the patterned 3rd insulating film & the 1st insulating film, and the 13th process by which the wiring grooves and the contact holes are filled with a metal film, thus forming the connection of the upper-level metal wiring and contacts with the lower level metal wiring.

【0029】

In the 3rd method for the formation of the wiring structure, because the 4th insulating film is located on the 3rd insulating film during the removal of the 1st resist pattern & the 2nd resist [...]

[...] pattern of the 8th process even if the 1st resist pattern is removed by oxygen plasma, the 3rd insulating film is on the 1st insulating film during the dry etching of the 3rd insulating film of the 10th process, so that the 3rd insulating film is not damaged. Also, in the 10th process, when the dry etching is performed on the 3rd insulating film, because the 2nd insulating film is located on the 1st insulating film, the 1st insulating is not damaged.

【0030】

In the case of the 3rd method for the formation of the wiring structure, it is desirable, for the 1st insulation film and the 3rd insulation film, that at least 1 of them is mainly composed of an organic composition.

【0031】

In the case of the 3rd method for the formation of the wiring structure, it is desirable, for the dimensions of contact holes of the 2nd resist pattern for the formation of the opening portions to be, vis-à-vis the design dimensions of the contact holes, larger in the direction vertical to the direction in which the upper-level metal wiring extends.

【0032】

The 4th method for the formation of the wiring structure includes as the 1st process by the 1st insulating film is formed over the lower-level metal wiring, the 2nd process by which the 2nd insulating film that has a composition that differs from the composition of the 1st insulating film is formed over the 1st insulating film, the 3rd process by which a 3rd insulating film that has a composition that differs from the composition of the 2nd insulating film is formed over the 2nd insulating film, the 4th process by which a thin film is formed over the 3rd insulating film, the 5th process by which a first resist pattern is formed on the thin film, the 6th process by which the thin film is etched using the 1st resist pattern as a mask so as to form a mask pattern from the thin film wherein there are formed openings for the formation of the wiring grooves, the 7th process by which the 1st resist pattern is removed and the 2nd resist pattern is formed on the 4th insulating film and the mask pattern, with the 2nd resist pattern having openings for the formation of the contact holes, the 8th process by which dry etching of the 3rd insulation film is performed using the 2nd resist pattern & the mask pattern as a mask so as to pattern the 4th insulating film so that it has openings for the formation of the contact holes, the 9th process by which dry etching of the 2nd insulating film is performed using the 3rd insulating film as a mask so that the 2nd insulating film is patterned to have the openings for the formation of the contact holes, the 10th process by the dry etching of the patterned 4th insulating film and the 2nd insulating film is performed using [...]

[...] respectively the mask 3rd pattern and the patterned 1st insulating film as the masks, thus forming the wiring grooves in the patterned 3rd insulating film and the patterned the 1st insulating film so that it has openings for the formation of the wiring grooves, and the 11th process by which the wiring grooves and the contact holes are filled with a metal film, thus forming the connection of the upper-level metal wiring and contacts with the lower level metal wiring.

【0033】

According to the 4th method for the formation of the wiring structure, during the dry etching of the 3rd insulating film in the course of the 8th process, the 2nd insulating film is located on the 1st insulating film so that the 1st insulating film is not damaged.

【0034】

In the case of the 4th method for the formation of the wiring structure, it is desirable, for the 1st insulation film and the 3rd insulation film, that at least 1 of them is mainly composed of an organic composition.

【0035】

In the case of the 4th method for the formation of the wiring structure, it is desirable, for the dimensions of contact holes of the 2nd resist pattern for the formation of the opening portions to be, vis-à-vis the design dimensions of the contact holes, larger in the direction vertical to the direction in which the upper-level metal wiring extends.

【0036】

【Descriptions of the Preferred Embodiments】

In the following are descriptions of each of the embodiments of the present invention; therein, organic film includes both films that are composed solely of organic composition and films mainly composed of organic composition. In each of the embodiments, it is possible to change a film that is mainly composed of organic composition with a film that is solely composed of organic composition.

(1st Embodiment)

In the following is given explanations of the method for the formation of the wiring structure that relates to the 1st embodiment of the present invention whilst referring to Figure 1 (a) ~ (c), Figure 2 (a) ~ (3) and Figure 3 (a) ~ (c).

【0037】

First, as is shown in Figure 1(a), silicon nitride film 102 is formed over the 1st metal wiring 101 that is formed on semi-conductor substrate 100, with the silicon nitride film thickness at, for example, 50nm, and used to protect 1st metal wiring 101 during later etching step(s), and then 1st organic film 103 (1st insulating film), which has a mainly organic composition, is formed to a thickness of, for example, 1μm, on silicon dioxide film 102, and then organic composition containing silicon dioxide film 104 (2nd insulating film), which contains organic composition in the silicon dioxide is formed to a thickness of, for example, 50nm, on 1st organic film 103. Then 2nd organic film 105, which is of mainly organic composition, is formed to a thickness of, for example, 400nm over silicon dioxide film 104, which contains organic composition, and titanium nitride film 106 is formed to a thickness of, for example, 50nm on 2nd organic film 105.

【0038】

For the method of deposition of 1st and 2nd organic films 103 and 105, the method may be arbitrary; for example, the deposition may be by means of a plasma CVD process wherein a reactive gas that is mainly composed of perfluorodecalin can be used. Also, for the 1st and 2nd organic films 103 and 105, it is possible to use hydrocarbon films or hydrocarbon films that contain fluorine may be used for formation by means of plasma CVD, coating or thermal CVD.

【0039】

For the method of deposition of 1st and 2nd organic films 103 and 105, the method may be arbitrary; for example, the deposition may be by means of a plasma CVD process wherein a reactive gas that is mainly composed of perfluorodecalin and an organic silane such as hexamethyl disiloxane, arylalkoxy silane and alkylalkoxy silane may be used to obtain an organic/inorganic hybrid film.

【0040】

Also, in regards to the method of deposition of the silicon dioxide, it is not particularly limited; for example, the CDV method wherein reactive gas which is mainly composed of perfluorodecalin may be used. In this manner, silicon dioxide film 104 that contains organic composition and has taken in a phenyl group that has bound with the silicon atoms in the silicon dioxide may be obtained.

【0041】

As substitutes for titanium nitride film 106, the 1st and 2nd organic films 103 & 105 and the silicon dioxide film 104 that contains organic composition have a high degree of etching selectivity, which is to say it is possible to use a thin film with an amply slow etching speed such as, for example a silicon dioxide film.

【0042】

Next, as is shown in Figure 1(b), after using a lithographic process in order to form 1st resist pattern 107 that has opening portions for the formation of wiring grooves, dry etching is performed vis-à-vis the titanium nitride film 106, using this 1st resist pattern as a mask, and as is shown in Figure 1(c), mask pattern 108 is formed from the titanium nitride film 106.

【0043】

Next, after forming 2nd resist pattern 109 that has, without removing 1st resist pattern 107, openings for the formation of the wiring grooves due to the lithographic process, dry etching vis-à-vis 2nd organic, patterned 2nd organic film 105A on which are opening portions for the formation of the contact holes is formed. In this case, because 2nd organic film 105 and 1st resist pattern 107 and 2nd resist pattern 109 are such that their composition is mainly organic, the etching rate vis-à-vis 2nd organic film 105 and the etching rate vis-à-vis 1st and 2nd resist patterns 107 & 109 are approximately equal so that 1st resist pattern 107 & 2nd resist pattern 109 are removed with the dry etching vis-à-vis 2nd organic film 105.

【0044】

It should be noted that in the dry etching process vis-à-vis 2nd organic film 105, any residual 2nd resist pattern 109 is not a hindrance. The reason for this is that any residual 2nd resist pattern 109 is removed by the later performed process wherein patterned 2nd organic film 105 (please refer to Figure 2(c)).

【0045】

Next, silicon dioxide film 104, which contains organic component(s), is dry etched using 2nd organic film 105A as a mask; thus patterned silicon dioxide film 104A, which contains organic component(s) and which has openings for the formation of the contact holes as shown in Figure 2(b). In this process, it is possible by the selecting etching conditions such that that the silicon dioxide film 104, which contains organic component(s), is etched at a rate that is higher than that of the patterned 2nd organic film 105 to prevent the erroneous etching of patterned 2nd organic film 105A.

【0046】

Next, patterned 2nd organic film 105A is dry etched using mask pattern 108 as a mask so that, as shown in Figure 2(c), wiring grooves 111 in the patterned 2nd organic film, are formed; the 1st organic film 103 is also dry etched, using patterned silicon dioxide film 104A which contains organic component(s) as a mask so that, as shown in Figure 2(c), patterned 1st organic film 103A which has the contact holes is formed.

【0047】

Next, using as a mask patterned silicon dioxide film 104A which contains organic components, dry etching is performed vis-à-vis silicon nitride film 102, and as a result thereof, as shown in Figure 3(a), patterned silicon nitride film 102 is formed and the 1st metal wiring 101 within contact holes 110 is exposed.

【0048】

Next, as shown in Figure 3(b), adhesion layer 112, which is composed of titanium nitride, is deposited to a thickness of, for example, 50nm on the wall surfaces of contact holes 110 and wiring grooves 111. Then metal film 113 is deposited over the entire surface of the substrate in order to completely fill in contact holes 110 and wiring grooves 111. The metal for metal film 113 may be any metal such as copper, aluminum, gold, silver, nickel, cobalt, tungsten or any alloy thereof, and any deposition method such as plating, CVD or sputtering may be used for the deposition of metal film 113.

【0049】

Next, as shown in Figure 3(c), the respective portions of adhesive layer 112, metal film 113 and masking pattern 108, which are deposited on the patterned 2nd organic film 105A, are removed by a method such as the CMP method, and as result thereof, 2nd metal wiring 114 & contacts 115, which connect the 1st and 2nd metal wiring 101 & 113, are formed from metal film 113.

【0050】

It should be noted that it is possible to form a multi-level wiring structure by forming respective films, wiring and connects on 2nd metal wiring 114 through the same steps described in the above.

【0051】

In the 1st embodiment, the silicon dioxide film 104, which has an organic composition, is formed by a CVD process using reactive gases which are mainly composed of phenyltrimethoxy silane so that it [104] has a structure in which a phenyl group (organic) which is bonded to a silicon atom is introduced into the silicon dioxide. Thus this [104] may be processed using a conventional CVD oxide film and also, the relative dielectric constant [of 104] is low as that of conventional CVD oxide film. Therefore it [104] can adhere strongly to organic films, oxide films and metal films.

【0052】

Also, after the formation mask pattern 108 from titanium nitride film 106, 2nd resist pattern 109 is formed without removing 1st resist pattern 107, and 1st & 2nd resist patterns 107 & 109 are removed while 2nd organic film 105 is being dry etched; thus it is not necessary to ash and remove the 1st & 2nd resist patterns 107 & 109 using oxygen plasma, which is to say that it is possible to prevent 2nd organic film 105 from being damaged during the ashing and resist pattern removal. Thus, although 2nd organic film 105, which has a low relative dielectric capacitance, is used as an inter-level insulating, a standard resist application may be applied to this embodiment.

【0053】

Also, wiring grooves 111 are formed by dry etching patterned 2nd organic film [...]

[...] 105A whilst using mask pattern 108 as a mask and using patterned silicon dioxide film 104A, which contains organic components, as an etch stopper, so that the depth of wiring grooves 111 matches the thickness of the 2nd organic film 105; in other words, the depth of wiring grooves 111 can be defined by self-alignment.

【0054】

Below is an explanation of the problems caused by the misalignment of 2nd resist pattern 109 vis-à-vis 1st resist pattern 107, and the measures taken to resolve the said problems.

【0055】

First is a description with reference to Figures 4(a) through 4(c), Figures 5(a) through 5(c), and Figures 6(a) thorough 6(c) regarding the problems when 2nd resist pattern is misaligned.

【0056】

In the same manner as with the 1st embodiment, as is shown in Figure 4(a), silicon nitride film 102 is initially formed to be a thickness of, for example, 50nm and is formed on the 1st metal wiring 101 that is formed on semi-conductor substrate 100; thus 1st organic film 103, which is of a mainly organic composition, is formed to a thickness of, for example, 1µm on silicon nitride film 102.

【0057】

Next, silicon dioxide film 104, which is of a mainly organic composition, is formed to be of a thickness of, for example. 50nm on 1st organic film 103, after which 2nd organic film 105, which is of a mainly organic composition, is formed to be of a thickness of, for example, 400nm on the silicon dioxide film 104, which is of a mainly organic composition, and titanium nitride film 106 is formed to be of a thickness of, for example, 50nm on 2nd organic film 105.

【0058】

Next, as shown in Figure 4(b), 1st resist pattern 107, which has opening portions for the formation of wiring grooves, is formed on titanium nitride film 106, after which titanium nitride film 106 is dry etched using 1st resist pattern 107 as a mask; thus mask pattern 108 is formed from titanium nitride film 106.

【0059】

Next, as shown in Figure 5(a), 2nd organic film 105, [...]

[...] which has opening portions for the formation of contact holes, is formed on 2nd organic film 105 without removal of 1st resist pattern. In this case, a comparison of Figure 5(a) and Figure 1c will show that 2nd resist pattern 109 is misaligned vis-à-vis 1st resist pattern 107.

【0060】

Next, misaligned vis-à-vis the 1st resist pattern 10 organic film 105 is dry etched so as to form patterned 2nd organic film 105, which, as shown in Figure 5(b); as in the case of the 1st embodiment, since 2nd organic film 105 and 1st & 2nd resist patterns 107 & 109 are of mainly organic compositions, 1st and 2nd resist patterns 107 & 109 are simultaneously removed with the dry etching of 2nd organic film 105. In this case, since the 2nd resist pattern 109 is misaligned vis-à-vis 1st resist pattern 107, the diameters of the openings for the formation of the contact holes, which are provided in 2nd organic film 105A are smaller than desired.

【0061】

Next, as shown in Figure 5(c), silicon dioxide film 104, which is organic in composition, is dry etched using patterned 2nd organic film 105A as a mask; thus patterned silicon dioxide film 105A, which is organic in composition and which has opening portions for the formation of contact holes is formed.

【0062】

Next, as shown in Figure 6(a), patterned 2nd organic film 105A is dry etched using mask pattern 108 as a mask, thereby forming wiring grooves 111 in the patterned 2nd organic film 105A; simultaneously, 1st organic film 103 is also dry etched using patterned silicon dioxide film 104, which is of an organic composition, as a mask, thereby forming patterned 1st organic film 103A, which has contact holes 110. Then, as shown in Figure 6(a), silicon nitride film 102 is dry etched using patterned silicon dioxide film 104A, which is of an organic composition, as a mask, thereby forming patterned silicon nitride film 102A and exposing 1st metal wiring 101 within the contact holes 102

【0063】

Next, adhesion layer 112, which consists of titanium nitride, is deposited in a thickness of, for example, 50nm on the walls of contact holes 11- and wiring grooves 111; thereafter, a metal film is deposited over the entire surface of the substrate and the respective portions of adhesion layer 112, the metal film and mask pattern 108, which are deposited on patterned 2nd organic film 105A, are removed using a method such as, for example, the CMP method. As a result, 2nd metal wiring 114 is formed with certainty but since the diameter of contact holes 110 is smaller than is desired, contact holes 110 cannot be completely filled in with the metal film, and 1st and second metal wiring 101 and 112 cannot be connected to each other, thus resulting in contact failure.

【0064】

Below is an explanation, with reference to Figures 7(a) ~ 7(c) and Figures 8(a) through 8(c) as to the measures to be taken in order to resolve the problems caused by the misalignment of 2nd resist pattern 109.

【0065】

First, 2nd resist pattern 109, which has opening portions for the formation of contact holes, is formed through the same process steps with reference to Figure 4(a) through 4(c) and Figure 5(a) but in this case 2nd resist pattern 109 is also misaligned vis-à-vis 1st resist pattern 107 (please refer to Figure 5(a)).

【0066】

As shown in Figure 7(a), 1st resist pattern 107 and mask pattern 108 are dry etched using 2nd resist pattern 109 as a mask; in this way, the portions of 1st resist pattern 107 that do not overlap with the 2nd resist pattern are removed and each opening of mask pattern 108 is expanded so as to be equal to or larger than each opening for the formation of the wiring grooves or each opening for the formation of the contact holes. As a result, the pattern for the opening portions of the 2nd resist pattern for the formation of contact holes 109 can be transferred to 1st resist pattern 107 and mask pattern 108.

【0067】

Next, as shown in Figure 7(b), [...]

[...] 2nd organic film 105 is dry etched, thereby forming patterned 2nd organic film 105A which has opening portions for the formation of contact holes. In this case, since 2nd organic film 105 and 1st & 2nd resist pattern 107 & 109 are all of a mainly organic composition, 1st & 2nd resist patterns 107 & 109 are simultaneously removed by the dry etching of 2nd organic film 105.

【0068】

Next, silicon dioxide film 104, which is of an organic composition, is dry etched using patterned 2nd organic film 105A as a mask, and as in shown in Figure 7(c), patterned silicon dioxide film 104A, which is of an organic composition and which has the openings for the formation contact holes, is formed

【0069】

As described in the above, 2nd resist pattern 109 is misaligned vis-à-vis 1st resist pattern 107 but in this case, the pattern for the openings of the 2nd resist pattern for the formation of contact holes 109 has been successfully transferred to 1st resist pattern 107 and mask pattern 108 so that the diameter of the openings for the formation of the contact holes, which have been formed in patterned 2nd organic film 105A and patterned silicon dioxide film 104A, which is of an organic composition, is of a predetermined size.

【0070】

Next, patterned 2nd organic film 105 is dry etched using masking pattern 108 as a mask, thereby forming wiring grooves 111 in patterned 2nd organic film 105, and as shown in Figure 8(a), at the same time 1st organic film 103 is also dry etched using patterned silicon dioxide film 104A, which is of an organic composition, as a mask, thereby forming patterned 1st organic film 103A, which has contact holes 110.

Subsequently, silicon nitride film 102A is dry etched using patterned silicon dioxide film 104A, which is of an organic composition, as a mask, thereby, as shown in Figure 8(b), forming patterned silicon nitride film 102A and exposing metal wiring 101 within contact holes 110.

【0071】

Next, adhesion layer 112, which is made of titanium nitride is deposited in a thickness of, for example, 50nm onto the wall surfaces of contact holes 110 and wiring grooves 111, and thereafter a metal film is deposited over the entire surface of the substrate and the respective portions of adhesion layer 112, the metal film and masking pattern 108, which are deposited on patterned 2nd organic film 105A, are removed by means of a method such as, for example, the CMP method. As a result, as is shown in Figure 8c, 2nd metal wiring 114 and contacts 115 are formed out of titanium nitride film 112 and the metal film.

(2nd Embodiment)

Below is an explanation of the wiring structure formation method as relates to the 2nd embodiment, with Figure 9(a) ~ (c), Figure 10(a) ~ (c) and Figure 11 (a) ~ (c) used as reference.

【0072】

First, as is shown in Figure 9(a), silicon nitride film 202 is formed to a thickness of, for example, 50nm over metal wiring 201, which is formed on semi-conductor substrate 200. Then 1st organic film 203 (1st insulating film), which is of a mainly organic composition, is formed to a thickness of, for example, 50nm on the 1st organic film 203, and then 2nd organic film 205 (3rd insulating film), which is of a mainly organic composition, is formed to a thickness of, for example, 50nm on 2nd organic film 205.

【0073】

As for the deposition method for 1st & 2nd organic films 203 & 205, there are no specific limitations; for example, the deposition may be a CVD process wherein a reactive gas that is mainly composed of phenyltrimethoxy silane. Also, for 1st & 2nd organic films 203 & 205, hydrocarbon films or hydrocarbon films that contain fluorine that have been formed by plasma CVD, coating or thermal CVD may be used.

【0074】

Also, in regards to the deposition method for silicon dioxide film 204, which is of an organic composition, there are no specific limitations but the CVD method which [...]

[...] uses a reactive gas wherein of pheyltrimethoxy silane is a main ingredient is one method that comes to mind.

【0075】

Also, a thin film demonstrating high etch selectivity with respect to 1st & 2nd organic films 203 & 205 such as silicon dioxide film 204, which are films that can be etched at a sufficiently low rate may be used instead of titanium nitride film 206.

【0076】

Next, as shown in Figure 9(b), after 1st resist pattern 207, which has openings for the formation of the wiring grooves, is formed by a lithographic process on titanium nitride film 206, titanium nitride film 206 is dry etched using 1st resist pattern as a mask, thereby forming, as shown in Figure 9(c), mask pattern 208 out of titanium nitride film 206.

【0077】

Next, 2nd resist pattern 209, which has opening portions for the formation of the contact holes, is formed by a lithographic method without removing 1st resist pattern 207, and then, as shown in Figure 10(a), 2nd resist pattern 205 is dry etched, thereby forming patterned 2nd organic film, which has opening portions for the formation of the contact holes. In this case, since 2nd organic film 205 and 1st & 2nd resist patterns 207 & 209 are all mainly of an organic composition, 2nd organic film 205 is etched at a rate that is substantially equal to that of 1st & 2nd resist patterns 207 & 209; thus when 2nd organic film 205 is dry etched, 1st & 2nd resist patterns 207 & 209 are also removed at the same time.

【0078】

If there is the danger that 2nd resist pattern 209 may have been misaligned vis-à-vis 1st resist pattern 207, [...]

[...] then 1st resist pattern and mask pattern 208 should be dry etched using 2nd resist pattern 209 as a mask. In this way the parts of 1st resist pattern 207 that do not overlap with 2nd resist pattern 209 are removed and the openings of mask pattern 208 are expanded so as to be equal or larger than the openings for the formation of the wiring grooves & contact holes as described in the 1st embodiment.

【0079】

Next, silicon dioxide film 205A, which is of an organic composition, is dry etched using patterned 2nd organic film 205A as mask, thereby forming patterned silicon dioxide 204A, which has opening portions for the formation of the contact holes as shown in Figure 10(b). After that, patterned 2nd organic film 205A is dry etched using mask pattern 208 as a mask, thereby forming wiring grooves 211 in patterned 2nd organic film 205, and as shown in Figure 10(c), at the same time 1st organic film 203 is also dry etched, which has contact holes 210. etched using patterned silicon dioxide film 204 as a mask, thereby forming patterned 1st organic film 203A

【0080】

Next, silicon nitride film 202 is dry etched using patterned silicon dioxide film 204, which is of an organic composition, as a mask, thereby, as shown in Figure 11(a), forming patterned silicon nitride film 202A and exposing 1st metal wiring 201 within contact holes 210.

【0081】

Next, patterned 1st & 2nd organic films 203 and 205A are subjected to plasma processing wherein ammonium gas is used. As a result, as shown in Figure 11(b), adhesion layer 212, which includes amino groups and amide groups, is deposited on the wall surfaces of patterned 1st organic film 203 that is exposed inside contact holes 210 and on the wall surfaces of patterned 2nd organic film 205A, which is exposed inside wiring grooves 211. Thereafter, metal wiring 213 is deposited over the entire surface of the substrate to completely fill in contact holes 210 and wiring grooves 211. Metal film 213 may be of any metal; copper, aluminum, gold, silver, nickel, cobalt, tungsten or an alloy thereof may be used. Also, metal film 213 [...]

[...] may be deposited by any method, with plating, CVP and sputtering given as examples thereof.

【0082】

Next, as shown in Figure 11c, the respective portions of metal film 213 and mask pattern 208, which are deposited on the patterned 2nd organic film 205Am are removed by a method such as, for example, the CMP method, and as a result, 2nd metal wiring 214 and contacts 215 are formed out of metal fil 213.

【0083】

(3rd Embodiment)

Below is an explanation of the wiring structure formation method as relates to the 3rd embodiment, with Figure 12(a) ~ (c), Figure 13(a) ~ (c) and Figure 14(a) ~ (c) used as reference.

【0084】

First, as is shown in Figure 12(a), silicon nitride film 302 is formed over 1st metal wiring 301, which is formed over 1st metal wiring 301, which is formed on semi-conductor substrate 300, and silicon nitride film 302 is formed to a thickness of, for example, 50nm and is in order to protect 1st metal wiring 301 during subsequent etching processes; then 1st silicon dioxide film 302(1st insulating film), which is of an organic composition, is formed to a thickness of, for example, 1μm on silicon nitride film 302. Next, low dielectric constant SOG film 304 (2nd insulating film), which is of an organic composition, is deposited to a thickness of, for example, 400nm on 1st silicon dioxide film 303, which is of an organic composition; the 2nd silicon dioxide film (3rd insulating film) is formed to a thickness of, for example, 50 nm on low dielectric constant SOG film 304, and titanium nitride film 206isformed to a thickness of, for example, 50nm on 2nd m 305 silicon dioxide film, which is of an organic composition.

【0085】

Any method may be used to deposit 1st & 2nd silicon dioxide films 303 & 305; [...]

[...] for example, they may be deposited by a CVD process using a reactive gas that is mainly composed of phenylmethoxy silane. An HSQ film may be used with a low dielectric constant SOG film that has a siloxane skeleton.

【0086】

Next, a thin film demonstrating high etching selectivity with respect to 1st & 2nd silicon dioxide films 303 & 305, which are of an organic composition, and low dielectric constant SOG film 304, in other words a film that is etched at a sufficiently low rate such as silicon nitride film may be used instead of titanium nitride film 306.

【0087】

Next, as is shown in Figure 12(b), 1st resist pattern 307, which has opening portions for the formation of the wiring grooves, is formed by a lithographic process on titanium nitride film 306, after which, as is shown in Figure 12c, titanium nitride film 306 is dry etched using 1st resist pattern 306 as a mask, thereby forming mask pattern 308 out of titanium nitride film 306.

【0088】

Next, as is shown in Figure 13(a), 1st resist pattern 307 is removed and then 2nd resist pattern 309, which has opening portions for the formation of the contact holes, is formed on 2nd silicon dioxide film 305, which is of an organic composition. Then 2nd silicon dioxide film 305 and low dielectric constant SOG film 303 are sequentially dry etched using 2nd resist pattern as mask; as a result, as is shown in Figure 13(b), patterned low dielectrics constant SOG film 204A and patterned 1st silicon dioxide film 303A, which is of an organic composition and which has contact holes 310 are formed.

【0089】

Next, as shown in Figure 13(c), 2nd resist pattern 309 is removed and patterned 2nd silicon dioxide film 305A, which is of an organic composition, is dry etched using mask pattern 308 as a mask, [...]

[...] thereby forming the opening portions for the formation of the wiring grooves in patterned 2nd silicon dioxide film 305, and then patterned low dielectric constant SOG film 304A is dry etched using silicon dioxide film 305A, which has the opening portions for the formation of the wiring grooves, as a mask, thus forming wiring grooves 311. In forming wiring grooves 311, by selecting etching conditions such that 1st silicon dioxide film 303A is etched at rate sufficiently lower than that for low dielectric constant SOG film 304A, it is possible to secure sufficient selectivity for patterned silicon dioxide film 303A; thus the depth of wiring grooves 311 can be clearly determined at the sum of the thickness of 2nd silicon dioxide film 305, which is of an organic composition and low dielectric constant SOG film 304.

【0090】

If resist pattern 309 may have been misaligned vis-à-vis 1st resist pattern 307, mask pattern, it is desirable that prior to the dry etching of silicon dioxide film 305, which is of an organic composition, using 2nd resist pattern 309 as a mask, mask pattern 308 be dry etched using 2nd resist pattern 309 as a mask, which is to say that if mask pattern 308 is partially exposed inside the openings of 2nd resist pattern 309 in the forming of the contact holes on account of the misalignment of 2nd resist pattern 309 vis-à-vis 1st resist pattern 307, then mask pattern 308 is dry etched using 2nd resist pattern 309 as a mask. In this way, the openings of mask pattern 309 are expanded to include the openings for the formation of the wiring grooves and the contact holes.

【0091】

Next, nitride film 302 is dry etched using patterned 1st silicon dioxide film 303A, which is of an organic composition, as a mask thereby, as is shown in Figure 14(a), forming patterned silicon nitride film 302A and exposing 1st metal wiring 301 within the contact holes 310

【0092】

Next, as is shown in Figure 14(b), adhesion layer 312, [...]

[...] which is made of titanium nitride, is deposited so as to have a thickness of, for example, 50nm is on the wall surfaces of contact holes 310 and wiring grooves 311. Then metal film 313 is deposited over the entire surface of the substrate to completely fill n contact holes 310 and wiring grooves 311. There are no particular limitations as to the composition of metal film 313; for example, copper, aluminum, gold, silver, nickel, cobalt, tungsten or any alloy thereof may be used, and there are no particular limitations as to the method of deposition – for example, plating, CVD or sputtering may be used.

【0093】

Next, as is shown in Figure 14c, the respective portion of adhesion layer 312, metal film 313 and mask pattern 308, which are deposited on patterned 2nd silicon dioxide film 305, which is of an organic composition, are removed using a method such as, for example, the CMP method, and as a result, 2nd metal wiring 314 and contacts 315, which connect 1st & 2nd metal wirings 310 & 314 and contacts 315, thus connecting 1st & 2nd metal wirings 301 & 314, are made out of metal film 312.

【0094】

A multi-level wiring structure may be formed by forming the respective films, wirings, connects and contacts on 2nd metal wiring 314 by the same processes as described in the above.

【0095】

According to the 3rd embodiment, while 1st resist pattern 307 is ashed and removed with oxygen plasma, because 2nd silicon dioxide film 305, which is of an organic composition, is located on low dielectric constant SOG film 304, low dielectric constant SOG film 304 is not exposed to the oxygen plasma.

【0096】

Also, after 2nd silicon dioxide film 305, which is of an organic composition, low dielectric constant SOG film 304 and 1st silicon dioxide film 303, which is of an organic composition have been sequentially dry etched using 2nd resist pattern 309 as a mask, 2nd resist pattern 309 is ashed and removed with oxygen plasma so that the regions of patterned low dielectric constant SOG film 304A, which are exposed inside the openings for the formation of the contact holes, are damaged by the exposure to the oxygen plasma. However the damaged layer, which is formed in patterned low dielectric constant SOG film 304A, can be removed when wiring grooves 311 are formed in patterned low dielectric constant SOG film 304A so it is not harmful to the subsequent processes.

【0097】

Accordingly, low dielectric constant SOG film 304 may be made of a material that can deteriorate due to oxygen plasma. For example, in general, if an HSQ film is exposed to oxygen plasma, the Si-H bonds thereof are oxidized and the moisture content quantity and the relative dielectric constant thereof both increase and cause deterioration in the element reliability and performance but according to the 3rd embodiment, patterned low dielectric constant SOG film 304, in which wiring grooves 311 have already been formed, is not affected by oxygen plasma so that even if an HSQ film is used as an inter-level insulating film, the deterioration in element reliability and performance can be avoided.

(Variant Example of the 3rd Embodiment)

【0098】

First, as shown in Figure 15(a), silicon nitride film 352 is formed over 1st metal wiring 351, which is formed on semi-conductor substrate 350; silicon nitride film 352 is formed to a thickness of, for example, 50nm to protect the 1st metal wiring 351 during subsequent etching processes, and thereafter 1st silicon dioxide film 353 (1st insulating film) is formed to a thickness of, for example, 1μm on silicon nitride film 352. Next, organic film 354 (2nd insulating film) is deposited to a thickness of, for example, 400nm on 1st silicon dioxide film 353. Then 2nd silicon dioxide film 355 (3rd insulating film) is formed to a thickness of, for example, 50nm on organic film 354, after which titanium nitride film 356 is formed to a thickness of, for example, 50nm on 2nd silicon dioxide film.

【0099】

There are no specific restrictions as to the deposition method for 1st *2nd silicon dioxide films 353 & 355; for example CVD method wherein a reactive gas with a mostly organic composition composed of phenyltrimethoxy silane may be used.

【0100】

It should be noted that a thin film demonstrating a high etch selectivity vis-à-vis 1st & 2nd silicon dioxide films 353 & 355 and organic film, which is say [...]

[...] 355 and organic films that are etched at a sufficiently low rate such as silicon nitride films) may be used instead of titanium nitride film 356.

【0101】

Next, as is shown in Figure 15(b), 1st resist pattern 357, which has opening portions for the formation of the wiring grooves, is formed by a lithographic process on titanium nitride film 356, and thereafter, as is shown Figure 15(c), titanium nitride 356 is dry etched using 1st resist pattern 357 as a mask to form mask pattern 358 out of titanium nitride film 356.

【0102】

Next, as is shown in Figure 16(a), 1st resist pattern 357 is removed and then 2nd resist pattern 359, which has the opening portions for the formation of contact holes, is formed on 2nd silicon dioxide 355. Then 2nd silicon dioxide film 358 and organic film 354 are sequentially dry etched using 2nd resist pattern 359 as a mask, thereby forming patterned 2nd silicon dioxide film 355A and patterned organic film 354A, which has opening portions for the formation of contact holes as is shown in Figure 16(b). In this case, 2nd resist pattern 359 is removed during the etching of organic film 354.

【0103】

Next, as is shown in Figure 16(c), 1st silicon dioxide film 353 is dry etched using patterned 2nd silicon dioxide film 355A and patterned organic film 354 as a mask, thereby forming patterned 1st silicon dioxide film 353A, which has contact holes 361. In the etching process, mask pattern 358 is transferred to patterned 2nd silicon dioxide film 355A so that the opening portions for the formation of the wiring grooves are formed in patterned 2nd silicon dioxide film 355A.

【0104】

Next, as is shown in Figure 16(d), patterned organic film 354A is dry etched using mask pattern 358 and patterned 2nd silicon dioxide film 355A, which has the opening portions for the formation of the grooves, as a mask, thereby forming wiring grooves 362; in forming wiring grooves 362, [...]

[...] by selecting the etching conditions so that 1st silicon dioxide film 353A is etched at a rate that is sufficiently lower than that of organic film 354A, it is possible to achieve sufficient selectivity for patterned 1st silicon dioxide film 353A; thus the depth of wiring grooves 362 can clearly be determined at the sum of the thickness of 2nd silicon dioxide film 355 and organic film 354.

【0105】

If 2nd resist pattern 359 as a mask 359 may have been misaligned vis-à-vis 1st resist pattern 357, then it is desirable that before 2nd silicon dioxide film 355 is dry etched using 2nd resist pattern 359 as a mask, mask pattern 358 be dry etched using 2nd resist pattern 359 as a mask. That is to say, if mask pattern 358 is partially exposed inside the openings of 2nd resist pattern 359 that are for the formation of the contact holes on account of the misalignment of 2nd resist pattern 359 vis-à-vis the 1st resist pattern 357, then mask pattern 358 is dry etched using 2nd resist pattern 359 as a mask; in the way, the openings of mask pattern 358 are expanded so as to include the openings for the formation of the wiring grooves and contact holes.

【0106】

Next, silicon nitride film 352 is dry etched using patterned 1st silicon dioxide film 358A as a mask, thereby, as is shown in Figure 17(a), forming patterned silicon nitride film 352A and exposing 1st metal wiring 351 within contact holes 361.

【0107】

Next, as is shown in Figure 17(b), adhesion layer 363, which is made of titanium nitride, is deposited to a thickness of, for example, 50nm on the wall surfaces of contact holes 361 and wiring grooves 362, after which metal film 364 is deposited over the entire surface of the substrate so as to completely fill in contact holes 361 and wiring grooves 362. There are no specific limitations for the composition of metal film 364; for example, copper, aluminum, gold, silver, nickel, cobalt, tungsten or any alloy [...]

[..] thereof may be used. Also, there are no specific limitations as to the deposition method for metal film 364; for example, plating, CVD or sputtering may be used.

【0108】

Next, as is shown in figure 17c, the respective portions of adhesion layer 363, metal film 364 and mask pattern 358, which are deposited of patterned 2nd silicon dioxide film 355A, are removed by such as the CMP method, and as a result thereof, 2nd metal wiring 365 and contacts 366, which connect 1st & 2nd metal connects 351 & 365 are formed out of metal film 364.

【0109】

It should be noted that a thin film demonstrating high etch selectivity with respect to 2nd metal wiring 365 through the same process as those described above>

【0110】

According to the variant of the 3rd embodiment, while 1st resist pattern 357 is ashed and removed by oxygen plasma, organic film 354 is not exposed to the oxygen plasma because 2nd silicon dioxide film 355 is located on organic film 354.

【0111】

Also, 2nd resist pattern 359 is removed while 2nd silicon dioxide film 355 and organic film 354 are dry etched using 2nd resist pattern 359 as a mask, and thus since there is no need to ash and remove 2nd resist pattern 359 using oxygen plasma, organic film 354 is not exposed to oxygen plasma.

(4th Embodiment)

Below is an explanation of the wiring structure formation method as relates to the 3rd embodiment, with Figure 18(a) ~ (c), Figure 19(a) ~ (c) and Figure 20(a) ~ (c) used as reference.

【0112】

First, as is shown in Figure 18(a), silicon nitride film 402 is formed over 1st metal wiring on semi-conductor substrate 400 to be of a thickness of, for example, 50nm in order to protect [...]

[...] 1st metal wiring 401 during subsequent etching process, and thereafter, 1st low dielectric constant SOG film (1st insulating film), which has a siloxane skeleton, is formed to a thickness of, for example, 1 μ m on silicon nitride film 402, Next, silicon dioxide film 404 (2nd insulating film), which contains organic components in the silicon dioxide, is deposited to form a thickness of, for example, 50nm on 1st low dielectric constant SOG film 403, and then 2nd low dielectric constant SOG film 405 (3rd insulating film), which has a siloxane skeleton, is formed to a thickness of, for example, 400 nm on silicon dioxide film 404, which contains organic components, on 2nd low dielectric constant SOG film 405.

【0113】

It is possible for 1st & 2nd low dielectric constant SOG films 403 & 405 to HSQ films. There are no specific limitations on the deposition method for silicon dioxide film 404, which contains organic components; for example, it may be deposited by a CVD method wherein a reactive gas of mainly phenyltrimethoxy silane composition. Then silicon dioxide film 404, which has a structure wherein a phenyl group that is bonded to a silicon atom is introduced into the silicon dioxide, can be obtained.

【0114】

It should be noted that a thin film demonstrating high etch selectivity with respect to 1st & 2nd low dielectric constant SOG films 404 & 405 and silicon dioxide film 404, which contains organic components such as to make possible etching at a sufficient low rate (such as silicon nitride film), thus making it possible for it to be used instead of titanium nitride film 406.

【0115】

Next, as is shown in Figure 18(b), 1st resist pattern 407, which has opening portions for the formation of the wiring grooves, is formed by a lithographic process on titanium nitride film 406; thereafter titanium nitride film 406 is dry etched using 1st resist pattern 407 as a mask, thereby, as is shown in Figure 18(c), mask pattern 408 out of titanium nitride film 406.

【0116】

Next, 2nd resist pattern 409, which has opening portions for the formation of the contact holes, is formed by a lithographic process on 2nd low dielectric constant [...]

[...] SOG film 405 without removing 1st resist pattern 407, and then 2nd low dielectric constant SOG film 405 and silicon dioxide film 404, which contains organic components, are sequentially dry etched using 2nd resist pattern 49 as a mask, thereby, as is shown in Figure 19(a), forming patterned 2nd low dielectric constant SOG film 405A and patterned silicon dioxide film 404A.

【0117】

Next, 1st & 2nd resist patterns 407 & 409 are ashed and removed with oxygen plasma, as a result thereof, as is shown in Figure 19(b) damaged layer 410 is unintentionally formed in the respective portions of patterned 2nd low dielectric constant SOG film 405A and 1st low dielectric constant SOG film 403, which are exposed inside the opening portions for the formation of the contact holes.

【0118】

Next, patterned 2nd low dielectric constant SOG film 405A is dry etched using mask pattern 408 as a mask, thereby, as is shown in Figure 19(c), forming wiring grooves 412 in patterned 2nd low dielectric constant SOG film, whilst 1st low dielectric constant SOG film 403 is dry etched using patterned silicon dioxide film 404A as a mask, thereby, as is shown in Figure 19c, forming patterned 1st low dielectric constant SOG film 404A, which has contact holes 411. Damaged layer 410 is removed from patterned 2nd low dielectric constant SOG film by performing this dry etching process and 1st low dielectric constant SOG film 403.

【0119】

Next, silicon nitride film 402 is dry etched using patterned silicon dioxide film 402, which contains organic components, as a mask, thereby, as is shown in Figure 20(a), forming patterned silicon nitride film 402A and exposing 1st metal wiring 401 within contact holes 411.

【0120】

Next, as is shown in Figure 20(b), adhesion layer 413, which is made of titanium nitride, is deposited to a thickness of, for example, 50nm on the wall surfaces of [...]

[...] of contact holes 411 and wiring grooves 412; thereafter, metal film 414 is deposited over the entire surface of the substrate to completely fill in contact holes 411 and wiring grooves. There is no specific limitation on the metal composition for metal film 414; for example, copper, aluminum, gold, silver, nickel, cobalt, tungsten or an alloy thereof may be used, and also there are no specific limitations as to the deposition method for metal film 414; for example, it is possible to use plating, CVD or sputtering.

【0121】

Next, as is shown in Figure 20c, the respective portions of adhesion layer 413, metal film 414 and mask pattern 408, which are deposited on patterned 2nd low dielectric constant SOG film 405A, are removed by a method such as, for example, the CMP method, and as a result thereof, 2nd metal wiring 415 and contacts 417, which connect 1st & 2nd metal connects 401 & 415, are formed out of metal film 414.

【0122】

It should be noted that it is possible to form a multi-level wiring structure by forming the respective films, wirings and contacts on 2nd metal wiring 415 through the same processes as described above.

【0123】

According to the 4th embodiment, while 1st & 2nd resist patterns 407 & 409 are ashed and removed with oxygen plasma, damaged layer 410 is formed on 1st low dielectric constant SOG film 403 and patterned 2nd low dielectric constant SOG film 405A but it is possible to remove damaged layer 410 while contactholes 411 and wiring grooves 412 are formed.

【0124】

Accordingly, it is possible for 1st & 2nd low dielectric constant SOG films 403 & 405 to be of material that can be degraded by oxygen plasma. For example, if an HSQ film is exposed to oxygen plasma, the Si-H bonds thereof are oxidized and the moisture content and the relative dielectric constant thereof both increase so that there is element reliability and performance deterioration [...]

[...] but with the 4th embodiment, patterned 1st low dielectric constant SOG film 403A, wherein contact holes 411 have already been formed, and patterned 2nd low dielectric constant SOG film 405A, wherein wiring grooves 412 have already been formed, are no longer affected by the oxygen plasma so that even if an HSQ film is used as an inter-level insulating film, the deterioration in element reliability and performance can be avoided. (5th Embodiment)

Below is an explanation of the wiring structure formation method as relates to the 3rd embodiment, with Figure 21(a) ~ (c), Figure 22(a) ~ (c) and Figure 23(a) ~ (d) used as reference.

【0125】

First, as is shown in Figure 21(a), silicon nitride film 502 is formed on 1st metal wiring 501, which is formed on semi-conductor substrate 500 to a thickness of, for example, 50nm in order to protect the 1st metal wiring during subsequent etching; thereafter, 1st organic film 503 (1st insulating film), which is of a mainly organic composition, is deposited to a thickness of, for example, 400nm on silicon nitride film 502. Next, 1st silicon dioxide film 504 (2nd insulating film) is deposited to a thickness of, for example, 100nm on 1st organic film 503, and then 2nd organic film 505 (3rd insulating film), which is of a mainly organic composition, is deposited to a thickness of, for example, 300nm on this 1st silicon dioxide film 504. Next, 2nd silicon dioxide film 506 (4th insulating film) is deposited to a thickness of, for example, 200nm on 2nd organic film 505, and titanium nitride film (thin film) is deposited to a thickness of, for example, 50nm on 2nd silicon dioxide film 506.

【0126】

There are no specific limitations regarding the method by which 1st & 2nd organic films 503 & 505 may be deposited; for example, the deposition may be by plasma CVD process using a reactive gas that is mainly composed of perfluorodecalin. Also, hydrocarbon films and hydrocarbon films that contain fluorine and that are formed by plasma CVD, by coating or thermal CVD may be used as 1st & 2nd organic films 503 & 505. More specifically, organic films 503 and 505 may be made of polytetrafluoroethylene, polytetrafluoroethylene which contains oxygen, polyimide fluoride or polyaryl ether.

【0127】

There are no specific limitations as to the method with which 1st & 2nd silicon dioxide films 504 & 506 may be deposited; for example, the deposition may be by plasma CVD.

【0128】

It should be noted that a thin film demonstrating high etch selectivity with respect to 1st & 2nd organic films 503 & 505 and silicon dioxide film 504, in other words, a thin film that can be etched at sufficiently slow rate (such as silicon nitride film) may be used instead of titanium nitride film 506.

【0129】

Next, as is shown in Figure 21(b), 1st resist pattern 508, which has the opening portions for the formation of the wiring grooves, is formed by a lithographic process vis-à-vis titanium nitride film 507, and then titanium nitride film 507 is dry etched, using 1st resist pattern 508 as a mask, thereby forming, as is shown in Figure 21(c), mask pattern 509, which has opening portions for the formation of the wiring grooves, from titanium nitride film 507.

【0130】

Next, as is shown in Figure 22(a), 1st resist pattern 505, is removed by, for example, oxygen plasma. In this case, even if 1st resist pattern 508 is ashed and removed using oxygen plasma, the quality of 2nd organic film 505 is not degraded because 2nd silicon dioxide film 506 is located on 2nd silicon dioxide film 505, which is of mainly organic composition.

【0131】

Next, as is shown in Figure 22(b), 2nd resist pattern 510, which has the opening portions for the formation of the contact holes, is formed by a lithographic process on mask pattern 509, and thereafter, 2nd silicon dioxide film 506 is dry etched, using mask pattern 509 as a mask, thereby, as is shown in Figure 22(c), patterned 2nd silicon dioxide film 506A, which has the opening portions for the formation of the contact holes.

【0132】

I
Next, 2nd organic film 505 is dry etched using patterned 2nd silicon dioxide film 506A as a mask, thereby, as is shown in Figure 23(a), forming patterned 2nd silicon dioxide film 505A, which has the opening portions for the formation of contact holes. In this case, 2nd organic film 505 and 2nd resist pattern 505 [...]

[...] are both of mainly organic composition, and organic film 505 is etched at substantially the same rate as that of 2nd resist pattern 510 so that when 2nd organic film 505 is dry etched, 2nd resist pattern 510 is also removed at the same time. Patterned 2nd silicon dioxide film 506A functions as an etch stopper during the dry etching of 2nd resist pattern 510.

【0133】

It should be noted that it is not an issue if a portion of 2nd resist pattern 510 remain in the process of dry etching 2nd organic film 505. The reason for this is because it is possible to remove the residual 2nd resist pattern 510 during the subsequent process of dry etching 1st organic film 503 (please refer to Figure 23(c)).

【0134】

Next, patterned 2nd silicon dioxide film 506A and 1st silicon dioxide film 504 are dry etched using mask pattern 509 and patterned 2nd organic film 505A as the respective masks, thereby, as is shown in Figure 23(c), forming patterned 2nd silicon dioxide film 506B, which has the opening portions for the formation of the wiring grooves and patterned 1st silicon dioxide film 504, which has the opening portions for the formation of the contact holes.

【0135】

Next, patterned silicon dioxide film 504A and 1st organic film 503 are dry etched using mask pattern 509 and patterned 1st silicon dioxide film 504A as the respective masks, thereby, as is shown in Figure 23(c), patterned 1st organic film 503A, which has contact holes 512.

【0136】

Next, silicon nitride film 502 is dry etched using patterned 1st silicon dioxide film 504 as a mask, thereby forming patterned [...]

[...] silicon nitride film 502A (please refer to Figure 23(d)) and exposing 1st metal wiring 501 within the contact holes 512. Next, although this is not shown in the figures, in the same manner as in the 1st embodiment, an adhesion layer, which is made of titanium nitride, is deposited so as to have a thickness of, for example, 50 nm on the wall surfaces of contact holes 512 and wiring grooves 511, and then a metal film is deposited over the entire surface of the substrate in order to completely fill in contact holes 512 and wiring grooves 511. There are no specific limitations as to the metal composition of the metal film; for example, copper, aluminum, gold, silver, nickel, cobalt, tungsten or an alloy thereof may be used and also there are no specific limitations as to the manner of deposition; for instance, it is possible to use plating, CVD or sputtering. Next, the respective portions of the adhesion layer, the metal film and mask pattern 509, which are deposited on patterned 2nd silicon dioxide film 506B, are removed by a method such as the CMP method, and as is shown in Figure 26(d) and Figure 29(b), 2nd metal wiring 513 and contacts 514, which connect 1st & 2nd metal wirings 501 & 513, are formed.

【0137】

It should be noted that it is possible for a multi-level wiring structure to be formed by forming the respective films, wirings and contacts on 2nd metal wiring 513 through the same process as described above.

【0138】

According to the 5th embodiment, degradation of 2nd organic film 505, which is readily damaged by oxygen plasma, does in the course of the removal of 1st resist pattern 508 using oxygen plasma because 2nd silicon dioxide film is located on 2nd organic film 505,.

【0139】

Also, in the dry etching process vis-à-vis 2nd organic film 505, because 1st silicon dioxide film 504 functions as an etch stopper, it is possible to prevent degradation of the film quality of 1st organic film 503.

(Variant of the 5th Embodiment)

Below is an explanation of the wiring structure formation method as relates to the 3rd embodiment, with Figure 24(a) ~ (c), Figure 25(a) ~ (c), Figure 26(a) ~ (d), Figure 27(a), Figure 27(b), Figure 28(a), Figure 28(b), Figure 28(a) and Figure 29(b) are used as reference.

【0140】

First, as is shown in Figure 24(a), after silicon nitride film 552 is formed to a thickness of, for example, 50nm on semi-conductor substrate 551 in order to protect 1st metal wiring 551 during subsequent etching process; after that 1st organic film 553 (1st insulating film), which is of a mainly organic composition, is deposited to a thickness of, for example 400nm on silicon nitride film 552. Next, 1st silicon dioxide film 554 (2nd insulating film) is formed to a thickness of, for example, 100nm on 1st organic film 553, after which 2nd organic film 555 (3rd insulating film), which is of a mainly organic composing, is deposited to a thickness of, for example, 300nm on 1st silicon dioxide film 554. Next, 2nd silicon dioxide film 556 (4th insulating film) is deposited to a thickness of, for example, 200nm on 2nd organic film 555, and titanium nitride is deposited to a thickness of, for example, 50nm on 2nd silicon dioxide film 556.

【0141】

As for the deposition method for 1st & 2nd organic films 553 & 555 and 1st & 2nd silicon dioxide films 554 & 556, together with it being in the same as in the 5th embodiment, it is possible to use a thin film has high etching selectivity vis-à-vis 1st & 2nd organic films 553 & 555 and 1st & 2nd silicon dioxide films 554 & 556.

【0142】

Next, as is shown in Figure 24(b), 1st resist pattern 558, which has opening portions for the formation of the wiring grooves, is formed on titanium nitride film 557, and thereafter titanium nitride film 557 is dry etched using 1st resist pattern 558 as a mask, thus, as is shown in Figure 24(c), forming out of titanium nitride film 557 mask pattern 559, which has opening portions for the formation of wiring grooves.

【0143】

Next, as is shown in Figure 25(a) and Figure 27(a), after the removal of 1st resist pattern 558, 2nd resist patter 560, [...]

[...] which has opening portions for the formation of the control holes, is formed on mask 559. In that case, as a characteristic of the variant of the 5th embodiment, as is shown in Figure 25(b), the sizes of 2nd resist pattern 560's opening portions for the formation of the contact holes are set so as to be larger than the designed sizes of the contact holes in the respective vertical and parallel directions vis-à-vis the wiring holes for the formation of 2nd metal wiring. The reason(s) for this is/are described later.

【0144】

Next, 2nd silicon dioxide film 556 is dry etched using 2nd resist pattern 560 and mask pattern 559 as a mask, thereby, as is shown in Figure 25c and Figure 27(b), forming pattern 2nd silicon dioxide film 556A, which has the opening portions for the formation of the contact holes.

【0145】

As it has been described above, the sizes of the opening portions of 2nd resist pattern 560 for the formation of the contact holes are set so as to be larger than the designed sizes of the contact holes in the respective vertical and parallel directions vis-à-vis the wiring grooves for the formation of 2nd metal wiring, so that even if the opening portions of 2nd resist pattern 560, which is for the formation of the contact holes, are misaligned vis-à-vis the opening portions of mask pattern 559, which is for the formation of the wiring grooves, it is possible for the opening portions of patterned 2nd silicon dioxide film 556A, which is for the formation of the contact holes, to self-align vis-à-vis the opening portions of mask pattern 559, which is for the formation of the wiring grooves; this is because the opening portions of patterned 2nd silicon dioxide film 556A, which is for the formation of the contact holes in the respective regions where the opening portions of 2nd resist pattern 560, which are for the formation of the contact holes, overlap with the corresponding opening portions of mask pattern 559, which is for the formation of the wiring grooves.

【0146】

Also, the sizes of the opening portions of 2nd resist pattern 560, which are for the formation of the contact holes are extended in the direction that is parallel to the wiring grooves for the formation of the 2nd metal wiring so that the contact area between contacts 564, which are to be formed later, and 2nd metal wiring 563 (please refer to figure 26(d)) expands, and as a result thereof, it is possible for contacts 564 to connect with certainty 1st & 2nd metal wirings 551 & 563.

【0147】

Next, 2nd organic film 555 is dry etched using patterned 2nd silicon dioxide film 556A as a mask, thereby, as is shown in Figure 26(a) and Figure 28(a), forming patterned 2nd organic film 555A, which has opening portions for the formation of patterned 2nd organic film 555A, which has opening portions for the formation of the contact holes. [...]

[...] In this case, 2nd organic film 555 and 2nd resist pattern 560 are both of mainly organic composition, and 2nd organic film 555 is etched at a rate that is substantially equal to that of 2nd resist pattern 560 so that when 2nd organic film 555 is dry etched, 2nd resist pattern 560 is also removed at the same time. It should be noted that, in the process of dry etching 2nd organic film 555, residual 2nd resist pattern 560 does not pose an issue. This is because residual 2nd resist pattern 560 is removed during a subsequent dry etching process vis-à-vis 1st organic film 553 (please refer to Figure 26(c)).

【0148】

Next, patterned 2nd organic film 556A and 1st silicon dioxide film 554 are dry etched using mask pattern 559 and patterned 2nd organic film 55A as respective masks, thereby, as is shown in Figure 26(b) and Figure 28(b), forming patterned 2nd silicon dioxide film 556B which has the wiring grooves, and patterned 1st silicon dioxide film 554A, which has the opening portions for the formation of the contact holes.

【0149】

Next, patterned 2nd organic film 555A is dry etched using mask pattern 559 and 2nd patterned silicon dioxide film 556A as a mask, and 1st organic film 553 is dry etched using patterned 1st silicon dioxide film 556A as a mask, thereby, as is shown in Figure 26(c) and Figure 29(a), forming patterned 2nd organic film 555B, which has wiring grooves 561, and patterned 1st organic film 553A, which has contact holes 562.

【0150】

Next, silicon nitride film 552 is dry etched using patterned 1st silicon dioxide film 554 as a mask, thereby forming patterned silicon nitride film 552A, which has contact holes (please refer to Figure 26(d)), [...]

[...] and exposing 1st metal wiring 551 within contact holes 562. Next, although this is not shown in the figures, in the same manner as in the 1st embodiment, an adhesion layer, which is made of titanium nitride, is deposited so as to have a thickness of, for example, 50 nm on the wall surfaces of contact holes 562 and wiring grooves 561, and then a metal film is deposited over the entire surface of the substrate in order to completely fill in contact holes 562 and wiring grooves 561, after which the respective portions of the adhesion layer, the metal film and mask pattern 559, which are deposited on patterned 2nd silicon dioxide film 556B, are removed by a method such as the CMP method, and as is shown in Figure 26(d) and Figure 29(b), 2nd metal wiring 563 and contacts 564, which connect 1st & 2nd metal wirings 551 & 563, are formed.

【0151】

It should be noted that it is possible to form a multi-level wiring structure by forming the respective films, wirings and contacts on 2nd metal wiring 563 through the same processes as described above.

【0152】

According to the variant of the 5th embodiment, the dimensions of 2nd resist pattern 560's opening portions for the formation of the contact holes are set so as to be larger in the respective vertical and parallel directions vis-à-vis the wiring grooves for the formation of 2nd metal wirings than the designed dimensions for the of the contact holes so that even if the opening portions of 2nd resist pattern 560, which are for the formation of the contact holes, are misaligned vis-à-vis mask pattern 559's opening portions for the formation of the wiring grooves, the patterned 2nd silicon dioxide film 556A's opening portions for the formation of the contact holes can be formed so as to self-align vis-à-vis the mask pattern 559's opening portions for the formation of the wiring grooves because the patterned 2nd silicon film 556A's opening portions for the formation of the contact holes are formed with the respective regions where 2nd resist pattern 560's opening portions for the formation of the contact holes overlap with the corresponding mask pattern 559's opening portions for the formation of the wiring grooves. Accordingly, the connection between contact 564 and 2nd metal wiring 563 is obtained with certainty.

【0153】

Also, the dimensions of 2nd resist pattern 560's opening portions for the formation of the contact holes are extended in the direction that is parallel vis-à-vis the wiring grooves that are the formation of 2nd metal wiring 563 so that the contact area(s) between contact 564 and 2nd metal wiring 563 [...]

[...] expands so that it is possible for contacts 564 to connect with certainty 1st & 2nd metal wirings 551 & 563.

【0154】

Figure 36 illustrates what is, in the variant of the 5th embodiment, the positional relationship between mask pattern's 559's opening portions for the formation of the grooves and 2nd resist pattern 569's opening portions for the formation of the contact holes; as can be learned from Figure 36, the dimensions of 2nd resist pattern 560's opening portions for the formation of the contact holes are larger than those of the designed dimensions.

【0155】

Figure 37(a) illustrates what is, in the variant of the 5th embodiment, the respective positional relationship between mask pattern 559 and 2nd resist pattern 560, and between 1st metal wiring 551 and contacts 564. The upper portion of Figure 37(a) illustrates the positional relationship between mask pattern 559's opening portions for the formation of the wiring grooves and 2nd resist pattern 560's associated opening portions for the formation of the contact holes, and the middle portion of Figure 37(a) illustrates a cross sectional view of the upper portion when it is taken along the line A-A. and the lower portion of Figure 37(a) illustrates the positional relationship between 1st metal wiring 551 and contact 564 that is associated therewith, and Figure 37(b) illustrates what is, in the variant of the 5th embodiment, in the upper portion of Figure 37(b) the respective positional relationships between mask pattern 509's opening portions for the formation of wiring grooves and 2nd resist pattern 510's associated openings for the formation of contact holes, and the middle portion of Figure 37(b) illustrates a cross section of the upper portion taken along line B-B, and the lower portion of Figure 37(b) illustrates the positional relationship between 1st metal wiring 501 and associated contact 514.

【0156】

According to the 5th embodiment, in establishing the dimensions of 2nd resist pattern 510's opening portions for the formation of the contact holes at the designed dimensions, if the 2nd resist pattern 510's opening portion for the formation of contact holes have been misaligned vis-à-vis mask pattern 509's opening portions for the formation of the wiring grooves, then, as is shown in Figure 37(b), the contact areas (which are indicated by hatching) between contacts 514 and 1st metal wiring 501 greatly decreases. In contrast, establishing the dimensions of 2nd resist pattern 560's opening portions for the forming of contacts holes so that they are larger than those of the design dimensions thereof as in the variant of the 5th embodiment, even if 2nd resist pattern 560's opening portions for the formation of the contact holes has been misaligned vis-à-vis mask pattern 559's associated opening portions for the formation of wiring grooves, [...]

[...] the contact areas (which are indicated by hatching) between contacts 564 and 1st metal wiring 551 does not decrease by much.

(6th Embodiment)

Below is an explanation of the wiring structure formation method as relates to the 6rd embodiment, with Figure 30(a) ~ (c), Figure 31(a) ~ (c) and Figure 32(a) ~ (c) used as reference.

【0157】

First, as is shown in Figure 30(a), silicon nitride film 602 is formed over 1st metal wiring 601, which is formed on semi-conductor substrate 600; silicon nitride film 602 is formed to a thickness of, for example, 50nm so as to protect the 1st metal wiring during subsequent etching; then 1st organic film 603 (1st insulating film) which is mainly of a organic composition) is deposited at a thickness of, for example, 400nm on silicon nitride film 602. Then silicon dioxide film 604 (2nd insulating film), which is of a mainly organic composition) at a thickness of, for example, 100nm on 1st organic film 603. And then 2nd organic film 605 (3rd insulating film), which is of a mainly organic composition, is deposited at a thickness of, for example, 300nm on silicon dioxide film 604. Titanium nitride film 606 is deposited at a thickness of, for example, 50nm, on 2nd organic film 605.

【0158】

There are no specific limitations regarding the method by which 1st & 2nd organic films 603 & 605 may be deposited; for example, the deposition may be by plasma CVD process using a reactive gas that is mainly composed of perfluorodecalin. Also, hydrocarbon films and hydrocarbon films that contain fluorine and that are formed by plasma CVD, by coating or thermal CVD may be used as 1st & 2nd organic films 603 & 605. More specifically, organic films 603 and 605 may be made of polytetrafluoroethylene, polytetrafluoroethylene which contains oxygen, polyimide fluoride or polyaryl ether.

【0159】

There are no specific limitations as to the method with which silicon dioxide film 604 may also be deposited; for example, the deposition may be by plasma CVD.

【0160】

It should be noted that a thin film demonstrating high etch selectivity with respect to 1st & 2nd organic films 603 & 605 and silicon dioxide film 604, in other words, a thin film that can be etched at sufficiently slow rate (such as silicon nitride film) may be used instead of titanium nitride film 606.

【0161】

Next, as is shown in Figure 30(b), 1st resist pattern 607, which has the opening portions for the formation of the wiring grooves, is formed by a lithographic process vis-à-vis titanium nitride film 606, and then titanium nitride film 606 is dry etched, using 1st resist pattern 607 as a mask, thereby forming, as is shown in Figure 30(c), mask pattern 608, which has opening portions for the formation of the wiring grooves, from titanium nitride film 606.

【0162】

Next, as is shown in Figure 31(a), 1st resist pattern 607 is removed using, for example, an organic remover solution. In this way, since 2nd organic film 605 is not exposed to the oxygen plasma, degradation of the quality of 2nd organic film 605 does not occur.

【0163】

Next, as is shown in Figure 31(b), 2nd resist pattern 609, which has the opening portions for the formation of the contact holes, is formed by a lithographic process vis-à-vis mask pattern 609, after which 2nd organic film 605 is dry etched using 2nd resist pattern 609 and mask pattern 608 as a mask, thereby forming, as is shown in Figure 31(c), patterned organic film 605A, which has the opening portions for the formation of the contact holes. In this case, 2nd organic film 605 and 2nd resist pattern 609 are both mainly of organic composition, and 2nd organic film 605 is etched at a substantially equal rate vis-à-vis that of 2nd resist pattern 609 so that when 2nd organic film 605 is etched, 2nd resist pattern 609 is also simultaneously removed.

【0164】

It should be noted that part of 2nd resist pattern may remain in the dry etching process of 2nd organic film 605. The reason for this is that residual 2nd resist pattern 609 can be removed during a subsequent process of dry etching 1st organic film 603 (please refer to Figure 32(b)).

【0165】

Next, silicon dioxide film 604 is dry etched using patterned 2nd organic film 605A as a mask, thereby, as shown in Figure 32(a), forming patterned silicon dioxide film 604A, which has opening portions for the formation of contact holes.

【0166】

Next, patterned 2nd organic film 605A and 1st organic film 603 are dry etched using mask pattern 608 and patterned silicon dioxide film 604A as the respective masks, thereby forming, as is shown in Figure 32(b), patterned 2nd organic film 605A, which has wiring grooves 610 and patterned 1st organic film 603A which has contact holes 611.

【0167】

Next, patterned silicon dioxide film 604A and silicon nitride film 602 are dry etched using mask pattern 608 and patterned 1st organic film 603A as the respective masks, thereby forming patterned silicon dioxide film 604B, which has the wiring grooves (please refer to Figure 32(c)) and patterned silicon nitride film 602A, which has the contact holes (please refer Figure 32(c)), and exposing 1st metal wiring 601 within contact holes 611. Next, although this is not reflected in the figures, after an adhesion layer, which is made of titanium nitride, is deposited so as to have a thickness of, for example, 50nm on the wall surfaces of contact holes 611 and wiring grooves 610 in the same manner as in the 1st embodiment. Next, a metal film is deposited over the entire surface of the substrate so as to completely fill in contact holes 611 and wiring grooves 610. There are no specific limitations as to the composition of the metal film; for example, copper, aluminum, gold, silver, nickel, cobalt, tungsten or an alloy thereof may be used, and there are also no specific limitations on the deposition method for the metal films; for example, plating, CVD or sputtering may be used. Next, the respective portions of the adhesion layer, the metal film and mask pattern 608 are removed using, for example a CMP method, and as is shown in Figure 32(c), 2nd metal wiring 612, contacts 613, and the connections for 1st & 2nd metal wiring 601 [...]

[...] & 612 are formed.

【0168】

It should be noted that it is possible to form a multi-level wiring structure by forming respective films, wiring and connects on 2nd metal wiring 612 through the same steps described in the above.

【0169】

According to the 6th embodiment, the dry etching is performed using patter mask 608, which has the opening portions for the formation of the wiring grooves wiring grooves, and together with forming patterned 2nd organic film 605B, dry etching is performed using patterned silicon dioxide film 604A as a mask to form patterned 2st organic film 603A, which has contact holes 611; this to say because it is possible to form both wiring grooves 610 and contact holes 611 with the same etching process, the number of processes is controlled and dual damascene structures can be formed.

【0170】

According to the 6th embodiment, because for the removal of 1st resist pattern 607 what is used is, for example, an organic remover solution, no degradation in the film quality of 2nd organic film 605 occurs.

【0171】

Also, in the dry etching process of 2nd organic film 605, because silicon dioxide film 604 functions as an etching stopper, it is possible to prevent deterioration in the condition of 1st organic film 603 from occurring.
(Variant Example of the 6th Embodiment)

Below is an explanation of the wiring structure formation method as relates to the 6rd embodiment, with Figure 33(a) ~ (c), Figure 34(a) ~ (c) and Figure 35(a) ~ (c) used as reference.

【0172】

First, as is shown in Figure 33(a), silicon nitride film 652 is formed on 1st metal wiring 651, which is formed semi-conductor substrate 650, to a thickness of, for example, 50nm in order to protect 1st metal wiring 651 during subsequent etching process; thereafter, 1st organic film 653 (1st insulating film), which has a mainly organic composition, is formed to a thickness of, for example, 400nm on [...]

[...] this silicon dioxide film 652, and then silicon dioxide film 654 (2nd insulating film) is formed to a thickness of, for example, 100nm on 1st organic film 653. Next 2nd organic film 655 (3rd insulating film), which is of mainly organic composition, is formed to a thickness of, for example, 300nm over silicon dioxide film 154. Next, titanium nitride film 656 (thin film) is formed to a thickness of, for example, 50nm on 2nd organic film 155.

【0173】

There are no specific limitations regarding the method by which 1st & 2nd organic films 653 & 655 may be deposited; for example, the deposition may by plasma CVD process using a reactive gas that is mainly composed of perfluorodecalin. Also, hydrocarbon films and hydrocarbon films that contain fluorine and that are formed by plasma CVD, by coating or thermal CVD may be used as 1st & 2nd organic films 603 & 605, and specifically, 1st & 2nd organic films 653 & 655 may be made of polytetrafluoroethylene, polytetrafluoroethylene which contains oxygen, polyimide fluoride or polyaryl ether.

【0174】

There are no specific limitations regarding the deposition method for silicon dioxide film 654; for example, film 654 may be deposited by a plasma CVD method.

【0175】

It should be noted that a thin film demonstrating high etch selectivity with respect to 1st & 2nd organic films 653 & 655 and silicon dioxide film 654, which are films that can be etched at a sufficiently low rate, may be used instead of titanium nitride film 206.

【0176】

Next, as is shown in Figure 30(b), 1st resist pattern 657, which has the opening portions for the formation of the wiring grooves, is formed by a lithographic process vis-à-vis titanium nitride film 656, and then titanium nitride film 656 is dry etched, using 1st resist pattern 657 as a mask, thereby forming, as is shown in Figure 33(c), mask pattern 658, which has opening portions for the formation of the wiring grooves, from titanium nitride film 656.

【0177】

Next, as is shown in Figure 34(a), 1st resist pattern 657 is removed using, for example, an organic remover solution. In this way, since 2nd organic film 655 is not exposed to the oxygen plasma, degradation of the quality of 2nd organic film 605 does not occur.

【0178】

Next, as is shown in Figure 34(b), 2nd resist pattern 659, which has the opening portions for the formation of the contact holes, is formed by a lithographic process vis-à-vis mask pattern 659. In this variant of the 6th embodiment, the dimensions of 2nd resist pattern 659's opening portions for the formation of the contact holes are set to be larger than the dimensions of the contact holes in the respective vertical and parallel directions to the wiring grooves for the formation of the 2nd metal wiring. The reason(s) thereof will be described later.

【0179】

Next, 2nd organic film 655 is dry etched using 2nd resist pattern 659 and mask pattern 658 as a mask, thereby, as is shown in Figure 34(c). In this case, 2nd organic film 655 and 2nd resist pattern 659 are both of mainly organic composition; forming patterned 2nd organic film 655A, which has the wiring grooves (please refer to Figure 32(c)) and patterned silicon nitride film 602A, which has the contact holes (please refer Figure 32(c)), and exposing 1st metal wiring 601 within contact holes 611. Next, although this is not reflected in the figures, after 2nd organic film 655 is etched at a rate that is substantially equal to that of 2nd resist pattern 659 so that when 2nd organic film 655 is dry etched, 2nd resist pattern 659 is also removed at the same time. It should be noted that there may be left some residual 2nd resist pattern 659 but this is not an issue. This is because the residual 2nd resist pattern 659 can be removed during a subsequent of dry etching 1st organic film 653 (please refer to Figure 35(b)).

【0180】

Next, silicon dioxide film 654 is dry etched using patterned 2nd organic film 655Q as a mask, thereby, as is shown in Figure 35(b), forming patterned 2nd organic film 655B, which has wiring grooves 660, and patterned 1st organic film 653, which has contact holes 661.

【0181】

Next, patterned 2nd organic film 655A and 1st organic film 653 are dry etched using mask pattern 658 and patterned silicon dioxide film 654A as respective masks, thereby, as is shown in Figure 35(b), forming patterned 2nd organic 655B, which has wiring grooves 660, and patterned 1st organic film 653, which has contact holes 661.

【0182】

Next, patterned silicon dioxide film 654A and silicon nitride film 652 are dry etched using mask pattern 658 and patterned 1st organic film 653A as the respective masks, thereby forming patterned silicon dioxide film 654B, which has the wiring grooves (please refer to Figure 35(c)) and patterned silicon nitride film 652A, which has the contact holes (please refer to Figure 35(c)), and exposing 1st metal wiring 651 within contact holes 661. Next, although this is not shown in the figures, as in the 1st embodiment, an adhesion layer that is made of titanium nitride is deposited to a thickness of, for example, 50nm on the wall surfaces of contact holes 661 and wiring grooves 660. In this embodiment, there are no specific limitations as to the metal composition of the metal film; for example, it is possible to use copper, aluminum, gold, silver, nickel, cobalt, tungsten or any alloy thereof, and also, there are no limitations as to the deposition method; for example, it is possible to use plating, CVD or sputtering. Next, the respective portions of the adhesion layer, the metal film and mask pattern 658, which are deposited on patterned 2nd organic film 655B, are removed by a method such as the CMP method, and as a result thereof, as is shown in Figure 35(c), 2nd metal wiring 662 and contacts 663, which connect 1st & 2nd metal wirings 651 & 662 are formed.

【0183】

It should be noted that it is possible to form a multi-level wiring structure by forming the respective films, wirings and contacts of 2nd metal wiring 662 through the same process as described above

【0184】

According to the variant of the 6th embodiment, the dimensions of 2nd resist pattern 659's opening portions for the formation of the contact holes are set to be larger than the design dimensions of the contact holes in the respective vertical and parallel direction vis-à-vis the wiring grooves for forming 2nd metal wiring, and accordingly, even if 2nd resist pattern 659's opening portions for the formation of the contact holes are misaligned vis-à-vis mask pattern 658's opening portions for the formation of the wiring grooves, patterned 2nd organic film 655A's opening portions for the formation of the contact holes can be formed so as to be self-aligning vis-à-vis the mask pattern 658's opening portions for the formation of the wiring grooves because patterned 2nd organic film 655A's opening portions for the formation of the contact holes are formed in the respective regions where 2nd resist pattern 659's opening portions for the formation of the contact holes overlap with mask pattern 658's corresponding opening portions for the formation of the wiring grooves so that there is certainty as to the connections between contact 663 and 2nd metal wiring 662.

【0185】

Also, the dimensions of 2nd resist pattern 659's opening portions for the formation of the contact holes is also extended in the direction that is parallel to the wiring grooves for the formation of 2nd metal wiring so that contacts 663 and 1st & 2nd metal wiring 651 & 662 are certain.

【0186】

【Effects of the Invention】

According to the 1st method for the formation of the wiring structure, the ashing process for removal that uses oxygen plasma on the 1st resist pattern and the 2nd resist pattern becomes unnecessary so that it becomes possible to avoid the damage that can occur to 3rd insulating film in the removal of the resist pattern by ashing; thus, although the 3rd insulating film is damaged by the oxygen plasma, it is possible to use an insulating film of low specific inductive capacity, thus making it possible to form inter-level film of low specific inductive capacity whilst using a conventional resist process.

【0187】

Also, in the course of forming the wiring grooves by performing dry etching whilst using the mask pattern as a mask vis-à-vis the 3rd insulating film, because the 2nd insulating film can function as [...]

[...] an etching stopper, it is possible to coordinate the depth of the wiring grooves to match the film thickness of the 3rd insulating film, which permits self-alignment of the depth of the wiring grooves.

【0188】

When the 1st method for the formation of wiring structure is equipped with a process between Process 10 and Process 11 for the formation of an adhesion layer that is made of a metal film in the portions of the wiring contact holes in grooves in the 3rd insulating film that are exposed and in the portions of the contact holes in 1st insulating film that are exposed, it is possible to achieve adhesion between the upper-level metal wiring and the 3rd insulating film.

【0189】

When in the 1st method for the formation of wiring structure the 3rd insulating film is mainly of an organic composition, in Process 8, it is possible to achieve with certainty etching conditions such that the etching rates of the etching vis-à-vis the 3rd insulating film, the 1st resist pattern and the 2nd resist pattern is high whilst the etching rate of the etching vis-à-vis the 2nd insulating film is low.

【0190】

In this case, if a process the 3rd insulating film is formed using a CVD method wherein perfluorodecalin is contained within the reactive gases, it is possible to form with certainty a 3rd insulating film which is mainly organic in composition whilst having low specific inductive capacity.

【0191】

Also, in this case, if the 1st insulating film is one that is mainly organic in composition, in Process 9, it is possible to achieve with certainty etching conditions wherein the etching rate of the etching that is performed vis-à-vis the 2nd insulation film is high whilst the etching rate of the etching that is performed vis-à-vis the 3rd insulating film is low; together with this, in Process 10 it is also possible with certainty to achieve etching conditions wherein the etching rate of the etching that is performed vis-à-vis the 1st insulating film and the 3rd insulating film whilst the etching rate of the etching that is performed vis-à-vis the mask pattern and the 2nd insulating film is low.

【0192】

In the case that the 1st insulating film and the 2nd insulating film are mainly organic in composition, if a process whereby an adhesion layer is formed by plasma processing that uses reactive gases that contain nitrogen is equipped between Process 10 and Process 11 for the exposed portions of the wiring grooves of the 3rd insulating film and the exposed portions of the contact holes of the 1st insulating film, it is [...]

[...] possible to achieve with certainty adhesion of the upper-level metal wiring with the 1st insulating film that is mainly organic in composition & the 3rd insulating film.

【0193】

In the case that the 1st insulating film is mainly organic in composition, when Process 1 includes a CVD method that includes the use of reactive gases that contain perfluorodecalin, it is possible to form with certainty the 1st insulating film such that it is mainly organic in composition whilst also having low specific inductive capacity.

【0194】

According to the 2nd method for the formation of wiring structure, when in Process 10 the 1st resist pattern & the 2nd resist patterns are being removed, even if a damaged layer is formed in the opening portions for the formation of the contact holes in the 1st resist pattern and the 2nd resist pattern, because such this damaged layer will be certain to be removed in the course of Process 11, it is possible to use for purposes of the 1st & 3rd insulating films insulating films of low dielectric capacitance even though damage from the oxygen plasma will be sustained, thus making it possible to use a standard resist process whilst forming inter-level insulating films of low dielectric capacity.

【0195】

In the 2nd method for the formation of the wiring structure, if the 3rd insulating film is a low dielectric capacitance SOG that has a siloxane skeleton, it possible to use a standard resist process whilst forming inter-level insulating films of low dielectric capacitance.

【0196】

According to the 3rd method for the formation of the wiring structure, in the course of removal of the 1st resist pattern, the 4th insulating film is located on the 3rd insulating film, so that even if the 1st resist pattern is removed by the oxygen plasma, the 3rd insulating film will not be damaged, and in Process 10, when the dry etching is performed vis-à-vis the 3rd insulating film the 2nd insulating film is located on the 1st insulating film so that the 1st insulating film is not damaged; thus for purposes of the 1st insulating film and the 3rd insulating film, although damage from the oxygen plasma or the dry etching is sustained, it is possible to use standard resist processing whilst forming low dielectric capacitance inter-level films.

【0197】

With the 3rd method for the formation of the wiring structure, if at least 1 of the 1st insulating film and the 3rd insulating film is mainly of organic composition, it is possible to have low dielectric capacitance in the inter-level insulating films.

【0198】

With the 3rd method for the formation of the wiring structure, if the dimensions of the opening portions for the formation of the contact holes of the 2nd resist pattern are larger in the vertical direction vis-à-vis the direction in which the upper level of the metal wiring extends, even if the positioning of the opening portions for the formation of the contact holes of the 2nd resist pattern vis-à-vis the opening portions for the formation of the wiring of the mask pattern, the opening portions for the formation of the contact holes of the mask pattern will overlap the opening portions for the formation of the contact holes of the 2nd resist pattern and the opening portions for the formation of the wiring of the mask pattern so that the opening portions for the formation of the contact holes of the 4th insulating film will self-adjust to form in the region of the opening portions for the formation of the wiring of the mask pattern. Thus it is possible to achieve with certainty the connection the contact and the upper level of the metal wiring.

【0199】

With the 4th method for the formation of the wiring structure, in Process 8, in the course of performing the dry etching vis-à-vis the 3rd insulating film, the 2nd insulating film is located on the 1st insulating film and the 1st insulating will not sustain damage so for the 1st insulating film it is possible to use insulating film of low dielectric capacitance even though damage from the dry etching will be sustained, and thus it is possible to use a standard resist process whilst forming inter-level insulation films of low dielectric capacitance.

【0200】

With the 4th method for the formation of the wiring structure, if at least 1 of the 1st insulating film and the 3rd insulating film is mainly of organic composition, it is possible to have low dielectric capacitance in the inter-level insulating films.

【0201】

With the 4th method for the formulation of the wiring structure, if the dimensions of the opening portions for the formation of the contact holes of the 2nd resist pattern are larger in the vertical direction vis-à-vis the direction in which the upper level of the metal wiring extends, [...]

[...] even if the positioning of the opening portions for the formation of the contact holes of the 2nd resist pattern vis-à-vis the opening portions for the formation of the wiring of the mask pattern, the opening portions for the formation of the contact holes of the mask pattern will overlap the opening portions for the formation of the contact holes of the 2nd resist pattern and the opening portions for the formation of the wiring of the mask pattern so that the opening portions for the formation of the contact holes of the 4th insulating film will self-adjust to form in the region of the opening portions for the formation of the wiring of the mask pattern. Thus it is possible to achieve with certainty the connection the contact and the upper level of the metal wiring.

【Simple Explanation of the Figures】

【Figure 1】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 1st embodiment of the present invention.

【Figure 2】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 1st embodiment of the present invention.

【Figure 3】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 1st embodiment of the present invention.

【Figure 4】

(a) ~ (c) are cross-sectional diagrams that explain the problematic points when the 2nd resist patterns causes misalignment in the formulation method of the wiring structure that relates to the 1st embodiment of the present invention.

【Figure 5】

(a) ~ (c) are cross-sectional diagrams that explain the problematic points when the 2nd resist patterns causes misalignment in the formulation method of the wiring structure that relates to the 1st embodiment of the present invention.

【Figure 6】

(a) ~ (c) are cross-sectional diagrams that explain the problematic points when the 2nd resist patterns causes misalignment in the formulation method of the wiring structure that relates to the 1st embodiment [...]

[...] of the present invention.

【Figure 7】

(a) ~ (c) are cross-sectional diagrams that explain the problematic points when the 2nd resist patterns causes misalignment in the formulation method of the wiring structure that relates to the 1st embodiment of the present invention.

【Figure 8】

(a) ~ (c) are cross-sectional diagrams that explain the problematic points when the 2nd resist patterns causes misalignment in the formulation method of the wiring structure that relates to the 1st embodiment of the present invention.

【Figure 9】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 2nd embodiment of the present invention.

【Figure 10】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 2nd embodiment of the present invention.

【Figure 11】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 2nd embodiment of the present invention.

【Figure 12】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 3rd embodiment of the present invention.

【Figure 13】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 2nd embodiment of the present invention.

【Figure 14】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 2nd embodiment of the present invention.

【Figure 15】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation [...]

[...] method of the wiring structure that relates to a variant example of the 3rd embodiment.

【Figure 16】

(a) ~ (d) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to a variant example of the 3rd embodiment.

【Figure 17】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to a variant example of the 3rd embodiment.

【Figure 18】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 4th embodiment of the present invention.

【Figure 19】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 4th embodiment of the present invention.

【Figure 20】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 4th embodiment of the present invention.

【Figure 21】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 5th embodiment of the present invention.

【Figure 22】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 5th embodiment of the present invention.

【Figure 23】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 5th embodiment of the present invention.

【Figure 24】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to a variant example of the 5th embodiment.

【Figure 25】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to a variant example of the 5th embodiment.

【Figure 26】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to a variant example of the 5th embodiment.

【Figure 27】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to a variant example of the 5th embodiment.

【Figure 28】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to a variant example of the 5th embodiment.

【Figure 29】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to a variant example of the 5th embodiment.

【Figure 30】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 6th embodiment of the present invention.

【Figure 31】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 6th embodiment of the present invention.

【Figure 32】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to the 6th embodiment of the present invention.

【Figure 33】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to a variant example of the 6th embodiment.

【Figure 34】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to a variant example of the 5th embodiment.

【Figure 35】

(a) ~ (c) are cross-sectional diagrams wherein are shown the formulation method of the wiring structure that relates to a variant example of the 5th embodiment.

【Figure 36】

A plan view wherein is shown, as relates to the variant example of the 5th modification, the relationship between the opening portion(s) for wiring formation of the mask pattern with the opening portion(s) for the formation of the contact holes of the 2nd resist pattern.

【Figure 37】

(a) is a diagram wherein is shown the positional relationship(s) between mask pattern & the 2nd resist pattern and the positional relationship(s) between the 1st metal wiring and the contact for the variant example of the 5th embodiment, and (b) is a diagram wherein is shown the positional relationship(s) between mask pattern & the 2nd resist pattern and the positional relationship(s) between the 1st metal wiring and the contact for the 5th embodiment.

【Explanation of the Markings】

- 100 Semi-Conductor Substrate
- 101 1st Metal Wiring
- 102 Silicon Nitride Film
- 102A Patterned Silicon Nitride Film
- 103 1st Organic Film (1st Insulating Film)
- 103A Patterned 1st Organic Film
- 104 Silicon Nitride Film Containing Organic [component(s)]
- 104A Silicon Nitride Film Containing Patterned Organic [component(s)]
- 105 2nd Organic Film (3rd Insulating Film)
- 105A Patterned 2nd Organic Film
- 106 Titanium Nitride (Thin Film)
- 107 1st Resist Pattern
- 108 Mask Pattern
- 109 2nd Resist Pattern
- 110 Contact Hole(s)
- 111 Wiring Groove(s)

112 Adhesive Level
113 Metal Wiring
114 2nd Metal Wiring
115 Contact
200 Semi-Conductor Substrate
201 1st Metal Wiring
202 Silicon Nitride Film
202A Patterned Silicon Nitride Film
203 1st Organic Film (1st Insulating Film)
203A Patterned 1st Organic Film
204 Silicon Nitride Film Containing Organic [component(s)] (2nd Insulating Film)
204A Silicon Nitride Film Containing Patterned Organic [component(s)]
205 2nd Organic Film (3rd Insulating Film)
205A Patterned 2nd Organic Film
206 Titanium Nitride Film
207 1st Resist Pattern
208 Mask Pattern
209 2nd Resist Pattern
210 Contact Hole(s)
211 Wiring Groove(s)
212 Adhesive Level
213 Metal Film
214 2nd Metal Wiring
215 Contact
300 Semi-Conductor Substrate
301 1st Metal Wiring
302 Silicon Nitride Film
302A Patterned Silicon Nitride Film
303 1st Organic [component] Containing Silicon Nitride Film (1st Insulating Film)

303A Silicon Nitride Film Containing Patterned 1st Organic [component(s)]
304 Low Dielectric Constant SOG Film (2nd Insulating Film)
304A Patterned Low Dielectric Constant SOG Film
305 Titanium Nitride Film
305A Silicon Nitride Film Containing Patterned 2nd Organic [component(s)]
307 1st Resist Pattern
308 Mask Pattern
309 2nd Resist Pattern
310 Contact Hole(s)
311 Wiring Groove(s)
312 Adhesive Level
313 Metal Film
314 2nd Metal Wiring
315 Contact
350 Semi-Conductor Substrate
351 1st Metal Wiring
352 Silicon Dioxide Film
352A Patterned Silicon Dioxide Film
353 1st Silicon Dioxide Film (1st Insulating Film)
353A Patterned 1st Silicon Dioxide Film
354 Organic Film (2nd Insulating Film)
354A 1st Metal Film
355 2nd Silicon Dioxide Film
357 1st Resist Pattern
359 2nd Resist Pattern

360 Opening Portion(s) for Formation of Contact Hole(s)
361 Contact Hole(s)
362 Wiring Groove(s)
363 Adhesive Level
364 Metal Film
365 2nd Metal Film
366 Contact(s)
400 Semi-Conductor Substrate
401 1st Metal Wiring
402 Silicon Nitride Film
402A Patterned Silicon Nitride Film
403 1st Low Dielectric Constant SOG Film (1st Insulating Film)
403A Patterned Low Dielectric Constant SOG Film
404 Silicon Dioxide Film Containing Organic [component(s)]
404A Silicon Dioxide Film Containing Patterned Organic [component(s)]
405 2nd Low Dielectric SOG Constant Film (3rd Insulating Film)
405A Patterned 2nd Low Dielectric SOG Constant Film
406 Titanium Nitride Film
407 1st Resist Pattern
408 Mask Pattern
409 2nd Resist Pattern
410 Damaged Level
411 Contact Hole(s)
412 Wiring Groove(s)
413 Adhesion Layer
414 Metal Film
415 2nd Metal Film
416 Contact(s)
500 Semi-Conductor Substrate

501 1st Metal Wiring
502 Silicon Nitride Film
502 Patterned Silicon Nitride Film
503 1st Organic Film (1st Insulating Film)
503A Patterned 1st Organic Film
504 1st Silicon Nitride Film (2nd Insulating Film)
504A Patterned 1st Silicon Nitride Film
505 2nd Organic Film (3rd Insulating Film)
505A Patterned 2nd Organic Film
505B Patterned 2nd Organic Film
506 2nd Organic Film (4th Insulating Film)
506A Patterned 2nd Organic Film
506B Patterned 2nd Organic Film
507 Titanium Nitride Film (Thin Film)
508 1st Resist Pattern
509 Mask Pattern
510 2nd Resist Pattern
511 Wiring Groove(s)
512 Contact Hole(s)
513 2nd Metal Wiring
514 Contact(s)
550 Semi-Conductor Substrate
551 1st Metal Wiring
552 Silicon Nitride Film
552A Patterned Silicon Nitride Film
553 1st Organic Film (1st Insulating Film)
553A Patterned 1st Organic Film
554 1st Silicon Dioxide Film (2nd Insulating Film)
554A Patterned 1st Silicon Dioxide Film

555 2nd Organic Film (3rd Insulating Film)
555A Patterned 2nd Organic Film
555B Patterned 2nd Organic Film
556 2nd Silicon Dioxide Film (4th Insulating Film)
556A Patterned 2nd Silicon Dioxide Film
556B Patterned 2nd Silicon Dioxide Film
557 Titanium Nitride Film (Thin Film)
558 1st Resist Pattern
559 Mask Pattern
560 2nd Resist Pattern
561 Wiring Groove(s)
562 Contact Hole(s)
563 2nd Metal Wiring
564 Contact(s)
600 Semi-Conductor Substrate
601 1st Metal Wiring
602 Silicon Nitride Film
602A Patterned Silicon Nitride Film
603 1st Organic Film (1st Insulating Film)
603A Patterned 1st Organic Film
604 Silicon Dioxide Film (2nd Insulating Film)
604A Patterned Silicon Dioxide Film
605 2nd Organic Film (3rd Insulating Film)
605A Patterned 2nd Organic Film
606 Titanium Nitride Film (Thin Film)
607 1st Resist Pattern
608 Mask Pattern
609 2nd Resist Pattern
610 Wiring Groove(s)

611 Contact Hole(s)
612 2nd Metal Wiring
613 Contact(s)
650 Semi-Conductor Substrate
651 1st Metal Wiring
652 Silicon Nitride Film
652A Patterned Silicon Nitride Film
653 1st Organic Film (1st Insulating Film)
654 Silicon Dioxide Film (2nd Insulating Film)
654A Patterned Silicon Dioxide Film
655 2nd Organic Film
655A Patterned 2nd Organic Film
656 Titanium Nitride Film (Thin Film)
657 1st Resist Pattern
658 Mask Pattern
659 2nd Resist Pattern
660 Wiring Groove(s)
661 Contact Hole(s)
662 2nd Metal Wiring
663 Contact(s)