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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
GLOBALFOUNDRIES U.S. INC., and
QUALCOMM INCORPORATED,
Petitioner,

v.

KAIST IP US LLC,
Patent Owner.

Case IPR2017-01046
Patent 6,885,055 B2

Before KERRY BEGLEY, MINN CHUNG, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

This case concerns U.S. Patent No. 6,885,055 B2 (Ex. 1001, "the '055 patent"). Samsung Electronics Co., Ltd., Globalfoundries U.S. Inc., and QUALCOMM Incorporated (collectively "Petitioner") filed a Petition seeking *inter partes* review of claims 1–6, 11, 12, and 14–17 of the '055 patent (Paper 1, "Pet."). KAIST IP US LLC ("Patent Owner") filed a Preliminary Response. Paper 10 ("Prelim. Resp.").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). An *inter partes* review may be authorized only if the information presented in the Petition and the Preliminary Response shows that there is a reasonable likelihood that Petitioner would prevail with respect to at least one claim challenged in the Petition. 35 U.S.C. § 314(a).

Petitioner challenges claims 1–6, 11, 12, and 14–17 of the '055 patent as unpatentable under 35 U.S.C. § 103. Pet. 2–3. Based on the arguments and evidence presented in the Petition and Preliminary Response, we determine that Petitioner has not established a reasonable likelihood that it would prevail with respect to at least one of the claims challenged in the Petition. Therefore, institution of an *inter partes* review is denied.

I. BACKGROUND

A. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), the parties identify the following civil action involving the '055 patent: *KAIST IP US LLC v. Samsung Electronics Co.*, No. 2:16-cv-01314-JRG-RSP (E.D. Tex., filed November 29, 2016). Pet. 1; Paper 5, 1 (Patent Owner's Mandatory Notices).

The parties also identify IPR2017-01047 in which the same Petitioner challenges claims 7, 9, 10, 13, and 19 of the '055 patent. Pet. 1; Paper 5, 1.

B. Petitioner's Asserted Grounds of Unpatentability

Petitioner advances four grounds of unpatentability under 35 U.S.C. § 103(a) in relation to the challenged claims in the '055 patent:

	References	Challenged Claim(s)
1	Inaba,[1] Hieda,[2] and Mizuno[3]	1–6, 11, 12, and 14–17
2	Inaba, Hieda, Mizuno, and Seliskar[4]	15
3	Inaba and Hieda	1–6, 11, 12, and 14–17
4	Inaba, Hieda, and Seliskar	15

Pet. 2–3. Petitioner supports its challenge with a Declaration of Dr. Jeffrey Bokor. Ex. 1002. Patent Owner supports its Preliminary Response with a Declaration of Kelin Kuhn, Ph.D. Ex. 2001.

[1] Inaba et al., U.S. Patent No. 6,525,403 B2, filed September 24, 2001 and issued February 25, 2003, Ex. 1005 ("Inaba").

[2] Hieda, U.S. Publication No. 2002/0011612, published January 31, 2002, Ex. 1006 ("Hieda").

[3] Mizuno et al., U.S. Patent No. 5,844,278, issued December 1, 1998, Ex. 1007 ("Mizuno"). Hieda and Mizuno are asserted as prior art to the '055 patent under pre-AIA 35 U.S.C. § 102(b). Pet. 3.

[4] Seliskar et al., U.S. Patent No. 6,355,532 B1, filed October 6, 1999 and issued March 12, 2002, Ex. 1008 ("Seliskar"). Inaba and Seliskar are asserted as prior art to the '055 patent under pre-AIA 35 U.S.C. § 102(e). Pet. 3.

C. The ’055 Patent (Ex. 1001)

The ’055 patent issued from U.S. Application No. 10/358,981, filed February 4, 2003. Ex. 1001, [21], [22].

The ’055 patent relates to a double-gate Fin Field Effect Transistor (“FinFET”). *Id.* at [57], 1:6–7. According to the ’055 patent, a FinFET is a conventional CMOS[5] structure that enables reduced channel length and nano-sized devices. *Id.* at 1:15–28, 1:65–67, 2:37–39, 3:21–29, Figs. 1c, 2. The ’055 patent identifies disadvantages of conventional double-gate MOS devices fabricated on Silicon On Insulator (“SOI”) substrates. *Id.* at [57], 1:46–64, 3:64–4:7. According to the ’055 patent, these problems are addressed by providing a double-gate FinFET device fabricated on a bulk silicon substrate, where the Fin active region is connected to the substrate. *Id.* at [57], 1:8–14, 4:10–19.

An embodiment is shown in Figure 3a of the ’055 patent, which is reproduced below:

[5] We understand MOS as an acronym for Metal Oxide Semiconductor and CMOS as an acronym for Complementary Metal Oxide Semiconductor.

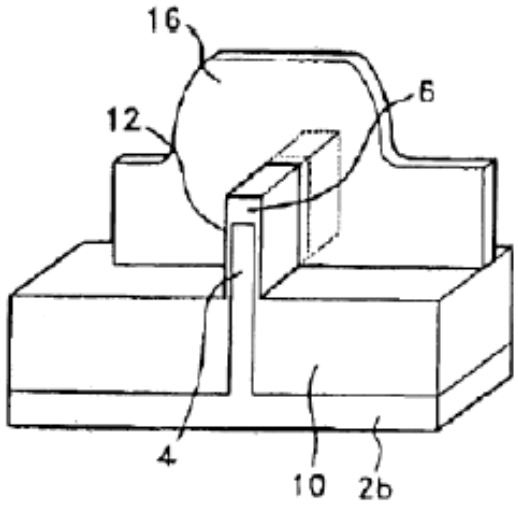

Fig. 3a

Figure 3a of the ’055 patent shows a perspective view of a FinFET device, including bulk silicon substrate 2b, Fin active region 4, second oxide layer 10, gate oxide layer 12 at both side-walls of Fin active region 4, first oxide layer 6 on the upper surface of Fin active region 4, and gate 16 on first oxide layer 6 and second oxide layer 10. Ex. 1001, 4:62–65, 5:36–48. Fin active region 4 consists of single crystalline silicon with the shape of a wall on the surface of bulk silicon substrate 2b and is connected to bulk silicon substrate 2b. *Id.* at 5:36–40. A source/drain region is formed on both sides of Fin active region 4, except where the gate 16 overlaps with the Fin active region. *Id.* at 5:48–51.

According to the ’055 patent, the device structure shown in Figure 3a differs from a conventional FinFET structure in that “Fin active region 4 is not floating and is connected to the bulk silicon substrate” (*id.* at 6:16–17) and “the device is fabricated on a bulk wafer rather than a SOI wafer” (*id.* at 6:25–26). The ’055 patent states that this structural change results in improved device characteristics by removing the floating body problem and

providing more efficient transfer of heat from the channel to the substrate. *Id.* at 6:17–24. A cost advantage is also noted. *Id.* at 6:25–26.

A metal layer for wiring is omitted from Figure 3a of the ’055 patent (*id.* at 6:12), but is shown in plain view in Figure 6d, which is reproduced below:

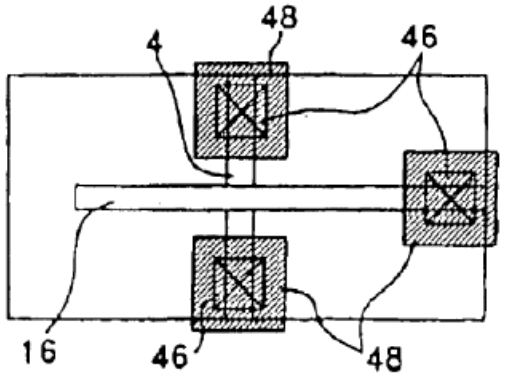

Fig. 6d

Figure 6d of the ’055 patent shows the masking steps for implementing a FinFET device, including contact regions 46 and metal layer 48, which are formed at the source/drain and gate 16 contact regions. *Id.* at 5:4–6, 5:51–53, 7:37–43.

D. Illustrative Claim

The ’055 patent includes 19 claims, of which claims 1, 7, and 13 are independent. The Petition in IPR2017-01046 challenges claim 1 and the claims that depend, directly or indirectly, from claim 1, i.e., claims 2–6, 11, 12, and 14–17. Claim 1 is the sole independent claim challenged in the Petition and is reproduced below, with parenthetical letters (a)–(j) added to correspond with Petitioner’s identification of the claim elements:

1. (a) A double-gate FinFET device, comprising:

(b) a bulk silicon substrate;

> (c) a Fin active region which is a wall-shape single crystalline silicon on a surface of the bulk silicon substrate and connected to said bulk silicon substrate;
>
> (d) a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate;
>
> (e) a gate oxide layer which is formed on both side-walls of the Fin active region protruded from said second oxide layer;
>
> (f) a first oxide layer which is formed on the upper surface of said Fin active region with a thickness greater or equal to that of the gate oxide;
>
> (g) a gate which is formed on said first and second oxide layer;
>
> (h) a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region; and
>
> (i) a contact region and a metal layer which are formed at said source/drain and gate contact region,
>
> (j) wherein the thickness of said gate oxide layer is between 0.5 nm and 10 nm, and the thickness of said first oxidation layer is between 0.5 nm and 200 nm.

Ex. 1001, 12:2–27.

II. DISCUSSION

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *Cuozzo Speed Tech., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016). Under that standard, we generally give claim terms their ordinary and customary meaning, as understood by a person of ordinary skill in the art in the context of the entire

patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

For purposes of IPR2016-01046, the parties contend that the claim terms should be given their plain and ordinary meaning. Neither party proposes an express construction for any claim term. Pet. 15–16; Prelim. Resp. 28.

Consistent with the parties' contentions, we determine that no claim term requires express construction for purposes of this Decision. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art ("POSA") would have had at least a master's degree or higher in materials science, physics, electrical engineering, or related disciplines, and three to four years of experience in the design and fabrication of metal-oxide semiconductor field-effective-transistors ("MOSFETs"). Pet. 4–5 (citing Ex. 1002 ¶ 18). Petitioner contends that more education can supplement practical experience and vice versa. *Id.* at 5.

Patent Owner does not dispute a POSA's level of education as defined by Petitioner (Prelim. Resp. 10–12), but argues that "a POSA's experience would have been limited to *planar* MOSFETs, as opposed to non-planar, three-dimensional MOSFET devices" (*id.* at 11). Patent Owner contends that "a POSA would have had several years of *practical* experience in the design and fabrication of *planar* MOSFETs." *Id.*

We determine that it is unnecessary to resolve the parties' dispute regarding the level of ordinary skill in the art for purposes of this Decision. For the reasons discussed below, Petitioner has not established a reasonable

likelihood of prevailing on its contention of obviousness under either party's definition of a POSA.

C. Petitioner's Grounds 1 and 2

Petitioner's Ground 1 contends that claims 1–6, 11, 12, and 14–17 of the '055 patent are unpatentable as obvious in view of Inaba, Hieda, and Mizuno. Pet. 16–72. Petitioner's Ground 2 contends that, in the alternative, claim 15 is unpatentable as obvious in view of Inaba, Hieda, Mizuno, and Seliskar. *Id.* at 72–76. Patent Owner opposes both of these grounds. Prelim. Resp. 32–62.

1. Inaba (Ex. 1005)

Inaba discloses a metal-insulator semiconductor field effect transistor ("MISFET") having a three-dimensional structure. Ex. 1005, 1:16–17, 4:10–13.

Inaba discloses six embodiments. *Id.* at 3:35–4:5. The Petition focuses on the embodiments shown in Figures 6 and 8. Pet. 9–11.

A first embodiment is shown in Figure 6, which is reproduced below:

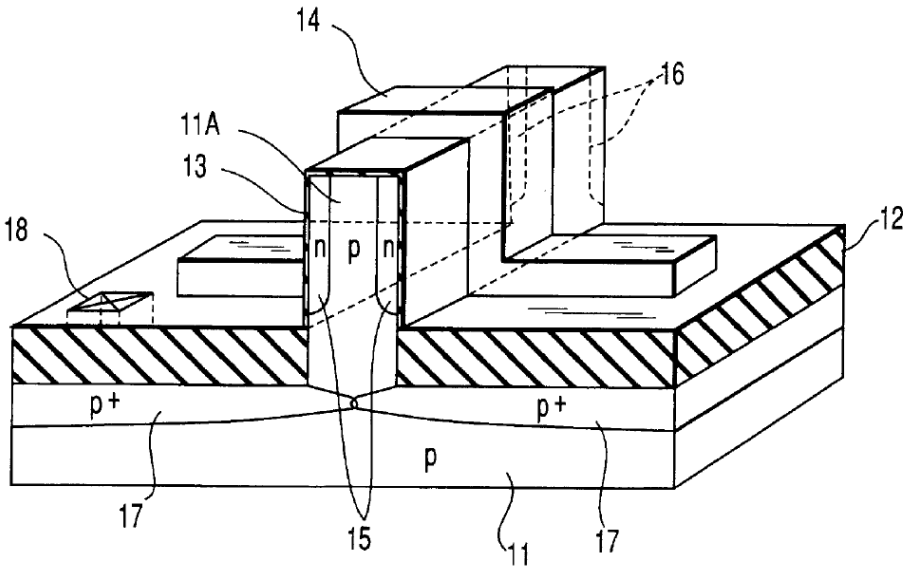

FIG. 6

Inaba Figure 6 shows a semiconductor device, including p-type silicon semiconductor substrate 11 processed to have substrate projection 11A, which forms a device region. Ex. 1005, 4:14–18, Fig. 6. Device isolation insulating film 12 is formed on semiconductor substrate 11 in device isolation regions. *Id.* at 4:20–21, Fig. 6. Gate insulating film 13, e.g., silicon oxide, is formed on the top and side surfaces of substrate projection 11A. *Id.* at 4:29–33, Fig. 6. Gate electrode 14 is formed on a portion of gate insulating film 13 and on a portion of device isolation insulating film 12. *Id.* at 4:34–37, Fig. 6. Source and drain regions 15 and 16 are formed by ion implantation in the side surfaces and optionally the top surface of projection 11A on opposite sides of gate electrode 14. *Id*. at 4:37–52, Fig. 6. Heavily doped regions 17 are formed in the substrate below device isolation insulating film 12 and substrate projection 11A. *Id.* at 4:55–56, Fig. 6. Contact plug 18 electrically connects an interconnect layer (not shown in Figure 6) to heavily doped regions 17 of semiconductor substrate

11. *Id.* at 4:64–5:4, Fig. 6. Another contact (not shown in Figure 6) connects gate electrode 14 to an interconnect layer. *Id.* at 5:8–11, Fig. 6.

A second embodiment is shown in Figure 8, which is reproduced below:

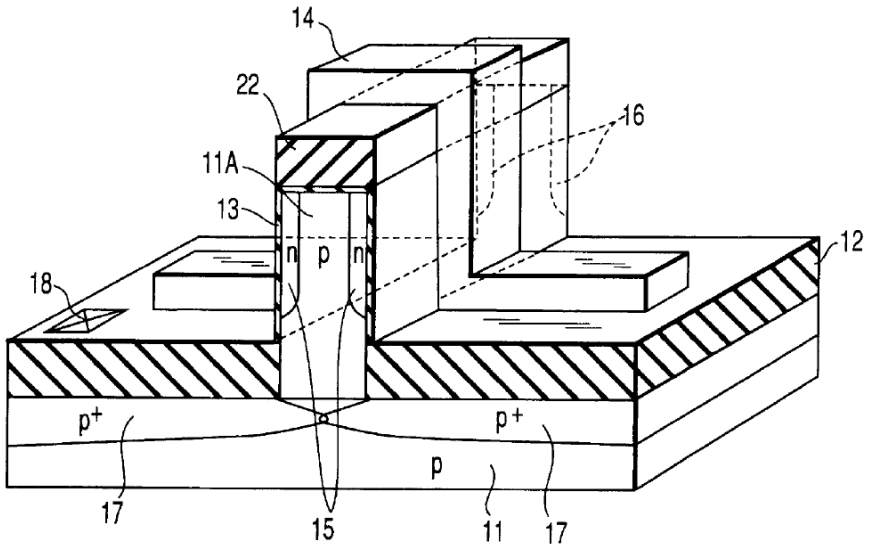

FIG. 8

Inaba Figure 8 shows a semiconductor device. Ex. 1005, 7:56–57. In the Figure 8 embodiment, insulating film 22 is between gate electrode 14 and the top surface of substrate projection 11A. *Id.* at 7:58–59, 7:66–8:3. According to Inaba, insulating film 22 is made sufficiently thick so as not to allow a channel to be formed in the top surface of the substrate projection under normal operating voltages. *Id.* at 7:10–17, 7:66–8:3.

Patent Owner directs us to Inaba Figure 14 (Prelim. Resp. 36, 54), which shows a fifth embodiment and is reproduced below:

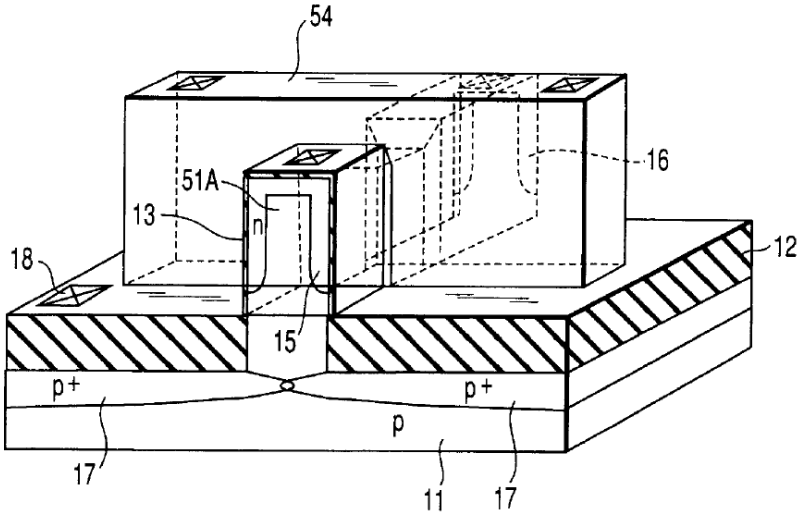

FIG. 14

Inaba Figure 14 shows a semiconductor device, including substrate projection 51A, device isolation insulating film 12, gate insulating film 13, source and drain diffusion layers 15 and 16, and gate electrode 54. Ex. 1005, 12:58–59, 13:6–29. Inaba's Figure 14 embodiment aims to reduce the difference in level between the gate contact area and the source and drain contact areas, compared with other disclosed embodiments. *Id.* at 12:28–33, 12:53–57, 13:19–22. To accomplish this, substrate projection 51A is made thick in the source and drain portions and thin in the channel portion, and gate electrode 54 is made from a thick film of polysilicon, which is polished to have a height as shown in Figure 14. *Id.* at 13:6–19. According to Inaba, the Figure 14 structure permits contact holes to be formed simultaneously on gate electrode 54 and source and drain diffused layers 15 and 16 and also permits the aspect ratio of the contact holes to be reduced. *Id.* at 13:30–34.

2. Hieda (Ex. 1006)

Hieda discloses a MOS transistor structure having a semiconductor layer having a convex configuration approximately perpendicular to a

semiconductor substrate; a gate insulating film and a gate electrode formed on both sides of the convex semiconductor layer; a source region, a drain region, and a channel provided in the convex semiconductor layer; and a channel width determined by the depth of the source/drain region. Ex. 1006, [57], ¶ 3.

Hieda discloses 27 embodiments. *Id.* ¶¶ 43–168. A first embodiment is shown in Figure 1, which is reproduced below:

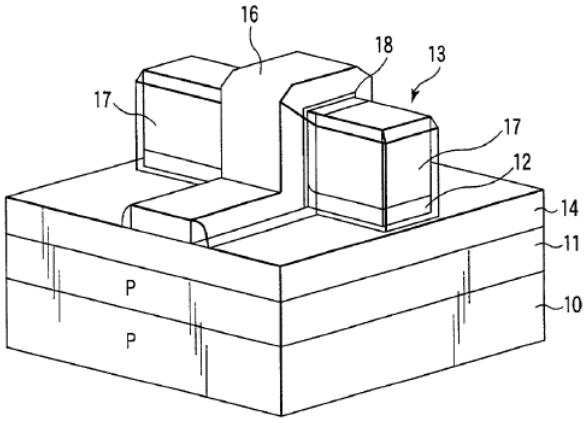

FIG. 1

Hieda Figure 1 shows a MOSFET, including silicon substrate 10, p-type well 11, punch-through stopper layer 12, convex thin film silicon layer 13, also referred to as fence 13, isolation insulating film 14, gate electrode 16, source/drain region 17, and gate insulating film 18. Ex. 1006 ¶¶ 174–179. Plan and sectional views of the first embodiment are shown in Figures 2A–2D, which are reproduced below:

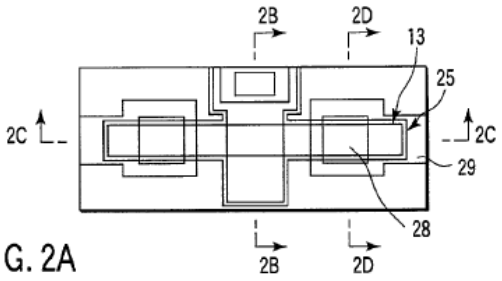

FIG. 2A

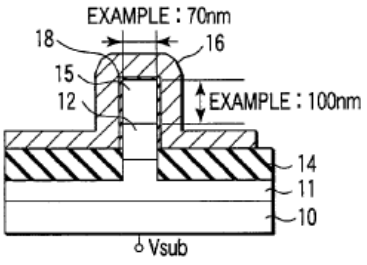

FIG. 2B

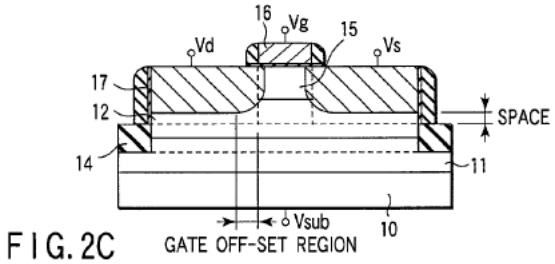

FIG. 2C

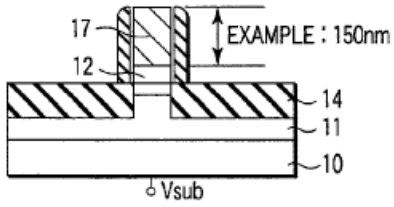

FIG. 2D

Figure 2A of Hieda shows a plan view of a MOSFET, including contact plug 28 and wiring layer 29, which are omitted from Figures 1 and 2B–2D. Ex. 1006 ¶ 174.[6] Figures 2B–2D of Hieda show sectional views of a MOSFET, including channel region 15, in addition to the structures identified above with reference to Figure 1.

A method for manufacturing a MOSFET according to the first embodiment is illustrated by Hieda Figures 3 to 11. *Id.* ¶ 180. Figures 11A and 11B are reproduced below.

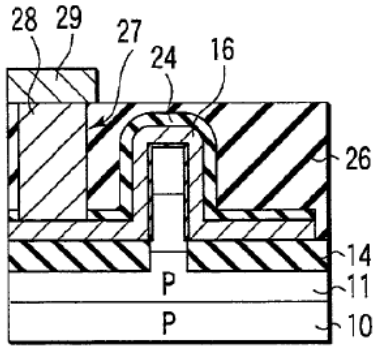

FIG. 11A

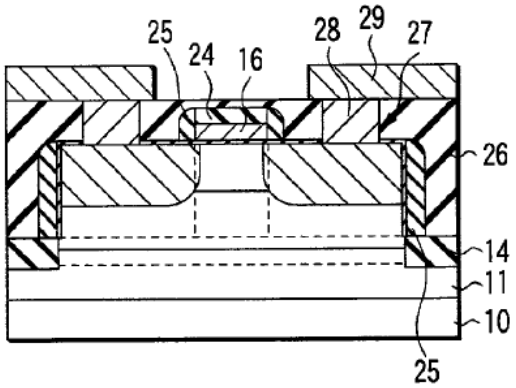

FIG. 11B

Hieda Figures 11A and 11B are sectional views of a semiconductor device, including gate cap insulating film 24, side-wall insulating film 25, interlayer insulating film 26, contact hole 27, contact plug 28, and wiring layer 29.

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[6] Hieda Figure 2A also shows side-wall insulating film 25. Ex. 1006 ¶¶ 210–212, 214, 218, Figs. 9B, 29.

Ex. 1006 ¶¶ 180, 204, 210, 223. According to Hieda, contact hole 27 is formed in interlayer insulating film 26 and filled with conductive material to form contact plug 28, which is in electrical contact with subsequently formed wiring layer 29. *Id.* ¶ 223.

3. Claim 1

Petitioner contends that Inaba teaches all elements of claim 1, except for claim elements 1(i) and 1(j). Pet. 16–44. Our analysis focuses on claim element 1(i), which recites: "a contact region and a metal layer which are formed at said source/drain and gate contact region." Ex. 1001, 12:23–24.

Petitioner contends that Inaba in combination with Hieda discloses or suggests this feature. Pet. 33. More specifically, Petitioner contends that Inaba's Figure 8 embodiment discloses both source/drain contacts and a gate contact, but does not describe these aspects in great detail. *Id.* at 33–34. Petitioner contends that Hieda discloses a FinFET device similar to that disclosed in Inaba and that Hieda Figures 2A, 11A, and 11B disclose a gate contact region and metal layer (e.g., contact plug 28) and a source/drain contact region and metal layer (e.g., contact plug 28). *Id.* at 34–37.

Petitioner contends "it would have been obvious to combine the teachings of Inaba and Hieda for the purpose of providing contacts to the gate and source/drain." Pet. 38. Petitioner asserts that a "POSA would have looked to Hieda to implement the gate and source/drain contact areas in Inaba's device because both references are directed to FinFET devices while Hieda goes on to describe the details of the source/drain and gate contact areas." *Id.* Petitioner further asserts that a POSA would have been motivated to make the proposed combination "so that each of [Inaba's source, drain, and gate] regions can be electrically connected to other

devices (such as other FinFETs) and signals on the chip" and to "ensure proper device operation in Inaba, particularly given Inaba's own disclosures regarding the need for [source, drain, and gate] contacts." *Id.* (citing Ex. 1002 ¶¶ 85–86; Ex. 1005, 4:49–54, 5:8–9, 10:40–46, 12:28–33).

Patent Owner challenges the sufficiency of Petitioner's reasons for combining Inaba and Hieda. Prelim. Resp. 32–48. Patent Owner argues that a POSA would not have looked beyond Inaba to ensure proper device operation because Inaba discloses all essential device features, including a contact configuration. *Id.* at 34, 36 (citing Ex. 1005, Fig. 14). Patent Owner argues that a POSA would not have relied on Hieda for additional details relating to the source/drain contacts because Inaba's Figure 8 embodiment needs a different contact architecture than Hieda due to Inaba's thin-sidewall source/drain regions. *Id.* at 35. Patent Owner additionally argues there would have been no reasonable expectation of success for Petitioner's proposed combination because Hieda's contact architecture depends on a full-fin source/drain, which differs from Inaba's thin sidewall source/drain regions. *Id.* at 38–40. Patent Owner argues that Petitioner's proposed combination would have generated unpredictable and undesirable "ripple effects" and that Petitioner's analysis fails to address the complexities of semiconductor device fabrication. *Id.* at 38, 44–47.

The legal conclusion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning" for combining elements in the manner claimed. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

> To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.

In re Magnum Oil Tools Int'l, Ltd., 829 F.3d 1364, 1380 (Fed. Cir. 2016) (citing *KSR*, 550 U.S. at 418)). Although the *KSR* test is flexible, we "must still be careful not to allow hindsight reconstruction of references . . . without any explanation as to *how* or *why* the references would be combined to produce the claimed invention." *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1066 (Fed. Cir. 2016) (citation omitted).

Here, Patent Owner persuades us that Petitioner's reasoning with respect to claim element 1(i) and the proposed combination of Inaba and Hieda is insufficient to support institution of *inter partes* review.

On this record, Petitioner's assertion that both Inaba and Hieda are directed to FinFET devices (Pet. 38) is not sufficient to support Petitioner's proposed combination. That reasoning is too generalized and does not address the specific elements of Inaba and Hieda that Petitioner seeks to modify and combine. *See ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012) (asserted motivation to combine is insufficient if it is "generic and bears no relation to any specific combination of prior art elements" and "fails to explain why a person of ordinary skill in the art would have combined elements from specific references in the way the claimed invention does").

Petitioner's assertion that Hieda provides details regarding the source/drain and gate contact areas that are lacking in Inaba (Pet. 38) is not adequately supported by the record. We find that both Inaba and Hieda disclose contacts. For example, Inaba discloses both (1) a contact that

electrically connects an interconnect layer to a gate electrode, and (2) contacts that electrically connect interconnect layers to the source and drain diffused layers. Ex. 1005, 4:49–54, 5:8–11, 13:20–23, 13:30–34, Fig. 14. Inaba also discloses contact plug 18 that electrically connects an interconnect layer to heavily doped regions 17 of semiconductor substrate 11. *Id.* at 4:64–5:4, Figs. 6, 8. Although Petitioner and its declarant assert that Inaba does not describe the details of the source, drain, and gate contact areas (Pet. 34; Ex. 1002 ¶ 85), they do not address Inaba Figure 14. Nor does Petitioner explain sufficiently *why* a POSA would have replaced Inaba's contact architecture with Hieda's.

Petitioner asserts that a POSA would have been motivated to combine Hieda's contact plug and metal layer with Inaba so that Inaba's source, drain, and gate regions can be electrically connected and to ensure proper device operation. Pet. 38. That reasoning is inadequate under the present circumstances. As discussed above, Inaba discloses interconnect layers and contacts to the source, drain, and gate regions, and Petitioner does not explain *why* a POSA would have substituted Hieda's contacts and metal layers for Inaba's.

Petitioner also fails to explain sufficiently *how* a POSA would have implemented Hieda's source/drain contact areas in Inaba's device. Although not explicitly stated, for claim element 1(i), Petitioner appears to be proposing a modification of Inaba's Figure 8 embodiment. Pet. 33–34. That is the embodiment Petitioner relies upon for claim elements 1(a)–(h). *Id.* at 16–33. In Inaba Figure 8, the source and drain regions 15 and 16 are shown as being formed only in the side surfaces of substrate projection 11A. Ex. 1005, Fig. 8. Petitioner quotes Inaba's description of the Figure 6

embodiment that source and drain regions "may also be formed in the top surface of the projection ***as required***." Pet. 38 (emphasis added, quoting Ex. 1005, 4:51–52). Petitioner does not, however, explain whether source and drain regions in the top surface of the projection would be ***required, or even compatible***, with Inaba's Figure 8 embodiment.

Such compatibility is not self-evident. According to Inaba, "no channel is formed in the top surface of the substrate projection" in the Figure 8 embodiment and "only the side surfaces of the projection" are used as the channel. Ex. 1005, 7:1–12. Inaba describes the Figure 8 embodiment as including insulating film 22—the feature Petitioner relies upon to show claim element 1(f) (Pet. 30–31)—and discloses that the film is sufficiently thick to prevent a channel from being formed in the top surface of the substrate projection. Ex. 1005, 7:10–17, 7:66–8:3. For claim element 1(h)—a source/drain region—Petitioner relies on Inaba's disclosure that impurities are "introduced into the side surfaces of the projection 11A." Pet. 32 (citing Ex. 1005, 8:18–22, 4:42–45, Figs. 6, 8). With respect to the Figure 6 embodiment, Inaba discloses that source/drain regions "may also be formed in the top surface of the projection" and "[i]n that case, contact can be made to interconnect layers via the drain and source regions formed in the top surface." Ex. 1005, 4:52–54. Petitioner does not explain sufficiently how or why a POSA would have combined an optional feature of Inaba's Figure 6 embodiment (source/drain regions formed in the top surface of the projection) with a feature of Inaba's Figure 8 embodiment (thick insulating film 22) that prevents a channel from being formed in the top surface of the substrate projection. Nor does Petitioner explain sufficiently how or why a POSA would have formed contacts to the top surface of a projection or

fence, such as contact plug 28 shown in Hieda Figures 2A and 11B, in an embodiment like Inaba's Figure 8, which does not have a source or drain region formed in the top surface of the projection and includes thick insulating film 22 on that surface. Ex. 1005, Fig. 8.

Petitioner nowhere clearly explains, nor cites evidence showing, how the combination of Inaba's Figure 8 embodiment and Hieda's source/drain contacts is supposed to work. For example, Petitioner does not explain how Hieda's top surface contact plugs 28 would have provided an electrical connection to Inaba's side surface source and drain regions 15 and 16. Nor does Petitioner present argument or evidence sufficient to show that a POSA would have had a reasonable expectation of success in making the proposed combination. Although Petitioner cites paragraphs 85 and 86 of the Bokor declaration, those paragraphs provide no greater level of detail than the Petition. *Compare* Pet. 38–39, *with* Ex. 1002 ¶¶ 85, 86. The complexities of semiconductor device fabrication and operation demand a more fulsome explanation than has been provided by Petitioner and its declarant. *Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017) ("[A] clear, evidence-supported account of the contemplated workings of the combination is a prerequisite to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination and reasonably expect success in doing so.").

Accordingly, we determine that Petitioner's arguments and evidence do not establish a reasonable likelihood of prevailing on its contention that claim 1 is unpatentable as obvious in view of Inaba, Hieda, and Mizuno.

4. Claims 2–6, 11, 12, and 14–17

Claims 2–6, 11, 12, and 14–17 of the '055 patent each depends directly or indirectly from claim 1. Ex. 1001, 12:28–45, 13:30–39, 14:22–34.

The deficiencies in Petitioner's arguments and evidence regarding claim element 1(i), as discussed above, are not remedied by Petitioner's arguments and evidence regarding claims 2–6, 11, 12, and 14–17. *See* Pet. 44–72. Nor are they remedied by Petitioner's arguments and evidence regarding claim 15 and Seliskar. *See id.* at 72–76.

Regarding claim 6, for example, Petitioner relies on its analysis for claim element 1(i), including Hieda's disclosure of source, drain, and gate contacts in Figures 2A, 11A, and 11B. *Id.* at 55–57. Petitioner's claim 6 analysis assumes that a POSA has already drawn from Hieda's disclosure regarding source/drain contacts to modify Inaba's Figure 8 embodiment. *Id.* at 61. Petitioner does not explain how its arguments and evidence regarding claim 6 would have supported the combination of Inaba and Hieda with respect to claim element 1(i).

Accordingly, we conclude that Petitioner has not demonstrated a reasonable likelihood of prevailing on its challenges to claims 2–6, 11, 12, and 14–17 based on Grounds 1 and 2 for the same reasons as discussed above with respect to claim 1.

D. Petitioner's Grounds 3 and 4

Petitioner's Ground 3 contends that claims 1–6, 11, 12, and 14–17 of the '055 patent are unpatentable as obvious in view of Inaba and Hieda, without relying on Mizuno. Pet. 76–80. Petitioner's Ground 4 contends that claim 15 is unpatentable as obvious in view of Inaba, Hieda, and Seliskar,

without relying on Mizuno. *Id.* at 80–81. Patent Owner opposes both of these grounds. Prelim. Resp. 63–66.

Petitioner's Grounds 3 and 4 rely on the same analysis for claim element 1(i) as discussed above with respect to Grounds 1 and 2. Pet. 76, 80–81. Accordingly, we conclude that Petitioner has not demonstrated a reasonable likelihood of prevailing on its challenge to claims 1–6, 11, 12, and 14–17 based on Grounds 3 and 4 for the same reasons as discussed above with respect to Grounds 1 and 2.

III. *CONCLUSION*

Petitioner has not demonstrated a reasonable likelihood of prevailing with respect to claims 1–6, 11, 12, and 14–17 of the '055 patent challenged in the Petition.

IV. ORDER

Accordingly, it is

ORDERED that the Petition is denied.

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