

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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UNIFIED PATENT INC.,  
Petitioner

v.

PLECTRUM LLC,  
Patent Owner

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IPR2017-01430  
Patent 5,978,951

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Before KEN B. BARRETT, MIRIAM L. QUINN, and  
SHEILA F. McSHANE, *Administrative Patent Judges*.

McSHANE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION  
*Inter Partes* Review  
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

## I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 8 and 11 of U.S. Patent No. 5,978,951 (Ex. 1001, “the ’951 patent”) are unpatentable and Petitioner has not shown, by a preponderance of the evidence, that claims 1–6, 12–14, and 21–24 of the ’951 patent are unpatentable.

### A. Procedural Background

Unified Patents Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–6, 8, 11–14, and 21–24 (“the challenged claims”) of the ’951 patent pursuant to 35 U.S.C. §§ 311–319. Paper 3 (“Pet.”). The Declaration of Dr. Srinivasan Seshan (“Seshan Declaration”) in support of the Petition was filed. Ex. 1007. Plectrum LLC (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 7 (“Prelim. Resp.”). Pursuant to 35 U.S.C. § 314(a), on November 14, 2017, we instituted *inter partes* review on the following ground:

-whether claims 8 and 11 would have been obvious under  
35 U.S.C. § 103(a) in view of Cheriton<sup>1</sup> and Jain<sup>2</sup>.

See Paper 8 (“Inst. Dec.” or “Dec.”). Subsequent to institution, Petitioner filed a Request for Rehearing, which was denied. Papers 10, 11. Patent

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<sup>1</sup> U.S. Patent No. 6,091,725 (issued July 18, 2000) (Ex. 1002).

<sup>2</sup> European Patent Application No. 0 522 743 A1 (published January 13, 1993) (Ex. 1003).

Owner filed a Patent Owner Response. Paper 12 (“PO Resp.”). Petitioner filed a Reply to the Patent Owner Response. Paper 14 (“Pet. Reply”).

On April 24, 2018, the Supreme Court held that a final written decision in an *inter partes* review must decide the patentability of all claims challenged in the petition. *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018) (“SAS”). Pursuant to *SAS*, on May 3, 2018, we instituted *inter partes* review on the following additional grounds:

-whether claims 1, 2, and 21 would have been obvious under 35 U.S.C. § 103(a) in view of Cheriton;

-whether claims 3, 5, and 6 would have been obvious under 35 U.S.C. § 103(a) in view of Cheriton and Kessler<sup>3</sup>;

-whether claims 4 and 22–24 would have been obvious under 35 U.S.C. § 103(a) in view of Cheriton, Kessler, and Jain; and

-whether claims 12–14 would have been obvious under 35 U.S.C. § 103(a) in view of Cheriton and Jain.

*See* Paper 15; *see also PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360–61 (Fed. Cir. 2018) (reading “the *SAS* opinion as interpreting the statute to require a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”); *Guidance on the Impact of SAS on AIA Trial Proceedings* (April 26, 2018) (available at <https://www.uspto.gov/patents-application-process/patent-trial-and->

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<sup>3</sup> R.E. Kessler, *Inexpensive Implementations of Set-Associativity*, ACM SIGARCH COMPUTER ARCHITECTURE NEWS–SPECIAL ISSUE: PROCEEDINGS OF THE 16TH ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, 17:3, 131–139 (June 1989) (Ex. 1004). Petitioner provides a stamped copy of the portion of the Proceedings (Ex. 1005), and a declaration attesting to the authenticity of the document and its public availability. Ex. 1006.

appealboard/trials/guidance-impact-sas-aia-trial) (“[I]f the PTAB institutes a trial, the PTAB will institute on all challenges raised in the petition.”). The parties were requested to advise the Board if they wished to change the case schedule or submit further briefing in light of the institution on additional claims and grounds. Paper 15, 1. Petitioner requested leave to file additional supplemental briefing on the newly-instituted grounds, and the request was granted. Paper 16, 2–3. Petitioner later raised a request to submit additional evidence and that request was denied. Paper 17, 2–7. Petitioner filed a Supplemental Reply (Paper 18, “Pet. Supp. Reply”).

An oral hearing was held on August 2, 2018. A transcript of the hearing is included in the record. Paper 29 (“Tr.”).

#### *B. Related Proceedings*

Patent Owner indicates that related matters are these Eastern District of Texas cases: *Plectrum LLC v. Arista Networks, Inc.*, Case No. 4:17-cv-00076; *Plectrum LLC v. Brocade Communications Systems, Inc.*, Case No. 4:17-cv-00077; *Plectrum LLC v. Extreme Networks, Inc.*, Case No. 4:17-cv-00079; *Plectrum LLC v. Facebook, Inc.*, Case No. 4:17-cv-00081; *Plectrum LLC v. Fortinet, Inc.*, Case No. 4:17-cv-00082; *Plectrum LLC v. Huawei Technologies USA, Inc.*, Case No. 4:17-cv-00083; *Plectrum LLC v. Juniper Networks, Inc.*, Case No. 4:17-cv-00084; *Plectrum LLC v. AT&T, Inc.*, Case No. 4:17-cv-00120; *Plectrum LLC v. Broadcom Corporation*, Case No. 4:17-cv-00121; *Plectrum LLC v. Comcast Corporation*, Case No. 4:17-cv-00123; *Plectrum LLC v. F5 Networks, Inc.*, Case No. 4:17-cv-00124; *Plectrum LLC v. NEC Corporation of America*, Case No. 4:17-cv-00125; *Plectrum LLC v. Verizon Communications, Inc.*, Case No. 4:17-cv-00126;

*Plectrum LLC v. Nokia USA, Inc.*, Case No. 4:17-cv-00140; and *Plectrum LLC v. Oracle Corporation*, Case No. 4:17-cv-00141. Paper 6, 2.

*C. The '951 Patent*

The '951 patent is entitled “High Speed Cache Management Unit for Use in a Bridge/Router,” and was filed as application No. 08/927,336 on September 11, 1997, and issued on November 2, 1999. Ex. 1001, [21], [22], [45], [54].

The '951 patent is directed to providing a network address cache. Ex. 1001, 1:23–31. The network address cache maintains hardware address and age tables, searches the address table for addresses received in network frames, and returns address search results, such as the destination port(s) for the received frame. *Id.* at 1:30–39. When a frame is received, the addresses in the frame are looked up, and the data associated with the cached addresses is returned in order to process the frame. *Id.* at 1:41–52.

Figure 2, reproduced below, depicts a block diagram illustrating a network interface module coupled to a motherboard via a backplane. Ex. 1001, 2:56–59.

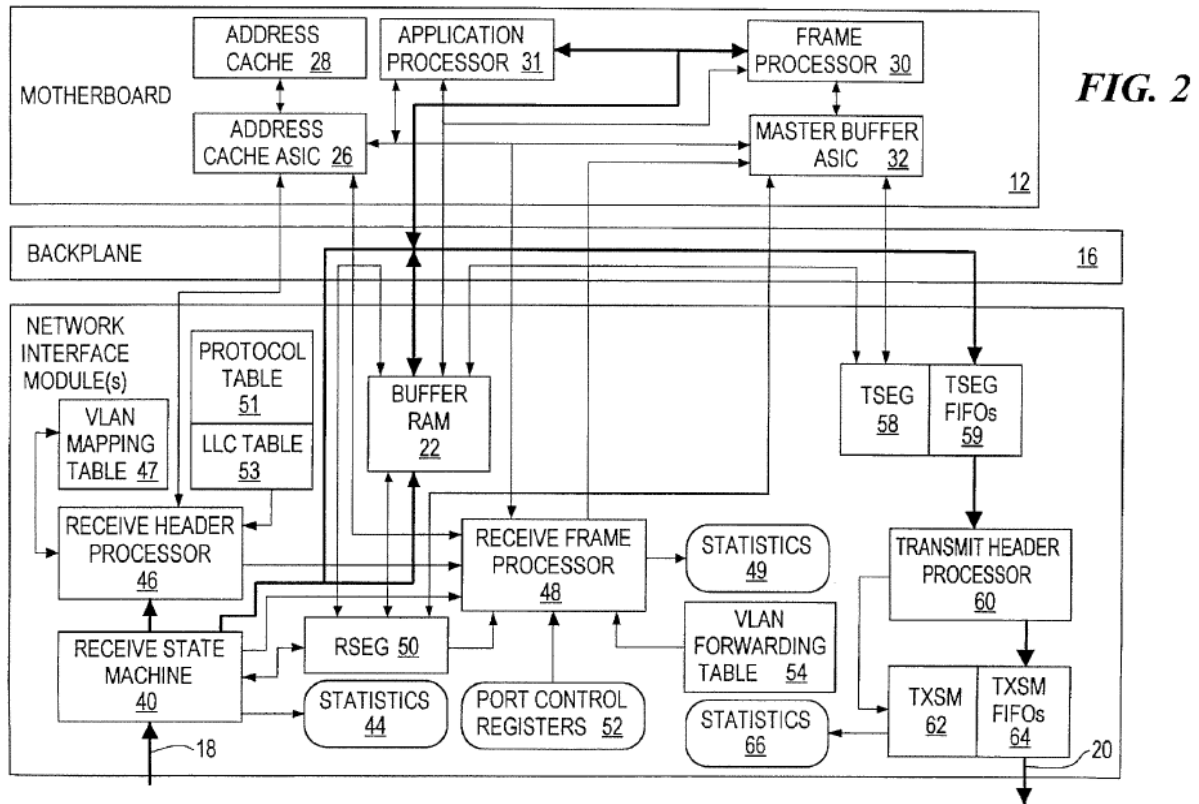


Figure 2, above, illustrates that the network interface module receives and sends data via input port 18 and output port 20, and when a frame is received, it is sent to receive header processor 46. Ex. 1001, 3:31–35, 3:61–64. Motherboard 12 includes address cache ASIC (“ACA”) 26, with associated cache 28, frame processor 30, application processor 31, and master buffer ASIC (“MBA”) 32. *Id.* at 3:57–60. Receive header processor 46 derives information from the header and passes that information to the ACA. *Id.* at 7:53–59. ACA 26 looks up addresses cached in associated cache 28. *Id.* at 4:20–21.

In an embodiment of the ’951 patent, cache 28 is a 4-way associative cache, where each row of the cache is associated with one entry from each of

the four sets. Ex. 1001, 5:14–17. Figure 4A, reproduced below, depicts the arrangement of cache 28.

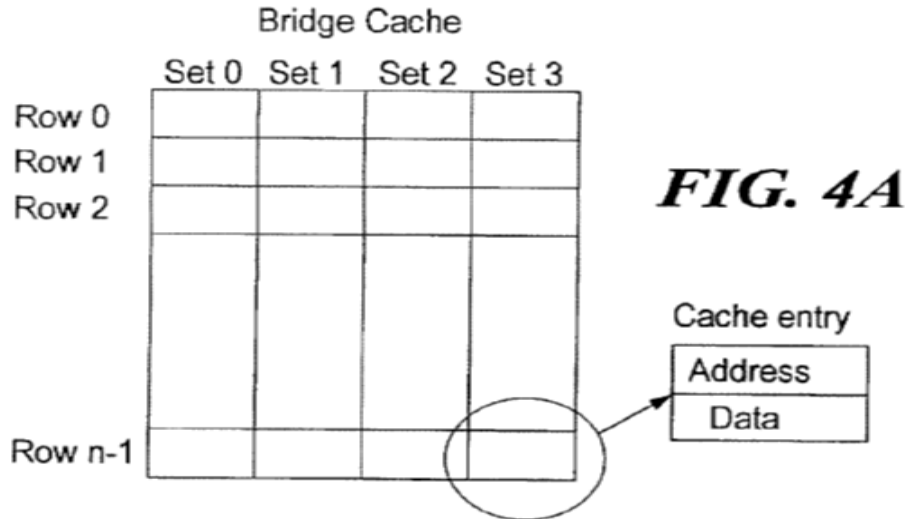


Figure 4A, above, illustrates the organization of a portion of cache 28. Ex. 1001, 2:64–65, 5:14–17. A cache lookup is started by the receipt of an address to be searched by the ACA. *Id.* at 5:25–27. A cyclic redundancy code (“CRC”) process is performed by a CRC engine on the address to generate a code, and the code is then used to identify a cache row. *Id.* at 5:27–31. The ACA uses an algorithm to identify a set order for address comparison, and a valid table is used for reference to identify if any of the sets are invalid. *Id.* at 5:30–34. A most likely valid set in the identified row is chosen, and the stored value is compared against the address from which the CRC is generated. *Id.* at 5: 34–37. If a match occurs, the associated data is returned, and if no match occurs, the next valid set in the row is selected and compared to the received address. *Id.* at 5:37–41. Upon a match, the frame is forwarded. *Id.* at 4:60–5:1.

Illustrative independent claims 1 and 8 are reproduced below.

1. A method for selecting an output port eligible to be used for transmission of a frame received at a computer network device, wherein said computer network device has at least one input port and a plurality of output ports and said received frame has a source address and a received destination address, said method comprising the steps of:

- receiving said frame at one of said at least one input port of said computer network device;

- parsing said received destination address from said received frame;

- processing said received destination address with a code generator to generate a coded address;

- comparing said coded address to a value associated with a row within said cache;

- in the event of a match between said coded address and said value associated with said row, comparing said received destination address with a cached destination address associated with a first entry in said row;

- in the event of a match between said received destination address and said cached destination address associated with said first entry, reading a port mask associated with said first entry to identify at least one port from said plurality of output ports which is eligible for transmission of said received frame.

8. A cache management unit of a data unit forwarding network device, comprising:

- an input register for receiving data unit header information including received source and destination address;

- a cyclic redundancy code (CRC) generator in communication with said input register for executing a CRC algorithm on each of said received source and destination addresses from said input register to form respective CRC encoded addresses;

- an input packetizer in communication with said CRC generator and said input register for formatting said CRC encoded



addresses and for receiving said received source and destination addresses from said input register;

a cache lookup unit and an associated cache in communication with said input packetizer for searching said cache with said formatted CRC encoded addresses;

an output packetizer in communication with said cache lookup unit for receiving and formatting retrieved source and destination address information from said cache; and

output register in communication with said output packetizer for receiving said formatted retrieved source and destination address information.

Ex. 1001, 16:22–45, 17:22–46.

## II. ANALYSIS

### *A. Real Parties-in-Interest*

The statute governing *inter partes* review proceedings sets forth certain requirements for a petition for *inter partes* review, including that “the petition identif[y] all real parties in interest.” 35 U.S.C. § 312(a); *see also* 37 C.F.R. § 42.8(b)(1) (requirement to identify real parties-in-interest in mandatory notices). In accordance with 35 U.S.C. § 312(a)(2) and 37 C.F.R. § 42.8(b)(1), Petitioner identifies Unified Patents Inc. as the sole real party-in-interest and “certifies that no other party exercised control or could exercise control over Unified’s participation in this proceeding, the filing of this petition, or the conduct of any ensuing trial.” Pet. 1. Petitioner provides verified Voluntary Interrogatory Responses (Ex. 1020) in support of the assertion that Unified is the sole real party-in-interest.

In its Response, Patent Owner argues the Petition should be denied because Petitioner fails to provide sufficient evidence to show that it has named all real parties-in-interest. *See* PO Resp. 8–15. More specifically, Patent Owner alleges that when sufficient evidence to the contrary is

provided by a patent owner, the ultimate burden of proof remains with petitioner to establish that it has identified all real parties in interest. *Id.* at 8–9 (citing *Jiawei Tech. Ltd. v. Simon Nicholas Richmond*, IPR2014-00935, slip op. at 5 (PTAB August 21, 2015) (Paper 52); *Corning Optical Comms. RF, LLC v. PPC Broadband, Inc.*, IPR2014-00440, slip op. at 5–6 (PTAB August 18, 2015) (Paper 68); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,759–60 (Aug. 14, 2012)).<sup>4</sup> Patent Owner contends that Petitioner’s primary source of revenue is from subscription fees or other payments made by its member companies, and these fees are paid are “expressly for the purpose of funding [Petitioner’s] defensive patent activities, such as filing IPR petitions.” *Id.* at 10 (citing Ex. 2003, 3–5, 8; Ex. 2005; Ex. 1020, 2). Patent Owner argues that Petitioner has no other source of revenue, and the members’ annual subscription fees “are in fact funding this IPR,” and these facts give rise to a strong inference that the Petitioner’s members have “implicitly authorized” the filing of this IPR. *Id.* at 12–13.

Patent Owner alleges that Petitioner’s purpose and business model is to undertake activities to serve the beneficial interests of its members in defending against patents. PO Resp. 10. Patent Owner references an early press release by Petitioner that indicates that Petitioner “aims to level the playing field” for companies that include Google, NetApp, and others. *Id.* (citing Ex. 2002). Patent Owner refers to Petitioner’s alleged “collaborative deterrent strategy” that is implemented in connection with its members. *Id.* Patent Owner refers to Petitioner’s strategy that uses “Micro-Pools” of

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<sup>4</sup> Evidentiary issues related to real parties-in-interest are discussed below in view of the more recent Federal Circuit case, *Worlds Inc. v. Bungie, Inc.*, 903 F. 3d 1237 (Fed. Cir. 2018).

member groups, in order to align deterrent solutions with its participating companies. *Id.* at 10–11. Patent Owner further alleges that Petitioner “has made clear that filing IPR Petitions is an important aspect of its collaborative defense strategy that it executes in coordination with and on behalf of its members.” *Id.* at 11. Patent Owner argues that Petitioner has no strategic technologies to sell, short of its defense services to its member technology members. *Id.* Patent Owner alleges that the member companies “would not agree to pay large annual subscription fees to [Petitioner] unless those companies saw [Petitioner’s] filing of IPR petitions as serving the technology companies’ interests.” *Id.* at 12.

Patent Owner also contends that Petitioner’s interrogatory responses (Ex. 1020) fail to establish that all real parties-in-interest have been named in the Petition because: (1) the interrogatories fail to address communications relating to the selection of the patent to challenge; (2) the statement that this IPR is not funded by members is limited to direct funding, but there must be indirect funding; and (3) the issue of whose beneficial interest being served is not addressed.<sup>5</sup> PO Resp. at 13–14.

Petitioner bears the burden of persuasion in establishing that all real parties in interest have been named. *See Worlds Inc.*, 903 F. 3d at 1241–1242. Petitioner’s identification of the real parties-in-interest is generally

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<sup>5</sup> The interrogatory responses were signed by Mr. Kevin Jakel, the CEO of Petitioner, Unified Patents Inc. *See* Ex. 1020. In its Response, Patent Owner indicated an intent to depose Mr. Jakel as part of its routine discovery, but there is no notice of that deposition in the record, and Patent Owner does not refer to any deposition testimony. *See* PO Resp. 13 n.2. Patent Owner also “reserve[d] its right to seek additional discovery on the real party-in-interest issue”; however, no related request for this discovery was made. *See id.*

accepted at the time of filing the petition, unless the patent owner produces “*some* evidence that tends to show that a particular third party should be named as a real party in interest . . . . A mere assertion that a third party is an unnamed real party in interest, without any support for that assertion, is insufficient to put the issue into dispute.” *Id.* at 1244.

“Determining whether a non-party is a ‘real party in interest’ demands a flexible approach that takes into account both equitable and practical considerations, with an eye toward determining whether the non-party is a clear beneficiary that has a preexisting, established relationship with the petitioner.” *Applications in Internet Time, LLC v. RPX Corp.*, 897 F.3d 1336, 1351 (Fed. Cir. 2018) (“*AIT*”). Whether a particular entity is a real party-in-interest is a “highly fact-dependent question” that is assessed “on a case-by-case basis.” Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,759 (Aug. 14, 2012) (citing *Taylor v. Sturgell*, 553 U.S. 880, 893–95 (2008)). While multiple factors may be relevant to the inquiry, “[a] common consideration is whether the non-party exercised or could have exercised control over a party’s participation in a proceeding.” *Id.*; *see also Zoll Lifecor Corp. v. Philips Elec. North Am. Corp.*, Case IPR2013–00609, slip op. at 10 (PTAB Mar. 20, 2014) (Paper 15). Relevant factors in the real parties-in-interest analysis include “Party A’s relationship with the petitioner; Party A’s relationship to the petition itself, including the nature and/or degree of involvement in the filing; and the nature of the entity filing the petition.” Trial Practice Guide, 48,760.

Patent Owner generally contends that Petitioner’s members are the intended beneficiaries of this *inter partes* review and their subscription fees have funded it. PO Resp. 8–12. Patent Owner provides no evidence, for

example, identifying any member entity that it alleges is controlling this particular proceeding, or a member that has financed, in whole or in part, this proceeding. *See id.*; *see also* Ex. 1020, 2–5. In *AIT*, the analysis of real parties-in-interest requires more than determining whether a party generally benefits from an *inter partes* review; *AIT* considered the ties between the filing entity and another party and the nature and degree of relationship between them and how that is relevant to the particular *inter partes* review. *See AIT*, 897 F.3d at 1339–1342, 1355–1358. The fact that members provide payment to Petitioner for a subscription to Petitioner’s services alone is insufficient to show that specific members are funding, directly or indirectly, this *inter partes* review. Based on the full record, the evidence is insufficient to support that Petitioner has requested this *inter partes* review proceeding on behalf of any particular member (*see* Ex. 1020 at 5), or to support that any of Petitioner’s members have had control over when and how Petitioner spent the revenue received from its members related to this proceeding (*see id.* at 2–3, 5). In sum, there is insufficient evidence that any specific member derives benefit from this proceeding.

Although the evidence demonstrates that Petitioner made decisions regarding this *inter partes* review proceeding, including which patent and claims to challenge, as discussed, there is insufficient evidence in the record that any particular member provided input regarding this proceeding, nor is there support that is contrary to Petitioner’s bearing the cost of this proceeding. *See* Ex. 1020 at 2–5. We acknowledge that the evidence shows Petitioner’s business is to “deter NPE litigation by protecting technology sectors.” *Id.* at 2; *see also* Ex. 2002; Ex. 2003, 3–5. And Petitioner does this by, at least in part, filing IPRs. *Id.* Thus, like in *ATI*, there is evidence

that Petitioner is not a traditional trade association, but a company seeking to protect its clients from patent risk in return for payment. *See* Ex. 1020 at 5 (stating that members pay a yearly subscription in return for Petitioner performing “NPE-deterrent activities”); Ex. 2002 (“Because companies only participate in (and pay for) those Micro-Pools they choose, Unified Patents tightly aligns its deterrent solution with its participating companies.”). However, unlike in *ATI*, we have no evidence tying Petitioner’s NPE-deterrent activities to any *particular* member interested in the outcome of this proceeding, such as a member that has been accused previously of patent infringement. From the evidence presented, we have insufficient information regarding whether Petitioner evaluated any of its member’s interests when determining whether to file IPR petitions, such that we could assess the likelihood of unnamed real parties-in-interest. Instead, we have here Patent Owner’s mere assertions that unnamed real parties-in-interest *might* exist. Accordingly, we find that Patent Owner has not produced evidence tending to show that any particular party should be named as a real party-in-interest. Based on our review of the evidence before us, including Petitioner’s verified interrogatory responses, Petitioner has demonstrated, by the preponderance of the evidence, that it is the sole real party-in-interest.

Thus, on the complete record before us, we find the evidence insufficient to support denial of the Petition for failure to name all real parties-in-interest.

*B. Level of Ordinary Skill in the Art*

Dr. Seshan testifies that a person of ordinary skill in the art for the ’951 patent would have been an electrical engineer or computer engineer having a bachelor’s degree and two years of experience in designing

network switching/routing hardware, or equivalent postgraduate education, such as a master’s degree focused in networking systems. Ex. 1007 ¶ 45; *see also* Pet. 16. Patent Owner does not provide alternative proposed qualifications for a person of skill in the art. *See* PO Resp. 1–16.

We adopt and apply the assessment of the level of ordinary skill in the art articulated by Petitioner to our obviousness analysis in this proceeding. In addition, we note that the art of record in this proceeding—namely, Cheriton, Kessler, and Jain—is indicative of the level of ordinary skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

### *C. Claim Construction*

Petitioner asserts that because the ’951 patent expired on September 11, 2017, a district court-type claim construction under *Phillips v. AWH Corp.* should be applied pursuant to 37 C.F.R. § 42.100. Pet. 18. With this, Petitioner asserts that the ordinary and customary meaning of the claim terms, as understood by one of ordinary skill at the time of the invention, should be applied. *Id.* Petitioner presents proposed constructions for the terms “code generator,” “coded address,” and “encoding.” *Id.* at 19–20. Patent Owner does not dispute the ’951 patent expiry date represented in the Petition, and does not present its own proposed constructions or dispute Petitioner’s proposed constructions of claim terms. PO Resp. 1–16.

We determine that it is not necessary to provide an express construction of any claim term for our analysis in this Final Written Decision. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”).

*D. Obviousness of Claims 1, 2, and 21 over Cheriton, Claims 3, 5, and 6 over Cheriton and Kessler, and Claims 4 and 22–24 over Cheriton, Kessler, and Jain*

Petitioner contends that independent claims 1, 2, and 21 are obvious over Cheriton, claims 3, 5, and 6 are obvious over Cheriton and Kessler, and claims 4 and 22–24 are obvious over Cheriton, Kessler, and Jain. Pet. 21–51; Pet. Supp. Reply 2–9. To support its contentions, Petitioner provides evidence and explanations as to how the prior art allegedly teaches each claim limitation. *Id.* Petitioner also relies upon the Seshan Declaration to support its positions. Ex. 1007. Patent Owner counters that the prior art does not render these claims obvious because the Petition provides only conclusory statements that lack support, and the prior art fails to teach some of the claim limitations. Prelim. Resp. 5–10.

On the complete record, we determine that Petitioner’s explanations and evidence are insufficient to support the obviousness grounds asserted under Cheriton for independent claims 1, 2, and 21, and also are insufficient for the obviousness grounds for dependent claims 3–6 and 22–24 under Cheriton in combination with other prior art. We begin our discussion with a brief summary of Cheriton, Kessler, and Jain, and then address the evidence, analysis, and arguments presented by the parties.

*1. Cheriton (Ex. 1002)*

Cheriton is directed to a network device that switches network traffic based upon network addresses. Ex. 1002, 1:20–22, 4:58–61. Cheriton discloses caching network addresses, with supporting hardware. *Id.* at 5:32–38. Figure 4, reproduced below, depicts a block diagram of Cheriton’s network switching device. *Id.* at 5:60–61.



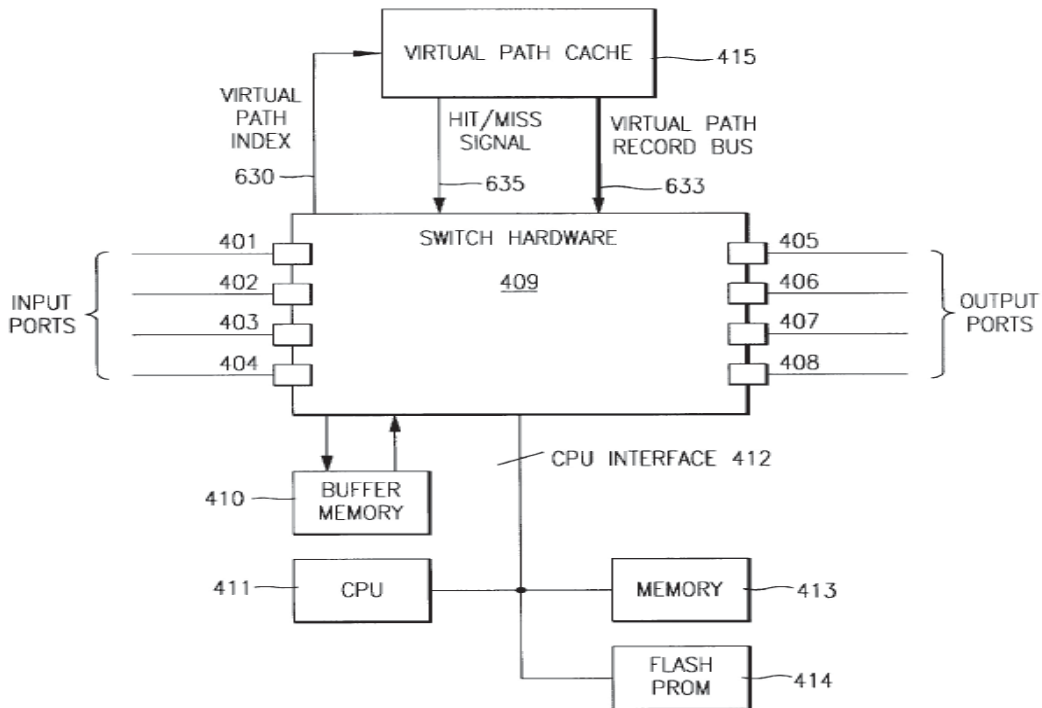


FIG. 4

As depicted in Figure 4, input ports 401–404 receive data, and switch hardware is used to decode the source and destination addresses and generates virtual path index 630. Ex. 1002, 5:32–34, 8:32–34, 10:41–45. Virtual path index 630 enters hash function 631 (shown in Figure 6), and a lookup for virtual path cache 415 is performed. *Id.* at 9:34–38, 10:42–45. Cheriton compares the received address against the stored tag fields, and the matching record is output. *Id.* at 9:38–43. The stored entry is used to identify a respective output port (404–408), on which the packet is to be transmitted, and switch hardware 409 forwards the data packet accordingly. *Id.* at 7:51–53, 10:57–59, Fig. 3.

## 2. Kessler (Ex. 1004)

Kessler is directed to implementations of set-associativity in cache memories. Ex. 1004, 131. Kessler discusses addressing the order of entries in a cache, and refers to a “MRU [most-recently-used] Approach” where

tags are examined in order from the most recently used to least recently used. *Id.* at 132. Entries that have been most recently accessed are stored in a list of entries referred to as an “MRU list per set.” *Id.*

### 3. *Jain (Ex. 1003)*

Jain is directed to data communications and recognizing local area network addresses. Ex. 1003, 2:3–4. A destination address list is used which contains a set of addresses that are compared to the destination address of received frames. *Id.* at 3:3–5, 5:58–61. A “hashing function generator is supplied to operate upon the received bit stream.” *Id.* at 5:58–6:1. In a preferred embodiment, “the hashing function generator is a Cyclic Redundancy Check [CRC] generator, although the teaching of the invention is not limited to only the use of a CRC technique.” *Id.* at 6:1–2. Jain discloses that the hash function generator may employ XOR methods, among other techniques. *Id.* at 6:2–4.

### 4. *Analysis*

Petitioner bears the burden of proving unpatentability of the challenged claims, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail on its challenges, Petitioner must demonstrate by a preponderance of the evidence that the challenged claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406

(2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.<sup>6</sup> *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Claim 1

Petitioner alleges that Cheriton teaches or suggests all the limitations of independent claim 1 in the view of one of ordinary skill in the art. Pet. 21–36. Petitioner contends that Cheriton teaches a method that selects an output port for transmission of a received frame. *Id.* at 24 (citing Ex. 1002, 7:17–21, 7:50–52, 9:4–20, Fig. 3; Ex. 1007 ¶ 67). Petitioner argues that Cheriton teaches a computer network device with input and output ports, which receives a frame at an input port, and parses a received destination address from a received frame. *Id.* at 25–27 (citing, *inter alia*, Ex. 1002, 6:8–11, 6:49–51, 8:24–26, 8:32–34, 9:34–36, 10:42–44, Figs. 2, 4; Ex. 1007 ¶¶ 70, 73, 75, 78, 79). Petitioner asserts that Cheriton teaches the claim 1 limitation “*processing said received destination address with a code generator to generate a coded address*” by its teaching of a hash function 632 that takes the destination and source addresses as input, and produces a hash output that is the virtual path cache index 632, as shown in Figure 7. *Id.* at 28–30 (citing Ex. 1002, 9:6–8, 9:34–38, 9:48–56, Fig. 7; Ex. 1007 ¶¶ 82–85). Petitioner argues that, even though Cheriton’s hash function uses both source and destination as inputs, Cheriton still meets the

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<sup>6</sup> Patent Owner does not present arguments or evidence of objective indicia of nonobviousness.

claim 1 limitation of processing a destination address because the limitation does not require processing using only a destination address. *Id.* at 29.

Petitioner alleges that Cheriton teaches the claim 1 limitation of “*comparing said coded address to a value associated with a row within a cache*” because Cheriton discloses that virtual path cache index 632 “is used to ‘look[] up the four parallel sets of the virtual path cache SRAMs 601 through 604.’” Pet. 30 (citing Ex. 1002, 9:34–38). Petitioner refers to Cheriton’s description of the virtual path cache index 632 for “index[ing] the four set associative virtual path cache 601 through 604,” and the virtual path index 632 is “further compared.” *Id.* (citing Ex. 1002, 10:46–50). Petitioner argues that “[t]o the extent *Cheriton* does not explicitly state that the lookup or indexing was done by comparing the virtual path cache index to a value associated with a row in the cache, it would have been obvious to a person of ordinary skill in the art to compare the virtual path cache index in such a fashion.” *Id.* Petitioner further alleges that “*Cheriton* would have compared the virtual path cache index to either the row number or cache offset associated with a row of data” because “[t]his comparison would have been necessary to retrieve the data from the row.” *Id.* at 30–31 (citing Ex. 1007 ¶ 88). Dr. Seshan repeats the same assertion, and testifies that “[s]uch an approach would have been nothing more than using a known technique (comparing an index value to an identifier value to determine if the identifier represents the desired row of cache) in a known way to implement a described function.” Ex. 1007 ¶ 88; *see also* Pet. 31.

In its Supplemental Reply, Petitioner argues that because the record demonstrates that it would have been obvious to use row-based SRAMs in Cheriton, “it would have it would have been obvious for Cheriton’s

disclosed actions on its disclosed data to have been used in row-based SRAMs.” Pet. Supp. Reply 1–2. Petitioner alleges that row-based SRAMs were well-known in the prior art, and Fujishima is a corroborative reference. *Id.* at 2–3 (citing Ex. 1007 ¶¶ 62–64; Ex. 1019, 5:38–44, 12:49–54).

Dr. Seshan testifies that Cheriton’s cache is organized as a 4-way associative cache, and one of ordinary skill would understand that this type of cache “would organize the sets as entries in a row.” Ex. 1007 ¶ 62 (citing Ex. 1019, 12:49–54). Dr. Seshan further testifies that “[t]he lookup index generated by the hash function is used to look up a row of four sets in the cache.” *Id.* (citing Ex. 1002, 9:34–38). Petitioner further argues that it was obvious for Cheriton’s SRAMs to have rows because: (1) row-based SRAMs were not just known, but were common; (2) it would have been obvious to try row-based SRAMs because there was a limited number of ways to arrange SRAM memory; (3) the use of row-based SRAMs would have been obvious as the application of a well-known technique; and (4) there was a high expectation of success with row-based SRAM solutions. Pet. Supp. Reply 3–5.

For the claim 1 limitation “*in the event of a match between said coded address and said value associated with said row, comparing said received destination address with a cached destination address associated with a first entry in said row,*” Petitioner argues that, “after the appropriate row in the SRAMs have been looked up,” the “tag field 310 from each set of SRAMs will be compared against the virtual path index 630.” Pet. 32 (citing Ex. 1002, 9:38–43). Petitioner refers to Figure 6 of Cheriton, citing that “virtual path index is further compared in parallel against the outputs from the four set associate cache 601 through 604 via the four comparators 611

through 614.” *Id.* (citing Ex. 1002, 10:49–52). Petitioner argues that in Cheriton, “tag field 310 has four subfields: the destination address field 411 . . . .” *Id.* at 33 (citing Ex. 1002, 7:24–26). Petitioner avers that “by comparing the tag field from the cache SRAM to the received virtual path index,” Cheriton discloses the “*comparing said received destination address with cached destination address associated with a first entry in said row*” limitation of claim 1. *Id.* In support, Dr. Seshan testifies that “[a]s shown in FIG. 6 of *Cheriton* within each SRAM the appropriate row is looked up and the cached virtual path record is output and is compared (using comparators 611–614) to the virtual path index.” Ex. 1007 ¶ 92. Dr. Seshan further testifies that:

*Cheriton* describes in the event of a *match between said coded address and said value associated with said row (i.e., once the virtual path cache index has looked up a cache row)*, comparing said received destination address (the destination address portion of the virtual path index) with a *cached destination address (the destination address subfield of the tag field) associated with a first entry in said row (stored in the first SRAM)*.

*Id.* ¶ 94 (emphasis added). Petitioner also argues that the cache address lookup described in the ’951 patent and its file history is the same as that described in Cheriton. Pet. Supp. Reply 7–8.

Patent Owner argues that Cheriton fails to teach the “row” limitations of the claims. Prelim. Resp. 6–9. Patent Owner asserts that “Cheriton does not once use the words ‘row’ or ‘rows’ to describe the organization of its cache.” *Id.* at 6. Patent Owner contends that “indexing in and of itself does not necessarily indicate the use of rows” because “data can be stored sequentially in blocks, instead of rows.” *Id.* at 7. Patent Owner also asserts that Fujishima, the reference used by Petitioner to allegedly represent the

understanding of one of ordinary skill in the art, does not disclose that all 4-set associative caches use rows, and cache memories can be organized by several methods, including tree structures. *Id.* at 7–8 (citing Ex. 1019, 12:49–54; Ex. 2001, 4:24–36, 7:24–41).

Patent Owner also argues that Petitioner fails to “sufficiently explain how *Cheriton*’s virtual path cache index is compared to a value associated with a row in the cache (claim 1) or used to ‘identify’ a row in the cache or any entry in a cache row (claims 2 and 21).” Prelim. Resp. 8. Patent Owner asserts that, in addition to Petitioner assuming that *Cheriton*’s cache has rows, Petitioner assumes that any “indexing” or “looking up” in *Cheriton* “is done relative to cache rows.” *Id.* At the oral hearing, Patent Owner argued that in *Cheriton*, parallel comparison of entries in four SRAMs is taught, but not the claimed method of going to a row in a cache and first checking the first elements in row. Tr. 24:10–19. Patent Owner further alleges that Petitioner’s conclusory statements, and its expert’s testimony that merely repeats the Petition’s arguments, fail to explain how limitations are taught by the prior art. Prelim. Resp. 7–9.

Petitioner clarified at the oral hearing that it does not assert that *Cheriton* explicitly discloses row-based SRAMs. Tr. 8:19–21. We concur with Petitioner’s clarification—all of the references to *Cheriton* in the Petition and Dr. Seshan’s testimony do not identify a teaching or suggestion of the use of any row-based SRAM in *Cheriton*. *See* Pet. 30–31; Ex. 1007 ¶¶ 87–89. Rather, in its Supplemental Reply and at oral argument, Petitioner bases its arguments on the alleged known use of rows in SRAMs in the view of one of ordinary skill in the art, contending that it would be obvious to

implement Cheriton in that configuration. *See* Pet. Supp. Reply 1–5; Tr. 9:23–10:5, 10:24–11:2.

Having considered the complete trial record, we determine that Petitioner has failed to sufficiently demonstrate that Cheriton teaches or suggests all the limitations of claim 1.

More specifically, we are not persuaded by Petitioner’s arguments that Cheriton teaches or suggests the claim 1 limitations of “*comparing*” a “*coded address to a value associated with a row*” or “*in the event of a match between*” the “*coded address and said value associated with the row,*” “*comparing*” the “*received destination address with a cached destination address associated with a first entry in said row.*” Petitioner’s expert, Dr. Seshan, testifies that Cheriton’s cache is a 4-set associative cache and a person of ordinary skill would understand that this type of associative cache “would organize the sets as entries in a row,” with Fujishima referred to for corroboration. *See* Ex. 1007 ¶ 62. We do not find, however, that Fujishima serves as corroborating evidence to support Dr. Seshan’s opinion, because although Fujishima uses a 4-way set associative cache, which may be organized in rows, it does not teach or suggest that all 4-way set associative caches would be organized in rows. *See* Ex. 1007 ¶ 62; Ex. 1019, 11:49–54, 12:49–54.

In any event, even if we were to assume, based on Dr. Seshan’s testimony, that Cheriton’s SRAMs are organized by rows, Petitioner’s arguments and evidence are insufficient to support that Cheriton teaches or suggests the claim 1 limitation of “*comparing*” a “*coded address to a value associated with a row within said cache.*” Cheriton describes the use of a



hash function 631 that produces a virtual patch cache index 632 as depicted in Figure 7, reproduced below. Ex. 1002, 9:34–37.

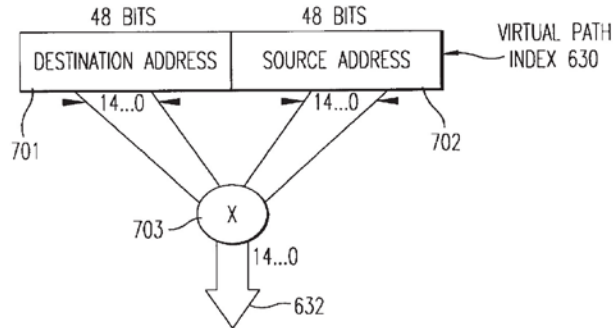


FIG. 7

The virtual patch cache index 632, produced by hashing as depicted in Figure 7 above, “looks up the four parallel sets of the virtual path cache SRAMs 601 through 604,” as depicted in Figure 6 of Cheriton, reproduced below. Ex. 1002, 9:34–38.

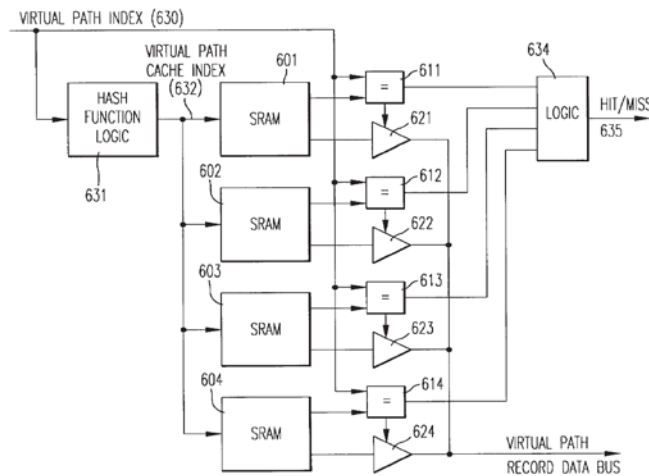


FIG. 6

Although, as depicted in Figure 6 above and described in Cheriton, “four parallel sets of the virtual path cache SRAMs 601 through 604” are looked up, there are no teachings or suggestions in Cheriton identified by Petitioner where, even if the SRAMs are organized by rows, there is a comparison of a

coded address [Cheriton’s virtual path cache index] to a “value associated with a row.” *See* Pet. 30–31 (citing Ex. 1002, 9:34–38). Petitioner alleges that it would have been obvious to one of ordinary skill in the art to compare the virtual path cache index to a value associated with a row in the cache, and this approach would have been “nothing more than using a known technique” “in a known way to implement a described function.” *Id.* (citing Ex. 1002, 10:47–49; Ex. 1007 ¶ 88). In support, Dr. Seshan testifies that “[i]n order to index into the cache, Cheriton would have compared the virtual path cache index to either the row number or cache offset associated with a row of data,” and then Dr. Seshan circularly alleges that this “comparison would have been necessary to retrieve the data from a row.” Ex. 1007 ¶ 88. Dr. Seshan testifies that this approach would have been using a known technique in a known way to implement the described function. *Id.*

There is no evidence provided to support Petitioner’s arguments because, even if it would have been obvious to use row-based SRAMs in Cheriton, it does not necessarily follow that the claimed method step directed to the specific claimed actions would be obvious based only upon the use of a row structure. *See* Pet. 30–31. As discussed above, claim 1’s “comparing” limitation requires a specific method of indexing a cache by comparing a coded address to a value associated with a row. Although Cheriton discloses that virtual path cache SRAMs 601 through 604 are looked up as depicted in Figure 6, even if the SRAMs of Cheriton are organized by rows, there is no disclosure that this is done by *comparing the coded address with a value associated with a row within a particular cache [a specific SRAM]*. Petitioner appears to acknowledge that Cheriton does

not teach or suggest this limitation, and instead refers to the use of comparison of a coded address to a value associated with a row as a known technique that could be implemented in a known way for the described function. However, Dr. Seshan’s testimony that this method of “comparison would have been necessary to retrieve the data from a row,” is not explained and is conclusory, as is Dr. Seshan’s testimony that one of ordinary skill would view the modifications to Cheriton’s teachings as only a substitution of a known technique.<sup>7</sup> *See* Ex. 1007 ¶ 88. Accordingly, we afford little weight to Dr. Seshan’s opinions on this limitation. *See* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”). Moreover, Petitioner must provide documentary evidence to support its proposed modifications to Cheriton because the claimed step of comparing a coded address with a value associated with a row is “more than a peripheral issue” and “therefore requires a core factual finding.” *See K/S HIMPP v. Hear-Wear Techs., LLC*, 751 F.3d 1362, 1365 (Fed. Cir. 2014).

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<sup>7</sup> At the oral hearing, Petitioner provided new and additional arguments on alleged “routine substitution” in comparison with Fujishima. *See* Tr. 38–40; *Dell, Inc. v. Acceleron, LLC*, 818 F.3d 1293, 1301 (Fed. Cir. 2016). As noted at the hearing, some of the associated demonstratives do not reflect evidence of record (*id.*), but, in any event, Petitioner’s arguments extend beyond the teachings of Cheriton, as well as the understanding of one of skill in the art as reflected in the testimony of Dr. Seshan, and there is an absence of explanations with supporting rationale underpinnings provided by Petitioner to alternatively modify Cheriton’s teachings based upon Fujishima’s teachings. Thus, even if we considered the untimely and improperly presented new arguments, the lack of evidentiary support persuades us that Petitioner has not met its burden.

In its Supplemental Reply, Petitioner also alleges that there are similarities in “address-based lookup” discussed in the ’951 patent, and its file history, with Cheriton, and such similarities support the teaching of the “comparison” step of claim 1. Pet. Supp. Reply 7–8. We do not find Petitioner’s argument persuasive. The ’951 patent and its file history describe the use of hash [coded address] for indexing to select a particular desired *row* having plural entries; in contrast, as discussed above, there is no teaching or suggestion of a comparison to select a row with entries in Cheriton. *Compare* Ex. 1002, 5:47–50 *with* Ex. 1017, 5.

We also do not find Petitioner’s arguments and evidence sufficiently support that Cheriton teaches or suggests the claim 1 limitation of “*comparing*” the “*received destination address with a cached destination address associated with a first entry in said row.*”

Petitioner asserts that this claim limitation is taught by Cheriton “by comparing the tag field from the cache SRAM to the received virtual path index,” where the “virtual path index 630 [] is the source-destination address pair of the incoming datagram.” Pet. 33 (citing Ex. 1002, 7:24–26, 9:33–34). Dr. Seshan testifies that, based on Figure 6 of Cheriton, “the appropriate row is looked up and the cached virtual path record is output and is compared (using comparators 611–614) to the virtual path index. Thus, each of the plural entries in the row (the entry in each SRAM) is compared in parallel.” Ex. 1007 ¶ 92. Dr. Seshan then testifies: “Cheriton describes . . . comparing said received destination address (the destination address portion of the virtual path index) with a cached destination address (the destination address subfield of the tag field) associated with a first entry in said row (stored in the first SRAM).” *Id.* ¶ 94.

Figure 3, reproduced below, is an illustration of a virtual path record data structure, with a virtual path record stored in SRAM[s], such as those shown, for instance, in Figure 6. See Ex. 1002, 5:32–37, 5:58, 8:24–29, 9:38–42.

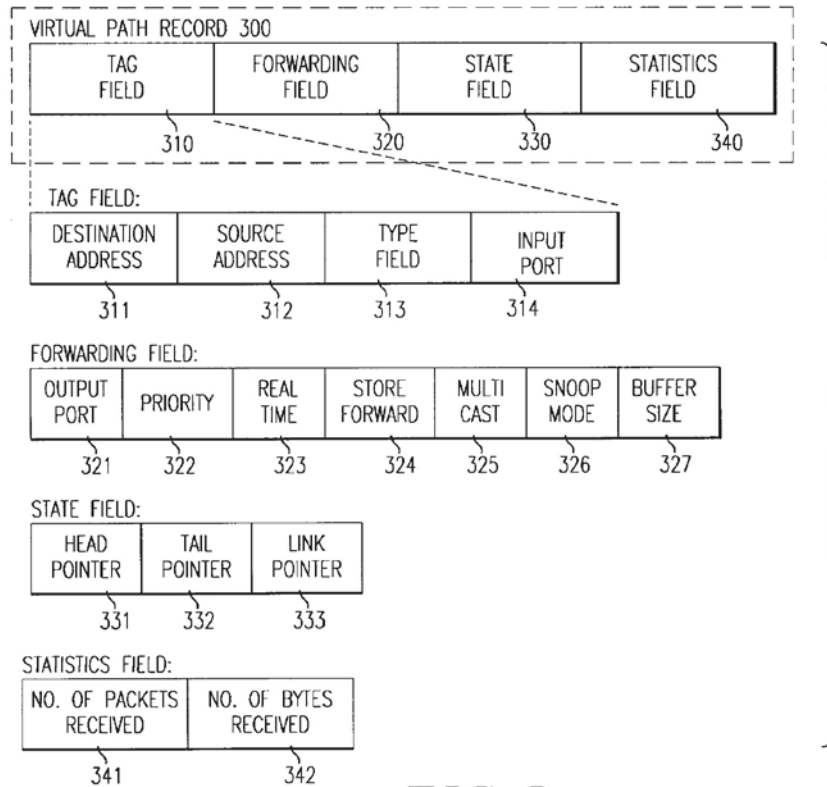


FIG. 3

As depicted in Figure 3 above, and as further described in Cheriton, tag field 310 is used to match an incoming datagram packet against a virtual path record. Ex. 1002, 7:23–27. Although tag field 310 may be represented as the first portion of data in a virtual path record, Cheriton does not disclose that a tag field would be associated with the first *entry* [the first virtual path record] in a row of the cache.<sup>8</sup> Dr. Seshan testifies that a cached destination

<sup>8</sup> Petitioner makes an alternative argument that different data elements such as fields, and specifically tag fields, could be considered an “entry” under

address [tag field] is associated with “a first entry in said row (stored in the first SRAM).” Ex. 1007 ¶ 94. However, there is no explanation provided for why an entry stored in a first SRAM would be the *first entry in a row* in that particular SRAM or why a row would be organized with a first SRAM entry as the *first entry in a row*. Absent an identification of underlying evidence supporting Dr. Seshan’s testimony, which concerns an issue that is more than peripheral, we find the evidence provided by Petitioner for the teaching of this limitation to be insufficient. *See* 37 C.F.R. § 42.65(a); *K/S HIMPP*, 751 F.3d at 1365.

Thus, based on the complete record before us, we determine that Petitioner has not shown by a preponderance of the evidence that claim 1 is unpatentable as obvious over Cheriton.

*Claim 2*

Independent claim 2 recites the limitations “*using said received, encoded address information to identify one of said cache rows,*” and “*retrieving first address information from a first entry of said identified row.*” Ex. 1001, 16:54–57. In the Petition, Petitioner relies on essentially the same evidence for claim 2 as that identified to support the alleged obviousness based on Cheriton of the similar claim 1 limitations of “*comparing*” a “*coded address to a value associated with a row*” and “*comparing*” the “*received destination address with a cached destination address associated with a first entry in said row.*” *Compare* Pet. 39–41, *with id.* at 30–33; *see also* Pet. Supp. Reply 6, 8.

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claims 2 and 21. *See* Pet. Supp. Reply 5–6. We address this alternative argument under the “Claim 21” subsection below.

For the same reasons we did not find Petitioner’s arguments and evidence sufficient to show that Cheriton teaches or suggests similar limitations in claim 1, we also find Cheriton’s teachings or suggestions are insufficient to teach the limitations of claim 2 referred to above. We additionally determine that Petitioner fails to provide sufficient evidence to demonstrate that Cheriton teaches or suggests the claim 2 limitation of “*a cache comprised of plural rows, each having plural respective entries,*” in the view of one of ordinary skill in the art for the reasons we discuss for a similar limitation of claim 21 below.

Thus, based on the complete record before us, we determine that Petitioner has not shown by a preponderance of the evidence that claim 2 is unpatentable as obvious over Cheriton.

Claim 21

Independent claim 21 recites the limitations of “*a cache having plural rows, each of said rows having plural entries, wherein each of said entries has an address and is comprised of a first value and a second value.*” Ex. 1001, 18:55–58. For Cheriton’s alleged teaching of this claim 21 limitation, Petitioner refers to the arguments and evidence provided for claim 2, which recites “*a cache comprised of plural rows, each having plural respective entries*” in its preamble. Pet. 45 (citing Pet. 37–38; Ex. 1007 ¶ 137). More specifically, the Petition alleges Cheriton is a 4-set associative cache, and that by Cheriton’s lookup of “*the four parallel sets of the virtual path cache SRAMs 601 through 604,*” the four parallel sets would be looked up using the same index address, and would form “*a single cache row with plural entries (i.e., one entry per set within the row accessed via the index address).*” *Id.* at 37–38 (citing Ex. 1002, 9:29–30, 9:36–38; Ex. 1007 ¶ 105).

Dr. Seshan's testimony is essentially identical to the analysis in the Petition, and Dr. Seshan concludes that "*Cheriton* discloses a cache comprised of plural rows (the rows indexed by the index address), each having plural respective entries (the four parallel sets)." Ex. 1007 ¶¶ 105–106. In its Supplemental Reply, Petitioner also refers to Dr. Seshan's testimony, which states that based on Fujishima, one of ordinary skill in the art would understand that a 4-set associative cache "would organize the sets as entries in a row." Pet Supp. Reply 5 (citing Ex. 1007 ¶ 62; Ex. 1019, 12:49–54). Patent Owner argues, and we agree, the referenced portion of Fujishima does not support that all 4-way associative caches use rows, and, moreover, we do not discern that the referenced portion of Fujishima discloses organizing entries from different SRAMs in a row. *See* Prelim. Resp. 7; Ex. 1019, 12:49–52.

We do not find sufficient evidence to support Petitioner's assertion that, with *Cheriton*'s lookup of the four parallel sets of virtual path cache SRAMs, any entries selected from the respective SRAMs would then be organized as individual entries on a single row, as claim 21 requires. We find Dr. Seshan's testimony to be conclusory, and absent an identification of underlying facts supporting Dr. Seshan's conclusions, concerning an issue that is more than peripheral in nature, we find the evidence provided by Petitioner for the teaching of this limitation to be insufficient. *See* 37 C.F.R. § 42.65(a); *K/S HIMPP*, 751 F.3d at 1365.

In its Supplemental Reply, Petitioner additionally argues that the data elements, including fields such as a tag field, as shown in Figure 3 of *Cheriton*, would also be "entries," and multiple entries would be stored in a row when using row-based SRAMs. Pet. Supp. Reply 5–6. However, the



evidence of record supports that under Cheriton, the respective fields are part of the data structure of the virtual path records. *See* Ex. 1002, 5:58, 7:10–21. And contrary to Petitioner’s argument on this issue, Dr. Seshan testifies that “[e]ach *entry* in the *Cheriton* cache consists of a virtual path record that is written into the virtual path cache,” and each virtual path record contains a tag field and forwarding field. Ex. 1007 ¶¶ 139–140 (citing Ex. 1002, 7:17–20, 9:18–20); *see also* Pet. 45. In light of Dr. Seshan’s testimony, which is that “entries” as claimed are the entire virtual path record of Cheriton, we are not persuaded by Petitioner’s argument that Cheriton’s “tag fields” elements of virtual path records should be considered “entries” under claims 2 and 21.

Thus, based on the complete record before us, we determine that Petitioner has not shown by a preponderance of the evidence that claim 21 is unpatentable as obvious over Cheriton.

*Dependent Claims 3, 5, and 6*

Claims 3, 5, and 6 depend directly or indirectly from claim 2. Ex. 1001, 16:66–17:5, 17:9–15. Petitioner contends that claims 3, 5, and 6 are obvious over Cheriton and Kessler. Pet. 51–56. The additional evidence presented in the Petition for dependent claims 3, 5, and 6 is directed only to the limitations of the dependent claims, and does not remedy the Petition’s failure to sufficiently demonstrate the obviousness of independent claim 2. *See id.* at 51–56; Pet. Supp. Resp. 9.

In light of the insufficiency of the evidence to demonstrate that claim 2 is obvious over Cheriton, there is also insufficient evidence to demonstrate the obviousness of dependent claims 3, 5, and 6.

*Dependent Claims 4 and 22–24*

Claim 4 depends indirectly from claim 2, and claims 22–24 depend directly or indirectly from claim 21. Ex. 1001, 17:6–8, 19:8–20:6. Petitioner contends that claims 4 and 22–24 are obvious over Cheriton, Kessler, and Jain. Pet. 57–62. The additional evidence presented in the Petition for dependent claims 4 and 22–24 is directed only to the limitations of the dependent claims, and does not remedy the Petition’s failure to sufficiently demonstrate the obviousness of independent claims 2 or 21. *See* Pet. 58–62; Pet. Supp. Resp. 9.

In light of the insufficiency of the evidence to demonstrate that claims 2 and 21 are obvious over Cheriton, there is also insufficient evidence to demonstrate the obviousness of dependent claims 4 and 22–24.

*Conclusion*

Accordingly, based on the complete record before us, we determine that Petitioner has not shown by a preponderance of the evidence that claims 1, 2, and 21 are obvious over Cheriton, that claims 3, 5, and 6 are obvious over Cheriton and Kessler, or that claims 4 and 22–24 are obvious over Cheriton, Kessler, and Jain.

*E. Obviousness of Claims 8 and 11–14 over Cheriton and Jain*

Petitioner contends that independent claim 8 and dependent claims 11–14 are obvious over Cheriton and Jain. Pet. 62–71; Pet. Supp. Reply 2–9. To support its contentions, Petitioner provides evidence and explanations as to how the prior art allegedly teaches each claim limitation. *Id.* Petitioner also relies upon the Seshan Declaration to support its positions. Ex. 1007. Patent Owner counters that the prior art does not render these claims obvious because the Petition provides only conclusory

statements that lack support, the Petition fails to adequately explain a rationale to combine Cheriton and Jain, and the prior art fails to teach some limitations of the claims. PO Resp. 1–8.

On the complete record, we determine that Petitioner’s explanations and evidence in support of the obviousness ground relying on Cheriton and Jain for claims 8 and 11 are sufficient but Petitioner’s explanations and evidence in support of the obviousness ground based on Cheriton and Jain for claims 12–14 are not sufficient. We address the evidence, analysis, and arguments presented by the parties below.

*1. Analysis*

*Claim 8*

Petitioner asserts, and we agree, that Cheriton in combination with Jain discloses a cache management unit with an input register for receiving data unit header information including received source and destination address. Pet. 62–63 (citing Ex. 1007 ¶ 192). More specifically, Petitioner refers to Cheriton’s teaching of a datagram arriving through network ports, which has a datagram packet header that has source and destination fields, as well as other header information, which are stored in a portion of shared buffer memory, i.e., an input register. *Id.* at 63 (citing Ex. 1002, 6:49–53, 8:32–36; Ex. 1007, ¶¶ 194–195). Petitioner argues, and we agree, that it would have been obvious to use CRC hashing and the CRC generator of Jain in the XOR-based hashing and hashing functions of Cheriton. *Id.* at 58–60, 64 (citing Ex. 1002, 9:48–51; Ex. 1003, 6:1–2; Ex. 1007 ¶¶ 176–177, 181, 197). Petitioner contends, and we agree, that Cheriton in view of Jain teaches executing a CRC algorithm on the received source and destination addresses, and forming CRC encoded addresses. *Id.* at 64. Petitioner also

contends, and we agree, that the CRC generator of Jain produces 32-bit values and the virtual path cache of Cheriton uses a 15-bit index value, so one of ordinary skill in the art would have formatted the output of Jain to conform to Cheriton. *Id.* at 65 (citing Ex. 1002, 9:55–56; Ex. 1003, 6:9; Ex. 1007 ¶ 200). Petitioner avers, and we agree, that Cheriton teaches the use of an input packetizer (hash function logic of Cheriton) in communication with Jain’s CRC generator and with formatting of CRC encoded addresses. *Id.* at 65–66 (citing Ex. 1007 ¶ 201).

Petitioner further alleges, and we agree, that Cheriton teaches the claim 8 limitation of a “cache lookup unit” by its use of comparators and with tri-state buffers receiving the source and destination address information and formatting for placement onto a data bus. Pet. 67 (citing Ex. 1002, 10:52–56; Ex. 1007 ¶ 207). Petitioner asserts, and we agree, that Cheriton’s tri-state buffer and/or data bus interface circuitry serve as an output packetizer that communicates with the cache lookup unit and for formatting. *Id.* at 67–68 (citing Ex. 1007 ¶¶ 208–209). Petitioner further argues, and we agree, that Cheriton discloses the use of an output register for receiving formatted source and destination address information. *Id.* at 68–69 (citing Ex. 1007 ¶¶ 211–212).

Petitioner alleges that one of ordinary skill in the art would have found it obvious to combine the teachings of Cheriton and Jain because Cheriton discloses that alternative hashing functions may be employed in its invention, Jain teaches that the CRC-based hashing function is an alternative to the XOR-based hashing function of Cheriton, and “[s]uch a combination would be nothing more than the routine substitution of one known element for another known element, with both elements performing their known and

well-understood function.” *Id.* at 58 (citing Ex. 1002, 9:48–51; Ex. 1007 ¶ 177). Dr. Seshan testifies that “Jain thus describes, as an alternative to an XOR-based hashing function, the use of a CRC hashing function in hashing a network address.” Ex. 1007 ¶¶ 174–175 (citing Ex. 1003, 3:3–5, 5:58–6:4, 6:7–9); *see also* Pet. 58.

Having considered the complete record now before us, we determine that Petitioner has provided sufficient evidentiary support that the combination of Cheriton and Jain teaches each and every limitation of claim 8, and also has provided sufficient rationale for combining the teachings of Cheriton and Jain.

Patent Owner argues that the Petition fails to adequately explain how Cheriton and Jain teach the use of an input packetizer and output packetizer of claim 8. PO Resp. 7–8. Patent Owner alleges that the Petition “does not identify how any of the hash function logic, the tri-state buffer, or the data bus interface circuitry of Cheriton” packetizes or identifies something that is packetized. *Id.* at 7. Patent Owner also argues that Dr. Seshan’s testimony is conclusory. *Id.* at 7–8.

As discussed above, Petitioner maps the hash function logic of Cheriton, modified in view of Jain, to the “input packetizer.” Pet. 64–66 (citing Ex. 1002, 9:34–38, 9:55–56; Ex. 1003, 6:9; Ex. 1007 ¶¶ 199–201). Petitioner refers to cited portions of Cheriton and Jain to support how the data is modified by the hash tag logic. *See id.* Petitioner maps Cheriton’s tri-state buffer and data bus interface circuitry, which formats source and destination address information for placement onto the data bus, as the “output packetizer,” alleging also that one of ordinary skill in the art would understand that, depending on the bus, additional signaling might be

required for output to the bus. *Id.* at 67–68 (citing Ex. 1002, 10:52–56; Ex. 1007 ¶¶ 207–209).

We do not find persuasive Patent Owner’s arguments that the Petition’s support for Cheriton’s teachings of input and output “packetizers” is insufficient. The ’951 patent does not require that its “packets” be in a specialized form. The ’951 patent refers to units of information or data transmitted between devices or components, and “packetizing” refers to the assembly of units of the information and data. *See e.g.*, Ex. 1001, 1:42–46, 4:20–32, 7:45–50, 7:56–58, 8:11–16, 8:29–35, 9:16–18. For instance, for the “input packetizer,” the ’951 patent describes information is “strip[ped] . . . out of the received frame,” the NIC “creates a packet to be sent,” and “a packet” is constructed with “the SA [source address], DA [destination address], and protocol ID derived from the received frame.” *See* Ex. 1001, 7:45–50, 7:56–58. For the output packetizer, the ’951 patent explains “[t]he ACA collects the results from each of the SA and DA lookups, packages them in an output packet, and sends them.” *Id.* at 9:16–18. As discussed above, the Petition refers to Cheriton’s components that reformat and assemble information and data as the input and output “packetizers,” with Dr. Seshan providing supporting testimony. Cheriton’s teachings are consistent with the “packetizing” performed in the ’951 patent. Additionally, Patent Owner provides no arguments for alternative interpretations of “packetizing,” nor does Patent Owner present expert testimony concerning how a person of ordinary skill in the art would have understood packetizing or Cheriton’s teachings differently from the evidence presented by Petitioner.

Patent Owner also argues that, although Petitioner argues that Cheriton states that other hash functions can be used and Jain allegedly describes that CRC hashing is an alternative to XOR-based hashing where this “may suggest that it would have been *possible* for one of ordinary skill in the art to use Jain’s CRC hashing in place of hash function logic,” Petitioner fails to address how and why one of skill would have replaced Cheriton’s hash logic or why this would have been a routine substitution. PO Resp. 5–7.

Jain states that “[i]n a presently preferred embodiment of the invention the hashing function is a CRC generator;” however, “the invention is not limited to only the use the use of a CRC technique . . . For example, the hash function generator may employ specific bits of the destination address, a correlation of address bits, checksums, or XOR folding.” Ex. 1003, 6:1–4. Dr. Seshan testifies that “*Jain* describes the use of a CRC hashing function as an alternative to the use of XOR-based hashing for hashing a network address,” and “*Cheriton* itself notes that the XOR function ‘is used for illustration only’ and that ‘it will be apparent to anyone skilled in the art that other hash functions from the one shown can be used.’” Ex. 1007 ¶ 176 (citing Ex. 1002, 9:48–51). Dr. Seshan testifies that the use of Jain’s CRC hashing in Cheriton would have been a routine substitution with the elements using their known and well-understood functions, which is “particularly true in light of Cheriton’s explicit note that alternative hash functions might be employed, and Jain’s explicit teaching that a CRC-based hashing function is an alternative to an XOR-based hashing function.” *Id.* ¶ 177.

Contrary to Patent Owner’s arguments, Petitioner presents, as summarized above, a persuasive rationale for substitution of Jain’s CRC-based hashing for Cheriton’s XOR-based hashing function. Dr. Seshan’s supporting testimony is unrebutted by expert testimony from Patent Owner or any contrary evidence. *See* Tr. 15:20–16:13. Additionally, Dr. Seshan’s testimony is supported by evidence of record—that is, Jain’s description of CRC-based hashing and XOR-based hashing as alternative options, and Cheriton’s use of XOR-hashing but with indication that other hashing options may be acceptably employed. *See* Ex. 1002, 9:48–51; Ex. 1003, 6:1–4.

Therefore, based on the complete record before us, we determine that Petitioner has shown by a preponderance of the evidence that claim 8 is unpatentable as obvious over Cheriton and Jain.

*Claim 11*

Claim 11 depends from claim 8, and additionally claims “*wherein said cache lookup unit comprises a cache lookup controller for searching said cache with said formatted CRC encoded addresses.*” Ex. 1001, 17:55–58. The Petition refers to the supporting evidence provided for the teaching of the claim 8 limitation of the “cache lookup unit,” which refers to Cheriton’s disclosures relating to “look[ing] up” and searching caches. Pet. 69 (citing Pet. 66; Ex. 1002, 9:34–38, 10:46–49; Ex. 1007 ¶¶ 204–205, 215–216). We have reviewed Petitioner’s explanations and supporting evidence regarding dependent claim 11, and find they sufficiently support that Cheriton teaches all the claim 11 limitations. Patent Owner provides no additional arguments for claim 11, except those discussed for base



independent claim 8, which we have not found persuasive for the reasons discussed above. PO Resp. 5–8.

Therefore, based on the complete record before us, we determine that Petitioner has shown by a preponderance of the evidence that claim 11 is unpatentable as obvious over Cheriton and Jain.

Claims 12–14

Claim 12 recites “[t]he cache management unit of claim 8, wherein said cache is provided as plural rows each having plural entries, each entry comprising an address value and an associated data value;” claim 13 recites “[t]he cache management unit of claim 12, wherein said cache lookup controller is adapted for identifying a row of said cache using said CRC encoded addresses;” and claim 14 recites “[t]he cache management unit of claim 12, wherein said cache lookup controller is adapted for comparing one of said received source and destination addresses to said address value of at least one of said plural entries of said identified cache row.” Ex. 1001, 17:59–18:5.

For claim 12, the limitation of “*plural rows each having plural entries*” and for claim 14, the limitation of “*at least one of the plural entries of said identified cache row,*” are similar to the claim 21 limitation of “*a cache having plural rows, each of said rows having plural entries.*” For the alleged teachings of this claim limitation, the Petition relies upon the teachings of Cheriton only and the same evidence as that provided by Petitioner as allegedly teaching the similar limitation of claim 21. See Pet. 38, 45, 69–71; Pet. Supp. Reply 9. For the same reasons discussed for the deficiencies of the teachings of the “plural entries” limitation of claim 21, discussed *supra* Section II.D, we also determine that the evidence and

arguments provided by Petitioner are insufficient to support the prior art teaching of the similar limitations of claims 12 and 14.

The limitation of claim 13, for the “*cache lookup controller [] adapted for identifying a row of said cache,*” is similar to claim 2’s limitation of “*using . . . address information to identify one of said cache rows,*” and Petitioner relies upon the same evidence in Cheriton for the teachings of the respective limitations. *See* Pet. 39, 70. For the same reasons discussed for the deficiencies of the teachings for identification of the “row” limitations of claims 1 and 2, discussed *supra* Section II.D, we also determine that the evidence and arguments provided in the Petition are insufficient to support the prior art teaching of the similar limitation of claim 13.

Therefore, based on the complete record before us, we determine that Petitioner has not shown, by a preponderance of the evidence, that claims 12–14 are unpatentable as obvious over Cheriton and Jain.

### Conclusion

Accordingly, based on the complete record before us, we determine that Petitioner has shown by a preponderance of the evidence that claims 8 and 11 would have been obvious over Cheriton and Jain but Petitioner has not shown by a preponderance of the evidence that claims 12–14 would have been obvious over Cheriton and Jain.

### III. CONSTITUTIONALITY ISSUE

Patent Owner objects to the constitutionality of this *inter partes* review. PO Resp. 15 (citing *Oil States Energy Services, LLC v. Greene’s Energy Group, LLC*, No. 16-712 (U.S. Nov. 23, 2016, cert. granted June 12, 2017)). However, on April 24, 2018, the U.S. Supreme Court held that

“inter partes review does not violate Article III or the Seventh Amendment” of the Constitution. *Oil States Energy Servcs., LLC v. Greene’s Energy Grp., LLC*, 138 S. Ct.1365 (2018). Therefore, Patent Owner’s argument, which refers only to the reasons presented in *Oil States*, is moot.

#### IV. CONCLUSION

For the foregoing reasons, Petitioner has demonstrated by a preponderance of the evidence that claims 8 and 11 of the ’951 patent are unpatentable as obvious over Cheriton and Jain, but has not demonstrated by a preponderance of the evidence that claims 1, 2, and 21 of the ’951 patent are unpatentable as obvious over Cheriton, that claims 3, 5, and 6 are unpatentable as obvious over Cheriton and Kessler, that claims 4 and 22–26 are unpatentable as obvious over Cheriton, Kessler, and Jain, or that claims 12–14 are unpatentable as obvious over Cheriton and Jain.

#### V. ORDER

Accordingly, it is:

ORDERED that claims 8 and 11 of the ’951 patent have been shown to be unpatentable;

FURTHER ORDERED that claims 1–6, 12–14, and 21–24 of the ’951 patent have not been shown to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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