

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNIFIED PATENT INC.,
Petitioner

v.

PLECTRUM LLC,
Patent Owner

IPR2017-01430
Patent 5,978,951

Before KEN B. BARRETT, MIRIAM L. QUINN, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

McSHANE, *Administrative Patent Judge*.

DECISION

Partial Institution of *Inter Partes* Review
35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

Unified Patents Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–6, 8, 11–14, and 21–24 (“the challenged claims”) of U.S. Patent No. 5,978,951 (Ex. 1001, “the ’951 patent”) pursuant to 35 U.S.C. §§ 311–319. Paper 3 (“Pet.”). Plectrum LLC (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 7 (“Prelim. Resp.”).

We have authority under 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” See 37 C.F.R. § 42.4(a) (“The Board institutes the trial on behalf of the Director.”).

We determine that Petitioner has demonstrated that there is a reasonable likelihood that it would prevail with respect to at least one challenged claim. For the reasons described below, we institute an *inter partes* review of claims 8 and 11 of the ’951 patent.

B. Related Proceedings

Patent Owner indicates that related matters are these Eastern District of Texas district court cases: *Plectrum LLC v. Arista Networks, Inc.*, Case No. 4:17-cv-00076; *Plectrum LLC v. Brocade Communications Systems, Inc.*, Case No. 4:17-cv-00077; *Plectrum LLC v. Extreme Networks, Inc.*, Case No. 4:17-cv-00079; *Plectrum LLC v. Facebook, Inc.*, Case No. 4:17-cv-00081; *Plectrum LLC v. Fortinet, Inc.*, Case No. 4:17-cv-00082; *Plectrum LLC v. Huawei Technologies USA, Inc.*, Case No. 4:17-cv-00083; *Plectrum LLC v. Juniper Networks, Inc.*, Case No. 4:17-cv-00084; *Plectrum*

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LLC v. AT&T, Inc., Case No. 4:17-cv-00120; *Plectrum LLC v. Broadcom Corporation*, Case No. 4:17-cv-00121; *Plectrum LLC v. Comcast Corporation*, Case No. 4:17-cv-00123; *Plectrum LLC v. F5 Networks, Inc.*, Case No. 4:17-cv-00124; *Plectrum LLC v. NEC Corporation of America*, Case No. 4:17-cv-00125; *Plectrum LLC v. Verizon Communications, Inc.*, Case No. 4:17-cv-00126; *Plectrum LLC v. Nokia USA, Inc.*, Case No. 4:17-cv-00140; and *Plectrum LLC v. Oracle Corporation*, Case No. 4:17-cv-00141. Paper 6, 2.

C. The '951 Patent

The '951 patent is titled “High Speed Cache Management Unit for Use in a Bridge/Router,” and was filed as application No. 08/927,336 on September 11, 1997, and issued on November 2, 1999. Ex. 1001, [21], [22], [45], [54].

The '951 patent is directed to providing a network address cache. Ex. 1001, 1:23–31. The network address cache maintains hardware address and age tables, searches the address table for addresses received in network frames, and returns address search results, such as the destination port(s) for the received frame. *Id.* at 1:30–39. When a frame is received, the addresses in the frame are looked up, and the data associated with the cached addresses is returned in order to process the frame. *Id.* at 1:41–52.

Figure 2, reproduced below, depicts a block diagram illustrating a network interface module coupled to a motherboard via a backplane. Ex. 1001, 2:56–59.

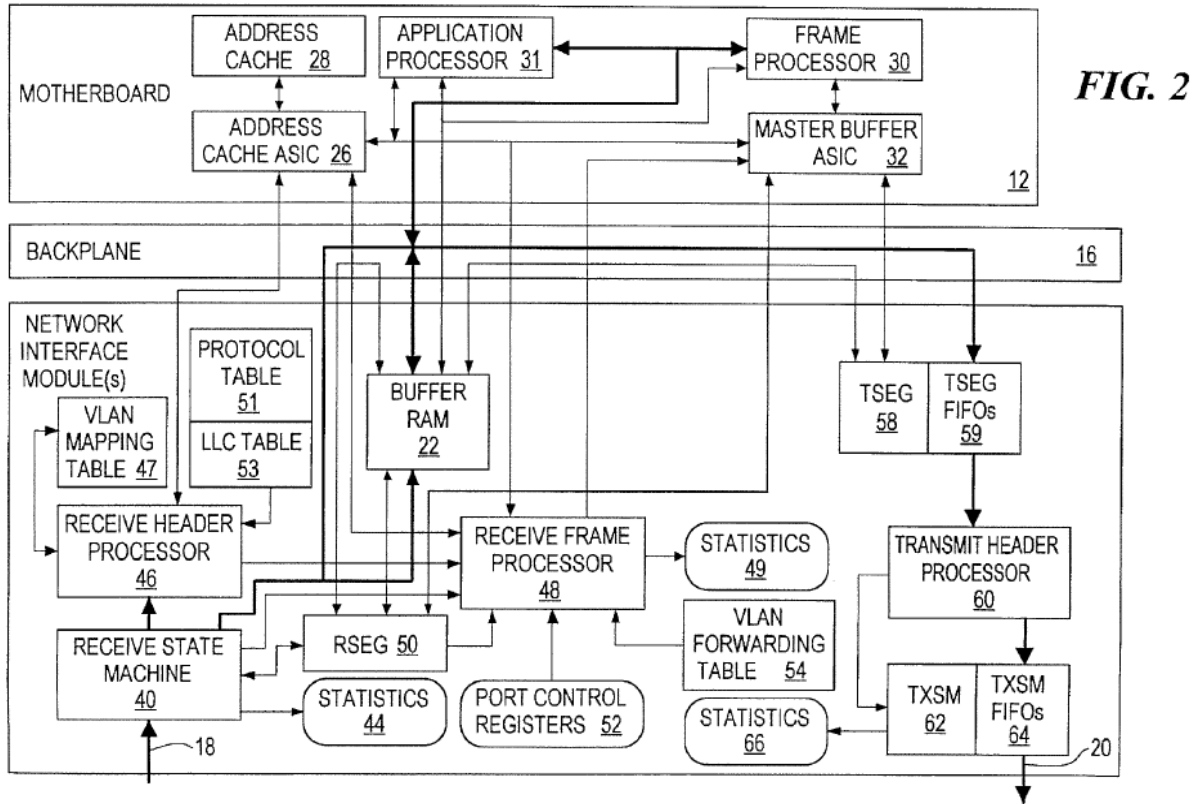


Figure 2, above, illustrates that the network interface module receives and sends data via input port 18 and output port 20, and when a frame is received, it is sent to receive header processor 46. Ex. 1001, 3:31–35, 3:61–64. Motherboard 12 includes address cache ASIC (“ACA”) 26, with associated cache 28, frame processor 30, application processor 31, and master buffer ASIC (“MBA”) 32. *Id.* at 3:57–60. Receive header processor 46 derives information from the header and passes that information to the ACA. *Id.* at 7:53–59. ACA 26 looks up addresses cached in associated cache 28. *Id.* at 4:20–21.

In an embodiment of the ’951 patent, cache 28 is a 4-way associative cache, where each row of cache is associated with one entry from each of the

four sets. Ex. 1001, 5:14–17. Figure 4A, reproduced below, depicts the arrangement of cache 28.

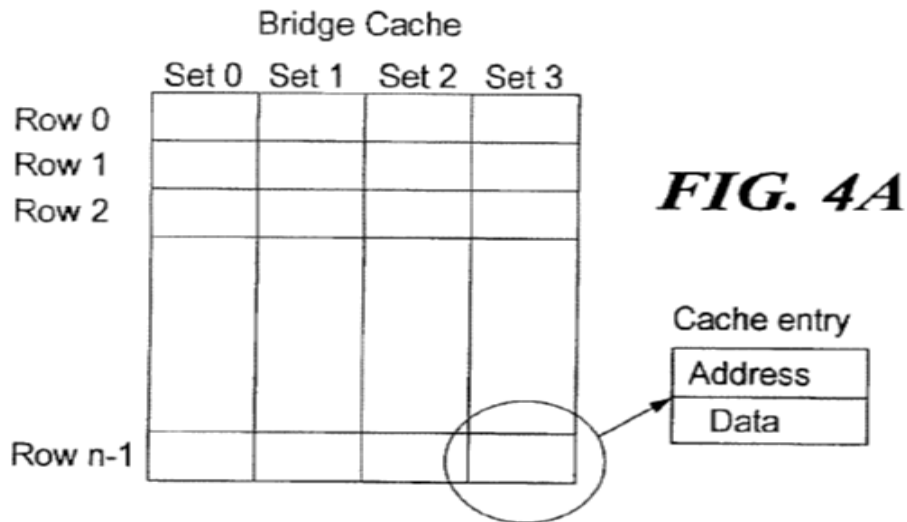


Figure 4A, above, illustrates the organization of a portion of cache 28. Ex. 1001, 2:64–65, 5:14–17. A cache lookup is started by the receipt of an address to be searched by the ACA. *Id.* at 5:25–27. A cyclic redundancy code (“CRC”) process is performed by a CRC engine on the address to generate a code, and the code is then used to identify a cache row. *Id.* at 5:27–31. The ACA uses an algorithm to identify a set order for address comparison, and a valid table is used for reference to identify if any of the sets are invalid. *Id.* at 5:30–34. A most likely valid set in the identified row is chosen, and the stored value is compared against the address from which the CRC is generated. *Id.* at 5: 34–37. If a match occurs, the associated data is returned, and if no match occurs, the next valid set in the row is selected and compared to the received address. *Id.* at 5:37–41. Upon a match, the frame is forwarded. *Id.* at 4:60–5:1.

Illustrative independent claims 1 and 8 are reproduced below.

1. A method for selecting an output port eligible to be used for transmission of a frame received at a computer network device,

wherein said computer network device has at least one input port and a plurality of output ports and said received frame has a source address and a received destination address, said method comprising the steps of:

receiving said frame at one of said at least one input port of said computer network device;

parsing said received destination address from said received frame;

processing said received destination address with a code generator to generate a coded address;

comparing said coded address to a value associated with a row within said cache;

in the event of a match between said coded address and said value associated with said row, comparing said received destination address with a cached destination address associated with a first entry in said row;

in the event of a match between said received destination address and said cached destination address associated with said first entry, reading a port mask associated with said first entry to identify at least one port from said plurality of output ports which is eligible for transmission of said received frame.

8. A cache management unit of a data unit forwarding network device, comprising:

an input register for receiving data unit header information including received source and destination address;

a cyclic redundancy code (CRC) generator in communication with said input register for executing a CRC algorithm on each of said received source and destination addresses from said input register to form respective CRC encoded addresses;

an input packetizer in communication with said CRC generator and said input register for formatting said CRC encoded addresses and for receiving said received source and destination addresses from said input register;

a cache lookup unit and an associated cache in communication with said input packetizer for searching said cache with said formatted CRC encoded addresses;

an output packetizer in communication with said cache lookup unit for receiving and formatting retrieved source and destination address information from said cache; and

output register in communication with said output packetizer for receiving said formatted retrieved source and destination address information.

Ex. 1001, 16:22–45; 17:22–46.

D. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability against the claims of the '951 patent:

Claims	Ground	Prior Art
1, 2, and 21	§ 103	Cheriton ¹
3, 5, and 6	§ 103	Cheriton and Kessler ²
4 and 22–24	§ 103	Cheriton, Kessler, and Jain ³
8 and 11–14	§ 103	Cheriton and Jain

Pet. 21–71.

¹ U.S. Patent No. 6,091,725 (issued July 18, 2000) (Ex. 1002).

² R.E. Kessler, *Inexpensive Implementations of Set-Associativity*, ACM SIGARCH COMPUTER ARCHITECTURE NEWS – SPECIAL ISSUE: PROCEEDINGS OF THE 16TH ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, 17:3, 131–139 (June 1989) (Ex. 1004). Petitioner provides a stamped copy of the portion of the Proceedings (Ex. 1005), and a declaration attesting to the authenticity of the document and its public availability. Ex. 1006.

³ European Patent Application No. 0 522 743 A1 (published January 13, 1993) (Ex. 1003).

II. ANALYSIS

A. *Real Parties-in-Interest*

The statute governing *inter partes* review proceedings sets forth certain requirements for a petition for *inter partes* review, including that “the petition identif[y] all real parties in interest.” 35 U.S.C. § 312(a); *see also* 37 C.F.R. § 42.8(b)(1) (requirement to identify real parties-in-interest in mandatory notices). In accordance with 35 U.S.C. § 312(a)(2) and 37 C.F.R. § 42.8(b)(1), Petitioner identifies Unified Patents Inc. as the sole real party-in-interest and “certifies that no other party exercised control or could exercise control over Unified’s participation in this proceeding, the filing of this petition, or the conduct of any ensuing trial.” Pet. 1. Petitioner provides Voluntary Interrogatory Responses (Ex. 1020) in support of the assertion that Unified is the sole real party-in-interest.

In its Preliminary Response, Patent Owner argues the Petition should be denied because Petitioner fails to identify other real parties-in-interest. *See* Prelim. Resp. 17–23. More specifically, Patent Owner alleges that Petitioner’s primary source of revenue is from subscription fees or other payments made by its member companies, and these fees are paid “expressly for the purpose of funding [Petitioner’s] defensive patent activities, such as filing IPR petitions.” *Id.* at 19 (citing Ex. 2003, 4; Ex. 2005). Patent Owner argues that Petitioner has no other source of revenue, so “third-party members are in fact funding this IPR,” and the facts give rise to a strong inference that the Petitioner’s members have “implicitly authorized” the filing of this IPR. *Id.* at 19, 21–22. Patent Owner also contends that the Petitioner’s interrogatory responses (Ex. 1020), fail to establish that all real parties-in-interest have been named in the Petition because: (1) the

interrogatories fail to address communications relating to the selection of the patent to challenge; (2) the statement that this IPR is not funded by members is limited to direct funding, but there must be indirect funding; and (3) the issue of whose beneficial interest being served is not addressed. *Id.* at 22–23.

Whether a particular entity is a real party-in-interest is a “highly fact-dependent question” that is assessed “on a case-by-case basis.” Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,759 (Aug. 14, 2012) (citing *Taylor v. Sturgell*, 553 U.S. 880, 893–95 (2008)). While multiple factors may be relevant to the inquiry, “[a] common consideration is whether the non-party exercised or could have exercised control over a party’s participation in a proceeding.” *Id.*; see also *Zoll Lifecor Corp. v. Philips Elec. North Am. Corp.*, Case IPR2013–00609, slip op. at 10 (PTAB Mar. 20, 2014) (Paper 15).

Patent Owner provides no evidence that any other entity actually is controlling this particular proceeding, or is providing direct financing for this particular proceeding. Ex. 1020, 2–5. The mere fact that members provide payment to Petitioner for a subscription to Petitioner’s services alone is insufficient to show that these members are funding this particular *inter partes* review. The evidence does not show an obligation on Petitioner’s part to file *inter partes* review proceedings on behalf of any member in return for payment (*see id.* at 5), nor does it show that Petitioner’s members have any control over when and how Petitioner spends the revenue received from its members (*see id.* at 2–3, 5). Instead, the evidence shows that Petitioner makes all decisions regarding any *inter partes* review proceeding, including which patents to challenge, *without*

input from its members, and that Petitioner alone bears all costs of any such proceeding. *See id.* at 2–5.

We have considered the parties’ arguments and, on the record before us and for purposes of this Decision, we are not persuaded that the Petition should be denied for failure to name all real parties-in-interest.

B. Unconstitutionality of Inter Partes Reviews

Patent Owner objects to the use of *inter partes* reviews as unconstitutional based, at least, upon the reasons presented in the petition for certiorari that was granted in *Oil States Energy Services, LLC v. Greene’s Energy Group, LLC* and asserts that institution should be denied on this basis. Prelim. Resp. 24; *see Oil States Energy Services LLC v. Greene’s Energy Group, LLC*, No. 16-712, 137 S. Ct. 2293, 2017 WL 2507340 (June 12, 2017).

Patent Owner’s arguments relate to the constitutionality of *inter partes* review generally. At this time, no court has found *inter partes* review unconstitutional, and we are bound by Federal Circuit precedent. *MCM Portfolio LLC v. Hewlett-Packard Co.*, 812 F.3d 1284 (Fed. Cir. 2015), *cert. denied*, – U.S. –, 137 S.Ct. 292 (2016). *Oil States* is before the U.S. Supreme Court, and Patent Owner’s arguments as to denial of this Petition on this basis are premature.

C. Claim Construction

Petitioner asserts that because the ’951 patent expired on September 11, 2017, a district court-type claim construction under *Phillips v. AWH Corp.* should be applied pursuant to 37 C.F.R. § 42.100. Pet. 18. With this, Petitioner asserts that the ordinary and customary meaning of the claim terms, as understood by one of ordinary skill at the time of the invention,

should be applied. *Id.* Petitioner presents proposed construction for the terms “code generator,” “coded address,” and “encoding.” *Id.* at 19–20. Patent Owner does not dispute the ’951 patent expiry date represented in the Petition, and does not present its own proposed constructions or dispute Petitioner’s proposed constructions of claim terms. Prelim. Resp. 1–24.

At this time, we determine that it is not necessary to provide an express construction of any term of the claims. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”). Under a district court-type standard, and absent any special definitions, terms are given “the meaning that [a] term would have to a person of ordinary skill in the art in question at the time of the invention.” *Phillips*, 415 F.3d at 1316. Herein, we give claim terms their ordinary and customary meaning, as they would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

D. Alleged Obviousness of Claims 1, 2, and 21 over Cheriton

Petitioner contends that claims 1, 2, and 21 are obvious over Cheriton. Pet. 21–51. To support its contentions, Petitioner provides evidence and explanations as to how the prior art teaches each claim limitation. *Id.* Petitioner also relies upon the Declaration of Dr. Srinivasan Seshan (“Seshan Declaration” (Ex. 1007)) to support its positions. Patent Owner counters that the prior art does not render claims 1, 2, and 21 obvious because the Petition provides only conclusory statements that lack support, and the prior art fails to teach some limitations of the claims. Prelim. Resp. 5–10.

On this record, we are not persuaded by Petitioner’s explanations and evidence in support of the obviousness grounds asserted under Cheriton for claims 1, 2, and 21. We begin our discussion with a brief summary of Cheriton, and then address the evidence, analysis, and arguments presented by the parties.

1. Cheriton (Ex. 1002)

Cheriton is directed to a network device that switches network traffic based upon network addresses. Ex. 1002, 1:20–22, 4:58–61. Cheriton discloses caching network addresses, with supporting hardware. *Id.* at 5:32–38. Figure 4, reproduced below, depicts a block diagram of Cheriton’s network switching device. *Id.* at 5:60–61.

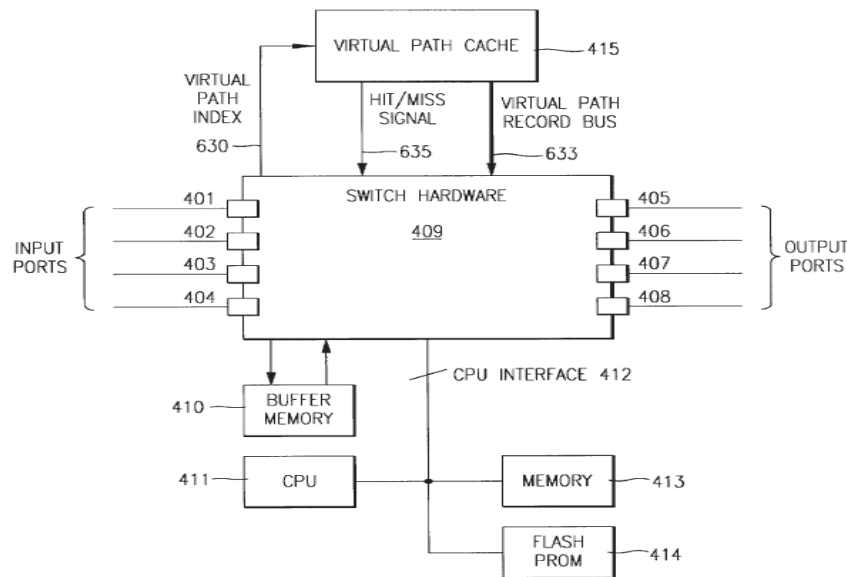


FIG. 4

As depicted in Figure 4, input ports 401–404 receive data, and switch hardware is used to decode the source and destination addresses and generates virtual path index 630. Ex. 1002, 5:32–34, 8:32–34, 10:41–45. Virtual path index 630 enters hash function 631 (shown in Figure 6), and a lookup for virtual path cache 415 is performed. *Id.* at 9:34–38, 10:42–45.

Cheriton compares the received address against the stored tag fields, and the matching record is output. *Id.* at 9:38–43. The stored entry is used to identify a respective output port (404–408), on which the packet is to be transmitted, and switch hardware 409 forwards the data packet accordingly. *Id.* at 7:51–53, 10:57–59, Fig. 3.

2. Analysis

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art;⁴ and (4) objective evidence of nonobviousness.⁵ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Petitioner alleges that Cheriton teaches all the elements of claim 1, 2, and 21. Pet. 21–51. In particular, Petitioner alleges that Cheriton teaches the claim 1 limitations of “comparing said coded address to a value associated with a row within a cache” and “comparing said received destination address with a cached destination address associated with a first entry in said row;” the claim 2 limitations of “a network element having a

⁴ Petitioner proposes an assessment of the level of ordinary skill in the art. Pet. 16; *see* Ex. 1007 ¶ 45. Patent Owner does not propose any required qualifications. Prelim. Resp. 1–24. At this juncture, we adopt Petitioner’s proposed qualifications.

⁵ There is no objective indicia of nonobviousness yet in the record.

cache comprised of plural rows,” “using said received, encoded address information to identify one of said cache rows,” and “retrieving first address information from a first entry of said identified row;” and the claim 21 limitation of “a cache having plural rows, each of said rows having plural entries,” in the view of one of skill in the art. *Id.* at 30–33, 37–40, 45.

Patent Owner argues that Cheriton fails to teach the “row” limitations of the claims. Prelim. Resp. 6–9. Patent Owner asserts that “Cheriton does not once use the words ‘row’ or ‘rows’ to describe the organization of its cache.” *Id.* at 6. Patent Owner contends that Cheriton’s indexing across four SRAM memories and organization, as a 4-set associative cache, does not teach the use of rows of data because data can be stored sequentially in blocks, instead of rows. *Id.* at 7. Patent Owner also asserts that Fujishima, a reference used by Petition to allegedly represent the understanding of one of ordinary skill in the art, does not disclose that all 4-set associative caches use rows, and cache memories can be organized by several methods, including tree structures. *Id.* at 7–8 (citing Ex. 1019, 12:49–54; Ex. 2001, 4:24–36, 7:24–41). Patent Owner also alleges that Petitioner’s conclusory statements, and its expert’s testimony, do not explain how the limitations are taught by the prior art and also fail meet Petitioner’s burden to demonstrate inherency. *Id.* at 7–9.

We find that the Petition lacks an adequate explanation of how Cheriton teaches a comparison of values associated with a row in a cache, which is necessary to determine that the Petition shows a reasonable likelihood of prevailing on the obviousness challenge based on Cheriton. Petitioner, and its expert, assert that Cheriton’s cache is searched by rows, but, we find that Cheriton does not support this assertion. *See* Pet. 30 (citing

Ex. 1002, 10:49–50; Ex. 1007 ¶ 87). Although Petitioner refers to Cheriton’s disclosure of 4-way associative cache use to “look[] up the four parallel sets of virtual path SRAMs” (Pet. 30), there is no disclosure that caches in Cheriton are organized by row. Cheriton’s index, at best, searches four SRAMs (601–604). *See* Ex. 1002, Fig. 6. This is not enough.

Cheriton, does not teach or suggest that searching the four memories is accomplished by comparing values in a row within the cache, as recited in the claims. Petitioner provides only a conclusory unsupported statements that values associated with a row are compared in Cheriton. *See* Pet. 30.

Petitioner then alleges that “[t]o the extent Cheriton does not explicitly state that the lookup or indexing was done by comparing the virtual path cache index to a value associated with a row in the cache” that “it would have been obvious to a person of ordinary skill in the art to compare the virtual path cache index in such a fashion.” Pet. 30. In support, Petitioner’s expert states that “Cheriton would have compared the virtual path cache index to either the row number or cache offset associated with a row of data” in indexing the cache. Ex. 1007 ¶ 88. This testimony is conclusory because it fails to provide any explanation as to why the indexing would be done in this manner. The expert also testifies that using this approach, “would have been nothing more than using a known technique” “in a known way to implement a described function,” but fails to provide the rationale as to why one of skill in the art would have implemented Cheriton in this manner. *See* Pet. 30. Petitioner’s reference to Fujishima also fails to demonstrate that it was known to one of skill in the art that caches, such as those in Cheriton, would have to use rows. Fujishima, at best, demonstrates that there could be row organization used in 4-set associative caches, but,

again, there is no rationale provided why Cheriton does have or would have rows. *See id.* at 23 (citing Ex. 1007 ¶ 62; Ex. 1019, 12:49–54).

Similarly, for the claim 1 limitation of “in the event of a match . . . comparing said received destination address with a cached destination address associated with a first entry in said row,” and the claim 2 limitation of “retrieving first address information from a first entry of said identified row,” Petitioner fails to provide a sufficiently supported rationale as to why Cheriton teaches that an address is associated with a “first entry in a row.” *See* Pet. 33, 40–41. We are not persuaded by Petitioner’s general and factually unsupported assertion that Cheriton’s SRAM has rows, for the reasons discussed above. And there is no factual support provided for Petitioner expert’s conclusory opinion that the “first entry in said row” would be the data that is used for comparison in Cheriton. *See* Ex. 1007 ¶¶ 94, 120. Accordingly, we find the expert’s opinions unpersuasive. *See* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *see also Rohm and Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092 (Fed. Cir. 1997). Additionally, absent an underlying factual basis to support Petitioner’s proposed modification to Cheriton, Petitioner’s arguments amount to “mere conclusory statements” that cannot support an obviousness rejection. *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (2006)).

Therefore, based on the record before us, Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 1, 2, and 21 would have been obvious over Cheriton.

D. Alleged Obviousness of Claims 3, 5, and 6 over Cheriton and Kessler

Petitioner contends that claims 3, 5, and 6 are obvious over Cheriton and Kessler. Pet. 51–56. Claims 3, 5, and 6 depend directly or indirectly from claim 2. Ex. 1001, 16:66–17:5, 17:9–15. As discussed above for the ground based on Cheriton, Petitioner has not shown sufficiently that Cheriton teaches the limitations of claim 2. Petitioner does not allege that Kessler teaches the limitations of claim 2, but rather relies upon Kessler to teach some of the additional limitations recited in the dependent claims. *See* Pet. 51–56. In light of Petitioner’s failure to demonstrate a reasonable likelihood of prevailing on its assertion that claim 2 would have been obvious over Cheriton, the obviousness ground that challenges dependent claims 3, 5, and 6 also fails.

Therefore, based on the record before us, Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 3, 5, and 6 would have been obvious over Cheriton and Kessler.

E. Alleged Obviousness of Claims 4 and 22–24 over Cheriton, Kessler, and Jain

Petitioner contends that claims 4 and 22–24 are obvious over Cheriton, Kessler, and Jain. Pet. 57–62. Claim 4 depends indirectly from claim 2, and claims 22–24 depend directly or indirectly from claim 21. Ex. 1001, 17:6–8, 19:8–20:6. As discussed above for the ground based solely on Cheriton, Petitioner has not shown sufficiently that Cheriton teaches the limitations of independent claims 2 and 21. Petitioner does not allege that the additional references of Kessler or Jain teach the limitations of claims 2 and 21, but rather relies upon Kessler and Jain to teach some of the additional limitations recited in the dependent claims. *See* Pet. 57–62. In light of Petitioner’s failure to demonstrate a reasonable likelihood of

prevailing on its assertion that claims 2 and 21 are obvious over Cheriton, the obviousness ground that challenges dependent claims 4 and 22–24 also fails.

Therefore, based on the record before us, Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 4 and 22–24 would have been obvious over Cheriton, Kessler, and Jain.

F. Alleged Obviousness of Claims 8 and 11–14 over Cheriton and Jain

Petitioner contends that claims 8 and 11–14 are obvious over Cheriton and Jain. Pet. 62–71. To support its contentions, Petitioner provides explanations as to how the prior art teach each claim limitation. *Id.* Petitioner also relies upon the Seshan Declaration to support its positions. Patent Owner counters that the prior art does not render claims 8 and 11–14 obvious because the Petition fails to adequately support the assertions, the prior art fails to sufficiently teach some limitations of the claim, and that a person of ordinary skill in the art would not be motivated to combine Cheriton and Jain. Prelim. Resp. 15–17.

On this record, we are persuaded by Petitioner’s explanations and evidence in support of the obviousness grounds asserted under Cheriton and Jain for claim 8 and 11, but not as to claims 12–14. We begin our discussion with a brief summary of Jain, and then address the evidence, analysis, and arguments presented by the parties.

1. Jain (Ex. 1003)

Jain is directed to data communications and recognizing local area network addresses. Ex. 1003, 2:3–4. A destination address list is used which contains a set of addresses that are compared to the destination

address of received frames. *Id.* at 3:3–5, 5:58–61. A “hashing function generator is supplied to operate upon the received bit stream.” *Id.* at 5:58–6:1. In a preferred embodiment, “the hashing function generator is a Cyclic Redundancy Check [CRC] generator, although the teaching of the invention is not limited to only the use of a CRC technique.” *Id.* at 6:1–2. Jain discloses that the hash function generator may employ XOR methods, among other techniques. *Id.* at 6:2–4.

2. Analysis

Claim 8

Petitioner asserts that Cheriton in combination with Jain discloses a cache management unit with an input register for receiving data unit header information including received source and destination address, a cyclic redundancy code generator that executes a CRC algorithm on the received source and destination addresses, an input packetizer communicating with the CRC generator and input register, a cache lookup unit and associated cache, and an output packetizer and output register. Pet. 62–68. Petitioner alleges that one of ordinary skill in the art would have found it obvious to combine the teachings of Cheriton and Jain because Cheriton discloses that alternative hashing functions may be employed in its invention, Jain teaches that the CRC-based hashing function is an alternative to the XOR-based hashing function of Cheriton, and “[s]uch a combination would be nothing more than the routine substitution of one known element for another known element, with both elements performing their known and well-understood function.” *Id.* at 58 (citing Ex. 1002, 9:48–51; Ex. 1007 ¶ 177).

We have reviewed the Petitioner’s evidence and explanations for the alleged teaching of the elements of claim 8, and are persuaded that the

evidence provided satisfies the reasonable likelihood threshold. Based on the current record, Petitioner also provides sufficiently persuasive rationale, that is, the stated interchangeability of hashing functions, for combining the teachings of Cheriton and Jain for purposes of this Decision.

Patent Owner argues that the Petition fails to adequately explain how Cheriton and Jain teach the use of an input packetizer and output packetizer as claimed. Prelim. Resp. 16–17. Patent Owner alleges, for instance, that the Petition “does not identify how any of the hash function logic, the tri-state buffer, or the data bus interface circuitry of Cheriton” packetizes or identifies something packetized. *Id.* at 16. Patent Owner also argues that under the obviousness analysis for claim 8, the Petition references the analysis of claim 22 for support, but there is a circular cross-reference back to claim 8. *Id.* at 15–16.

Petitioner maps the hash function logic of Cheriton, modified in view of Jain, to the “input packetizer.” Pet. 64–66 (citing Ex. 1002, 9:34–38, 9:55–56; Ex. 1003, 6:9; Ex. 1007 ¶¶ 199–201). Petitioner refers to cited portions of Cheriton and Jain in support of how the data is modified by the hash tag logic. *See id.* Petitioner maps Cheriton’s tri-state buffer, which formats source and destination address information for placement onto the data bus, as the “output packetizer,” alleging that one of ordinary skill in the art would also understand that, depending on the bus, additional signaling might be required for output to the bus. *Id.* at 67–68 (citing Ex. 1002, 10:52–56; Ex. 1007 ¶¶ 207–209).

We do not find persuasive Patent Owner’s arguments that the Petition’s support of input and output “packetizer” is insufficient at this juncture. Although the construction of the claim term “packetizer” was not

raised as an issue by either the Petitioner or Patent Owner, the '951 patent does not appear to require that “packets” be in a specialized form. Rather the '951 patent refers to units of information or data transmitted between devices or components, and “packetizing” refers to the assembly of units of the information and data. *See e.g.*, Ex. 1001, 1:42–46, 4:20–32, 7:45–50, 7:56–58, 8:11–16, 8:29–35, 9:16–18. As discussed above, the Petition refers to reformatting of information and data performed by the components of Cheriton mapped as the input and output “packetizers,” and, upon this record, we find sufficient support for the teachings of the respective claim limitations at this juncture.

We also do not find the Patent Owner’s argument concerning the alleged circular referencing between claims 8 and 22 concerning a CRC generator to be fully accurate. *See* Prelim. Resp. 15–17. Under the cross-referenced portion of claim 22, it states that “to implement the CRC hashing function of Jain, which would have been obvious *as set forth above*, it would have been obvious to use the CRC generator of Jain as the hash function logic of Cheriton.” Pet. 59 (emphasis added). This “above” discussion appears to refer to the discussion directed to the CRC hashing function of Jain as an alternative to the XOR-hashing of Cheriton for claim 4 in Section VII(C)(2), and additionally provides rationale for a combination of the references.⁶ *See id.* at 58–59. Cross-referenced portion of claim 22 also

⁶ The reference to claim “8” under Section VII(C)(3), also in a portion of the discussion of claim 22, appears to be a typographical error because the related information is described as “above,” where, instead, claim 8 is actually discussed further down in the Petition. *See* Pet. 59. It appears that claim 4 was the intended reference, but in any event, as discussed above, other evidence and argument provided and discussed in the Petition is

refers to paragraphs of the Seshan Declaration discussing the combination of the Cheriton and Jain that support the teachings of the limitations of claim 8 relating to the CRC generator. *See id.* at 59–60 (citing Ex. 1007 ¶¶ 181, 182).

Therefore, based on the record before us, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that claim 8 would have been obvious over Cheriton and Jain.

Claim 11

We have reviewed Petitioner’s explanations and supporting evidence regarding dependent claim 11, and find them persuasive. *See* Pet. 69. Patent Owner provides no additional arguments besides those discussed above in the context of the base independent claims, which we have not found persuasive. *See* Prelim. Resp. 15–17.

Based on the record before us, we determine that Petitioner has demonstrated a reasonable likelihood that it would prevail on its assertion that dependent claim 11 is unpatentable as obvious over Cheriton and Jain.

Claims 12–14

Claim 12 recites “[t]he cache management unit of claim 8, wherein said cache is provided as plural rows each having plural entries,” claim 13 is to “[t]he cache management unit of claim 12, wherein said cache lookup controller is adapted for identifying a row of said cache using said CRC encoded addresses,” and claim 14 recites “[t]he cache management unit of claim 12, wherein said cache lookup controller is adapted for comparing one of said received source and destination addresses to said address value of at

sufficient at this juncture, even absent the consideration of this potential typographic error.

least one of said plural entries of said identified cache row” Ex. 1001, 17:59–18:5. The Petition relies on arguments related to Cheriton’s alleged teachings of claim limitations as to the use of “rows,” which we have found insufficient for claims 1, 2, and 21, *supra* Section II.D.2. *See* Pet. 69–71 (citing Pet., Sect. VII(A)(3)). We therefore determine that the Petitioner has provided insufficient evidence to support obviousness of claims 12, 13, and 14 at this juncture for the reasons discussed *supra*, Section II.D.2.

Based on the record before us, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail on its assertion that claims 12–14 are unpatentable as obvious over Cheriton and Jain.

III. CONCLUSION

For the foregoing reasons, we conclude that the information presented demonstrates a reasonable likelihood that Petitioner will prevail in challenging claims 8 and 11 as unpatentable. At this stage, we have not made a final determination with respect to the patentability of the challenged claims or the construction of any claim term.

IV. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4(a), an *inter partes* review is hereby instituted on claims 8 and 11 as unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combination of Cheriton and Jain;

FURTHER ORDERED that no other grounds are authorized for this *inter partes* review other than those specifically identified above; and

FURTHERED ORDERED that pursuant to 35 U.S.C. § 314(c) and

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37 C.F.R. § 42.4(b), notice is hereby given of the institution of a trial. The trial will commence on the entry date of this decision.

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