

ARC for Sub-0.18 μ m Logic and Gigabit DRAM Frontend and Backend Processes

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Texas Instruments, Silicon Technology Development, Dallas, TX 75243

Abstract

We have developed different $\text{Si}_x\text{O}_y\text{N}_z$ antireflective coating (ARC) films for many different substrates for deep-UV lithography and implemented them into sub-0.18 μ m logic and Gigabit DRAM frontend and backend processes. The $\text{Si}_x\text{O}_y\text{N}_z$ film has dual functions: reducing substrate reflectivity to a minimum, and serving as a hardmask for poly and metal etch. These properties of $\text{Si}_x\text{O}_y\text{N}_z$ are crucial to tight CD control and fabrication of unique device structures. Plasma damage from ARC deposition is negligible. Using the designed $\text{Si}_x\text{O}_y\text{N}_z$ and linewidth reduction etch, sub-0.1 μ m metal gate nMOSFETs are demonstrated. Backend sub-0.25 μ m multilevel metal patterning and etch with $\text{Si}_x\text{O}_y\text{N}_z$ produce excellent metal profiles and 100% comb yield. A designed ARC also produces superior 1 Gigabit DRAM 0.16 μ m storage node contact patterning.

Introduction

The advantages of using antireflective coatings (ARC) for very small gate fabrication and critical dimension (CD) control have been reported on biased etch with organic ARC for I-line lithography [1], and for the inorganic ARC for sub-0.1 μ m gate fabrication in DUV lithography [2], however use of $\text{Si}_x\text{O}_y\text{N}_z$ ARC for frontend and backend processes in both Logic and DRAM has not been reported. TiN has been used as an I-line metal ARC but reflectivity is high (20-30%) in the DUV region. The high reflectivity of poly, metal, and poly/metal stack with oxide/nitride in 1G DRAMs has made DUV small feature patterning very difficult.

The reflectivity coupled with highly transparent photoresist degrades CD control particularly over rough, grainy, and topographical surfaces. The use of $\text{Si}_x\text{O}_y\text{N}_z$ ARC to eliminate reflective notching, to tightly control CD and to provide an etch hardmask has therefore become very critical for today's sub-0.18 μ m technology. This paper describes the design and implementation of $\text{Si}_x\text{O}_y\text{N}_z$ ARCs for sub-0.1 μ m poly and metal gates, 1G DRAM sub-0.18 μ m storage node contacts, and backend multilevel metal interconnects. ARC applications for 0.05 μ m poly gate NMOS transistors, for 1G DRAM frontend patterning, and for sub-0.18 μ m device backend multilevel metal interconnects are presented.

ARC Design and Lithography

ARCs work by phase shift cancellation of specific wavelengths. The three optical parameters of the $\text{Si}_x\text{O}_y\text{N}_z$ film: refractive index n , extinction coefficient k , and thickness d are specifically designed to ensure the reflected light that passes through the ARC/substrate is equal in amplitude but opposite in phase to the light reflected from the resist/ARC interface (see Fig. 1). More details about the design of $\text{Si}_x\text{O}_y\text{N}_z$ ARC have been described in reference [2]. Fig. 2a shows a reflectivity contour map of a specifically designed $\text{Si}_x\text{O}_y\text{N}_z$ ARC for Al with wide n (2.1 ± 0.1) and k (0.15 ± 0.05) windows. Fig. 2b shows the reflectivity change is less than 2% when the ARC thickness varies between 120Å-360Å.

DUV exposure latitude and depth-of-focus are much improved with the designed ARC. Fig. 3 shows the focus latitude with the ARC film for poly patterning. A 1.2 μ m depth-of-focus is obtained for 0.25 μ m features. Fig. 4 depicts the measured CD variation with the change of ARC film thickness. The CD variation is less than 5% with ARC thickness varying from 250Å to 550Å for a 300Å ARC. $\text{Si}_x\text{O}_y\text{N}_z$ ARC is used to pattern 0.16 μ m resist lines on polysilicon. 0.05 μ m gates are then formed using etch bias of 0.11 μ m. Excellent poly gate profiles were achieved, as shown by SEM and TEM in Fig. 5.

Results and Discussion

Sub-0.1 μ m metal gate NMOS transistor: In the replacement gate process, DUV patterning with a $\text{Si}_x\text{O}_y\text{N}_z$ ARC and linewidth reduction etch are used to fabricate poly gates down to 0.05 μ m. An oxide is deposited after source/drain implants and then removed from the top of poly gate by CMP. The poly gate is then removed by chemical wet etch and a 20Å gate oxide is regrown. Metal is deposited and etched to form the T-shaped metal gate [3].

The use of $\text{Si}_x\text{O}_y\text{N}_z$ ARC is crucial to fabricate 0.05 μ m poly-Si gates with DUV lithography. The selectivity of $\text{Si}_x\text{O}_y\text{N}_z$ during the linewidth reduction etch and poly-Si overetch further helps in maintain intact poly-Si lines where the resist thickness is marginal, such as for poly-Si over topography. Fig. 7 shows such a sub-0.1 μ m T-shaped metal gate (W or Al with TiN barrier). Fig. 8 shows output characteristics of 0.05 μ m W/TiN metal gate NMOS transistor. Fig. 9 shows the rolloff of V_t measured at $V_{DD}=1.5V$ for a Al/TiN metal gate transistor using 2.0nm oxide for several cases with and without a channel compensating arsenic and boron implants.

Sub-0.25 μ m multilevel interconnects: Pattern and etch of 0.20 μ m metal lines with excellent electrical properties have been demonstrated using $\text{Si}_x\text{O}_y\text{N}_z$ ARC in backend multilevel metal interconnects. Fig. 10 shows $\text{Si}_x\text{O}_y\text{N}_z$ not only functions as an ARC, but also serves a hardmask for etch. Without the $\text{Si}_x\text{O}_y\text{N}_z$ layer, metal erosion is observed due to the aggressive metal etch. It is interesting to note that resist selectivity for metal etch can be increased using $\text{Si}_x\text{O}_y\text{N}_z$ ARC layer, although the cause is not clear. More resists remains after metal etch with the presence of $\text{Si}_x\text{O}_y\text{N}_z$. Fig. 11 shows excellent metal profiles using the ARC. Electrical probe indicates a perfect cumulative distribution of electrical linewidth reduction and 100% comb yield. Fig. 12 shows such a distribution with different metal etch processes. The mean electrical critical dimension loss is less than 0.02 μ m with tight distribution for both 0.25 μ m line/space and sub-0.25 μ m features. Comb resistance greater than 1E8 ohm with tight cumulative probability distribution is shown in Fig. 13.

1G DRAM: Fig. 14 shows 1G DRAM storage node contact holes patterning. Without ARC film the holes have funnel-sharp pattern (a), with $\text{Si}_x\text{O}_y\text{N}_z$ ARC the 0.16 μ m contact holes are perfectly patterned (b). Inorganic ARC, such as $\text{Si}_x\text{O}_y\text{N}_z$, is important for 1G DRAM processing. Substrate topography damage has been observed when organic BARC material is used for patterning and etch because organic BARC etch is relatively non-selective.

ARC Process and Plasma Damage: The ARC stack is deposited in a cluster PECVD system. The n and k values are tuned by varying the process gas flow ratios. Excellent uniformity of n and k is obtained with a manufacturing deposition process tool. Plasma damage during ARC deposition was evaluated using a Keithley Quantox system. Surface static charge voltage (V_s) was measured using a vibrating Kelvin probe, and flatband voltage (V_{fb}) was measured using surface photovoltage, in which a pulsed light source is linked to the Kelvin probe and enables the stimulus and detection of surface photovoltage (Fig. 6). The plasma damage was measured with PECVD oxide and thermal oxide as references, and correlated to our previous Predator device plasma damage studies. Plasma damage for ARC deposition was negligible from Quantox measurement, the V_s was 0.33V and V_{fb} was 0.37V for 300Å ARC film, compared to 0.30V V_s and 0.21V V_{fb} for 300Å thermal oxide. Particle and metal contamination levels from PECVD deposition are not issues for ARC process manufacturing.

Conclusions

In summary, we have designed specific $\text{Si}_x\text{O}_y\text{N}_z$ ARCs for various substrates for deep-UV lithography. Fabrication of 0.05 μ m metal gate CMOS devices with excellent channel length control was demonstrated. Better CD control and large focus latitude were achieved using the inorganic ARC in DUV lithography for poly, backend multilevel metal, and 1G DRAM processing. The hardmask function offered by $\text{Si}_x\text{O}_y\text{N}_z$ ARC is crucial and beneficial to the fabrication of continuously scaled features. These results suggest great promise for extension of this technique to all levels of DUV patterning for sub-0.18 μ m advanced technology manufacturing.

References

- [1] G. Thakar, *et al.*, Symp. on VLSI Tech. Dig. p216, 1996.
- [2] W. Lee, *et al.*, Symp. on VLSI Tech. Dig. p131, 1997.
- [3] A. Chatterjee, *et al.*, IEEE IEDM Tech. Dig. p821, 1997.

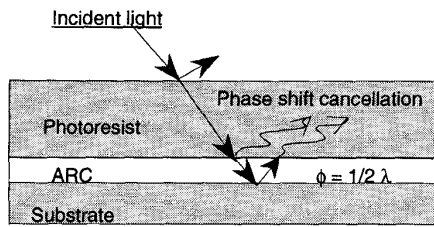


Fig. 1 Phase shift cancellation by optimization of ARC.

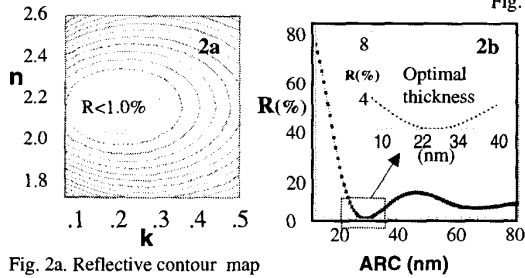


Fig. 2a. Reflective contour map for Al metal ARC (250Å).

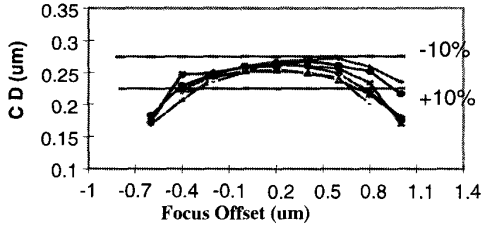


Fig. 3. The depth-of-focus is 1.2μm with ±10% CD variation.

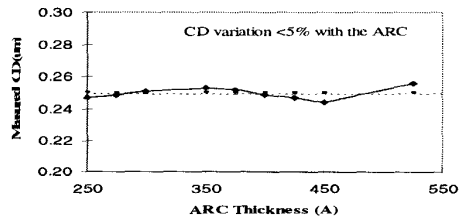


Fig. 4. Low CD variation with variation of ARC thickness.

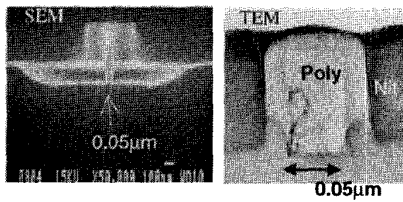


Fig. 5. SEM and TEM of 0.05μm poly pattern.

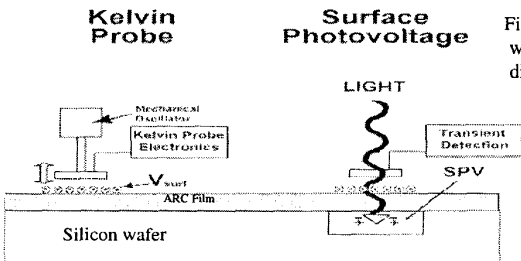


Fig. 6. Schematic setup for ARC film plasma damage studies.

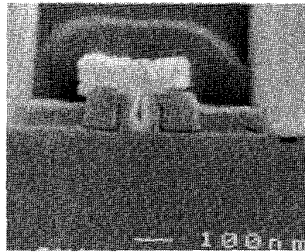


Fig. 7. Sub-0.1μm W/TiN gate NMOS transistor.

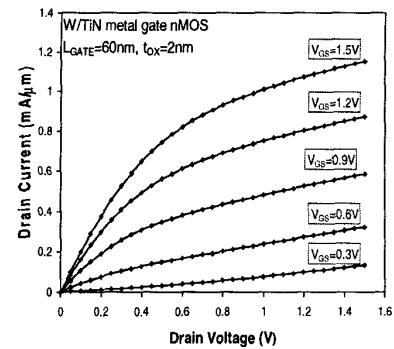


Fig. 8. The 0.06μm transistor output characteristics.

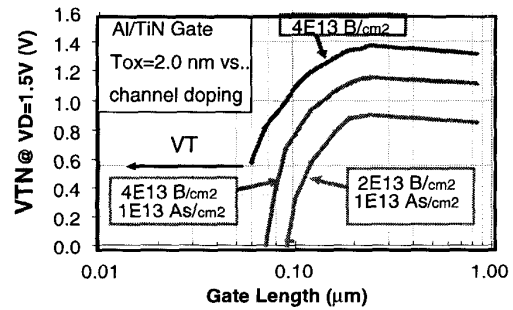


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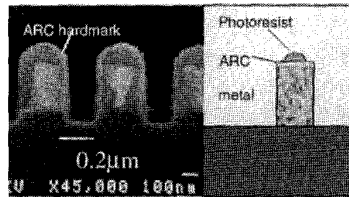


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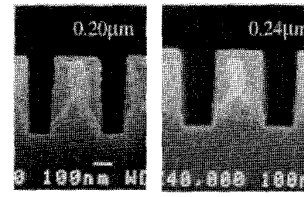


Fig. 11. Metal etch profile of 0.20 and 0.24μm lines using the ARC.

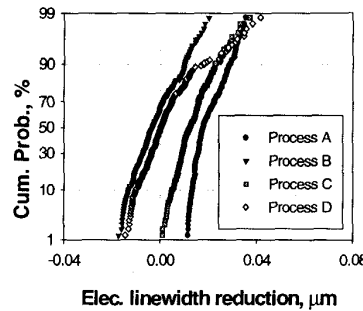


Fig. 12. Cumulative electrical line width reduction measurements with 4 different etch processes.

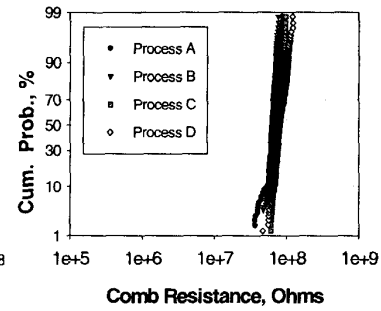


Fig. 13. Tight metal comb resistance cumulative distribution with 4 different etch processes.

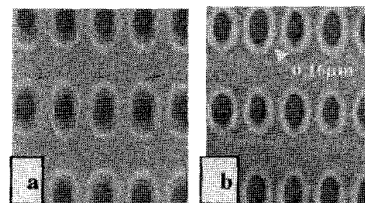


Fig. 14. 1G DRAM storage node contact holes patterning. Without ARC film the holes have funnel-sharp pattern (a), with Si₃O₄N₂ ARC the 0.16μm holes are perfectly patterned (b).

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M. Kakumu, Toshiba Corp.

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12.2	A Dynamic Depletion SOI MOSFET Model for SPICE , D. Sinitsky, S. Fung*, S. Tang, P. Su, M. Chan*, P. Ko* and C. Hu, University of California, Berkeley, CA and *Hong Kong University of Science and Technology, Hong Kong, China	114
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M. Ohkura, Hitachi, Ltd.

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- 13.1 A Highly Reliable 1T/1C Ferroelectric Memory,** D.-J. Jung, S.-Y. Lee, B.-J. Koo, Y.-S. Hwang, D.-W. Shin, J. -W. Lee, Y.-S. Chun, S.-H Shin, M.-H. Lee, H.-B. Park, S.-I. Lee, K. Kim and J.-G. Lee, Samsung Electronics, Co., Kyungki-do, Korea 122

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- 13.2 High Tolerance Operation of 1T/2C FeRAMs for the Variation of Cell Capacitors Characteristics,** N. Tanabe, S. Kobayashi, T. Miwa, K. Amanuma, H. Mori, N. Inoue, T. Takeuchi, S. Saitoh, Y. Hayashi, J. Yamada, H. Koike, H. Hada and T. Kunio, NEC Corp., Kanagawa, Japan 124

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- 13.3 A Scalable Single-Transistor/Single-Capacitor Memory Cell Structure Characterized by an Angled-Capacitor Layout for Megabit FeRAMs,** T. Kachi, K. Shoji, H. Yamashita*, T. Kisu*, K. Torii, T. Kumihashi, Y. Fujisaki and N. Yokoyama, Hitachi Ltd., Kokubunji, Tokyo, Japan and *Hitachi ULSI Engineering Corp., Tokyo, Japan 126

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- 13.4 Normally-off PLED (Planar Localised Electron Device) for Non-Volatile Memory,** H. Mizuta, K. Nakazato, P. Piotrowicz, K. Itoh*, T. Teshima*, K. Yamaguchi* and T. Shimada*, Hitachi Europe Ltd., Cambridge, UK and *Hitachi Ltd., Tokyo, Japan 128

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- 14.1 Source/Drain Extension Scaling for 0.1 μ m and Below Channel Length MOSFETs,** S. Thompson, P. Packan, T. Ghani, M. Stettler, M. Alavi, I. Post, S. Tyagi, S. Ahmed, S. Yang and M. Bohr, Intel Corp., Hillsboro, OR 132

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- 14.2 33nm Ultra-Shallow Junction Technology by Oxygen-Free and Point-Defect Reduction Process,** S. Shishiguchi, A. Mineji, T. Yasunaga and S. Saito, NEC Corp., Kanagawa, Japan 134

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- 14.3 High Performance RF Characteristics of Raised Gate/Source/Drain CMOS with Co Salicide,** T. Ohguro, H. Naruse, H. Sugaya, S. Nakamura, E. Morifuji, H. Kimijima, T. Yoshitomi, T. Morimoto, H.S. Momose, Y. Katsumata and H. Iwai, Toshiba Corp., Kawasaki, Japan 136

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- 14.4 Direct Channel Length Determination of sub-100nm MOS Devices Using Scanning Capacitance Microscopy,** R. Kleiman, M. O'Malley, F. Baumann, J. Garino, W. Timp and G. Timp, Bell Laboratories, Lucent Technologies, Murray Hill, NJ 138

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Technology:

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- 15.2 Optimization of a 0.18 μ m 1.5V CMOS Technology to Achieve 15 ps Gate Delay,** I.Y. Yang, P. Gilbert, C. Pettinato, S. Anderson, R. Woodruff, V. Misra, N. Bhat, K. Reid, T. Lii, C. Yuan, D. Dyer, D. O'Meara, S. Collins, H. De and S. Veeraraghavan, Motorola, Inc., Austin, TX 148

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- 15.3 A Highly Manufacturable 0.25 μ m Multiple-Vt Dual Gate Oxide CMOS Process for Logic/Embedded IC Foundry Technology,** M.H. Chang, J.K. Ting, J.S. Shy, L. Chen, C.W. Liu, J.Y. Wu, K.H. Pan, C.S. Hou, C.C. Tu, Y.H. Chen, S.L. Sue, S.M. Jang, S.C. Yang, C.S. Tsai, C.H. Chen, H.J. Tao, C.C. Tsai, H.C. Hsieh, Y.Y. Wang, R.Y. Chang, K.B. Cheng, T.Y. Chu, T.N. Yen, P.S. Wang, J.W. Weng, J.H. Hsu, Y.S. Ho, C.H. Ho, Y.C. Huang, R.Y. Shiue, B.K. Liew, C.H. Yu, S.C. Sun and J.Y.C. Sun, Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan, ROC 150

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- 15.4 A Manufacturable and Modular 0.25 μ m CMOS Platform Technology,** P. Tsui, H. Chuang, N. Bhat, E. Travis, S. Chheda, J. Grant, P. Gilbert, P. Chen, S. Poon, A. Kaiser, B. Anthony, T. White, J. West, T. Vuong, S. Mattay, B. Kruth, A. Perera, J. Porter, M. Schippers, I. Yang, V. Misra, S. Venkatesan, A. Nagy and T. Lii, Motorola, Austin, TX 152

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M. Ohkura, Hitachi, Ltd.

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- 16.1 Electromigration of Submicron Damascene Copper Interconnects**, C. Ryu, K.-W. Kwon, A.L.S. Loke, V. Dubin*, R. Kavari**, G. Ray** and S.S. Wong, Stanford University, Stanford, CA and *Advanced Micro Devices, Sunnyvale, CA and **Hewlett-Packard Labs, Palo Alto, CA

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- 16.2 A New Prediction Method for Oxide Lifetime and Its Application to Study Dielectric Breakdown Mechanism**, K. Okada, H. Kubo, A. Ishinaga and K. Yoneda, Matsushita Electronics Corp., Kyoto, Japan

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- 16.3 Performance and Reliability of Sub-100nm MOSFETs with Ultra Thin Direct Tunneling Gate Oxides**, Q. Xiang, G. Yeap, D. Bang, M. Song, K. Ahmed, E. Ibok and M.-R. Lin, Advanced Micro Devices, Inc., Sunnyvale, CA

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- 16.4 A New Degradation Scheme for Direct-Tunneling Ultrathin Gate Dielectric**, N. Kimizuka, T. Yamamoto and T. Mogami, NEC Corp., Kanagawa, Japan

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H. Hanafusa, Sanyo Electric Co., Ltd.

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- 17.1 CVD Photoresist Processes for Sub-0.18 μ m Design Rules**, T. Weidman, D. Sugiarto, M. Nault, D. Mui, Z. Osborne, C. Lee* and J. Yang*, Applied Materials, Santa Clara, CA and *Intel Corporation, Santa Clara, CA

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- 17.2 A Novel Resist and Post-Etch Residue Removal Process Using Ozonated Chemistries**, S. DeGendt, P. Snee, I. Cornelissen, M. Lux, R. Vos, P. Mertens, D. Knotter and M. Heyns, IMEC, Leuven, Belgium

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- 17.3 A Statistical Gate CD Control Including OPC**, A. Misaka, A. Goda, S. Odanaka, S. Kobayashi and H. Watanabe, Matsushita Electronics Corporation, Kyoto, Japan

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- 17.4 A Novel Etch Chemistry for Low-Damage Poly-Si Gate Patterning**, H. Richter, M.-A. Aminpur, A. Wolff, R. Sorge and W.-D. Rau, Institute for Semiconductor Physics, Frankfurt, Germany

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J. Ida, Oki Electric Industry Co., Ltd.

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- 18.1 A New Mode of Hot Carrier Degradation in 0.18 μ m CMOS Technologies**, C.T. Liu, E.J. Lloyd, C.P. Chang, K.P. Cheung, J. Colonell, W.Y.C. Lai, R. Liu, C.S. Pai, H. Vaidya and J.T. Clemens, Bell Laboratories, Lucent Technologies, Murray Hill, NJ

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- 18.3 Deuterium Process of CMOS Devices: New Phenomena and Dramatic Improvement**, Z. Chen, J. Lee, J. Lyding and K. Hess, University of Illinois, Urbana, IL

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- 18.4 Limitation of Post-Metallization Annealing Due to Hydrogen Blocking Effect of Multilevel Interconnect**, S. Ito, K. Noguchi, T. Horiuchi and J.T. Clemens*, NEC Corp., Kanagawa, Japan and *Bell Laboratories, Lucent Technologies Inc., Murray Hill, NJ

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J. Ida, Oki Electric Industry Co., Ltd.

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- 19.1 Highly-Reliable, Low-Resistivity bcc-Ta Gate MOS Technology Using Low-Damage Xe-Plasma Sputtering and Si-Encapsulated Silicidation Process**, K. Ino, T. Ushiki, K. Kawai, I. Ohshima, T. Shinohara and T. Ohmi, Tohoku University, Sendai, Japan

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- 19.2 Highly Uniform Heteroepitaxy of Cobalt Silicide by Using Co-Ti Alloy for Sub-Quarter Micron Devices**, T. Iinuma, H. Akutsu, K. Ohuchi, K. Miyashita, Y. Toyoshima and K. Suguro, Toshiba Corp., Yokohama, Japan

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- 19.3 Optimized Poly-Si-Ge-Gate Technology for Dual Gate CMOS Application**, W.-C. Lee, T.-J. King, and C. Hu, University of California, Berkeley, CA

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- 19.4 Pure Ge Mid-Gap Gate Within an Industrial High Performance and Low Standby Current 0.18 μ m CMOS Process**, J. Alieu, R. Gwoziecki, M. Paoli, T. Skotnicki, C. Hernandez, F. Martin, C. Mourrain, D. Bensahel, M. Basso*, J. Galvier and M. Haond*, France Telecom, Meylan Cedex, France and *Centre Commun CNET-SGS-Thomson Microelectronics, Crolles Cedex, France

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T. Shibata, University of Tokyo

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- 20.1 Microscopic and Statistical Approach to SILC Characteristics—Exponential Relation between Distributed Fowler Nordheim Coefficients and Its Physical Interpretation**, N. Tsuji, K. Sakakibara, N. Ajika and H. Miyoshi, Mitsubishi Electric Corp., Hyogo, Japan

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- 20.2 Gate-Oxide Degradation from Source/Drain (S/D) Boron Diffusion**, K.P. Cheung, C.-P. Chang, J. Colonell, W.Y.C. Lai, C.T. Liu, R. Liu, C.S. Pai, C. Rafferty, H. Vaidya and J.T. Clemens, Bell Laboratories, Lucent Technologies, Murray Hill, NJ

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S. Odanaka, Matsushita Electronics Corp.

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- 21.1 Trench Transformation Technology Using Hydrogen Annealing for Realizing Highly Reliable Device Structure with Thin Dielectric Films**, T. Sato, I. Mizushima, J. Iba, M. Kito, Y. Takegawa, A. Sudo and Y. Tsunashima, Toshiba Corp., Yokohama, Japan **206**

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- 21.2 A New STI Process Based on Selective Oxide Deposition**, N. Elbel, Z. Gabric, W. Langheinrich* and B. Neureither, Siemens AG, Munich, Germany and *SIMEC, Dresden, Germany **208**

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- 21.4 Characterization and Elimination of Trench Dislocations**, J. Damiano, C. Subramanian, M. Gibson, Y.-S. Feng, L. Zeng, J. Sebek, E. Deeters, C. Feng, T. McNelly, M. Blackwell, H. Nguyen, H. Tian, J. Scott, J. Zaman, C. Honcik, M. Miscione, K. Cox and J. Hayden, Motorola, Austin, TX **212**

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Chairpersons: D. Huber, Wacker Siltronic
E. Suzuki, Electrotechnical Laboratory

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- 22.1 Stacked Gate Dielectrics with TaO for Future CMOS Technologies**, I. Kizilyalli, P. Roy, F. Baumann*, R.Y. Huang, D. Hwang, C. Chacon, R. Irwin, Y. Ma, and G. Alers*, Bell Laboratories, Lucent Technologies, Orlando, FL and *Murray Hill, NJ **216**

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- 22.2 Highly Robust Ultra-Thin Gate Dielectric for Giga Scale Technology**, M. Khare, X.W. Wang, T.P. Ma, G.J. Cui*, T. Tamagawa*, B. Halpern* and J. Schmitt*, Yale University, New Haven, CT and *Jet Process Corp., New Haven, CT **218**

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- 22.3 Nitrogen Concentration Optimization for Down-Scaled CMOSFET with N₂O-Based Oxynitride Process**, Y. Okayama, K. Kasai, T. Yamaguchi, A. Ooishi, M. Takayanagi-Takagi, F. Matsuoka and M. Kinugawa, Toshiba Corp., Yokohama, Japan **220**

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- 22.4 Ultra-thin, 1.0-3.0nm Gate Oxides for High Performance sub-100nm Technology**, T. Sorsch, W. Timp, F. Baumann, K. Bogart, T. Boone, V. Donnelly, M. Green, K. Evans-Lutterodt, C.Y. Kim, S. Moccio, J. Rosamilia, J. Sapjeta, P. Silverman, B. Weir, and G. Timp, Bell Laboratories, Lucent Technologies, Murray Hill, NJ **222**