UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC. Petitioner

V.

THE BOARD OF TRUSTEES OF THE UNIVERSITY OF ILLINOIS Patent Owner

> Case IPR2013-00005 Patent 6,444,533 B1

Before SALLY GARDNER LANE, BRYAN F. MOORE, and MICHAEL J. FITZPATRICK, *Administrative Patent Judges*.

FITZPATRICK, Administrative Patent Judge.

DECISION TO INSTITUTE TRIAL FOR INTER PARTES REVIEW

BACKGROUND

Micron Technology, Inc. ("Micron") filed a Petition¹ requesting inter partes review of all claims (i.e., claims 1-8) of U.S. Patent 6,444,533 B1 (the "533 Patent") pursuant to 35 U.S.C. § 311. The Patent Owner, the Board of Trustees of the University of Illinois ("University"), filed a Preliminary Response² pursuant to 35 U.S.C. § 313. We have jurisdiction under 35 U.S.C. § 314.

Institution of inter partes review is authorized by statute when "the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. §314(a); *see also* 37 C.F.R. § 42.108.

We determine that the petition demonstrates that there is a reasonable likelihood that Micron would prevail with respect to at least one challenged claim, and we institute inter partes review as to claims 1-8 of the '533 Patent.

A. Related Proceedings

Micron indicates that it is a named defendant in pending litigation concerning the '533 Patent brought by the Patent Owner and styled *The Board of Trustees of the University of Illinois v. Micron Technology, Inc.*, Case No. 2:11-cv-02288 (C.D. Ill.). (Pet. 1.)

¹ Citations to the Petition may be abbreviated as "Pet."

² Citations to the Preliminary Response may be abbreviated as "Prelim. Resp."

Micron also has filed two additional petitions for inter partes review of two related patents: IPR2013-00006 regarding U.S. Patent 6,888,204 and IPR2013-00008 regarding U.S. Patent 5,872,387.

B. The '533 Patent

The '533 Patent (Ex. 1002), entitled "Semiconductor Devices And Methods For Same," issued on September 3, 2002, names Joseph W. Lyding and Karl Hess as inventors, and is assigned to the University. The '533 Patent issued from U.S. Application Serial No. 09/518,802, filed March 3, 2000.

The '533 Patent "relates to methods for treating semiconductor devices or components thereof in order to reduce the degradation of semiconductor device characteristics over time." (Col. 1, ll. 13-16.) In particular, the '533 Patent discloses methods of treating a semiconductor device by passivating (or annealing) the device with deuterium, an isotope of hydrogen. (Col. 2, ll. 25-28; Prelim. Resp. 1.) The '533 Patent explains:

[T]reatment with deuterium provides a reduction in the depassivation or "aging" of semiconductor devices due to hotcarrier effects. Such aging is evidenced, for example, by substantial degradations of threshold voltage, transconductance, or other device characteristics. In accordance with the present invention, semiconductor devices are fabricated using deuterium to condition the devices and stably reduce the extent of these degradations. (Col. 3, ll. 27-35.)

Prior to the '533 Patent, passivating with hydrogen³ was "a wellknown and established practice in the fabrication of semiconductor devices"

³ Our use of the term "hydrogen" and the symbol "H" in this Decision refers to naturally occurring hydrogen, which we understand to be predominantly protium but may include trace amounts of deuterium.

to remove defects that affect the operation of the devices. ('533 Patent col. 1, ll. 17-21; U.S. Patent 5,872,387 col. 1, ll. 10-14⁴; *see also* Reed Decl. ¶¶ 13-14.) According to the '533 Patent, it was "discovered that semiconductor devices, for example including MOS^5 devices, can be advantageously treated with deuterium to improve their operational characteristics." (Col. 2, ll.

22-25.)

C. Illustrative Claims

Claims 1 and 2 are the only independent claims of the '533 Patent.

They are illustrative of the claimed subject matter and read as follows:

1. A process for treating a semiconductor device including a semiconductor region and an insulating layer having an interface with the semiconductor region and a contact on said insulating layer overlying said interface, comprising the steps of forming said insulating layer with a thickness not exceeding about 55 Angstroms beneath said contact, and of annealing said semiconductor device, subsequent to completion of fabrication of said device, in an ambient including deuterium to form a concentration of deuterium at the interface between said semiconductor region and said insulating layer region effective to substantially reduce degradation of said device associated with hot carrier stress.

2. A process for treating an insulated gate field effect transistor device structure including a channel region extending between source and drain regions, a gate insulating layer having an interface with said channel region, and contacts to said source and drain regions and on said gate insulator layer,

⁴ U.S. Patent 5,872,387 issued from U.S. Application Serial No. 08/586,411, filed January 16, 1996, which is the earliest application to which the '533 Patent claims priority. It is not an exhibit in the instant proceeding although it is the subject of another Micron petition, case number IPR2013-00008. ⁵ MOS refers to metal oxide semiconductor. ('533 Patent col. 1, 11. 34-35; Reed Decl. ¶ 9.)

comprising forming said gate insulator beneath the gate contact to have a thickness not greater than about 55 Angstroms and, subsequent to formation of said source, drain and gate contacts, annealing the device in an ambient including deuterium at a temperature above about 200° C. and below a decomposition or melting temperature of said structure to form a concentration of deuterium at said interface region effective to substantially reduce degradation of said device associated with hot carrier stress by increasing a practical lifetime at least about 10 times that provided by a corresponding passivation with hydrogen, where practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

D. Prior Art Relied Upon

Micron challenges the patentability of claims 1-8 of the '533 Patent as

obvious under 35 U.S.C. § 103(a) in view of the following items of prior art:

Ex. 1004	US 5,478,765 to Kwong et al., issued December 26, 1995
	("Kwong")

- Ex. 1005 US 4,980,307 to Ito et al., issued December 25, 1990 ("Ito")
- Ex. 1006 WO 94/19829 to Lisenker et al., published September 1, 1994 ("Lisenker")
- Ex. 1007 Mikawa et al., "Electron Spin Resonance Study of Interface States Induced by Electron Injection in Metal-Oxide-Semiconductor Devices," 59 (6) J. Appl. Phys, 2054, March 15, 1986 ("Mikawa")
- Ex. 1009 US 4,027,380 to Deal et al., issued June 7, 1977 ("Deal")
- Ex. 1010 Gise et al., "Semiconductor and Integrated Circuit Fabrication Techniques," Reston Publishing Company, Inc., 1979 ("Gise")
- Ex 1011 Dillinger, "VLSI Engineering," Prentice Hall, 1988 ("Dillinger")

Further, Micron relies upon declaration testimony of its witness Michael L. Reed, Ph.D. (Ex. 1001: "Reed Decl.") originally submitted in this proceeding and declaration testimony of Robert M. Wallace, Ph.D. (Ex.

1013: "Wallace Decl.") previously submitted by the University during the prosecution of related U.S. Patent 6,888,204.

1. Lisenker (Ex. 1006)

Lisenker discloses "a method for producing semiconductor devices in which hydrogen-containing bonds in silicon dioxide are replaced with deuterium containing bonds. Specifically Si-H bonds are replaced with Si-D bonds and Si-OH bonds are replaced with Si-OD bonds." (P. 5, 1. 36 - p. 6,

1. 3.) Lisenker further discloses how the method may be carried out, stating:

a silicon wafer is contacted with a deuterium containing material to form Si-D and Si-OD bonds in a silicon dioxide layer and on a silicon surface at an interface with the silicon dioxide layer. Typical silicon dioxide layers suitable for treatment according to the present invention include isolation oxides, gate oxides, and various other oxide layers commonly used with semiconductor devices. According to the invention, deuterium or a deuterium-containing material is directed onto the device by, for example, annealing in a deuterium containing atmosphere, and/or cleaning with a deuterium compound such as D₂O, D₂SO₄, and DCl. In general, any hydrogen containing material used in VLSI^[6] fabrication can be replaced with corresponding deuterium containing material. (P. 4, 11. 20-34.)

Finally, Lisenker discloses the benefits of the method and how those benefits are obtained, stating:

The stability of oxide layers is improved in the present invention because the bond energy of the Si-H and Si-OH bonds is increased by replacing the hydrogen atoms with deuterium atoms. The Si-D and Si-OD bonds thus formed provide completed silicon dangling bonds that are less likely to break when exposed to electrical stresses. Therefore, the deuterium containing devices of the present invention have

⁶ VLSI stands for "very large scale integration." (Ex. 1011, Dillinger 4.)

improved stability, quality, and reliability. (P. 4, 1. 35 - p. 5, 1. 5.)

The University urges us not to consider Lisenker because it was before the Office during prosecution. (Prelim. Resp. 8.) Under 35 U.S.C. § 325(d), "the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." But, we are not required by statute to reject a petition based upon the fact that certain arguments or art were previously considered by the Office, and after reviewing the prior prosecution, we decline to do so in this case. The present record differs from the one before the Examiner. For example, we consider the Lisenker reference in view of the declaration testimony of Dr. Reed, which was not before the Examiner.

2. Ito (Ex. 1005)

Ito is entitled "Process For Producing A Semiconductor Device Having A Silicon Oxynitride Insulative Film." Ito states that "[t]he gate insulation film should have a thickness of from approximately 30 to 3000 angstroms[.]" (Col. 9, ll. 41-43.)

3. Deal (Ex. 1009)

Deal is entitled "Complimentary Insulated Gate Field Effect Transistor Structure And Process For Fabricating The Structure." It discloses much of the subject matter of claims 1-8, including in particular, post-metal annealing, albeit in hydrogen. (Col. 9, 11. 33-51.) Deal does not disclose using deuterium.

4. Reed Declaration (Ex. 1001)

Micron relies upon declaration testimony of Dr. Reed. Dr. Reed testifies that he has bachelor's, master's, and doctoral degrees in electrical engineering; has over twenty-five years of experience as a researcher and practitioner in electrical engineering; has industry experience as a process engineer focusing on integrated circuit processing and manufacturing of multi-project integrated circuit chips; and is currently a professor at the University of Virginia School of Engineering and Applied Science. (Reed Decl. ¶¶ 1-5.). We find Dr. Reed to be qualified to testify concerning the issues raised in the Micron Petition.

5. Wallace Declaration (Ex. 1013)

Micron relies upon declaration testimony of Dr. Wallace, submitted by the University during the prosecution of related U.S. Patent 6,888,204, that "post metal hydrogen annealing had been in widespread use in the semiconductor industry for many years." (Wallace Decl. ¶ 15 (citing a 1995 article).)

E. The Asserted Grounds

Micron challenges the patentability of claims 1-8 of the '533 Patent on twenty-one enumerated grounds. (Pet. 3-4.) In particular, Micron asserts that claims 1-8 are unpatentable under 35 U.S.C. § 103(a) as obvious over Lisenker alone, over eight different combinations of references based principally on Lisenker, over six different combinations of references based principally on Deal, and over six different combinations of references based principally on Dillinger.

ANALYSIS

A. Claim Construction

We generally give claim terms their ordinary and customary meaning as would be understood by one of ordinary skill in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc). In an inter partes review, "[a] claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b).

Pursuant to 37 C.F.R. § 42.104(b)(3), the Petition is to include a statement of how each challenged claim is to be construed. The Office Patent Trial Practice Guide ("Practice Guide"), however, states that "it may be sufficient for a party to provide a simple statement that the claim terms are to be given their broadest reasonable interpretation, as understood by one of ordinary skill in the art and consistent with the disclosure." 77 Fed. Reg. 48764 (Aug. 14, 2012). Micron has provided such a statement. (Pet. 5.)

The University asserts that the Petition should be denied because Micron has not provided the requisite claim construction. (Prelim. Resp. 16-17.) In so asserting, the University also relies on the Practice Guide, which further states "where a party believes that a specific term has meaning other than its plain meaning, the party should provide a statement identifying a proposed construction of the particular term and where the disclosure supports that meaning." 77 Fed. Reg. 48764. The University argues that Micron is of the belief that several of the claims require a construction that is different than the plain meaning since, in the district court litigation involving the '533 Patent, Micron asserted that several claim terms required construction. (Prelim. Resp. 15 (citing Ex. 2004).) The record in this

proceeding, however, lacks any constructions that may have been proposed by either party in the district court litigation.

We give each claim term its broadest reasonable interpretation as understood by one of ordinary skill in the art and consistent with the disclosure of the '533 Patent, as neither party has argued persuasively that any claim or term should be construed otherwise.⁷ For purposes of our Decision we find it useful to set forth, expressly, constructions for two claims terms.

First, we construe the term "subsequent to completion of fabrication of said device" appearing in claim 1 to mean after the contacts on the device are formed. This is the broadest reasonable interpretation consistent with the disclosure of the '533 Patent. (*See* Col. 4, 11. 41-43 ("subsequent to the fabrication of device **11** (e.g. subsequent to fabricating the gate, source and drain contacts))"; col. 4, 11. 52-53 ("after fabrication is completed (i.e. after the metal contacts are completed)").)

Second, we note the term "above about 200° C. and below a decomposition or melting temperature of said structure" appearing in claim 2 includes temperatures of up to about 1,000° C. (*See* Col. 5, ll. 1-7 ("The annealing process can be conducted . . . preferably at a temperature of at least about 200° C. up to the melting point or decomposition temperature of other components of the device, more preferably in the range of about 200°

⁷ Micron generally asserted that the claims should be "treated as product-byprocess claims[.]" (Pet. 5-6.) Each of the claims, however, is explicitly a "process" or "method," and Micron did not provide any basis or reasons for construing them as product-by-process claims. Hence, we reject Micron's request to treat them as product-by-process claims.

C. to about 1000° C., and most typically in the range of about 200° C. to about 800° C.").)

B. Claims 1-8 As Obvious Over Lisenker Alone

1. Claim 1

We find that Lisenker, as discussed above and below, teaches the subject matter of claim 1 except for the step of "forming said insulating layer with a thickness not exceeding about 55 Angstroms beneath said contact[.]"

The Supreme Court has held that the obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). In that regard, we credit the testimony of Micron's witness Dr. Reed that, at the time of filing the '533 Patent, it would have been apparent to one of ordinary skill in the art to reduce the thickness of the gate insulating film of Lisenker to 55 Angstroms or less consistent with the general decades-long trend of device miniaturization in the semiconductor industry. (Reed Decl. ¶ 38.)

We also credit Dr. Reed's testimony that, at the time of filing the '533 Patent, others already had made gate insulating films having thicknesses of 55 Angstroms or less. (Reed Decl. ¶ 39 (citing Kwong col. 1, 11. 40-45); Reed Decl. ¶ 43 (citing Ito col. 9, 11. 39-62).) The combination of familiar elements according to known methods to achieve predictable results, such as reducing the thickness of the gate insulating film of Lisenker to 55 Angstroms or less, is likely to be obvious. *See KSR*, 550 U.S. at 401.

Accordingly, based on the present record, which lacks sufficient evidence of criticality of the thickness limitation, there is a reasonable likelihood that Micron will prevail on its assertion that claim 1 would have been obvious over Lisenker to a person of ordinary skill in art under 35 U.S.C. § 103(a).

In reaching this conclusion, we have considered the University's preliminary arguments but we do not find them persuasive as discussed below.

The University does not rely on the about 55 Angstroms or less thickness limitation as distinguishing its claimed inventions over the prior art. Rather, it argues that "[t]he independent claims generally have two distinctive limitations: (1) the deuterium anneal is performed postfabrication, or after the formation of the metal contacts; and (2) the postfabrication anneal results in a device where the deuterium is retained at the interface of the semiconductive layer and gate insulator." (Prelim. Resp. 2.)

With respect to the first allegedly distinctive limitation, we find that Lisenker is not limited to annealing in, or passivating with, deuterium prior to formation of the metal contacts. Lisenker states that "[t]he formation of Si-D and Si-OD bonds is accomplished in the present invention by contacting a silicon wafer with deuterium or a deuterium containing compound *before, during, and/or after* formation [sic, of] a device oxide layer." (P. 6, ll. 10-14 (emphasis added).) Lisenker further discloses:

The present invention can be implemented throughout the VLSI fabrication procedure. A typical fabrication procedure will include various doping, etching, annealing, deposition, cleaning, passivation, and oxidation steps. In each instance in which hydrogen or a hydrogen containing compound is employed, deuterium or a deuterium containing compound can be used in its place. This is particularly important in those fabrication steps in which a permanent oxide layer is being formed or treated. (P. 8, 11. 29-37.)

In short, "any hydrogen containing material used in VLSI fabrication can be replaced with corresponding deuterium containing material." (P. 4, ll. 32-34.)

The University, citing a 1995 publication, previously conceded that "post metal hydrogen annealing had been in widespread use in the semiconductor industry for many years[.]" (Wallace Decl. ¶ 15; *see also* Reed Decl. ¶ 15 (testifying that it was "standard practice" in the industry).) Thus, as Lisenker teaches the substitution of deuterium wherever hydrogen is used including "annealing" and "after formation", it teaches that substitution during post-metal annealing.

With respect to the second allegedly distinctive limitation, i.e., that deuterium is retained at the interface, Lisenker expressly discloses this result. (P. 10, ll. 32-35 ("[T]he semiconductor devices of this invention will have at this interface a ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds that is substantially greater than ratio of naturally occurring deuterium to hydrogen.").)

The University next argues that Lisenker teaches away from the claimed invention "because the deuterium added during a pre-fabrication anneal would migrate away from the interface due to subsequent thermal processing required to fabricate the metal layers." (Prelim. Resp. 7.) We do not find this argument persuasive.

As we already have discussed above, Lisenker is not limited to substituting deuterium for hydrogen only during pre-metal annealing. Rather, Lisenker teaches that it "can be implemented throughout the VLSI fabrication procedure" including during the "various doping, etching,

annealing, deposition, cleaning, passivation, and oxidation steps" of a typical fabrication procedure. (P. 8, ll. 29-35.)

Moreover, the University's teaching away argument is directly at odds with the Lisenker disclosure, which states:

The regions where the deuterated bonds provide the greatest benefit in terms of device performance is at the interface of silicon-silicon dioxide layers. Thus, the semiconductor devices of this invention will have at this interface a ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds that is substantially greater than ratio of naturally occurring deuterium to hydrogen. (P. 10, 11. 29-35.)

The University also argues that post-metal deuterium annealing (as opposed to pre-metal deuterium annealing) yielded results that were unexpected at the time of the filing of the '533 Patent. But, it does not cite to the prosecution history of the '533 Patent in support of this argument or otherwise direct us to evidence sufficient to show unexpected results. (Prelim. Resp. 7-8.) From our own review of the '533 Patent disclosure, we cannot find any recognition or even mention of results (whether expected or unexpected) from post-metal deuterium annealing versus pre-metal deuterium annealing. Rather, the disclosure is focused on the broader concept of simply whether to use deuterium at all. (*See, e.g.,* col. 2, Il. 22-25 ("It has been discovered that semiconductor devices, for example including MOS devices, can be advantageously treated with deuterium to improve their operational characteristics."))

The '533 Patent does not distinguish between the benefits of pre- and post-metal deuterium annealing, and repeatedly teaches that the invention involves either (or both). (*See, e.g.,* col. 4, ll. 32-35 ("In accordance with the invention, the semiconductor device will be treated with deuterium *during or*

after completion of fabrication so as to condition the device to improve its operating characteristics.") (emphasis added); col. 4, ll. 40-44 ("in preferred aspects of the present invention, *during or subsequent to the fabrication* of device (e.g. subsequent to fabricating the gate, source and drain contacts), deuterium, either in atomic, ionic or molecular form, is disposed at the interface"); col. 4, ll. 48-53 ("deuterium conditioning or passivation of the device 12 can be achieved in a variety of ways. For instance, device 11 can be heated in the presence of a flowing, mixed or static deuterium-enriched ambient at one or more stages of fabrication, and/or after fabrication is completed").)

Based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 1 would have been obvious over Lisenker to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

2. Claim 2

Independent claim 2 requires "annealing the device in an ambient including deuterium at a temperature above about 200° C. and below a decomposition or melting temperature of said structure to form a concentration of deuterium at said interface region *effective to substantially reduce degradation of said device associated with hot carrier stress by increasing a practical lifetime at least about 10 times that provided by a corresponding passivation with hydrogen, where practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.*" (emphasis added).

Lisenker discloses conducting the deuterium annealing preferably at about 500° C. (P. 9, 1. 20.) This is within the claimed temperature range,

which we have construed to include from about 200° C. to at least about 1,000° C.

The italicized portion of the above-quoted limitation is the inherent result of the claimed process. Also, Lisenker expressly recognizes that "the deuterium containing devices of the present invention have improved stability, quality, and reliability." (P. 5, 11. 4-5.)

Accordingly, based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 2 would have been obvious over Lisenker to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

3. Claim 3

Claim 3 depends from claim 2 and additionally recites "wherein said temperature is about 400° C." Lisenker discloses conducting the deuterium annealing "preferably" at about 500° C and one atmosphere of pressure but notes that other acceptable conditions would be apparent to a person of skill in the art. (P. 9, 1l. 20-25.) Dr. Reed has testified that post-metal anneals are generally conducted at about 400° C. to about 500° C. (Reed Decl. ¶¶ 15-16.) Thus, based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 3 would have been obvious over Lisenker to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

4. Claim 4

Claim 4 depends from claim 1 and additionally recites "wherein said deuterium-enriched ambient comprises deuterium gas and one or more inert gases." Lisenker discloses this additional limitation with nitrogen used as the inert gas. (P. 8, 1. 37 - p. 9, 1. 1.) Thus, based on the record before us,

there is a reasonable likelihood that Micron will prevail on its assertion that claim 4 would have been obvious over Lisenker to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

5. Claim 5

Claim 5 depends from claim 4 and additionally recites "wherein said ambient includes 1% to 100% by volume deuterium gas." Lisenker discloses this additional limitation with specific examples of 50% deuterium and "pure" (100%) deuterium. (P. 6, ll. 16-22.) Thus, based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 5 would have been obvious over Lisenker to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

6. Claim 6

Claim 6 depends from claim 1 and additionally recites that the "ambient comprises deuterium gas and one or more of hydrogen, nitrogen, argon, and helium gas." Lisenker discloses this additional limitation wherein the ambient is a mixture of deuterium gas (D_2) and nitrogen gas (N_2). (P. 8, 1. 37 – p. 9, 1. 1.) Thus, based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 6 would have been obvious over Lisenker to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

7. *Claim* 7

Claim 7 depends from claim 1 and additionally recites "wherein said insulative layer comprises an oxide or nitride of silicon." Lisenker discloses this additional limitation wherein the insulative layer is silicon dioxide. (P. 4, ll. 20-27.) Thus, based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 7 would have

been obvious over Lisenker to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

8. Claim 8

Claim 8 depends from claim 1 and additionally recites "annealing said device at a temperature of at least about 400° C." Lisenker discloses this additional limitation wherein the temperature is about 500° C. (P. 9, 1. 21.) Thus, based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 8 would have been obvious over Lisenker to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

C. Claims 1-8 As Obvious Over Lisenker In View Of Ito

Micron relies on Ito as providing an express teaching of the thickness limitations required by independent claims 1 and 2. (Pet. 21.) We credit the testimony of Dr. Reed that, at the time of filing the '533 Patent, it would have been apparent to a person of ordinary skill in the art to employ insulating layers as small as 30 Angstroms in Lisenker as taught by Ito. (Reed Dec. ¶¶ 43-44.)

Based on the present record, there is a reasonable likelihood that Micron will prevail on its assertion that claims 1-8 would have been obvious over Lisenker in view of Ito to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

D. Claims 1-8 As Obvious Over Deal In View Of Lisenker

Micron asserts that Deal teaches the subject matter of claim 1 except that Deal employs hydrogen for the post-metal anneal instead of deuterium. (Pet. 25-27.) We agree and note that the University has not, in its Preliminary Response, disputed the asserted teachings of Deal.

Micron next asserts that it would have been obvious for a person of ordinary skill in the art at the time of the invention of the '533 Patent to modify Deal to employ deuterium instead of hydrogen as taught by Lisenker. We credit the testimony of Dr. Reed and in particular that portion set forth at paragraph 50 of his testimony, which states:

At the time of the priority date of the '533 patent, the benefits of substituting deuterium for hydrogen were known. As I have discussed previously, Lisenker teaches the substitution of deuterium for hydrogen and states that such a substitution results in "bonds that are less likely to break when exposed to electrical stresses," which improves device "stability, quality, and reliability." [Lisenker 5, II. 2-5.] It would have been apparent to incorporate the teachings of Lisenker with the '380 patent [Deal] because both references are directed to improving the quality of the Si/SiO2 interface, which has a direct impact on the device quality. Lisenker suggests that "any hydrogen containing material used in VLSI fabrication can be replaced with corresponding deuterium containing material," [Lisenker 4, II. 32-34.] which would include the '380 patent's postmetallization anneal.

Based on the present record, there is a reasonable likelihood that Micron will prevail on its assertion that claims 1-8 would have been obvious over Deal in view of Lisenker to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

E. Claims 1-8 As Obvious Over Deal In View Of Ito and Lisenker Micron relies on Ito as providing an express teaching of the thickness limitations required by independent claims 1 and 2. (Pet. 43.) We credit the testimony of Dr. Reed that, at the time of filing the '533 Patent, it would have been apparent to a person of ordinary skill in the art to employ in Deal

(in view of Lisenker) insulating layers as small as 30 Angstroms as taught by Ito. (Reed Dec. ¶¶ 47-48.)

Based on the present record, there is a reasonable likelihood that Micron will prevail on its assertion that claims 1-8 would have been obvious over Deal in view of Ito and Lisenker to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

F. Other Asserted Grounds

The other asserted grounds of the Petition (*see* pp. 3-4) are unnecessary as cumulative in light of the determination that there is a reasonable likelihood that claims 1-8 are unpatentable as set forth above. Accordingly, the Petition is denied as to these other asserted grounds.

SUMMARY

Petitioner, Micron, has demonstrated that there is a reasonable likelihood of prevailing on its challenge to the patentability of all claims of the '533 Patent.

The Petition is granted as to the following grounds:

- I. Claims 1-8 as obvious over Lisenker;
- II. Claims 1-8 as obvious over Lisenker in view of Ito;
- III. Claims 1-8 as obvious over Deal in view of Lisenker; and
- IV. Claims 1-8 as obvious over Deal in view of Lisenker and Ito.

ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is granted as to claims 1-8 of the '533 Patent on the grounds identified as I - IV above;

FURTHER ORDERED that the Petition is denied on all grounds not identified as I - IV above;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), inter partes review of the '533 Patent is hereby instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; and

FURTHER ORDERED that an initial conference call with the Board is scheduled for 2:00 PM ET on April 9, 2013. The parties are directed to the Office Trial Practice Guide, 77 Fed. Reg. 48756, 48765-66 (Aug. 14, 2012) for guidance in preparing for the initial conference call, and should come prepared to discuss any proposed changes to the Scheduling Order entered herewith and any motions the parties anticipate filing during the trial.

PETITIONER:

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