

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTEL CORPORATION,  
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,  
Patent Owner.

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Case IPR2018-00756  
Patent 6,346,736 B1

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Before DAVID C. McKONE, MATTHEW R. CLEMENTS, and  
SCOTT E. BAIN, *Administrative Patent Judges*.

Opinion for the Board filed by *Administrative Patent Judge* BAIN.

Opinion Dissenting filed by *Administrative Patent Judge* CLEMENTS.

BAIN, *Administrative Patent Judge*.

DECISION  
Denying Institution of *Inter Partes* Review  
35 U.S.C. § 314(a)

## I. INTRODUCTION

Intel Corporation (“Petitioner”) filed a Petition for an *inter partes* review of claims 6–9, 11, 13, 14, 16, and 20 of U.S. Patent No. 6,346,736 B1 (“the ’736 patent,” Ex. 1103). Paper 2 (“Pet.”). Godo Kaisha IP Bridge 1 (“Patent Owner”) timely filed a Preliminary Response. Paper 9 (“Prelim. Resp.”). We have jurisdiction under 35 U.S.C. § 314.

Upon consideration of the Petition, the Preliminary Response, and the evidence of record, we determine that the Petition presents substantially the same prior art or arguments as those previously presented to the Office and, therefore, we exercise our discretion under 35 U.S.C. § 325(d) to deny institution of an *inter partes* review.

## II. BACKGROUND

### *A. Related Matters*

Petitioner identifies *Godo Kaisha IP Bridge 1 v. Intel Corporation*, Case No. 2:17-cv-00676 (E.D. Tex.), as a matter that may “affect, or be affected by” a decision in this proceeding. Pet. 1; 37 C.F.R. § 42.8(b)(2). Also, in addition to this Petition, Petitioner has filed another petition for an *inter partes* review of the ’736 patent (claims 1–5), in a case designated IPR2018-00753.

### *B. The ’736 patent*

The ’736 patent, titled “Trench Isolated Semiconductor Device,” issued on February 12, 2002. Ex. 1103, [45], [54]. The application was filed on December 22, 1999 as U.S. Application No. 09/469,498 (“the ’498 application,” Ex. 1104), and is a divisional of U.S. Application No. 08/978,137 (“the ’137 application,” Ex. 2101) filed on November 25, 1997. Ex. 1103, [22]. The ’137 application eventually issued as U.S. Patent No.

6,130,139. *Id.* at [62]. The '736 patent claims priority to JP 08-314762, filed on November 26, 1997, and JP 09-023844, filed on February 6, 1997. *Id.* at [30].

The '736 patent is directed to a semiconductor device featuring reduced “total wiring-to-substrate capacitance” and higher operating speed. Ex. 1103, Abstract, 1:6–10. According to the '736 patent, as semiconductor devices have become “increasingly miniaturized” and “higher-density,” a “trench isolation technique” has been used to provide insulation between individual elements within the semiconductor. *Id.* at 1:10–15. Trench isolation involves forming a “trench” in a semiconductor substrate and filling it with insulating material, in order to electrically isolate the elements separated by the trench. *Id.* at 1:16–18. The insulating material’s surface is then made planar with the top of the semiconductor substrate, by chemical mechanical polishing (“CMP”). *Id.* at 1:19–24.

The '736 patent describes that when the area of trench isolation is large, the CMP sometimes becomes uneven, so to avoid this problem “dummy semiconductor structures” are included in the isolation regions. *Id.* at 1:24–29. Dummy semiconductor structures are portions of the substrate not dug out when forming the trench, and ensure that there is a uniform density of trenches and substrate across the entire surface. *Id.* at 1:24–34. An example of a device using such dummy semiconductor structures is shown in Figure 19 of the '736 patent, reproduced below.

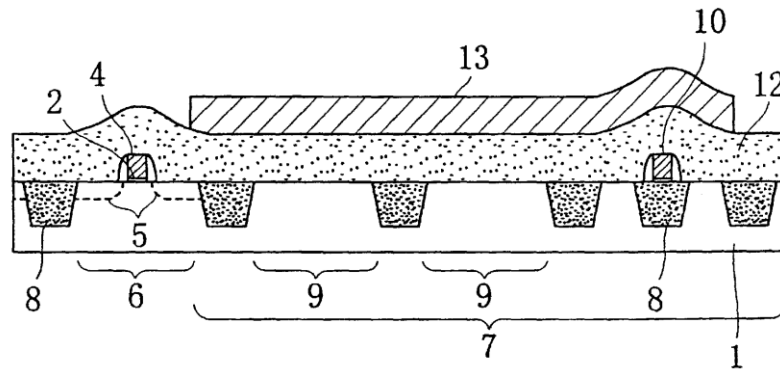


Fig. 19 PRIOR ART

Figure 19, labeled “PRIOR ART” in the ’736 patent, is a “cross-sectional view of a conventional semiconductor device,” including isolation region 7 with dummy “semiconductor portions 9” interspersed between “trench portions 8” (filled with a silicon oxide film). *Id.* at 1:35–51. A metal “wire 13” is separated from silicon substrate 1 by an interlayer insulating film 12. *Id.*

According to the ’736 patent, the “prior art” arrangement depicted above produces undesirable side effects. Specifically, the inclusion of dummy semiconductor portions 9 in the isolation region 7 results in slower operating speeds due to an increased capacitance between the wire 13 and the substrate 1, referred to as “wiring-to-substrate capacitance.” *Id.* at 2:50–67, 3:24–29 (emphasis added). The wiring-to-substrate capacitance causes charge traveling through the wire 13 to accumulate above the interlayer insulating film 12 instead of continuing along the wire 13 to the part of the circuit where the charge is intended to go. *Id.* at 3:33–48. As a result, the operating speed of the device decreases. *Id.* at 3:24–29.

To overcome these side effects, the ’736 patent discloses several solutions in various embodiments. One such embodiment includes a PN junction buried within the semiconductor substrate and below the interlayer

insulating film. *Id.* at 29:45–61. The elements of this embodiment are recited in claim 1 of the '736 patent, which is not at issue in this proceeding. *See* IPR2018-00753, Paper 11 (related proceeding, discussing claim 1).

An alternative embodiment, the elements of which are recited in independent claim 6, features “a dielectric film” layered between the semiconductor substrate and the interlayer insulating film. *Id.* at 24:35–37, 30:12–28. This “dielectric film” embodiment is illustrated in Figure 12, reproduced below.

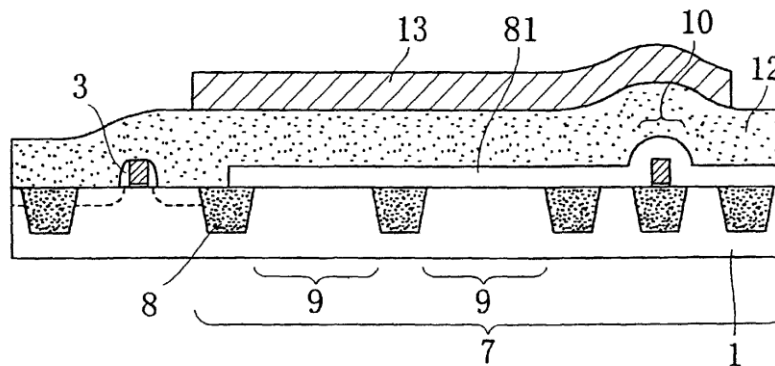


Fig. 12

Figure 12 is a cross section of a semiconductor device isolation region 7 (including dummy semiconductor portions 9) and wire 13 separated by “underlying insulating film 81,” which the Specification describes as a dielectric “preferably composed of at least one of a silicon oxide film and a silicon nitride film.” *Id.* at 4:58–59, 23:1–27, 24:34–43. The dielectric film layer (underlying insulating film 81) increases the distance between the wire and the substrate, and thereby decreases wiring-to-substrate capacitance.

*Id.* at 24:34–48.<sup>1</sup> The decreased capacitance improves operating speed of the device. *Id.* at 24:42–44.

Another alternative embodiment, the elements of which are recited in independent claim 13, features a “resistor film” formed between the interlayer insulating film and substrate. *Id.* at 16:19–35, 31:1–18. This “resistor film” embodiment is shown in Figure 5, reproduced below.

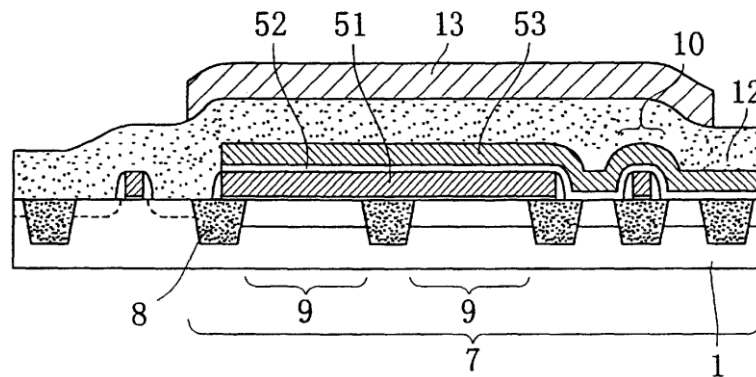


Fig. 5

Figure 5 depicts a cross section of a semiconductor device, with semiconductor device isolation region 7 (including dummy semiconductor portions 9) and wire 13 separated by “silicon oxide film 52” and “high resistor film 53” (resistor film). *Id.* at 15:53–16:35. The resistor film reduces the charge accumulation on the surfaces of the interlayer insulating film 12 by decreasing the voltage across the interlayer insulating film. *Id.* at 16:19–35. This reduces the “time required for charging or discharging between the wiring and high resistor[,] resulting in the semiconductor device operating at a higher speed.” *Id.* at 16:32–35.

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<sup>1</sup> Capacitance is inversely proportional to the distance between two conducting plates (e.g., the substrate and the wire). *Id.* at 24:39–43.

*C. Illustrative Claims*

Independent claims 6 and 13, the sole independent claims at issue in this proceeding, are illustrative of the claimed subject matter and recite (with emphases added to indicate the differences in the claims):

6. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and

*a dielectric film interposed between at least said dummy semiconductor portions of said isolation region and said interlayer insulating film.*

13. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and

*a resistor film formed under said wire, and between said interlayer insulating film and at least said dummy semiconductor portions of said isolation region.*

Ex. 1103, 30:12–27, 31:1–18.

*D. The Asserted Ground of Unpatentability*

Petitioner asserts a single ground of unpatentability under 35 U.S.C. § 103(a), challenging claims 6–9, 11, 13, 14, 16, and 20 of the '736 patent based on the following combination:

1. “Admitted Prior Art” (“APA”) disclosed in the '736 patent, including: Figures 19, 20(a)–20(g), 21(a), and 21(b) (each labeled “PRIOR ART”), column 1, lines 35–37 (“conventional” trench-isolated semiconductor), and column 1, lines 60–62 (“conventional” trench-isolated semiconductor);

and

2. Oshima (U.S. Patent No. 5,814,848; issued September 29, 1998) (Ex. 1118, “Oshima”).

Pet. 3–5. Petitioner also relies on the testimony of its expert, Dr. John C. Bravman, in support of its unpatentability challenge. *See* Ex. 1101 (“Bravman Decl.”).

In the Preliminary Response, Patent Owner disputes Petitioner’s asserted ground in two respects, contending (1) the APA is not “prior art consisting of patents or printed publications” under 35 U.S.C. § 311(b), and (2) that we should exercise our discretion under 35 U.S.C. § 325(d) and deny institution, because substantially the same art and arguments were considered during examination of the '736 patent. *See generally* Prelim. Resp.



### III. ANALYSIS

#### *A. Claim Construction*

The '736 patent is expired. Prelim. Resp. 14; Ex. 1103, [62]. Our review of claim terms of an expired patent is similar to that of a district court's review. *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012). Specifically, we apply the principle that the words of a claim are given their ordinary and customary meaning, as understood by a person of ordinary skill in the art at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). In determining the meaning of a claim limitation, we look principally to the intrinsic evidence of record, examining the claim language, the written description, and the prosecution history, if in evidence. *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Neither party proposes explicit constructions for any claim limitations at this stage of the proceeding. Pet. 34; Prelim. Resp. 14. We determine that no claim term requires express construction. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”).

#### *B. Principles of Law*

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying

factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art;<sup>2</sup> and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

*C. Overview of Prior Art Relied Upon by Petitioner*

*1. “Admitted Prior Art” in ’736 Patent<sup>3</sup>*

Petitioner’s challenge in this proceeding is based primarily on the alleged APA in the ’736 patent. Pet. 26–27; *see also id.* at 10, 34–36, 40–81. Specifically, Petitioner contends the APA discloses *every* limitation in claim 6 except the last one, i.e., “a dielectric film interposed between at least said dummy semiconductor portions of said isolation region and said interlayer insulating film.” Pet. 26–27. Similarly, Petitioner contends the APA discloses *every* limitation in claim 13 except the last one, i.e., “a resistor film formed under said wire, and between said interlayer insulating

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<sup>2</sup> Petitioner asserts that a person of ordinary skill in the art at the time of the invention would have had at least a B.S. degree in electrical engineering, materials science or engineering, or chemical engineering (or equivalent education), and would have two or three years of experience with integrated circuit manufacturing, fabrication, and structures. Pet. 33 (citing Ex. 1101 ¶¶ 75–76). Patent Owner does not dispute Petitioner’s characterization, nor offer its own description of the level of ordinary skill in the art. Accordingly, we adopt Petitioner’s description of the level of ordinary skill, for purposes of this decision.

<sup>3</sup> For the reasons discussed in Section III.D, *infra*, we do not reach Patent Owner’s argument that the alleged APA cannot be a basis of any ground of unpatentability under 35 U.S.C. § 311(b) (which limits grounds of asserted unpatentability to “prior art consisting of patents and printed publications”). Prelim. Resp. 15–16.

film and at least said dummy semiconductor portions of said isolation region.” *Id.*

The alleged APA includes Figure 19 of the ’736 patent, which is labeled “PRIOR ART.” *See supra* Sect. II.B (Figure 19 reproduced). According to Petitioner, Figure 19 depicts the following elements recited in claims 6 and 13 and thus indicates these elements were known to one of ordinary skill in the art: substrate (Fig. 19 element 1); active region (Fig. 19 element 6); isolation region (Fig. 19 element 7); first trench portion and second trench portion (Fig. 19 element 8, multiple depictions); dummy semiconductor portions (Fig. 19 element 9); interlayer insulating film (Fig. 19 element 12); and wire (Fig. 19 element 13). Pet. 10, 26; *see supra* Sect. II.B (Figure 19).

Petitioner further asserts that the APA includes a disclosure in the ’736 patent that using a trench isolation technique tends to “increase[e] the wiring-to-substrate capacitance,” thereby “reducing the operating speed of the semiconductor device.” Ex. 1103, 1:7–15, 3:1–30; Pet. 37. Petitioner contends that this disclosure would have motivated ordinary skill in the art to combine the APA with Oshima, discussed below, which Petitioner contends teaches the final element of each of claims 6 and 13 (the dielectric film and resistor film, respectively). Pet. 37; *see also id.* 49–52.

## 2. Oshima

Oshima is directed to a “semiconductor integrated circuit having reduced wiring capacitance.” Ex. 1118, [54]. Oshima’s disclosure describes “circuit block [i.e., active] regions” and a “bus line region” containing “bus lines [] and wires.” *Id.* at 4:50–56. Oshima discloses various methods of





said dummy semiconductor portions of said isolation region and said interlayer insulating film.” *Id.* at 26–27, 41–58; *see supra* Sect. III.C.1. The dielectric film limitation, Petitioner argues, is disclosed in Oshima. *Id.* at 57–58.<sup>5</sup> Specifically, Petitioner asserts Oshima discloses an “oxide film 12 is interposed between the field oxide film 4 of the bus line region 3 and the interlayer insulating film 6,” which “markedly reduce[s] the wiring capacitance.” Pet. 57–58; Ex. 1118, Fig. 2E, 1:56–62, 5:37–44; *see also id.* at 4:47–6:33, 5:13–20 (“the thicker the oxide film 12 is, the better will be the result.”).

Regarding independent claim 13, Petitioner argues that the APA discloses every limitation except “a resistor film formed under said wire, and between said interlayer insulating film and at least said dummy semiconductor portions of said isolation region.” Pet. 26–27, 41–62; *see supra* Sect. III.C.1. The resistor film limitation, Petitioner argues, is disclosed in Oshima’s description of “a poly silicon layer 9 [] formed . . . all over the surface of the entire field oxide film 4,” as shown in Oshima Figures 2A–2E. *Id.* at 59–62 (citing Ex. 1118, 4:47–5:21); *see supra* Sect. III.C.2. Alternatively, Petitioner contends the resistor film limitation is disclosed in Oshima’s description of “poly silicon film 9,” an alternative embodiment of Oshima shown in Figure 3. Pet. 61; Ex. 1118, 6:37–42; *see supra* Sect. III.C.2.

Petitioner argues it “would have been obvious to a person of ordinary skill in the art to integrate Oshima’s oxide film 12 (claim 6) or poly silicon

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<sup>5</sup> Petitioner “alternatively” argues that Oshima discloses some of the other elements recited in claims 6 and 13, i.e., partially redundant to some disclosures in the APA. *See, e.g.*, Pet. 58, 64, 72.

layer 9 (claim 13) into the APA, which [] expressly discloses all other elements” of these claims, based upon teachings in both references that it is desirable to reduce wire-to-substrate capacitance in semiconductor devices formed using the trench isolation technique. Pet. 62–63.

Patent Owner responds that Petitioner’s challenge “essentially repackages art, arguments and issues already considered by the Patent Office” in examination of the ’736 patent, and that the Board should, therefore, exercise its discretion under 35 U.S.C. § 325(d) to deny institution. Prelim. Resp. 1, 18–48. Patent Owner contends the Office “cited and discussed the []APA in detail during prosecution” of the ’736 patent family, and “explicitly considered the same substance of the []APA that Petitioner cites.” *Id.* at 19. Moreover, Patent Owner asserts that although Oshima was not considered during prosecution, the Office considered Ishimaru and Suzuki, which have the “same structures” as Oshima, for “substantially the same disclosures as Oshima.” *Id.* at 20, 25.

For the reasons explained below, we agree with Patent Owner’s foregoing assertions, and we exercise our discretion under 35 U.S.C. § 325(d) to deny institution.

*1. Discretion Under 35 U.S.C. § 325(d)*

Institution of *inter partes* review is discretionary. *See Harmonic Inc. v. Avid Tech, Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”). Section 325(d) grants us the express discretion to deny a petition when “the same or substantially the same prior art or arguments previously were presented to the Office.” 35 U.S.C. § 325(d).

In evaluating whether to exercise our discretion under Section 325(d), we weigh the following non-exclusive factors: “(a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art; (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of prior art or arguments.” *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, slip op. at 17–18 (Paper 8, Dec. 15, 2017) (informative).

We analyze these factors below, in view of the record in this case, and find that, on balance, the factors weigh in favor of exercising our discretion under 35 U.S.C. § 325(d).

*(a) The similarities and material differences  
between the asserted art and the prior art  
involved during examination*

Petitioner relies on the combination of APA and Oshima as establishing obviousness of claims 6–9, 11, 13, 14, 16, and 20. Pet. 3–5, 40–81. As discussed below, the Office explicitly considered and discussed Petitioner’s primary reference, the APA, during examination of the ’137 application. Ex. 2101, 335–37 (file history of the ’137 application); *see supra* Sect. II.B (explaining that the ’736 patent issued from the ’498 application, which is division of the ’137 application). Although the Office



did not consider Petitioner’s secondary reference, Oshima, during examination of the ’137 and ’498 applications, we find that Ishimaru and Suzuki – references the Office did consider and analyze in the examination of the ’498 application – are substantially similar to Oshima. The record reflects that the Office considered and analyzed the same disclosures in Ishimaru and Suzuki that Petitioner now relies upon in Oshima. Ex. 1104, 164–166, 186–189.

Regarding the APA, Petitioner asserts that Figure 19 of the ’736 patent discloses every limitation of claim 6 of the ’736 patent except the “dielectric film.” Pet. 26–27, 40–58. During examination of the ’137 application, the Office considered Figures 20(a)–(g) as “admitted prior art” for essentially the same disclosures as Figure 19. Ex. 2101, 335–37. Figures 20(a)–(g) (also labeled “PRIOR ART”) illustrate a “process of manufacturing the conventional semiconductor device” that is shown in Figure 19. Ex. 1103, 1:60–63, 11:18–20.<sup>6</sup> Figure 20(g) is reproduced below.

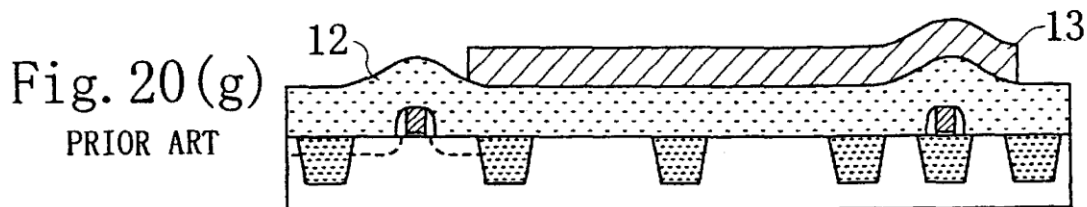


Figure 20(g) depicts a cross section of a “conventional” semiconductor device following a series of fabrication steps (previous steps being shown in Figures 20(a)–(f)). Ex. 1103, 2:37–39, 11:19–20. In Figure

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<sup>6</sup> The Examiner’s citation to Figures 20(a)–(g) in this portion of the file history referred to then-pending claim 19, which was directed to a method of manufacturing (fabricating) the semiconductor device. Ex. 2101, 336–37.

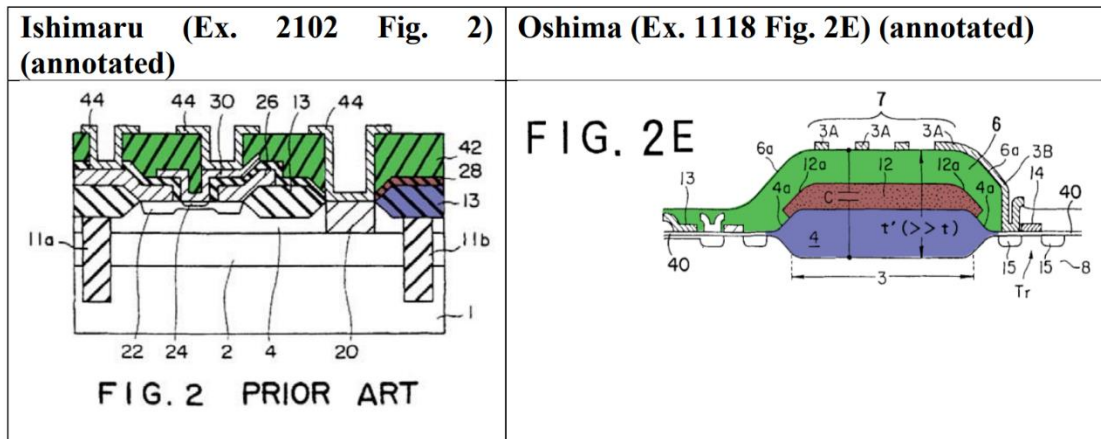
20(g), silicon oxide film has been deposited to form “interlayer insulating film 12,” upon which “wire 13” is formed. *Id.* at 2:37–39.

The result of the fabrication process shown in APA Figure 20(g), expressly considered by the Office in the ’137 examination, is identical to the structure shown in APA Figure 19 relied on by Petitioner. *Compare* Ex. 1103, Fig. 19 *with id.*, Fig. 20(g). Moreover, the entirety of the APA was before the Office during examination of the ’137 and ’498 applications because the APA, as defined by Petitioner, is contained within those applications.

The Office did not consider Oshima during prosecution. Prelim. Resp. 20. The Office, however, considered Ishimaru, which features the same “dielectric film” that Petitioner alleges is disclosed in Oshima. Ex. 1104, 163–164 (file history of ’736 patent). The Examiner found Ishimaru discloses a “dielectric film (28, Fig. 2) interposed between interlayer insulating film and said semiconductor portions and trench portion.” *Id.* at 164. An illustrative comparison of Ishimaru Figure 2 and Oshima Figure 2E, as annotated in the Preliminary Response (at 21), is reproduced below.<sup>7</sup>

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<sup>7</sup> Patent Owner’s annotated Ishimaru Figure 2 and Oshima Figure 2E are identical to the original figures in those references, with the addition of color.



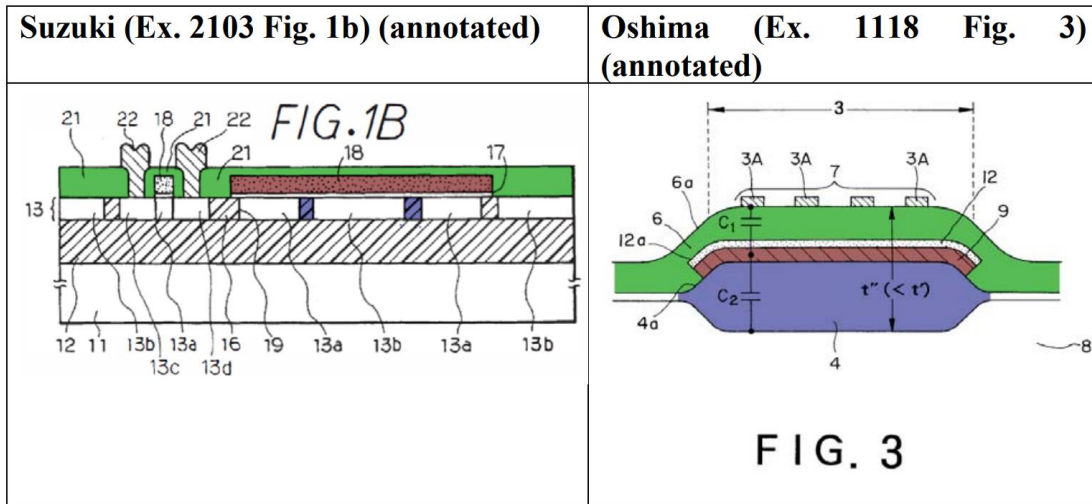
Ishimaru Figure 2, which was before the Office, depicts a semiconductor device including buried layer 2, substrate 1, and a dielectric film (“insulating layer 28”) located between an oxide film (“separation region 13”) and an insulating film (“interlayer insulating film 42”).

Ex. 2102, 1:43–51. Similarly, Petitioner’s asserted prior art, Oshima Figure 2E, illustrates a semiconductor device including a dielectric film (“oxide film 12”) located between an oxide film (“field oxide film 4”) and an insulating film (“interlayer insulating film 6”). Pet. 39–40; Ex. 1118, 1:43–51.

The dielectric film in both Ishimaru and Oshima is utilized to increase the insulating film thickness in the isolation region, thereby decreasing capacitance. Ex. 2102, 1:33–36; Ex. 1118, 5:40–44. Although Ishimaru does not disclose a wire above semiconductor portions and a second trench portion, neither does Oshima. Ex. 1118, 1:45–57, Fig. 2E.

The Office also considered Suzuki, which features the same “resistor film” that Petitioner alleges is disclosed in Oshima. Ex. 1104, 164–65 (file history of ’736 patent). The Examiner found Suzuki discloses a “resistor film (18, Fig. 1B) formed between said interlayer insulating film and at least

said semiconductor portions of said isolation region.” *Id.* An illustrative comparison of Suzuki Figure 1B and Oshima Figure 3, as annotated in the Preliminary Response (at 25), is reproduced below.<sup>8</sup>



Suzuki Figure 1B, which was before the Office, depicts a semiconductor device including a resistor film (“gate wiring 18”) located between an oxide film (“insulating material 16”) and an insulating film (“interlayer insulating film 21”). Ex. 2013, 4:37–38, 6:24–25. Similarly, Petitioner’s asserted prior art, Oshima Figure 3, illustrates a resistor film (“polysilicon film 9”) located between an oxide film (“field oxide film 4”) and an insulating film (“interlayer insulating film 6”). Pet. 39–40; Ex. 1118, Fig. 3, 6:34–47.

In view of the foregoing, we find substantial similarities between the asserted art and the prior art involved during examination. Neither Petitioner nor Patent Owner identify any material differences between the asserted art and the prior art involved during examination.

<sup>8</sup> Patent Owner’s annotated Suzuki Figure 1B and Oshima Figure 3 are identical to the original figures in those references, with the addition of color.

*(b) The cumulative nature of the asserted art  
and the prior art evaluated during examination*

As discussed above, the APA, which constitutes Petitioner's primary reference, was expressly evaluated by the Office during examination of the '137 application. As further discussed above, Petitioner's secondary reference, Oshima, is structurally similar to Ishimaru and Suzuki, which were also evaluated by the Office during examination of the '498 application. Specifically, the particular structures in Oshima on which Petitioner relies in challenging claim 6 (the dielectric film) and claim 13 (the resistor film) are found in Ishimaru and Suzuki, respectively, and the Office expressly evaluated those structures. *See supra* subsection (a).

Because the Office expressly considered the APA, and Petitioner relies on Oshima for the same teachings that the Office evaluated in Ishimaru and Suzuki (*see supra* subsection (a)), we find the references in the Petition are substantially cumulative of art evaluated during examination. *See, e.g., Unified Patents, Inc. v. Berman*, IPR2016-01571, slip op. at 11–12 (Paper 10, Dec. 14, 2016) (Informative) (denying institution where secondary reference in petition was used “in substantially the same manner” as reference evaluated in prosecution).

*(c) The extent to which the asserted art was evaluated  
during examination, including whether the prior art  
was the basis for rejection*

The Office rejected claims in the '137 application based on the APA asserted by Petitioner. Ex. 2101, 335–37. Then-pending claim 19 of that application, directed to a method of fabricating a semiconductor device, recited limitations including a “semiconductor substrate,” an “active region,” an “isolation region,” “dummy semiconductor portions,” “first and second

trenches,” “buried” portions of said trenches, a “wire,” and an “interlayer insulating film” – essentially the same structures that Petitioner contends are disclosed in the APA. *Id.* at 131–32; *see also* Pet. 26–27. The Office rejected the claim as obvious over the APA and another reference, Kinoshita, which the Examiner relied on for its teaching of an additional element in then-pending claim 19. Ex. 2101, 335–37; *see also id.* (obviousness rejection over APA and Beitman).

As discussed above, the Office did not consider Oshima, but did rely on the structurally similar Ishimaru and Suzuki references for the same disclosure as the Petitioner cites in Oshima. *See supra* subsection (a). The Office rejected then-pending claims 1–9 of the ’498 application as anticipated by Ishimaru. Ex. 1104, 163–164. In particular, the Office rejected claims 4–7 based in part on Ishimaru’s disclosure of a “dielectric film (28, Fig. 2) interposed between an interlayer insulating film and semiconductor portions and trench portion.” *Id.* at 164. The Office further rejected then-pending claims 10–18 as anticipated by Suzuki. *Id.* at 164–65. In particular, the Office rejected the claims based in part on Ishimaru’s disclosure of a “resistor film (18, Fig. 1B) formed between said interlayer insulating film and at least said semiconductor portions of said isolation region.” *Id.* at 165.

Accordingly, we find a substantial portion of the art asserted in Petitioner’s challenge was evaluated during examination and was the basis for a rejection during examination.

*(d) The extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art*

As discussed above, the manner in which Petitioner relies on the prior art is substantially similar to the issues raised and considered in examination of the '137 and '498 applications.

Petitioner contends that the APA discloses every limitation of claims 6 and 13 except the “dielectric film” (claim 6) and “resistor film” (claim 13) limitations, which are disclosed in Oshima. *See, e.g.*, Pet. 26–27, 34–36, 59–62. Regarding claim 6, Petitioner argues it would have been obvious for a person of ordinary skill in the art to use the dielectric film of Oshima (oxide film 12) as the “dielectric film” of claim 6. *Id.* at 57–59. Regarding claim 13, Petitioner argues it would have been obvious for a person of ordinary skill in the art to use the resistor film of Oshima (polysilicon layer 9) as the “resistor film” of claim 13. *Id.* at 59–62.

The Office, however, however, applied the APA to the same limitations as Petitioner, and subsequently applied Ishimaru for the dielectric film limitation and Suzuki for the resistor film limitation. *See supra* subsections (a)–(c). Although the Office did not reject the claims in the '137 and '498 applications over the express combination of APA with Oshima, Petitioner does not argue (and the record does not reflect) how the arguments in the Petition are new, unique or materially different from those considered during examination. Moreover, the fact that Petitioner relies on the APA for nearly every element of claims 6 and 13, and the Office expressly considered the APA, is indicative of substantial overlap.

*(e) Whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art*

Petitioner does not make any express arguments regarding Examiner error in its Petition. Although Petitioner notes that Oshima was not considered during prosecution, Petitioner makes no corresponding statement about the APA. Pet. 38. Petitioner also does not point out or argue whether the Examiner erred in evaluating any of the prior art during prosecution, including prior art that is, as explained above, substantially similar to the prior art asserted here. *See supra* subsections (a)–(d).

Accordingly, we do not find that Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art.

*(f) The extent to which additional evidence and facts presented in the Petition warrant reconsideration of prior art or arguments*

On this record, we do not find any new or meaningful evidence or facts presented in the Petition that warrant reconsideration of the extensive prosecution history of the '736 patent, which involved the same and substantially similar prior art and arguments. Neither the Petition, nor the testimony of Dr. Bravman relied upon by Petitioner, reveal anything about the prior art or arguments in the prosecution history, beyond a generic summary. *See, e.g.*, Ex. 1101 ¶¶ 71–74. Moreover, neither the Petition nor the testimony of Dr. Bravman indicate how the analysis in the Petition is unique or more extensive than that conducted by the Office in evaluating the multiple applications in the '736 patent family.

We agree with Patent Owner's contention that the Office has already considered the structures cited by Petitioner, and the alleged motivations to combine. *See supra* subsections (a)–(d). Also, although Petitioner's expert, Dr. Bravman, testifies that a person of ordinary skill in the art at the time of



the invention would have considered it obvious to “integrate Oshima’s oxide film 12 or polysilicon layer 9 into the APA,” Dr. Bravman’s testimony does not offer any support for this contention, beyond information already considered by the Office. *See, e.g.*, Ex. 1101 ¶114 (asserting that the APA “readily provides the motivation” to combine in its description of undesirable side effects of wiring-to-substrate capacitance in shallow trench isolation semiconductors); Pet. 66–67.

## *2. Weighing the Factors*

In summary, Petitioner’s primary reference, the APA, was considered by the Office, and cited and discussed in rejections. Petitioner’s secondary reference, Oshima, is substantially similar to the Ishimaru and Suzuki references that were considered and cited by the Office, and is relied upon by Petitioner for the same structures teaching the same claim elements. Moreover, the arguments Petitioner advances in its Petition are substantially similar to those considered by the Office in examination and in rejecting the claims.

Taking into account the factors discussed above, on balance we find that they weigh in favor of exercising our discretion and denying institution under section 325(d).<sup>9</sup>

## IV. CONCLUSION

Based upon our review of the information presented in the Petition, the Preliminary Response, and the evidence of record, we exercise our

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<sup>9</sup> Although our discussion centers on independent claims 6 and 13 of Petitioner’s challenge, the dependent claims rely upon the same prior art and arguments. Neither of the parties argue, and the record does not indicate, that the dependent claims present any issues distinct from claims 6 and 13 under 35 U.S.C. § 325(d).

discretion under 35 U.S.C. § 325(d) and deny institution. Accordingly, the Petition is *denied*, and no trial is instituted.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is *denied*, and no trial is instituted.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTEL CORPORATION,  
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,  
Patent Owner.

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Case IPR2018-00753  
Patent 6,346,736 B1

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Before DAVID C. McKONE, MATTHEW R. CLEMENTS, and  
SCOTT E. BAIN, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*, dissenting.

I respectfully dissent from the majority’s application of 35 U.S.C. § 325(d) to the facts of this case. In my opinion, the asserted ground of unpatentability—that claims 6–9, 11, 13, 14, 16, and 20 are unpatentable under 35 U.S.C. § 103 as obvious over the combination of APA and Oshima—is not “substantially the same prior art or arguments” as overcome during prosecution of the challenged claims.

During prosecution, pending claims 4–7 and 9 (corresponding to challenged claims 6–9 and 11) were rejected under 35 U.S.C. § 102 as

anticipated by Ishimaru. Ex. 1004, 163–66. Applicants amended the claims into the form in which they issued (*compare* Ex. 1004, 179–183, 192–197 *with* Ex. 1001, 30:12–32:31) and argued that the amended claims are not anticipated by Ishimaru (Ex. 1004, 185–189) or by Suzuki (*id.* at 189–190).

With respect to Ishimaru, Applicants argued it did not anticipate pending claim 4 (issued claim 6) because it does not disclose the recited “second trench portion filled with an insulating material formed so as to separate a plurality of dummy semiconductor portions in the isolation region.” Ex. 1004, 186, 188 (referring to arguments about claim 1).

Applicants argued

Ishimaru fails to disclose a second trench portion filled with an insulating material formed so as to separate a plurality of dummy semiconductor portions in the isolation region. *Indeed, Ishimaru does not disclose or suggest the use of any dummy semiconductor portions.* For example, referring to Fig. 6, the two semiconductor portions disclosed therein are utilized to form a bipolar transistor and a MOS transistor. There are no dummy semiconductor portions.

Specifically, the trenches 11e, 11f and 11a of Fig. 5 and Fig. 6 as disclosed by Ishimaru all correspond with the first trench portion of the present invention. These trenches are formed to separate the bipolar transistor region from the MOS transistor region. Moreover, trenches 11g and 11d are formed to separate the base layer 22, which is formed in the bipolar transistor region (active region) from the buried collector lead electrode layer 20.

Thus, the plurality of trench portions (11a–11f) disclosed by Ishimaru do not correspond with the second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in isolation region as set forth in claims 1, 4, 10 and 12 of the present invention.

*Id.* (emphasis added). Applicants then argued that, because Ishimaru does not disclose any dummy semiconductor portions, it does not disclose the novel PN junction “formed in the dummy semiconductor portion” and does not disclose a wire formed on an interlayer insulating film “covering the dummy semiconductor portions.” *Id.* at 187. Finally, Applicants argued that the Examiner’s reliance on Figures 1 and 2 of Ishimaru, which depict prior art, in combination with Figures 5 and 6 of Ishimaru, which depict the invention of Ishimaru, was improper in an anticipation rejection. *Id.*

The Examiner subsequently issued a Notice of Allowance. *Id.* at 199.

Thus, Applicants overcame the anticipation rejection during prosecution by alleging that features known in the art—i.e., dummy semiconductor portions—were not disclosed in Ishimaru, and by arguing that it was improper to rely on a combination of Ishimaru’s Figures 1 and 2 with Ishimaru’s Figures 5 and 6. Both of these arguments were specifically tailored to the rejection, which was based on anticipation rather than obviousness.

Here, in contrast, the alleged ground of unpatentability is based on obviousness and the evidence shows that the recited “dummy semiconductor portions” were known in the art prior to the filing of the ’736 patent. Notwithstanding an examiner’s reliance on the APA during prosecution of the parent application of the ’736 patent, I am not persuaded that the Examiner of the challenged claims considered the APA when examining the challenged claims.

Because Applicants narrowly overcame the Ishimura rejection during prosecution based on arguments specific to anticipation and because the ground of unpatentability asserted by Petitioner is based on obviousness

over the combination of APA and Oshima, I believe the prior art and arguments are not “substantially the same” as “previously were presented to the Office” and, therefore, I would not exercise our discretion to deny institution under § 325(d). Instead, I would institute because I believe Petitioner has established a reasonable likelihood that it would succeed in showing that at least one challenged claim would have been obvious over the combination of APA and Oshima. Moreover, I am not persuaded that Petitioner’s reliance on APA in this case is improper. Patent Owner’s argument that “the Board has repeatedly held that AAPA alone does not qualify as a prior art patent or printed publication” (Prelim. Resp. 13) is not persuasive because Petitioner’s asserted ground of unpatentability relies upon a combination of APA with Oshima, not upon APA “alone.”

IPR2018-00756  
Patent 6,346,736 B1

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