

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION
Petitioner

v.

GODO KAISHA IP BRIDGE 1
Patent Owner

DECLARATION OF JOHN C. BRAVMAN UNDER 37 C.F.R. § 1.68 IN
SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 6,346,736

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I, John C. Bravman, do hereby declare as follows:

I. Introduction

1. I have been retained as an expert witness on behalf of Intel Corporation (“Intel”) for the above-captioned Petition for *Inter Partes* Review (“IPR”) of U.S. Patent No. 6,346,736 (“the ’736 Patent”) (Ex. 1103). I am being compensated for my time in connection with this IPR at my standard consulting rate of \$500 per hour. My compensation is not affected by the outcome of this matter.
2. I have been asked to provide my opinions regarding whether claims 6, 7-9, 11, 13, 14, 16, and 20 (“Challenged Claims”) of the ’736 Patent are invalid as anticipated or would have been obvious to a person having ordinary skill in the art at the time of the alleged invention.
3. The ’736 Patent issued on February 12, 2002, from U.S. Patent Appl. No. 09/469,498 (“the ’498 Application”), filed on December 22, 1999, which was a division of U.S. Patent Appl. No. 08/978,137, filed on November 25, 1997, now U.S. Patent No. 6,130,139. For the purposes of my Declaration, I have been asked to assume that the priority date of the alleged invention recited in the ’736 Patent is November 26, 1996.
4. The face of the ’736 Patent names Takaaki Ukeda, Chiaki Kudo, and Toshiki Yabu as the purported co-inventors and identifies Matsushita

Electric Industrial Co., Ltd. as the purported assignee of the '736 Patent. I have reviewed the Patent Office "Assignments on the Web" record for the '736 Patent. This record indicates that the original assignee, Panasonic Corporation (formerly Matsushita Electric Industrial Co., Ltd.), assigned the '736 Patent to Godo Kaisha IP Bridge 1 ("IP Bridge") on or around January 17, 2014 (Ex. 1105).

5. In preparing this Declaration, I have reviewed the '736 Patent, the file history of the '736 Patent ("736 Patent File History") (Ex. 1104), prior-art references, references from the time of the alleged invention, and statements made regarding the alleged meaning and scope of terms and phrases recited in the Challenged Claims.
6. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and I have considered the viewpoint of a person having ordinary skill in the relevant art as of the priority date of the '736 Patent. My opinions are based, at least in part, on the following:
 - Admitted Prior Art ("APA") from the '736 Patent (Ex. 1103)
 - U.S. Patent No. 5,814,848 ("Oshima") (Ex. 1118)
7. I have considered certain issues from the perspective of a person of ordinary skill in the art as described below at the time the '736 Patent was filed. In

my opinion, a person of ordinary skill in the art for the '736 Patent would have found the Challenged Claims of the '736 Patent invalid.

II. Background and Qualifications

8. My academic training was at Stanford University, where I received my Bachelor of Science degree in Materials Science and Engineering in 1979, and a Master of Science degree in 1981, also in Materials Science and Engineering. I completed my Doctor of Philosophy degree in Materials Science and Engineering in 1984, with a dissertation that focused on the nature of silicon — silicon dioxide interfaces as found in integrated circuit (“IC”) devices.
9. From 1979 to 1984, while a graduate student at Stanford, I was employed part-time by Fairchild Semiconductor in their Palo Alto Advanced Research Laboratory. I worked in the Materials Characterization group. In 1985, upon completion of my doctorate, I joined the faculty at Stanford as Assistant Professor of Materials Science and Engineering. I was promoted to Associate Professor with tenure in 1991, and achieved the rank of Professor in 1995. In 1997 I was named to the Bing Professorship.
10. At Stanford, I was Chairman of the Department of Materials Science and Engineering from 1996 to 1999, and Director of the Center for Materials Research from 1998 to 1999. I served as Senior Associate Dean of the

School of Engineering from 1993 to 2001 and the Vice Provost for Undergraduate Education from 1999 to 2010. On July 1, 2010, I retired from Stanford University and assumed the Presidency of Bucknell University, where I also became a Professor of Electrical Engineering.

11. I have worked for more than 35 years in the areas of thin film materials processing and analysis. Much of my work has involved materials for use in microelectronic interconnects and packaging, and in superconducting structures and systems. With regard to ICs, I led investigations involving aluminum, copper and tungsten metallizations, polycrystalline silicon, metal silicides, a variety of oxide and nitride dielectrics, and barrier layers such as titanium and tantalum-based nitrides. Further, my research blended fundamental aspects of the behavior of microelectromechanical systems—specifically, compliant multilayer cantilever beams—for possible test probe and package implementations. In this work my group investigated the mechanical behavior of package underfill systems, focusing on the relationship between microstructures, processing, and adhesion. I have also led multiple development efforts of specialized equipment and methods for determining the microstructural and mechanical properties of materials and structures. My group designed and built the first high voltage SEM for in-situ studies of electromigration, the first high temperature wafer curvature

system, and the first microtensile tester for micron-scale structures, amongst many others. As a graduate student I developed one of the earliest methodologies for obtaining high resolution cross section transmission electron micrographs of IC structures.

12. I have taught a wide variety of courses at the undergraduate and graduate level in materials science and engineering, emphasizing both basic science and applied technology, including coursework in the areas of IC materials and processing. Some of these courses focused on processes (*e.g.*, cleaning, etching, deposition, doping, oxidation, etc.) used in the production of IC. More than two thousand students have taken my classes, and I have trained 24 doctoral students, most of whom now work in the microelectronics industry.
13. I am a member of many professional societies, including the Materials Research Society, the Institute of Electrical and Electronic Engineers, ASM International, the Microscopy Society of America, and the American Physical Society. I served as President of the Materials Research Society in 1994.
14. A copy of my curriculum vitae (including a list of all of my publications) is attached as Exhibit 1102.

III. Understanding of Patent Law

15. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions.

My understanding of the law is as follows:

A. Claim Construction

16. I have been informed that claim construction is a matter of law and that the final claim construction will ultimately be determined by the Board. For the purposes of my analysis in this proceeding and with respect to the prior art, I have been informed that I should apply what is known as the “Phillips” standard.
17. I understand that the Phillips standard does not mean the broadest possible interpretation. Rather, unless a term has been given a specific definition, the meaning is the plain and ordinary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure.

B. Prior Art

18. I understand that prior art to the '736 Patent includes patents and printed publications in the relevant art that predate the priority date of the '736 Patent.

C. Anticipation

19. I understand that a claim is invalid if it is anticipated. Anticipation of a claim requires that every element of a claim be disclosed expressly or inherently in a single prior-art reference, arranged in the prior-art reference as arranged in the claim.

D. Obviousness

20. I understand that a claim is invalid, even if it is not anticipated, if it is obvious to a person having ordinary skill in the relevant art at the time of the alleged invention. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time the application was filed.
21. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:
- the level of ordinary skill in the art at the time the application was filed;
 - the scope and content of the prior art; and
 - what differences, if any, existed between the claimed invention and the prior art.

22. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to one having ordinary skill in the art. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;
- whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

23. I understand that one of ordinary skill in the art has ordinary creativity, and is not an automaton. While it may be helpful to identify a reason to combine multiple prior art references, common sense should guide, and there is no rigid requirement for a teaching, suggestion, or motivation to combine.
24. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.
25. I understand that certain factors—often called “secondary considerations”—may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

IV. Summary of Opinions

26. It is my opinion that every limitation described in the Challenged Claims of the '736 Patent are disclosed by the prior art, and are anticipated and/or rendered obvious by the prior art.

V. Brief Description of the Technology

27. The '736 Patent generally “relates to a semiconductor device having a trench-isolated structure and, more particularly, to a method of reducing the capacitance between the wiring and substrate of the semiconductor device.” '736 Patent at 1:6-9.

A. Semiconductor Devices

28. Modern integrated circuits (or “ICs”) are electrical circuits that include millions or billions of discrete semiconductor devices integrated together over a semiconducting base layer (or “substrate”) such as silicon. A semiconductor is a material that has a conductivity somewhere between a conductor (high conductivity) and an insulator (low conductivity), and which can be controlled over a wide range by the proper incorporation of small quantities of selected impurities called “dopants.”
29. Many of the semiconducting devices serve as electronic switches called “transistors.” Transistors are created by implanting dopant atoms that effectively add a charge to the substrate to make certain regions more conductive. The dopants can be either negative (“n-type”) or positive (“p-

type”). Applying a small voltage across one pair of the transistor’s terminals controls the current through another pair of terminals. In this way, a transistor can be used as an electronic switch that is either “off” or “on.” An “off” state usually corresponds to a digital “0,” while an “on” state usually corresponds to a digital “1” — this binary language forms the basis of modern computing.

30. Two types of transistors that are well-known in the art are metal-oxide semiconductor field effect transistors (MOSFETs) and bipolar junction transistors (BJTs). BJTs comprise an emitter region, a base region, and a collector region. Adjacent regions are oppositely doped (either “nnp” or “pnp”). Thus, in a pnp BJT transistor, illustrated below, there is a p-type emitter, an n-type base, and a p-type collector. See Sedra, Adel S., *Microelectronics Circuits* (3rd ed., 1991) (“Sedra”) at 11-12 (Ex. 1107).

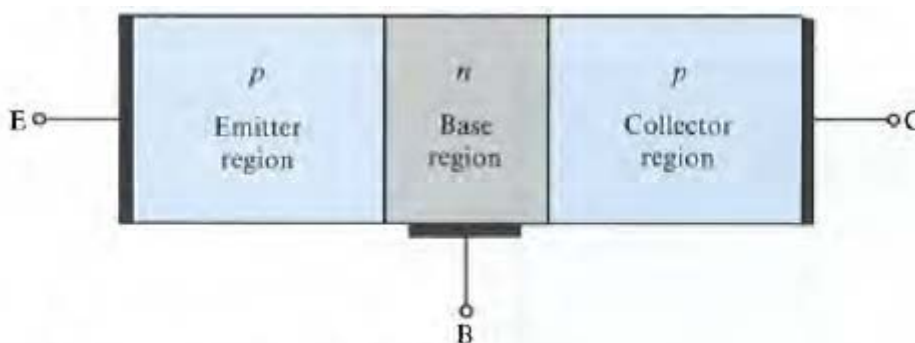


Fig. 4.2 A simplified structure of the *pnp* transistor.

MOSFETs have four doped regions: a source, a gate (or “gate electrode”), a drain, and the body (or substrate). In modern devices the gate is typically a

metal or metal silicide, and thus no longer considered “doped.” The source and drain terminals are doped regions of the substrate, while the gate is sits atop a dielectric layer, such as silicon dioxide or variants thereof. An illustration of a MOSFET transistor is shown below. *See id.* at 14-22.

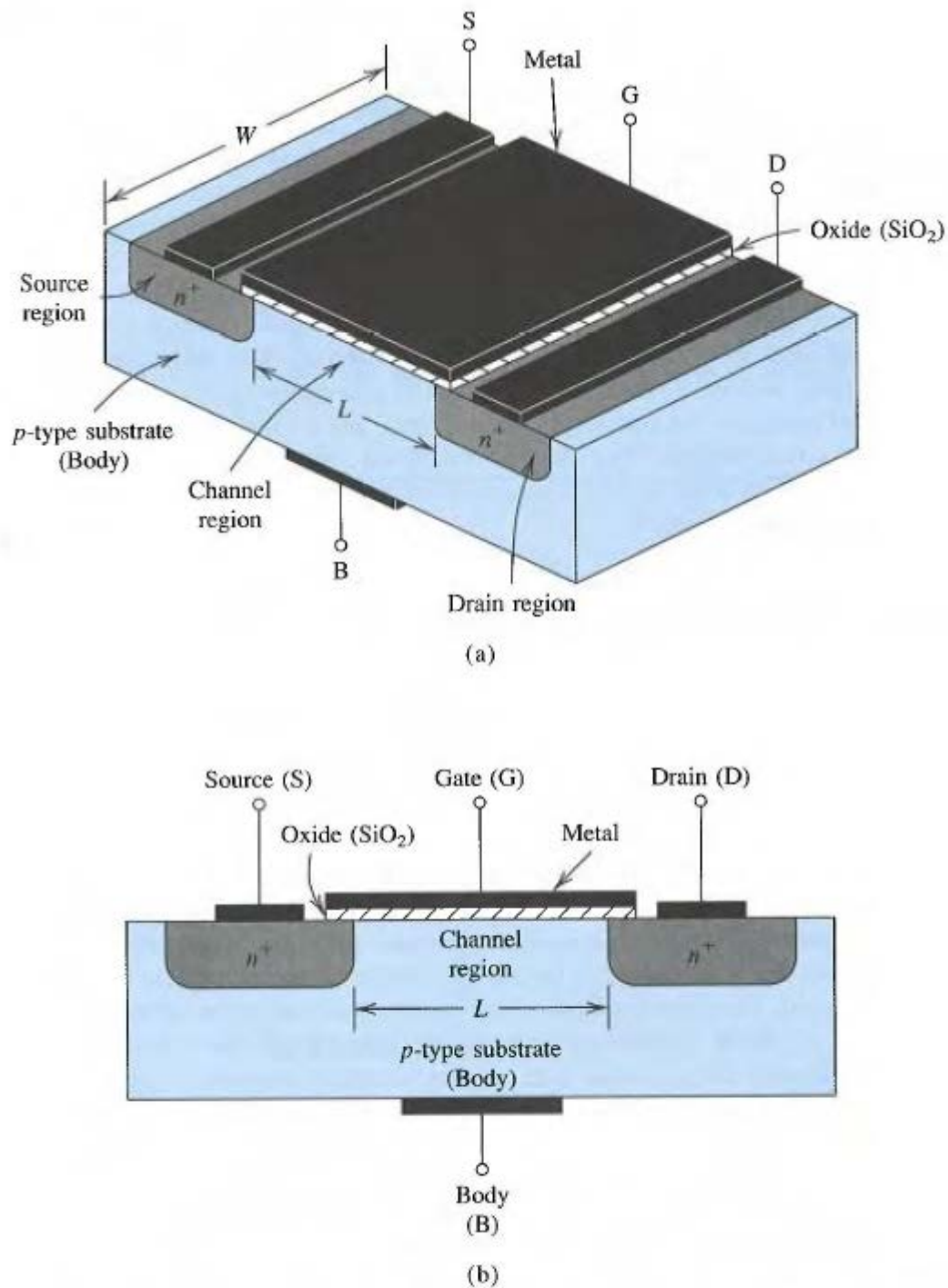


Fig. 5.1 Physical structure of enhancement-type NMOS transistor: (a) perspective view; (b) cross section. Typically $L = 1$ to $10\ \mu\text{m}$, $W = 2$ to $500\ \mu\text{m}$, and the thickness of the oxide layer is of the order of $0.1\ \mu\text{m}$.

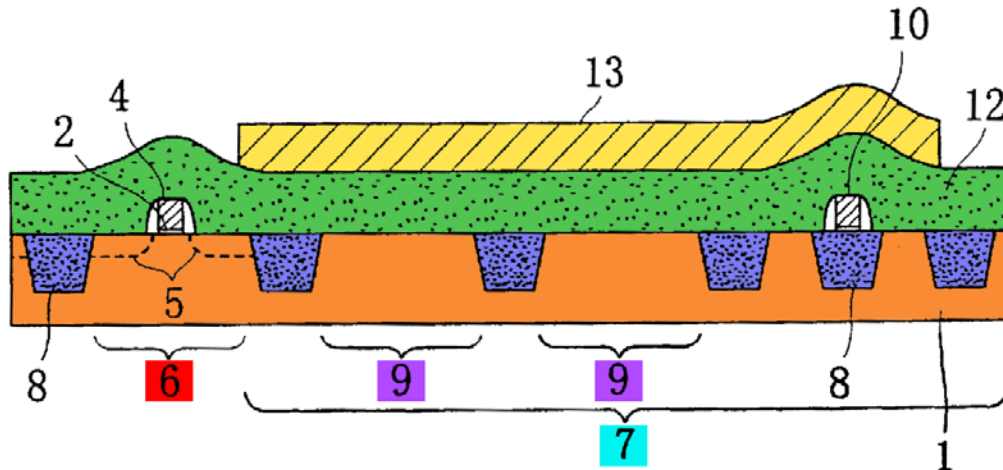
31. A voltage applied to the gate controls the current flow between the source and the drain in the area of the substrate labeled “channel region” in the

figure above. The vast majority of transistors in modern ICs are MOSFETs or derivatives thereof.

32. FIG. 19 (annotated) of the '736 Patent (which illustrates the prior art), below, shows a semiconductor device having a MOSFET. *See* '736 Patent at 1:35-37 ("FIG. 19 shows an example of the conventional trench-isolated semiconductor device"). The source and drain of the transistor are labeled as "5," the gate 4, and the oxide upon which the gate sits 2. The transistor is contained in an "active region," labeled "6," in contrast to the "isolation region," labeled "7." Active regions are portions of the semiconductor that contain transistors and are adjacent to and surrounded by isolation regions, which do not contain transistors and whose purpose is to electrically isolate the active regions. *See* John Uyemura, *Fundamentals of MOS Digital Integrated Circuits* (Addison-Wesley Publishing Company 1988) ("Uyemura"), at 42 (Ex. 1110).
33. The active region is bounded by trench portions 8, which are trenches etched into the substrate and filled with an insulating material. The trench portions in the isolation region separate several dummy semiconductor portions 9, which, as will be explained below, assisted with the planarization issue that previous generations of semiconductors suffered from.

34. Also illustrated in FIG. 19 of the '736 Patent is the interlayer insulating film 12, which is formed over both the active and isolation regions. The interlayer insulating film insulates the wire 10 formed above it from the transistors and substrate below it.

Fig. 19
PRIOR ART



35. Individual transistors are coupled together via electrically conductive pathways called “interconnects,” *e.g.*, wire 13 in FIG. 19 (annotated) above. There are many levels of interconnects, called “metal layers,” in a modern-day IC.

B. Isolating Transistors

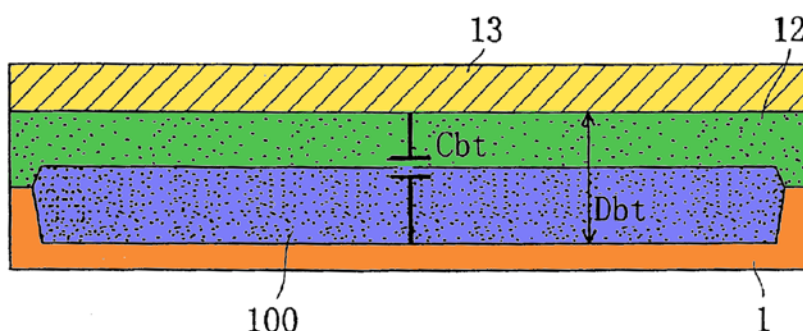
36. In 1965, Gordon Moore, the co-founder of Fairchild Semiconductor and Intel, authored a paper in which he described a phenomenon in which the

number of components in an IC doubled periodically and regularly. Moore, Gordon E. “Cramming More Components Onto Integrated Circuits.” *Electronics*, vol. 38, no. 8, Apr. 19, 1965 at 6 (Ex. 1119). Although this prediction has slowed in recent years, the concept that transistor density on ICs increases at a rapid pace still holds true and has become known as Moore’s Law. This trend has been the bedrock of increased processor and memory performance over the past decades, and has driven the need for all components of integrated circuits to diminish in size consistent with the need to improve overall performance and the laws of physics.

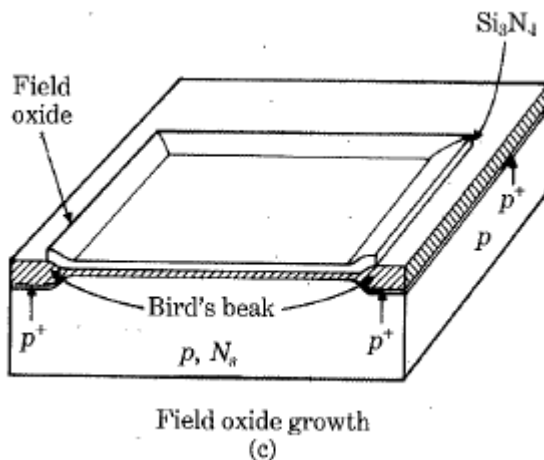
37. As transistor density increased, signal “leakage” between transistors became an important issue for IC designers to overcome. To prevent this effect, the industry began electrically isolating transistors from each other. One of the early methods of isolating transistors was called Local Oxidation of Silicon (LOCOS).
38. LOCOS was developed as early as 1970. Appels, J. A., et al. “Some Problems of MOS Technology.” *Philips Technical Review*, vol. 31, nos. 7/8/9, 1970 at 5 (Ex. 1120). An oxide film is thermally grown in specific regions of the substrate in order to electrically isolate transistors from each other. *See, e.g.*, Uyemura at 46.

39. The '736 patent illustrates a semiconductor with LOCOS isolation in FIG. 21(b) (annotated), below. The LOCOS film is labeled 100 and isolates transistors on either side of it (not shown). Wire 13 is also shown above interlayer insulating film 12.

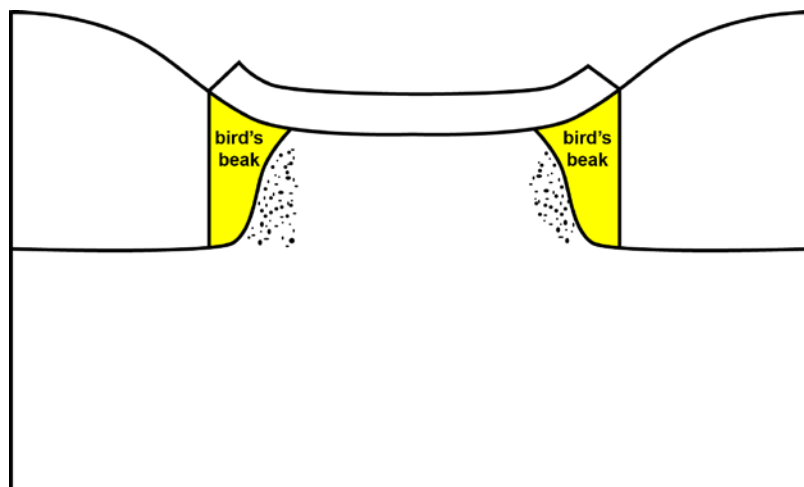
Fig. 21(b)
PRIOR ART



40. LOCOS had at least three drawbacks, however. First was the formation of what is known as the “bird’s beak.” This structural phenomenon can be seen by the sloped edges of LOCOS film 100 in APA FIG. 21(b) (annotated) above. It is also illustrated below.



Uyemura at 47



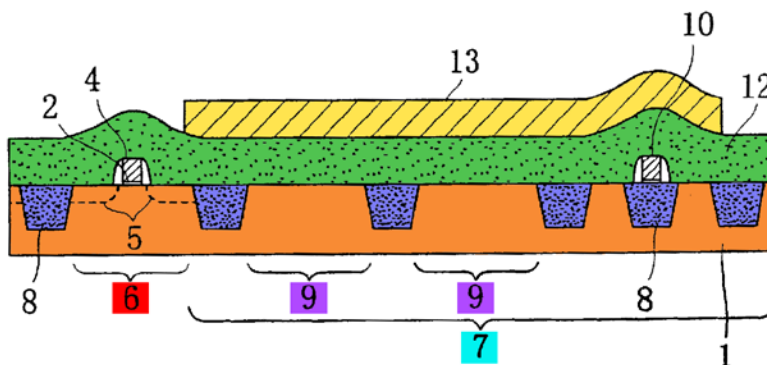
41. The “bird’s beak” is an unavoidable side effect of LOCOS growth and occurs when some of the oxidizing gas diffuses laterally under the nitride mask. *See* Uyemura at 46. The net effect is called “encroachment”—a reduced area for the formation of transistors than what was originally defined by the patterning mask. *Id.*; *see also* U.S. Patent No. 4,571,819 (“Rogers”) at 1:25-30 (discussing three drawbacks of LOCOS, one of which is “the formation of the so-called bird’s beak oxide configuration and the associated encroachment of the field oxide beneath the oxidation mask. Encroachment by the bird’s beak oxide limits the percentage of chip surface area which is available for device formation.”) (Ex. 1112).
42. A second problem with LOCOS was the lack of planarity that resulted during photolithographic operations in which layers of material are deposited on each other. *See* Rogers at 1:32-38 (“[T]he characteristic non-

planar surface topography makes it difficult to perform the increasingly high resolution photolithographic operations which are required to fabricate VLSI circuits.”); U.S. Patent No. 5,702,976 (“Schuegraf”) at 1:55-59 (“Another problem associated with the LOCOS process is the resulting circuit planarity or lack thereof. For submicron devices, planarity becomes an important issue, often posing problems with subsequent layer conformality and photolithography.”) (Ex 1113).

43. The third main drawback of using LOCOS (or any wide field oxide region) was the “pattern dependence” effect. During various parts of the manufacturing process, polishing must occur so that the surface of the partially fabricated IC is flat. Large areas of oxide make it difficult to planarize fully the surface of the IC while polishing. For example, over-polishing may result in a phenomenon known as “dishing,” in which thinning occurs in large oxide regions. The ’736 Patent describes the issue: “In the case where the trench occupies a large area in a CMP process for planarization . . . [this causes] pattern dependence, which causes polishing properties to vary depending on the area of a region to be planarized.” ’736 Patent at 1:24-34.
44. Shallow trench isolation (STI) structures were developed and eventually replaced LOCOS. Instead of having a large field oxide region, as in LOCOS

structures, STI usually incorporates shallow trenches filled with an insulating material. *See, e.g.*, Uyemura at 46-48, Schuegraf at 1:60-2:24. STI was known at least as early as the 1980s. *See* U.S. Patent No. 4,519,128 (“Chesebro”) at Abstract (Ex. 1111); Rogers at Abstract. The ’736 patent also acknowledges that semiconductors with STI isolation were known in the prior art, as shown in FIG. 19 (annotated) below. *See also* ’736 Patent at 1:35-37 (“FIG. 19 shows an example of the **conventional** trench isolated semiconductor device . . .”).

Fig. 19
PRIOR ART



45. Because LOCOS was simpler to implement, LOCOS was a common method of isolating transistors through the mid-1990s. At that time, however, the benefits realized by STI—namely, the ability to further increase transistor density, as discussed in the next paragraph—outweighed the increased complexity associated with STI. Thus, due to the benefits that STI offered,

the industry transitioned from using LOCOS to using STI to isolate transistors.

46. STI addressed problems associated with LOCOS that were discussed above. First, there is no “bird’s beak” associated with STI because trenches are etched with more precision than allowed by thermal growth of oxide, as done with LOCOS. This meant that more space was available for the inclusion of more transistors, and greatly enabled the increases of transistor density that Moore’s Law predicted. *See, e.g.,* Shuegraf at 2:22-24 (“Shallow trench isolation has the advantage[] of eliminating the bird’s beak of LOCOS”).
47. Second, the surface of a substrate with STI trenches was relatively more planar owing to the use of CMP polishing as part of the STI trench formation process.
48. Third, because there was usually no longer a single, wide area of oxide that needed to be polished, as in LOCOS, STI also “provid[ed] a high degree of surface planarity” due to the use of dummy patterns. Shuegraf at 2:22-24. The ’736 Patent also acknowledges the improved planarity of STI over LOCOS. ’736 Patent at 1:52-59; ’736 Patent File History at Amendment dated July 17, 2001 at 185(“[I]t is a known technique to form dummy

semiconductor portions in an isolation region in order to obtain an isolation region having a planarized surface.”).

49. LOCOS and STI were used for the same purpose—isolating transistors—and the semiconductor industry transitioned from using the former to using the latter. *See, e.g.*, Schuegraf at 2:20-22 (“Shallow Trench Isolation (STI) is used primarily for isolating devices of the same type and is often considered an alternative to LOCOS isolation”); U.S. Patent No. 4,957,590 (“Douglas”) at 4:10-16 (“Field oxide 12, preferably silicon dioxide (SiO₂), is grown or deposited in selected portions of the surface of the substrate 10 for isolation of active regions from one another according to the well known local oxidation (LOCOS) isolation technique; of course, other isolation techniques such as trench isolation may alternatively be used.”) (Ex. 1114); U.S. Patent No. 5,976,939 (“Thompson”) at 3:8-10 (“[I]solation technologies such as local oxidation of silicon (LOCOS) may be used instead of trenches.”) (Ex. 114); U.S. Patent No. 6,165,826 (“Chau”) at 5:56-67 (“Although STI isolation regions are preferred because of their ability to be formed to small dimensions with a high degree of planarity, other methods can be used such as, but not limited to, LOCOS”) (Ex. 1116); U.S. Patent No. 5,733,812 (“Ueda”) at 22:49-52 (“Although the isolation is composed of the LOCOS film in the above embodiments, the present invention is not limited thereto.

The present invention is also applicable to an isolation of trench structure or the like.”) (Ex. 1117).

C. Capacitance

50. Capacitance describes the ability of a structure to store electric charge. The most basic type of capacitor comprises two parallel metal plates separated by a fixed distance that is typically filled with an insulating material. If a voltage is applied across the plates, charge accumulates on the plates—positive charge on one plate, and negative charge on the other. All basic undergraduate physics and electrical engineering courses teach this concept. The specific formula for capacitance given the above scenario is:

$$C = \frac{Q}{V} = \epsilon_r \epsilon_0 \frac{A}{d}$$

where:

C is the capacitance,

Q is the charge held,

V is the voltage applied across the plates,

ϵ_r is the relative permittivity, or dielectric constant, which varies between materials,

ϵ_0 is the permittivity of free space ($\approx 8.854 * 10^{-12}$ F/m), and

d is the distance between the plates.

See also Dorf and Tallarida, *Pocket Book of Electrical Engineering Formulas* (CRC Press 1993) (“Dorf”) at 8 (Ex. 1109).

51. As can be seen from the equation above, capacitance can increase or decrease based on a variety of factors. If, for instance, the distance between the plates increases, or the size of the plates decreases, all else being equal, the capacitance of the plates will decrease. Conversely, if the distance between the plates decreases, or the size of the plates increases, all else being equal, the capacitance of the plates will increase.
52. The dielectric constant is a value that is reflective of the properties of the material between the plates. Thus, for example, the dielectric constant of air is very close to 1, while that for silicon dioxide is about 3.9. This means that, all else being equal, two metal plates separated by air will have a lower capacitance than those separated by silicon dioxide.
53. The '736 patent explains that STI, while addressing problems associated with LOCOS, also had its own drawback: it increased the capacitance between the wire and substrate (labeled 1 and 13, respectively, in FIG. 19 of the '736 Patent, above), which had the undesirable effect—called “RC delay”—of reducing the speed at which the semiconductor could operate.
54. RC delay becomes more acute as transistor dimensions decrease. Saraswat, Krishna C. et al. “Effect of Scaling of Interconnections on the Time Delay of

VLSI Circuits.” *IEEE Journal of Solid-State Circuits*, vol. SC-17, no. 2, April 1982 (“Saraswat”) at 4 (“[a]s the minimum feature size is made smaller, the area of cross section of the interconnection also reduces. At the same time, a higher integration level allows the chip area to increase, causing the length of the interconnections to increase. The net effect of this ‘scaling of interconnections’ is reflected into an appreciable RC time delay. For a very large chip with extremely small geometries, the time delay associated with interconnections could become an appreciable portion of the total time delay, and hence the circuit performance could no longer be decided by the device performance.”) (Ex. 1106).

55. This “wiring-to-substrate” capacitance issue was well-known in the industry long before the priority date of the ’736 patent. *See* U.S. Patent No. 5,107,302 (“Iranmanesh”) at 1:37-39 (“It is well known that device performance is impacted by the capacitance between the interconnect and the underlying substrate.”) (Ex. 1108); Oshima at 1:14-23 (“With the steady advance of the integration rate of semiconductor integrated circuits, the integrated circuits have become more and more microminiaturized As a result, the proportion of the wiring capacitance to the capacitance load of the respective circuit signals has increased.”); U.S. Patent No. 4,960,725 (“Noguchi”) at 1:41-54 (“[I]t is considered that there are three different

types of capacitance elements When the size of a transistor becomes smaller . . . the above mentioned capacitances (i) and (ii) are reduced. However, the capacitance (iii) [a capacitance between the substrate 1 and the conductive layer 10] tends to increase”) (Ex. 1121).

56. In its discussion of the prior art, the '736 Patent models the wiring-to-substrate capacitance in both LOCOS and STI devices, as shown below in FIGS. 21(a) and (b) (annotated), as the capacitance between two parallel plates separated by a dielectric. *See* '736 patent at 3:7-12 (“In the case where a member interposed between the wiring and substrate is composed of a homogeneous material, the wiring-to-substrate capacitance per unit area is inversely proportional to the distance between the wiring and substrate, so that the capacitance is larger as the distance is shorter.”), 3:7-12.

Fig. 21(a)
PRIOR ART

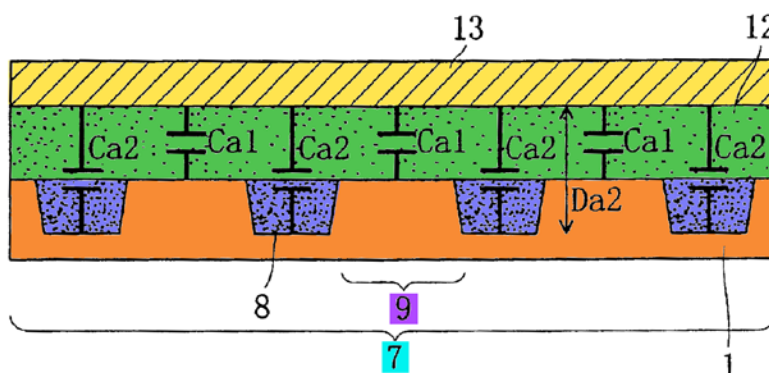
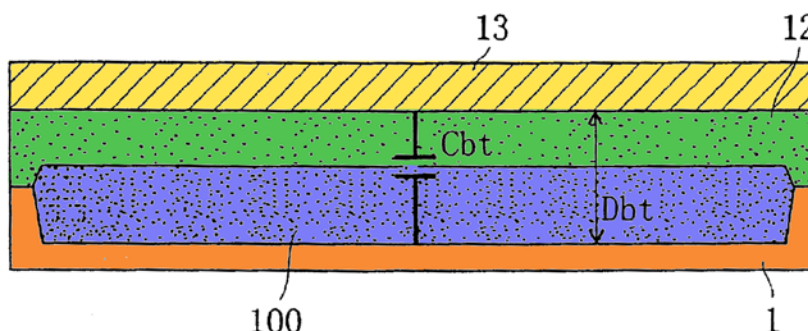


Fig. 21 (b)
PRIOR ART



57. The industry has been modeling the wiring-to-substrate capacitance in this way for quite some time. For example, Saraswat models the wiring-to-substrate capacitance of the semiconductor in its Fig. 1 (annotated), below, in this way using the same equation that I described above:

$$C_{ox} = K_{ox} \epsilon_0 \frac{WL}{X_{ox}} .^1 \text{ Saraswat at 5 (annotated figure); see also Noguchi at 3:37-4:10.}$$

¹ Saraswat uses different variable names than I do, but they represent equivalent concepts. Saraswat's K_{ox} is equivalent to my ϵ_r (dielectric constant), and he more specifically represents the area (A in my equation) as the product of the width W and length L of the interconnect. He also represents the distance (d in my equation) as X_{ox} . Saraswat at 5.

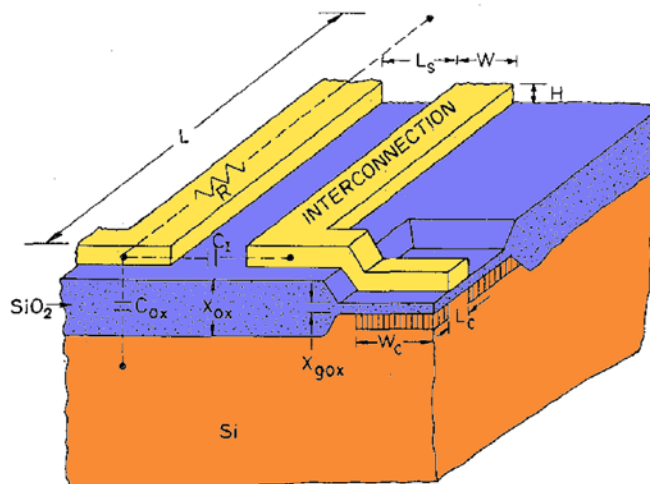
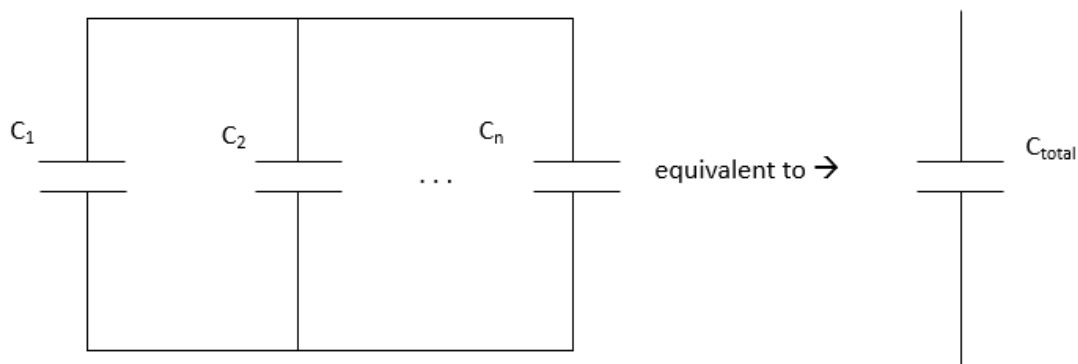


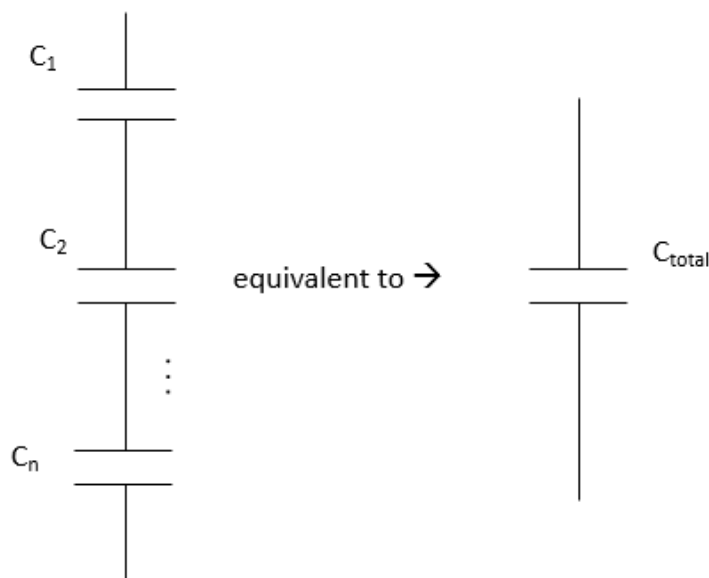
Fig. 1. Cross section of MOS transistors and parasitics associated with the interconnections.

58. Thus, in devices with LOCOS isolation, the wiring-to-substrate capacitance is simply given by C_{bt} in FIG. 21(b) (annotated), above. But for devices with STI, the capacitance must be modeled as several parallel-plate capacitors connected in parallel. The concept of capacitors in “series” or in “parallel” is taught in introductory electrical engineering courses. For capacitors connected in parallel:



$$C_{total} = C_1 + C_2 + \dots C_n$$

For capacitors connected in series:



$$C_{total} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \dots + \frac{1}{C_n}}$$

See also Dorf at 9.

59. Thus, the same set of capacitors arranged in parallel have a greater capacitance than if they are arranged in series. Additionally, the capacitors in parallel have a total capacitance that is greater than any single capacitor, and the capacitors in series have a total capacitance that is smaller than any single capacitor.
60. The '736 Patent represents the total capacitance "Cat" of the prior art STI structure shown in FIG. 21(a) as:

$$Cat = \Sigma Ca1 + \Sigma Ca2$$

'736 Patent at 3:1-6. Because Ca1 and Ca2 are connected in parallel, these two values are added linearly to obtain the total capacitance.

61. If the distance Da2 in FIG. 21(a) is equal to the distance Dbt in FIG 21(b) (which shows the prior art LOCOS-isolated structure), we can assume that Ca2 is equal to Cbt (and all else being equal). But the *overall* wiring-to-substrate capacitance Cat in FIG. 21(a) will be greater than the *overall* wiring-to-substrate capacitance in FIG. 21(b). This is because the Ca1 values are greater than the Ca2 values,² so the parallel sum of those values (*see supra*) will be greater than either of those values individually. Thus, $Cat > Cbt$: STI may suffer from larger wiring-to-substrate capacitances than LOCOS-isolated devices. *See* '736 Patent at 3:1-23.

D. Summary of the '736 Patent

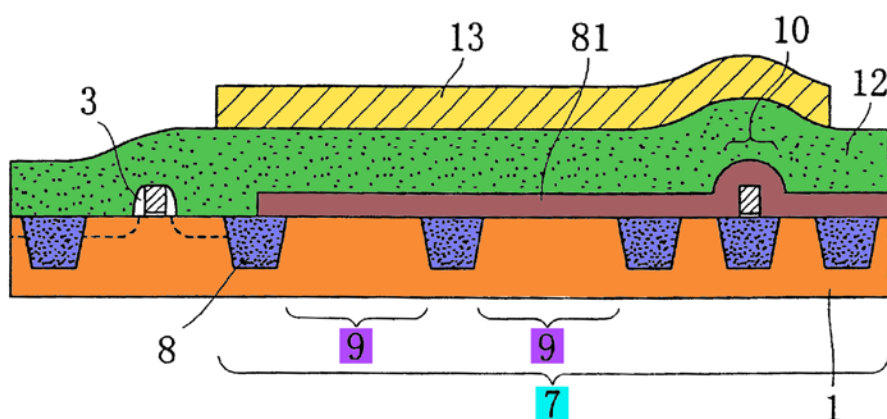
62. The '736 Patent purports to solve the increased wiring-to-substrate capacitance that results from the transition from LOCOS to STI. Relevant to the Challenged Claims, it does so by introducing either a “dielectric film”

² This is true because distance and capacitance are inversely proportional, as described above. The distance between the wire 13 and the substrate 1 is smaller than the distance between the wire 13 and the bottom of trench 8, meaning that the capacitance of the former is larger than the capacitance of the latter.

(claim 6) or a “resistor film” (claim 13) between the interlayer insulating film and the substrate. *See* '736 Patent at FIGS. 5, 7 (embodiments of claim 13), 12 (embodiment of claim 6), 15:67-16:18 (discussing FIG. 5), 18:28-51 (discussing FIG. 7), 23:22-27 (discussing FIG. 12).

63. With respect to the dielectric film (claim 6), the '736 Patent states that its insertion increases the distance between the wire (the first plate) and the substrate (the second plate), leading to a reduction in capacitance. '736 Patent at 24:34-43; *see supra* § V.C. The patent also states that the dielectric film introduces a second capacitance, which, when added in series with the capacitance of the interlayer insulating film, reduces the overall capacitance. '736 Patent at 4:28-35; *see supra* § V.C. '736 Patent FIG. 12 (annotated), showing the resistor film labeled as 81, is shown below.

Fig. 12



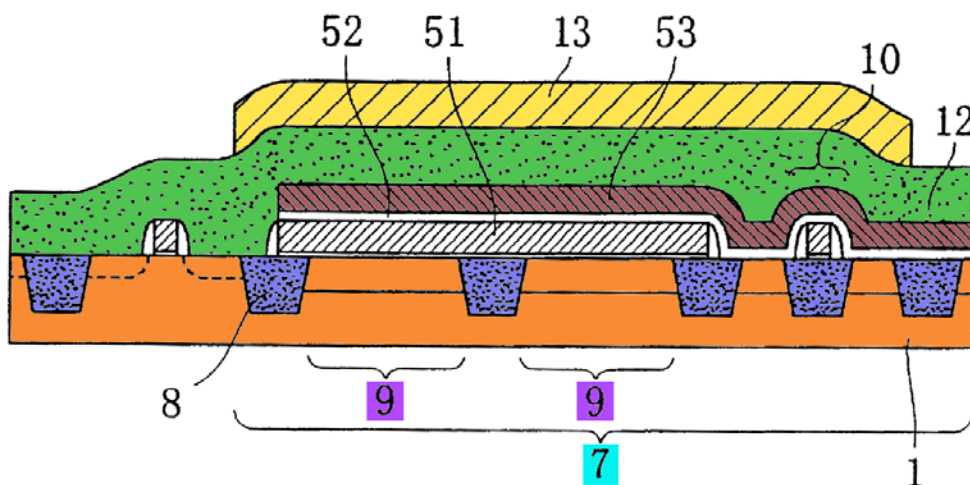
64. With respect to the resistor film (claim 13), the '736 Patent provides a silicon oxide film 52 and a high resistor film 53 formed over dummy gate

51, polysilicon wire 10, and substrate 1. The '736 Patent describes the high resistor film 53 as being a polysilicon film and having “a sheet resistance film higher than that of the first-layer polysilicon film composing the gate electrode 4” '736 patent at 16:6-15. The '736 patent goes on to state that

it is sufficient to consider the capacitance between the wiring and high resistor film instead of the capacitance between the wiring and substrate. In this case, since the resistance of the polysilicon film composing the high resistor film 53 is high, a voltage drop occurs between the top face of the high resistor film 53 and the surface of the semiconductor substrate 1. Accordingly, the voltage applied to the top and bottom faces of the interlayer insulating film is reduced, though the capacitance of the interlayer insulating film 12 remains unchanged. Since the amount of charge accumulated in the top and bottom faces of the interlayer insulating film 12 decreases in direct proportion to the voltage applied thereto, the time required for charging or discharging between the wiring and high resistor is reduced

'736 Patent at 16:20-33. Figure 5 (annotated), which reflects this embodiment of claim 6, is shown below. The high resistor film is labeled as 53.

Fig. 5



65. Because the wire 13 and the resistor film 53, separated by interlayer insulating film 12, acts as a capacitor in series with a second capacitor comprising resistor film 53 and the substrate 1, overall capacitance between the wire and the substrate decreases. Once two capacitors are placed in series, the charge and voltage across each of them decreases in proportion to each of their capacitances (a material property that does not change). Thus, the charge collected on the top and bottom faces of the interlayer insulating

film decreases as dictated by the equation $C = Q/V$ (*see supra* § V.C), where C is constant (since it is a material property of the interlayer insulating film).

66. In other words, the '736 Patent takes advantage of two long-known, basic phenomena: (1) that increasing the distance between the plates of a capacitor decreases the capacitance, and (2) that capacitors in series reduce overall capacitance.

67. Claims 6 and 13 recite exemplary systems, reproduced below:

6, 13. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

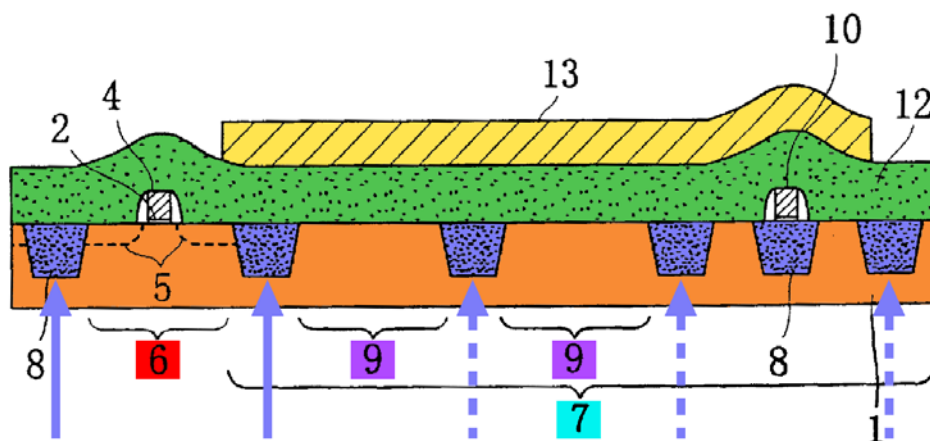
a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and

[6 only] a dielectric film interposed between at least said dummy semiconductor portions of said isolation region and said interlayer insulating film.

[13 only] a resistor film formed under said wire, and between said interlayer insulating film and at least said dummy semiconductor portions of said isolation region.

68. Importantly, the '736 Patent acknowledges that the first five elements are all found in the prior art. *See, e.g.,* '736 Patent FIG. 19 (annotated) below (showing substrate 1, active region 6, isolation region 7, first trench portion 8 (indicated with solid blue arrows), second trench portion 8 (indicated with dotted blue arrows), dummy semiconductor portions 9, interlayer insulating film 12, and wire 13), 1:35-59 (describing FIG. 19).

Fig. 19
PRIOR ART



69. Thus, the inventive aspects of claim 6 and 13 are the addition of the dielectric film or resistor film, respectively, shown below in dark red, which creates an additional capacitance in series between the wire and the substrate, increases the distance between the wire and the substrate, and/or reduces the charge buildup on either side of the interlayer insulating film, leading to reducing the negative effects associated with increased wiring-to-substrate capacitance. '736 Patent at 3:32-48, 4:16-35, 5:7-26, 15:53-16:35, 18:14-19:17, 23:2-27.

semiconductor devices: the '736 Patent merely applied a well-known solution to a well-known problem.

E. Summary of the Prosecution History

71. The '736 patent was filed on December 22, 1999 as a “division of application No. 08/987,137, filed on Nov. 25, 1997, now Pat. No. 6,130,139,” '736 patent at Title Page, (62), and claims priority to JP 08-314762, filed on November 26, 1996 and JP 09-023844, filed on February 6, 1997. *See id.*
72. On February 26, 2001, the claims were rejected as being anticipated over prior art references that are not relied upon in my declaration. *See* '736 Patent File History at Non-Final Rejection dated Feb. 26, 2001 at 161-167. On July 17, 2001, Applicants amended the claims and argued that the prior art references do not teach the claims. *Id.* at Amendment dated July 17, 2001, at 178-197.
73. In the process, the applicant confirmed that the structures described in the admitted prior art and the wiring-to-substrate capacitances that arise from such structures were well-known in the art. *See* '736 Patent File History at Remarks dated July 17, 2001, at 185 (“More specifically, it is a known technique to form dummy semiconductor portions in an isolation region in order to obtain an isolation region having a planarized surface. Indeed,

without such dummy semiconductor portions, it would be difficult to obtain a planarized surface of the isolation region. However, prior to the present invention there has been the problem that the formation of the dummy semiconductor portions increases the wiring-to-substrate capacitance in the isolation region, as is described in the “BACKGROUND OF THE INVENTION” portion of the specification and Figs. 21(a) – 21(c).”).

74. In the applicant’s successful attempt to traverse the prior art over which the claims were initially rejected, the applicant made the following narrowing amendments to independent claim 1, as shown below, where underlines represent additions and strikethroughs represent deletions from the originally proposed claim:

1. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region
surrounding said active region;

a ~~plurality of~~ first trench portions ~~each formed in said isolation region and~~
filled with an insulating material formed to separate said active region
from said isolation region;

a second trench portion filled with an insulating material formed to separate
a plurality of dummy semiconductor portions ~~interposed between said~~
~~individual trench portions~~ in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and

[claim 6 only] a dielectric film interposed between at least said semiconductor portions of said isolation region and said interlayer insulating film.

[claim 13 only] a resistor film formed under said wire, and between said interlayer insulating film and at least said semiconductor portions of said isolation region.

VI. Level of Ordinary Skill in the Pertinent Art

75. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.
76. It is my opinion that a POSITA at the time of invention of the '736 Patent is a person with a bachelor's degree in electrical engineering, materials science or engineering, or chemical engineering (or equivalent experience), and

would have two or three years of experience with integrated circuit manufacturing, fabrication, and structures. This was the typical level of experience of persons working with processes for manufacturing semiconductor device structures at the time of the alleged invention.

VII. Claim Construction

77. It is my understanding that the '736 Patent expired on November 25, 2017.

It is further my understanding that, for an expired patent, the claims should be given a district court-type of claim construction. It is my understanding that this standard entails construing claims as one of ordinary skill in the art in the relevant field of the invention would.

VIII. Detailed Invalidity Analysis

78. I have been asked to provide an opinion as to whether the Challenged Claims of the '736 Patent are invalid in view of the prior art. The discussion below provides a detailed invalidity analysis of how the prior art references identified in Section I disclose, either alone or in combination, each element of the Challenged Claims and thereby invalidate the claims.

79. As part of my invalidity analysis, I rely upon the priority date of the '736 Patent as the time of the alleged invention. I have also considered the level of ordinary skill in the pertinent art.

80. As part of my obviousness analysis, I have considered the scope and content of the prior art, and whether any differences between the claimed invention and the prior art are such that the subject matter, as a whole, would have been obvious to a person having ordinary skill in the art as of the priority date for the '736 Patent.

81. I describe in detail below the scope and content of the prior art, as well as any differences between the alleged invention and the prior art, on an element-by-element basis for the Challenged Claims.

A. Background on Prior Art References

82. Before providing a detailed analysis of how the prior art invalidates the Challenged Claims, I provide a brief summary of the asserted prior art. As explained below, Oshima discloses an oxide film and a polysilicon layer that reduces wiring-to-substrate capacitance, as required by the Challenged Claims.

1. Background on the APA

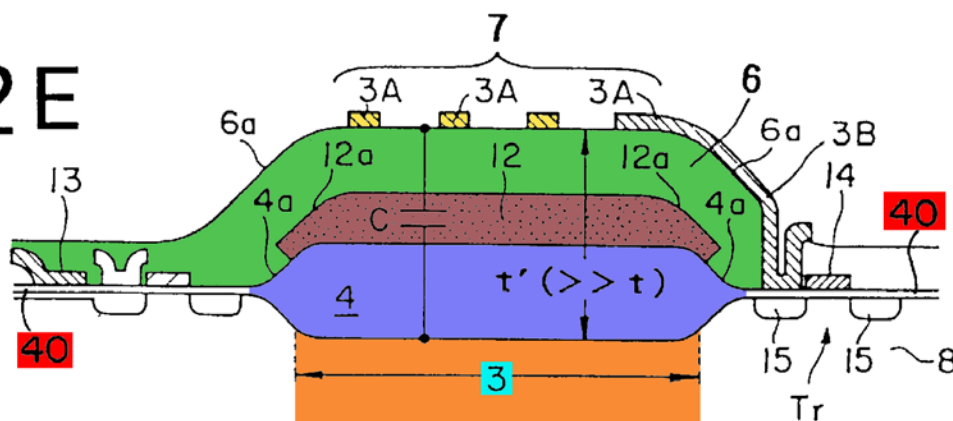
83. As discussed above, the APA discloses all elements of claim 1 except for the last. The APA also admits that the problem of increased wiring-to-substrate capacitance in STI-isolated devices was well-known ('736 Patent at 3:1-30), meaning that there was already a motivation for a POSITA to find solutions

for the problem. *See, e.g.*, Noguchi at 1:12-16, '736 Patent File History at Remarks, 185.

2. Background on Oshima

84. Oshima is titled “Semiconductor Integrated Circuit Having Reduced Wiring Capacitance.” Oshima at cover. Oshima was filed in the U.S. on May 31, 1996. *Id.* Oshima issued as U.S. Patent No. 5,814,848 on September 29, 1998 to Kabushiki Kaisha Toshiba and names Shigeo Oshima as the inventor. *Id.*
85. Oshima describes a semiconductor in which “the wiring capacitance of the bus line region is reduced, so that the operation speed can be increased, the power consumption can be decreased, and the chip size can be reduced.” *Id.* at Abstract. Like that of the ’736 Patent, the purpose of the invention of Oshima is to reduce the capacitance between the wire and the substrate. *E.g., id.* at 1:5-10, 1:14-2:34.
86. Oshima Figures 2E and 3 (annotated) illustrate exemplary systems:

FIG. 2E



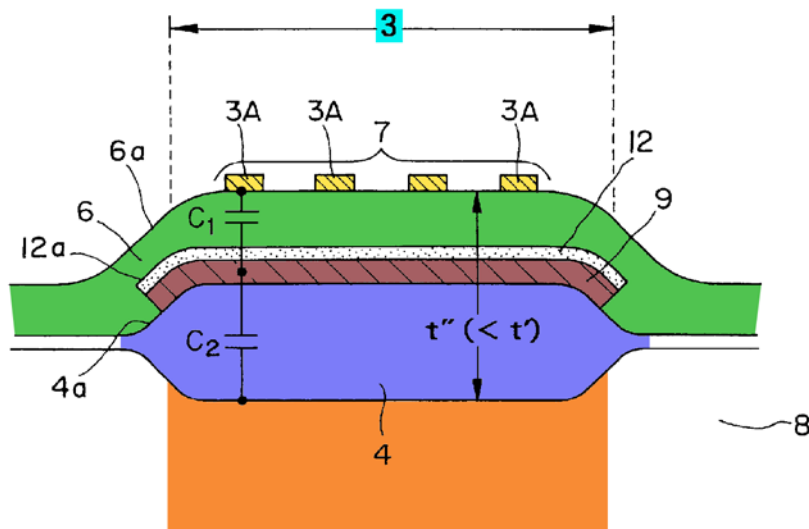


FIG. 3

87. In Figure 2E, a “bus line region 3” is shown with wires 3A on top of interlayer insulating film 6. Oshima at 4:52-56, 5:32-35, 5:45-58. This area can also be called an isolation region since it is not an active area and it serves to separate transistors in active areas. *See id.* at 2:5-12, 4:57-62, 5:33-44. Oshima teaches a reduction in wiring-to-substrate capacitance in this region by oxidizing a poly silicon layer 9 (not shown in FIG. 2E) into oxide film 12. *Id.* at 5:13-20, 5:37-44. “In order to reduce the wiring capacitance, the thicker the oxide film 12 is, the better will be the result.” *Id.* at 5:17-18.
88. A second embodiment is shown in Figure 3. In this embodiment, Oshima teaches a polysilicon layer 9 under the bus line region 3. Oshima at 6:37-42. Oshima explains that this disclosure also reduces wiring-to-substrate capacitance: “the capacitance C between the bus line region wiring layer 7

and the semiconductor substrate 7 [sic] can be reduced as $1/C = (1/C1) + (1/C2)$ where C1 denotes the capacitance between the poly silicon layer 9 and the bus line region wiring layer 7, and C2 denotes the capacitance between the poly silicon layer 9 and the semiconductor substrate 8.” Oshima at 6:43-54. Oshima therefore teaches that the poly silicon layer 9 adds a capacitance in series, which as I discussed above, reduces overall capacitance. *See supra* § V.C.

B. The Challenged Claims Are Invalid Over the APA and Oshima

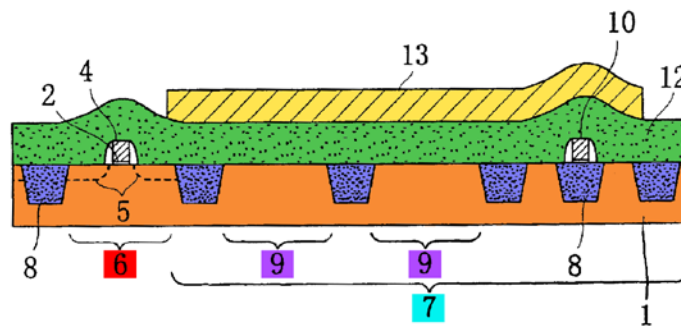
89. It is my opinion that Oshima and the APA render obvious the Challenged Claims. The APA discloses every element of the claims except for a “resistor film” or “dielectric film.” But Oshima discloses these element in its two separate embodiments, and it would have been obvious for a POSITA to combine Oshima with the APA in this way. Alternatively, Oshima discloses each and every element of the Challenged Claims, except that it discloses LOCOS isolation instead of STI. But, as acknowledged by the APA, STI was well-known to be more advantageous than LOCOS for isolating transistors, and so it would have been obvious to a POSITA to substitute STI for LOCOS.

1. **Claims 6 and 13**

(1) **Element 6[a]/13[a]: “A semiconductor device, comprising”**

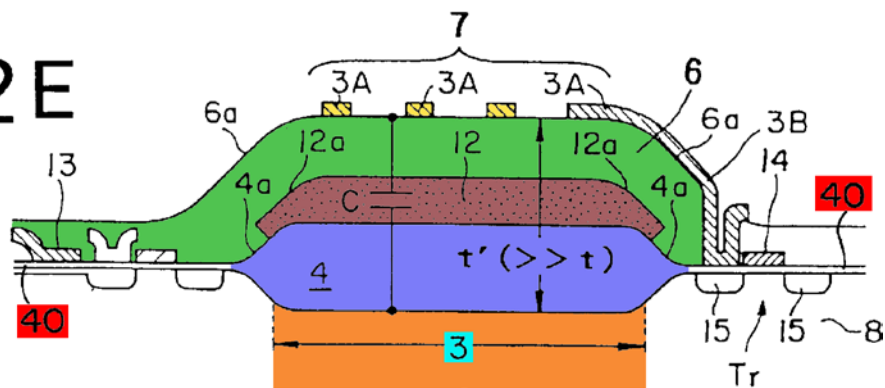
90. The APA admits that this element was well-known ('736 Patent at 1:35-37), and illustrates one such prior art semiconductor device in FIG. 19 (annotated), below.

Fig. 19
PRIOR ART



91. Oshima also discloses this element since it discloses a “semiconductor integrated circuit having reduced wiring capacitance.” Oshima at Title; *see also id.* at Abstract, 1:6-10, 2:38-43, 2:66-3:20, 4:63-5:3, 7:46-59. An exemplary semiconductor device is shown in FIG. 2E (annotated), below.

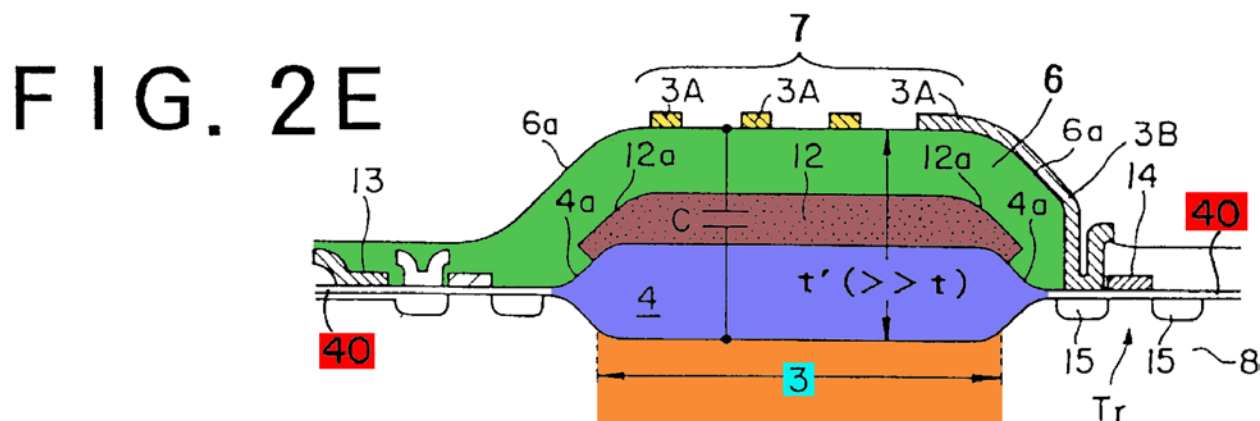
FIG. 2E



(2) **Element 6[b]/13[b]: “a semiconductor substrate having an active region and an isolation region surrounding said active region”**

92. The '736 patent admits that this limitation was well-known in the prior art. APA FIG. 19 shows “an active region 6 of a P-type silicon substrate 1” '736 patent at 1:38-41. APA also teaches that an “isolation region 7 surrounding the active region 6 is formed” ('736 patent at 1:41-43) and that “[t]he semiconductor portions 9 [in the isolation region] may be considered as dummy active regions which do not function as active regions.” '736 patent at 2:10-12.

93. Oshima discloses a semiconductor substrate, which can be seen below in FIG. 2E (annotated), labeled with numeral 8. *See* Oshima at 5:23-30, 6:61-64 (describing substrate 8).



94. Oshima also discloses an active region, which it calls a “circuit block region 2,” also “indicated by reference numeral 40,” on the left and right sides of FIG. 2E; specifically, it can be seen that transistors are formed in the active region by gate electrodes 14 and source/drain regions 15, for example, as indicated by the “Tr” label in FIG. 2E. Oshima at 4:63-5:3, 4:57-62.
95. Oshima discloses an isolation region in the center of FIG. 3 (*i.e.*, separating the adjacent active regions). The '736 Patent describes the isolation region as a region that electrically isolates individual transistors found within active regions. *See* '736 Patent at 11:34-43 (“As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the

individual trench portions 8 and not serving as active regions.”). Like the APA, the region in the center of Oshima’s FIG. 2E is also used to isolate the transistors in the active regions; Oshima calls this isolation region the “bus line region 3.” *See* Oshima at 4:57-62 (“an element separating field oxide film 4 is formed all over the surface of the semiconductor substrate 8 in such a way as to become selectively thick at only the region where the bus line regions 3 are to be formed”); *see also id.* at 1:16-20, 4:57-62, 5:33-44, 6:34-64; *cf.* ’736 Patent at 1:38-44 (an “isolation region 7 surrounding the active region 6 is formed”).

96. Such regions were well-known in the prior art. *E.g.*, Uyemura at 42 (isolation regions are used to electrically isolate “neighboring devices”); Ueda at 2:46-50; Douglas at 4:10-16; Schugraf at 1:37-45; Noguchi at Abstract.

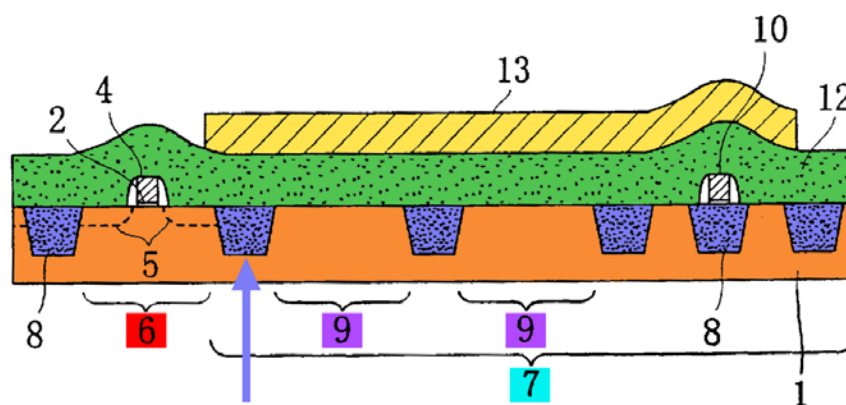
(3) Element 6[c]/13[c]: “a first trench portion filled with an insulating material formed to separate said active region from said isolation region”

“a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region”

97. The APA admits elements 6[c]/13[c] and 6[d]/13[d] were known in the art. It states that an “isolation region 7 surrounding the active region 6 is formed with a plurality of trench portions 8 each filled with a silicon oxide film.”

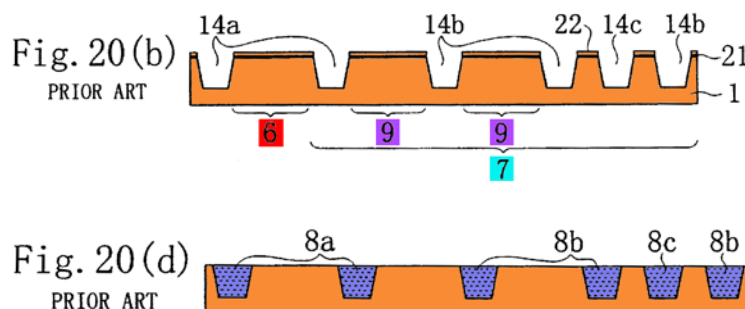
'736 patent at 1:41-44. Silicon oxide is an insulating material. The second-to-left trench portion 8, highlighted with a blue arrow below in APA FIG. 19 (annotated), separates the active region 6 and the isolation region 7.

Fig. 19
PRIOR ART

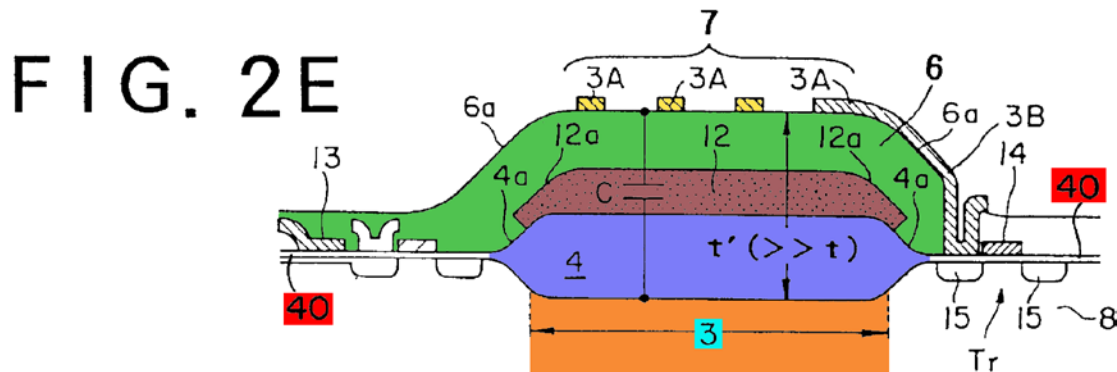


98. The APA provides further detail on the trench portions and the dummy semiconductor portions: “Between the individual trench portions 8, there are provided semiconductor portions 9 having top surfaces at the same level as the top surfaces of the trench portions.” ’736 Patent at 1:44-47; *see also id.* at 2:7-25 (“[i]n the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14 [which correspond to trench portions 8, as shown below in FIGS. 20(b) and 20(d) (annotated)]. The semiconductor portions 9 may be

considered as dummy active regions which do not function as active regions.”).

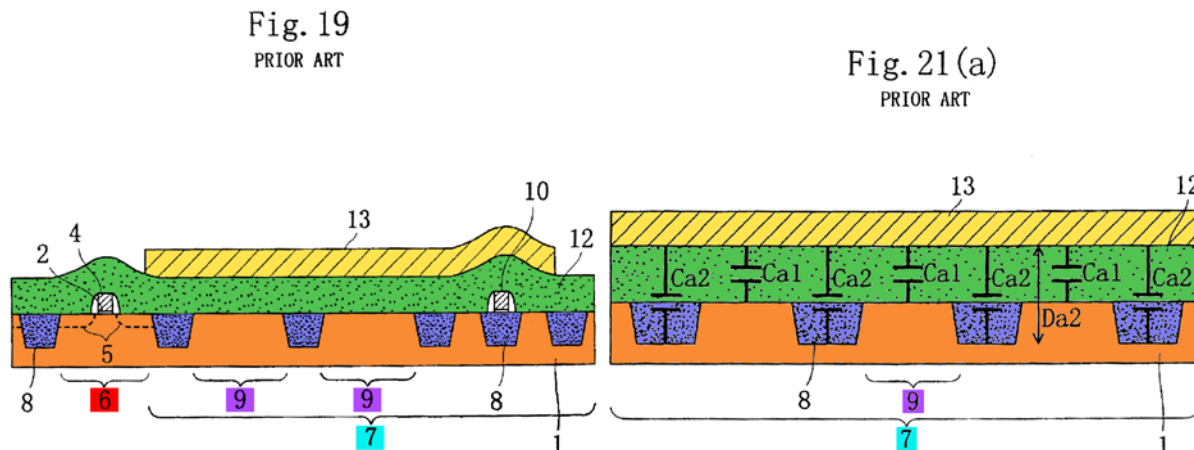


99. Oshima also discloses this element. It discloses a field oxide film 4 that is selectively thicker only at the bus line regions 3. Oshima at 4:57-62. The field oxide film 4, which can be seen below in Oshima FIG. 2E (annotated), separates the circuit block regions (indicated by numeral 40). *Id.*



100. It would have been obvious to a POSITA at the time of the '736 Patent to form dummy semiconductor regions by replacing Iranmanesh's field oxide film 4 with STI trenches for the reasons discussed above in Section V.B (discussing drawbacks of LOCOS, including the "bird's beak," planarity, and pattern dependence issues, how STI addressed all three, and discussing

how both are directed to solving the same problem). Indeed, the APA itself acknowledges that as transistor dimensions shrink, it is more desirable to replace LOCOS devices with STI devices ('736 Patent at 1:10-34) and it illustrates such a device as APA in FIGS. 19 and 21(a) (annotated) below.



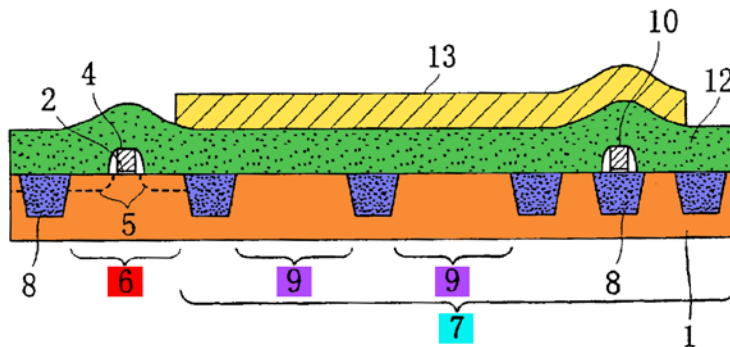
101. Moreover, both the '736 Patent and Oshima are directed towards mitigating the problems that arise from device miniaturization in the context of wiring-to-substrate capacitance. For instance, Oshima notes that “the integrated circuits have become more and more microminiaturized . . . so that space required for a wiring region (a bus line region) for connecting the circuit blocks to one another has increased. As a result, the proportion of the wiring capacitance to the capacitance load of the respective circuit signals has increased,” and that prior art solutions such as increasing the thickness of insulating films were not well suited, especially if an increase of transistor size was to be avoided. Oshima at 1:14-2:34; '736 Patent at 1:6-9; *see also*

Oshima at Abstract (“In a semiconductor integrated circuit, the wiring capacitance of the bus line region is reduced, so that the . . . chip size can be reduced.”).

(4) Element 6[d]/13[d] “an interlayer insulating film formed to extent continuously over said active region and said isolation region”

102. The APA admits that this element was well-known, and shows an interlayer insulating film 12 that extends continuously over the active region 6 and isolation region 7 of the device shown in FIG. 19 (annotated), below. ’736 Patent at FIG. 19, 1:49-51.

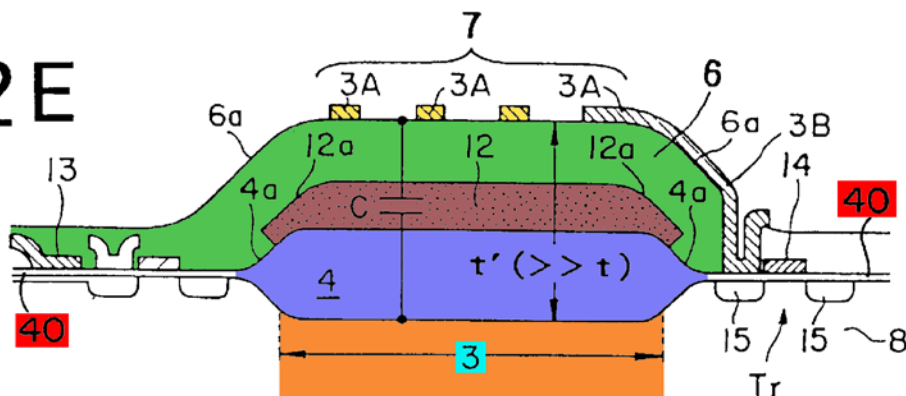
Fig. 19
PRIOR ART



103. Oshima also discloses this element. It discloses “an interlayer insulating film 6 [that] is formed over the entire surface of integrated circuit 1.” Oshima at FIG. 2E (annotated), 5:31-32; *see also id.* at 4:57-5:3, 6:34-64. The interlayer insulating film in Oshima is deposited after the circuit block

regions (numeral 40) and field oxide film 4 and oxide film 12 in bus line region 3 are formed. *Id.*

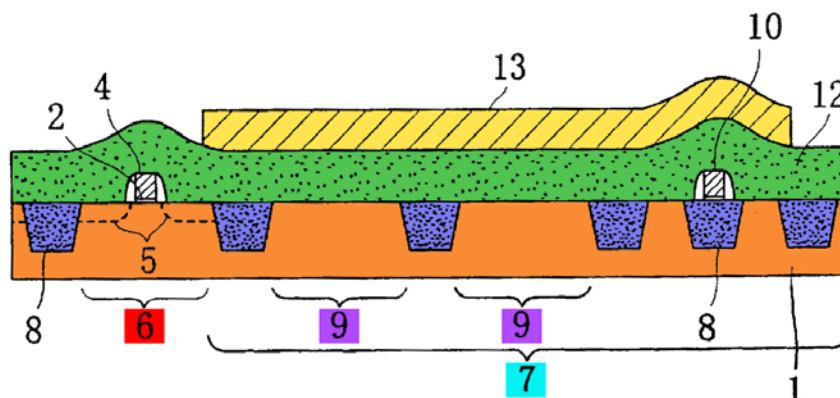
FIG. 2E



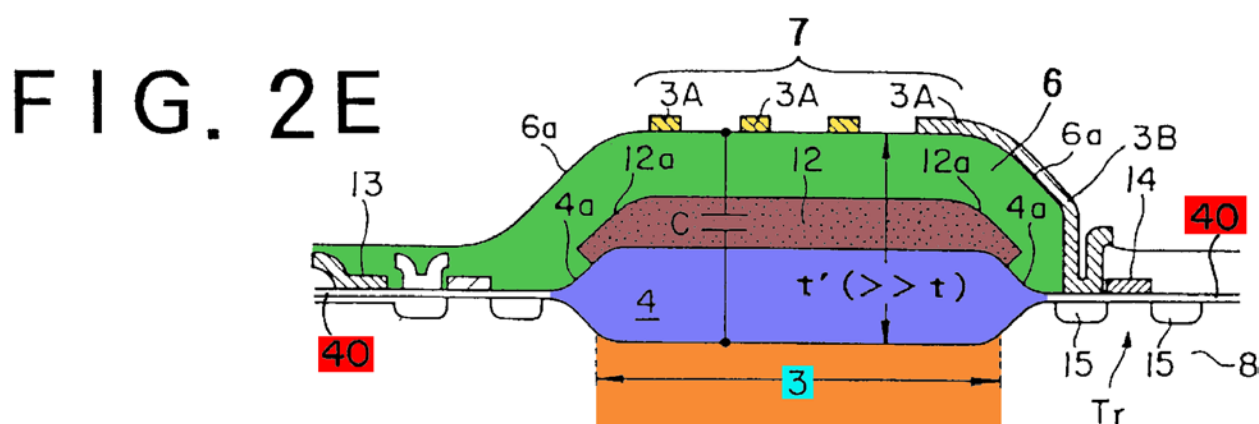
- (5) **Element 6[e]/13[e] “a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region”**

104. The APA discloses this element since it shows wire 13 formed on interlayer insulating film 12, and which covers the dummy semiconductor portions 9 and isolation region 7 of the device shown in FIG. 19 (annotated), below.

Fig. 19
PRIOR ART



105. Oshima also discloses this element because it discloses that “a bus line region wiring layer 7 is formed on the interlayer insulating film layer 6 at the area corresponding to the bus line region 3.” Oshima at 5:33-35; *see also* FIG. 2E. Oshima gives further disclosure about the wires: “there are arranged bus lines 3A and wires 3B for connecting the bus line 3A to circuits formed in the circuit block region 2.” *Id.* at 4:50-56.



106. While Oshima FIG. 2E (annotated) above shows wires running into and out of the page (rather than covering the dummy semiconductor portions and second trench portions in the isolation region—which would have been obvious to implement into Oshima as discussed *supra* in Sections V.B, VIII.B.1(3)), it would have been obvious to a POSITA that the wires in Oshima FIG. 2E could have just as easily been rotated 90 degrees so that they run across the page, as shown in the APA in the '736 Patent. *See* '736 Patent at FIG. 19. Such an orientation is simply a design choice that is made by the layout engineer depending on which components of the device need

to be interconnected. For example, Oshima FIG. 1 shows a different orientations for wires 3A, which run into the page, and wires 3B, which run across the page. Thus, such different orientations would be found in different regions of the semiconductor device and would lead to expected behavior of delivering the desired signal or power in a manner that was desired by a layout engineer. It would have been merely a substitution of one known element for another that obtained predictable results.

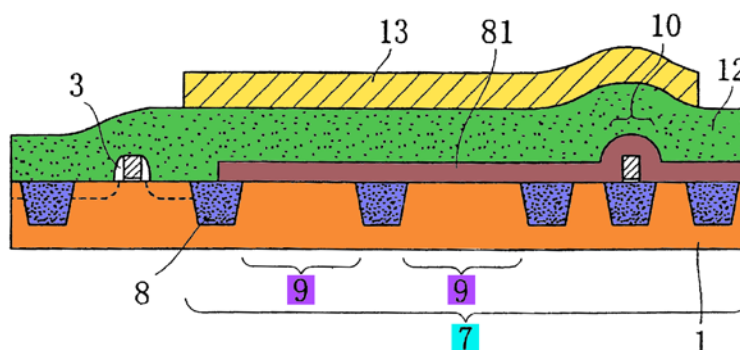
(6) Element 6[f] “a dielectric film interposed between at least said dummy semiconductor portions of said isolation region and said interlayer insulating film.”

107. Oshima discloses this element. The claimed dielectric film is disclosed by Oshima’s oxide film 12, which is placed between the field oxide film 4 of the bus line region 3 and the interlayer film 6. Oshima at 4:47-6:33. Oshima specifies that “the oxide film 12 can be grown by thermal oxidation In order to reduce the wiring capacitance, the thicker the oxide film 12 is, the better will be the result.” Oshima at 5:13-20. This is true because, as Oshima points out, the greater “t” (thickness between the plates) is in the equation $C_p = \epsilon/t$, the smaller the capacitance is. Oshima at 1:56-62.

[illegible]

Oshima at FIG. 2E (annotated)

Fig. 12



'736 Patent at FIG. 12 (annotated)

108. Oshima also explains that the purpose of adding the oxide film 12 is the same as the '736 Patent's purpose of adding its dielectric film. Oshima explains that "[a]s a result of the above-mentioned process, the thickness of the interlayer film 6 formed between the semiconductor substrate 8 and the bus line region wiring layer 7 can be increased Therefore, it is possible to markedly reduce the wiring capacitance" Oshima at 5:37-44."

Compare '736 Patent at 24:35-43 (“the underlying insulating film 81³ composed of the silicon oxide film is present over the isolation region 7, so that the distance between the wiring and the substrate is longer than in the conventional semiconductor device shown in [APA] FIG. 19. Since the wiring-to-substrate capacitance decreases in inverse proportion to the distance, the wiring-to-substrate capacitance is reduced in the semiconductor device according to the present embodiment, resulting in a higher operating speed.”).

109. Although Oshima does not disclose the oxide film 12 “between at least said *dummy semiconductor portions of said isolation region* and said interlayer insulating film,” it would have been obvious for a POSITA to integrate Oshima’s oxide film into the APA, as I discuss below in Section VIII.B.1(7). Or, it would have been obvious for a POSITA to replace Oshima’s field oxide film 4 with trenches and dummy semiconductor portions, as I discussed above in Section VIII.B.1(3).

³ The discussion of FIG. 12 in the '736 patent refers to the claim dielectric film as an “underlying insulating film,” but these refer to the same thing.

(7) **Element 13[f] “a resistor film formed under said wire, and between said interlayer insulating film and at least said dummy semiconductor portions of said isolation region”**

110. Oshima discloses a resistor film via its disclosure of poly silicon layer 9. It specifies that in the process of forming oxide film 12, “a poly silicon layer 9 is formed . . . all over the surface of the entire field oxide film 4 [and] the poly silicon layer 9 is oxidized into an oxide film 12.” Oshima at 4:46-5:21. This process is shown in Oshima FIGS. 2A through 2E, in which the entire polysilicon is oxidized. But Oshima’s second embodiment discloses a case “where the additional thermal process is limited due to the restriction of the processing conditions, [so] it is impossible to perfectly oxidize the poly silicon layer 9 formed under the bus line region 3. Therefore, the poly silicon layer 9 *inevitably remains* under the oxide film 12 formed by thermal oxidization.” Oshima at 6:34-42. This is shown in FIG. 3 (annotated), below.

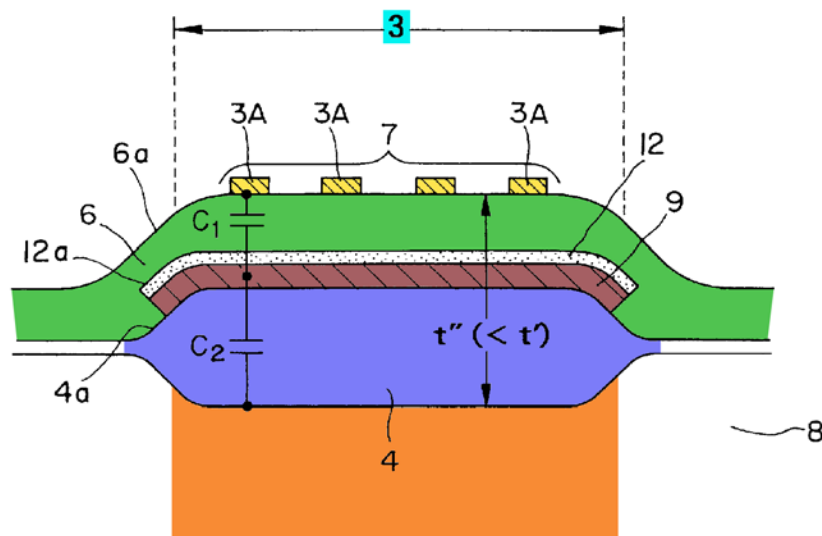


FIG. 3

111. Oshima's poly silicon layer 9 is thus similar to the '736 Patent's polysilicon resistor film 53. *See* Oshima at 6:37-42, 6:43-64 (explaining how poly silicon layer 9 reduces wiring-to-substrate capacitance); *see also* '736 Patent at 16:3-7, 16:11-15, 18:28-19:12 (allowing for various levels of resistivity).
112. Oshima's poly silicon film 9 is also formed under the wiring layer 7. As I explained above, it would have been obvious to a POSITA to change the orientation of the wires in Oshima to have them cover the trench and dummy semiconductor portions (which would have been obvious to implement in Oshima, *see supra* Section VIII.B.1(3)). *See supra* § VIII.B.1(5).
113. And Oshima's poly silicon film 9 is also between the interlayer insulating film 6 and the field oxide film 4 of the bus line region 3 (the isolation

region). *See supra* § VIII.B.1(3) (obvious to replace the field oxide film 4 with STI and dummy semiconductor portions).

114. It would have been obvious for a person of ordinary skill in the art to integrate Oshima's oxide film 12 (claim 6) or poly silicon layer 9 (claim 13) into the APA. The APA readily provides the motivation to do so: it acknowledges that the increased wiring-to-substrate capacitance for devices isolated with STI is greater than that for devices isolated with large field oxide regions, such as LOCOS. '736 Patent at 1:10-34; *see also supra* § V.C (discussing that such a problem was well-known in the art by the priority date of the '736 Patent). Oshima is also directed to ***the very same problem*** that the '736 Patent is seeking to solve. *See* Oshima at Abstract, 1:5-10, 1:14-23, 2:29-34, 2:37-43 (“[I]t is an object of the present invention to provide a semiconductor integrated circuit . . . which can realize the high speed operation, low power consumption, and chip size reduction, by reducing the wiring capacitance”). And indeed, Oshima proposes the ***very same solution***. *Id.* at 5:37-44 (“As a result . . . the thickness of the interlayer film 6 formed between the semiconductor substrate 8 and the bus line region wiring layer 7 can be increased Therefore, it is possible to markedly reduce the wiring capacitance”), 6:43-64 (“it is possible to reduce the capacitance C, as compared with the conventional structure

having no floating terminal between the bus line region wiring layer 7 and the semiconductor substrate 8.”).

115. Oshima takes advantage of fundamental characteristics of a capacitor—namely that (1) increasing distance between the capacitor “plates,” and (2) placing capacitors in series—to reduce wiring-to-substrate capacitance. *See supra* § V.C. Thus, a POSITA reading Oshima and the APA would have understood that combining known elements (*i.e.*, oxide film 12 or poly silicon film 9) would have led to such expected results.
116. Alternatively to implementing Oshima’s oxide film 12 or poly silicon film 9 into the APA, it would have been obvious to substitute Oshima’s field oxide film 4 with a combination of trench portions and dummy semiconductor portions due to the advantages of STI over LOCOS, which the APA acknowledges. *See supra* § VIII.B.1(3).

(8) Additional Reasons to Combine the APA and Oshima

117. Various other motivations to combine exist as well. As already explained, all of the limitations of claims 6 and 13 except for the last of each are disclosed in the APA (*see supra* § V.D), and Oshima teaches the last limitations oxide film 12 or poly silicon film 9 leads to a reduction of wiring-to-substrate capacitance. A POSITA would have been motivated to implement these structures into the APA in light of the reasons explained

immediately above in order to reduce the increased wiring-to-substrate capacitance issue that both the APA and Oshima identified as problematic. *See, e.g.*, Oshima at 5:37-44, 6:43-64; '736 Patent at 3:7-13, 16:19-35, 24:34-43.

118. Indeed, both the APA and Oshima seek to mitigate the increased capacitance that occurs with the miniaturization of semiconductor components. Specifically, the APA explains that one side-effect of such miniaturized structures shown in FIG. 19 is that the wire-to-substrate capacitance is undesirably higher than the structures that utilize LOCOS, an isolation technique which could no longer reliably be used as structures became smaller in each successive “generation.” *See* '736 patent at 2:50-3:30 (“Although the formation of the island pattern composed of the dummy semiconductor portions in the isolation region has the advantage of achieving planarization with excellent in-plane uniformity, it also has the possibility of increasing the wiring-to-substrate capacitance and resultantly reducing the operating speed of the semiconductor device.”). In other words, APA admits that the undesirable effect of increasing wiring-to-substrate capacitance as a result of miniaturization was well-known.
119. Oshima similarly notes that “the wiring capacitance of the bus line region is reduced, so that the operation speed can be increased, the power

consumption can be decreased, *and the chip size can be reduced.*” Oshima at Abstract; *see also id.* at 2:19-28, Saraswat at 4. It was well known that “the suppression of an increase of the wiring capacitance” was “particularly serious.” Oshima at 2:29-34.

120. Oshima further explains that, with its invention, “it is possible to markedly reduce the wiring capacitance down to about 12 to 25% of that of the conventional integrated circuit” Oshima at 5:41-44.
121. Thus a POSITA would have been motivated to incorporate Oshima’s oxide film 12 or poly silicon film 9 into the APA to reduce the increased wiring-to-substrate capacitance, which was already a well-known problem: doing so is a simple combination of known prior art elements (oxide film 12 and poly silicon film 9) according to known methods and yields predictable results (increasing the distance between capacitor plates, or placing capacitors in series reduces overall capacitance).
122. To summarize, Oshima, like the ’736 Patent, sought to solve the problem of increased wiring-to-substrate capacitance, which, as both explain, is a problem that is more acute as semiconductor devices get smaller. Both model the wiring-to-substrate capacitance using the parallel plate model. And both implement a dielectric film or resistor film to increase the distance

between the wire and the substrate (claim 6) or act as a capacitor in series (claims 6 and 13) in order to reduce overall wiring-to-substrate capacitance.

2. **Claim 7**

(1) **Element 7[a]: “A semiconductor device according to claim 6”**

123. Claim 7 depends from claim 6. As described above, the APA and Oshima disclose every element of claim 6.

(2) **Element 7[b]: “wherein said dielectric film is an underlying insulating film interposed between said interlayer insulating film and said dummy semiconductor portions and said second trench portion.”**

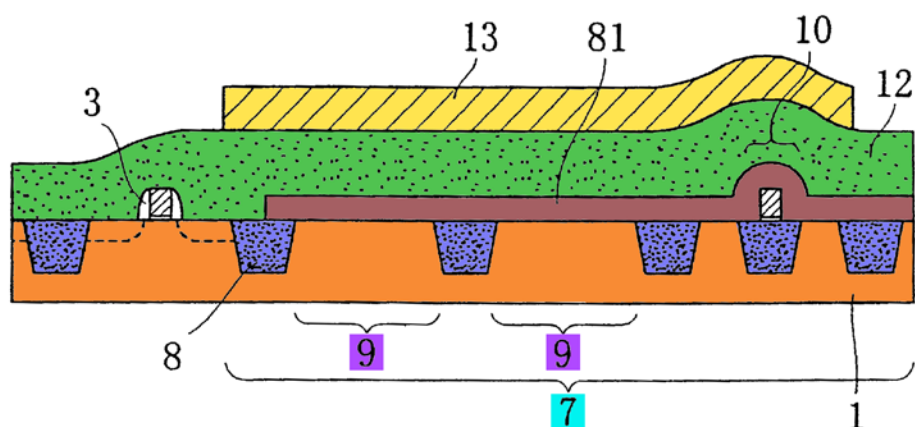
124. As explained above, Oshima discloses an oxide film 12 between the interlayer insulating film 6 and the field oxide film 4 in the bus line region 3. Oshima at 4:46-6:33, FIG 2E. It would have been obvious to a POSITA to incorporate Oshima’s oxide film 12 into the APA. *See supra* § VIII.B.1(6). Doing so would result in the oxide film being an underlying film between the interlayer insulating film 12 and the dummy semiconductor portions and second trench portions, as required by this limitation.

125. Alternatively, as I explained above, replacing Oshima’s field oxide film 4 with trench portions and dummy semiconductor portions would have been obvious to a POSITA. *See supra* § VIII.B.1(3).

[illegible]

Oshima at FIG. 2E (annotated)

Fig. 12



'736 Patent at FIG. 12 (annotated)

126. Thus, the APA in combination with Oshima disclose this element of claim 7 of the '736 Patent, and invalidate claim 7.

3. Claim 8

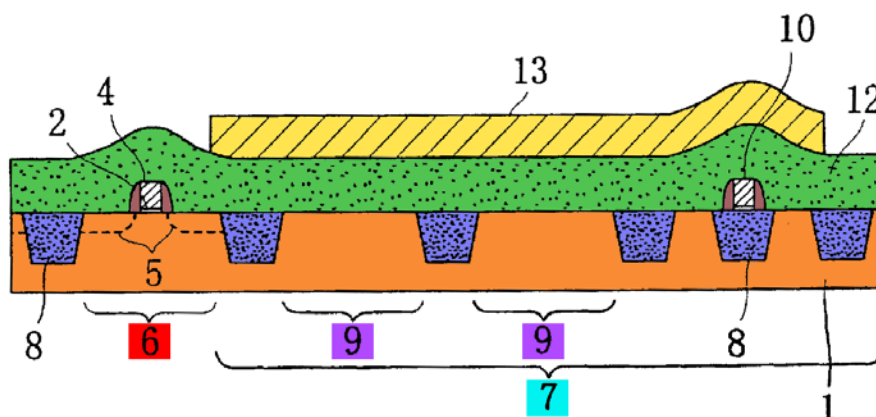
(1) Element 8[a]: “A semiconductor device according to claim 7”

127. Claim 8 depends from claim 7. As described above, the APA and Oshima disclose every element of claim 7.

- (2) **Element 8[b] “further comprising a gate electrode formed on the semiconductor substrate within said active region and sidewalls made of an insulating material and formed on both side faces of said gate electrode, wherein said underlying insulating film is formed of the same film as forming said sidewalls.”**

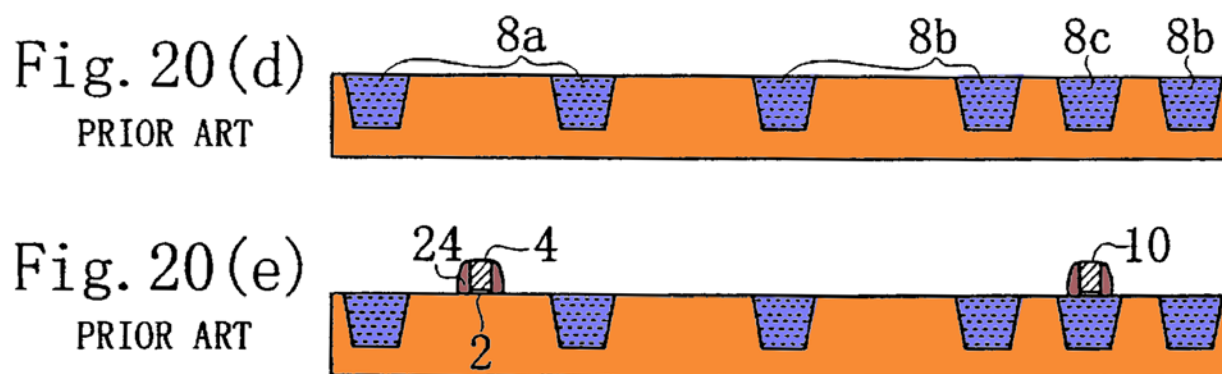
128. The APA discloses a gate electrode, formed with sidewalls, within the active region of the semiconductor substrate, as shown below in FIG. 19 (annotated). The gate electrode is labeled with numeral 4 and is between sidewalls (unlabeled in FIG. 19). See '736 Patent at 1:38-40 (“As shown in FIG. 19, an active region 6 of a P-type silicon substrate 1 is formed with . . . a gate electrode 4 made of a polysilicon film . . .”).

Fig. 19
PRIOR ART



129. The sidewalls are also made of the same material as underlying insulating film 81, as required by this claim element. The '736 Patent describes the

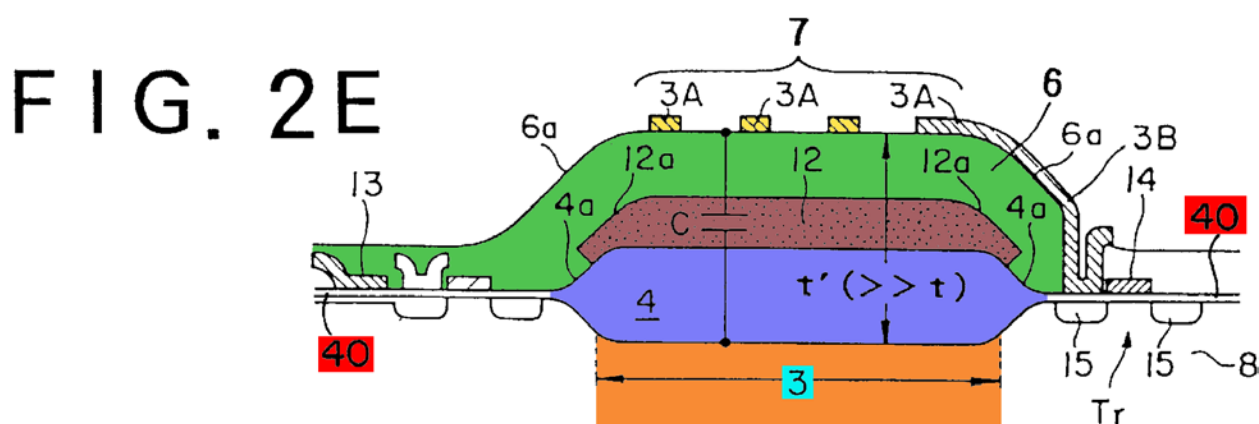
manufacturing process of the device shown in FIG. 19, and when describing the formation of the sidewalls, it states: “In the step shown in FIG. 20(e), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique.” ’736 Patent at 2:26-29. FIG. 20(e) (annotated), as well as the manufacturing step leading up to it, FIG 20(d) (annotated), is shown below. Such a “known technique” included creating sidewalls from a silicon oxide. *See, e.g.*, U.S. Patent No. 4,786,609 (“Chen”) at 1:41-44, 5:3-10 (Ex. 1122); ’736 Patent at FIG. 13(g), 24:9-16 (explaining that both the sidewalls in FIG. 12 (the same as those in APA FIG. 19) and the underlying insulating film are formed from a single silicon oxide film 82, implying that the sidewalls in APA FIG. 19 are also made of a silicon oxide).



130. The semiconductor device of the APA, however, does not have the underlying insulating film 81. As I discussed above, however, it would have been obvious to implement Oshima’s oxide film 12 into the APA. *See supra*

§ VIII.B.1(6). Both Oshima's oxide film 12 and the sidewalls described in the APA are of the same material. *See* Oshima at 5:13-18; '736 Patent at 2:24-29, 24:9-14.

131. Or, it would have been obvious to modify Oshima such that it discloses this claim element. Oshima discloses an active region with a gate electrode, labeled 14 in FIG. 2E (annotated) below. *See also* Oshima at 4:63-5:3.



132. While Oshima does not explicitly show sidewalls around the gate electrode, they were well-known to a POSITA at the time of the '736 Patent. For example, as I discussed immediately above, the APA itself acknowledges that sidewalls were known. '736 Patent at 2:26-29. It was also known to POSITAs at the time of the invention of the '736 Patent to use silicon oxide as sidewalls. Chen at Abstract, FIG. 1j, 1:13-58 (explaining the benefits of using sidewalls on gate electrodes), 2:27-36 (Ex. 1122).

133. It would have been obvious to a POSITA to implement the sidewalls taught in the APA. Implementing the sidewalls would have been standard practice

at the time of the '736 Patent, and would not have materially contributed to the complexity of the manufacturing process of the integrated circuit. Sidewall spacers allow the fabrication of “lightly doped drain” regions, and thus contribute to the enhanced reliability of devices through reduction of so-called hot carrier effects.

134. Thus, the APA and Oshima invalidate claim 8.

4. **Claim 9**

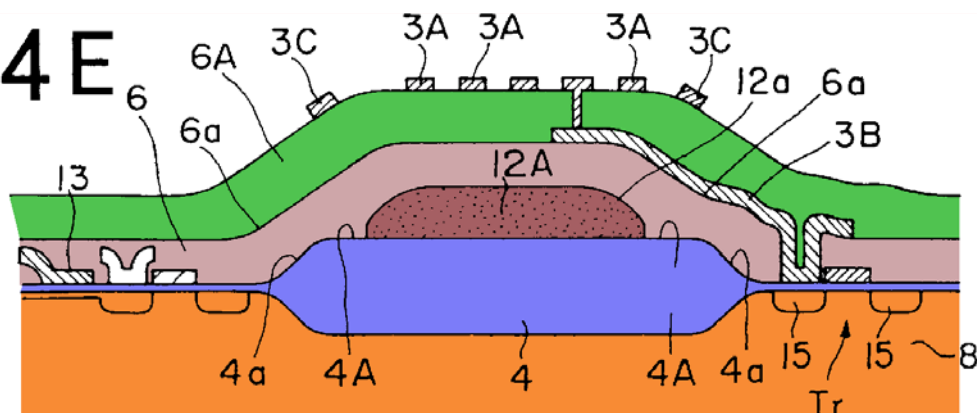
(1) **Element 9[a]: “A semiconductor device according to claim 8”**

135. Claim 9 depends from claim 8, which depends from claim 7, which depends from claim 6. As described above, the APA and Oshima disclose every element of claim 8.

(2) **Element 9[b]: “wherein said underlying insulating film is composed of a multilayer film.”**

136. Oshima discloses this element. It discloses an embodiment—shown below in FIG. 4E (annotated)—where an additional insulating film 6 is formed atop oxide film 12A. Oshima at 7:7-9. Thus, the “multilayer film” required by this element is disclosed by the additional insulating film 6 and the oxide film 12A.

FIG. 4E



5. Claim 11

(1) Element 11[a]: “A semiconductor device according to claim 6”

137. Claim 11 depends from claim 6. As described above, the APA and Oshima disclose every element of claim 6.

(2) **Element 11[b]: “wherein said dielectric film is composed of at least one of a silicon oxide film and a silicon nitride film.”**

138. Oshima discloses this element because Oshima describes the poly silicon layer 9 as being oxidized into oxide film 12. Oshima at 5:13-14. Thus, because oxide film 12 is formed via a reaction between oxygen and silicon, it is a silicon oxide film.

139. Thus, Oshima discloses this element of claim 11 of the '736 Patent, and the
APA in combination with Oshima invalidates claim 11.

6. **Claim 14**

(1) **Element 14[a]: “A semiconductor device according to claim 13”**

140. Claim 14 depends from claim 13. As described above, the APA and Oshima disclose every element of claim 13.

(2) **Element 14[b]: “wherein said resistor film is an underlying resistor film formed to extend continuously over said dummy semiconductor portions and said second trench portions.”**

141. As explained above, Oshima discloses a poly silicon layer 9 beneath the interlayer insulating film 6, and as extending continuously over the field oxide film 4 in bus line region 3. *See* Oshima at 6:34-64, FIG 3. It would have been obvious to a POSITA to incorporate Oshima’s poly silicon layer 9 into the APA. *See supra* § VIII.B.1(7). Doing so would result in the poly silicon layer 9 being an extending continuously over the dummy semiconductor portions and second trench portions, as required by this limitation.

142. Alternatively, as I explained above, replacing Oshima’s field oxide film 4 with trench portions and dummy semiconductor portions would have been obvious to a POSITA. *See supra* § VIII.B.1(3).

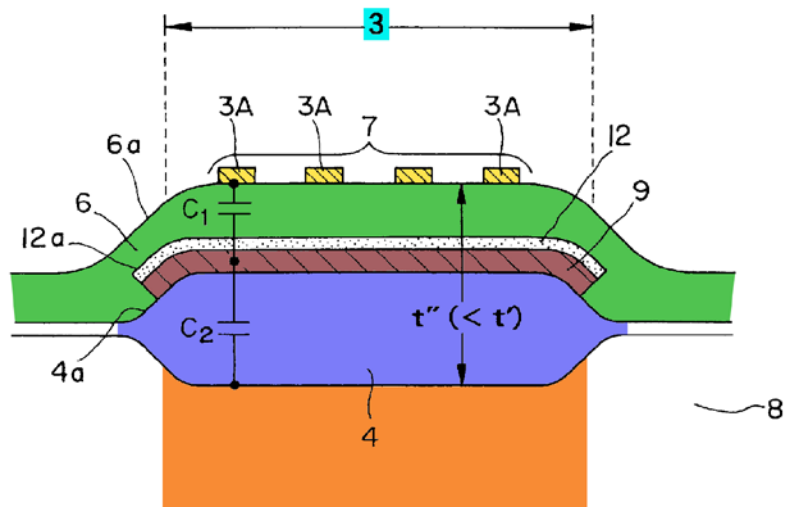
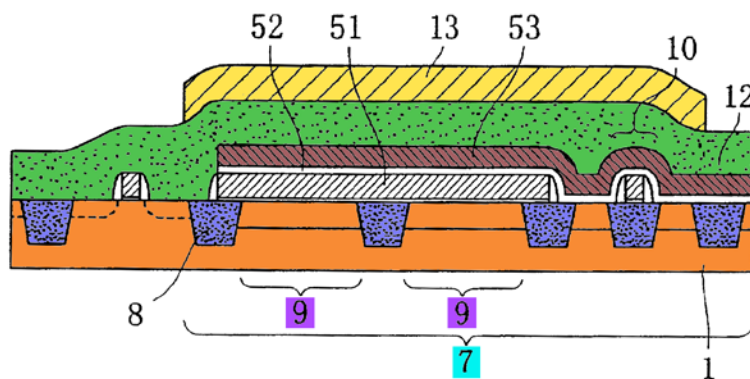


FIG. 3

Oshima at FIG. 3 (annotated)

Fig. 5



'736 Patent at FIG. 5 (annotated)

143. Thus, the APA in combination with Oshima disclose this element of claim 14 of the '736 Patent, and invalidate claim 14.

7. **Claim 16**

(1) **Element 16[a]: “A semiconductor device according to claim 13”**

144. Claim 16 depends from claim 13. As described above, the APA and Oshima disclose every element of claim 13.

(2) **Element 16[b]: “further comprising an element having an electrode member composed of a conductor film formed on the semiconductor substrate within said active region, wherein said resistor film is composed of the same material as composing said electrode member.”**

145. As explained above, Oshima discloses that “*a poly silicon layer 9* is formed . . . all over the surface of the entire field oxide film 4, in order to form *plate electrodes 13 of memory cells* and *gate electrodes 14 of the transistors* (both shown in FIG. 2(E)) in the circuit block region (i.e., active region) 2 . . .” Oshima at 4:63-5:3. The plate electrodes and gate electrodes, which are contained in the active region of Oshima (in circuit block 2, indicated by numeral 40), disclose the claimed electrode member. The electrodes in Oshima are created from the same material as poly silicon layer 9. Although Oshima FIG. 3 (annotated) below does not show the circuit block 2 (40 in FIG. 2E) or the electrodes, a POSITA would understand that those structures would be contained on the left and right sides of the figure, as they are in FIG. 2E (annotated) below.

FIG. 2E

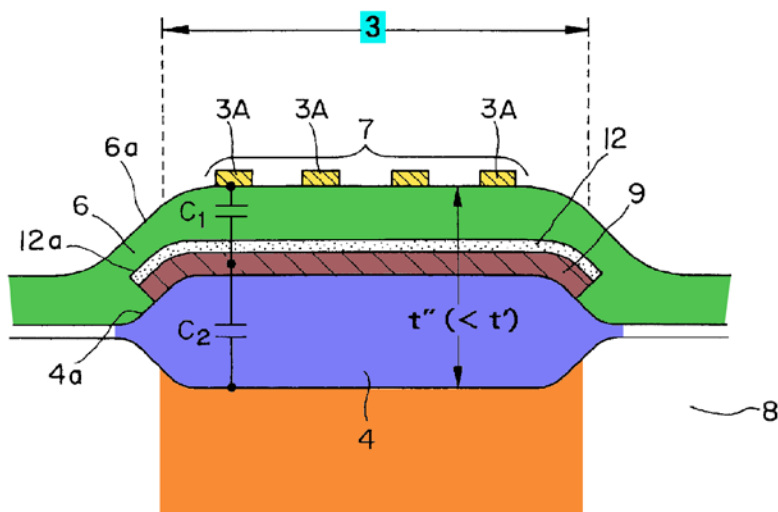
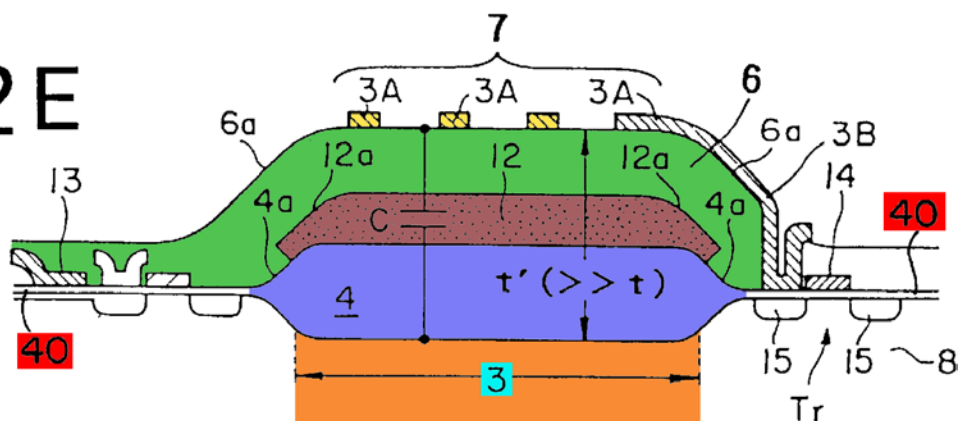


FIG. 3

146. Accordingly, Oshima teaches this limitation, and the APA in combination with Oshima discloses claim 16 of the '736 patent.

8. **Claim 20**

(1) **Element 20[a]: "A semiconductor device according to claim 13"**

147. Claim 20 depends from claim 13. As described above, the APA and Oshima disclose every element of claim 20.

(2) Element 20[b]: “wherein said resistor film is composed of at least one of a polysilicon film and an amorphous silicon film.”

148. Oshima discloses “poly silicon film 9,” which is, as this claim element requires, composed of a polysilicon film. Accordingly, Oshima teaches this limitation, and the APA in combination with Oshima discloses claim 20 of the ’736 patent.

IX. Secondary Considerations of Non-Obviousness

149. It is my opinion that secondary considerations do not support the non-obviousness of the Challenged Claims of the ’736 Patent. I have seen no evidence of secondary considerations that would tend to show non-obviousness, including commercial success, long-felt need, failure of others, skepticism, praise, teaching away, recognition of a problem, or copying by competitors.

150. I am aware that Matsushita Electric Industrial Co. (“Matsushita”), which changed its name to Panasonic Corporation (“Panasonic”) in 2008,⁴ is a consumer electronics company that sells products such as air conditions, refrigerators, washing machines, and televisions. But I am not aware of any

⁴ See, e.g., <http://news.panasonic.com/global/press/data/en081001-4/en081001-4.html> (last accessed Feb. 1, 2018) (Oct. 1, 2008 press release regarding the name change) (Ex. 1123).

innovation related to reducing wiring-to-substrate capacitance by Matsushita or Panasonic. I am not aware of any products relevant to the technology described in the '736 Patent developed by Matsushita or Panasonic, any customers of either, or anything suggesting commercial success of any such products developed by Matsushita or Panasonic. In addition to my personal knowledge of semiconductor design and fabrication, I have performed a general search of resources available to me and have likewise been unable to identify any commercial success of such products developed by Matsushita or Panasonic.

151. I am also generally familiar with Godo Kaisha IP Bridge 1 (“IP Bridge”), but I am not aware of any innovations related to reduced wiring-to-substrate capacitance technologies by IP Bridge. As I understand it, IP Bridge is a non-practicing entity in the business of monetizing patents. Thus, I am not aware of any products developed by IP Bridge, any customers of IP Bridge, or anything suggesting commercial success of any products developed by IP Bridge. In addition to my personal knowledge of semiconductor manufacturing, fabrication, and structures, I have performed a general search of resources available to me and have likewise been unable to identify any commercial success of products developed by IP Bridge.

152. I am also unaware of any long-felt need at the time of the '736 Patent for a reduced wiring-to-substrate capacitance semiconductor utilizing the elements recited in the Challenged Claims. The solutions proposed by the '736 Patent were well-known at that time, including (but not limited to) the systems described in Iranmanesh, which pre-dates the '736 Patent.
153. Nor am I aware of any failure of others to design or implement a reduced wiring-to-substrate capacitance semiconductor similar to the one recited in the Challenged Claims. In fact, I believe there are similar, if not identical, devices, including but not limited to the ones described in Iranmanesh.
154. I have reviewed references from around the time of the alleged invention, and am not aware of any skepticism, praise, or teaching away by others of the reduced wiring-to-substrate capacitance semiconductor recited in the Challenged Claims. In fact, the opposite is true: prior-art references disclose the device of the Challenged Claims.
155. I am unaware of any recognition given to any reduced wiring-to-substrate capacitance semiconductor that embodies the Challenged Claims, including any such system that may have been used in products from the various assignees/assignors of the '736 Patent.
156. I am not aware of any evidence that others have copied the invention recited in the Challenged Claims.

157. Should IP Bridge assert that secondary considerations support a finding of non-obviousness, I reserve the right to submit another declaration addressing those new assertions.

X. Conclusion

158. I, John Bravman, hereby declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both. *See* 18 U.S.C. § 1001.

Date: March 7, 2018

Respectfully submitted,



John Bravman, Ph.D.