

257	509
Class	Subclass
ISSUE CLASSIFICATION	

PATENT NUMBER
6346736
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U.S. UTILITY Patent Application

③ 40 O.I.P.E.	PATENT DATE
SCANNED AA Q.A. CC	FEB 12 2002

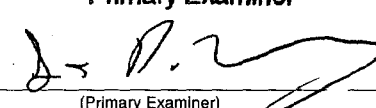
CLASS 257	SUBCLASS 509 509	ART UNIT	EXAMINER Meier
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TITLE OF INVENTION:

protection device in
Div

APPLICANT(S):

ISSUING CLASSIFICATION									
ORIGINAL				CROSS REFERENCE(S)					
CLASS		SUBCLASS		CLASS		SUBCLASS (ONE SUBCLASS PER BLOCK)			
257		509		257		545			
INTERNATIONAL CLASSIFICATION									
401C 33100									
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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. 21	Figs. Drwg. 89	Print Fig. 154	Total Claims 20	Print Claim for O.G. 1
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	<div>Stephen D. Meier Primary Examiner</div> <div> (Primary Examiner) (Date)</div>			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____				10-16-01	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	<div>T. BELL.</div> <div>(Legal Instruments Examiner) (Date)</div>			ISSUE FEE	
				Amount Due \$1280- Date Paid 12-12-01	
				ISSUE BATCH NUMBER N51	

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QUERY

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET
09/469,498	12/22/99	438	2822	43889/898

APPLICANT

TAKAAKI UKEDA, OSAKA, JAPAN; CHIAKI KUDO, KYOTO, JAPAN; TOSHIKI YABU, OSAKA, JAPAN.

CONTINUING DOMESTIC DATA***

VERIFIED THIS APPLN IS A DIV OF 08/978,137 11/25/97 Patent 6,130,139
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371 (NAT'L STAGE) DATA***

VERIFIED
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FOREIGN APPLICATIONS***

VERIFIED JAPAN 8-314762 11/26/96
JAPAN 9-023844 02/06/97
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IF REQUIRED, FOREIGN FILING LICENSE GRANTED 02/02/00

Foreign Priority claimed 35 USC 119 (a-d) conditions met	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> no <input checked="" type="checkbox"/> Yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Verified and Acknowledged	Examiner's Initials Initials	JPX	21	18	4

SEE CUSTOMER NUMBER: 020277

ADDRESS

TITLE
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME A Trench Isolated Semiconductor Device

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:	<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit
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PATENT APPLICATION



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CONTENTS

Date Received
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Date Mailed

1. Application <i>21 Part</i> papers.		
2. <i>Cited Art</i>	<i>12/22/99</i>	
3. <i>Fee / Amendment</i>	<i>12/22/99</i>	
4. <i>Rejection (3 months)</i>	<i>2-26-01</i>	
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8. Formal Drawings (<i>21</i> sheets) set <i>12-12-01</i>		
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US006346736B1

(12) **United States Patent**
Ukeda et al.

(10) **Patent No.:** **US 6,346,736 B1**
(45) **Date of Patent:** **Feb. 12, 2002**

(54) **TRENCH ISOLATED SEMICONDUCTOR DEVICE**

(75) Inventors: **Takaaki Ukeda**, Osaka; **Chiaki Kudo**, Kyoto; **Toshiki Yabu**, Osaka, all of (JP)

(73) Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/469,498**

(22) Filed: **Dec. 22, 1999**

Related U.S. Application Data

(62) Division of application No. 08/978,137, filed on Nov. 25, 1997, now Pat. No. 6,130,139.

Foreign Application Priority Data

Nov. 26, 1996 (JP) 8-314762
Feb. 6, 1997 (JP) 9-023844

(51) **Int. Cl.⁷** **H01L 33/00**

(52) **U.S. Cl.** **257/509; 257/545**

(58) **Field of Search** 257/509, 506, 257/545, 598

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* cited by examiner

Primary Examiner—Stephen D. Meier

(74) *Attorney, Agent, or Firm*—McDermott & Will & Emery

(57) ABSTRACT

The top surface of a P-type semiconductor substrate is partitioned into an active region to be formed with an element and an isolation region surrounding the active region. The isolation region is composed of trench portions and dummy semiconductor portions. An interlayer insulating film is deposited on the substrate, followed by a wire formed thereon. In each of the semiconductor portions, an impurity diffusion layer is formed simultaneously with the implantation of ions into the element so that a PN junction is formed between the impurity diffusion layer and the silicon substrate. A capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions is obtained by adding in series the capacitance in the impurity diffusion layer to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. What results is a semiconductor device having lower total wiring-to-substrate capacitance and a higher operating speed.

20 Claims, 21 Drawing Sheets

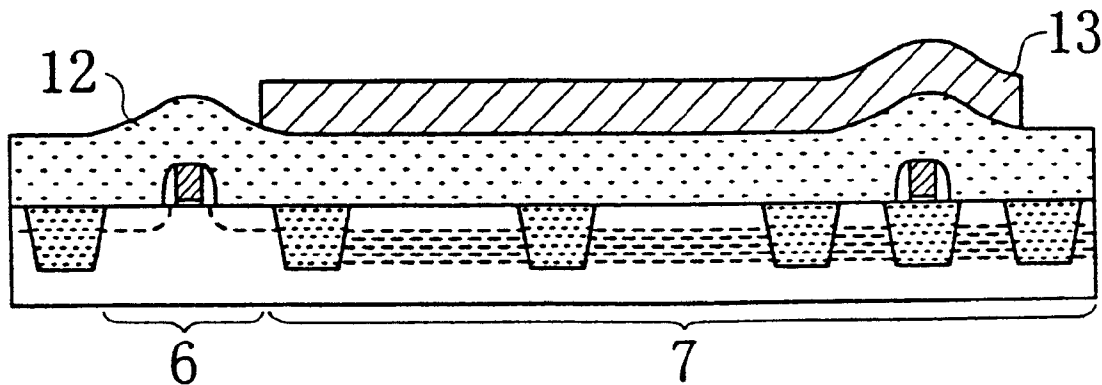


Fig. 1(a)

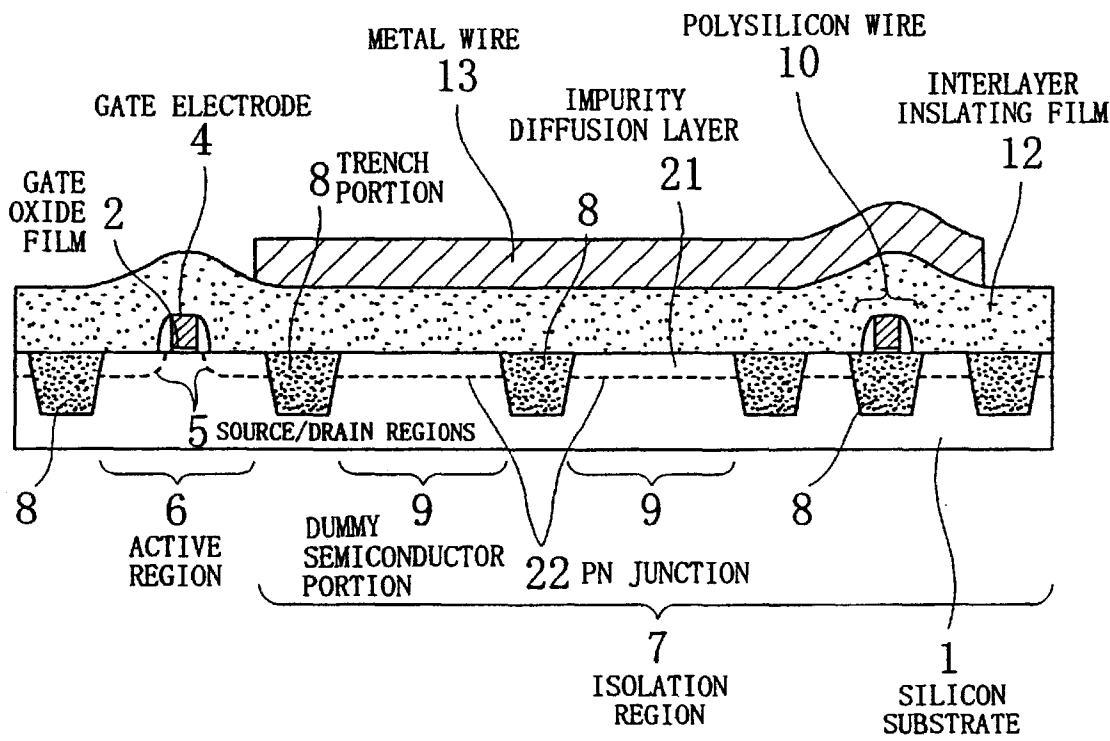
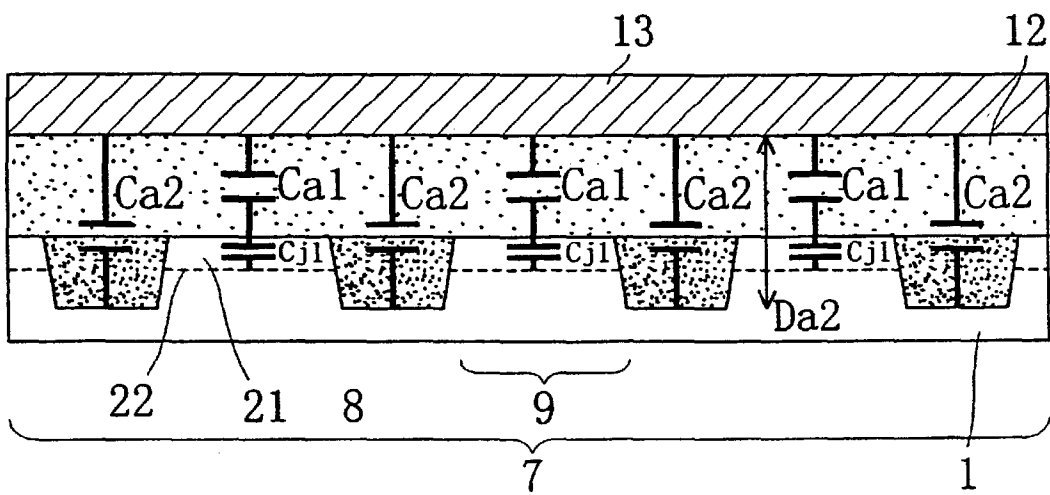


Fig. 1(b)



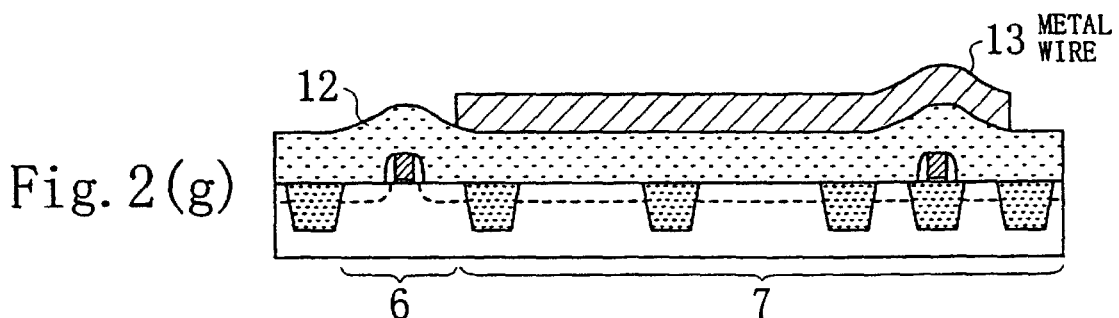
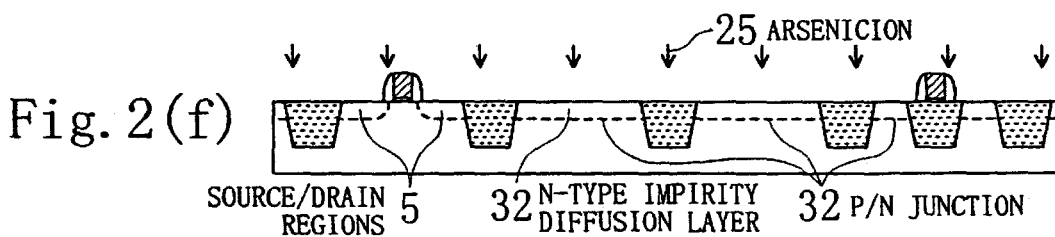
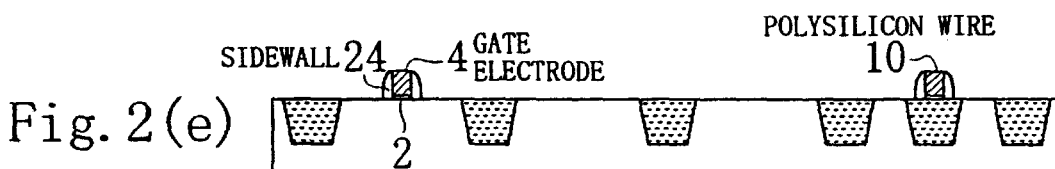
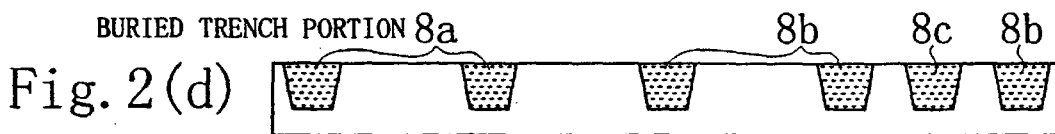
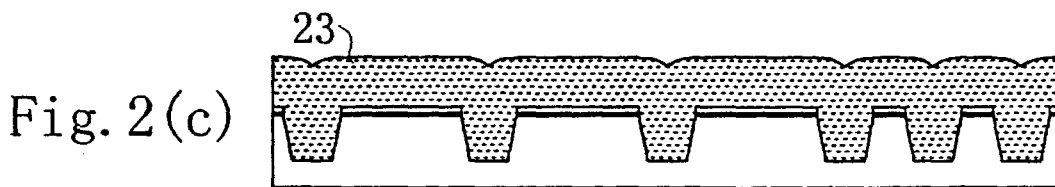
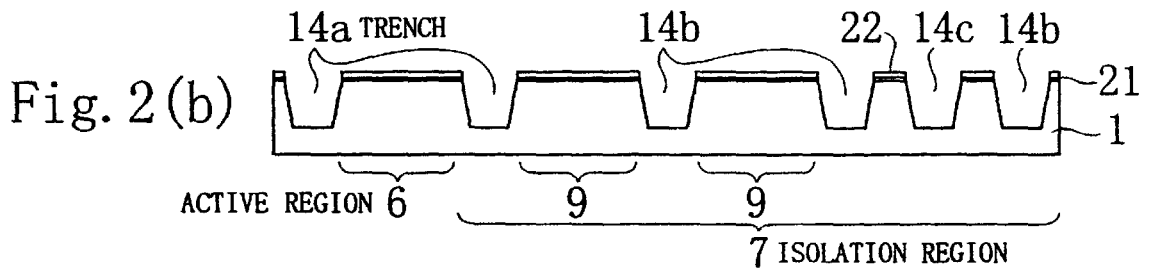
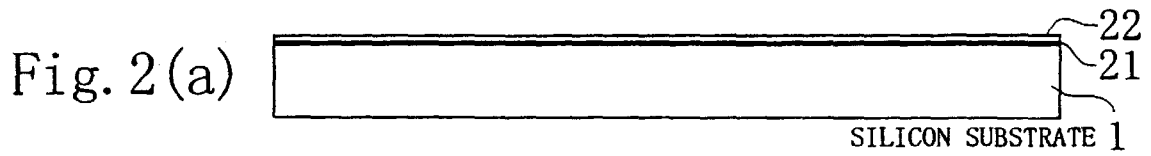


Fig. 3

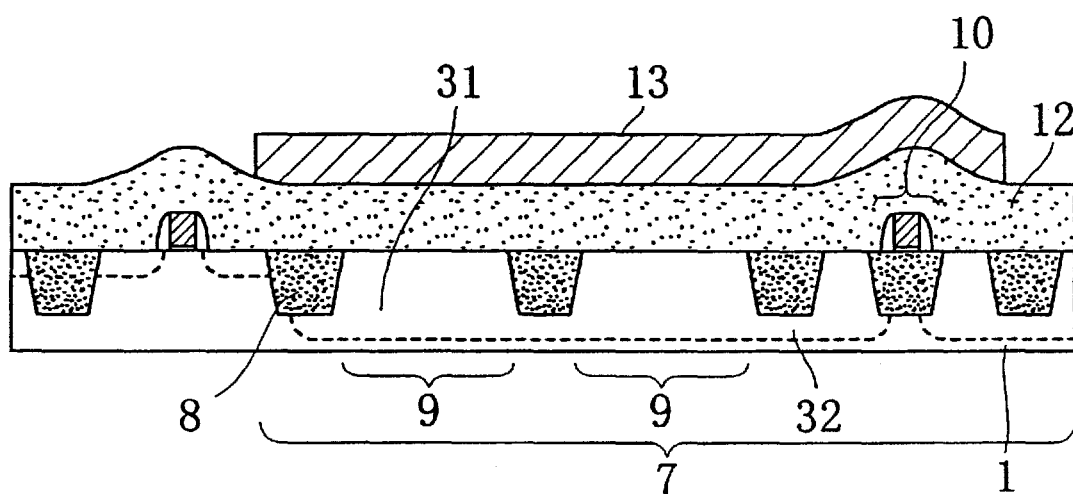


Fig. 4

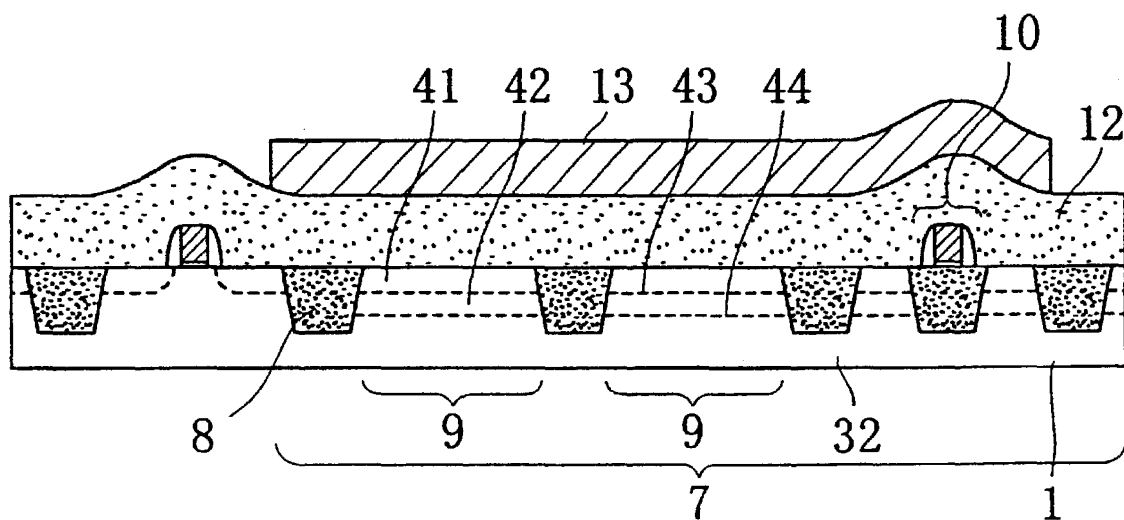
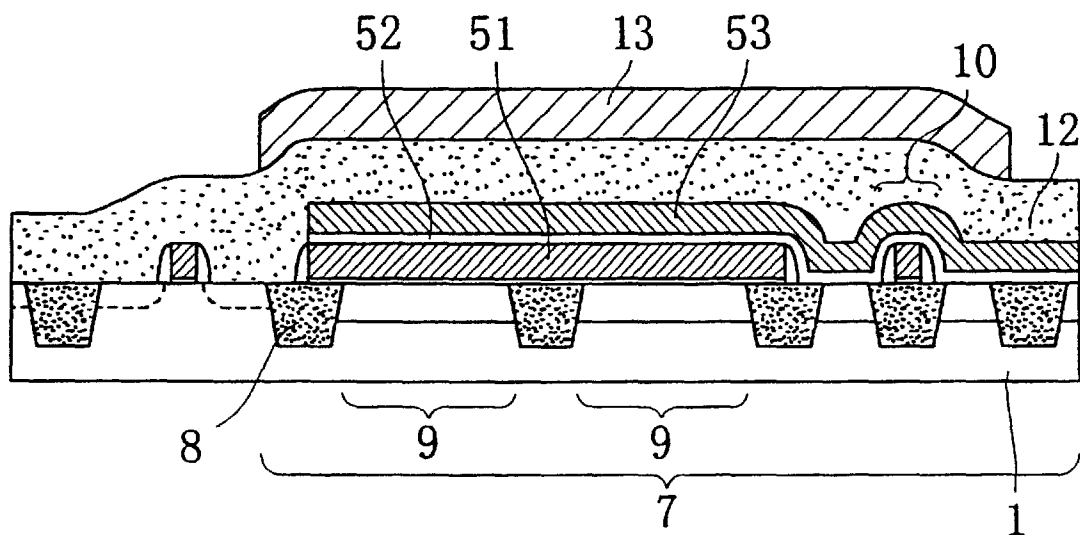


Fig. 5



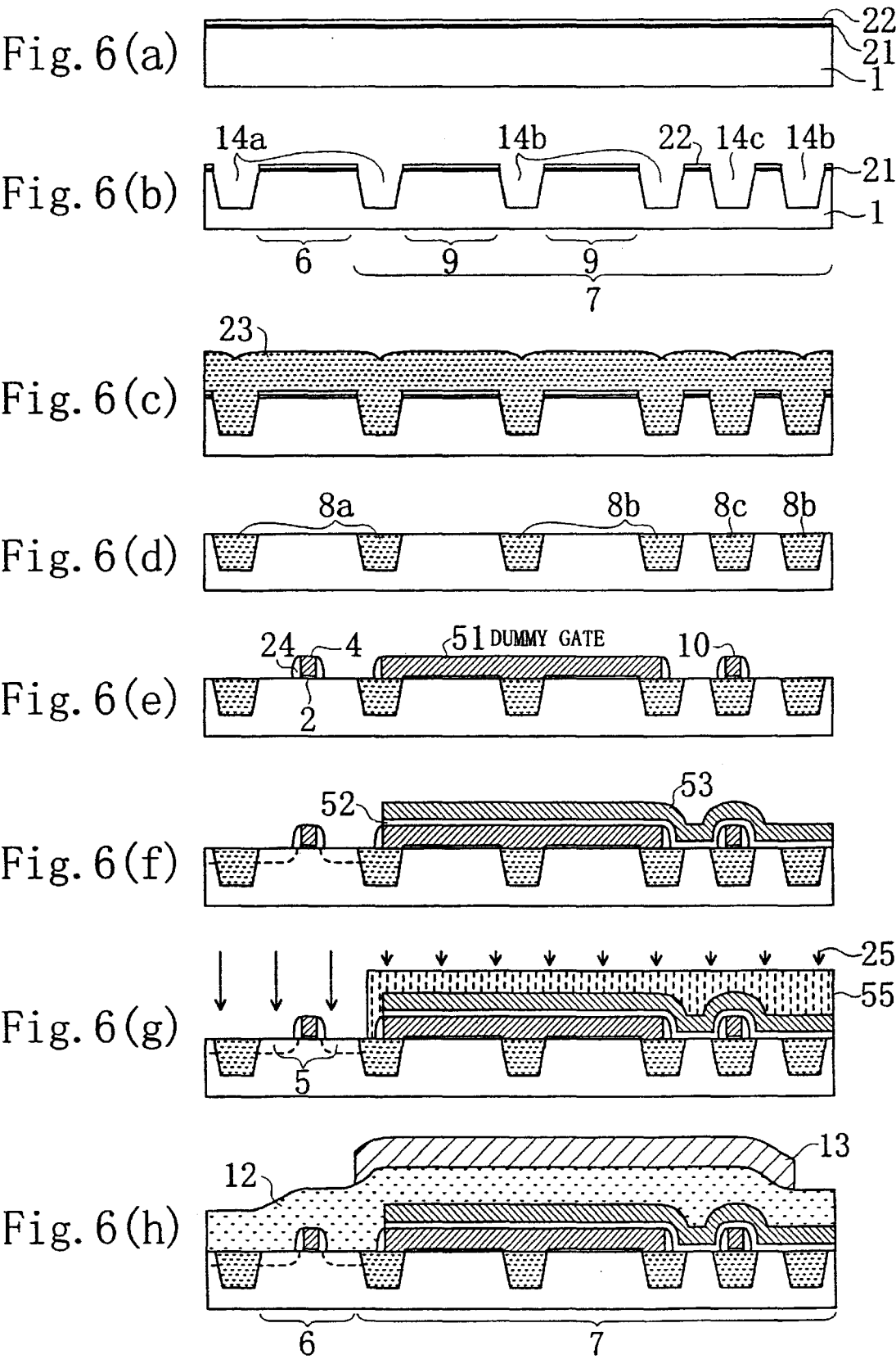


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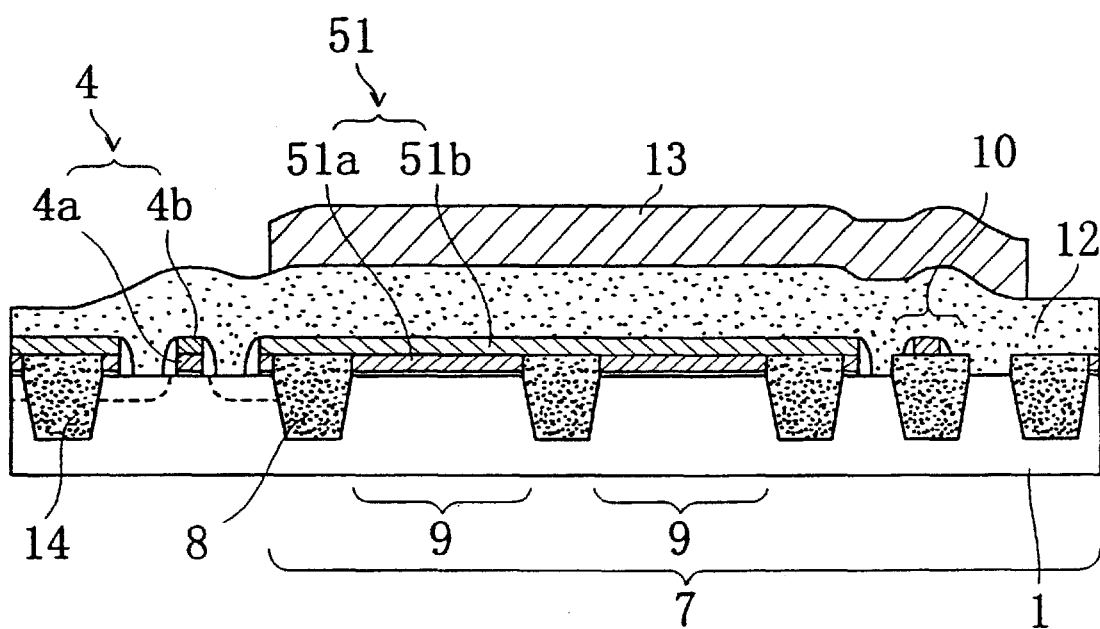
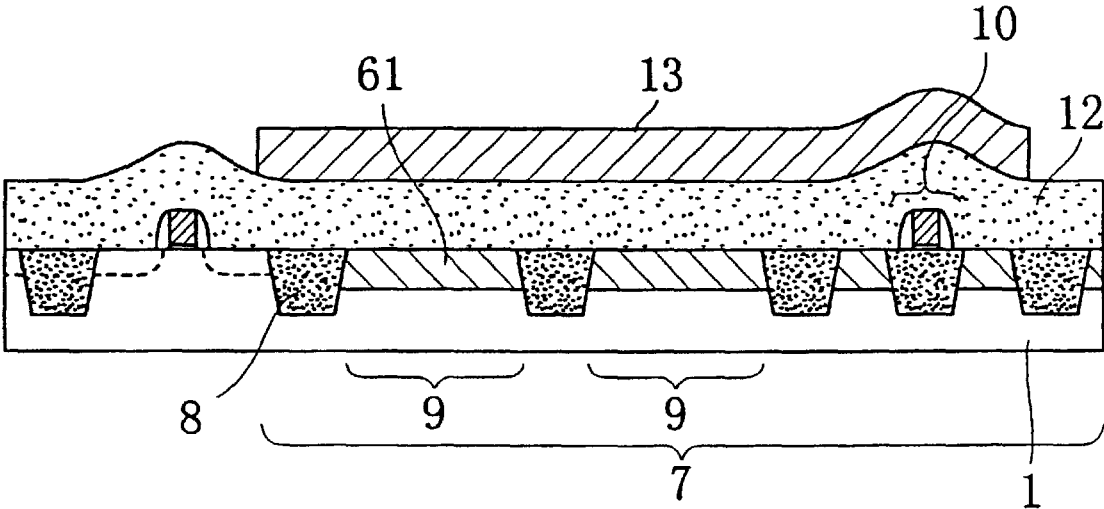
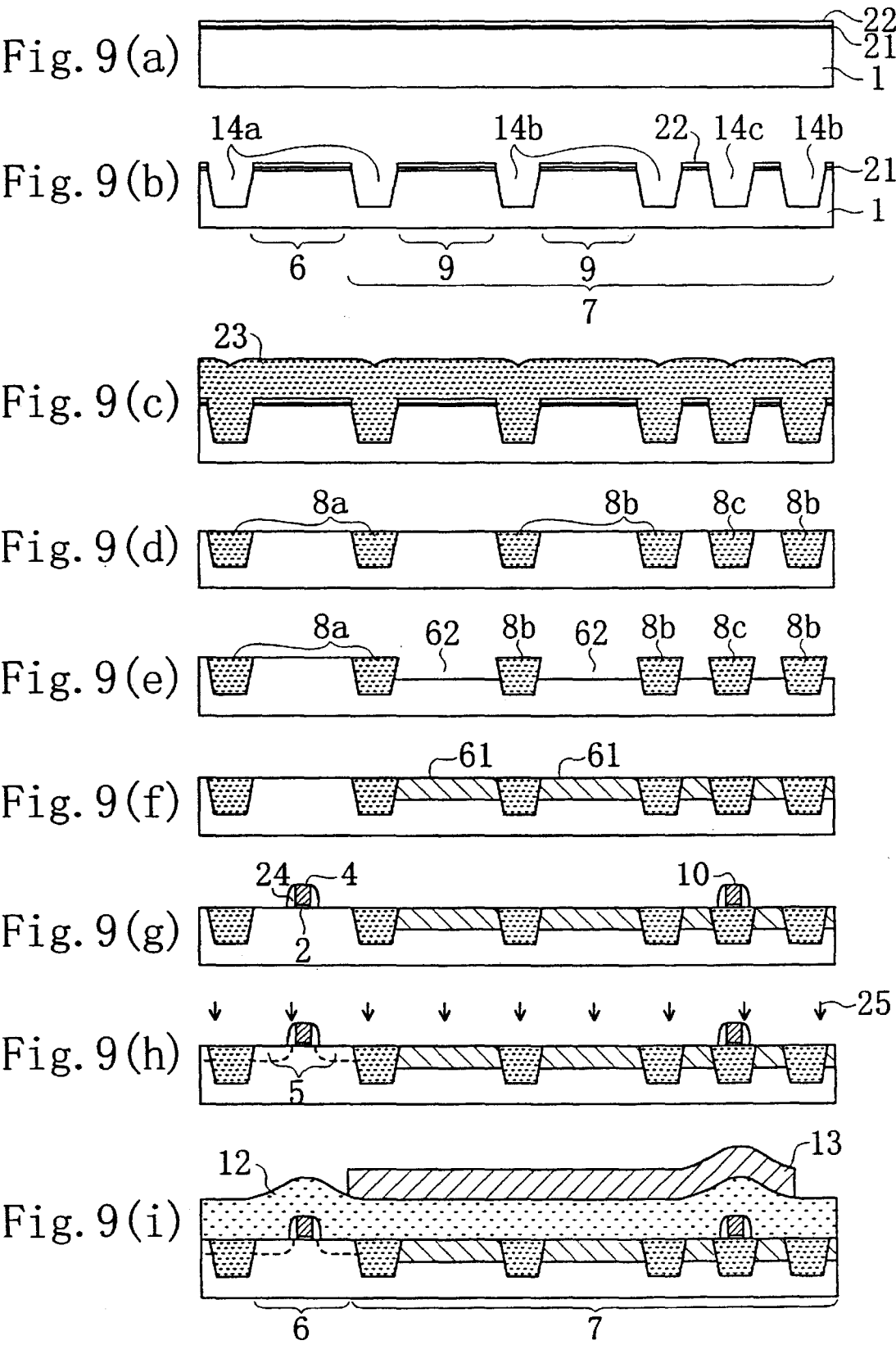


Fig. 8





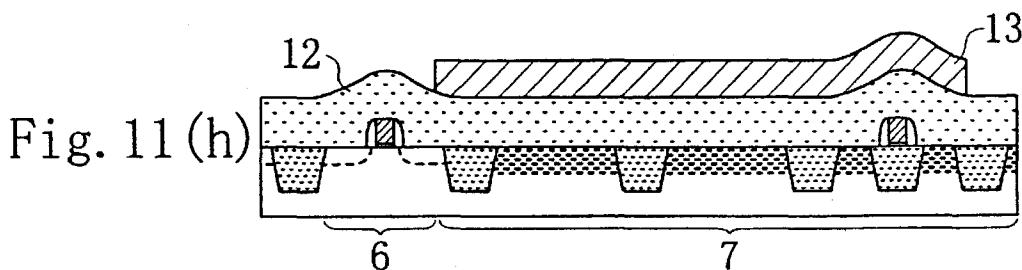
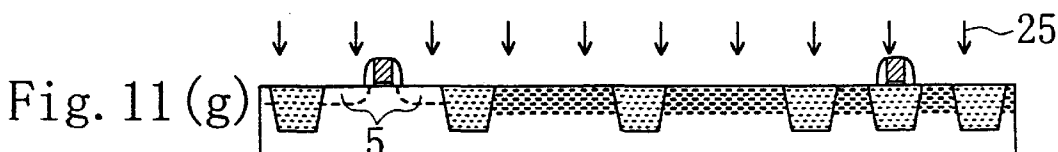
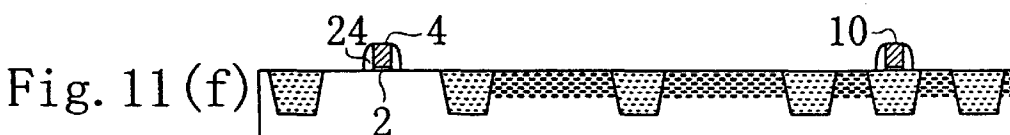
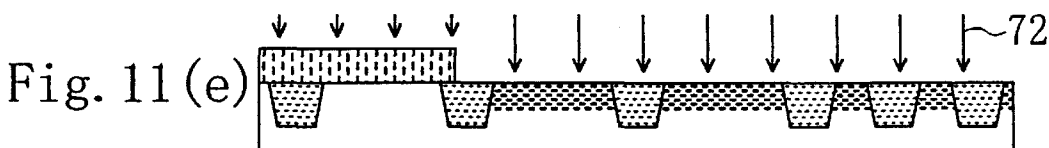
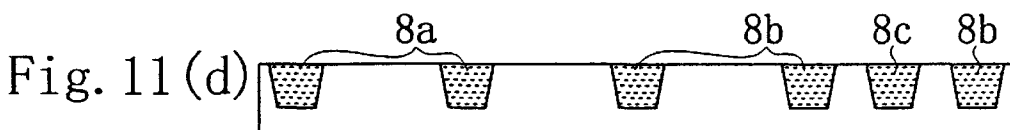
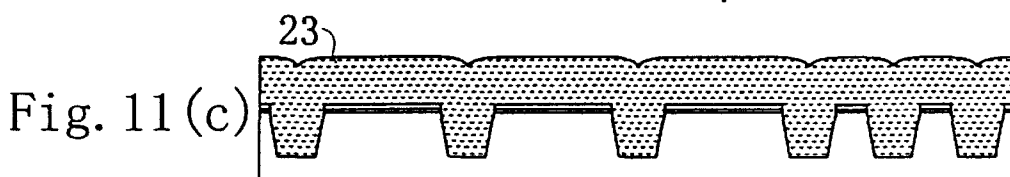
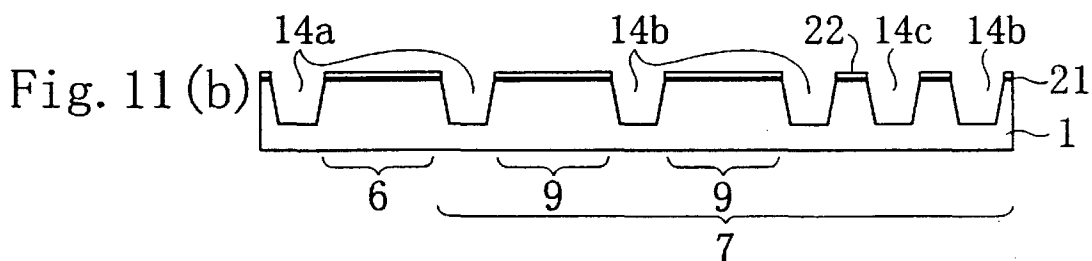
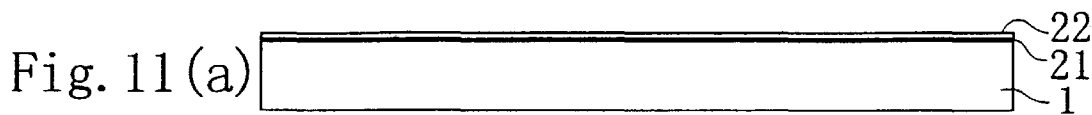
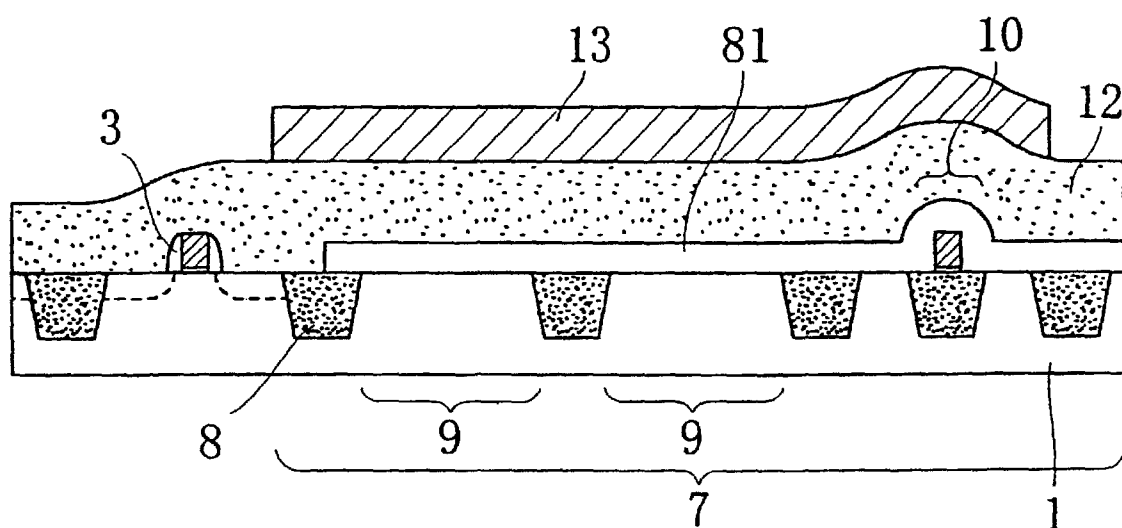


Fig. 12



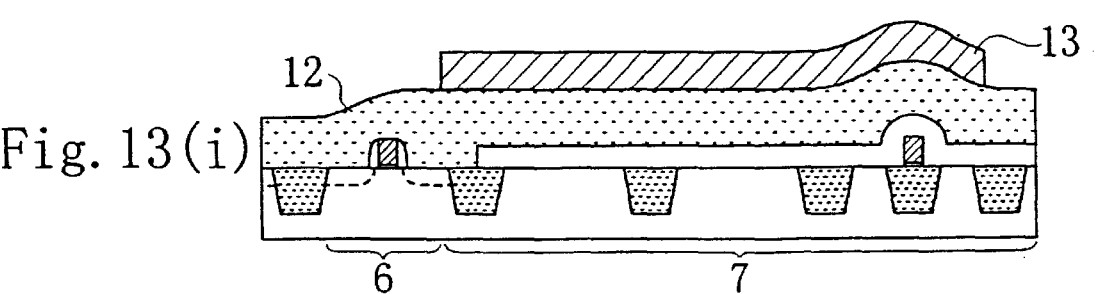
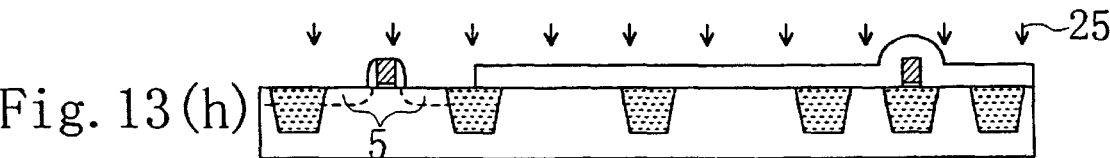
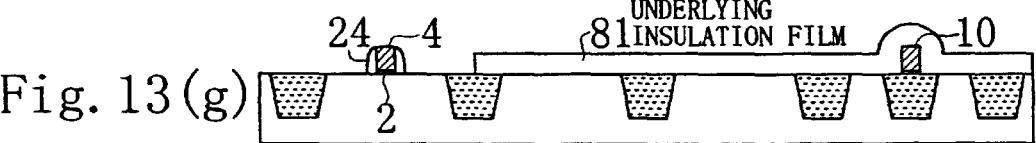
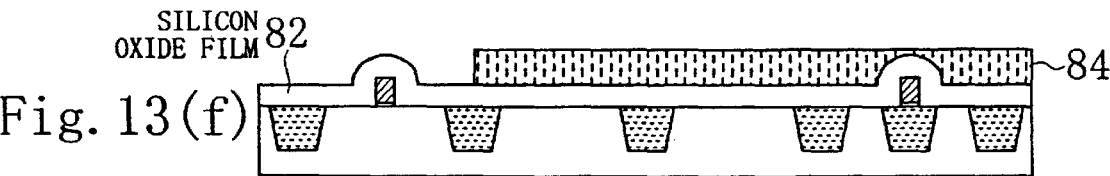
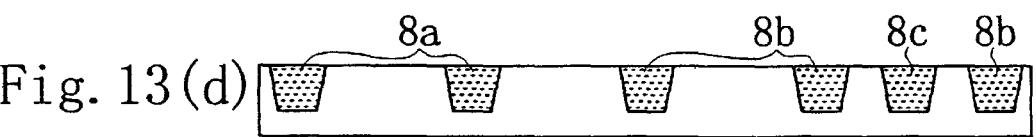
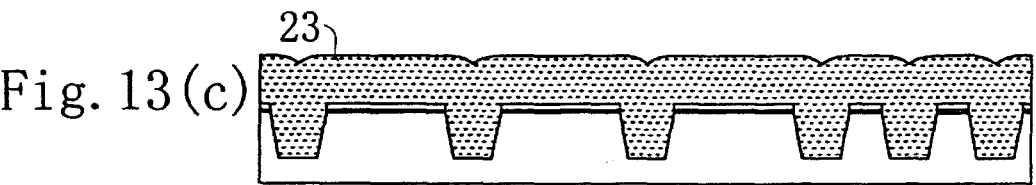
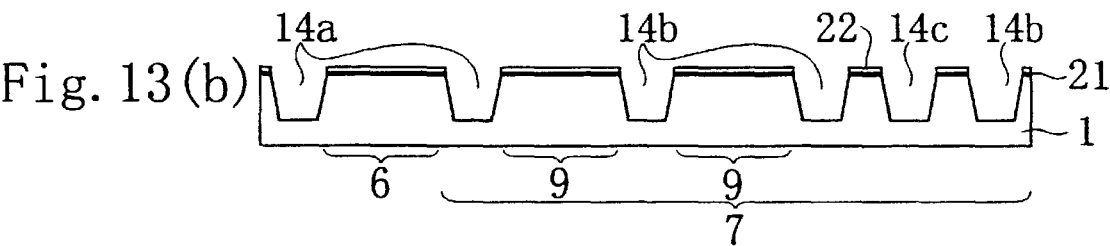
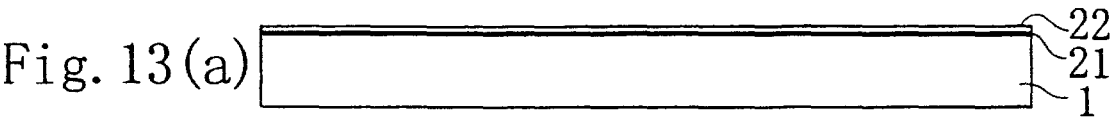


Fig. 14(a)

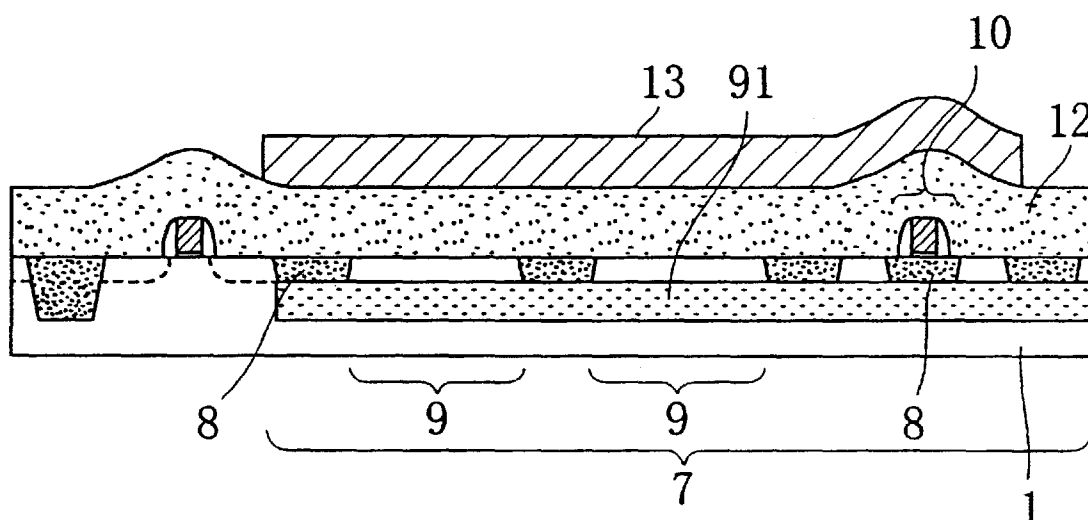
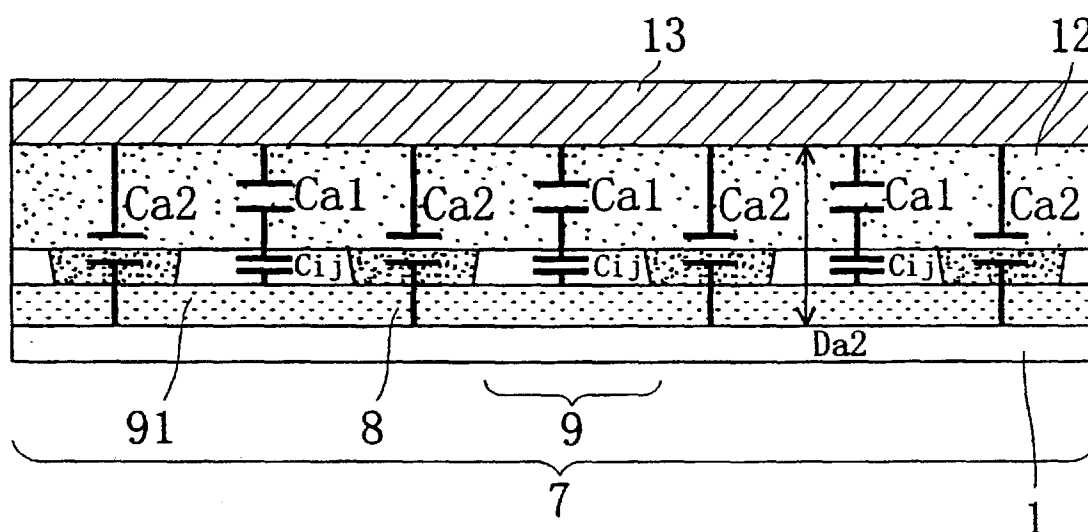
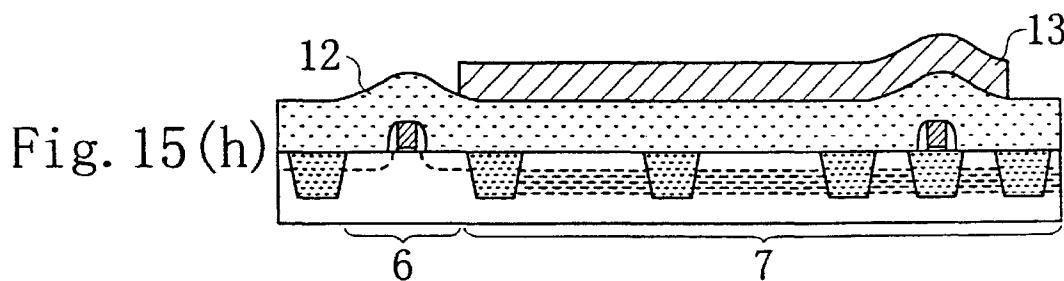
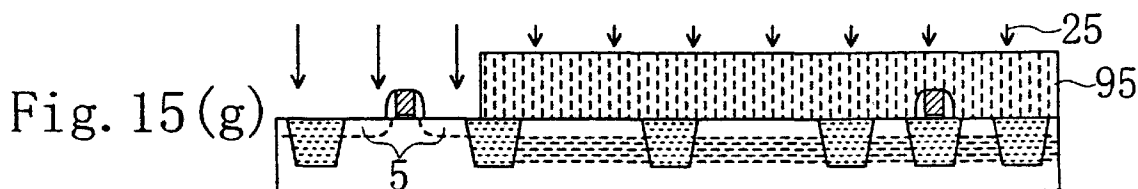
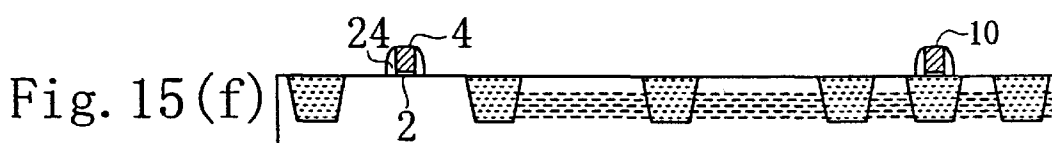
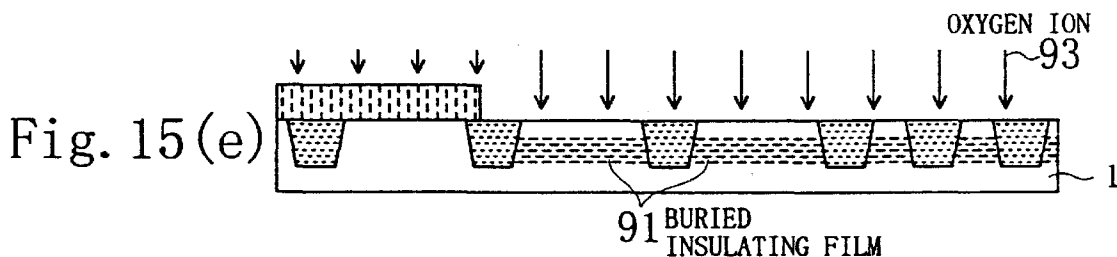
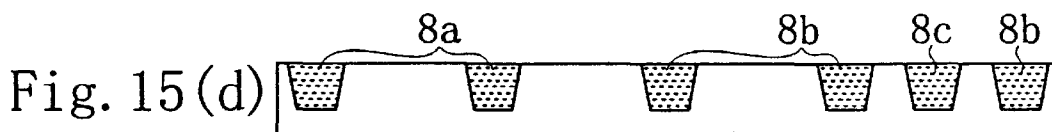
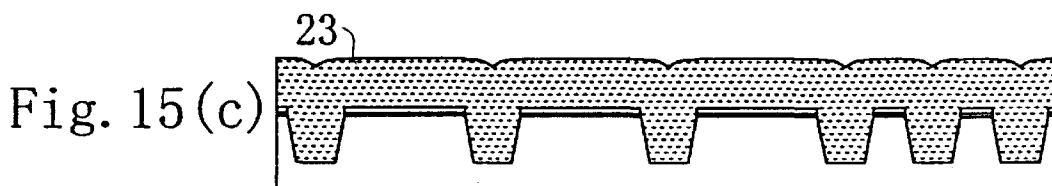
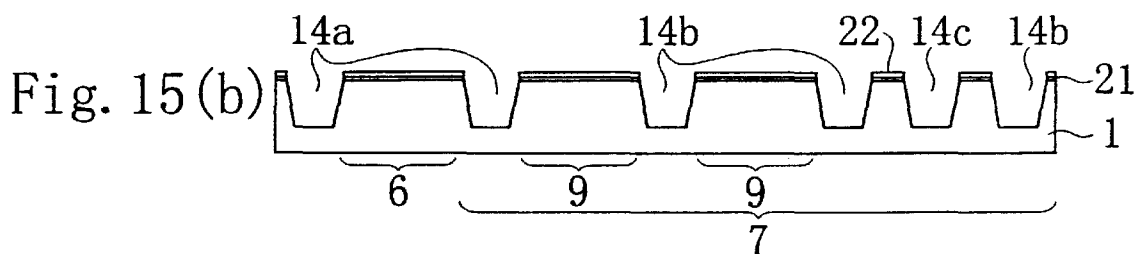
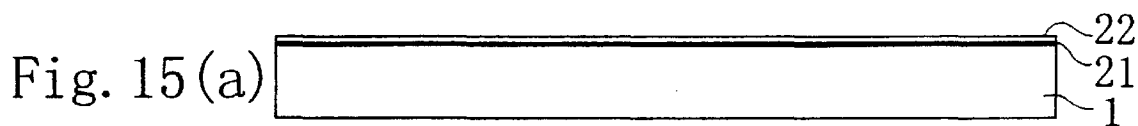
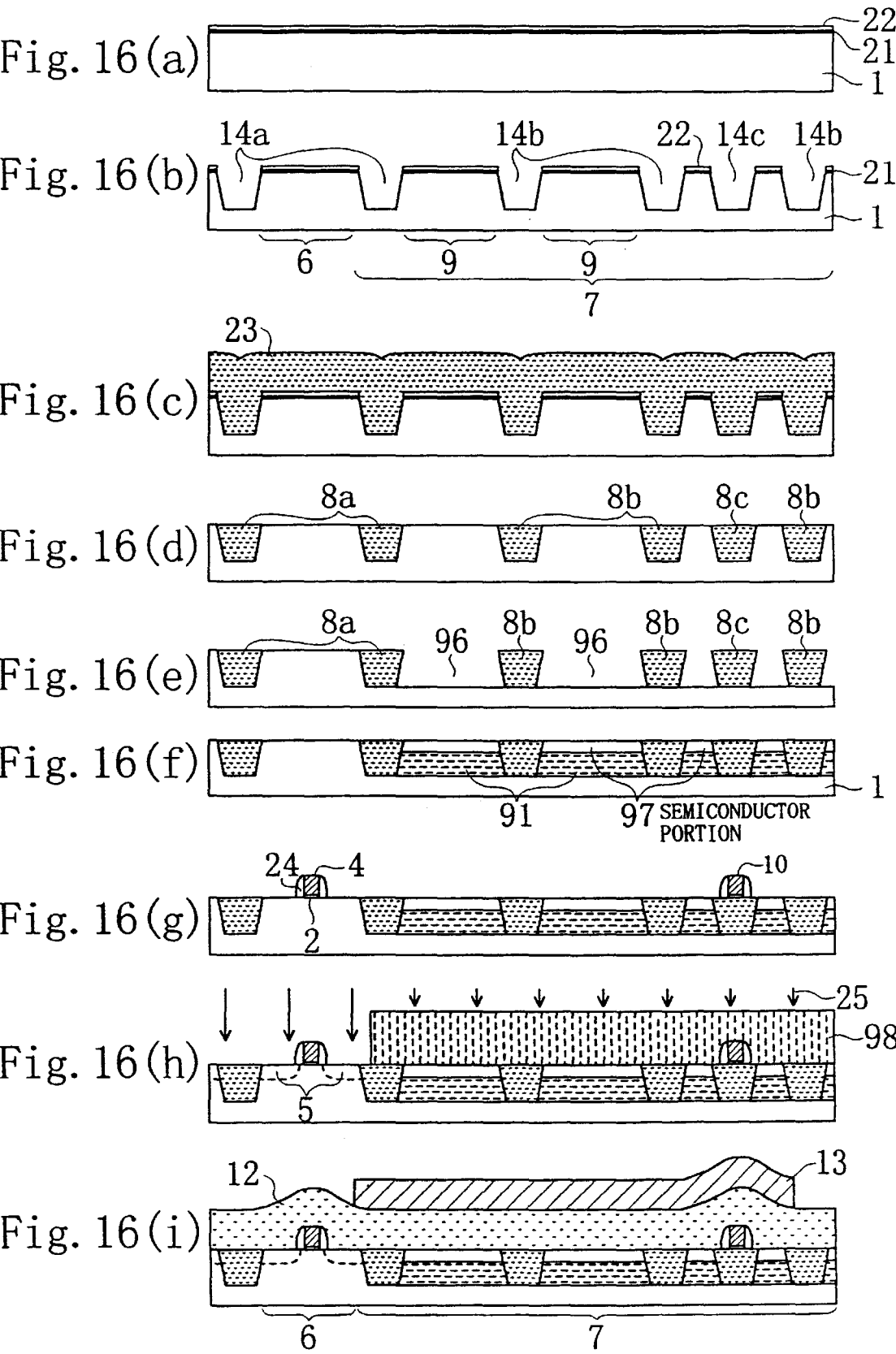
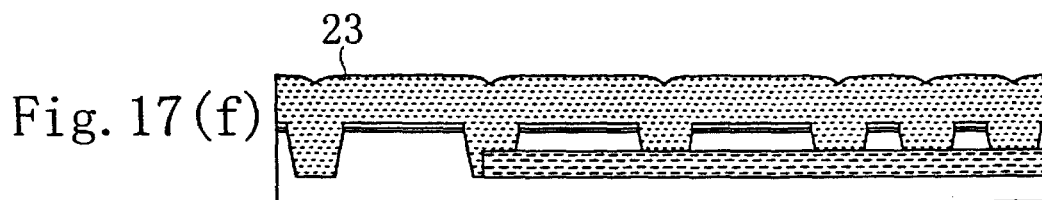
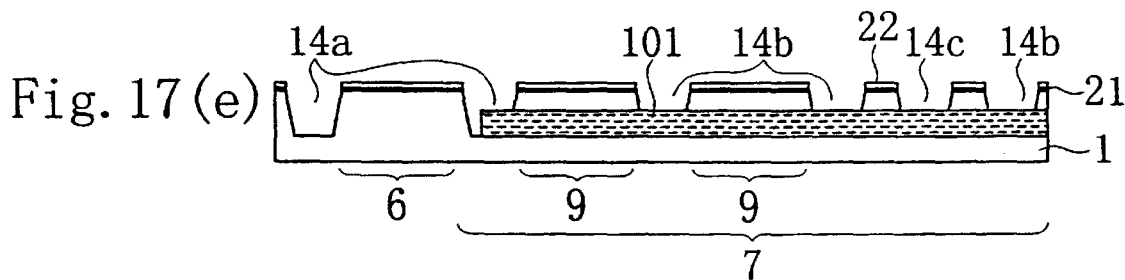
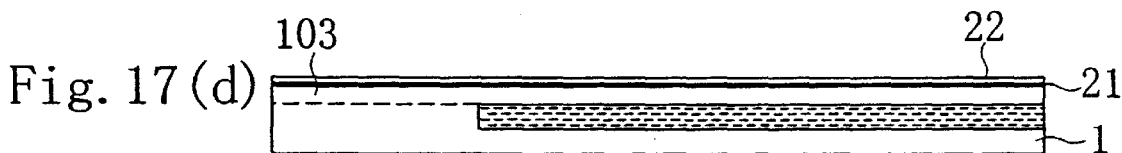
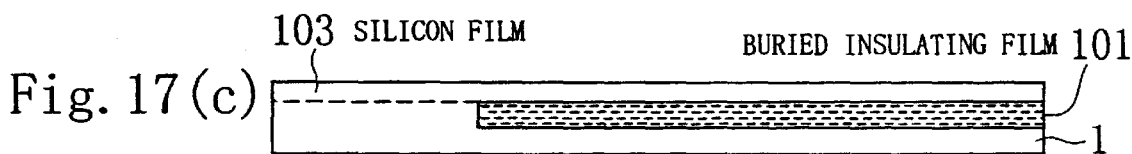


Fig. 14(b)









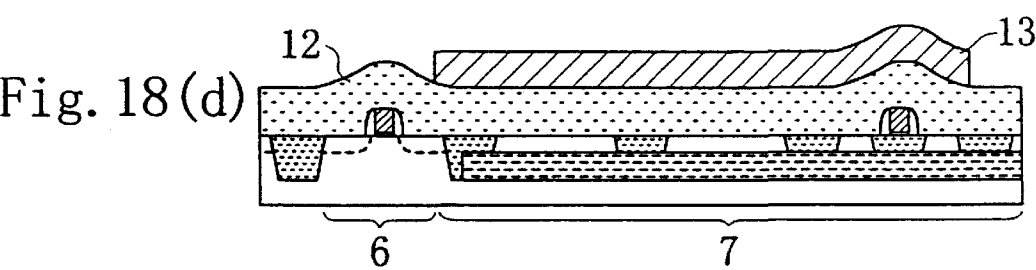
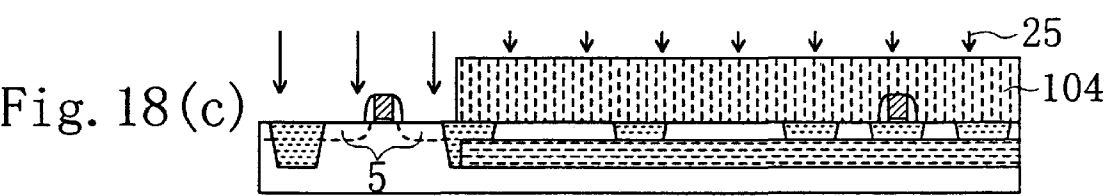
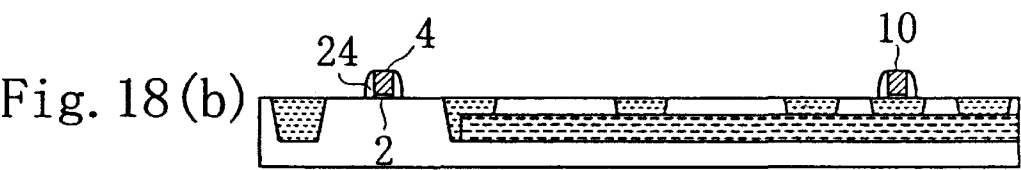
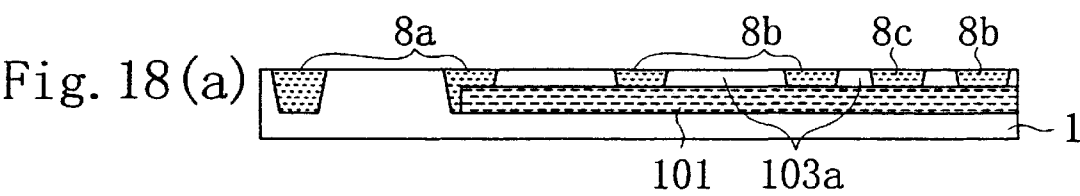
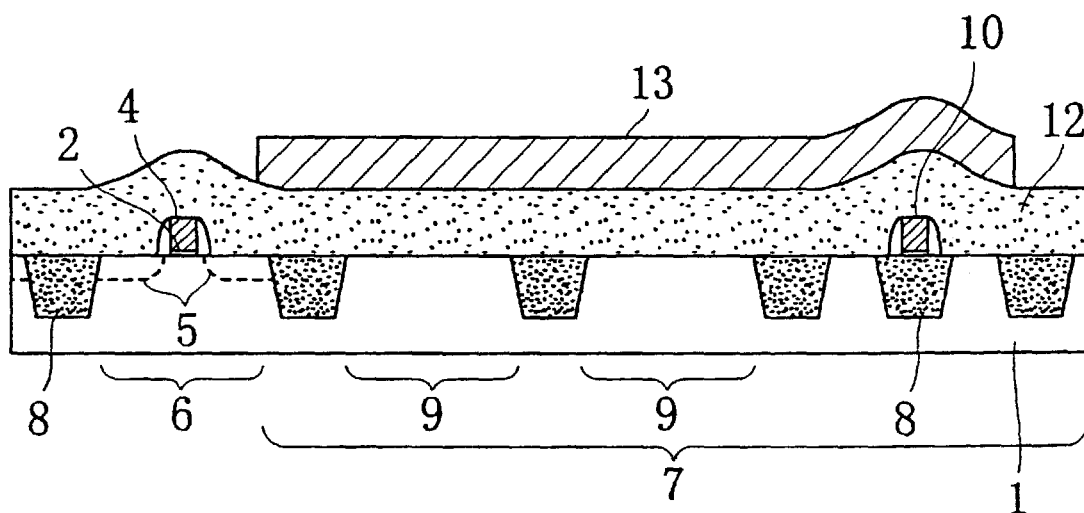


Fig. 19
PRIOR ART



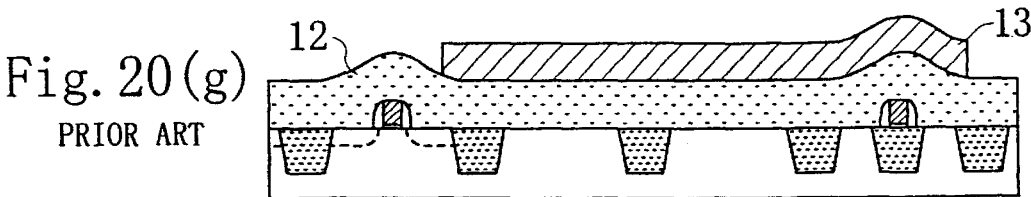
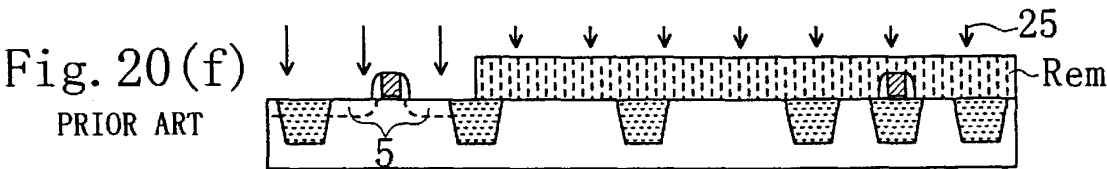
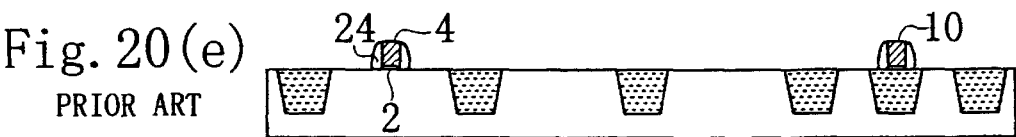
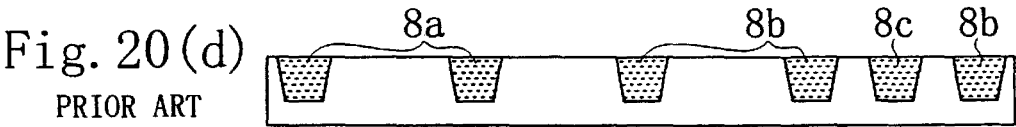
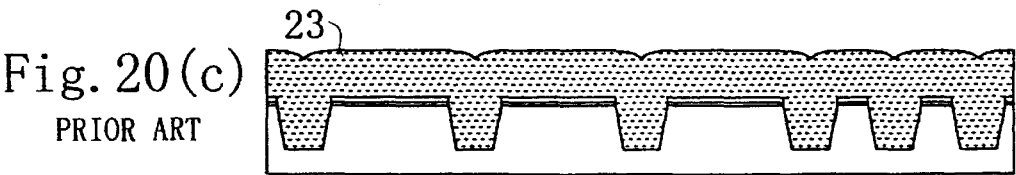
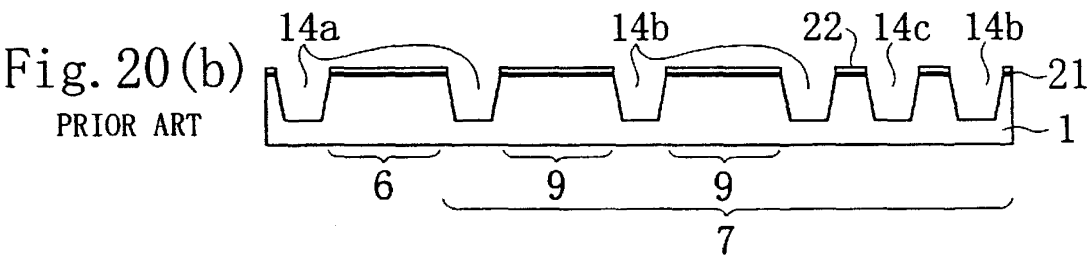
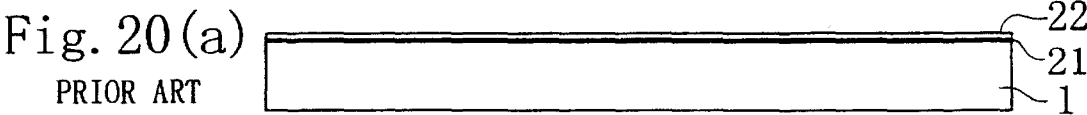


Fig. 21(a)
PRIOR ART

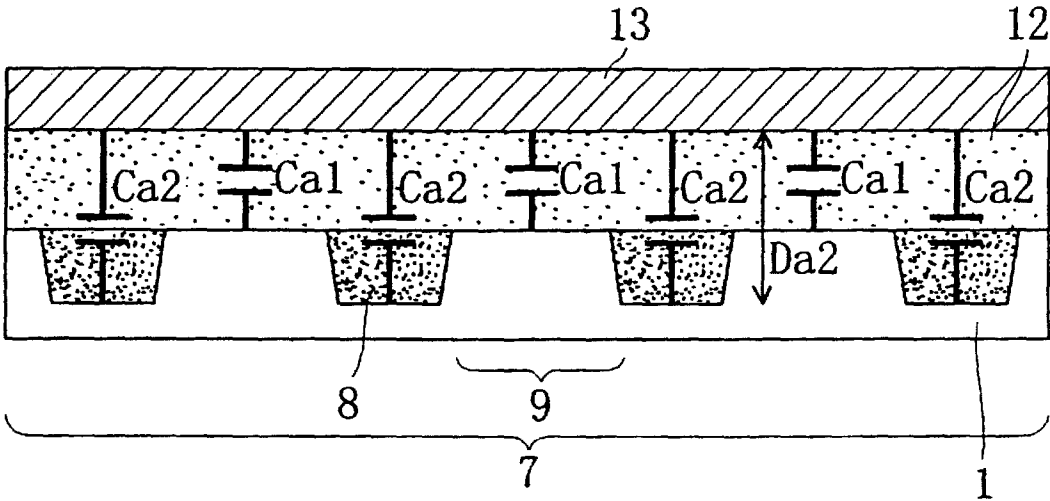
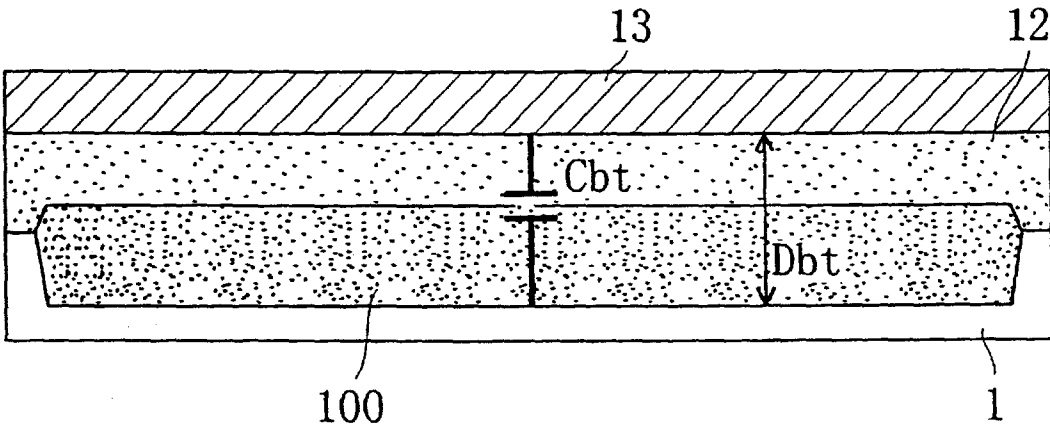


Fig. 21(b)
PRIOR ART



1

TRENCH ISOLATED SEMICONDUCTOR DEVICE

This is a divisional application of Ser. No. 08/978,137, Nov. 25, 1997 now U.S. Pat. No. 6,130,139.

The present invention relates to a semiconductor device having a trench-isolated structure and, more particularly, to a method of reducing the capacitance between the wiring and substrate of the semiconductor device.

As higher-density and increasingly miniaturized semiconductor devices have been implemented in recent years, repeated attempts have been made to substitute a trench isolation technique for a LOCOS technique which is most prevalently used to form isolation for providing insulation between individual elements of the semiconductor devices. In accordance with the trench isolation technique, an insulating material is filled in a trench formed in a semiconductor substrate to form isolation.

Since planarization of a surface of a semiconductor substrate including the insulating material filled in the trench is important to the trench isolation technique, chemical mechanical polishing (CMP) has been used as a planarizing technique which achieves excellent in-plane uniformity free from pattern dependence. In the case where the trench occupies a large area in a CMP process for planarization, the provision of dummy island semiconductor portions has been proposed to avoid trouble resulting from so-called pattern dependence, which causes polishing properties to vary depending on the area of a region to be planarized. In other words, the trench is divided into a plurality of narrow trenches so that the surface of the semiconductor substrate is exposed between the individual trenches to form the dummy semiconductor portions which do not serve as active regions.

FIG. 19 shows an example of the conventional trench-isolated semiconductor device having the dummy island semiconductor portions.

As shown in FIG. 19, an active region 6 of a P-type silicon substrate 1 is formed with: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5 into which an impurity has been introduced. An isolation region 7 surrounding the active region 6 is formed with a plurality of trench portions 8 each filled with a silicon oxide film. Between the individual trench portions 8, there are provided semiconductor portions 9 having top surfaces at the same level as the top surfaces of the trench portions 8. On the trench portions 8 also, there is provided a polysilicon wire 10 formed simultaneously with the gate oxide film 2 and the gate electrode 4 of an element. An interlayer insulating film 12 is deposited over the entire surface of the substrate, followed by a metal wire 13 provided thereon.

In this case, if the trench portions have such large widths as shown in FIG. 21(b), a silicon oxide film filled in each of the trench portions is polished during the CMP process for planarizing the whole substrate so that the surface thereof is depressed due to pattern dependence, which leads to the trouble of degraded planarity or the like. The isolation structure as shown in FIG. 19 has been proposed to prevent such trouble resulting from pattern dependence.

FIGS. 20(a) to 20(g) are cross-sectional views illustrating a process of manufacturing the conventional trench-isolated semiconductor device having an NMOS transistor.

In the step shown in FIG. 20(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 20(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate

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1. However, the trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions.

In the step shown in FIG. 20(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 20(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wires and the silicon substrate.

In the step shown in FIG. 20(e), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 and the polysilicon wire 10 are formed simultaneously.

In the step shown in FIG. 20(f), arsenic ions 25 are implanted into the active region 6 of the NMOSFET region by using a resist mask Rem covering the PMOSFET region and the isolation region to form the source/drain regions 5. The NMOSFET is formed by the foregoing process steps.

In the step shown in FIG. 20(g), the silicon oxide film is deposited to form the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

In the foregoing step shown in FIG. 20(f), ions of such an impurity as phosphorus or arsenic have been implanted into the gate electrode 4 and source/drain regions 5 of the active region 6 in the step shown in FIG. 20(f). However, impurity ions are not implanted in principle in the region other than the active region 6, though they may be introduced slightly extensively into the periphery of the isolation region in considerations of mask displacement. Hence, impurity ions are not implanted in the dummy semiconductor portions 9 between the individual trench portions 8.

A description will be given to the wiring-to-substrate capacitance of the trench-isolated semiconductor device having the small trench portions 8 which are discretely located and the dummy semiconductor portions 9 as shown in FIG. 19 and in a semiconductor device having a wide isolating/insulating film such as a LOCOS film. FIG. 21(a) is a cross-sectional view for illustrating, by way of example, the wiring-to-substrate capacitance in the isolation region 7 having the dummy semiconductor portions 9. FIG. 21(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance of the semiconductor device having a LOCOS isolation film 100 and no dummy semiconductor portion. It is assumed here that impurity ions have not been implanted in the isolation region 7 during the implantation of ions into the source/drain regions and that the area occupied by the whole isolation region 7 is equal in each of the two semiconductor devices.

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In the semiconductor device shown in FIG. 21(a), a total wiring-to-substrate capacitance C_{at} corresponds to the sum of capacitances $Ca1$ and $Ca2$, which is represented by the following equation (1):

$$C_{at} = \Sigma Ca1 + \Sigma Ca2 \quad (1).$$

In the case where a member interposed between the wiring and substrate is composed of a homogeneous material, the wiring-to-substrate capacitance per unit area is inversely proportional to the distance between the wiring and substrate, so that the capacitance is larger as the distance is shorter. If the total wiring-to-substrate of the semiconductor device shown in FIG. 21(b) is represented by C_{bt} when the dimension $Da2$ shown in FIG. 21(a) is equal to the dimension Dbt shown in FIG. 21(b), the following inequality (2) is satisfied:

$$C_{at} > C_{bt} \quad (2),$$

which indicates that the wiring-to-substrate capacitance C_{at} in the structure shown in FIG. 21(a) is larger than the wiring-to-substrate capacitance C_{bt} in the structure shown in FIG. 21(b).

Although the formation of the island pattern composed of the dummy semiconductor portions in the isolation region has the advantage of achieving planarization with excellent in-plane uniformity, it also has the possibility of increasing the wiring-to-substrate capacitance and resultantly reducing the operating speed of the semiconductor device.

SUMMARY OF THE INVENTION

In view of the foregoing, the present invention has been achieved based on the principle that, if each electrode of a parallel-plate capacitor occupies an equal area, the capacitance of the capacitor is generally smaller as the distance between the electrodes is larger or on the physical phenomenon that, even when the capacitor has equal capacitance, the amount of charge accumulated therein is smaller as the voltage between the electrodes is lower.

It is therefore an object of the present invention to increase the operating speed of a trench-isolated semiconductor device comprising an isolation region consisting of trench portions and dummy semiconductor portions by providing therein means for reducing the wiring-to-substrate capacitance in the isolation region or means for reducing the amount of charge accumulated in the capacitance present between the wiring and substrate in the isolation region.

A first semiconductor device according to the present invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; and at least one PN junction formed in the semiconductor portions underlying the wire.

In the arrangement, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the upper portion of the PN junction of each of the semiconductor portions to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. Accordingly, the wiring-to-substrate capacitance of the

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whole semiconductor device is reduced, resulting in the semiconductor device operating at a higher speed.

The PN junction may include a plurality of PN junctions formed in the semiconductor portions.

The arrangement achieves a further reduction in wiring-to-substrate capacitance, resulting in a higher operating speed.

The active region may be formed with an impurity diffusion region and a PN junction may be formed at a bottom face of the impurity diffusion region, the PN junction of the isolation region being positioned at a level lower than the PN junction of the active region.

The arrangement further reduces the wiring-to-substrate capacitance.

A second semiconductor device according to the present invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; and a dielectric film interposed between at least the semiconductor portions of the isolation region and the interlayer insulating film.

In the arrangement, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the dielectric film to the capacitance in the interlayer insulating film, so that the total wiring-to-substrate capacitance is lowered. Consequently, the operating speed of the semiconductor device is increased.

As the dielectric film, an underlying insulating film may be provided between the interlayer insulating film and the semiconductor portions and trench portions.

There can be further provided a gate electrode formed on the semiconductor substrate within the active region and sidewalls made of an insulating material and formed on both side faces of the gate electrode such that the underlying insulating film is formed of the same film as forming the sidewalls.

The underlying insulating film may be composed of a multilayer film.

The arrangement enables the underlying insulating film for reducing the wiring-to-substrate capacitance to be composed by using the sidewalls required to form a MOSFET of so-called LDD structure. Consequently, the wiring-to-substrate capacitance can be reduced, while avoiding an increase in manufacturing cost.

The dielectric film may be formed in an upper portion of each of the semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top face of each of the trench portions.

Preferably, the dielectric film is composed of at least one of a silicon oxide film and a silicon nitride film.

A third semiconductor device according to the present invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the

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isolation region; a wire formed on the interlayer insulating film; and a buried insulating film formed in an inner portion of each of the semiconductor portions in the isolation region.

The arrangement allows a reduction in the wiring-to-substrate capacitance of the entire isolation region, resulting in a significant reduction in operating speed.

A fourth semiconductor device according to the present invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; and a resistor film formed between the interlayer insulating film and at least the semiconductor portions of the isolation region.

In the arrangement, a voltage drop in the resistor film reduces the amount of charge accumulated in the wiring-to-substrate capacitance in the region of the semiconductor device containing the resistor film, though the wiring-to-substrate capacitance is not reduced in the region. Consequently, the time required for charging or discharging is reduced, resulting in the semiconductor device operating at a higher speed.

As the resistor film, an underlying resistor film may be formed to extend continuously over the semiconductor portions and trench portions.

The arrangement allows the wiring-to-substrate capacitance to be reduced by using various films having electric resistivity which are formed on the semiconductor substrate.

There can further be provided a resistor element formed on the semiconductor substrate and having a high resistor film such that the underlying resistor film is formed of the same film as composing the high resistor film of the resistor element.

In the arrangement, the underlying resistor film having the same resistance as the high resistor film used as a resistor element achieves a remarkable voltage dropping effect.

There can further be provided an element having an electrode member composed of a conductor film formed on the semiconductor substrate within the active region such that the resistor film is composed of the same material as composing the electrode member.

There can further be provided a FET having a gate electrode composed of a first conductor film formed on the semiconductor portion within the active region and a second conductor film deposited on the first conductor film such that a top surface of the first conductor film of the gate electrode is at approximately the same level as a top surface of each of the trench portions, while a region of the resistor film overlying each of the semiconductor portions is formed of the same two films as composing the first and second conductor films of the gate electrode and a region of the resistor film overlying each of the trench portions is composed of the same material as composing the first conductor film of the gate electrode.

Each of the arrangements eliminates the necessity for an additional step of forming the resistor film, so that the wiring-to-substrate capacitance is reduced, while an increase in manufacturing cost is prevented.

The resistor film may be formed in an upper portion of each of the semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top surface of each of the trench portions.

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The resistor film may be composed of a silicon film containing at least one of an oxygen atom and a nitrogen atom.

The resistor film may be composed of at least one of a polysilicon film and an amorphous silicon film.

The arrangement allows the formation of the resistor film by using the polysilicon film or amorphous silicon film to compose the gate electrode and the resistor element and thereby prevents an increase in manufacturing cost.

A first method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region of a first conductivity type, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of introducing an impurity containing at least an impurity of a second conductivity type into the dummy semiconductor portions of the isolation region to form at least one PN junction in the dummy semiconductor portions; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

The method enables the formation of the semiconductor device including the dummy semiconductor portions each having the PN junction. The capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the upper portion of the PN junction of each of the semiconductor portions to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. Accordingly, the wiring-to-substrate capacitance of the whole semiconductor device is reduced, resulting in the semiconductor device operating at a higher speed.

The third and fourth steps may include forming a gate electrode of a FET as the element on the active region, introducing the impurity of the second conductivity type into the active region and the dummy semiconductor portions, and thereby forming source/drain regions of the FET, while forming the at least one PN junction in the dummy semiconductor portions.

The method enables the formation of the semiconductor device operating at a high speed by using a typical manufacturing process for forming a FET without an additional step of forming the PN junction in each of the dummy semiconductor portions.

The third step may include forming a gate electrode of a FET as the element on the active region by using a first mask covering the isolation region and introducing the impurity of the second conductivity type into the active region to form source/drain regions of the FET and the fourth step may include introducing the impurity containing at least the impurity of the second conductivity type into the dummy semiconductor portions by using a second mask covering the active region to form the at least one PN junction in the dummy semiconductor portions.

The method enables the formation of the semiconductor device having an arbitrary number of PN junctions without placing restraints on the depth and impurity concentration of the PN junction in the active region, resulting in a semiconductor device having minimum wiring-to-substrate capacitance.

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A second method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming a resistor film on each of the dummy semiconductor portions of the isolation region; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

The method enables the formation of the semiconductor device comprising the resistor film between the interlayer insulating film and dummy semiconductor portions of the isolation region. A voltage drop in the resistor film reduces the amount of charge accumulated in the wiring-to-substrate capacitance, though the wiring-to-substrate capacitance is not reduced in the region containing the resistor film of the semiconductor device. Consequently, the time required for charging or discharging is reduced, resulting in the semiconductor device operating at a higher speed.

The fourth step may include composing the resistor film of a film containing at least one of polysilicon and amorphous silicon.

The fourth step may include composing the resistor film of a multilayer film constituted by two or more conductor films with at least an insulating film interposed therebetween.

The fourth step may include introducing an impurity at a concentration of 1×10^{20} atoms·cm⁻³ or lower into the resistor film.

A third method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of implanting ions into an upper portion of each of the dummy semiconductor portions to form a high resistor portion therein; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

The method allows the formation of the semiconductor device comprising the high resistor portion between the interlayer insulating film and dummy semiconductor portions of the isolation region. As described above, a voltage drop in the region containing the high resistor portion of the semiconductor device reduces the amount of charge accumulated in the wiring-to-substrate capacitance. What results is the semiconductor device which requires a shorter time for charging or discharging and therefore operates insulating film at a higher speed.

The fourth step may include implanting ions containing at least an atom having an oxidizing function to form the high resistor portion.

The fourth step may include implanting ions containing at least an atom having a nitriding function to form the high resistor portion.

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A fourth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming an underlying insulating film over the dummy semiconductor portions of the isolation region; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

In accordance with the method, there is formed the semiconductor device including the underlying insulating film beneath the interlayer insulating film in the isolation region thereof. Consequently, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the underlying insulating film to the capacitance in the interlayer insulating film, so that the total wiring-to-substrate capacitance is reduced. What results is the semiconductor device operating at a high speed.

The third step and the fourth step may include forming a gate electrode of a FET forming the element on the active region, depositing a dielectric film on the substrate, performing anisotropic etching with respect to the dielectric film by using a mask covering the isolation region, and thereby leaving sidewalls on both side faces of the gate electrode, while leaving the underlying insulating film over the dummy semiconductor portions.

The method enables the formation of a semiconductor device operating at a high speed by using a typical manufacturing process for forming a FET without an additional step of forming the underlying insulating film.

The fourth step may include forming the underlying insulating film of a dielectric film containing at least silicon oxide.

The fourth step may include forming the underlying insulating film of a dielectric film containing at least silicon nitride.

A fifth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming depressed portions by etching the dummy semiconductor portions and filling an insulating material in the depressed portions to form inter-trench insulating films each having a top face at the same level as respective top faces of the first and second buried trench portions; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

In accordance with the method, there is formed the semiconductor device comprising the inter-trench insulating films between the interlayer insulating films and dummy semiconductor portions of the isolation region thereof.

Consequently, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the inter-trench buried insulating films to the capacitance in the interlayer insulating film, so that the total wiring-to-substrate capacitance is reduced. What results is the semiconductor device operating at a high speed.

The fourth step may include forming each of the inter-trench insulating films of a dielectric film containing at least silicon oxide.

The fourth step may include forming each of the inter-trench insulating films of a dielectric film containing at least silicon nitride.

A sixth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of implanting oxygen ions into each of the dummy semiconductor portions to form a buried insulating film in an inner portion thereof; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

A seventh method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming third trenches by etching the semiconductor portions and filling an insulating material in the third trenches to form buried insulating films each having a top face at a level lower than respective top faces of the first and second buried trench portions; a fourth step of growing semiconductor films on the buried insulating films, with the active region covered with a mask member, to form dummy semiconductor portions; a sixth step of forming an interlayer insulating film over an entire surface of the substrate; a fifth step of forming an element on the active region; a seventh step of forming a wire on the interlayer insulating film.

An eighth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench extending over an entire isolation region of the substrate region, while leaving an active region of the substrate region; a second step of filling an insulating material in the first trench to form a buried insulating film having a top face at the same level as a top face of the isolation region; a third step of growing a semiconductor film over the active region and the buried insulating film; a fourth step of forming, in the semiconductor substrate, a second trench for partitioning the semiconductor film and the substrate region into the active region and the isolation region and a third trench for partitioning the portion of the semiconductor film overlying the isolation

region into a plurality of dummy semiconductor portions; a fifth step of filling an insulating material in each of the second and third trenches to form a first buried trench portion and a second buried trench portion; a sixth step of forming an element on the portion of the semiconductor film overlying the active region; a seventh step of forming an interlayer insulating film over an entire surface of the substrate; and an eighth step of forming a wire on the interlayer insulating film.

In accordance with the methods, there are obtained semiconductor devices each comprising a buried insulating film at a depth of each of the dummy semiconductor portions of the isolation region. What results is the semiconductor device having smaller wiring-to-substrate capacitance and operating at a higher speed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(a) is a cross-sectional view of a semiconductor device according to a first embodiment, having shallow PN junctions formed in the semiconductor portions thereof and

FIG. 1(b) is an enlarged cross-sectional view of an isolation region for illustrating the wiring-to-substrate capacitance in the semiconductor device;

FIGS. 2(a) to 2(g) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to the first embodiment;

FIG. 3 is a cross-sectional view of a semiconductor device according to a second embodiment, having shallow PN junctions formed in the semiconductor portions thereof;

FIG. 4 is a cross-sectional view of a semiconductor device according to a third embodiment, having two PN junctions in the semiconductor portions thereof;

FIG. 5 is a cross-sectional view of a semiconductor device according to a fourth embodiment, having a high resistor film formed on the semiconductor portions thereof;

FIGS. 6(a) to 6(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a fourth embodiment;

FIG. 7 is a cross-sectional view of a semiconductor device according to a fifth embodiment, having a multilayer gate provided therein;

FIG. 8 is a cross-sectional view of a semiconductor device according to an eighth embodiment, having an inter-trench film formed on each of the semiconductor portions thereof;

FIGS. 9(a) to 9(i) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to the sixth embodiment;

FIG. 10 is a cross-sectional view of a semiconductor device according to a seventh embodiment, having a high resistor portion in the upper portion of each of the semiconductor portions;

FIGS. 11(a) to 11(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a seventh embodiment;

FIG. 12 is a cross-sectional view of a semiconductor device according to an eighth embodiment, having an underlying, having an underlying insulating film formed beneath an interlayer insulating film;

FIGS. 13(a) to 13(i) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to the eighth embodiment;

FIG. 14(a) is a cross-sectional view of a semiconductor device according to a ninth embodiment, having a buried insulating film formed over the entire isolation region and

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FIG. 14(b) is an enlarged cross-sectional view of the isolation region for illustrating the wiring-to-substrate capacitance in the semiconductor device;

FIGS. 15(a) to 15(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to the ninth embodiment;

FIGS. 16(a) to 16(i) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a tenth embodiment;

FIGS. 17(a) to 17(f) are cross-sectional views illustrating the first half of a process of manufacturing a semiconductor device according to an eleventh embodiment;

FIGS. 18(a) to 18(d) are cross-sectional views illustrating the second half of the process of manufacturing the semiconductor device according to the eleventh embodiment;

FIG. 19 is a cross-sectional view of a conventional semiconductor device;

FIGS. 20(a) to 20(g) are cross-sectional views illustrating a process of manufacturing the conventional semiconductor device; and

FIG. 21 is a cross-sectional view for illustrating the wiring-to-substrate capacitance in each of a conventional trench-isolated semiconductor device and a conventional LOCOS-isolated semiconductor device.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to the drawings, the embodiments of the present invention will be described.
(First Embodiment)

FIG. 1(a) is a cross-sectional view of a semiconductor device having a MOSFET according to a first embodiment. As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as the MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Each of the semiconductor portions 9 formed in the isolation region 7 is provided with an impurity diffusion layer 21 into which an N-type impurity of the conductivity type opposite to that of the silicon substrate 1 has been introduced, so that a PN junction 22 is formed between the impurity diffusion layer 21 and the silicon substrate 1. The PN junction 22 is positioned at a level between those of the top and bottom faces of the trench portions 8.

FIG. 1(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance in the isolation region 7 of the semiconductor device according to the present embodiment. As shown in the drawing, the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment includes the components of capacitances Ca1 and Ca2, similarly to the wiring-to-substrate capacitance of the conventional semiconductor device shown in FIG. 21(a). Moreover, since the PN junction 22 is

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formed in each of the semiconductor portions 9, another capacitance Cj1 is added in series to the capacitance Ca1. Hence, the total wiring-to-substrate capacitance Cjt is represented by the following equation (3):

$$C_{jt} = \Sigma \{ (Ca1 \times Cj1) / (Ca1 + Cj1) \} + \Sigma Ca2 \tag{3}$$

which is smaller than the total capacitance Cat represented by the equation (1). Accordingly, the following inequality (4) is satisfied (4):

$$C_{jt} < Cat \tag{4}$$

Thus, the wiring-to-substrate capacitance can be reduced in the semiconductor device according to the present embodiment owing to the PN junction 22 present in each of the dummy semiconductor portions 9 of the isolation region 7, which increases the operating speed of the semiconductor device.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 2(a) to 2(g) are cross-sectional views showing the structure of the semiconductor device having the NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 2(a), the thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 2(b), the plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active 6 region by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 2(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 2(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wires and the silicon substrate.

In the step shown in FIG. 2(e), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wires 10 by using a known technique. The gate electrode 4 and the polysilicon wires 10 can be formed simultaneously by using a common mask.

In the step shown in FIG. 2(f), arsenic ions 25 are implanted not only into the active region 6 but also into the entire isolation region 7. As a result, the NMOSFET having the source/drain regions 5 is formed in the active region 6. On the other hand, an N-type impurity diffusion layer 31 is

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formed in each of the dummy semiconductor portions 6 of the isolation region 7, resulting in a PN junction 32 formed between the N-type impurity diffusion layer 31 and the P-type silicon substrate 1. The present embodiment is characterized in that the PN junction 32 is positioned between the top and bottom faces of the buried trench portions 8.

In the step shown in FIG. 2(g), the silicon oxide film is deposited to form the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

In the case of providing the MOSFET in the active region as provided in accordance with the manufacturing method of the present embodiment, the PN junction 22 in each of the semiconductor portions 9 can be formed easily through the implantation of ions for forming the source/drain regions 5, so that manufacturing cost is not increased.

Although the present embodiment has described the case of using the P-type silicon substrate, it will be appreciated that the same effects as achieved in the present embodiment are also achieved in the case of using an N-type silicon substrate by introducing a P-type impurity into the upper portions of the semiconductor portions located between the individual trench portions and thereby forming the PN junctions between the resulting P-type impurity diffusion layers and the N-type silicon substrate.

Although the formation of the PN junctions 32 in the dummy semiconductor portions 9 of the isolation region 7 has been performed simultaneously with the formation of the source/drain regions 5 in the manufacturing method of the present embodiment, the formation of the dummy semiconductor portions 9 may be preformed at any stage of the process of manufacturing the semiconductor device, provided that the PN junctions can be formed in the dummy semiconductor portions.

(Second Embodiment)

FIG. 3 is a cross-sectional view of a semiconductor device according to a second embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET-composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Each of the semiconductor portions 9 formed in the isolation region 7 is provided with an impurity diffusion layer 31 in to which an N-type impurity of the conductivity type opposite to that of the impurity introduced into the silicon substrate 1 has been introduced, so that a PN junction 32 is formed between the impurity diffusion layer 31 and the silicon substrate 1. The PN junction 32 is positioned at a level lower than the bottom faces of the trench portions 8.

The wiring-to-substrate capacitance in the isolation region 7 of the present embodiment is represented by the following equation (5):

$$C_{jt} = \sum \{ (C_{a1} \times C_{j1}) / (C_{a1} + C_{j1}) \} + \sum \{ (C_{a2} \times C_{k1}) / (C_{a2} + C_{k1}) \} \quad (5),$$

which is smaller than the total capacitance Cat represented by the equation (1). In the foregoing equation (5), Ck1

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represents the capacitance between the bottom face of the trench portion 8 and the PN junction 32. Hence, the following inequality (6) is satisfied, similarly to the first embodiment:

$$C_{jt} < C_{at} \quad (6).$$

Thus, the wiring-to-substrate capacitance can also be reduced in the semiconductor device according to the present embodiment since the PN junction 32 is present in each of the dummy semiconductor portions 9 of the isolation region 7, similarly to the first embodiment, so that the operating speed of the semiconductor device is increased. In particular, the present embodiment can reduce the wiring-to-substrate capacitance in the entire isolation region containing not only the semiconductor portions 9 but also the trench portions, so that the effect of increasing the operating speed is remarkable.

Although it is difficult to form the PN junction 32 as formed in the present embodiment through the implantation of impurity ions for forming the source/drain regions of the MOSFET, the impurity concentration and the depth of ionic penetration into the substrate can be controlled arbitrarily, so that a higher effect of reducing the capacitance is achieved. In particular, since the PN junction 32 is positioned at a level lower than the bottom faces of the trench portions 8, a higher effect of reducing the capacitance is achieved.

Although the present embodiment has described the case of using the P-type silicon substrate, an N-type silicon substrate may also be used instead. In this case, a PN junction can be formed by introducing a P-type impurity into the semiconductor portions and thereby forming an impurity diffusion layer, so that the same effects as achieved in the present embodiment are achieved.

(Third Embodiment)

FIG. 4 is a cross-sectional view of a semiconductor device according to a third embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Each of the dummy semiconductor portions 9 formed in the isolation region 7 is provided with a P-type impurity diffusion layer 41 and an N-type impurity diffusion layer 42, which are arranged in this order from the surface of the silicon substrate. As a result, a first PN junction 43 is formed between the P-type impurity diffusion layer 41 and the N-type impurity diffusion layer 42, while a second PN junction 44 is formed between the N-type impurity diffusion layer 42 and the P-type silicon substrate 1. The first and second PN junctions 43 and 44 are positioned at levels between the top and bottom faces of the trench portions 8.

If respective junction capacitances in the P-type and N-type impurity diffusion layers 41 and 42 are designated as Cj1 and Cj2, a total wiring-to-substrate capacitance Cjt in

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the semiconductor device according to the present embodiment is represented by the following equation (7):

$$C_{jt} = \Sigma \{ 1 / [(1 / Ca1) + (1 / Cj1) + (1 / Cj2)] \} + \Sigma Ca2 \tag{7}$$

which is smaller than the total capacitance Cat of the semiconductor device according to the first embodiment represented by the equation (1). Hence, the following equation (8) is satisfied:

$$C_{jt} < Cat \tag{8}$$

Since the present embodiment has provided the plurality of PN junctions 43 and 44 in the respective dummy semiconductor portions of the isolation region 7, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions 9 of the semiconductor device can be represented by the capacitance obtained by connecting in series the respective capacitances in the P-type and N-type impurity diffusion layers 41 and 42 to the capacitance in the interlayer insulating film. Consequently, the wiring-to-substrate capacitance of the semiconductor device can further be reduced than in the first embodiment, resulting in the semiconductor device operating at a higher speed.

Although the present embodiment has described the case where the two PN junctions 43 and 44 are formed of the two impurity diffusion layers, if three or more PN junctions are formed of three or more impurity diffusion layers, the total wiring-to-substrate capacitance can be represented in the same fashion as represented by the equation (7). For example, if m PN junctions (m is an integer equal to or more than 3) are formed in each of the dummy active regions 9 and n PN junctions (n is an integer equal to or more than 3) are formed immediately under the trench portion 8, the total wiring-to-substrate capacitance Cjt is represented by the following equation (9):

$$C_{jt} = \Sigma \{ 1 / [(1 / Ca1) + \Sigma (1 / Cjm)] \} + \Sigma \{ 1 / [(1 / Ca2) + \Sigma (1 / Cjn)] \} \tag{9}$$

which is smaller than the total capacitance Cat represented by the equation (1). Hence, the following inequality (10) is satisfied:

$$C_{jt} < Cat \tag{10}$$

In the case of using the structure, the wiring-to-substrate capacitance can be reduced significantly since not only the capacitance component in the region containing the semiconductor portions of the isolation region 7 but also the capacitance component in the region containing the trench portions thereof is also reduced.
(Fourth Embodiment)

FIG. 5 is a cross-sectional view of a semiconductor device according to a fourth embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. In addition, a dummy

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gate 51 composed of a polysilicon film formed simultaneously with the gate electrode 4 extends continuously over the semiconductor portions 9 and trench portions 8. Over the dummy gate 51, the polysilicon wire 10, and a surface of the silicon substrate (except for the active region), a silicon oxide film 52 and a high resistor film 53 composed of a polysilicon film are further formed in layers. The dummy gate 51 has been formed by patterning a first-layer polysilicon film used commonly to form the gate electrode 4 and the polysilicon wire 10 so that it is at a given distance from each of the gate electrode 4 and the polysilicon wire 10. The polysilicon film composing the high resistor film 53 has a sheet resistance film higher than that of the first-layer polysilicon film composing the gate electrode 4 and the like and an impurity concentration of $1 \times 10^{20} \text{ cm}^{-3}$ or less. The sheet resistance of the dummy gate 51 can also be held high by covering the isolation region with a resist film or the like during the implantation of an impurity into the active region.

In the semiconductor device according to the present embodiment, it is sufficient to consider the capacitance between the wiring and high resistor film instead of the capacitance between the wiring and substrate. In this case, since the resistance of the polysilicon film composing the high resistor film 53 is high, a voltage drop occurs between the top face of the high resistor film 53 and the surface of the semiconductor substrate 1. Accordingly, the voltage applied to the top and bottom faces of the interlayer insulating film is reduced, though the capacitance of the interlayer insulating film 12 remains unchanged. Since the amount of charge accumulated in the top and bottom faces of the interlayer insulating film 12 decreases in direct proportion to the voltage applied thereto, the time required for charging or discharging between the wiring and high resistor is reduced, resulting in the semiconductor device operating at a higher speed.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 6(a) to 6(h) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 6(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 6(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 6(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 6(d), the silicon oxide film 23 is polished by a CMP process. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form a plurality of buried trench portions 8

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each filled with a silicon oxide film and having a planarized surface. The buried trench portions **8** include: buried trench portions **8a** functioning as isolation; buried trench portions **8b** forming the dummy semiconductor portions **9**; and buried trench portions **8c** for providing insulation between the polysilicon wires and the silicon substrate.

In the step shown in FIG. 6(e), there are formed the gate oxide film **2**, the gate electrode **4** having sidewalls **24** on the side faces thereof, and the polysilicon wires **10** by using a known technique. During the process, the dummy gate **51** is formed simultaneously with the gate electrode **4** and the polysilicon wire **10** and at a given distance from each of the gate electrode **4** and the polysilicon wire **10**, so that the dummy gate **51** neither cross nor contact the gate electrode **4** and the polysilicon wire **10**. The gate electrode **4**, the polysilicon wire **10**, and the dummy gate **51** can be formed simultaneously by using a common semiconductor mask. The dummy gate **51** has a sheet resistance higher than those of the gate electrode **4** and polysilicon wire **10**, which are used as interconnections, and has an impurity concentration adjusted to be 1×10^{20} atoms·cm⁻³ or lower by ion implantation or the like.

In the step shown in FIG. 6(f), the silicon oxide film **52** and the high resistor film **53** made of polysilicon are formed over the isolation region **7**. The high resistor film **53** has a sheet resistance higher than those of the gate electrode **4** and polysilicon wires **10** and has an impurity concentration adjusted to be 1×10^{20} atoms·cm⁻³ or lower by ion implantation or the like. The silicon oxide film **52** and the high resistor film **53** are formed to provide a MIM capacitor and a resistor.

In the step shown in FIG. 6(g), a resist mask **55** covering at least the isolation region **7** is formed and arsenic ions **25** are implanted into the active region **6** to form the NMOS having the source/drain regions **5**. During the process, arsenic ions are not implanted in the isolation region **7**.

In the step shown in FIG. 6(h), a silicon oxide film is deposited to form the interlayer insulating film **12**, followed by a metal wire **13** formed thereon.

In the semiconductor device according to the present embodiment, it is sufficient to consider the capacitance between the wiring and high resistor film instead of the capacitance between the wiring and substrate. In this case, since the resistance of the polysilicon film composing the high resistor film **53** is high, a voltage drop occurs between the top face of the high resistor film **53** and the surface of the semiconductor substrate **1**. Accordingly, the voltage applied to the top and bottom faces of the interlayer insulating film is reduced, though the capacitance of the interlayer insulating film **12** remains unchanged. Since the amount of charge accumulated in the top and bottom faces of the interlayer insulating film **12** decreases in direct proportion to the voltage applied thereto, the time required for charging or discharging between the wiring and high resistor is reduced, resulting in the semiconductor device operating at a higher speed.

The high-resistance film **53** according to the present embodiment can be formed easily at low cost by patterning the same film as composing, e.g., the high resistor film of the resistor element and local wiring. Instead of forming the dummy gate **51**, it is possible to form films corresponding to the high resistor film **53**, the silicon oxide film **52**, and the dummy gate **51** from three films composing the upper-layer film, capacitor insulating film, and lower-layer film composing the MIM capacitor formed anywhere on the semiconductor substrate.

It is also possible to increase the operating speed of the semiconductor device by reducing the time required for

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charging or discharging without forming either of the dummy gate **51** and the high resistor film **53** as well as the silicon oxide film **52**.

Although the description has been given to the case where the high resistor film **53** composed of the polysilicon film and the silicon oxide film **52** are stacked in layers on the isolation region **7**, similar effects can also be achieved in the case of using an amorphous silicon film or a silicon nitride film instead of the polysilicon film. In particular, the use of an insulating film composed of a silicon oxide film allows a reduction in total capacitance and a further increase in the operating speed of the semiconductor device.

(Fifth Embodiment)

FIG. 7 is a cross-sectional view of a semiconductor device according to a fifth embodiment.

As shown in the drawing, an active region **6** of a P-type silicon substrate **1** is provided with an element functioning as a MOSFET composed of: a gate oxide film **2**; a gate electrode **4**; and source/drain regions **5**. An isolation region **7** for electrically isolating the individual elements is formed with a plurality of trench portions **8** each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions **9** provided between the individual trench portions **8** and not serving as active regions. On one of the trench portions **8** formed in the isolation region **7**, there is provided a polysilicon wire **10** formed simultaneously with the gate electrode **4**.

In the present embodiment, the gate electrode **4** consists of a lower-layer portion **4a** made of a first conductor film composed of a polysilicon film or the like and an upper-layer portion **4b** made of a second conductor film composed of a tungsten film or the like. In the isolation region **7**, there is provided a dummy gate **51** consisting of a lower-layer portion **51a** composed of the same first conductor film as composing the lower-layer portion **4a** of the gate electrode **4** and an upper-layer portion **51b** composed of the same second conductor film composing the upper-layer portion **4b** of the gate electrode **4**. The lower-layer portion **51a** of the dummy gate **51** has a top surface at the same level as the top face of each of the trench portions **8**, so that planarization is achieved between the lower-layer portion **51a** and the trench portions **8**. The polysilicon wire **10** is composed only of the second conductor film composing the upper-layer portion **4b** of the gate electrode **4**. The dummy gate **51** has been formed at a given distance from each of the gate electrode **4** and polysilicon wire **10** so as to improve pattern accuracy in a photolithographic process in accordance with a line-and-space relationship. There are also provided an interlayer insulating film **12** composed of a silicon oxide film deposited over the entire surface of the substrate and a metal wire **13** formed on the interlayer insulating film **12**.

In accordance with a process of manufacturing the semiconductor device according to the present embodiment, the structure of the semiconductor device as shown in FIG. 7 can be implemented by the following procedure, though the drawing thereof is omitted here.

First, the gate insulating film and the first conductor film composed of a polysilicon film or the like are deposited on the semiconductor substrate, which are partially opened to form trenches. Thereafter, an insulating film is deposited on the substrate to fill in the trenches for planarization, thereby forming trench portions. Subsequently, the second conductor film of tungsten or the like is deposited on the planarized substrate and patterned to form the gate electrode **4**, the dummy gate **51**, and the polysilicon wires **10**. After that, the interlayer insulating film **12** and the metal wire **13** can be formed by a well-known method.

In the present embodiment also, the operating speed can be increased by reducing the amount of charge accumulated in the top and bottom faces of the interlayer insulating film, similarly to the fourth embodiment. In the semiconductor device having such a structure as used in the present embodiment, the upper-layer portion **4b** of the gate electrode **4** is typically composed of a low resistor film composed of silicide or the like. However, since the wiring-to-substrate voltage is also applied in series to the upper-layer and lower-layer portions **4b** and **4a**, the amount of charge is effectively reduced by a voltage drop and the operating speed of the semiconductor device is increased remarkably.

Although the present embodiment has not used such a high resistor film as used in the fourth embodiment, it will be appreciated that a high resistor film may be provided over the dummy gate with an insulating film interposed therebetween.

(Sixth Embodiment)

FIG. **8** is a cross-sectional view of a semiconductor device according to a sixth embodiment.

As shown in the drawing, an active region **6** of a P-type silicon substrate **1** is provided with an element functioning as a MOSFET composed of: a gate oxide film **2**; a gate electrode **4** made of a polysilicon film; and source/drain regions **5**. An isolation region **7** for electrically isolating the individual elements is formed with a plurality of trench portions **8** each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions **9** provided between the individual trench portions **8** and not serving as active regions. On one of the trench portions **8** formed in the isolation region **7**, there is provided a polysilicon wire **10** formed simultaneously with the gate insulating film **2** and the gate electrode **4**. There are further provided an interlayer insulating film **12** made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire **13** formed on the interlayer insulating film **12**.

In the isolation region **7**, inter-trench insulating films **61** each composed of a silicon oxide film and surrounded by the trench portions **8** are formed to overlie the dummy semiconductor portions **9** and underlie the interlayer insulating film **12**. The top faces of the inter-trench insulating films **61** are at the same level as the top faces of the buried trench portions **8**, while the bottom faces thereof are at a level between the top and bottom faces of the buried trench portions **8**.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. **9(a)** to **9(i)** are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process thereof.

In the step shown in FIG. **9(a)**, a thin silicon oxide film **21** having a thickness of 10 nm and a silicon nitride film **22** are formed sequentially on the P-type silicon substrate **1**.

In the step shown in FIG. **9(b)**, a plurality of trenches **14** each having a given width are formed in the silicon substrate **1**. The trenches **14** include: trenches **14a** formed to surround the active region **6** to be formed with the element; trenches **14b** formed in the isolation region **7** separated from the active region **6** by the trenches **14a** to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches **14c** for forming the polysilicon wires. In the isolation region **7** also, the semiconductor portions **9** have been provided to form at least one projecting portion surrounded by the trenches **14**. The semiconductor portions **9** may be considered as dummy active

regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire **10**, which is to be formed in the subsequent step.

In the step shown in FIG. **9(c)**, a silicon oxide film **23** is deposited over the entire surface of the substrate to fill in the trenches **14**.

In the step shown in FIG. **9(d)**, the silicon oxide film **23** is polished by a CMP method. Subsequently, the silicon nitride film **22** and the silicon oxide film **21** are removed selectively to form the plurality of buried trench portions **8** each filled with the silicon oxide film and having a planarized surface. The buried trench portions **8** include: buried trench portions **8a** functioning as isolation; buried trench portions **8b** forming the dummy semiconductor portions **9**; and buried trench portions **8c** for providing insulation between the polysilicon wires and the silicon substrate.

In the step shown in FIG. **9(e)**, the semiconductor portions of the isolation region **7** are subjected to dry etching for forming trenches **62**.

In the step shown in FIG. **9(f)**, a silicon oxide film is filled in each of the trenches **62** to form the inter-trench insulating film **61**.

In the step shown in FIG. **9(g)**, there are formed the gate oxide film **2**, the gate electrode **4** having sidewalls **24** on the side faces thereof, and the polysilicon wire **10** by using a known technique. The gate electrode **4** and the polysilicon wire **10** can be formed simultaneously by using a common semiconductor mask.

In the step shown in FIG. **9(h)**, arsenic ions **25** are implanted from above to form the NMOSFET having the source/drain regions **5** in the active region **6**. Although the arsenic ions **25** are also implanted into the isolation region **7** during the process, no trouble occurs. In the case of using a resist mask covering a region to be formed with a PMOSFET, however, the isolation region **7** may be covered with the resist mask.

In the step shown in FIG. **9(i)**, a silicon oxide film is deposited to form the interlayer insulating film **12**, followed by the metal wire **13** formed thereon.

In the semiconductor device according to the present embodiment, the inter-trench insulating films **61** each composed of the silicon oxide film are formed over the dummy semiconductor portions **9** of the isolation region **7** and under the interlayer insulating film **12** to be surrounded by the buried trench portions **8**. The top faces of the inter-trench insulating films **61** are at the same level as the top faces of the buried trench portions **8**, while the bottom faces thereof are at a level between the top and bottom faces of the buried trench portions **8**.

Thus, in the semiconductor device according to the present embodiment, the inter-trench insulating films **61** are formed by filling the silicon oxide films in the respective dummy semiconductor portions **9** that have been lowered in level, so that the distance between the wiring and the substrate is longer than in the conventional semiconductor device shown in FIG. **19**. Since the wiring-to-substrate capacitance decreases in inverse proportion to the distance, the wiring-to-substrate capacitance is smaller in the semiconductor device according to the present embodiment than in the conventional semiconductor device, resulting in a higher operating speed.

Although the present embodiment has described the case where the silicon oxide film is buried in each of the semiconductor portions, similar effects can also be achieved if an insulating film composed of a silicon nitride film is used.

Although the semiconductor portions 9 have been lowered in level and filled with the silicon oxide films prior to the formation of the gate electrode, the method of manufacturing a semiconductor device according to the present invention is not limited to such an embodiment. The same effects as achieved in the present embodiment can also be achieved if the steps of lowering the semiconductor portions 9 in level and filling the silicon oxide films therein are performed after the formation of the gate electrode or prior to the formation of trench isolation.

(Seventh Embodiment)

FIG. 10 is a cross-sectional view of a semiconductor device according to a seventh embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

In upper portions of the dummy semiconductor portions 9 of the isolation region 7, oxygen atoms have been introduced by ion implantation or the like to form high resistor portions 71 each composed of a high-resistance silicon layer. Although the bottom faces of the high resistor portions 71 are at a level between the top and bottom faces of the trench portions 8, they may be positioned at a level lower than the bottom faces of the trench portions 8.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 11(a) to 11(h) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process thereof.

In the step shown in FIG. 11(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 11(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 11(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 11(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon

nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 11(e), a resist mask 73 covering the active region 6 is formed and oxygen ions 72 are implanted only into the isolation region 7 to form the high resistor portions 71 in the outermost surface of the silicon substrate, in which the oxygen ions have been introduced as an impurity in the semiconductor portions 9 of the isolation region 7.

In the step shown in FIG. 11(f), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 and the polysilicon wire 10 can be formed simultaneously by using a common semiconductor mask.

In the step shown in FIG. 11(g), arsenic ions are implanted from above the substrate to form the NMOSFET having the source/drain regions 5 in the active region 6. Although the arsenic ions 25 are also implanted into the isolation region 7 during the process, no trouble occurs. In the case of using a resist mask covering a region to be formed with a MOSFET, however, the isolation region 7 may be covered with the resist mask.

In the step shown in FIG. 11(h), a silicon oxide film is formed as the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

The semiconductor device according to the present embodiment is characterized in that the oxygen atoms have been introduced into the upper portions of the semiconductor portions 9 of the isolation region 7 by ion implantation or the like to form the high resistor portions 71 each composed of a high-resistance silicon layer. Although the bottom faces of the high resistor portions 71 are at a level between the top and bottom faces of the buried trench portions 8, they may be positioned at a level lower than the bottom faces of the buried trench portions 8.

Since the high resistor portions 71 each composed of a high-resistance silicon layer have been formed in the dummy semiconductor portions 9 of the silicon substrate, a voltage drop occurs in the high resistor portions 71 of the silicon substrate when a voltage is placed between the wiring and the substrate. Consequently, a potential difference between the wiring and semiconductor portions 9 is reduced so that the amount of charge is reduced in direct proportion to the placed voltage, though the capacitance of the interlayer insulating film 12 between the wiring and the semiconductor portions 9 is equal to that of the interlayer insulating film 12 in the conventional semiconductor device shown in FIG. 19. Accordingly, the time required for charging or discharging is reduced and the operating speed of the semiconductor device is increased.

Although the present embodiment has described the case where oxygen atoms are introduced as an impurity into the dummy semiconductor portions 9, similar effects can be achieved if nitrogen atoms are introduced.

Although the high resistor portions are formed prior to the formation of the gate electrode in the present embodiment, they may be formed at any stage of the process of manufacturing the semiconductor device provided that oxygen atoms can be introduced into the semiconductor portions.

(Eighth Embodiment)

FIG. 12 is a cross-sectional view of a semiconductor device according to an eighth embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; sidewalls 3 formed on the side faces of the gate electrode 4 and composed of silicon oxide films; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Over the dummy semiconductor portions 9 and trench portions 8 of the isolation region 7, an underlying insulating film 81 made of a silicon oxide film has been formed simultaneously with the sidewalls on the side faces of the gate electrode 4. The underlying insulating film 81 has been formed to cover the entire polysilicon wire 10.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 13(a) to 13(i) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 13(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 13(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 13(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 13(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 13(e), there are formed the gate oxide film 2, the gate electrode 4 made of polysilicon, and

the polysilicon wire 10 by using a known technique. The gate electrode 4 can be formed simultaneously with the polysilicon wire 10 by using a common semiconductor mask.

In the step shown in FIG. 13(f), a silicon oxide film 82 is deposited over the entire surface of the substrate, followed by a resist mask 84 formed thereon to cover the isolation region 7.

In the step shown in FIG. 13(g), a silicon oxide film 82 is removed selectively by anisotropic dry etching using the resist mask 84 to form an underlying insulating film 81 over the isolation region 7, while the sidewalls are formed on the side faces of the gate electrode 4. The polysilicon wire 10 is completely covered with the underlying insulating film 81.

In the step shown in FIG. 13(h), arsenic ions 25 are implanted from above to form the NMOSFET having the source/drain regions 5 in the active region 6. Although the arsenic ions are also implanted into the isolation region 7 during the process, no trouble occurs. However, in the case of using a resist mask covering a region to be formed with a PMOSFET, the isolation region 7 may be covered with the resist mask.

In the step shown in FIG. 13(i), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

The semiconductor device according to the present embodiment is characterized in that the underlying insulating film 81 composed of the silicon oxide film is formed simultaneously with the sidewalls on the side faces of the gate electrode 4 to extend over the dummy semiconductor portions 9 and buried trench portions 8 of the isolation region 7. The resulting underlying insulating film 81 covers the entire polysilicon wire 10.

Thus, in the semiconductor device according to the present embodiment, the underlying insulating film 81 composed of the silicon oxide film is present over the isolation region 7, so that the distance between the wiring and the substrate is longer than in the conventional semiconductor device shown in FIG. 19. Since the wiring-to-substrate capacitance decreases in inverse proportion to the distance, the wiring-to-substrate capacitance is reduced in the semiconductor device according to the present embodiment, resulting in a higher operating speed.

Although the present embodiment has described the case where the underlying insulating film 81 is composed of the silicon oxide film, similar effects can also be achieved if an insulating film composed of a silicon nitride film is used.

Although the present embodiment has described the case where the underlying insulating film is composed of a single-layer film, the underlying insulating film may be composed of a multi-layer film. For example, in the case where the sidewalls consist of L-shaped portions extending over the side faces of the gate electrode and the substrate and of upper wedge-shaped portions or, alternatively, the sidewalls are provided along with an on-gate protective film, the underlying insulating film should be composed of a multi-layer film. It will be appreciated that, in that case also, the same effects as achieved in the present embodiment are achieved.

(Ninth Embodiment)

FIG. 14(a) is a cross-sectional view of a semiconductor device according to a ninth embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the

individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Under the dummy semiconductor portions 9 and the trench portions 8, a buried insulating film 91 composed of a silicon oxide film is formed in contact with the bottom faces of the trench portions 8. As a result, the side faces of the semiconductor portions 9 are in contact with the trench portions 8, while the bottom faces thereof are in contact with the buried insulating film 91.

FIG. 14(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment. In the semiconductor device according to the present embodiment, since the buried insulating film 91 composed of the silicon oxide film is formed in the silicon substrate, the capacitance Cij becomes a half of the capacitance Cj1 shown in FIG. 1(b) or less (T. Nishimura and Y. Inoue: Proceedings of VLSI TECHNOLOGY WORKSHOP ON "WHAT IS THE FUTURE OF SOI?" (1995) p.123).

Therefore, the total wiring-to-substrate capacitance Cijt of the semiconductor device is represented by the following equation (11):

$$Cijt = \{ (Ca1 \times Cij) / (Ca1 + Cij) \} + \Sigma Ca2 \tag{11},$$

which is smaller than the total capacitance Cjt represented by the equation (3). Accordingly, the following inequality (12) is satisfied:

$$Cijt < Cjt \tag{12}.$$

Hence,

$$Cijt < Cat$$

is derived from the relationship represented by the equation (4), so that the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment is reduced, resulting in the semiconductor device operating at a higher speed.

FIGS. 15(a) to 15(h) are cross-sectional views of the structure of the semiconductor device having the NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 15(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 15(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semi-

conductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 15(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 15(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 15(e), a resist mask 92 covering the active region 6 is formed and oxygen ions 93 are implanted only into the isolation region 7 so that the buried insulating film 91 into which the oxygen atoms have been introduced as an impurity is formed. The buried insulating film 91 provides insulation between the silicon substrate 1 and the semiconductor portions 9 in the isolation region 7. In this case, the buried insulating film 91 is connected to the respective side faces of each of the individual trench portions 8a to 8c and energy for implanting the oxygen ions is set such that the semiconductor portions 9 are in the floating state.

In the step shown in FIG. 15(f), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 may be formed simultaneously with the polysilicon wire 10 by using a common semiconductor mask.

In the step shown in FIG. 15(g), a resist mask 95 is formed to cover the isolation region 7 and arsenic ions 25 are implanted into the active region 6 to form the NMOSFET having the source/drain regions 5. In this case, no implantation is performed with respect to the isolation region 7.

In the step shown in FIG. 15(h), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

In the semiconductor device formed by the manufacturing method according to the present embodiment, the buried insulating film 91 composed of the silicon oxide film is formed under the dummy semiconductor portions 9 and the buried trench portions 8 to be in contact with the bottom faces of the buried trench portions 8. As a result, the side faces of the semiconductor portions 9 are in contact with the buried trench portions 8, while the bottom faces thereof are in contact with the insulating film 91. Although the present embodiment has formed the buried insulating film by implanting oxygen ions prior to the formation of the gate electrode, the buried insulating film may be formed at any stage of the method of manufacturing the semiconductor device provided that oxygen atoms can be introduced into the semiconductor portions.

(Tenth Embodiment)

The present embodiment will basically describe another example of the manufacturing process shown in FIG. 14(b), which is for achieving the effect of capacitance reduction.

FIGS. 16(a) to 16(i) are cross-sectional views of the structure of a semiconductor device having an NMOSFET according to a tenth embodiment in the manufacturing process therefor.

In the step shown in FIG. 16(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on a P-type silicon substrate 1.

In the step shown in FIG. 16(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround an active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step. In the step shown in FIG. 15(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 16(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 16(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively except for the portions overlying the active region 6 to form a plurality of buried trench portions 8 each filled with a silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 16(e), the semiconductor portions 9 of the isolation region 7 are subjected to dry etching for forming trenches 96.

In the step shown in FIG. 16(f), a silicon oxide film is deposited in each of the trenches 96 to form a buried insulating film 91, followed by a silicon film deposited thereon to form semiconductor portions 97 serving as dummy active regions. The buried insulating films 91 are in contact with the buried trench portions 8a to 8c.

In the step shown in FIG. 16(g), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 may be formed simultaneously with the polysilicon wire 10 by using a common semiconductor mask.

In the step shown in FIG. 16(h), a resist mask 98 is formed to cover the isolation region 7 and arsenic ions 25 are implanted into the active region 6 to form the NMOSFET having source/drain regions 5. In this case, implantation may be performed with respect to the isolation region 7, though it is not performed in the example.

In the step shown in FIG. 16(i), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

The manufacturing method according to the present embodiment also enables the formation of a semiconductor device having the same structure as the semiconductor device according to the ninth embodiment, resulting in smaller wiring-to-substrate capacitance and a higher operating speed.

Although the present embodiment has grown the silicon oxide films and the silicon films in the trenches 96 prior to forming the gate electrode, the silicon oxide films and the silicon films may be grown at any stage of the process of

manufacturing the semiconductor device provided that they can be grown and buried in the trenches 96. (Eleventh Embodiment)

The present embodiment will also basically describe still another example of the manufacturing process shown in FIG. 14(b), which is for achieving the effect of capacitance reduction.

FIGS. 17(a) to 17(f) and FIGS. 18(a) to 18(d) are cross-sectional views showing the structure of a semiconductor device having an NMOSFET according to an eleventh embodiment in the manufacturing process therefor.

In the step shown in FIG. 17(a), a trench 102 is formed in a region of a P-type silicon substrate 1 in which an isolation region is to be formed.

In the step shown in FIG. 17(b), a silicon oxide film is filled in the trench 102 to form an insulating film 101 so that the entire surface of the substrate is planarized.

In the step shown in FIG. 17(c), a silicon film 103 is epitaxially grown over the entire surface of the substrate. During the step, since single-crystal silicon is grown on single-crystal silicon in an active region 6, a semiconductor region having an excellent crystallographic property is formed therein, while a silicon film having an inferior crystallographic property is formed on the silicon oxide film in the isolation region 7. However, since the silicon film in the isolation region 7 does not function as an active region, the inferior crystallographic property thereof will not adversely affect the properties of the semiconductor device.

In the step shown in FIG. 17(d), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the silicon film 103.

In the step shown in FIG. 17(e), a plurality of trenches 14 each having a given width are formed in the substrate. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step. In forming the trenches 14, etching is performed till the surface of the buried insulating film 101 is exposed in the trenches 14.

In the step shown in FIG. 17(f), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 18(a), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form a plurality of buried trench portions 8 each filled with a silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 18(b), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 is formed simultaneously with the polysilicon wire 10.

In the step shown in FIG. 18(c), arsenic ions 25 are implanted into the active region 6 to form source/drain

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regions 5 by using a resist mask 95 formed to cover the isolation region 7. The NMOSFET is formed by the foregoing process. Although arsenic ions 25 are not implanted in the isolation region 7 in the example, they may be implanted alternatively.

In the step shown in FIG. 18(d), a silicon oxide film is deposited to form an interlayer insulating film 12, followed by a metal wire 13 formed thereon.

The manufacturing method according to the present embodiment also enables the formation of a semiconductor device having the same structure as the semiconductor device according to the ninth embodiment, resulting in smaller wiring-to-substrate capacitance and a higher operating speed.

Although the present embodiment has formed the trench 102 in the silicon substrate 1 and buried the silicon oxide film therein to form a miniaturized gate electrode 4, the silicon oxide film may be formed directly on the isolation region without forming the trench if the semiconductor substrate inferior in planarity does not adversely affect the patterning of the gate during the formation of the gate electrode.

(Variations of Individual Embodiments)

Although the eighth embodiments of the present invention have been described, there are variations obtained by combining the individual embodiments with each other.

By way of example, the first embodiment used in combination with the second to eighth embodiments achieves a further reduction in wiring-to-substrate capacitance and a reduction in time required for charging or discharging, so that the resulting semiconductor device operates at a higher speed than in the case where each of the embodiments is used singly.

Thus, according to the present invention, the individual embodiments used in combination can achieve more remarkable effects than in the case where each of the embodiments is used singly.

Although each of the embodiments has used the NMOSFET as the element to be disposed in the active region 6, the present invention is not limited to such embodiments. The element includes an active element other than the MOSFET such as a bipolar transistor or diode or a passive element such as a capacitor.

We claim:

1. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and

at least one PN junction formed in said dummy semiconductor portions underlying said wire.

2. A semiconductor device according to claim 1, wherein said PN junction includes a plurality of PN junctions formed in said dummy semiconductor portions.

3. A semiconductor device according to claim 1, wherein said active region is formed with an impurity diffusion region and a PN junction is formed at a bottom face of said

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impurity diffusion region, the PN junction of said isolation region being positioned at a level lower than the PN junction of said active region.

4. A semiconductor device according to claim 1, wherein said PN junction formed in said dummy semiconductor portion is positioned at a level between a top surface and a bottom surface of said second trench portion.

5. A semiconductor device according to claim 1, wherein said PN junction formed in said dummy semiconductor portion is positioned at a level below a bottom surface of said second trench portion.

6. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and

a dielectric film interposed between at least said dummy semiconductor portions of said isolation region and said interlayer insulating film.

7. A semiconductor device according to claim 6, wherein said dielectric film is an underlying insulating film interposed between said interlayer insulating film and said dummy semiconductor portions and said second trench portion.

8. A semiconductor device according to claim 7, further comprising a gate electrode formed on the semiconductor substrate within said active region and sidewalls made of an insulating material and formed on both side faces of said gate electrode, wherein said underlying insulating film is formed of the same film as forming said sidewalls.

9. A semiconductor device according to claim 8, wherein said underlying insulating film is composed of a multilayer film.

10. A semiconductor device according to claim 6, wherein said dielectric film is formed in an upper portion of each of said dummy semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top face of each of said second trench portion.

11. A semiconductor device according to claim 6, wherein said dielectric film is composed of at least one of a silicon oxide film and a silicon nitride film.

12. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and

a buried insulating film formed only in said isolation region, and in an inner portion of each of said dummy semiconductor portions in said isolation region.

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13. A semiconductor device comprising:
a semiconductor substrate having an active region and an isolation region surrounding said active region;
a first trench portion filled with an insulating material formed to separate said active region from said isolation region;
a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;
an interlayer insulating film formed to extend continuously over said active region and said isolation region;
a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and
a resistor film formed under said wire, and between said interlayer insulating film and at least said dummy semiconductor portions of said isolation region.

14. A semiconductor device according to claim 13, wherein said resistor film is an underlying resistor film formed to extend continuously over said dummy semiconductor portions and said second trench portions.

15. A semiconductor device according to claim 14, further comprising a resistor element formed on said semiconductor substrate and having a high resistor film, wherein said underlying resistor film is formed of the same film as composing the high resistor film of said resistor element.

16. A semiconductor device according to claim 14, further comprising an element having an electrode member composed of a conductor film formed on the semiconductor substrate within said active region, wherein said resistor film is composed of the same material as composing said electrode member.

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17. A semiconductor device according to claim 14, further comprising a FET having a gate electrode composed of a first conductor film formed on the semiconductor portion within said active region and a second conductor film deposited on said first conductor film, wherein
a top surface of the first conductor film of said gate electrode is at approximately the same level as a top surface of said first trench portion and said second trench portion,
a region of said resistor film overlying each of said semiconductor portions is formed of the same two films as composing said first and second conductor films of said gate electrode, and
a region of said resistor film overlying said first trench portion and said second trench portion is composed of the same material as composing said first conductor film of said gate electrode.

18. A semiconductor device according to claim 13, wherein said resistor film is formed in an upper portion of each of said dummy semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top surface of said second trench portion.

19. A semiconductor device according to claim 18, wherein said resistor film is composed of a silicon film containing at least one of an oxygen atom and a nitrogen atom.

20. A semiconductor device according to claim 13, wherein said resistor film is composed of at least one of a polysilicon film and an amorphous silicon film.

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The present invention relates to a semiconductor device having a trench-isolated structure and, more particularly, to a method of reducing the capacitance between the wiring and substrate of the semiconductor device.

As higher-density and increasingly miniaturized semiconductor devices have been implemented in recent years, repeated attempts have been made to substitute a trench isolation technique for a LOCOS technique which is most prevalently used to form isolation for providing insulation between individual elements of the semiconductor devices. In accordance with the trench isolation technique, an insulating material is filled in a trench formed in a semiconductor substrate to form isolation.

Since planarization of a surface of a semiconductor substrate including the insulating material filled in the trench is important to the trench isolation technique, chemical mechanical polishing (CMP) has been used as a planarizing technique which achieves excellent in-plane uniformity free from pattern dependence. In the case where the trench occupies a large area in a CMP process for planarization, the provision of dummy island semiconductor portions has been proposed to avoid trouble resulting from so-called pattern dependence, which causes polishing properties to vary depending on the area of a region to be planarized. In other words, the trench is divided into a

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plurality of narrow trenches so that the surface of the semiconductor substrate is exposed between the individual trenches to form the dummy semiconductor portions which do not serve as active regions.

5 FIG. 19 shows an example of the conventional trench-isolated semiconductor device having the dummy island semiconductor portions.

As shown in FIG. 19, an active region 6 of a P-type silicon substrate 1 is formed with: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5 into which an impurity has been introduced. An isolation region 7 surrounding the active region 6 is formed with a plurality of trench portions 8 each filled with a silicon oxide film. Between the individual trench portions 8, there are provided semiconductor portions 9 having top surfaces at the same level as the top surfaces of the trench portions 8. On the trench portions 8 also, there is provided a polysilicon wire 10 formed simultaneously with the gate oxide film 2 and the gate electrode 4 of an element. An interlayer insulating film 12 is deposited over the entire surface of the substrate, followed by a metal wire 13 provided thereon.

In this case, if the trench portions have such large widths as shown in FIG. 21(b), a silicon oxide film filled in each of the trench portions is polished during the CMP process for planarizing the whole substrate so that the surface thereof is

depressed due to pattern dependence, which leads to the trouble of degraded planarity or the like. The isolation structure as shown in FIG. 19 has been proposed to prevent such trouble resulting from pattern dependence.

5 FIGS. 20(a) to 20(g) are cross-sectional views illustrating a process of manufacturing the conventional trench-isolated semiconductor device having an NMOS transistor.

10 In the step shown in FIG. 20(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

15 In the step shown in FIG. 20(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. However, the trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions.

20 In the step shown in FIG. 20(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in

the trenches 14.

In the step shown in FIG. 20(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to
5 form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for
10 providing insulation between the polysilicon wires and the silicon substrate.

In the step shown in FIG. 20(e), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known
15 technique. The gate electrode 4 and the polysilicon wire 10 are formed simultaneously.

In the step shown in FIG. 20(f), arsenic ions 25 are implanted into the active region 6 of the NMOSFET region by using a resist mask Rem covering the PMOSFET region and the isolation
20 region to form the source/drain regions 5. The NMOSFET is formed by the foregoing process steps.

In the step shown in FIG. 20(g), the silicon oxide film is deposited to form the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

25 In the foregoing step shown in FIG. 20(f), ions of such an

impurity as phosphorus or arsenic have been implanted into the gate electrode 4 and source/drain regions 5 of the active region 6 in the step shown in FIG. 20(f). However, impurity ions are not implanted in principle in the region other than the active region 6, though they may be introduced slightly extensively into the periphery of the isolation region in considerations of mask displacement. Hence, impurity ions are not implanted in the dummy semiconductor portions 9 between the individual trench portions 8.

10 A description will be given to the wiring-to-substrate capacitance of the trench-isolated semiconductor device having the small trench portions 8 which are discretely located and the dummy semiconductor portions 9 as shown in FIG. 19 and in a semiconductor device having a wide isolating/insulating film such as a LOCOS film. FIG. 21(a) is a cross-sectional view for illustrating, by way of example, the wiring-to-substrate capacitance in the isolation region 7 having the dummy semiconductor portions 9. FIG. 21(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance of the semiconductor device having a LOCOS isolation film 100 and no dummy semiconductor portion. It is assumed here that impurity ions have not been implanted in the isolation region 7 during the implantation of ions into the source/drain regions and that the area occupied by the whole isolation region 7 is equal in each of the two semiconductor devices.

In the semiconductor device shown in FIG. 21(a), a total wiring-to-substrate capacitance C_{at} corresponds to the sum of capacitances C_{a1} and C_{a2} , which is represented by the following equation (1):

5 $C_{at} = \Sigma C_{a1} + \Sigma C_{a2} \quad \dots (1).$

In the case where a member interposed between the wiring and substrate is composed of a homogeneous material, the wiring-to-substrate capacitance per unit area is inversely proportional to the distance between the wiring and substrate, so that the
10 capacitance is larger as the distance is shorter. If the total wiring-to-substrate of the semiconductor device shown in FIG. 21(b) is represented by C_{bt} when the dimension D_{a2} shown in FIG. 21(a) is equal to the dimension D_{bt} shown in FIG. 21(b), the following inequality (2) is satisfied:

15 $C_{at} > C_{bt} \quad \dots (2),$

which indicates that the wiring-to-substrate capacitance C_{at} in the structure shown in FIG. 21(a) is larger than the wiring-to-substrate capacitance C_{bt} in the structure shown in FIG. 21(b).

Although the formation of the island pattern composed of
20 the dummy semiconductor portions in the isolation region has the advantage of achieving planarization with excellent in-plane uniformity, it also has the possibility of increasing the wiring-to-substrate capacitance and resultantly reducing the operating speed of the semiconductor device.

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SUMMARY OF THE INVENTION

In view of the foregoing, the present invention has been achieved based on the principle that, if each electrode of a parallel-plate capacitor occupies an equal area, the capacitance of the capacitor is generally smaller as the distance between the electrodes is larger or on the physical phenomenon that, even when the capacitor has equal capacitance, the amount of charge accumulated therein is smaller as the voltage between the electrodes is lower.

It is therefore an object of the present invention to increase the operating speed of a trench-isolated semiconductor device comprising an isolation region consisting of trench portions and dummy semiconductor portions by providing therein means for reducing the wiring-to-substrate capacitance in the isolation region or means for reducing the amount of charge accumulated in the capacitance present between the wiring and substrate in the isolation region.

A first semiconductor device according to the present invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a

wire formed on the interlayer insulating film; and at least one PN junction formed in the semiconductor portions underlying the wire.

In the arrangement, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the upper portion of the PN junction of each of the semiconductor portions to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. Accordingly, the wiring-to-substrate capacitance of the whole semiconductor device is reduced, resulting in the semiconductor device operating at a higher speed.

The PN junction may include a plurality of PN junctions formed in the semiconductor portions.

The arrangement achieves a further reduction in wiring-to-substrate capacitance, resulting in a higher operating speed.

The active region may be formed with an impurity diffusion region and a PN junction may be formed at a bottom face of the impurity diffusion region, the PN junction of the isolation region being positioned at a level lower than the PN junction of the active region.

The arrangement further reduces the wiring-to-substrate capacitance.

A second semiconductor device according to the present

invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor

5 portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; and a dielectric film interposed between at least the semiconductor portions of
10 the isolation region and the interlayer insulating film.

In the arrangement, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the dielectric film to the
15 capacitance in the interlayer insulating film, so that the total wiring-to-substrate capacitance is lowered. Consequently, the operating speed of the semiconductor device is increased.

As the dielectric film, an underlying insulating film may be provided between the interlayer insulating film and the
20 semiconductor portions and trench portions.

There can be further provided a gate electrode formed on the semiconductor substrate within the active region and sidewalls made of an insulating material and formed on both side faces of the gate electrode such that the underlying insulating
25 film is formed of the same film as forming the sidewalls.

The underlying insulating film may be composed of a multilayer film.

The arrangement enables the underlying insulating film for reducing the wiring-to-substrate capacitance to be composed by
5 using the sidewalls required to form a MOSFET of so-called LDD structure. Consequently, the wiring-to-substrate capacitance can be reduced, while avoiding an increase in manufacturing cost.

The dielectric film may be formed in an upper portion of each of the semiconductor portions of the semiconductor substrate
10 to have a top face at approximately the same level as a top face of each of the trench portions.

Preferably, the dielectric film is composed of at least one of a silicon oxide film and a silicon nitride film.

A third semiconductor device according to the present
15 invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the
20 isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; and a buried insulating film formed in an inner portion of each of the semiconductor portions in the isolation region.

25 The arrangement allows a reduction in the wiring-to-

substrate capacitance of the entire isolation region, resulting in a significant reduction in operating speed.

A fourth semiconductor device according to the present invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; an a resistor film formed between the interlayer insulating film and at least the semiconductor portions of the isolation region.

In the arrangement, a voltage drop in the resistor film reduces the amount of charge accumulated in the wiring-to-substrate capacitance in the region of the semiconductor device containing the resistor film, though the wiring-to-substrate capacitance is not reduced in the region. Consequently, the time required for charging or discharging is reduced, resulting in the semiconductor device operating at a higher speed.

As the resistor film, an underlying resistor film may be formed to extend continuously over the semiconductor portions and trench portions.

The arrangement allows the wiring-to-substrate capacitance to be reduced by using various films having electric resistivity

which are formed on the semiconductor substrate.

There can further be provided a resistor element formed on the semiconductor substrate and having a high resistor film such that the underlying resistor film is formed of the same film as
5 composing the high resistor film of the resistor element.

In the arrangement, the underlying resistor film having the same resistance as the high resistor film used as a resistor element achieves a remarkable voltage dropping effect.

There can further be provided an element having an electrode
10 member composed of a conductor film formed on the semiconductor substrate within the active region such that the resistor film is composed of the same material as composing the electrode member.

There can further be provided a FET having a gate electrode
15 composed of a first conductor film formed on the semiconductor portion within the active region and a second conductor film deposited on the first conductor film such that a top surface of the first conductor film of the gate electrode is at approximately the same level as a top surface of each of the trench portions,
20 while a region of the resistor film overlying each of the semiconductor portions is formed of the same two films as composing the first and second conductor films of the gate electrode and a region of the resistor film overlying each of the trench portions is composed of the same material as composing the
25 first conductor film of the gate electrode.

Each of the arrangements eliminates the necessity for an additional step of forming the resistor film, so that the wiring-to-substrate capacitance is reduced, while an increase in manufacturing cost is prevented.

5 The resistor film may be formed in an upper portion of each of the semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top surface of each of the trench portions.

10 The resistor film may be composed of a silicon film containing at least one of an oxygen atom and a nitrogen atom.

 The resistor film may be composed of at least one of a polysilicon film and an amorphous silicon film.

15 The arrangement allows the formation of the resistor film by using the polysilicon film or amorphous silicon film to compose the gate electrode and the resistor element and thereby prevents an increase in manufacturing cost.

 A first method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region of a first conductivity type, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried

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trench portion; a third step of forming an element on the active region; a fourth step of introducing an impurity containing at least an impurity of a second conductivity type into the dummy semiconductor portions of the isolation region to form at least one PN junction in the dummy semiconductor portions; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

The methods enables the formation of the semiconductor device including the dummy semiconductor portions each having the PN junction. The capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the upper portion of the PN junction of each of the semiconductor portions to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. Accordingly, the wiring-to-substrate capacitance of the whole semiconductor device is reduced, resulting in the semiconductor device operating at a higher speed.

The third and fourth steps may include forming a gate electrode of a FET as the element on the active region, introducing the impurity of the second conductivity type into the active region and the dummy semiconductor portions, and thereby forming source/drain regions of the FET, while forming the at least one

PN junction in the dummy semiconductor portions.

The method enables the formation of the semiconductor device operating at a high speed by using a typical manufacturing process for forming a FET without an additional step of forming
5 the PN junction in each of the dummy semiconductor portions.

The third step may include forming a gate electrode of a FET as the element on the active region by using a first mask covering the isolation region and introducing the impurity of the second conductivity type into the active region to form
10 source/drain regions of the FET and the fourth step may include introducing the impurity containing at least the impurity of the second conductivity type into the dummy semiconductor portions by using a second mask covering the active region to form the at least one PN junction in the dummy semiconductor portions.

15 The method enables the formation of the semiconductor device having an arbitrary number of PN junctions without placing restraints on the depth and impurity concentration of the PN junction in the active region, resulting in a semiconductor device having minimum wiring-to-substrate capacitance.

20 A second method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for
25 partitioning the isolation region into a plurality of dummy

semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming a resistor film on each of the dummy semiconductor portions of the isolation region; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

10 The method enables the formation of the semiconductor device comprising the resistor film between the interlayer insulating film and dummy semiconductor portions of the isolation region. A voltage drop in the resistor film reduces the amount of charge accumulated in the wiring-to-substrate capacitance, 15 though the wiring-to-substrate capacitance is not reduced in the region containing the resistor film of the semiconductor device. Consequently, the time required for charging or discharging is reduced, resulting in the semiconductor device operating at a higher speed.

20 The fourth step may include composing the resistor film of a film containing at least one of polysilicon and amorphous silicon.

The fourth step may include composing the resistor film of a multilayer film constituted by two or more conductor films with 25 at least an insulating film interposed therebetween.

The fourth step may include introducing an impurity at a concentration of 1×10^{20} atoms \cdot cm⁻³ or lower into the resistor film.

5 A third method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy
10 semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of implanting ions into an upper portion of each of the dummy
15 semiconductor portions to form a high resistor portion therein; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

The method allows the formation of the semiconductor device
20 comprising the high resistor portion between the interlayer insulating film and dummy semiconductor portions of the isolation region. As described above, a voltage drop in the region containing the high resistor portion of the semiconductor device reduces the amount of charge accumulated in the wiring-to-
25 substrate capacitance. What results is the semiconductor device

which requires a shorter time for charging or discharging and therefore operates insulating film at a higher speed.

The fourth step may include implanting ions containing at least an atom having an oxidizing function to form the high
5 resistor portion.

The fourth step may include implanting ions containing at least an atom having a nitriding function to form the high resistor portion.

A fourth method of manufacturing a semiconductor device
10 according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy
15 semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming an underlying insulating film over the dummy
20 semiconductor portions of the isolation region; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

In accordance with the method, there is formed the
25 semiconductor device including the underlying insulating film

beneath the interlayer insulating film in the isolation region thereof. Consequently, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by
5 adding in series the capacitance in the underlying insulating film to the capacitance in the interlayer insulating film, so that the total wiring-to-substrate capacitance is reduced. What results is the semiconductor device operating at a high speed.

The third step and the fourth step may include forming a
10 gate electrode of a FET forming the element on the active region, depositing a dielectric film on the substrate, performing anisotropic etching with respect to the dielectric film by using a mask covering the isolation region, and thereby leaving
15 sidewalls on both side faces of the gate electrode, while leaving the underlying insulating film over the dummy semiconductor portions.

The method enables the formation of a semiconductor device operating at a high speed by using a typical manufacturing process for forming a FET without an additional step of forming the
20 underlying insulating film.

The fourth step may include forming the underlying insulating film of a dielectric film containing at least silicon oxide.

The fourth step may include forming the underlying
25 insulating film of a dielectric film containing at least silicon

nitride.

A fifth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region,
5 a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first
10 buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming depressed portions by etching the dummy semiconductor portions and filling an insulating material in the depressed portions to form inter-trench insulating films each having a top
15 face at the same level as respective top faces of the first and second buried trench portions; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

20 In accordance with the method, there is formed the semiconductor device comprising the inter-trench insulating films between the interlayer insulating films and dummy semiconductor portions of the isolation region thereof. Consequently, the capacitance component of the wiring-to-
25 substrate capacitance in the region containing the semiconductor

portions of the isolation region is obtained by adding in series the capacitance in the inter-trench buried insulating films to the capacitance in the interlayer insulating film, so that the total wiring-to-substrate capacitance is reduced. What results is the semiconductor device operating at a high speed.

The fourth step may include forming each of the inter-trench insulating films of a dielectric film containing at least silicon oxide.

The fourth step may include forming each of the inter-trench insulating films of a dielectric film containing at least silicon nitride.

A sixth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of implanting oxygen ions into each of the dummy semiconductor portions to form a buried insulating film in an inner portion thereof; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming

a wire on the interlayer insulating film.

A seventh method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region,
5 a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first
10 buried trench portion and a second buried trench portion; a third step of forming third trenches by etching the semiconductor portions and filling an insulating material in the third trenches to form buried insulating films each having a top face at a level lower than respective top faces of the first and second buried
15 trench portions; a fourth step of growing semiconductor films on the buried insulating films, with the active region covered with a mask member, to form dummy semiconductor portions; a sixth step of forming an interlayer insulating film over an entire surface of the substrate; a fifth step of forming an element on the active
20 region; a seventh step of forming a wire on the interlayer insulating film.

An eighth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region,
25 a first trench extending over an entire isolation region of the

substrate region, while leaving an active region of the substrate region; a second step of filling an insulating material in the first trench to form a buried insulating film having a top face at the same level as a top face of the isolation region; a third
5 step of growing a semiconductor film over the active region and the buried insulating film; a fourth step of forming, in the semiconductor substrate, a second trench for partitioning the semiconductor film and the substrate region into the active region and the isolation region and a third trench for partitioning the
10 portion of the semiconductor film overlying the isolation region into a plurality of dummy semiconductor portions; a fifth step of filling an insulating material in each of the second and third trenches to form a first buried trench portion and a second buried trench portion; a sixth step of forming an element on the portion
15 of the semiconductor film overlying the active region; a seventh step of forming an interlayer insulating film over an entire surface of the substrate; and an eighth step of forming a wire on the interlayer insulating film.

In accordance with the methods, there are obtained
20 semiconductor devices each comprising a buried insulating film at a depth of each of the dummy semiconductor portions of the isolation region. What results is the semiconductor device having smaller wiring-to-substrate capacitance and operating at a higher speed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(a) is a cross-sectional view of a semiconductor device according to a first embodiment, having shallow PN junctions formed in the semiconductor portions thereof and FIG.

5 1(b) is an enlarged cross-sectional view of an isolation region for illustrating the wiring-to-substrate capacitance in the semiconductor device;

FIGS. 2(a) to 2(g) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to
10 the first embodiment;

FIG. 3 is a cross-sectional view of a semiconductor device according to a second embodiment, having shallow PN junctions formed in the semiconductor portions thereof;

FIG. 4 is a cross-sectional view of a semiconductor device
15 according to a third embodiment, having two PN junctions in the semiconductor portions thereof;

FIG. 5 is a cross-sectional view of a semiconductor device according to a fourth embodiment, having a high resistor film formed on the semiconductor portions thereof;

20 FIGS. 6(a) to 6(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a fourth embodiment;

FIG. 7 is a cross-sectional view of a semiconductor device according to a fifth embodiment, having a multilayer gate provided
25 therein;

FIG. 8 is a cross-sectional view of a semiconductor device according to an eighth embodiment, having an inter-trench film formed on each of the semiconductor portions thereof;

FIGS. 9(a) to 9(i) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to the sixth embodiment;

FIG. 10 is a cross-sectional view of a semiconductor device according to a seventh embodiment, having a high resistor portion in the upper portion of each of the semiconductor portions;

FIGS. 11(a) to 11(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a seventh embodiment;

FIG. 12 is a cross-sectional view of a semiconductor device according to an eighth embodiment, having an underlying, having an underlying insulating film formed beneath an interlayer insulating film;

FIGS. 13(a) to 13(i) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to the eighth embodiment;

FIG. 14(a) is a cross-sectional view of a semiconductor device according to a ninth embodiment, having a buried insulating film formed over the entire isolation region and FIG. 14(b) is an enlarged cross-sectional view of the isolation region for illustrating the wiring-to-substrate capacitance in the semiconductor device;

FIGS. 15(a) to 15(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to the ninth embodiment;

FIGS. 16(a) to 16(i) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a tenth embodiment;

FIGS. 17(a) to 17(f) are cross-sectional views illustrating the first half of a process of manufacturing a semiconductor device according to an eleventh embodiment;

FIGS. 18(a) to 18(d) are cross-sectional views illustrating the second half of the process of manufacturing the semiconductor device according to the eleventh embodiment;

FIG. 19 is a cross-sectional view of a conventional semiconductor device;

FIGS. 20(a) to 20(g) are cross-sectional views illustrating a process of manufacturing the conventional semiconductor device; and

FIG. 21 is a cross-sectional view for illustrating the wiring-to-substrate capacitance in each of a conventional trench-isolated semiconductor device and a conventional LOCOS-isolated semiconductor device.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to the drawings, the embodiments of the present invention will be described.

(First Embodiment)

FIG. 1(a) is a cross-sectional view of a semiconductor device having a MOSFET according to a first embodiment. As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as the MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Each of the semiconductor portions 9 formed in the isolation region 7 is provided with an impurity diffusion layer 21 into which an N-type impurity of the conductivity type opposite to that of the silicon substrate 1 has been introduced, so that a PN junction 22 is formed between the impurity diffusion layer 21 and the silicon substrate 1. The PN junction 22 is positioned at a level between those of the top and bottom faces of the trench portions

8.

FIG. 1(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance in the isolation region 7 of the semiconductor device according to the present embodiment. As shown in the drawing, the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment includes the components of capacitances Ca1 and Ca2, similarly to the wiring-to-substrate capacitance of the conventional semiconductor device shown in FIG. 21(a). Moreover, since the PN junction 22 is formed in each of the semiconductor portions 9, another capacitance Cj1 is added in series to the capacitance Ca1. Hence, the total wiring-to-substrate capacitance Cjt is represented by the following equation (3):

$$C_{jt} = \sum \{ (C_{a1} \times C_{j1}) / (C_{a1} + C_{j1}) \} + \sum C_{a2} \quad \dots (3),$$

which is smaller than the total capacitance Cat represented by the equation(1). Accordingly, the following inequality (4) is satisfied(4):

$$C_{jt} < C_{at} \quad \dots (4).$$

Thus, the wiring-to-substrate capacitance can be reduced in the semiconductor device according to the present embodiment owing to the PN junction 22 present in each of the dummy semiconductor portions 9 of the isolation region 7, which increases the operating speed of the semiconductor device.

A description will be given next to a method of manufacturing a semiconductor device according to the present

embodiment. FIGS. 2(a) to 2(g) are cross-sectional views showing the structure of the semiconductor device having the NMOSFET according to the present embodiment in the manufacturing process therefor.

5 In the step shown in FIG. 2(a), the thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

10 In the step shown in FIG. 2(b), the plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active 6 region by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and
15 trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The
20 trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 2(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

25 In the step shown in FIG. 2(d), the silicon oxide film 23

is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The
5 buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wires and the silicon substrate.

10 In the step shown in FIG. 2(e), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wires 10 by using a known technique. The gate electrode 4 and the polysilicon wires 10 can be formed simultaneously by using a common mask.

15 In the step shown in FIG. 2(f), arsenic ions 25 are implanted not only into the active region 6 but also into the entire isolation region 7. As a result, the NMOSFET having the source/drain regions 5 is formed in the active region 6. On the other hand, an N-type impurity diffusion layer 31 is formed in each of the
20 dummy semiconductor portions 6 of the isolation region 7, resulting in a PN junction 32 formed between the N-type impurity diffusion layer 31 and the P-type silicon substrate 1. The present embodiment is characterized in that the PN junction 32 is positioned between the top and bottom faces of the buried trench
25 portions 8.

In the step shown in FIG. 2(g), the silicon oxide film is deposited to form the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

In the case of providing the MOSFET in the active region as provided in accordance with the manufacturing method of the present embodiment, the PN junction 22 in each of the semiconductor portions 9 can be formed easily through the implantation of ions for forming the source/drain regions 5, so that manufacturing cost is not increased.

Although the present embodiment has described the case of using the P-type silicon substrate, it will be appreciated that the same effects as achieved in the present embodiment are also achieved in the case of using an N-type silicon substrate by introducing a P-type impurity into the upper portions of the semiconductor portions located between the individual trench portions and thereby forming the PN junctions between the resulting P-type impurity diffusion layers and the N-type silicon substrate.

Although the formation of the PN junctions 32 in the dummy semiconductor portions 9 of the isolation region 7 has been performed simultaneously with the formation of the source/drain regions 5 in the manufacturing method of the present embodiment, the formation of the dummy semiconductor portions 9 may be preformed at any stage of the process of manufacturing the semiconductor device, provided that the PN junctions can be formed

in the dummy semiconductor portions.

(Second Embodiment)

FIG. 3 is a cross-sectional view of a semiconductor device according to a second embodiment.

5 As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is
10 formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided
15 a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

20 Each of the semiconductor portions 9 formed in the isolation region 7 is provided with an impurity diffusion layer 31 into which an N-type impurity of the conductivity type opposite to that of the impurity introduced into the silicon substrate 1 has been introduced, so that a PN junction 32 is formed between the impurity
25 diffusion layer 31 and the silicon substrate 1. The PN junction

32 is positioned at a level lower than the bottom faces of the trench portions 8.

The wiring-to-substrate capacitance in the isolation region 7 of the present embodiment is represented by the following equation (5):

$$C_{jt} = \Sigma \{ (C_{a1} \times C_{j1}) / (C_{a1} + C_{j1}) \} + \Sigma \{ (C_{a2} \times C_{k1}) / (C_{a2} + C_{k1}) \} \quad \dots (5),$$

which is smaller than the total capacitance C_{at} represented by the equation (1). In the foregoing equation (5), C_{k1} represents the capacitance between the bottom face of the trench portion 8 and the PN junction 32. Hence, the following inequality (6) is satisfied, similarly to the first embodiment:

$$C_{jt} < C_{at} \quad \dots (6).$$

Thus, the wiring-to-substrate capacitance can also be reduced in the semiconductor device according to the present embodiment since the PN junction 32 is present in each of the dummy semiconductor portions 9 of the isolation region 7, similarly to the first embodiment, so that the operating speed of the semiconductor device is increased. In particular, the present embodiment can reduce the wiring-to-substrate capacitance in the entire isolation region containing not only the semiconductor portions 9 but also the trench portions, so that the effect of increasing the operating speed is remarkable.

Although it is difficult to form the PN junction 32 as formed in the present embodiment through the implantation of impurity

ions for forming the source/drain regions of the MOSFET, the impurity concentration and the depth of ionic penetration into the substrate can be controlled arbitrarily, so that a higher effect of reducing the capacitance is achieved. In particular, 5 since the PN junction 32 is positioned at a level lower than the bottom faces of the trench portions 8, a higher effect of reducing the capacitance is achieved.

Although the present embodiment has described the case of using the P-type silicon substrate, an N-type silicon substrate 10 may also be used instead. In this case, a PN junction can be formed by introducing a P-type impurity into the semiconductor portions and thereby forming an impurity diffusion layer, so that the same effects as achieved in the present embodiment are achieved.

(Third Embodiment)

15 FIG. 4 is a cross-sectional view of a semiconductor device according to a third embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made 20 of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and 25 not serving as active regions. On one of the trench portions 8

formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Each of the dummy semiconductor portions 9 formed in the isolation region 7 is provided with a P-type impurity diffusion layer 41 and an N-type impurity diffusion layer 42, which are arranged in this order from the surface of the silicon substrate. As a result, a first PN junction 43 is formed between the P-type impurity diffusion layer 41 and the N-type impurity diffusion layer 42, while a second PN junction 44 is formed between the N-type impurity diffusion layer 42 and the P-type silicon substrate 1. The first and second PN junctions 43 and 44 are positioned at levels between the top and bottom faces of the trench portions 8.

If respective junction capacitances in the P-type and N-type impurity diffusion layers 41 and 42 are designated at C_{j1} and C_{j2} , a total wiring-to-substrate capacitance C_{jt} in the semiconductor device according to the present embodiment is represented by the following equation (7):

$$C_{jt} = \sum \{1/[(1/C_{a1}) + (1/C_{j1}) + (1/C_{j2})]\} + \sum C_{a2} \quad \dots (7),$$

which is smaller than the total capacitance C_{at} of the semiconductor device according to the first embodiment represented by the equation (1). Hence, the following equation

(8) is satisfied:

$$C_{jt} < C_{at} \quad \dots (8).$$

Since the present embodiment has provided the plurality of PN junctions 43 and 44 in the respective dummy semiconductor portions of the isolation region 7, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions 9 of the semiconductor device can be represented by the capacitance obtained by connecting in series the respective capacitances in the P-type and N-type impurity diffusion layers 41 and 42 to the capacitance in the interlayer insulating film. Consequently, the wiring-to-substrate capacitance of the semiconductor device can further be reduced than in the first embodiment, resulting in the semiconductor device operating at a higher speed.

Although the present embodiment has described the case where the two PN junctions 43 and 44 are formed of the two impurity diffusion layers, if three or more PN junctions are formed of three or more impurity diffusion layers, the total wiring-to-substrate capacitance can be represented in the same fashion as represented by the equation (7). For example, if m PN junctions (m is an integer equal to or more than 3) are formed in each of the dummy active regions 9 and n PN junctions (n is an integer equal to or more than 3) are formed immediately under the trench portion 8, the total wiring-to-substrate capacitance C_{jt} is represented by the following equation (9):

$$C_{jt} = \sum \{1/[(1/C_{a1}) + \sum (1/C_{jm})]\} \\ + \sum \{1/[(1/C_{a2}) + \sum (1/C_{jn})]\} \quad \dots (9),$$

which is smaller than the total capacitance C_{at} represented by the equation (1). Hence, the following inequality (10) is

5 satisfied:

$$C_{jt} < C_{at} \quad \dots (10).$$

In the case of using the structure, the wiring-to-substrate capacitance can be reduced significantly since not only the capacitance component in the region containing the semiconductor

10 portions of the isolation region 7 but also the capacitance component in the region containing the trench portions thereof is also reduced.

(Fourth embodiment)

FIG. 5 is a cross-sectional view of a semiconductor device

15 according to a fourth embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation

20 region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench

25 portions 8 formed in the isolation region 7, there is provided

a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. In addition, a dummy gate 51 composed of a polysilicon film formed simultaneously with the gate electrode 4 extends continuously over the semiconductor portions 9 and trench portions 8. Over the dummy gate 51, the polysilicon wire 10, and a surface of the silicon substrate (except for the active region), a silicon oxide film 52 and a high resistor film 53 composed of a polysilicon film are further formed in layers. The dummy gate 51 has been formed by patterning a first-layer polysilicon film used commonly to form the gate electrode 4 and the polysilicon wire 10 so that it is at a given distance from each of the gate electrode 4 and the polysilicon wire 10. The polysilicon film composing the high resistor film 53 has a sheet resistance film higher than that of the first-layer polysilicon film composing the gate electrode 4 and the like and an impurity concentration of $1 \times 10^{20} \text{ cm}^{-3}$ or less. The sheet resistance of the dummy gate 51 can also be held high by covering the isolation region with a resist film or the like during the implantation of an impurity into the active region.

In the semiconductor device according to the present embodiment, it is sufficient to consider the capacitance between the wiring and high resistor film instead of the capacitance between the wiring and substrate. In this case, since the resistance of the polysilicon film composing the high resistor film 53 is high, a voltage drop occurs between the top face of

the high resistor film 53 and the surface of the semiconductor substrate 1. Accordingly, the voltage applied to the top and bottom faces of the interlayer insulating film is reduced, though the capacitance of the interlayer insulating film 12 remains unchanged. Since the amount of charge accumulated in the top and bottom faces of the interlayer insulating film 12 decreases in direct proportion to the voltage applied thereto, the time required for charging or discharging between the wiring and high resistor is reduced, resulting in the semiconductor device operating at a higher speed.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 6(a) to 6(h) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 6(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 6(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity

obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 6(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 6(d), the silicon oxide film 23 is polished by a CMP process. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form a plurality of buried trench portions 8 each filled with a silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wires and the silicon substrate.

In the step shown in FIG. 6(e), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wires 10 by using a known technique. During the process, the dummy gate 51 is formed

simultaneously with the gate electrode 4 and the polysilicon wire 10 and at a given distance from each of the gate electrode 4 and the polysilicon wire 10, so that the dummy gate 51 neither cross nor contact the gate electrode 4 and the polysilicon wire 10. The gate electrode 4, the polysilicon wire 10, and the dummy gate 51 can be formed simultaneously by using a common semiconductor mask. The dummy gate 51 has a sheet resistance higher than those of the gate electrode 4 and polysilicon wire 10, which are used as interconnections, and has an impurity concentration adjusted to be 1×10^{20} atoms \cdot cm^{-3} or lower by ion implantation or the like.

In the step shown in FIG. 6(f), the silicon oxide film 52 and the high resistor film 53 made of polysilicon are formed over the isolation region 7. The high resistor film 53 has a sheet resistance higher than those of the gate electrode 4 and polysilicon wires 10 and has an impurity concentration adjusted to be 1×10^{20} atoms \cdot cm^{-3} or lower by ion implantation or the like. The silicon oxide film 52 and the high resistor film 53 are formed to provide a MIM capacitor and a resistor.

In the step shown in FIG. 6(g), a resist mask 55 covering at least the isolation region 7 is formed and arsenic ions 25 are implanted into the active region 6 to form the NMOS having the source/drain regions 5. During the process, arsenic ions are not implanted in the isolation region 7.

In the step shown in FIG. 6(h), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by

a metal wire 13 formed thereon.

In the semiconductor device according to the present embodiment, it is sufficient to consider the capacitance between the wiring and high resistor film instead of the capacitance between the wiring and substrate. In this case, since the resistance of the polysilicon film composing the high resistor film 53 is high, a voltage drop occurs between the top face of the high resistor film 53 and the surface of the semiconductor substrate 1. Accordingly, the voltage applied to the top and bottom faces of the interlayer insulating film is reduced, though the capacitance of the interlayer insulating film 12 remains unchanged. Since the amount of charge accumulated in the top and bottom faces of the interlayer insulating film 12 decreases in direct proportion to the voltage applied thereto, the time required for charging or discharging between the wiring and high resistor is reduced, resulting in the semiconductor device operating at a higher speed.

The high-resistance film 53 according to the present embodiment can be formed easily at low cost by patterning the same film as composing, e.g., the high resistor film of the resistor element and local wiring. Instead of forming the dummy gate 51, it is possible to form films corresponding to the high resistor film 53, the silicon oxide film 52, and the dummy gate 51 from three films composing the upper-layer film, capacitor insulating film, and lower-layer film composing the MIM capacitor formed

anywhere on the semiconductor substrate.

It is also possible to increase the operating speed of the semiconductor device by reducing the time required for charging or discharging without forming either of the dummy gate 51 and
5 the high resistor film 53 as well as the silicon oxide film 52.

Although the description has been given to the case where the high resistor film 53 composed of the polysilicon film and the silicon oxide film 52 are stacked in layers on the isolation region 7, similar effects can also be achieved in the case of using
10 an amorphous silicon film or a silicon nitride film instead of the polysilicon film. In particular, the use of an insulating film composed of a silicon oxide film allows a reduction in total capacitance and a further increase in the operating speed of the semiconductor device.

15 (Fifth Embodiment)

FIG. 7 is a cross-sectional view of a semiconductor device according to a fifth embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as
20 a MOSFET composed of: a gate oxide film 2; a gate electrode 4; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor
25 portions 9 provided between the individual trench portions 8 and

not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate electrode 4.

In the present embodiment, the gate electrode 4 consists of a lower-layer portion 4a made of a first conductor film composed of a polysilicon film or the like and an upper-layer portion 4b made of a second conductor film composed of a tungsten film or the like. In the isolation region 7, there is provided a dummy gate 51 consisting of a lower-layer portion 51a composed of the same first conductor film as composing the lower-layer portion 4a of the gate electrode 4 and an upper-layer portion 51b composed of the same second conductor film composing the upper-layer portion 4b of the gate electrode 4. The lower-layer portion 51a of the dummy gate 51 has a top surface at the same level as the top face of each of the trench portions 8, so that planarization is achieved between the lower-layer portion 51a and the trench portions 8. The polysilicon wire 10 is composed only of the second conductor film composing the upper-layer portion 4b of the gate electrode 4. The dummy gate 51 has been formed at a given distance from each of the gate electrode 4 and polysilicon wire 10 so as to improve pattern accuracy in a photolithographic process in accordance with a line-and-space relationship. There are also provided an interlayer insulating film 12 composed of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

In accordance with a process of manufacturing the semiconductor device according to the present embodiment, the structure of the semiconductor device as shown in FIG. 7 can be implemented by the following procedure, though the drawing thereof is omitted here.

First, the gate insulating film and the first conductor film composed of a polysilicon film or the like are deposited on the semiconductor substrate, which are partially opened to form trenches. Thereafter, an insulating film is deposited on the substrate to fill in the trenches for planarization, thereby forming trench portions. Subsequently, the second conductor film of tungsten or the like is deposited on the planarized substrate and patterned to form the gate electrode 4, the dummy gate 51, and the polysilicon wires 10. After that, the interlayer insulating film 12 and the metal wire 13 can be formed by a well-known method.

In the present embodiment also, the operating speed can be increased by reducing the amount of charge accumulated in the top and bottom faces of the interlayer insulating film, similarly to the fourth embodiment. In the semiconductor device having such a structure as used in the present embodiment, the upper-layer portion 4b of the gate electrode 4 is typically composed of a low resistor film composed of silicide or the like. However, since the wiring-to-substrate voltage is also applied in series to the upper-layer and lower-layer portions 4b and 4a, the amount of

charge is effectively reduced by a voltage drop and the operating speed of the semiconductor device is increased remarkably.

Although the present embodiment has not used such a high resistor film as used in the fourth embodiment, it will be appreciated that a high resistor film may be provided over the dummy gate with an insulating film interposed therebetween.

(Sixth Embodiment)

FIG. 8 is a cross-sectional view of a semiconductor device according to a sixth embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

In the isolation region 7, inter-trench insulating films

61 each composed of a silicon oxide film and surrounded by the trench portions 8 are formed to overlie the dummy semiconductor portions 9 and underlie the interlayer insulating film 12. The top faces of the inter-trench insulating films 61 are at the same level as the top faces of the buried trench portions 8, while the bottom faces thereof are at a level between the top and bottom faces of the buried trench portions 8.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 9(a) to 9(i) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 9(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 9(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided

to form at least one projecting portion surrounded by the trenches
14. The semiconductor portions 9 may be considered as dummy
active regions which do not function as active regions. The
trenches include one formed in a position immediately under the
5 polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 9(c), a silicon oxide film 23 is
deposited over the entire surface of the substrate to fill in the
trenches 14.

In the step shown in FIG. 9(d), the silicon oxide film 23
10 is polished by a CMP method. Subsequently, the silicon nitride
film 22 and the silicon oxide film 21 are removed selectively to
form the plurality of buried trench portions 8 each filled with
the silicon oxide film and having a planarized surface. The
buried trench portions 8 include: buried trench portions 8a
15 functioning as isolation; buried trench portions 8b forming the
dummy semiconductor portions 9; and buried trench portions 8c for
providing insulation between the polysilicon wires and the
silicon substrate.

In the step shown in FIG. 9(e), the semiconductor portions
20 of the isolation region 7 are subjected to dry etching for forming
trenches 62.

In the step shown in FIG. 9(f), a silicon oxide film is filled
in each of the trenches 62 to form the inter-trench insulating
film 61.

25 In the step shown in FIG. 9(g), there are formed the gate

oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 and the polysilicon wire 10 can be formed simultaneously by using a common semiconductor mask.

5 In the step shown in FIG. 9(h), arsenic ions 25 are implanted from above to form the NMOSFET having the source/drain regions 5 in the active region 6. Although the arsenic ions 25 are also implanted into the isolation region 25 during the process, no trouble occurs. In the case of using a resist mask covering a
10 region to be formed with a PMOSFET, however, the isolation region 7 may be covered with the resist mask.

In the step shown in FIG. 9(i), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

15 In the semiconductor device according to the present embodiment, the inter-trench insulating films 61 each composed of the silicon oxide film are formed over the dummy semiconductor portions 9 of the isolation region 7 and under the interlayer insulating film 12 to be surrounded by the buried trench portions
20 8. The top faces of the inter-trench insulating films 61 are at the same level as the top faces of the buried trench portions 8, while the bottom faces thereof are at a level between the top and bottom faces of the buried trench portions 8.

Thus, in the semiconductor device according to the present
25 embodiment, the inter-trench insulating films 61 are formed by

filling the silicon oxide films in the respective dummy semiconductor portions 9 that have been lowered in level, so that the distance between the wiring and the substrate is longer than in the conventional semiconductor device shown in FIG. 19. Since
5 the wiring-to-substrate capacitance decreases in inverse proportion to the distance, the wiring-to-substrate capacitance is smaller in the semiconductor device according to the present embodiment than in the conventional semiconductor device, resulting in a higher operating speed.

10 Although the present embodiment has described the case where the silicon oxide film is buried in each of the semiconductor portions, similar effects can also be achieved if an insulating film composed of a silicon nitride film is used.

Although the semiconductor portions 9 have been lowered in
15 level and filled with the silicon oxide films prior to the formation of the gate electrode, the method of manufacturing a semiconductor device according to the present invention is not limited to such an embodiment. The same effects as achieved in the present embodiment can also be achieved if the steps of
20 lowering the semiconductor portions 9 in level and filling the silicon oxide films therein are performed after the formation of the gate electrode or prior to the formation of trench isolation.
(Seventh Embodiment)

FIG. 10 is a cross-sectional view of a semiconductor device
25 according to a seventh embodiment.

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As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

In upper portions of the dummy semiconductor portions 9 of the isolation region 7, oxygen atoms have been introduced by ion implantation or the like to form high resistor portions 71 each composed of a high-resistance silicon layer. Although the bottom faces of the high resistor portions 71 are at a level between the top and bottom faces of the trench portions 8, they may be positioned at a level lower than the bottom faces of the trench portions 8.

A description will be given next to a method of manufacturing a semiconductor device according to the present

52

embodiment. FIGS. 11(a) to 11(h) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

5 In the step shown in FIG. 11(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

10 In the step shown in FIG. 11(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and
15 trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The
20 trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 11(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

25 In the step shown in FIG. 11(d), the silicon oxide film 23

is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The

5 buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

10 In the step shown in FIG. 11(e), a resist mask 73 covering the active region 6 is formed and oxygen ions 72 are implanted only into the isolation region 7 to form the high resistor portions 71 in the outermost surface of the silicon substrate, in which the oxygen ions have been introduced as an impurity in the

15 semiconductor portions 9 of the isolation region 7.

In the step shown in FIG. 11(f), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 and the polysilicon wire 10 can

20 be formed simultaneously by using a common semiconductor mask.

In the step shown in FIG. 11(g), arsenic ions are implanted from above the substrate to form the NMOSFET having the source/drain regions 5 in the active region 6. Although the arsenic ions 25 are also implanted into the isolation region 7

25 during the process, no trouble occurs. In the case of using a

resist mask covering a region to be formed with a PMOSFET, however, the isolation region 7 may be covered with the resist mask.

In the step shown in FIG. 11(h), a silicon oxide film is formed as the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

The semiconductor device according to the present embodiment is characterized in that the oxygen atoms have been introduced into the upper portions of the semiconductor portions 9 of the isolation region 7 by ion implantation or the like to form the high resistor portions 71 each composed of a high-resistance silicon layer. Although the bottom faces of the high resistor portions 71 are at a level between the top and bottom faces of the buried trench portions 8, they may be positioned at a level lower than the bottom faces of the buried trench portions 8.

Since the high resistor portions 71 each composed of a high-resistance silicon layer have been formed in the dummy semiconductor portions 9 of the silicon substrate, a voltage drop occurs in the high resistor portions 71 of the silicon substrate when a voltage is placed between the wiring and the substrate. Consequently, a potential difference between the wiring and semiconductor portions 9 is reduced so that the amount of charge is reduced in direct proportion to the placed voltage, though the capacitance of the interlayer insulating film 12 between the wiring and the semiconductor portions 9 is equal to that of the

interlayer insulating film 12 in the conventional semiconductor device shown in FIG. 19. Accordingly, the time required for charging or discharging is reduced and the operating speed of the semiconductor device is increased.

5 Although the present embodiment has described the case where oxygen atoms are introduced as an impurity into the dummy semiconductor portions 9, similar effects can be achieved if nitrogen atoms are introduced.

10 Although the high resistor portions are formed prior to the formation of the gate electrode in the present embodiment, they may be formed at any stage of the process of manufacturing the semiconductor device provided that oxygen atoms can be introduced into the semiconductor portions.

(Eighth Embodiment)

15 FIG. 12 is a cross-sectional view of a semiconductor device according to an eighth embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made
20 of a polysilicon film; sidewalls 3 formed on the side faces of the gate electrode 4 and composed of silicon oxide films; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an
25 insulating material and with dummy semiconductor portions 9

provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Over the dummy semiconductor portions 9 and trench portions 8 of the isolation region 7, an underlying insulating film 81 made of a silicon oxide film has been formed simultaneously with the sidewalls on the side faces of the gate electrode 4. The underlying insulating film 81 has been formed to cover the entire polysilicon wire 10.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 13(a) to 13(i) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 13(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 13(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate

1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity
5 obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy
10 active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 13(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in
15 the trenches 14.

In the step shown in FIG. 13(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with
20 the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon
25 substrate.

In the step shown in FIG. 13(e), there are formed the gate oxide film 2, the gate electrode 4 made of polysilicon, and the polysilicon wire 10 by using a known technique. The gate electrode 4 can be formed simultaneously with the polysilicon wire 10 by using a common semiconductor mask.

In the step shown in FIG. 13(f), a silicon oxide film 82 is deposited over the entire surface of the substrate, followed by a resist mask 84 formed thereon to cover the isolation region 7.

In the step shown in FIG. 13(g), a silicon oxide film 82 is removed selectively by anisotropic dry etching using the resist mask 84 to form an underlying insulating film 81 over the isolation region 7, while the sidewalls are formed on the side faces of the gate electrode 4. The polysilicon wire 10 is completely covered with the underlying insulating film 81.

In the step shown in FIG. 13(h), arsenic ions 25 are implanted from above to form the NMOSFET having the source/drain regions 5 in the active region 6. Although the arsenic ions are also implanted into the isolation region 7 during the process, no trouble occurs. However, in the case of using a resist mask covering a region to be formed with a PMOSFET, the isolation region 7 may be covered with the resist mask.

In the step shown in FIG. 13(i), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

5 The semiconductor device according to the present embodiment is characterized in that the underlying insulating film 81 composed of the silicon oxide film is formed simultaneously with the sidewalls on the side faces of the gate electrode 4 to extend over the dummy semiconductor portions 9 and buried trench portions 8 of the isolation region 7. The resulting underlying insulating film 81 covers the entire polysilicon wire 10.

10 Thus, in the semiconductor device according to the present embodiment, the underlying insulating film 81 composed of the silicon oxide film is present over the isolation region 7, so that the distance between the wiring and the substrate is longer than in the conventional semiconductor device shown in FIG. 19. Since the wiring-to-substrate capacitance decreases in inverse proportion to the distance, the wiring-to-substrate capacitance is reduced in the semiconductor device according to the present embodiment, resulting in a higher operating speed.

15 Although the present embodiment has described the case where the underlying insulating film 81 is composed of the silicon oxide film, similar effects can also be achieved if an insulating film composed of a silicon nitride film is used.

20 Although the present embodiment has described the case where the underlying insulating film is composed of a single-layer film, the underlying insulating film may be composed of a multi-layer film. For example, in the case where the sidewalls

consist of L-shaped portions extending over the side faces of the gate electrode and the substrate and of upper wedge-shaped portions or, alternatively, the sidewalls are provided along with an on-gate protective film, the underlying insulating film should
5 be composed of a multi-layer film. It will be appreciated that, in that case also, the same effects as achieved in the present embodiment are achieved.

(Ninth Embodiment)

FIG. 14(a) is a cross-sectional view of a semiconductor
10 device according to a ninth embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation
15 region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench
20 portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal
25 wire 13 formed on the interlayer insulating film 12.

Under the dummy semiconductor portions 9 and the trench portions 8, a buried insulating film 91 composed of a silicon oxide film is formed in contact with the bottom faces of the trench portions 8. As a result, the side faces of the semiconductor portions 9 are in contact with the trench portions 8, while the bottom faces thereof are in contact with the buried insulating film 91.

FIG. 14(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment. In the semiconductor device according to the present embodiment, since the buried insulating film 91 composed of the silicon oxide film is formed in the silicon substrate, the capacitance C_{ij} becomes a half of the capacitance C_{j1} shown in FIG. 1(b) or less (T. Nishimura and Y. Inoue: Proceedings of VLSI TECHNOLOGY WORKSHOP ON "WHAT IS THE FUTURE OF SOI?" (1995) p.123).

Therefore, the total wiring-to-substrate capacitance C_{ijt} of the semiconductor device is represented by the following equation (11):

$$C_{ijt} = \{(C_{a1} \times C_{ij}) / (C_{a1} + C_{ij})\} + \sum C_{a2} \quad \dots (11),$$

which is smaller than the total capacitance C_{jt} represented by the equation (3). Accordingly, the following inequality (12) is satisfied:

$$C_{ijt} < C_{jt} \quad \dots (12).$$

Hence,

Cijt < Cat

is derived from the relationship represented by the equation (4), so that the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment is reduced, resulting in the semiconductor device operating at a higher speed.

FIGS. 15(a) to 15(h) are cross-sectional views of the structure of the semiconductor device having the NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 15(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 15(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the

polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 15(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

5 In the step shown in FIG. 15(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The
10 buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

15 In the step shown in FIG. 15(e), a resist mask 92 covering the active region 6 is formed and oxygen ions 93 are implanted only into the isolation region 7 so that the buried insulating film 91 into which the oxygen atoms have been introduced as an impurity is formed. The buried insulating film 91 provides
20 insulation between the silicon substrate 1 and the semiconductor portions 9 in the isolation region 7. In this case, the buried insulating film 91 is connected to the respective side faces of each of the individual trench portions 8a to 8c and energy for implanting the oxygen ions is set such that the semiconductor
25 portions 9 are in the floating state.

In the step shown in FIG. 15(f), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 may be formed simultaneously with the polysilicon wire 10 by using a common semiconductor mask.

In the step shown in FIG. 15(g), a resist mask 95 is formed to cover the isolation region 7 and arsenic ions 25 are implanted into the active region 6 to form the NMOSFET having the source/drain regions 5. In this case, no implantation is performed with respect to the isolation region 7.

In the step shown in FIG. 15(h), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

In the semiconductor device formed by the manufacturing method according to the present embodiment, the buried insulating film 91 composed of the silicon oxide film is formed under the dummy semiconductor portions 9 and the buried trench portions 8 to be in contact with the bottom faces of the buried trench portions 8. As a result, the side faces of the semiconductor portions 9 are in contact with the buried trench portions 8, while the bottom faces thereof are in contact with the insulating film 91. Although the present embodiment has formed the buried insulating film by implanting oxygen ions prior to the formation of the gate electrode, the buried insulating film may be formed at any stage of the method of manufacturing the semiconductor device provided

that oxygen atoms can be introduced into the semiconductor portions.

(Tenth Embodiment)

The present embodiment will basically describe another
5 example of the manufacturing process shown in FIG. 14(b), which is for achieving the effect of capacitance reduction.

FIGS. 16(a) to 16(i) are cross-sectional views of the structure of a semiconductor device having an NMOSFET according to a tenth embodiment in the manufacturing process therefor.

10 In the step shown in FIG. 16(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on a P-type silicon substrate 1.

In the step shown in FIG. 16(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate
15 1. The trenches 14 include: trenches 14a formed to surround an active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and
20 trenches 14c for forming the polysilicon wires. In the isolation region 7 also, semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent
25 step. In the step shown in FIG. 15(c), a silicon oxide film 23

is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 16(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 16(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively except for the portions overlying the active region 6 to form a plurality of buried trench portions 8 each filled with a silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 16(e), the semiconductor portions 9 of the isolation region 7 are subjected to dry etching for forming trenches 96.

In the step shown in FIG. 16(f), a silicon oxide film is deposited in each of the trenches 96 to form a buried insulating film 91, followed by a silicon film deposited thereon to form semiconductor portions 97 serving as dummy active regions. The buried insulating films 91 are in contact with the buried trench portions 8a to 8c.

In the step shown in FIG. 16(g), there are formed the gate

oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 may be formed simultaneously with the polysilicon wire 10 by using a common semiconductor mask.

5 In the step shown in FIG. 16(h), a resist mask 98 is formed to cover the isolation region 7 and arsenic ions 25 are implanted into the active region 6 to form the NMOSFET having source/drain regions 5. In this case, implantation may be performed with respect to the isolation region 7, though it is not performed
10 in the example.

In the step shown in FIG. 16(i), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

The manufacturing method according to the present
15 embodiment also enables the formation of a semiconductor device having the same structure as the semiconductor device according to the ninth embodiment, resulting in smaller wiring-to-substrate capacitance and a higher operating speed.

Although the present embodiment has grown the silicon oxide
20 films and the silicon films in the trenches 96 prior to forming the gate electrode, the silicon oxide films and the silicon films may be grown at any stage of the process of manufacturing the semiconductor device provided that they can be grown and buried in the trenches 96.

25 (Eleventh Embodiment)

The present embodiment will also basically describe still another example of the manufacturing process shown in FIG. 14(b), which is for achieving the effect of capacitance reduction.

FIGS. 17(a) to 17(f) and FIGS. 18(a) to 18(d) are cross-sectional views showing the structure of a semiconductor device having an NMOSFET according to an eleventh embodiment in the manufacturing process therefor.

In the step shown in FIG. 17(a), a trench 102 is formed in a region of a P-type silicon substrate 1 in which an isolation region is to be formed.

In the step shown in FIG. 17(b), a silicon oxide film is filled in the trench 102 to form an insulating film 101 so that the entire surface of the substrate is planarized.

In the step shown in FIG. 17(c), a silicon film 103 is epitaxially grown over the entire surface of the substrate. During the step, since single-crystal silicon is grown on single-crystal silicon in an active region 6, a semiconductor region having an excellent crystallographic property is formed therein, while a silicon film having an inferior crystallographic property is formed on the silicon oxide film in the isolation region 7. However, since the silicon film in the isolation region 7 does not function as an active region, the inferior crystallographic property thereof will not adversely affect the properties of the semiconductor device.

In the step shown in FIG. 17(d), a thin silicon oxide film

21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the silicon film 103.

In the step shown in FIG. 17(e), a plurality of trenches 14 each having a given width are formed in the substrate. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step. In forming the trenches 14, etching is performed till the surface of the buried insulating film 101 is exposed in the trenches 14.

In the step shown in FIG. 17(f), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 18(a), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form a plurality of buried trench portions 8 each filled with a

silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 18(b), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 is formed simultaneously with the polysilicon wire 10.

In the step shown in FIG. 18(c), arsenic ions 25 are implanted into the active region 6 to form source/drain regions 5 by using a resist mask 95 formed to cover the isolation region 7. The NMOSFET is formed by the foregoing process. Although arsenic ions 25 are not implanted in the isolation region 7 in the example, they may be implanted alternatively.

In the step shown in FIG. 18(d), a silicon oxide film is deposited to form an interlayer insulating film 12, followed by a metal wire 13 formed thereon.

The manufacturing method according to the present embodiment also enables the formation of a semiconductor device having the same structure as the semiconductor device according to the ninth embodiment, resulting in smaller wiring-to-substrate capacitance and a higher operating speed.

Although the present embodiment has formed the trench 102 in the silicon substrate 1 and buried the silicon oxide film therein to form a miniaturized gate electrode 4, the silicon oxide film may be formed directly on the isolation region without forming the trench if the semiconductor substrate inferior in planarity does not adversely affect the patterning of the gate during the formation of the gate electrode.

(Variations of Individual Embodiments)

Although the eighth embodiments of the present invention have been described, there are variations obtained by combining the individual embodiments with each other.

By way of example, the first embodiment used in combination with the second to eighth embodiments achieves a further reduction in wiring-to-substrate capacitance and a reduction in time required for charging or discharging, so that the resulting semiconductor device operates at a higher speed than in the case where each of the embodiments is used singly.

Thus, according to the present invention, the individual embodiments used in combination can achieve more remarkable effects than in the case where each of the embodiments is used singly.

Although each of the embodiments has used the NMOSFET as the element to be disposed in the active region 6, the present invention is not limited to such embodiments. The element includes an active element other than the MOSFET such as a bipolar

We claim:

1. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

5 a plurality of trench portions each formed in said isolation region and filled with an insulating material;

semiconductor portions interposed between said individual trench portions in said isolation region;

10 an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film; and

at least one PN junction formed in said semiconductor portions underlying said wire.

2. A semiconductor device according to claim 1, wherein said

15 PN junction includes a plurality of PN junctions formed in said semiconductor portions.

3. A semiconductor device according to claim 1, wherein said

active region is formed with an impurity diffusion region and a PN junction is formed at a bottom face of said impurity diffusion

20 region, the PN junction of said isolation region being positioned at a level lower than the PN junction of said active region.

4. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

25 a plurality of trench portions each formed in said isolation

region and filled with an insulating material;

semiconductor portions interposed between said individual trench portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film; and

a dielectric film interposed between at least said semiconductor portions of said isolation region and said interlayer insulating film.

5. A semiconductor device according to claim 4, wherein said dielectric film is an underlying insulating film interposed between said interlayer insulating film and said semiconductor portions and trench portions.

8. A semiconductor device according to claim 7, further comprising a gate electrode formed on the semiconductor substrate within said active region and sidewalls made of an insulating material and formed on both side faces of said gate electrode, wherein said underlying insulating film is formed of the same film as forming said sidewalls.

9. A semiconductor device according to claim 8, wherein said underlying insulating film is composed of a multilayer film.

8. A semiconductor device according to claim 4, wherein said dielectric film is formed in an upper portion of each of said semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top face of each

of said trench portions.

11⁶. A semiconductor device according to claim 4⁶, wherein said dielectric film is composed of at least one of a silicon oxide film and a silicon nitride film.

- 5 10. A semiconductor device comprising:
- a semiconductor substrate having an active region and an isolation region surrounding said active region;
- a plurality of trench portions each formed in said isolation region and filled with an insulating material;
- 10 semiconductor portions interposed between said individual trench portions in said isolation region;
- an interlayer insulating film formed to extend continuously over said active region and said isolation region;
- a wire formed on said interlayer insulating film; and
- 15 a buried insulating film formed in an inner portion of each of said semiconductor portions in said isolation region.
11. A semiconductor device comprising:
- a semiconductor substrate having an active region and an isolation region surrounding said active region;
- 20 a plurality of trench portions each formed in said isolation region and filled with an insulating material;
- semiconductor portions interposed between said individual trench portions in said isolation region;
- an interlayer insulating film formed to extend continuously
- 25 over said active region and said isolation region;

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a wire formed on said interlayer insulating film; an
a resistor film formed between said interlayer insulating
film and at least said semiconductor portions of said isolation
region.

5 12. A semiconductor device according to claim 11, wherein
said resistor film is an underlying resistor film formed to extend
continuously over said semiconductor portions and trench
portions.

10 13. A semiconductor device according to claim 12, further
comprising a resistor element formed on said semiconductor
substrate and having a high resistor film, wherein said underlying
resistor film is formed of the same film as composing the high
resistor film of said resistor element.

14 14. A semiconductor device according to claim 13, further
15 comprising an element having an electrode member composed of a
conductor film formed on the semiconductor substrate within said
active region, wherein said resistor film is composed of the same
material as composing said electrode member.

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20 15. A semiconductor device according to claim 12, further
comprising a FET having a gate electrode composed of a first
conductor film formed on the semiconductor portion within said
active region and a second conductor film deposited on said first
conductor film, wherein

25 a top surface of the first conductor film of said gate
electrode is at approximately the same level as a top surface of

each of said trench portions,

a region of said resistor film overlying each of said semiconductor portions is formed of the same two films as composing said first and second conductor films of said gate electrode, and

a region of said resistor film overlying each of said trench portions is composed of the same material as composing said first conductor film of said gate electrode.

10 16. A semiconductor device according to claim 11, wherein said resistor film is formed in an upper portion of each of said semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top surface of each of said trench portions.

15 17. A semiconductor device according to claim 16, wherein said resistor film is composed of a silicon film containing at least one of an oxygen atom and a nitrogen atom.

18. A semiconductor device according to claim 11, wherein said resistor film is composed of at least one of a polysilicon film and an amorphous silicon film.

20 19. A method of manufacturing a semiconductor device, comprising:

25 a first step of forming, in a semiconductor substrate having a substrate region of a first conductivity type, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said

isolation region into a plurality of dummy semiconductor portions;

5 a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

a third step of forming an element on said active region;

10 a fourth step of introducing an impurity containing at least an impurity of a second conductivity type into said dummy semiconductor portions of said isolation region to form at least one PN junction in said dummy semiconductor portions;

a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating film.

15 20. A method of manufacturing a semiconductor device according to claim 19, wherein said third and fourth steps include forming a gate electrode of a FET as said element on said active region, introducing the impurity of the second conductivity type into said active region and said dummy semiconductor portions,
20 and thereby forming source/drain regions of said FET, while forming said at least one PN junction in said dummy semiconductor portions.

21. A method of manufacturing a semiconductor device according to claim 19, wherein

25 said third step includes forming a gate electrode of a FET

as said element on said active region by using a first mask covering said isolation region and introducing the impurity of the second conductivity type into said active region to form source/drain regions of said FET and

5 said fourth step includes introducing the impurity containing at least the impurity of the second conductivity type into said dummy semiconductor portions by using a second mask covering said active region to form said at least one PN junction in said dummy semiconductor portions.

10 22. A method of manufacturing a semiconductor device, comprising:

 a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and second
15 trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

 a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

20 a third step of forming an element on said active region;

 a fourth step of forming a resistor film on each of said dummy semiconductor portions of said isolation region;

 a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

25 a sixth step of forming a wire on said interlayer insulating

film.

23. A method of manufacturing a semiconductor device according to claim 22, wherein said fourth step includes composing said resistor film of a film containing at least one of polysilicon and amorphous silicon.

24. A method of manufacturing a semiconductor device according to claim 22, wherein said fourth step includes composing said resistor film of a multilayer film constituted by two or more conductor films with at least an insulating film interposed therebetween.

25. A method of manufacturing a semiconductor device according to claim 22, wherein said fourth step includes introducing an impurity at a concentration of 1×10^{20} atoms \cdot cm^{-3} or lower into said resistor film.

26. A method of manufacturing a semiconductor device, comprising:

a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

a third step of forming an element on said active region;

a fourth step of implanting ions into an upper portion of each of said dummy semiconductor portions to form a high resistor portion therein;

5 a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating film.

27. A method of manufacturing a semiconductor device according to claim 26, wherein said fourth step includes
10 implanting ions containing at least an atom having an oxidizing function to form said high resistor portion.

28. A method of manufacturing a semiconductor device according to claim 26, wherein said fourth step includes
15 implanting ions containing at least an atom having a nitriding function to form said high resistor portion.

29. A method of manufacturing a semiconductor device, comprising:

a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate
20 region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench
25 portion and a second buried trench portion;

a third step of forming an element on said active region;
a fourth step of forming an underlying insulating film over
said dummy semiconductor portions of said isolation region;
a fifth step of forming an interlayer insulating film over
5 an entire surface of the substrate; and
a sixth step of forming a wire on said interlayer insulating
film.

30. A method of manufacturing a semiconductor device
according to claim 29, wherein said third step and said fourth
10 step include forming a gate electrode of a FET forming said element
on said active region, depositing a dielectric film on the
substrate, performing anisotropic etching with respect to the
dielectric film by using a mask covering said isolation region,
and thereby leaving sidewalls on both side faces of said gate
15 electrode, while leaving said underlying insulating film over
said dummy semiconductor portions.

31. A method of manufacturing a semiconductor device
according to claim 29, wherein said fourth step includes forming
said underlying insulating film of a dielectric film containing
20 at least silicon oxide.

32. A method of manufacturing a semiconductor device
according to claim 29, wherein said fourth step includes forming
said underlying insulating film of a dielectric film containing
at least silicon nitride.

25 33. A method of manufacturing a semiconductor device,

comprising:

5 a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

10 a third step of forming an element on said active region;

a fourth step of forming depressed portions by etching said dummy semiconductor portions and filling an insulating material in said depressed portions to form inter-trench insulating films each having a top face at the same level as respective top faces
15 of said first and second buried trench portions;

a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating film.

20 34. A method of manufacturing a semiconductor device according to claim 33, wherein said fourth step includes forming each of said inter-trench insulating films of a dielectric film containing at least silicon oxide.

25 35. A method of manufacturing a semiconductor device according to claim 33, wherein said fourth step includes forming

each of said inter-trench insulating films of a dielectric film containing at least silicon nitride.

36. A method of manufacturing a semiconductor device, comprising:

5 a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

10 a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

a third step of forming an element on said active region;

15 a fourth step of implanting oxygen ions into each of said dummy semiconductor portions to form a buried insulating film in an inner portion thereof;

a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

20 a sixth step of forming a wire on said interlayer insulating film.

37. A method of manufacturing a semiconductor device, comprising:

25 a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region

and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

5 a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

10 a third step of forming third trenches by etching said semiconductor portions and filling an insulating material in said third trenches to form buried insulating films each having a top face at a level lower than respective top faces of said first and second buried trench portions;

a fourth step of growing semiconductor films on said buried insulating films, with said active region covered with a mask member, to form dummy semiconductor portions;

a fifth step of forming an element on said active region;

15 a sixth step of forming an interlayer insulating film over an entire surface of the substrate; and

a seventh step of forming a wire on said interlayer insulating film.

20 38. A method of manufacturing a semiconductor device, comprising:

a first step of forming, in a semiconductor substrate having a substrate region, a first trench extending over an entire isolation region of said substrate region, while leaving an active region of said substrate region;

25 a second step of filling an insulating material in said

first trench to form a buried insulating film having a top face at the same level as a top face of said isolation region;

a third step of growing a semiconductor film over said active region and said buried insulating film;

5 a fourth step of forming, in the semiconductor substrate, a second trench for partitioning said semiconductor film and said substrate region into the active region and the isolation region and a third trench for partitioning the portion of the semiconductor film overlying said isolation region into a
10 plurality of dummy semiconductor portions;

a fifth step of filling an insulating material in each of said second and third trenches to form a first buried trench portion and a second buried trench portion;

a sixth step of forming an element on the portion of said
15 semiconductor film overlying said active region;

a seventh step of forming an interlayer insulating film over an entire surface of the substrate; and

an eighth step of forming a wire on said interlayer insulating film.

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ABSTRACT OF THE DISCLOSURE

The top surface of a P-type semiconductor substrate is partitioned into an active region to be formed with an element and an isolation region surrounding the active region. The
5 isolation region is composed of trench portions and dummy semiconductor portions. An interlayer insulating film is deposited on the substrate, followed by a wire formed thereon. In each of the semiconductor portions, an impurity diffusion layer is formed simultaneously with the implantation of ions into the
10 element so that a PN junction is formed between the impurity diffusion layer and the silicon substrate. A capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions is obtained by adding in series the capacitance in the impurity diffusion layer to the
15 capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. What results is a semiconductor device having lower total wiring-to-substrate capacitance and a higher operating speed.

COMBINED DECLARATION/POWER OF ATTORNEY
FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

_____, the specification of which

(check one) ☒ is attached hereto.

_____ was filed on _____ as
Application Serial No. _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
<u>8-314762</u> (Number)	<u>JAPAN</u> (Country)	<u>26/11/1996</u> (Day/Month/Year Filed)	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
<u>9-023844</u> (Number)	<u>JAPAN</u> (Country)	<u>06/02/1997</u> (Day/Month/Year Filed)	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/> Yes <input type="checkbox"/> No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)
(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)

I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Raphael V. Lupo (Reg. No. 28,363); Jack Q. Lever, Jr. (Reg. No. 28,149); Kenneth L. Cage (Reg. No. 26,151); Stanislaus Aksman (Reg. No. 28,562); Paul Devinsky (Reg. No. 28,553); Edward E. Kubasiewicz (Reg. No. 30,020), Michael E. Fogarty (Reg. No. 36,139); Brian E. Ferguson (Reg. No. 36,801); Robert W. Zelnick (Reg. No. 36,976); and Wilhlem F. Gadiano (Reg. No. 37,136).

Please address all correspondence and telephone calls to:

Kenneth L. Cage, Esquire
McDERMOTT, WILL & EMERY
1850 K STREET, N.W., SUITE 500
WASHINGTON, D.C. 20006
(202) 778-8300

PAYOR NO.
020277

The undersigned hereby authorizes the U.S. attorneys named herein to accept and follow instructions from Maeda Patent Office as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by the undersigned.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Takaaki UKEDA

Inventor's signature Takaaki Ukeda Date Nov. 18, 1997

Residence* Osaka, Japan Citizenship Japan

Post Office Address 6-2-205, Myokenzaka, Katano-shi, Osaka 576, Japan

Full name of second inventor Chiaki KUDO

Inventor's signature Chiaki Kudo Date Nov. 18, 1997

Residence* Kyoto, Japan Citizenship Japan

Post Office Address 108-D-504, Uji-hanpaku, Uji-shi, Kyoto 614, Japan

Full name of third inventor Toshiki YABU

Inventor's signature Toshiki Yabu Date Nov. 18, 1997

Residence* Osaka, Japan Citizenship Japan

Post Office Address 4-14-1, Nagaodai, Hirakata-shi, Osaka 573-01, Japan

* City and State, or City and Country for foreign inventors

09/469498

Fig. 1(a)

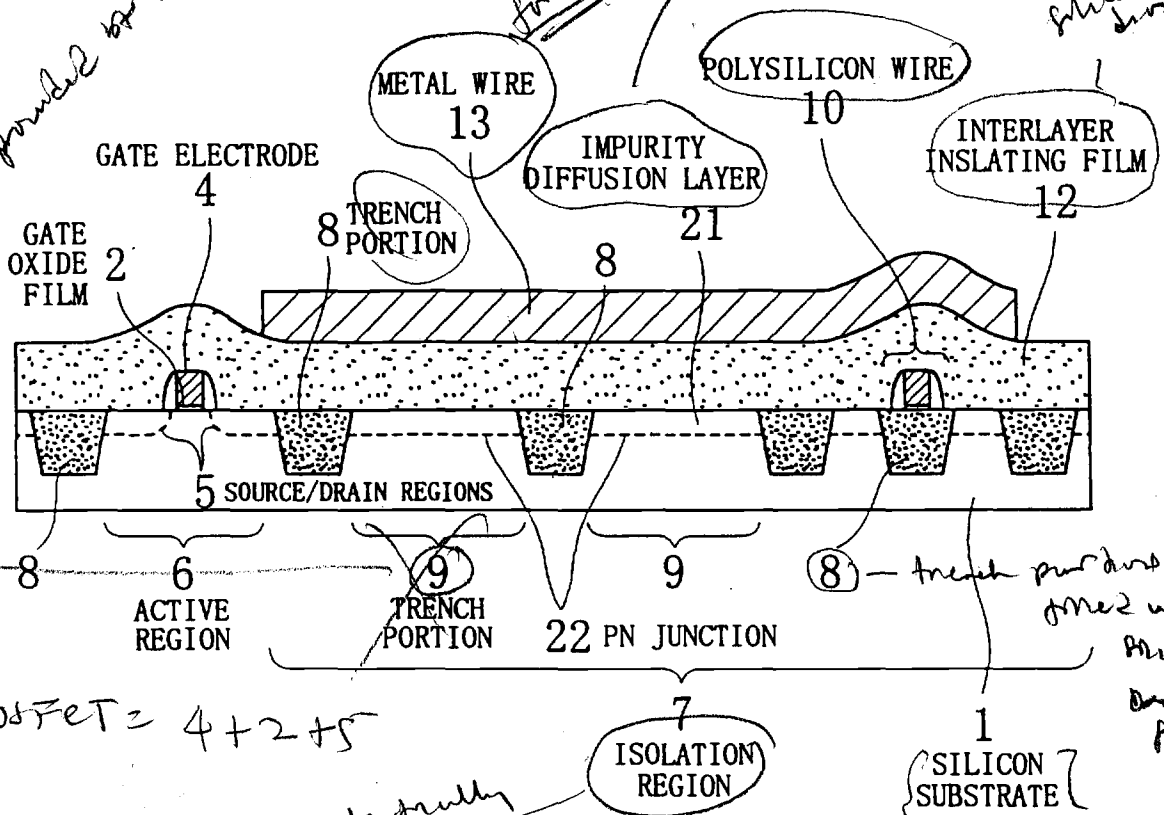
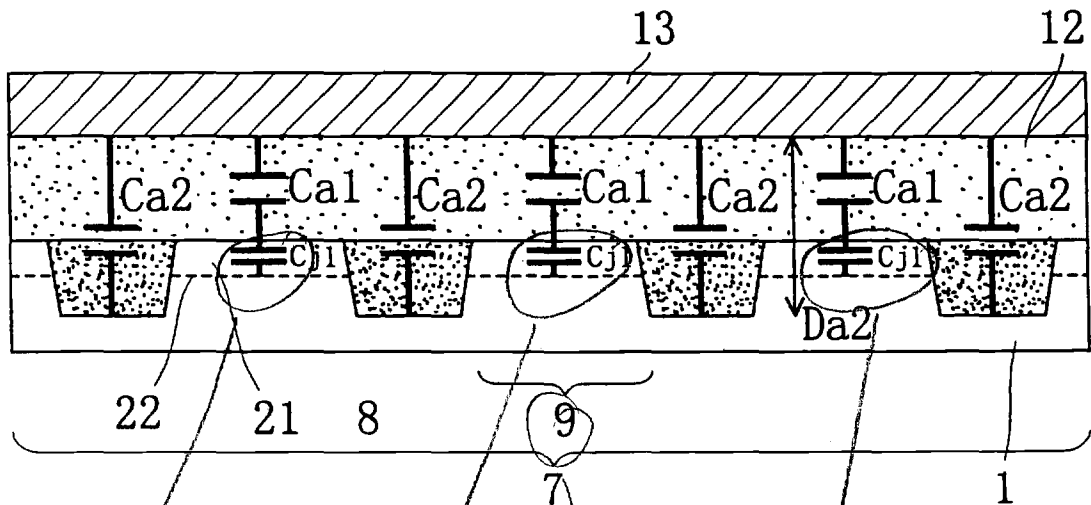


Fig. 1(b)



reduces the amount of dummy semiconductor portions added to the substrate

dummy semiconductor portions

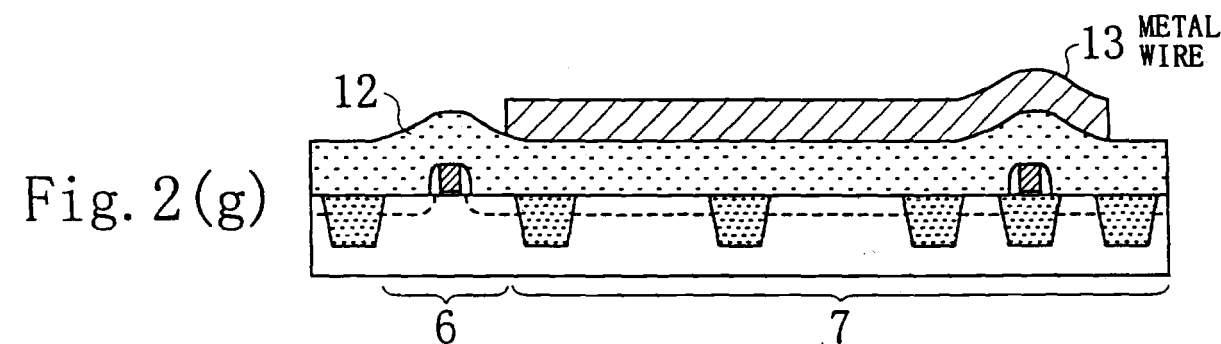
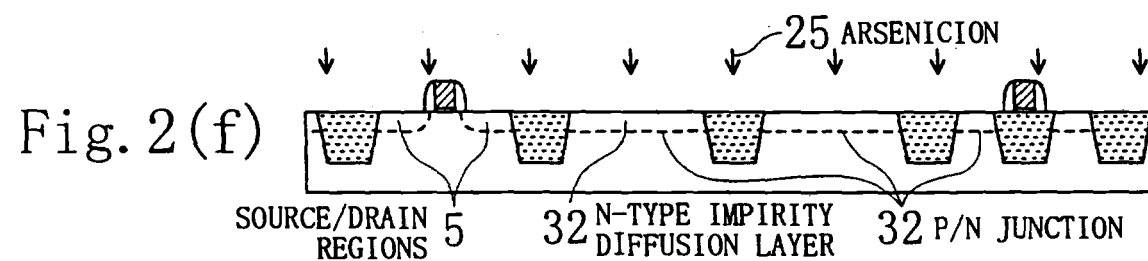
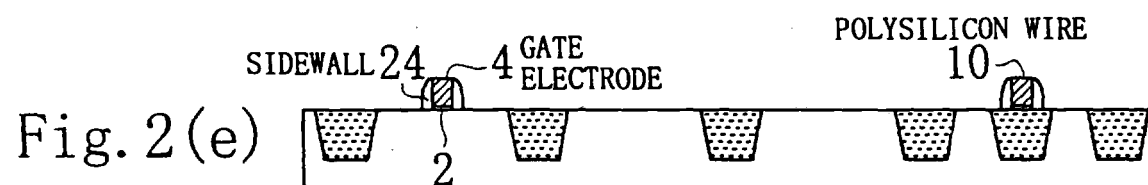
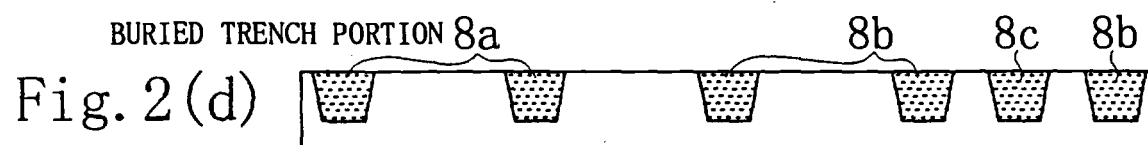
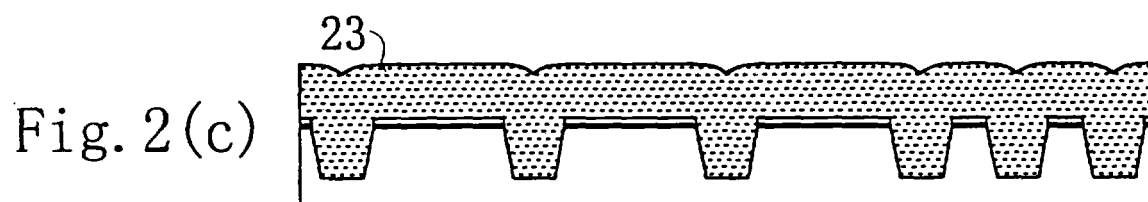
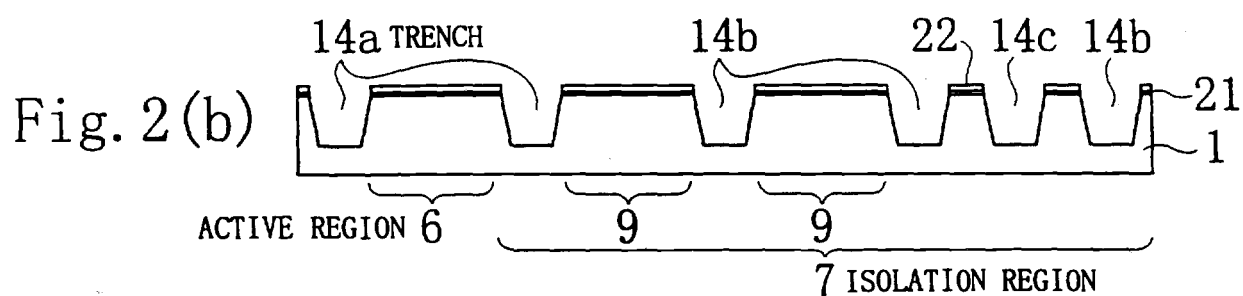
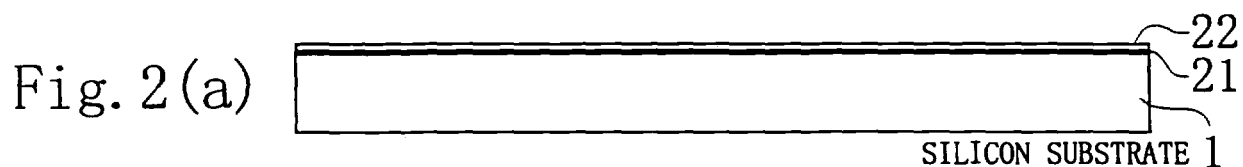


Fig. 3

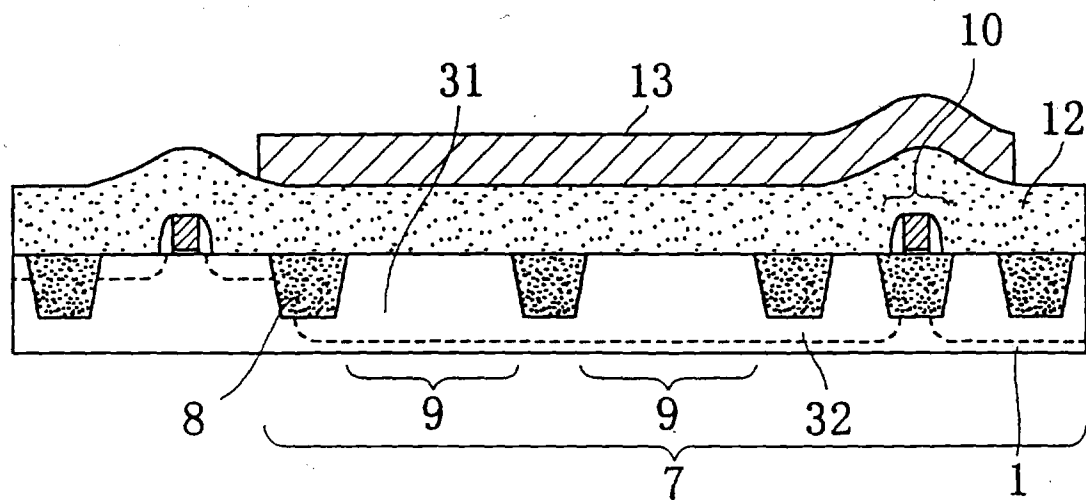


Fig. 4

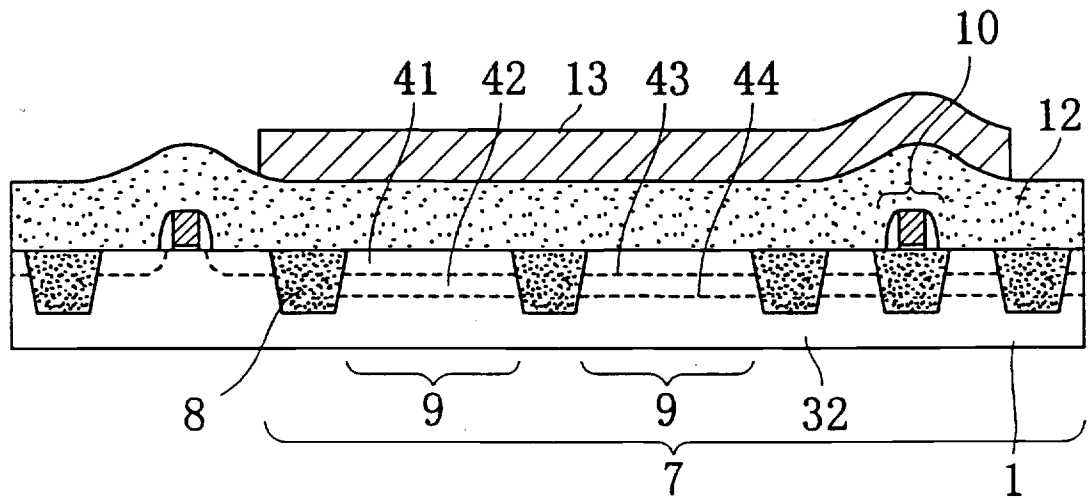
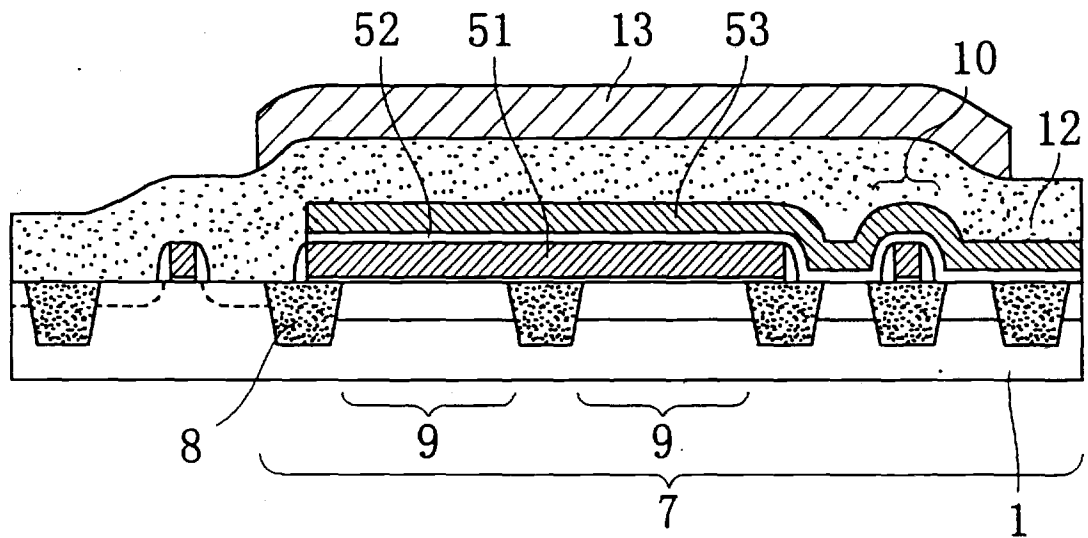


Fig. 5



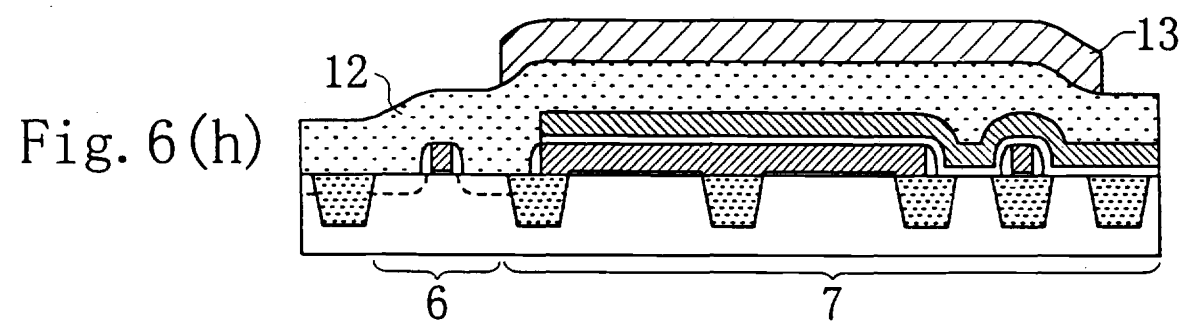
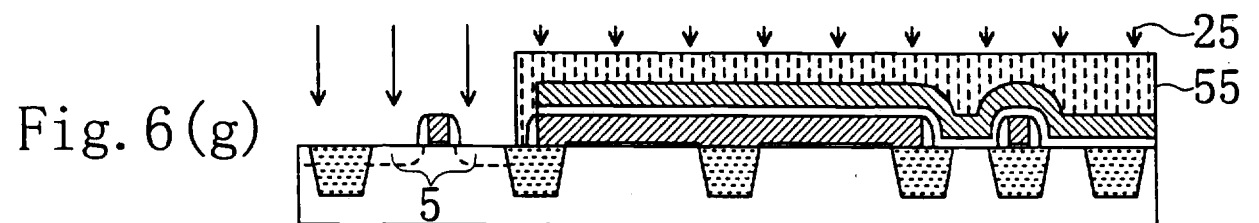
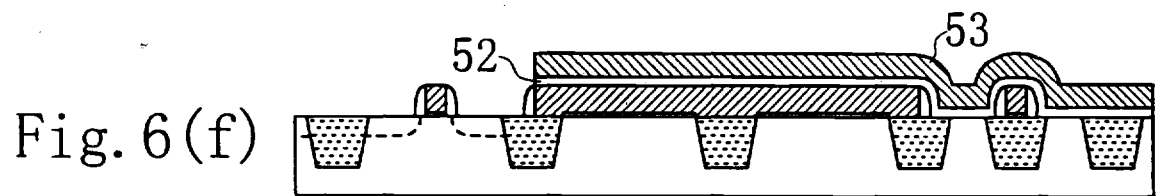
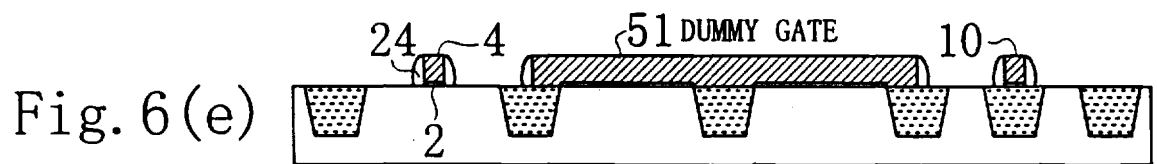
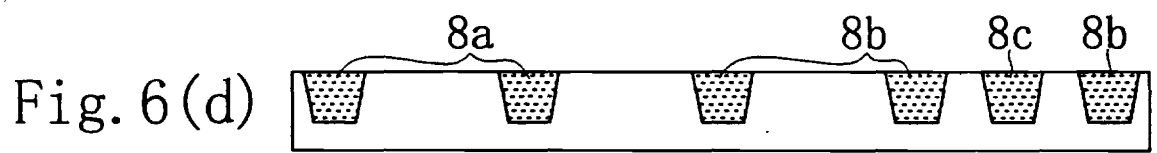
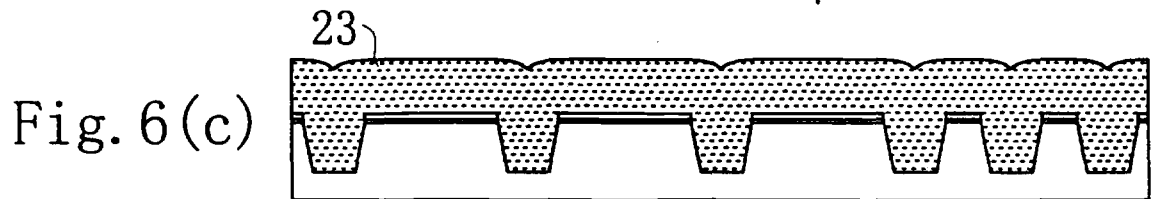
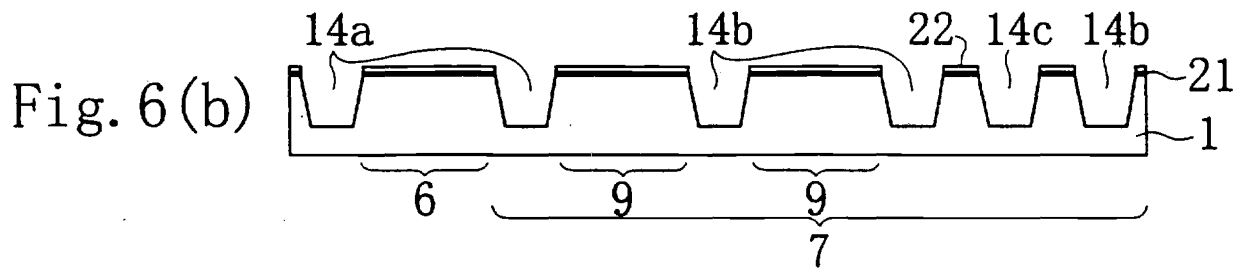
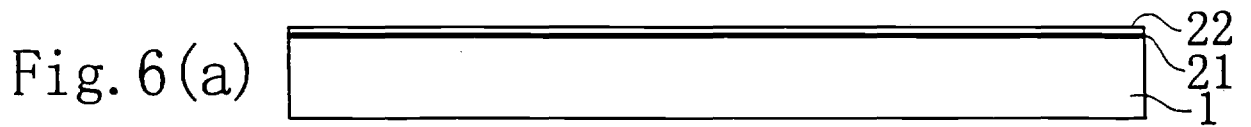


Fig. 7

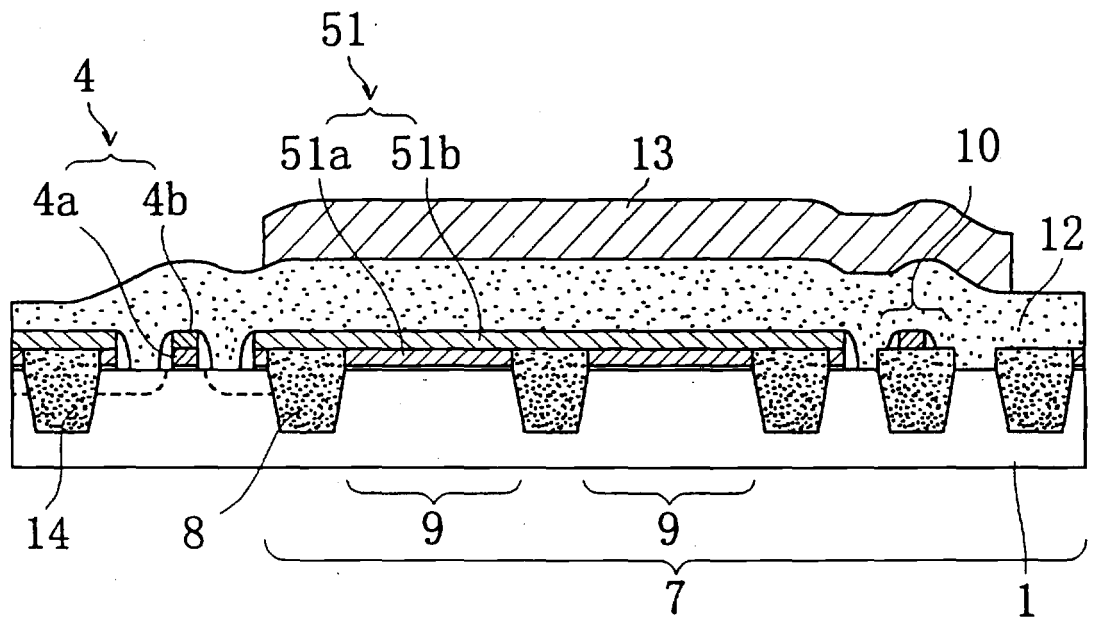


Fig. 8

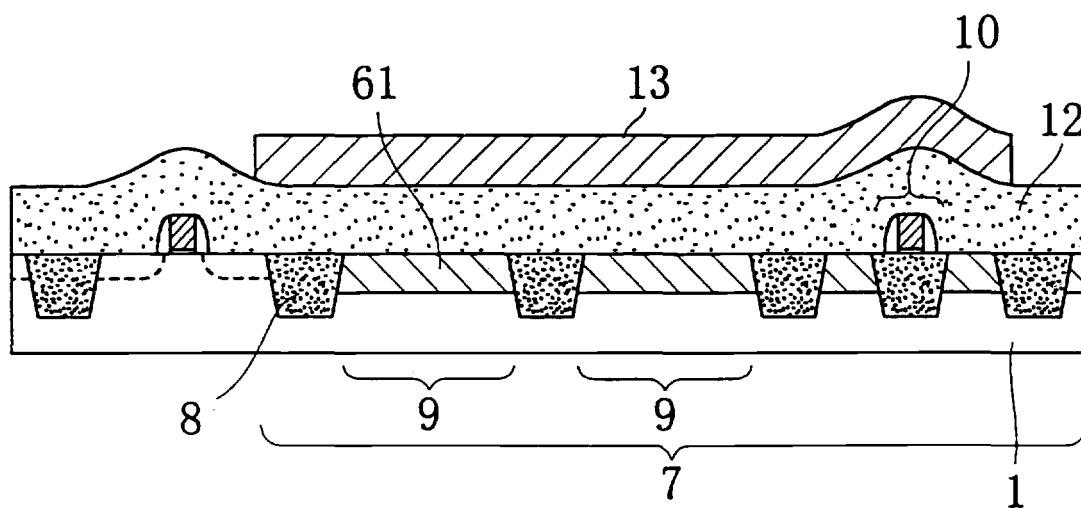


Fig. 9(a)

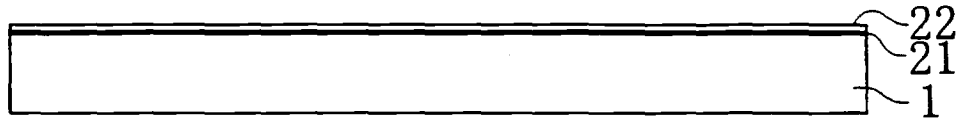


Fig. 9(b)

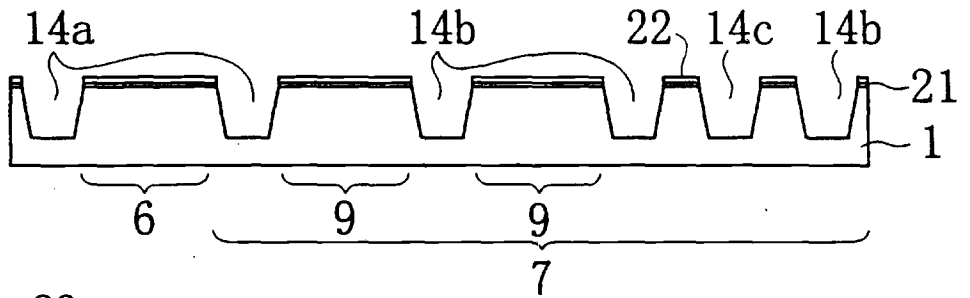


Fig. 9(c)

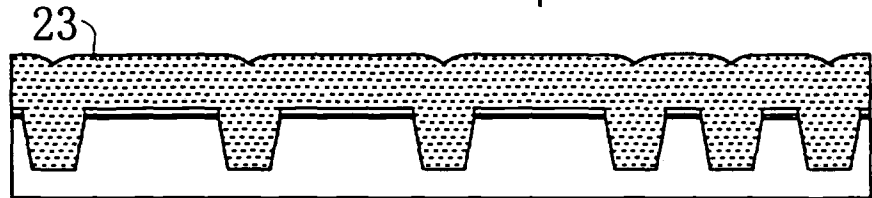


Fig. 9(d)

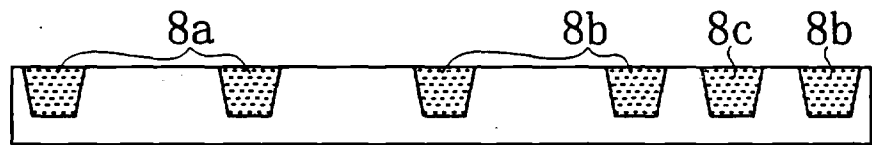


Fig. 9(e)

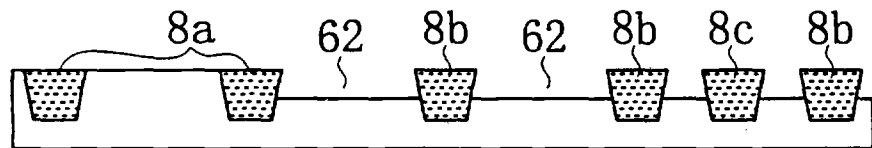


Fig. 9(f)

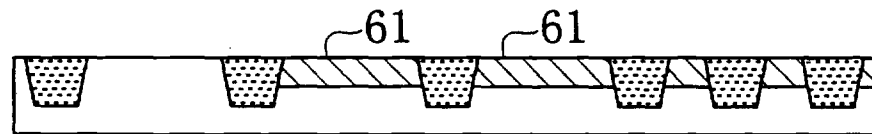


Fig. 9(g)

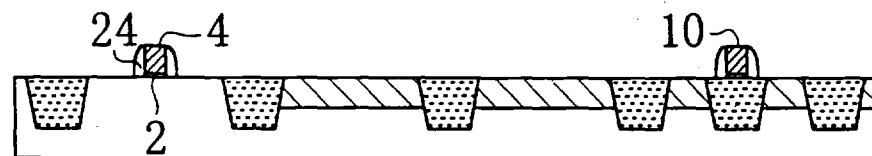


Fig. 9(h)

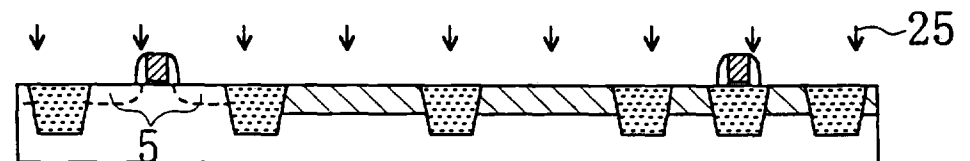


Fig. 9(i)

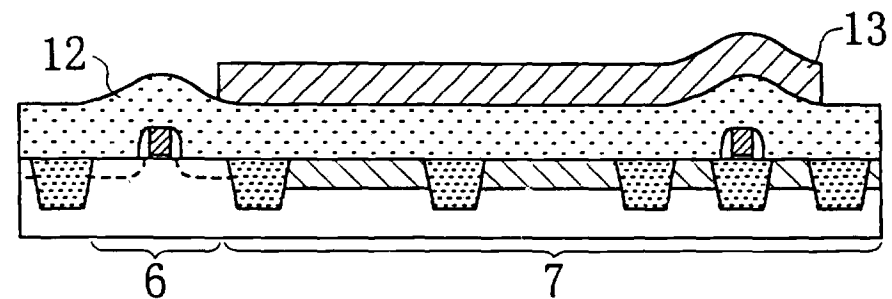
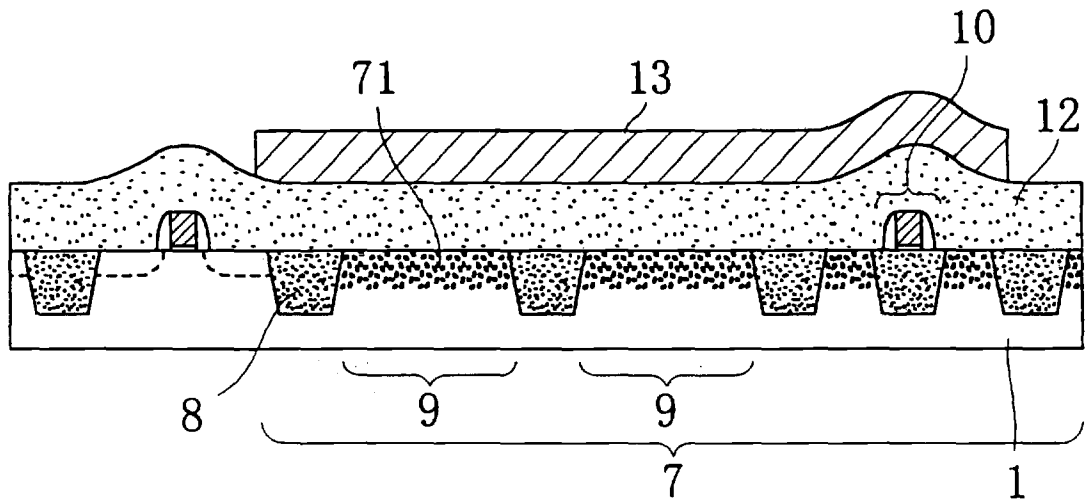


Fig. 10



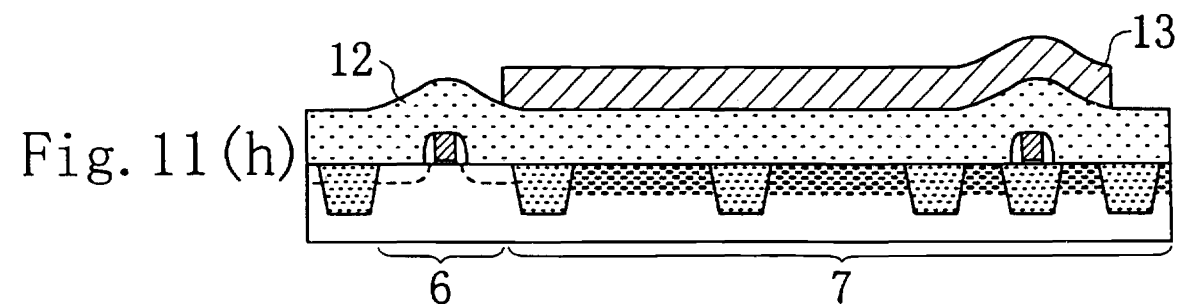
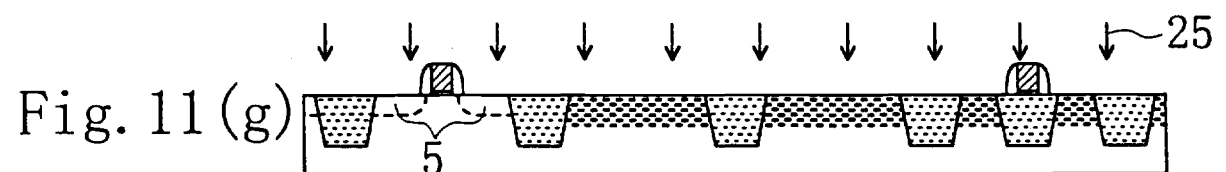
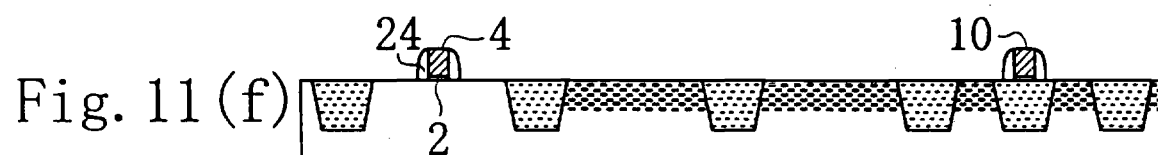
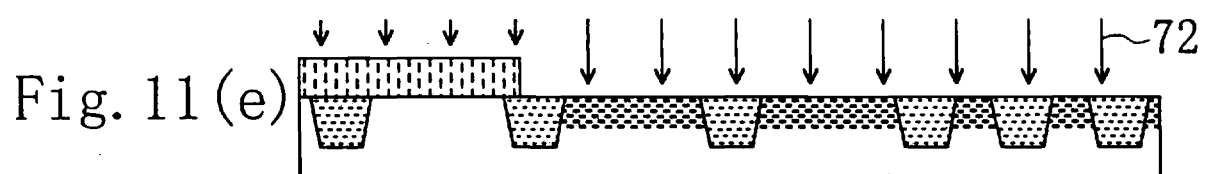
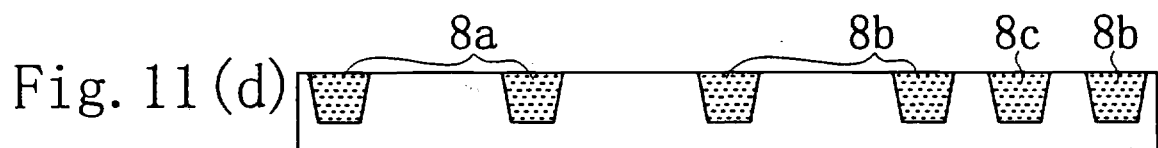
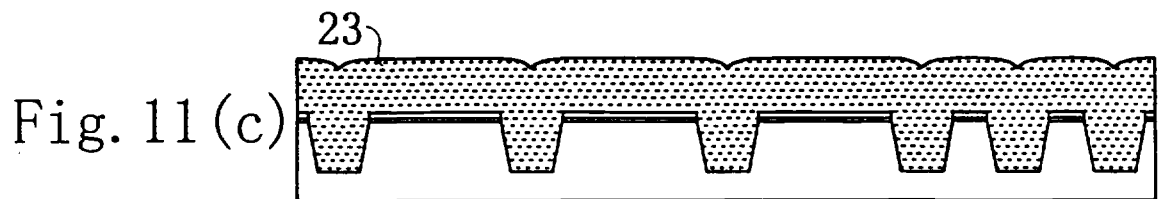
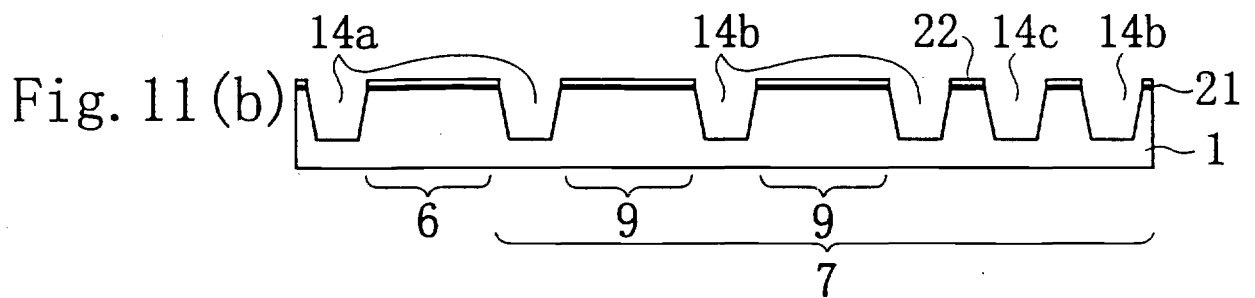
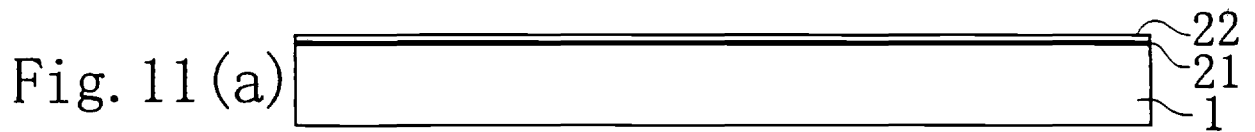
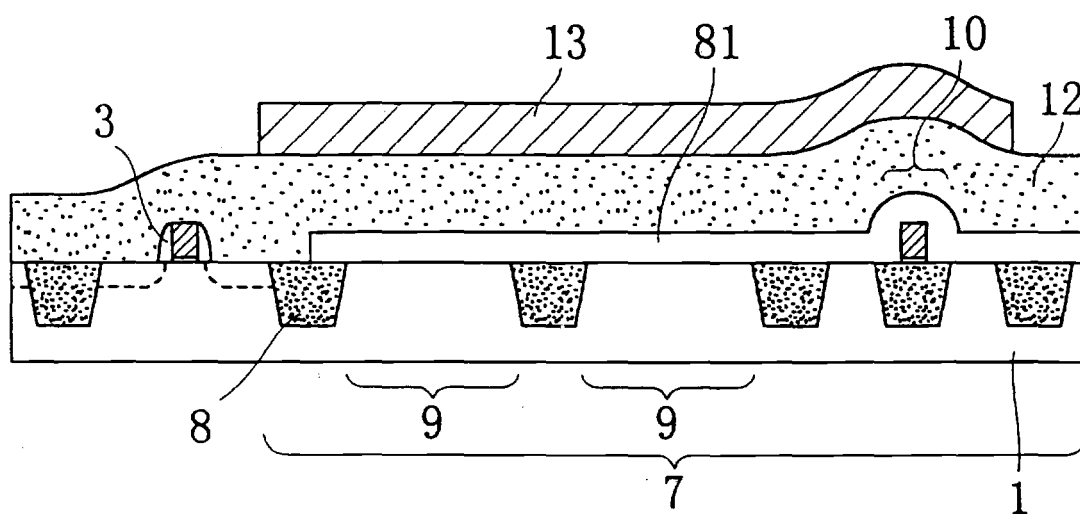


Fig. 12



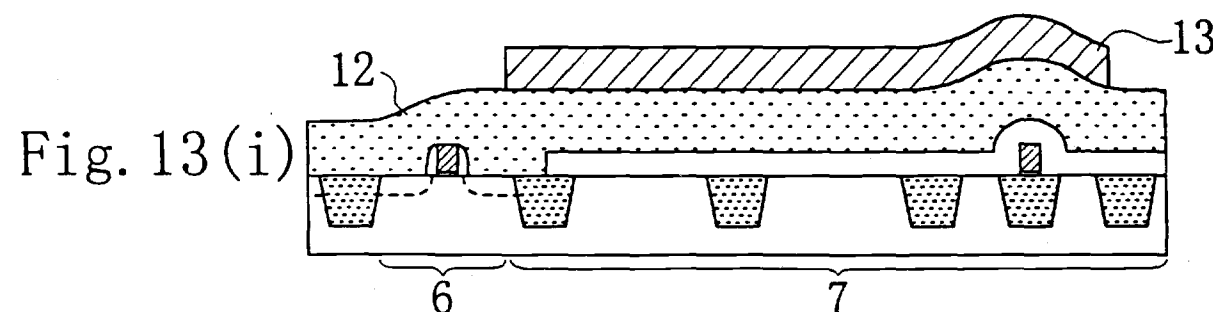
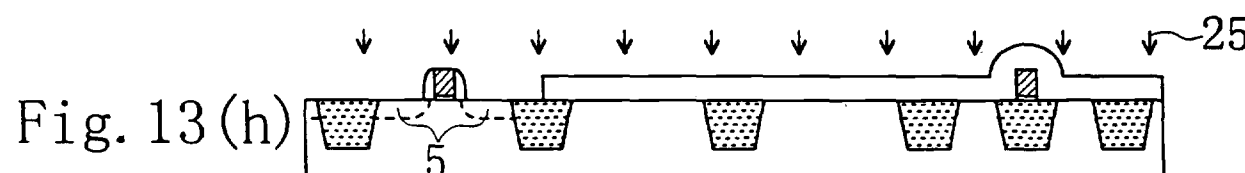
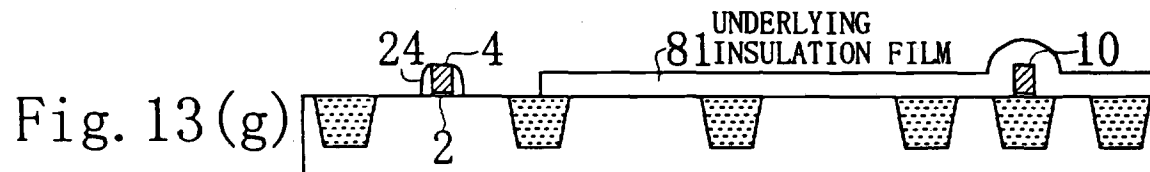
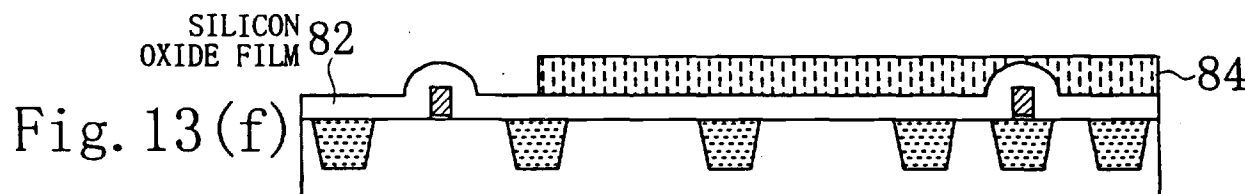
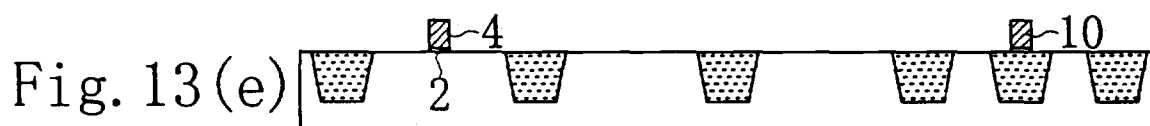
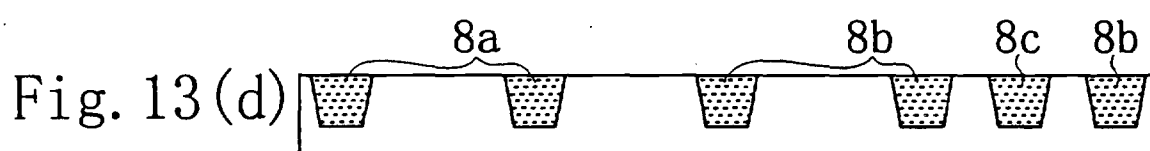
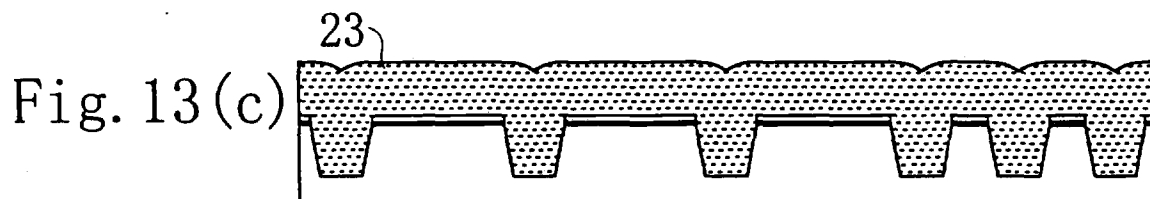
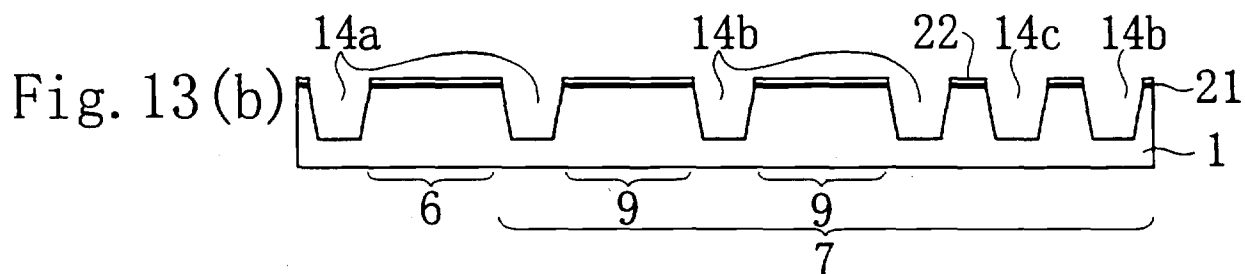
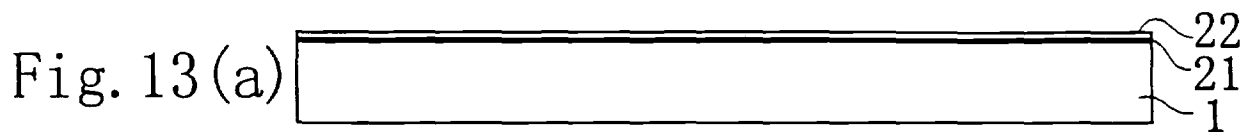


Fig. 14(a)

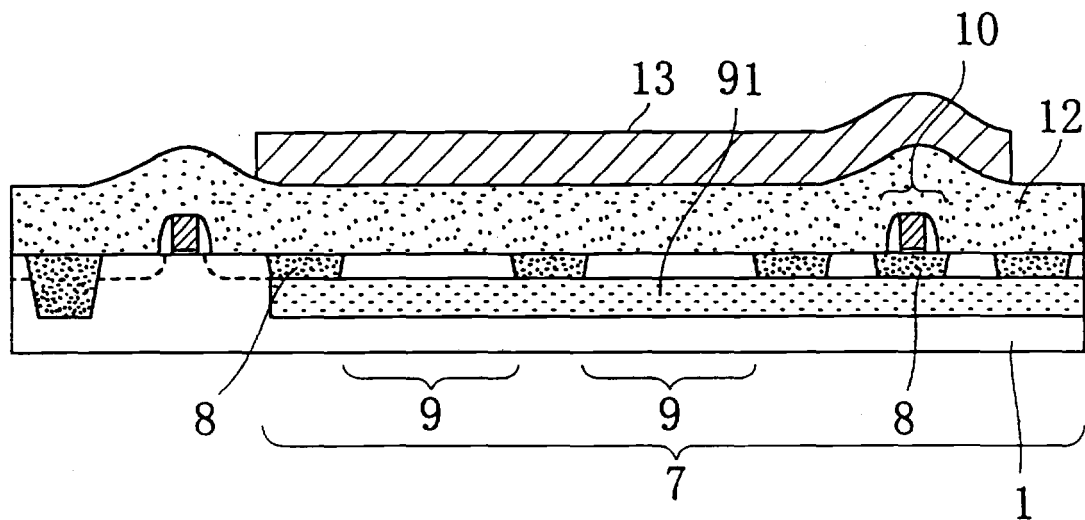
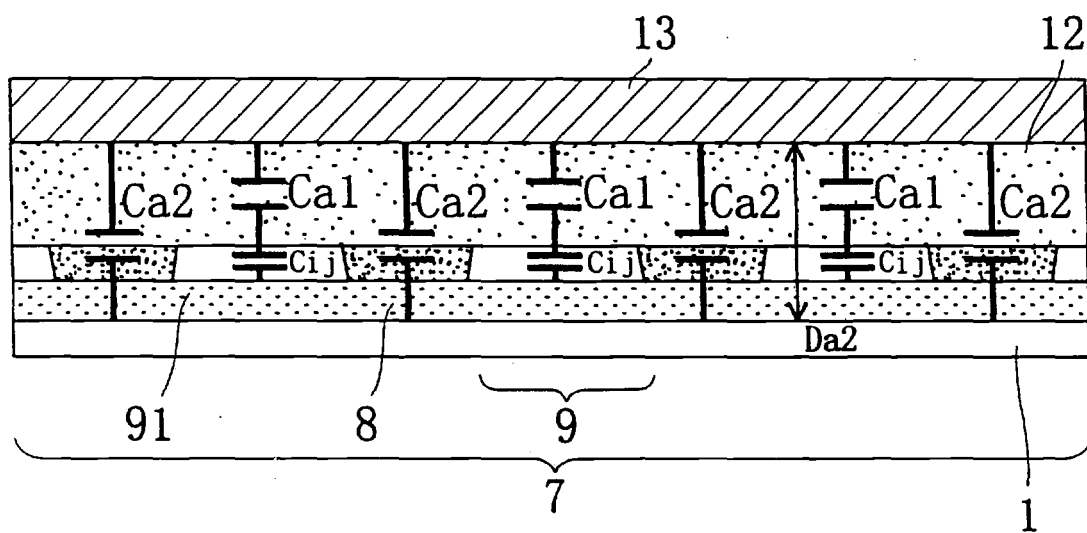
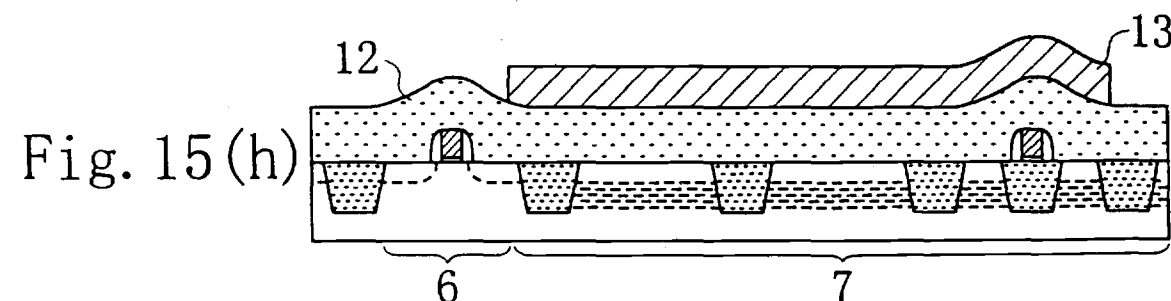
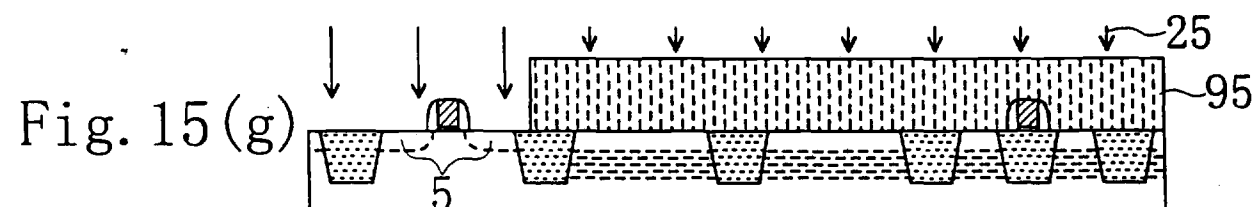
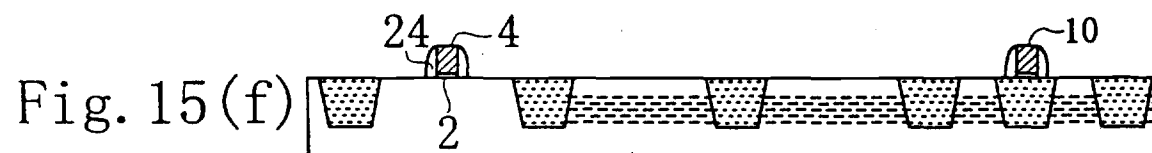
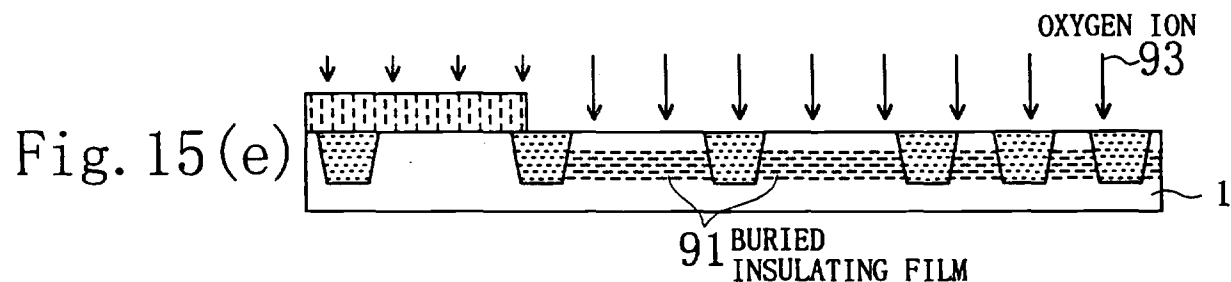
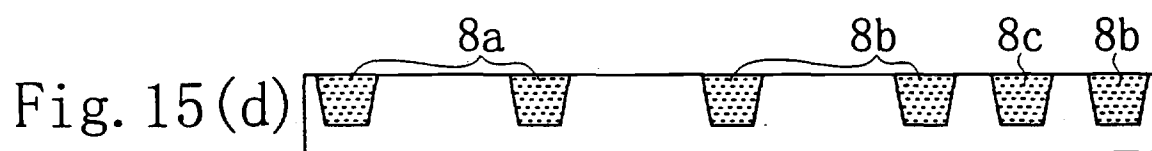
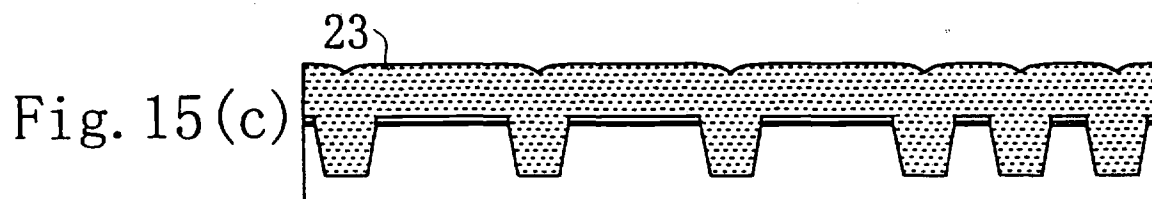
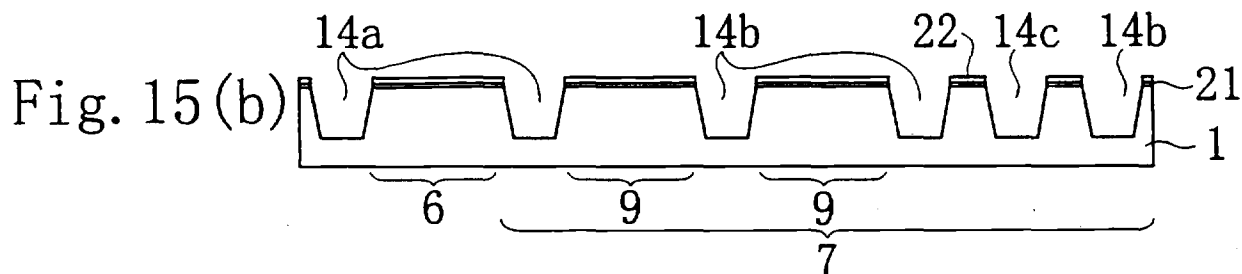
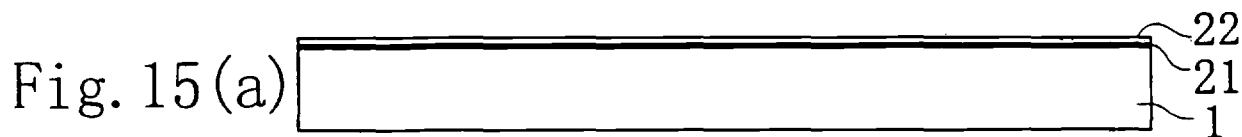
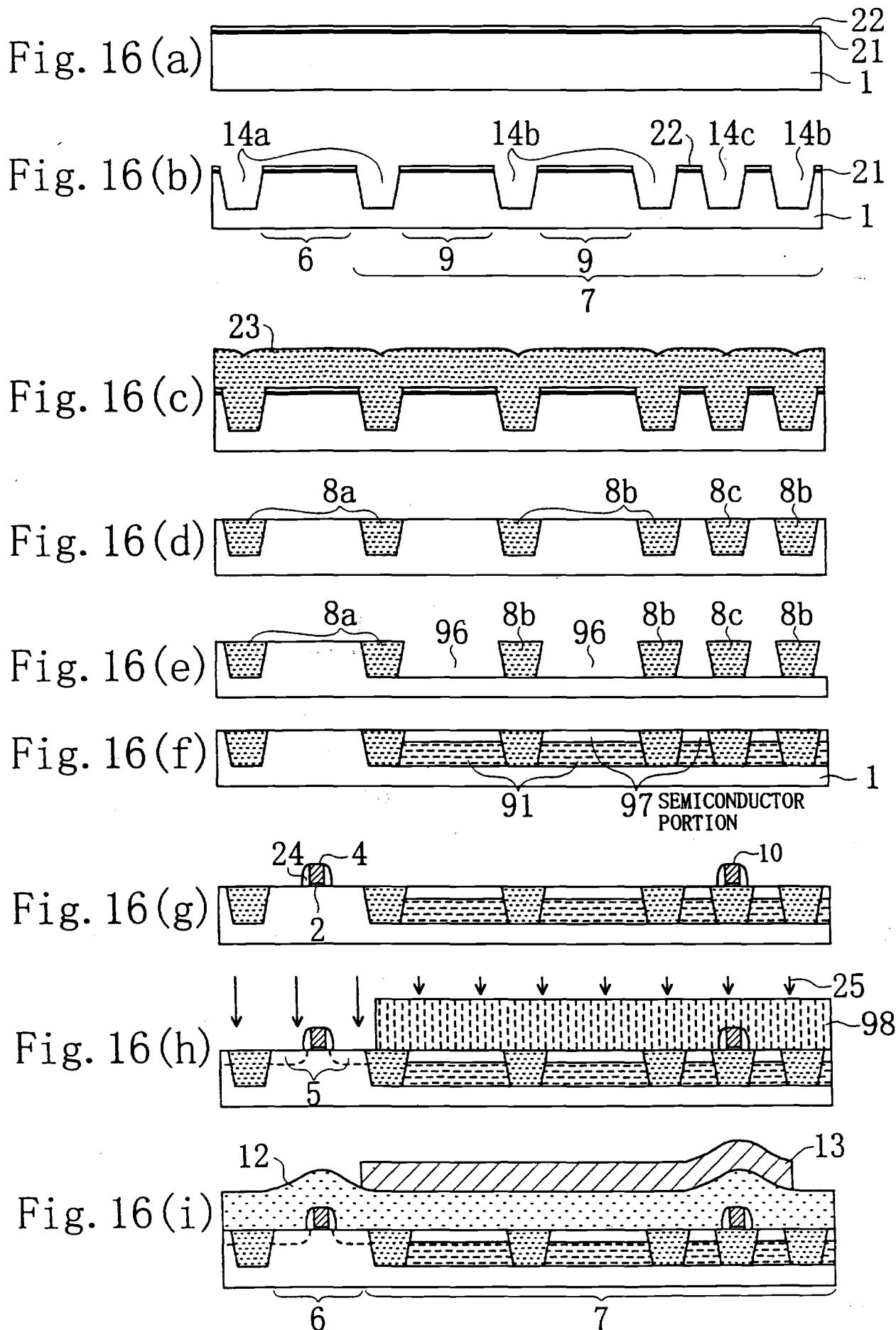
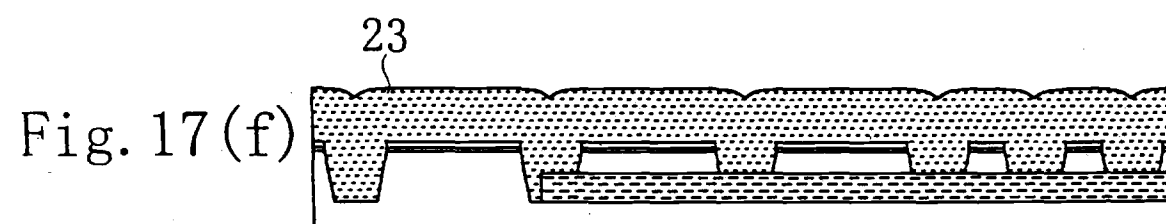
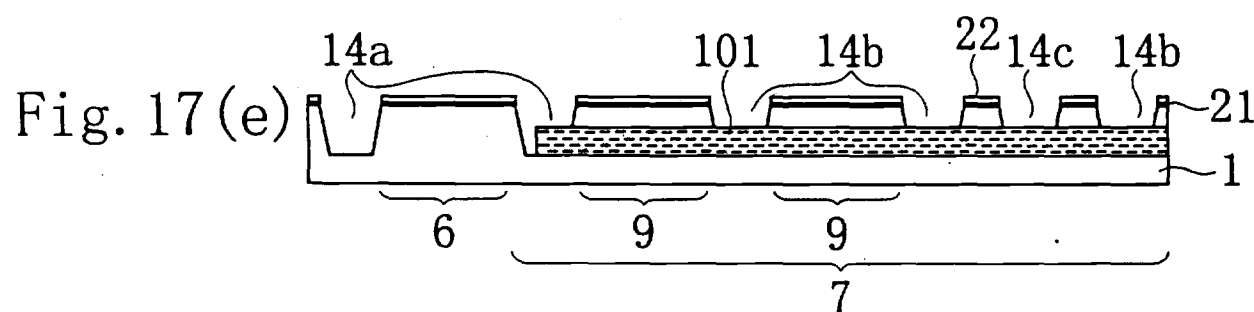
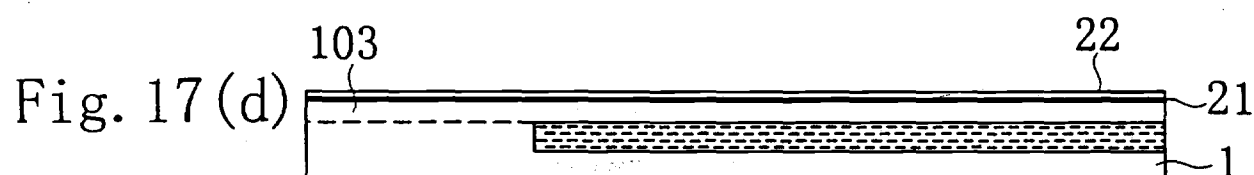
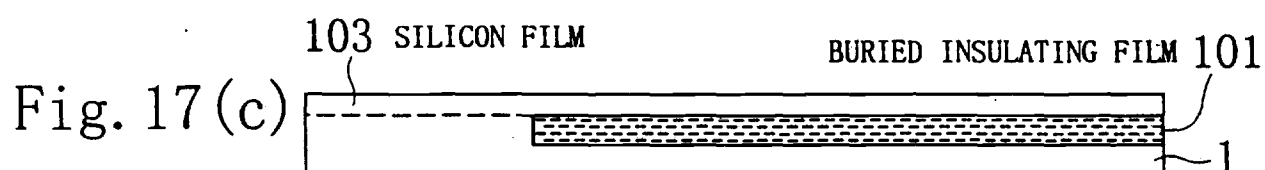


Fig. 14(b)









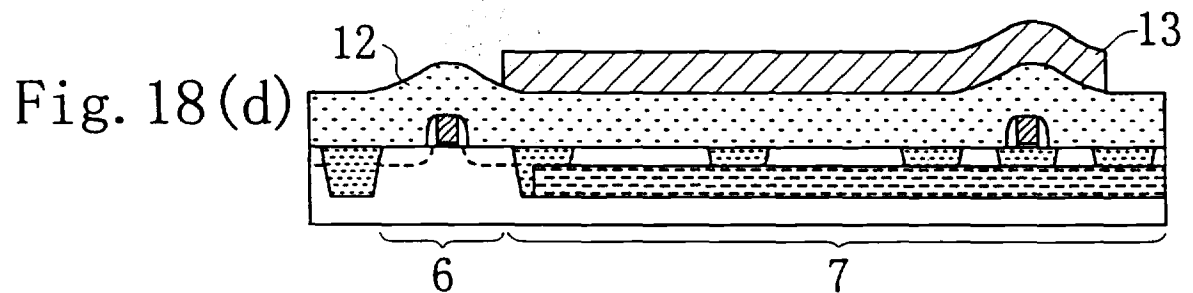
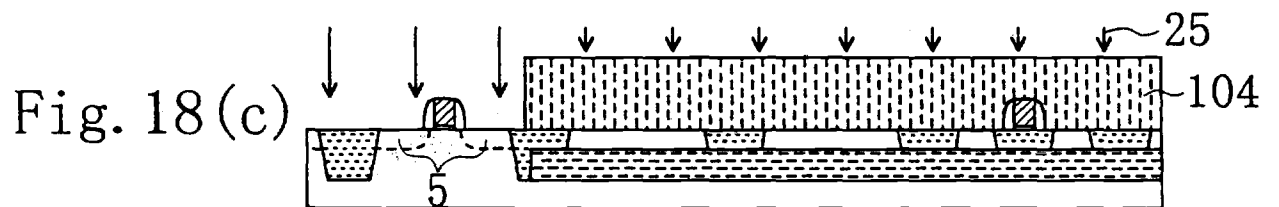
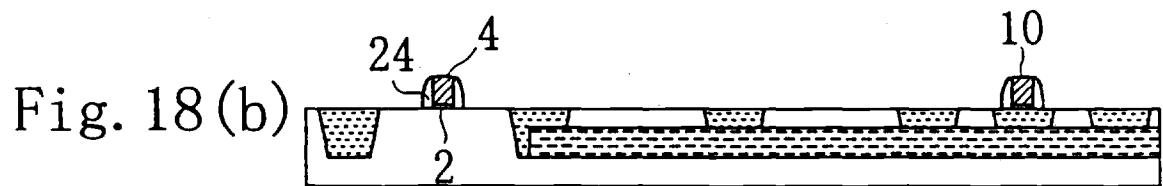
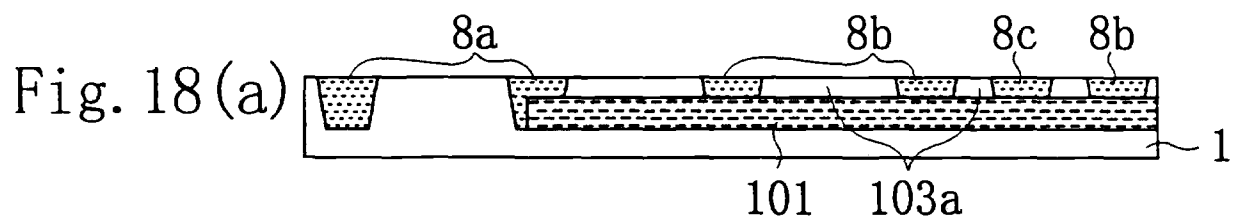


Fig. 19
PRIOR ART

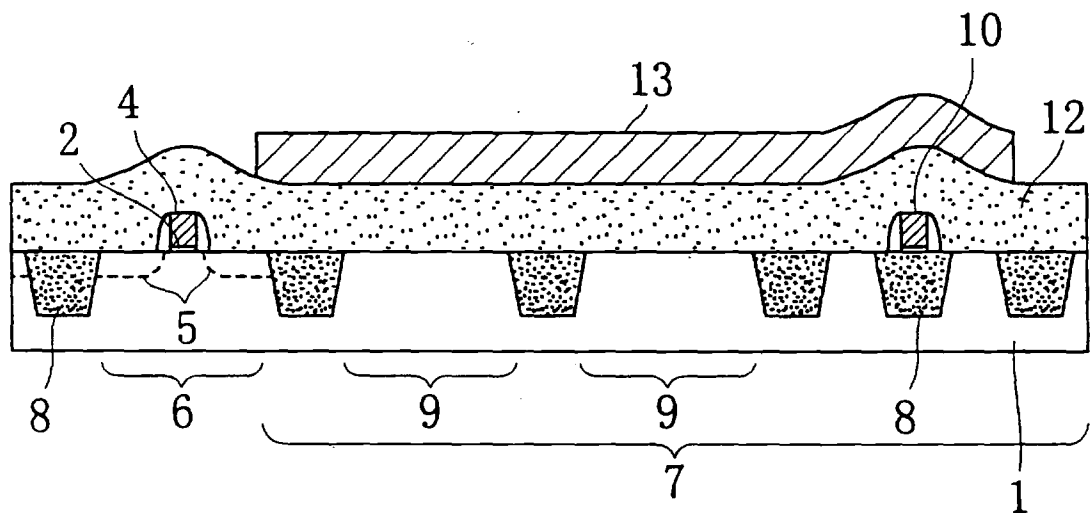


Fig. 20(a)
PRIOR ART



Fig. 20 (b)
PRIOR ART

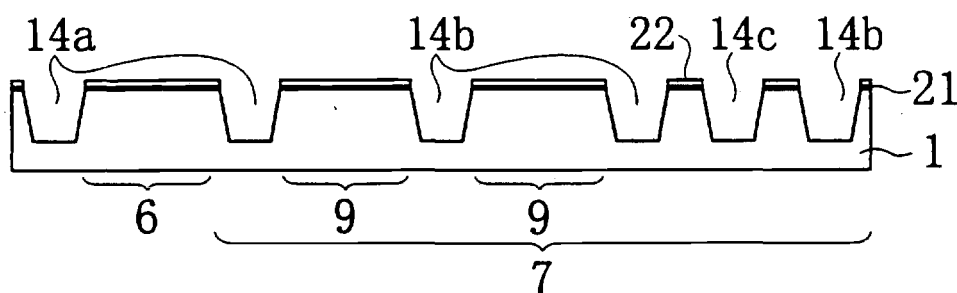


Fig. 20 (c)
PRIOR ART

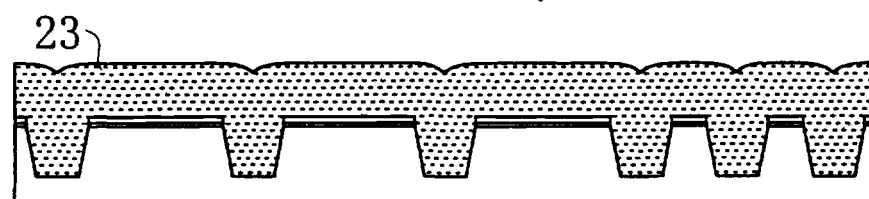


Fig. 20 (d)
PRIOR ART

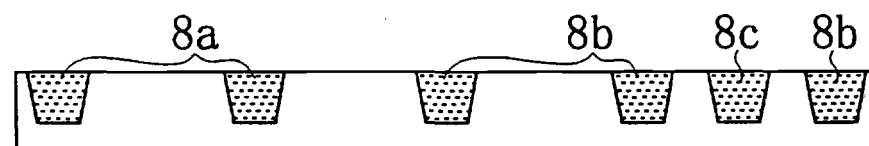


Fig. 20 (e)
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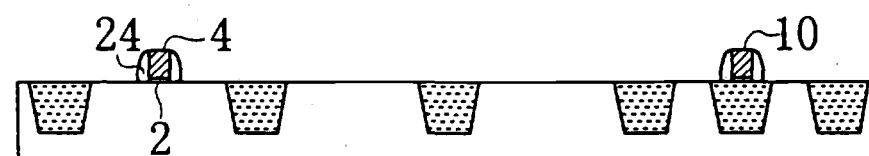


Fig. 20 (f)
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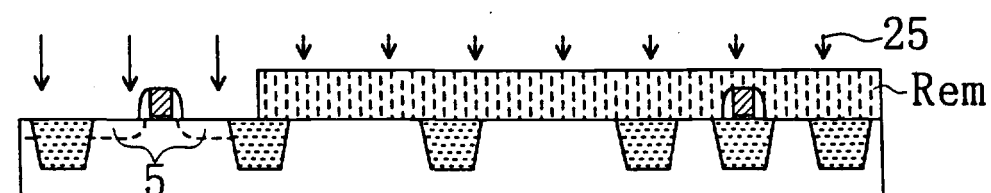


Fig. 20(g)
PRIOR ART

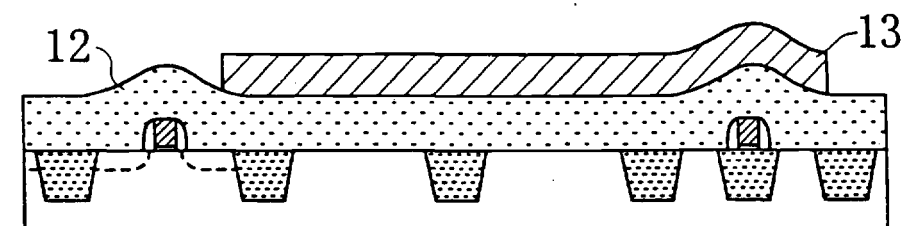


Fig. 21(a)

PRIOR ART

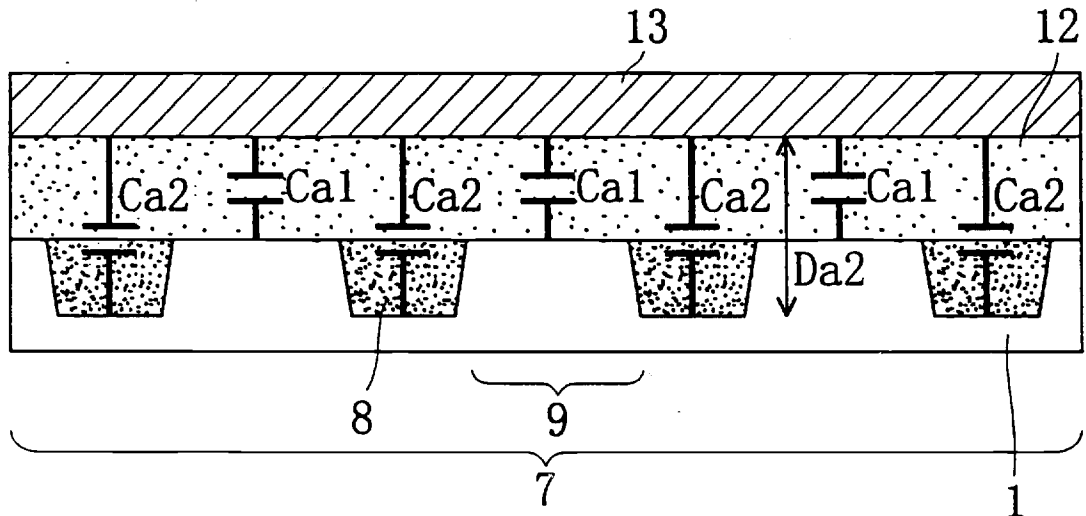
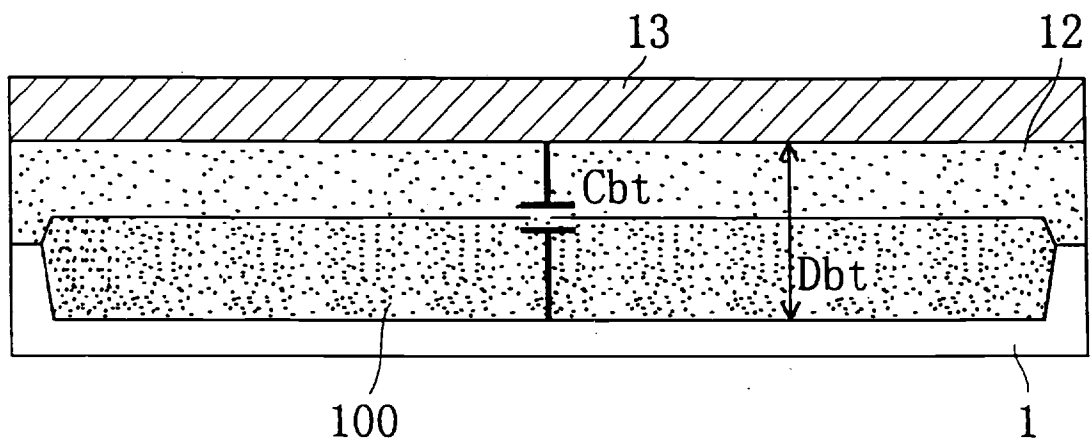


Fig. 21(b)

PRIOR ART



[Handwritten mark]

Cited Art
ATTORNEY DOCKET NO. 43889/898 #2
PATENT APPLICATION
5/24/00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Makoto KATO et al.)
Divisional Appln. Of:) **Group Art Unit: Not Yet Assigned**
Serial No.: 08/978,137, filed 11/25/97)
Serial No.: TO BE ASSIGNED) **Examiner: Not Yet Assigned**
Filed: December 22, 1999)
For: **METHOD OF MANUFACTURING**
TRENCH-ISOLATED SEMICONDUCTOR DEVICE

[Handwritten signature]

JC678 U.S. PTO
09/469498
12/22/99

INFORMATION DISCLOSURE STATEMENT

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure under 37 C.F.R. §§ 1.56 and 1.98,
Applicants wish to bring to the attention of the U.S. Patent and Trademark Office the
references listed on the enclosed Form PTO-1449, which were previously cited by both
Applicants and the Examiner in parent application Serial No. 08/978,137, filed on
November 25, 1997. Therefore, in accordance with 37 C.F.R. § 1.98(d), no copies of
the previously submitted information is provided.

WDC99 195075-1.043889.0898

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 13-0203. A duplicate copy of this communication is enclosed for accounting purposes.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: December 22, 1999

By: _____


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

WDC99 195075-1.043889.0898

- 2 -

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DeAmot 3/2

PATENT APPLICATION
ATTORNEY DOCKET NO. 43889/898

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Prior Application Art Unit: 2822

Examiner: K. Duong

Sir:

This is a request for filing a Continuation X Divisional application under 37 C.F.R. §1.53(b) of pending prior application Serial No. 08/978,137 filed November 25, 1997 of Takaaki UKEDA, Chiaki KUDO and Toshiki YABU for SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME.

- X Enclosed is a copy of the prior application including the oath or declaration and drawings, if any, as originally filed. I hereby verify that the attached papers are a true copy of prior application Serial No. 08/978,137, as originally filed on November 25, 1997.
- A verified statement claiming small entity status is enclosed or is on file in the prior application and such status is still proper and desired (37 C.F.R. §1.28(a)).
- X Cancel in this application original claims 19-38 of the prior application before calculating the filing fee. At least one original independent claim is retained for filing purposes.
- A Preliminary Amendment is enclosed. The claims have been numbered consecutively beginning with the number following the highest numbered original claim in the prior application.
- X The filing fee is calculated below:

CLAIMS AS FILED LESS ANY CLAIMS CANCELLED IN PARAGRAPH 2				
For	: Number Filed	: Number Extra:	Rate	: Basic Fee \$760.00
Total	:	:	:	:
Claims	: 18- 20 =	: 20	: x \$ 18.00 =	: 0.00
Independent	:	:	:	:
Claims	: 4- 3 =	: 1	: x \$ 78.00 =	: 78.00
Multiple Dependent Claims (if applicable)			: \$260.00 =	: 0.00
Total			=	: 838.00
Reduction by ½ for			:	:
filing by small entity			:	: - 0.00
TOTAL FILING FEE			:	: \$ 838.00

JC678 U.S. PTO
09/469498
12/22/99

6. X Please charge Deposit Account No. 13-0203 in the amount of \$ 838.00 to cover the filing fee.
7. X The Commissioner is hereby authorized to charge any fees due under 37 C.F.R. §1.16 and any other fees due under 37 C.F.R. §1.17 during the pendency of this application which may be required, or credit any overpayment to, Deposit Account No. 13-0203. A duplicate of this Divisional Application Transmittal Letter is enclosed for accounting purposes.
8. X Amend the specification by inserting before the first line, the following:

--This is a divisional application of Serial No. 08/978,137, November 25, 1997.

A new U.S. Patent to 130,139

9. Transfer the drawings from the prior application to this application and abandon the prior application as of the filing date accorded this application. An additional copy of this sheet is enclosed for filing in the prior application file.
10. X New formal drawings are enclosed or X will be submitted at a later date.
11. X The prior application is assigned of record to Matsushita Electric Industrial Co., Ltd.
12. X Priority of Application Serial No. 8-314762, filed on November 26, 1996 and Serial No. 9-023844, filed on February 6, 1997, both in Japan are claimed under 35 U.S.C. §119. Certified copies are enclosed or X are on file in the prior application.
13. X The power of attorney in the prior application is to at least one of the following: Raphael V. Lupo (Reg. No. 28,363); Jack Q. Lever, Jr. (Reg. No. 28,149); Kenneth L. Cage (Reg. No. 26,151); Michael E. Fogarty (Reg. No. 36,139); Brian E. Ferguson (Reg. No. 36,801); Edward E. Kubasiewicz (Reg. No. 30,020); Paul Devinsky (Reg. No. 28,553); Robert W. Zelnick (Reg. No. 36,976); and Willem F. Gadiano (Reg. No. 37,136).
14. A new power of attorney is enclosed.
15. X The power appears in the original declaration of the prior application.
16. Since the power of attorney does not appear in the original declaration, a copy of the power in the prior application is enclosed.
17. X Please address all correspondence to:

Michael E. Fogarty, Esq.
MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000

18. X Recognize as associate attorneys:

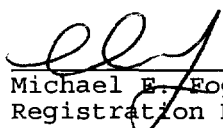
Edward A. Becker, Reg. No. 37,777; Stephen A. Becker, Reg. No. 26,527; Marcel K. Bingham, Reg. No. 42,327; John G. Bisbikis, Reg. No. 37,095; Daniel Bucca, Reg. No. 42,368; Stephen C. Carlson, Reg. No. 39,929; Thomas A. Corrado, Reg. No. 42,439; Paul Devinsky, Reg. No. 28,553; Laura A. Donnelly, Reg. No. 38,435; Margaret M. Duncan, Reg. No. 30,879; Brian E. Ferguson, Reg. No. 36,801; Keith E. George, Reg. No. 34,111; John A. Hankins, Reg. No. 32,029; Brian D. Hickman, Reg. No. 35,894; Eric J. Kraus, Reg. No. 36,190; Patrick B. Law, Reg. No. 41,549; Robert E. LeBlanc, Reg. No. 17,219; Christine F. Martin, Reg. No. 39,762; Michael A. Messina, Reg. No. 33,424; Eugene J. Molinelli, Reg. No. 42,901; Christopher J. Palermo, Reg. No. 42,056; Joseph H. Paquin, Jr., Reg. No. 31,647; Robert L. Price, Reg. No. 22,685; Gene Z. Robinson, Reg. No. 33,351; Joy Ann G. Serauskas, Reg. No. 27,952; David A. Spenard, Reg. No. 37,449; Arthur J. Steiner, Reg. No. 26,106; David L. Stewart, Reg. No. 37,578; Michael D. Switzer, Reg. No. 39,552; Leonid D. Thenor, Reg. No. 39,397; Keith J. Townsend, Reg. No. 40,358; Aaron Weisstuch, Reg. No. P41,557; Edward J. Wise, Reg. No. 34,523; and Alexander V. Yampolsky, Reg. No. 36,324.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: December 22, 1999

By:


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, D.C. 20006-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

A

A Partnership Including
Professional Corporations
600 13th Street, N.W.
Washington, D.C. 20005-3096
(202) 756-8000
Main Facsimile No. (202) 756-8087
Facsimile Operator No. (202) 756-8090

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MCDERMOTT, WILL & EMERY

FACSIMILE

FROM:

Sender: Brigitte DeHart, Direct Phone: 202-756-8641
Maintenance Fee Paralegal
Sender's E-Mail: bdehart@mwe.com
Secretary: _____ Direct Phone: _____
Client/Matter/Tkpr: 43889-898-6200 Date: January 7, 2002 Time Sent: _____
Number of pages including this page: 3

TO:

Name: Mr. Mike Stellabotte Facsimile No. 215-682-8284
U.S. Patent Office/ PATENT PROOF
Company: COPY PILOT PROJECT Contact No. _____

Re: Serial No. 09/469,498; filed Dec. 22, 1999; Our Ref: 43889-898

Attached please find your PATENT PROOF COPY PILOT PROJECT cover
sheet with our checks/comments for the above-identified patent application.

The information contained in this facsimile message is legally privileged and confidential information intended only for the use of the individual or entity named above. If the reader of this message is not the intended recipient, you are hereby notified that any dissemination, distribution, or copy of this facsimile is strictly prohibited. If you have received this facsimile in error, please notify us immediately by telephone and return the original message to us at the above address via the United States Postal Service. Thank you.
WDC99 542509-1.043889.0898

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McDermott, Will & Emery

Patent Proof Copy Pilot Project



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PATENT AND
TRADEMARK OFFICE

An Agency of the United States
Department of Commerce

Return Fax Sheet

Fax No. 215-682-8284

Application No. 09/469,498

Corrections to Copy—Please check corrections required.

- ☐ Incorrect, duplicated, omitted words
- ☐ Incorrect, omitted punctuation
- ☐ Incorrect, omitted spacing
- ☒ Other: 2nd column on cover page, under Foreign Patent Documents
- ☐ Check here if there were no errors on the proof copy
- ☐ Apply unentered/entered but missing/to be filed papers

	Date		Date
<input type="checkbox"/> CPA	_____	<input type="checkbox"/> Claim for Priority	_____
<input type="checkbox"/> RCE	_____	<input type="checkbox"/> Claim/Spec. Amendments	_____
<input type="checkbox"/> IDS	_____	<input type="checkbox"/> _____	_____
<input type="checkbox"/> Declaration	_____	<input type="checkbox"/> _____	_____
<input type="checkbox"/> Change of Attorney	_____	<input type="checkbox"/> _____	_____
<input type="checkbox"/> Small Entity Statement	_____	<input type="checkbox"/> Other: _____	_____
<input type="checkbox"/> Change of Address	_____	<input type="checkbox"/> _____	_____

POINT OF CONTACT FOR THIS APPLICATION: LORNA MULLEN-CUSTOMER NO. 20277-FAX NO. 202-756-8087

Reviewer: BRIGITTE DEHART On Ref 43889-898

Comments:

Please correct country of 4th foreign patent document.
Our records show this to be a European (EP) patent -
not Japanese (JP)

Applicant Proof Copy

Ukeda et al.

Application No.: 09/469,498

Response Date: Feb. 4, 2002

- ✓ (54) TRENCH ISOLATED SEMICONDUCTOR DEVICE
- ✓ (76) Inventors: Takasaki Ukeda, Osaka; Chiaki Kudo, Kyoto; Toshiki Yabu, Osaka, all of (JP)
- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

- ✓ (21) Appl. No.: 09/469,498
- ✓ (22) Filed: Dec. 22, 1999

Related U.S. Application Data

- ✓ (62) Division of application No. 08/978,137, filed on Nov. 25, 1997, now Pat. No. 6,130,139.

(30) Foreign Application Priority Data

- ✓ Nov. 26, 1996 (JP) 8-314762
- ✓ Feb. 6, 1997 (JP) 9-023844

- (51) Int. Cl.⁶ H01L 33/00
- (52) U.S. CL 257/509; 257/545
- (58) Field of Search 257/509, 506, 257/545, 598

(56) References Cited**U.S. PATENT DOCUMENTS**

- ✓ 3,622,382 A 11/1971 Brack et al. 428/448
- ✓ 4,929,566 A 5/1990 Beitman 438/423
- ✓ 4,948,742 A 8/1990 Nishimura et al. 438/423
- ✓ 5,270,265 A 12/1993 Hemmenway et al. 438/404
- ✓ 5,371,401 A * 12/1994 Kurita 257/254
- ✓ 5,426,062 A 6/1995 Hwang 438/423
- ✓ 5,663,588 A * 9/1997 Suzuki et al. 257/350
- ✓ 5,665,633 A 9/1997 Meyer
- ✓ 5,731,623 A * 3/1998 Ishimaru 257/517

- ✓ 5,760,444 A 6/1998 Okumura 257/350
- ✓ 5,856,218 A 1/1999 Kinoshita et al. 438/414
- ✓ 5,877,066 A 3/1999 Stolmeijer et al. 438/424
- 6,028,344 A * 2/2000 Hashimoto 257/587

FOREIGN PATENT DOCUMENTS

- EP 05-38807 10/1992 ✓
- JP 58-200554 11/1983 ✓
- JP 60-015944 1/1985 ✓
- ✓ EP 02-20500 9/1986 ✓ X
- JP 63-246842 10/1988 ✓
- JP 02-272745 11/1990 ✓
- JP 05-013565 1/1993 ✓

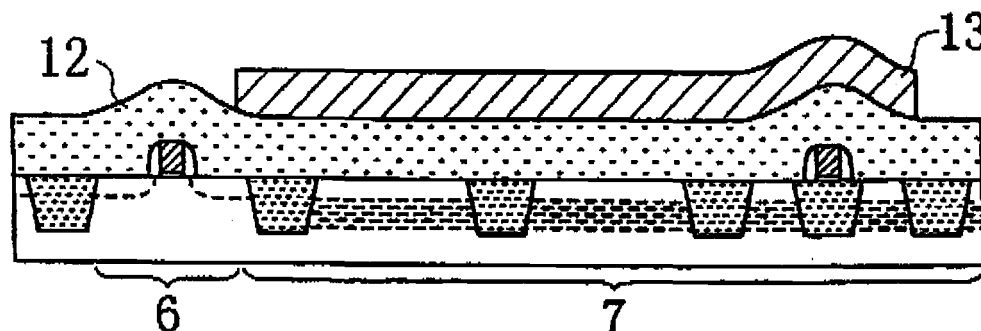
* cited by examiner

Primary Examiner—Stephen D. Meier

(57) ABSTRACT

The top surface of a P-type semiconductor substrate is partitioned into an active region to be formed with an element and an isolation region surrounding the active region. The isolation region is composed of trench portions and dummy semiconductor portions. An interlayer insulating film is deposited on the substrate, followed by a wire formed thereon. In each of the semiconductor portions, an impurity diffusion layer is formed simultaneously with the implantation of ions into the element so that a PN junction is formed between the impurity diffusion layer and the silicon substrate. A capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions is obtained by adding in series the capacitance in the impurity diffusion layer to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. What results is a semiconductor device having lower total wiring-to-substrate capacitance and a higher operating speed.

20 Claims, 21 Drawing Sheets





UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/469,498 12/22/99 UKEDA T 43889/898

020277 MMC2/0226
MCDERMOTT WILL & EMERY
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER

JOHNSON, C
ART UNIT PAPER NUMBER

2822
DATE MAILED: 02/26/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/469,498	UKEDA ET AL.	
	Examiner	Art Unit	
	Chauncey B. Johnson	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 12 December 1999.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-18 is/are pending in the application.

 4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-18 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

 a) ☒ All b) ☐ Some * c) ☐ None of:

 1. ☐ Certified copies of the priority documents have been received.

 2. ☒ Certified copies of the priority documents have been received in Application No. 08978137.

 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

 * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	18) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
16) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	19) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
17) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>2</u> .	20) <input type="checkbox"/> Other:

DETAILED ACTION

This office action is in response to the preliminary amendment filed December 12, 1999.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishimaru (5,731,623).

Ishimaru teaches all the limitations of claims 1-3 in the application as follows: an active region (38/39, Fig. 6) and an isolation region (Fig. 5 and Fig. 6) surrounding said active region; a plurality of trench portions (11a –11f; Figs. 5 & 6) formed in said isolation region and filled with insulating material; semiconductor portions interposed between said individual trench portions in said isolation region (Fig. 6); an interlayer insulating film formed to extend continuously over said active region and said isolation region (42, Figs. 1 & 2); a wire (30 & 44, Fig. 2) formed on said interlayer insulating film; plurality of PN junctions (1 & 2; Fig. 1 & 2) formed in said semiconductor portions underlying said wire; an active region formed with a impurity diffusion region and a PN junction is formed at a bottom face of said impurity diffusion region (Fig. 6); and the PN junction of said isolation region being positioned at a level lower than the PN junction of said active region (Fig. 6).

3. In re claims 4-7 Ishimaru teaches the following: a dielectric film (28, Fig. 2) interposed between interlayer insulating film and said semiconductor portions and trench portion; a gate electrode (Fig. 6) formed on the semiconductor substrate within said active region, with sidewalls (35, Fig. 6) made of an insulating material and formed of both sides faces of said gate electrode; said underlying insulating film is formed of the same film, such as an oxide (Column 4, lines 36-44), as that said side walls; and said dielectric film being composed of a multilayer film (28 & 6, Fig. 5).

4. In re claims 8-9 Ishimaru further teaches the following: the dielectric film is formed in an upper portion of said semiconductor portions to have a top face at approximately the same level as a top face of each of said trench portions (6, Fig. 4F); and said dielectric film is composed of silicon oxide (Column 6, lines 53-54).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 10 -18 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al (5,663,588). Suzuki teaches all the limitations of claims 10 -18 in the application as follows: a semiconductor substrate having an active region(13c,a,d; Fig. 1B) and an isolation region (13 a, b; Fig. 1B) surrounding said active region; a plurality of trench portions (19, Fig. 1B) each formed in said isolation region and filled with an insulating material (16, Fig. 1B); a semiconductor portions (Fig. 1B) interposed between

said individual trench portions in said isolation region; an interlayer insulating film (21, Fig. 1B) formed to extend continuously over said active region and said isolation region; a wire (22, Fig. 1B) formed on said interlayer insulating film; a buried insulating film (12, Fig. 1B) formed in an inner portion of each of said semiconductor portions in said isolation region; and a resistor film (18, Fig. 1B) formed between said interlayer insulating film and at least said semiconductor portions of said isolation region.

7. In re claims 12-14, Suzuki teaches the following: the resistor film is an underlying film formed to extend continuously over said semiconductor portions and trench portions (Fig. 1B); a resistor element (18, Fig. 1B) having a high resistor film, wherein said underlying resistor film is formed of the same film as composing the high resistor film of said resistor element; and an electrode member (18, Fig. 1B) composed of a conductor film formed on the semiconductor substrate within said active region, wherein said resistor film is composed of the same material as composing said electrode member (Column 4, lines 35-40).

8. In re claims 15-16, Suzuki teaches the following: a MOSFET having a gate electrode composed of a first conductor film (13, Fig. 1B; 13 a/b, Fig. 5) formed on the semiconductor portion within said active region; a second conductor film (18, Fig. 1B; Fig 5) deposited on said first conductor film; the top surface of the first conductor film of said gate electrode is at approximately the same level as a top surface of each of said trench portions (Fig. 1B); a region of said resistor film overlying each of said semiconductor portions is formed of the same two films as composing said first and second conductor films of said gate electrode (Fig. 1B); a region of said resistor film

Art Unit: 2822

overlying each of said trench portions is composed of the same material composing said first conductor film of said gate electrode (Figs. 1B, 5, 9, 10); said resistor film is formed in an upper portion of each of said semiconductor portions of the semiconductor substrate to have top face at approximately the same level as a top surface of each of said trench portions (Fig. 3F).

9. In re claims 17-18, Suzuki further teaches the following: the use of oxygen ion implants in forming SOI layers (Column 1, lines 40-45) such as the monocrystalline silicon layer (13, Fig. 1B) and the polycrystalline/resistor film layer (18, Fig. 1B); and said resistor film being composed of polycrystalline silicon (Column 4, lines 35-40).

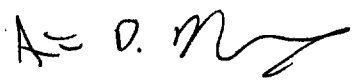
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chauncey Johnson whose telephone number is (703) 306-4826. The examiner can normally be reached on Monday through Friday 9:00 AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (703) 308-7382. The fax phone numbers for this Group is (703) 305-3432 or (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

CJ

Feb 15 , 2000.



Stephen D. Meier
Primary Examiner

Notice of References Cited				Application/Control No.		Applicant(s)/Patent Under Reexamination			
				09/469,498		UKEDA ET AL.			
				Examiner		Art Unit		Page 1 of 1	
				Chauncey B. Johnson		2822			
U.S. PATENT DOCUMENTS									
*		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	DOCUMENT SOURCE **		
							APS	OTHER	
<input type="checkbox"/>	A	6,028,344	Feb. 2000	Hashimoto	257	587	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	B	5,371,401	Dec. 1994	Kurita	257	254	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	C	5,731,623	Mar. 1998	Ishimaru	257	517	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	D	5,663,588	Sep. 1997	Suzuki et al	257	350	<input type="checkbox"/>	<input type="checkbox"/>	
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<input type="checkbox"/>	X							<input type="checkbox"/>	<input type="checkbox"/>

*A copy of this reference is not being furnished with this Office action. (See Manual of Patent Examining Procedure, Section 707.05(a).)

**APS encompasses any electronic search i.e. text, image, and Commercial Databases.

Form PTO-1449
(NW&E Ver. REV. 7-96)

Dept. of Commerce
PATENT & TRADEMARK OFFICE

ATTY DOCKET NO.
43889-898

APPLICATION
08/978,137

INFORMATION DISCLOSURE STATEMENT
(Use several sheets if necessary)

APPLICANT: Takaaki UKEDA et al.

FILING DATE: November 25, 1997

GROUP:
2822

12/23/99

09/469498

12/23/99

12/23/99

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	3,622,382	11/23/71	Brack et al.	428	448	
	4,929,566	05/29/90	Beitman	438	423	
	4,948,742	08/14/90	Nishimura et al.	438	423	
	5,426,062	06/20/95	Hwang	438	423	
	5,270,265	12/14/93	Hemmenway et al.	438	404	
	5,760,444	06/02/98	Okumura	257	350	
	5,856,218	01/05/99	Kinoshita et al.	438	414	
	5,877,066	03/02/99	Stolmeijer et al.	438	424	
	5,665,633	09/09/97	Meyer			
	5,663,588	02/09/97	Suzuki et al.			

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION	
					YES	NO
63-246842	10/13/88	JAPAN			XX	
60-015944	01/26/85	JAPAN			XX	
05-013565	01/22/93	JAPAN			XX	
05-38807	10/20/92	EUROPE			XX	
02-272745	11/07/90	JAPAN			XX	
02-20500	09/25/86	JAPAN			XX	
58-200554	11/22/83	JAPAN			XX	

EXAMINER

DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

109900PATPTOUDS-1449 PTO

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Confirmation
1	BRS	10	("3622382" or "4929566" or "4948742" or "5426062" or "5270265" or "5760444" or "5856218" or "5877066" or "5665633" or "5663588").pn	USPAT	2001/02/15 10:13		0
2	BRS	1	"5466623".PN.	USPAT	2001/02/12 11:05		0
3	BRS	1	"5468676".PN.	USPAT	2001/02/08 08:07		0
4	BRS	1	"5472905".PN.	USPAT	2001/02/08 08:08		0
5	BRS	1	"5473186".PN.	USPAT	2001/02/08 08:08		0
6	BRS	13	5473186.URPN.	USPAT	2001/02/08 08:09		0
7	BRS	1	"5457339".PN.	USPAT	2001/02/08 08:09		0
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9	BRS	1	"5468676".PN.	USPAT	2001/02/08 08:10		0
10	BRS	1	"5470783".PN.	USPAT	2001/02/08 08:10		0
11	BRS	1	"5472904".PN.	USPAT	2001/02/08 08:10		0
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Page 1 (CJohnson9, 02/21/2001, EAST Version: 1.01.0015)

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18	BRS	1	"5958795".PN.	USPAT	2001/02/08 08:13		0
19	BRS	4 3	(257/508) and (pn same junction)	USPAT	2001/02/09 08:17		0
20	BRS	1 8	4688069.URPN.	USPAT	2001/02/08 08:31		0
21	BRS	1 7 5	(257/506 or 257/509 or 257/508 or 257/545 or 257/598) and (pn same junction)	USPAT	2001/02/08 08:44		0
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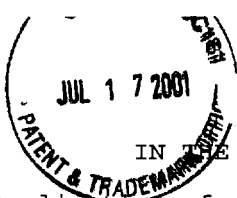
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30	BRS	1	"5731623".PN.	USPAT	2001/02/08 13:38		0
31	BRS	1	"5598015".PN.	USPAT	2001/02/08 13:39		0
32	BRS	1	"5598015".PN.	USPAT	2001/02/08 13:40		0
33	BRS	1	"5475257".PN.	USPAT	2001/02/08 13:40		0
34	BRS	1	"5444014".PN.	USPAT	2001/02/08 13:41		0
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36	BRS	1	"5319239".PN.	USPAT	2001/02/08 13:57		0
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39	BRS	1	"5457339".PN.	USPAT	2001/02/09 08:00		0
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43	BRS	1	"4939567".PN.	USPAT	2001/02/09 08:01		0
44	BRS	1	"4925805".PN.	USPAT	2001/02/09 08:01		0

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Page 4 (CJohnson9, 02/21/2001, EAST Version: 1.01.0015)

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64	BRS	1	"5319239".PN.	USPAT	2001/02/12 10:23			0
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70	BRS	1	"5093711".PN.	USPAT	2001/02/12 10:25			0
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72	BRS	1	"4862227".PN.	USPAT	2001/02/12 10:25			0
73	BRS	1	"4803528".PN.	USPAT	2001/02/12 10:26			0
74	BRS	1	"4717681".PN.	USPAT	2001/02/12 10:26			0
75	BRS	1	"4067100".PN.	USPAT	2001/02/12 10:26			0
76	BRS	1	"4849371".PN.	USPAT	2001/02/12 10:27			0
77	BRS	1	"4663831".PN.	USPAT	2001/02/12 10:27			0
78	BRS	1	"4404658".PN.	USPAT	2001/02/12 10:27			0
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83	BRS	1	5663588.pn.	USPAT	2001/02/15 10:19		0



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Takaaki UKEDA et al.

Serial No.: 09/469,498

Group Art Unit: 2822

Filed: December 22, 1999

Examiner: C. JOHNSON

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

AMENDMENT TRANSMITTAL

Honorable Commissioner of Patents
and Trademarks,
Washington, D.C. 20231

Sir:

1. X Transmitted herewith is an amendment for the above-identified application.

STATUS

2. X Applicant is is small entity - verified statement:
 attached already filed.
X other than a small entity.

EXTENSION OF TIME

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. §1.136 apply.

- (a) X Applicant petitions for an extension of time for the total number of months checked below:

EXTENSION (months)	FEE FOR SMALL ENTITY	FEE FOR OTHER THAN SMALL ENTITY
<u> </u> one month	\$ 55.00	\$ 110.00
<u>X</u> two months	195.00	390.00
<u> </u> three months	445.00	890.00
<u> </u> four months	695.00	1,390.00

Fee \$ 390.00

If an additional extension of time is required, please consider this a petition therefor.

 An extension for months has already been secured and the fee paid therefor of is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this Request \$

- (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time.

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4. X The fee for claims has been calculated as shown below:

	Claims Remaining After : Amendment	Highest Number Previously Paid For	Present Extra	Rate	Additional Fee
Total	:	:	:	:	:
Claims	: 20	: 20	: 0	: x \$ 18.00 =	: 0.00
Independent	:	:	:	:	:
Claims	: 4	: 4	: 0	: x \$ 80.00 =	: 0.00
Multiple Dependent Claims (first presentation)				: \$270.00 =	: 0.00
Total				=	: 0.00
Reduction by 1/2 for small entity				:	: 0
TOTAL FEE				:	: 0.00

(a) X No additional fee for claims is required.

-OR-

(b) The total additional fee for claims required \$.

FEE PAYMENT

5. Attached is a check in the amount of \$.

X Charge Deposit Account No. 50-0417 the amount of \$ 390.00. A duplicate copy of this Transmittal is enclosed for accounting purposes.

FEE DEFICIENCY

X If any additional extension and/or fee is required, this is the request therefor and to charge Deposit Account No. 50-0417.

AND/OR

X If any additional fee for claims is required, charge Deposit Account No. 50-0417. A duplicate copy of this Transmittal is enclosed for accounting purposes.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

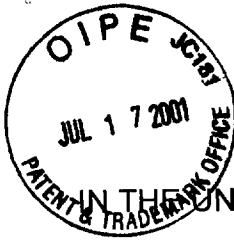
Date:

7/17/01

By:

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W., Suite 1200
Washington, D.C. 20005-3096
(202) 756-8000



ATTORNEY DOCKET NO. 43889-898

PATENT

#5/B(2)
T.BEL
7-24-01

UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Takaaki UKEDA et al.

Serial No.: 09/469,498

Filed : December 22, 1999
(DIV of SN: 08/978,137)

For: SEMICONDUCTOR DEVICE AND METHOD)
OF MANUFACTURING THE SAME)

)
) Group Art Unit: 2822
)
) Examiner: C. JOHNSON
)
)
)
)
)

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JUL 20 2001

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AMENDMENT UNDER 37 C.F.R § 1.111

Hon. Assistant Commissioner for Patents
Washington, DC 20231

Sir:

In response to the Office Action dated February 26, 2001, having a shortened statutory period for response set to expire May 26, 2001, a petition for two months extension of time up to and including July 26, 2001 being filed concurrently herewith, please amend the above-identified application as follows:

IN THE TITLE:

Please amend the title of the application to read --A TRENCH ISOLATED

SEMICONDUCTOR DEVICE--.

07/19/2001 ANABI1 00000057 500417 09469498

01 FC:116 390.00 CH

WDC99 459703-1.043889.0898

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IN THE DRAWINGS:

Please amend Fig. 1(a) as illustrated on the marked-up copy of the figure enclosed herewith. It is noted that the amendment to Fig. 1(a) corrects an inadvertent clerical error.

IN THE CLAIMS:

Please amend claims 1, 2, 4, 5, 8, 10, 11, 12, 15 and 16 and add new claims 39 and 40 to read as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

BB a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and

at least one PN junction formed in said dummy semiconductor portions underlying said wire.

2. (Amended) A semiconductor device according to claim 1, wherein said PN junction includes a plurality of PN junctions formed in said dummy semiconductor portions.

1/4. (Amended) A semiconductor device comprising:

- a semiconductor substrate having an active region and an isolation region surrounding said active region;
- a first trench portion filled with an insulating material formed to separate said active region from said isolation region;
- a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;
- an interlayer insulating film formed to extend continuously over said active region and said isolation region;
- a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and
- a dielectric film interposed between at least said dummy semiconductor portions of said isolation region and said interlayer insulating film.

1/6. (Amended) A semiconductor device according to claim 4, wherein said dielectric film is an underlying insulating film interposed between said interlayer insulating film and said dummy semiconductor portions and said second trench portion.

108. (Amended) A semiconductor device according to claim 4, wherein said dielectric film is formed in an upper portion of each of said dummy semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top face of each of said second trench portion.

110. (Amended) A semiconductor device comprising:

- a semiconductor substrate having an active region and an isolation region surrounding said active region;
- a first trench portion filled with an insulating material formed to separate said active region from said isolation region;
- a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;
- an interlayer insulating film formed to extend continuously over said active region and said isolation region;
- a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and
- a buried insulating film formed only in said isolation region, and in an inner portion of each of said dummy semiconductor portions in said isolation region.

111. (Amended) A semiconductor device comprising:

- a semiconductor substrate having an active region and an isolation region surrounding said active region;

a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and

a resistor film formed under said wire, and between said interlayer insulating film and at least said dummy semiconductor portions of said isolation region.

¹⁴₁₂. (Amended) A semiconductor device according to claim ¹³₁₁, wherein said resistor film is an underlying resistor film formed to extend continuously over said dummy semiconductor portions and said second trench portions.

¹⁷₁₅. (Amended) A semiconductor device according to claim ¹⁶₁₂, further comprising a FET having a gate electrode composed of a first conductor film formed on the semiconductor portion within said active region and a second conductor film deposited on said first conductor film, wherein

a top surface of the first conductor film of said gate electrode is at approximately the same level as a top surface of said first trench portion and said second trench portion,

a region of said resistor film overlying each of said semiconductor portions is formed of the same two films as composing said first and second conductor films of said gate electrode, and

a region of said resistor film overlying said first trench portion and said second trench portion is composed of the same material as composing said first conductor film of said gate electrode.

~~18~~ 15. (Amended) A semiconductor device according to claim ~~11~~ 13, wherein said resistor film is formed in an upper portion of each of said dummy semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top surface of said second trench portion.

Please add new claims 39 and 40 as follows:

~~139~~ 39. (New) A semiconductor device according to claim 1, wherein said PN junction formed in said dummy semiconductor portion is positioned at a level between a top surface and a bottom surface of said second trench portion.

~~140~~ 40. (New) A semiconductor device according to claim 1, wherein said PN junction formed in said dummy semiconductor portion is positioned at a level below a bottom surface of said second trench portion.

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claims 1, 2, 4, 5, 8, 10, 11, 12, 15 and 16 so as to clarify the intended subject matter of the present invention. In addition, new claims 39 and 40 have been added. Support for new claims 39 and 40 can be found in Figs. 1 and 3 and the corresponding disclosure set forth in the specification. No new matter has been added.

In addition, Applicants have amended Fig. 1(a) to indicate that reference numeral 9 corresponds to the "dummy semiconductor portion", and not the trench portion as erroneously indicated in the figure as originally filed. Support for the amendment can be found on page 27, lines 10-11 of the specification.

Finally, a copy of the PTO-1449 form originally submitted in an Information Disclosure Statement filed on December 12, 1999 is being enclosed herewith. A correction has been made to the sixth reference identified in the "Foreign Patent Documents" section. Specifically, reference number 02-20500 was incorrectly indicated as being a Japanese reference in the original PTO-1449 form. As set forth on the new form, the reference is a European reference. It is respectfully requested that the file in the USPTO be updated to reflect this correction such that any patent issuing from the above-identified application properly indicates the prior art of record.

For the following reasons, Applicants respectfully submit that the pending claims are not anticipated by the prior art for the reasons set forth below.

II. Claims 1-9 Are Not Anticipated By Ishimaru

Claims 1-9 were rejected under 35 U.S.C. § 102 as being anticipated by Ishimaru (USP No. 5,731,623). Applicants respectfully submit that claims 1-9, as amended, are clearly not anticipated by Ishimaru for the following reasons.

A. Claims 1-3

As recited by claims 1-3, the present invention relates to a novel trench-isolated semiconductor device. One of the novel features of the invention is the formation of an impurity region in the dummy semiconductor portions so as to result in the formation of at least one PN junction in the dummy semiconductor portions.

More specifically, it is a known technique to form dummy semiconductor portions in an isolation region in order to obtain an isolation region having a planarized surface. Indeed, without such dummy semiconductor portions, it would be difficult to obtain a planarized surface of the isolation region. However, prior to the present invention there has been the problem that the formation of the dummy semiconductor portions increases the wiring-to-substrate capacitance in the isolation region, as is described in the "BACKGROUND OF THE INVENTION" portion of the specification and Figs. 21(a)-21(c).

The Applicants' have discovered that the formation of the PN junction in the dummy semiconductor portions in the isolation region overcomes the foregoing problem. Specifically, as shown in Fig. 1(b) while the formation of the dummy semiconductor portions 9 produces an additional capacitance C_{j1} , because of formation of the PN junction 22 within the dummy semiconductor portions 9, the capacitance C_{j1}

is added in series to a capacitance C_{al} , which decreases the wiring-to-substrate capacitance in the isolation region. As a result, the operational speed of the device is advantageously increased.

Turning to the pending claims, claim 1 recites in-part that a second trench portion is formed in a dummy semiconductor portion and that at least one PN junction is formed in the dummy semiconductor portion.

Turning to the cited prior art, at a minimum, Ishimaru fails to disclose a second trench portion filled with an insulating material formed so as to separate a plurality of dummy semiconductor portions in the isolation region. Indeed, Ishimaru does not disclose or suggest the use of any dummy semiconductor portions. For example, referring to Fig. 6, the two semiconductor portions disclosed therein are utilized to form a bipolar transistor and a MOS transistor. There are no dummy semiconductor portions.

Specifically, the trenches 11e, 11f and 11a of Fig. 5 and Fig. 6 as disclosed by Ishimaru all correspond with the first trench portion of the present invention. These trenches are formed to separate the bipolar transistor region from the MOS transistor region. Moreover, trenches 11g and 11d are formed to separate the base layer 22, which is formed in the bipolar transistor region (active region) from the buried collector lead electrode layer 20.

Thus, the plurality of trench portions (11a-11f) disclosed by Ishimaru do not correspond with the second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in isolation region as set forth in claims 1, 4, 10 and 12 of the present invention.

Continuing, as Ishimaru fails to disclose a dummy semiconductor portion, Ishimaru also fails to disclose at least one PN junction being formed in the dummy semiconductor portion.

Furthermore, Ishimaru fails to disclose or suggest a wire formed on the interlayer insulating film covering the dummy semiconductor portions and the second trench portion in the isolation region, as set forth in at least Claims 1, 4, 10 and 11 of the present invention.

It is asserted in the pending rejection that Ishimaru teaches a wire (30, 44) formed on an interlayer insulating film in Fig. 2. However, trenches 11a and 11b of Fig. 2 as disclosed by Ishimaru correspond with the first trench portion of the present invention, as the bipolar transistor region (active region) is formed between trenches 11a and 11b. Thus, the wire (30, 44) disclosed by Ishimaru is formed on the active region, which is different from the wire formed on the interlayer insulating film covering the dummy semiconductor portions and the second trench portion in the isolation region, as recited by the pending claims.

It is further noted that Figs. 1 and 2 of Ishimaru relate to prior art to the device disclosed in Figs. 5 and 6 of Ishimaru. Accordingly, absent some motivation to combine the teaching of the prior art identified by Ishimaru with Ishimaru's alleged novel device, it is improper to pick and choose elements from different figures of Ishimaru representing unrelated devices when attempting to formulate an anticipation rejection under 35 U.S.C. § 102.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency,

in a single prior art reference, *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for all of the foregoing reasons, it is clear that Ishimaru does not anticipate either claim 1, or any claim dependent thereon.

B. Claims 4-9

Claims 4-9 were also rejected as being anticipated by Ishimaru. However, similar to claim 1, claim 4 also recites the formation of a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in the isolation region, and the formation of a dielectric film interposed between the dummy semiconductor portions and an interlayer insulating film.

In accordance with the device corresponding to claim 4, the capacitance component of the wiring-to-substrate capacitance in the region containing the dummy semiconductor portions of the isolation region is obtained by adding in series the capacitance in the dielectric film to the capacitance in the interlayer film. As a result, the total wiring-to-substrate capacitance is advantageously lowered. Consequently, the operating speed of the semiconductor device of the present invention is increased.

As explained above, at a minimum, Ishimaru fails to disclose: (1) a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in the isolation region; or (2) a wire formed on the interlayer insulating film covering the dummy semiconductor portions and the second trench portion in the isolation region.

As such, it is clear that Ishimaru also fails to anticipate either claim 4, or any of claims 5-9, which depend on claim 4.

Accordingly, for all of the foregoing reasons, it is respectfully submitted that claim 1-9 are not anticipated by Ishimaru.

III. **Claims 10-18 Are Not Anticipated By Suzuki**

Claims 10-18 were rejected under 35 U.S.C. § 102 as being anticipated by Suzuki (USP No. 5,663,588). Applicants respectfully submit that claims 10-18, as amended, are clearly not anticipated by Suzuki for the following reasons.

According to the semiconductor device of the present invention as recited by claim 10, the buried insulating film is formed **only** in the isolation region. As a result, the buried insulating film of the present invention is **not** formed below the active region. For example, referring to Fig. 14(a) of the present invention, as shown the buried insulating film 91 is formed only in the isolation region 7 and therefore is not formed below the active region 6 containing the MOSFET.

Turning to the prior art, Suzuki discloses a device comprising a buried oxide film 12 formed beneath a SOI substrate 13. However, as shown in Fig. 1B of Suzuki, the buried oxide film 12 is formed below both the active region and the isolation region. Thus, at a minimum, Suzuki fails to disclose a device having a buried insulating film formed only in the isolation region as recited by claim 10.

In addition, Suzuki fails to disclose or suggest a wire formed on the interlayer insulating film covering the dummy semiconductor portions and the second trench portion in the isolation region, as recited by both claims 10 and 11.

Continuing with claim 11, the claimed device further includes a resistor film which is formed under the wire and in between the interlayer insulating film and at least the

dummy semiconductor portions of the isolation region. Accordingly, the resistor film is formed in between the wiring and the dummy semiconductor portions. However, in contrast, Suzuki fails to disclose any feature above the gate wiring 18, which functions as a resistor film that corresponds to the wiring of the present invention.

It is asserted that Suzuki discloses a wiring (22) formed on the interlayer insulating film as shown in Fig.1B of Suzuki. However, the wiring (22) disclosed by Suzuki is formed on the active region, which is different from the wire formed on the interlayer insulating film covering the dummy semiconductor portions and the second trench portion in the isolation region, as recited by claim 11.

Accordingly, for all of the foregoing reasons, it is clear that Suzuki fails to anticipate either claim 10 or 11 or any claim dependent thereon.

IV. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an


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Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 7/17/21

By: 
Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W. , Suite 1200
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

WDC99 459703-1.043889.0898



VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title has been amended to read --A TRENCH ISOLATED SEMICONDUCTOR DEVICE--.

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IN THE CLAIMS:

Claims 1, 2, 4, 5, 8, 10, 11, 12, 15 and 16 have been amended as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

[a plurality of trench portions each formed in said isolation region and filled with an insulating material;

semiconductor portions interposed between said individual trench portions in said isolation region;]

a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

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a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and
at least one PN junction formed in said dummy semiconductor portions underlying said wire.

2. (Amended) A semiconductor device according to claim 1, wherein said PN junction includes a plurality of PN junctions formed in said dummy semiconductor portions.

4. (Amended) A semiconductor device comprising:
a semiconductor substrate having an active region and an isolation region surrounding said active region;
[a plurality of trench portions each formed in said isolation region and filled with an insulating material;

semiconductor portions interposed between said individual trench portions in said isolation region;]

a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and
a dielectric film interposed between at least said dummy semiconductor portions of said isolation region and said interlayer insulating film.

5. (Amended) A semiconductor device according to claim 4, wherein said dielectric film is an underlying insulating film interposed between said interlayer insulating film and said dummy semiconductor portions and said second trench [portions] portion.

8. (Amended) A semiconductor device according to claim 4, wherein said dielectric film is formed in an upper portion of each of said dummy semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top face of each of said second trench [portions] portion.

10. (Amended) A semiconductor device comprising:
a semiconductor substrate having an active region and an isolation region surrounding said active region;
[a plurality of trench portions each formed in said isolation region and filled with an insulating material;
semiconductor portions interposed between said individual trench portions in said isolation region;]

a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and

a buried insulating film formed only in said isolation region, and in an inner portion of each of said dummy semiconductor portions in said isolation region.

11. (Amended) A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

[a plurality of trench portions each formed in said isolation region and filled with an insulating material;

semiconductor portions interposed between said individual trench portions in said isolation region;]

a first trench portion filled with an insulating material formed to separate said active region from said isolation region;

a second trench portion filled with an insulating material formed to separate a plurality of dummy semiconductor portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film covering said dummy semiconductor portions and said second trench portion in said isolation region; and

a resistor film formed under said wire, and between said interlayer insulating film and at least said dummy semiconductor portions of said isolation region.

12. (Amended) A semiconductor device according to claim 11, wherein said resistor film is an underlying resistor film formed to extend continuously over said dummy semiconductor portions and said second trench portions.

15. (Amended) A semiconductor device according to claim 12, further comprising a FET having a gate electrode composed of a first conductor film formed on the semiconductor portion within said active region and a second conductor film deposited on said first conductor film, wherein

a top surface of the first conductor film of said gate electrode is at approximately the same level as a top surface of [each of] said first trench [portions] portion and said second trench portion,

a region of said resistor film overlying each of said semiconductor portions is formed of the same two films as composing said first and second conductor films of said gate electrode, and

a region of said resistor film overlying [each of] said first trench [portions] portion and said second trench portion is composed of the same material as composing said first conductor film of said gate electrode.

16. (Amended) A semiconductor device according to claim 11, wherein said resistor film is formed in an upper portion of each of said dummy semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top surface of [each of] said second trench [portions] portion.

Please add new claims 39 and 40 as follows:

39. (New) A semiconductor device according to claim 1, wherein said PN junction formed in said dummy semiconductor portion is positioned at a level between a top surface and a bottom surface of said second trench portion.

40. (New) A semiconductor device according to claim 1, wherein said PN junction formed in said dummy semiconductor portion is positioned at a level below a bottom surface of said second trench portion.



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/469,498 12/22/99 UKEDA

T 43889/898

020277
MCDERMOTT WILL & EMERY
600 13TH STREET, N.W.
WASHINGTON DC 20005-3096

MMC2/1016

EXAMINER

MEIER, S
ART UNIT PAPER NUMBER

2822
DATE MAILED:

10/16/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Notice of Allowability	Application No.	Applicant(s)	
	09/469,498	UKEDA ET AL.	
	Examiner	Art Unit	
	Stephen D. Meier	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to communication of 7/17/01.
2. ☒ The allowed claim(s) is/are 1-18, 39 and 40.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 08/978,137.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**


7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8. ☒ CORRECTED DRAWINGS must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No. _____.
 - (b) ☒ including changes required by the proposed drawing correction filed 17 July 2001, which has been approved by the Examiner.
 - (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1 <input type="checkbox"/> Notice of References Cited (PTO-892) 3 <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 5 <input checked="" type="checkbox"/> Information Disclosure Statements (PTO-1449), Paper No. _____ 7 <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material	2 <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 4 <input type="checkbox"/> Interview Summary (PTO-413), Paper No. _____ 6 <input type="checkbox"/> Examiner's Amendment/Comment 8 <input type="checkbox"/> Examiner's Statement of Reasons for Allowance 9 <input type="checkbox"/> Other
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Stephen D. Meier
 Primary Examiner



NOTICE OF ALLOWANCE AND ISSUE FEE DUE

020277
MCDERMOTT MILL & EMERY
600 13TH STREET, N.W.
WASHINGTON DC 20005-3096

MMC2/1016

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/469,498	12/22/99	020	MEIER, S	2002 10/16/01
First Named Applicant	UKEDA, 35 USC 154(b) term ext. = 0 Days.			

TITLE OF INVENTION / A TRENCH ISOLATED SEMICONDUCTOR DEVICE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3 43849/898	257-509.000	N51	UTILITY	NO	\$1280.00	01/16/02

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

- I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or

B. If the status is the same, pay the FEE DUE shown above.
- If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.
- II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.
- III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 06/30/99. (0651-0033)

Form PTO-1449 (NW&E Ver. REV. 7-96)		US Dept. of Commerce PATENT & TRADEMARK OFFICE		ATTY DOCKET NO. 43889-898		APPLICATION 09/469,498	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) <div style="border: 2px solid black; border-radius: 50%; width: 100px; height: 100px; margin: 10px auto; text-align: center; line-height: 100px;"> JUL 17 2001 PATENT & TRADEMARK OFFICE </div>				APPLICANT: Takaaki UKEDA et al.			
				FILING DATE: December 22, 1999		GROUP: 2822	

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
u		3,622,382	11/23/71	Brack et al.	428	448	
		4,929,566	05/29/90	Beitman	438	423	
		4,948,742	08/14/90	Nishimura et al.	438	423	
		5,426,062	06/20/95	Hwang	438	423	
		5,270,265	12/14/93	Hemmenway et al.	438	404	
		5,760,444	06/02/98	Okumura	257	350	
		5,856,218	01/05/99	Kinoshita et al.	438	414	
		5,877,066	03/02/99	Stolmeijer et al.	438	424	
		5,665,633	09/09/97	Meyer	/		
y		5,663,588	02/09/97	Suzuki et al.	/		

FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION	
							YES	NO
u		63-246842	10/13/88	JAPAN	/		XX	
		60-015944	01/26/85	JAPAN	/		XX	
		05-013565	01/22/93	JAPAN	/		XX	
		05-38807	10/20/92	EUROPE	/		XX	
		02-272745	11/07/90	JAPAN	/		XX	
		02-20500	09/25/86	EUROPE	/		XX	
u		58-200554	11/22/83	JAPAN	/		XX	

EXAMINER <div style="font-family: cursive; font-size: 1.2em;">S. Maier</div>	DATE CONSIDERED <div style="font-family: cursive; font-size: 1.2em;">10/4/01</div>
---	---

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

DEPARTMENT PPC PP

TEAM TI

PATENT # 05503670

WEEK DATE 10-29-01

RESEARCH REQUEST

Need description for 13(i) - reference is
made to 13(i) in CA 23

Action Requested by: Claudia Date: 12-3

DESCRIPTION OF RESOLUTION

Please complete Disposition section

Figure 13 i is now described
on page 25

Action Requested by: JF Date: 12-28

DISPOSITION

☐ MAKE CORRECTION:

☐ In Production

☐ External Department: _____
Please specify department and wand to group

☐ USE AS IS

☐ COMMUNICATION:

☐ Distribute Department wide as example only

☐ Manual Improvement/Suggestion Form Needed*
*Response is for this patent only unless this box is checked

☐ NON CONFORMING:

☐ Return on Query

☐ Return to FMF

~ Do not release non-conforming files ~

PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with application fees, to:

Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

DEC 12 2001

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

020277
MCDERMOTT WILL & EMERY
600 13TH STREET, N.W.
WASHINGTON DC 20005-3096

MMC2/1016

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/469,498	12/22/99	020	MEIER, S	2822 10/16/01
First Named Applicant	UKEDA,	35 USC 154(b) term ext. =	0 Days.	

TITLE OF INVENTION A TRENCH ISOLATED SEMICONDUCTOR DEVICE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3	43889/898	257-509.000	N51 UTILITY	NO	\$1280.00	01/16/02

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 McDERMOTT, WILL
& EMERY
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

(B) RESIDENCE: (CITY & STATE OR COUNTRY)

Osaka, JAPAN

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

- ☐ Issue Fee
- ☐ Advance Order - # of Copies _____

4b. The following fees or deficiency in these fees should be charged to:

DEPOSIT ACCOUNT NUMBER 500417
(ENCLOSE AN EXTRA COPY OF THIS FORM)

- ☒ Issue Fee 4
- ☒ Advance Order - # of Copies _____

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature)

Michael E. Fogarty, Reg. #36,139

(Date)

12/12/2001

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

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12.00 CN

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PTOL-85B (REV.10-96) Approved for use through 06/30/99. OMB 0651-0033

Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Docket No.: 43889-898



#8
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Takaaki UKEDA

Serial No.: 09/469,498

Filed: December 22, 1999

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:
:

BATCH NO.: N51

Group Art Unit: 2822

Allowed: October 16, 2001

Examiner: S. Meier

For: A TRENCH ISOLATED SEMICONDUCTOR DEVICE (As Amended)

LETTER SUBMITTING FORMAL DRAWINGS

Box Issue Fee
Commissioner for Patents
Washington, DC 20231

Sir:

In response to the Notice of Allowability dated October 16, 2001, submitted herewith are twenty-one (21) sheets of Formal Drawings in connection with the above referenced application.

Respectfully submitted,

MCDERMOTT, WILL & EMERY


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 MEF:blp
Date: December 12, 2001
Facsimile: (202) 756-8087

Fig. 1(a)

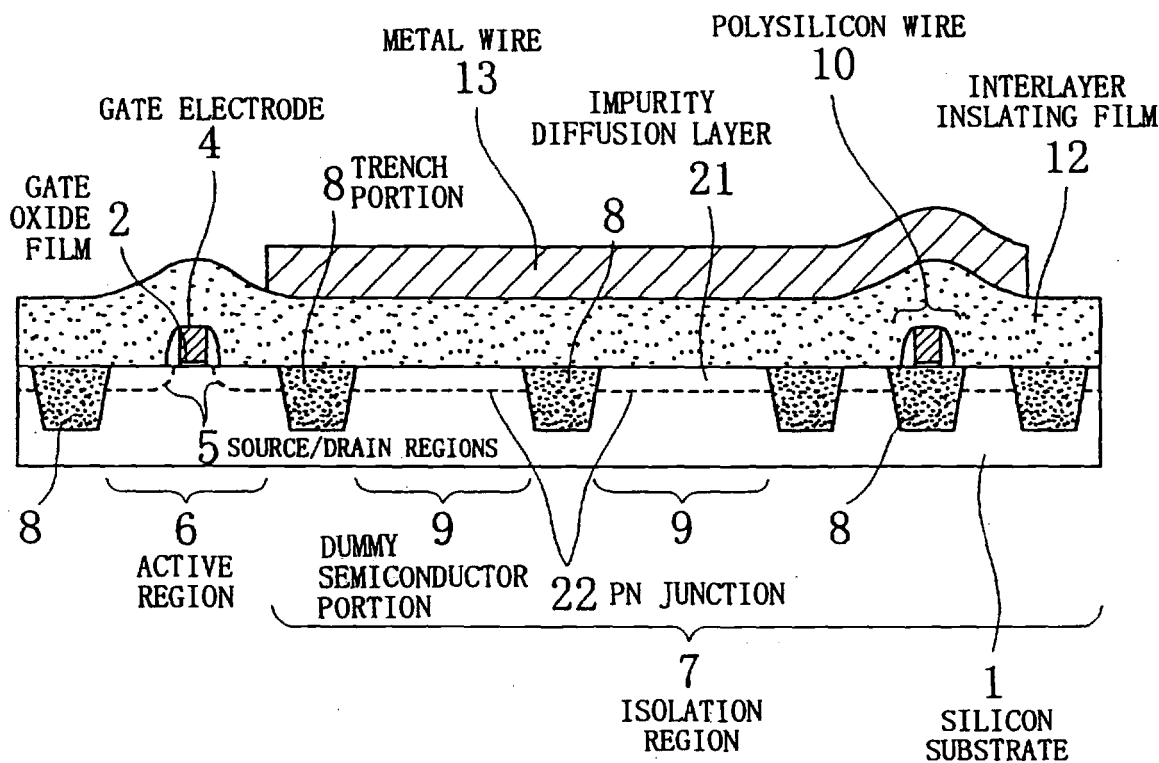
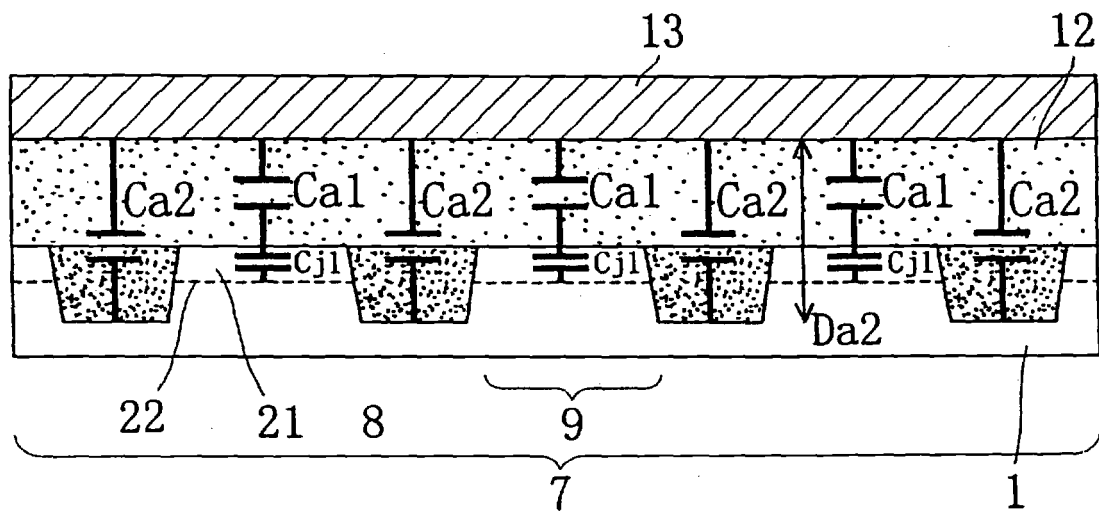


Fig. 1(b)



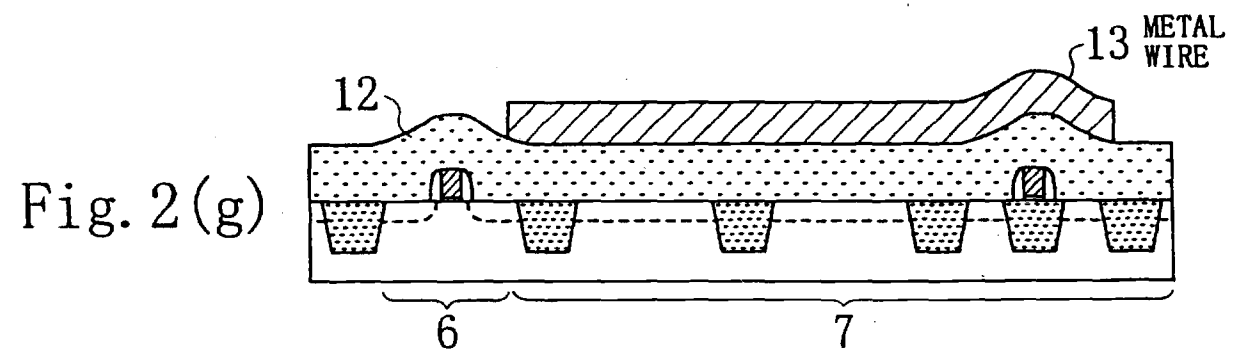
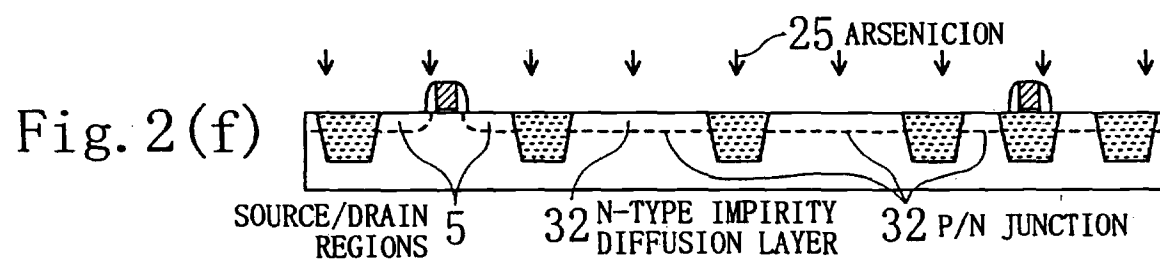
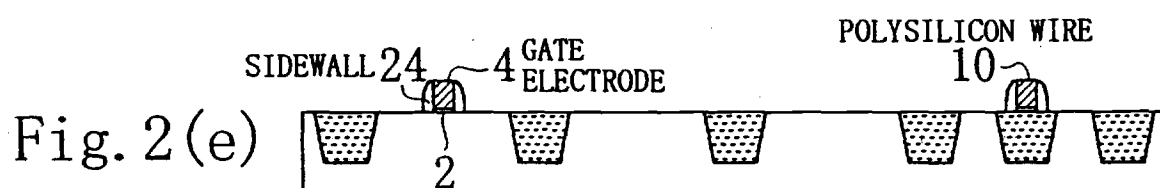
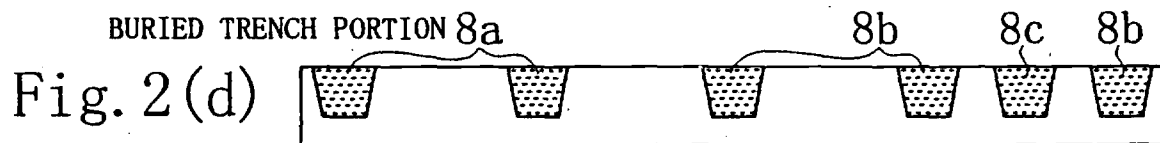
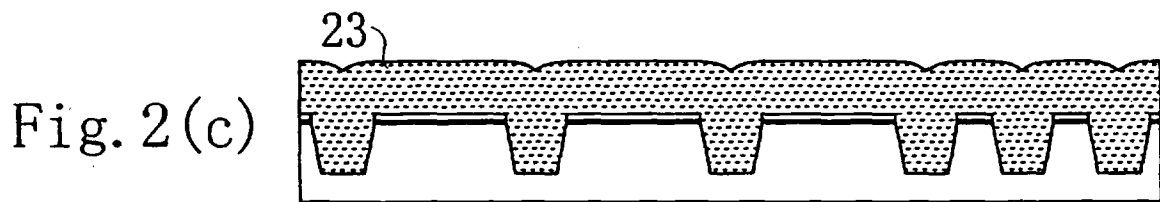
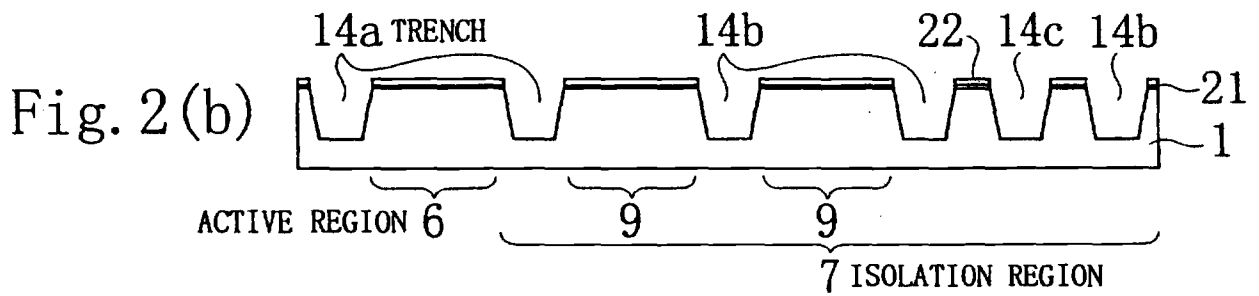
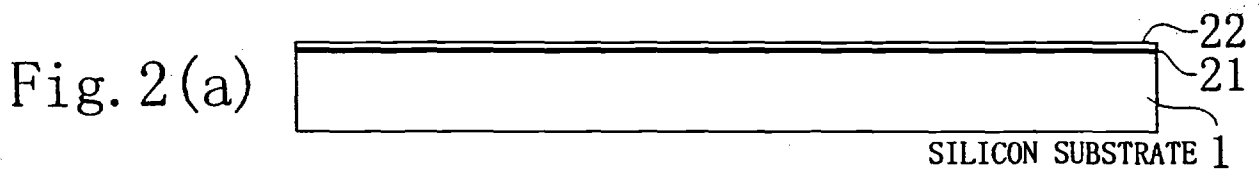


Fig. 3

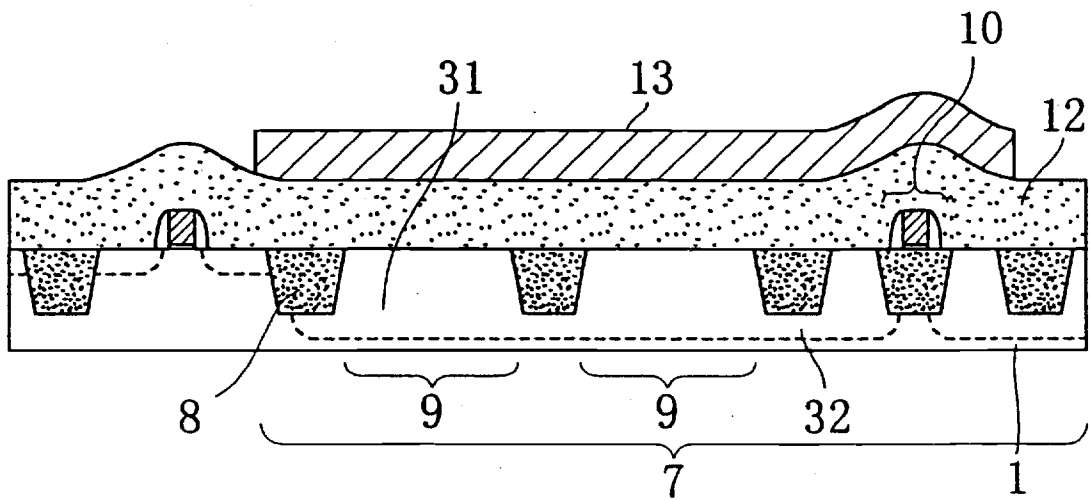


Fig. 4

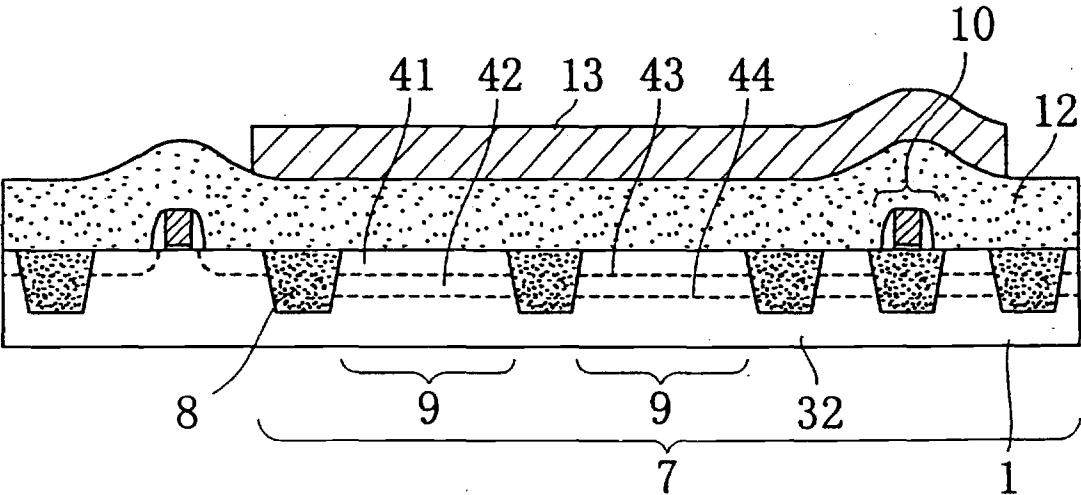
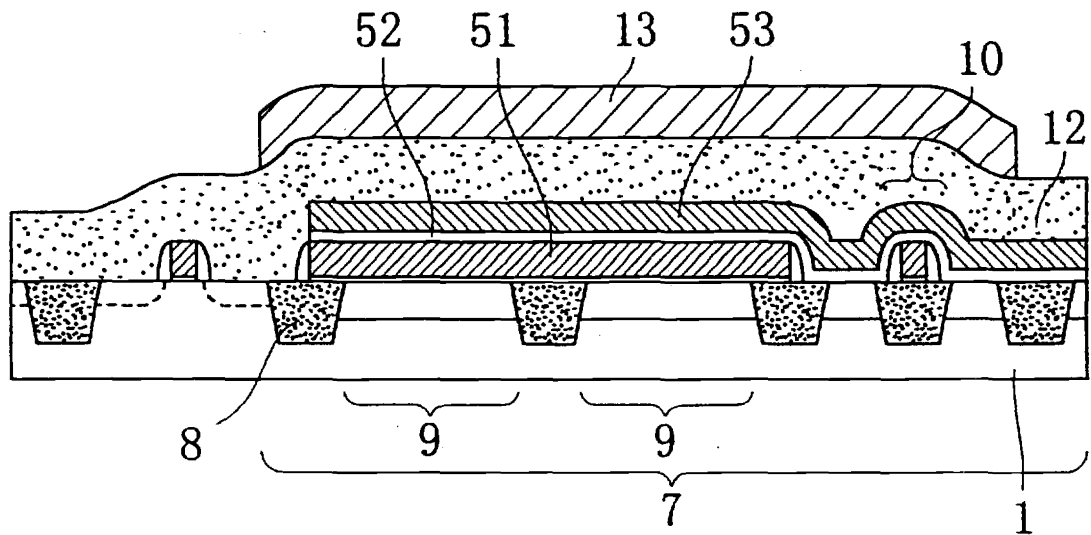


Fig. 5



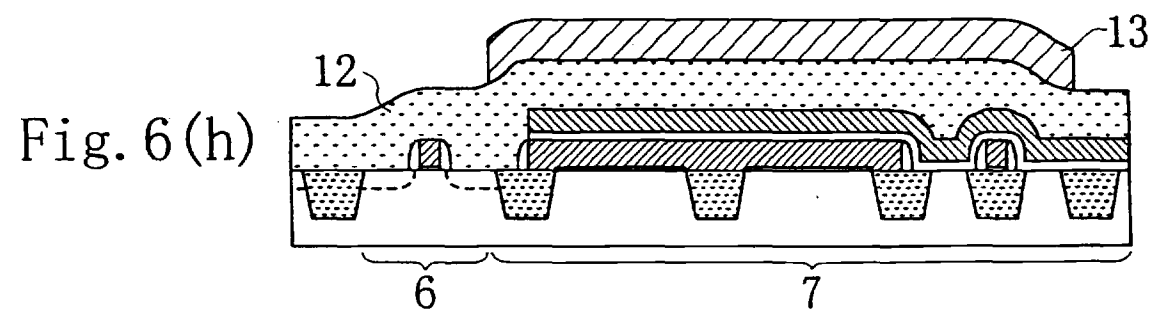
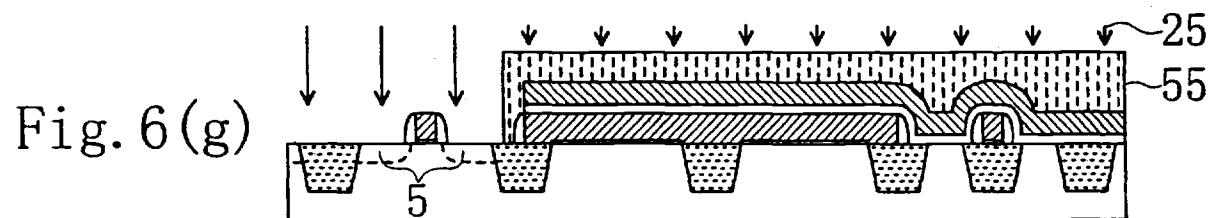
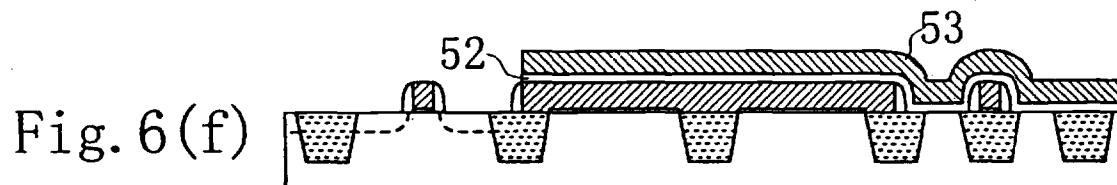
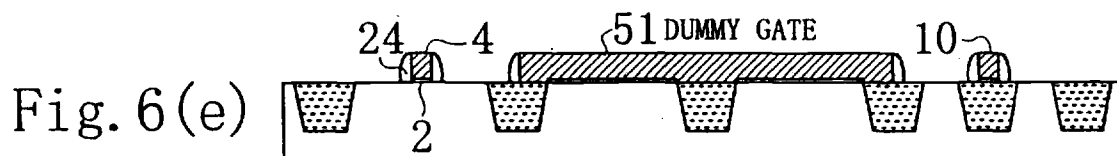
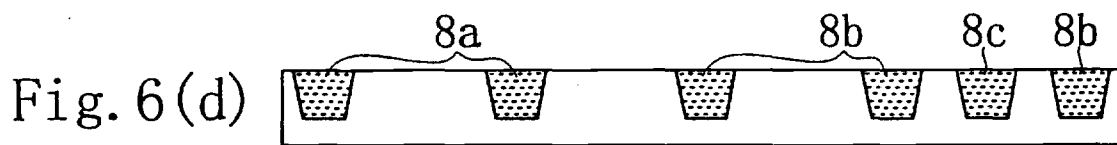
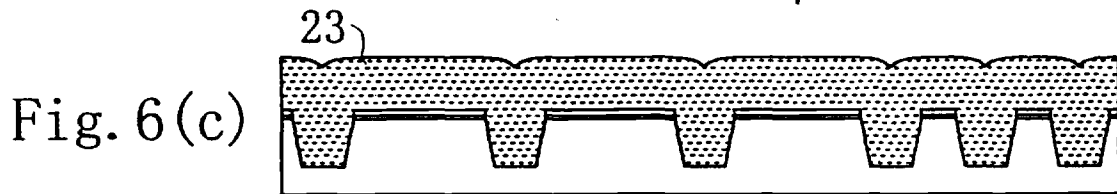
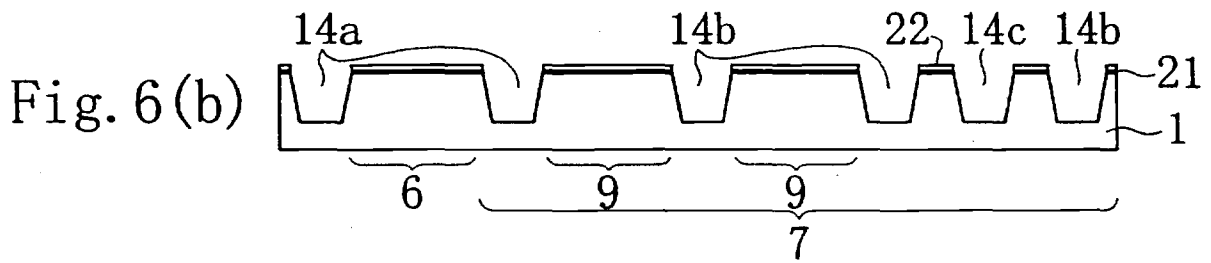


Fig. 7

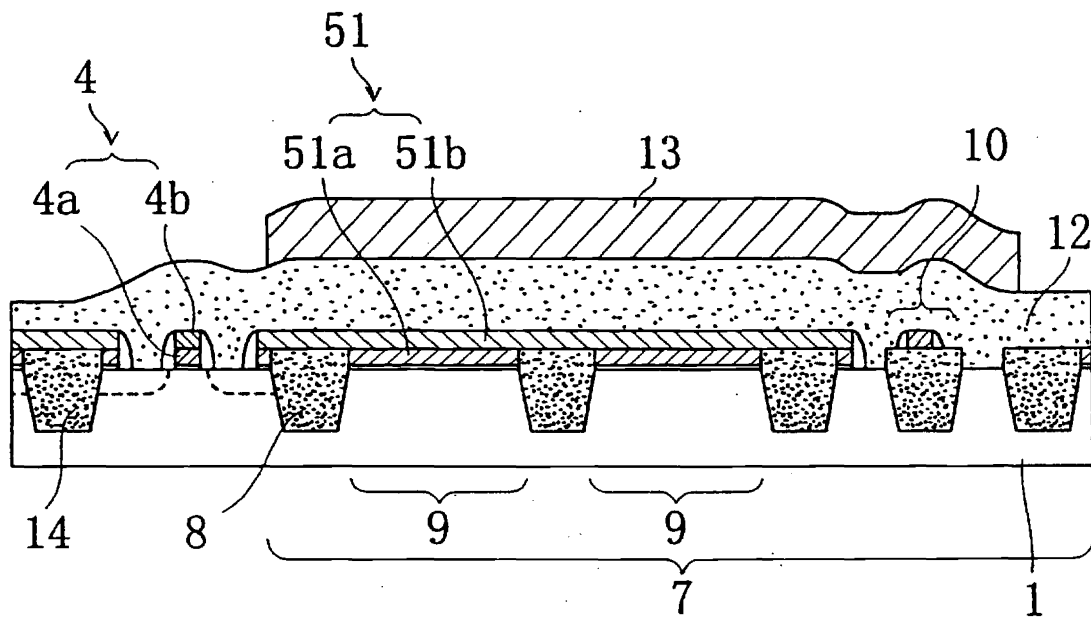
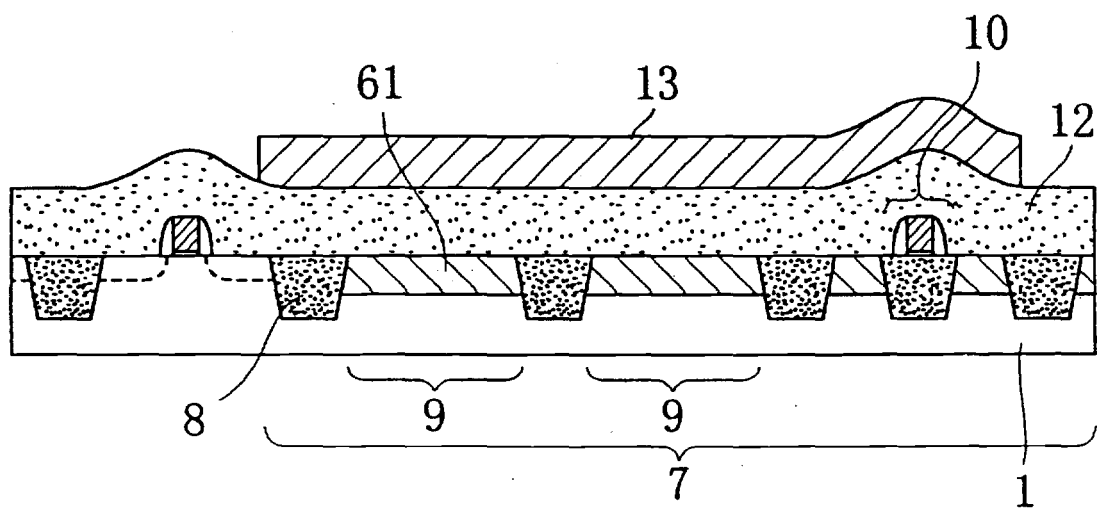


Fig. 8



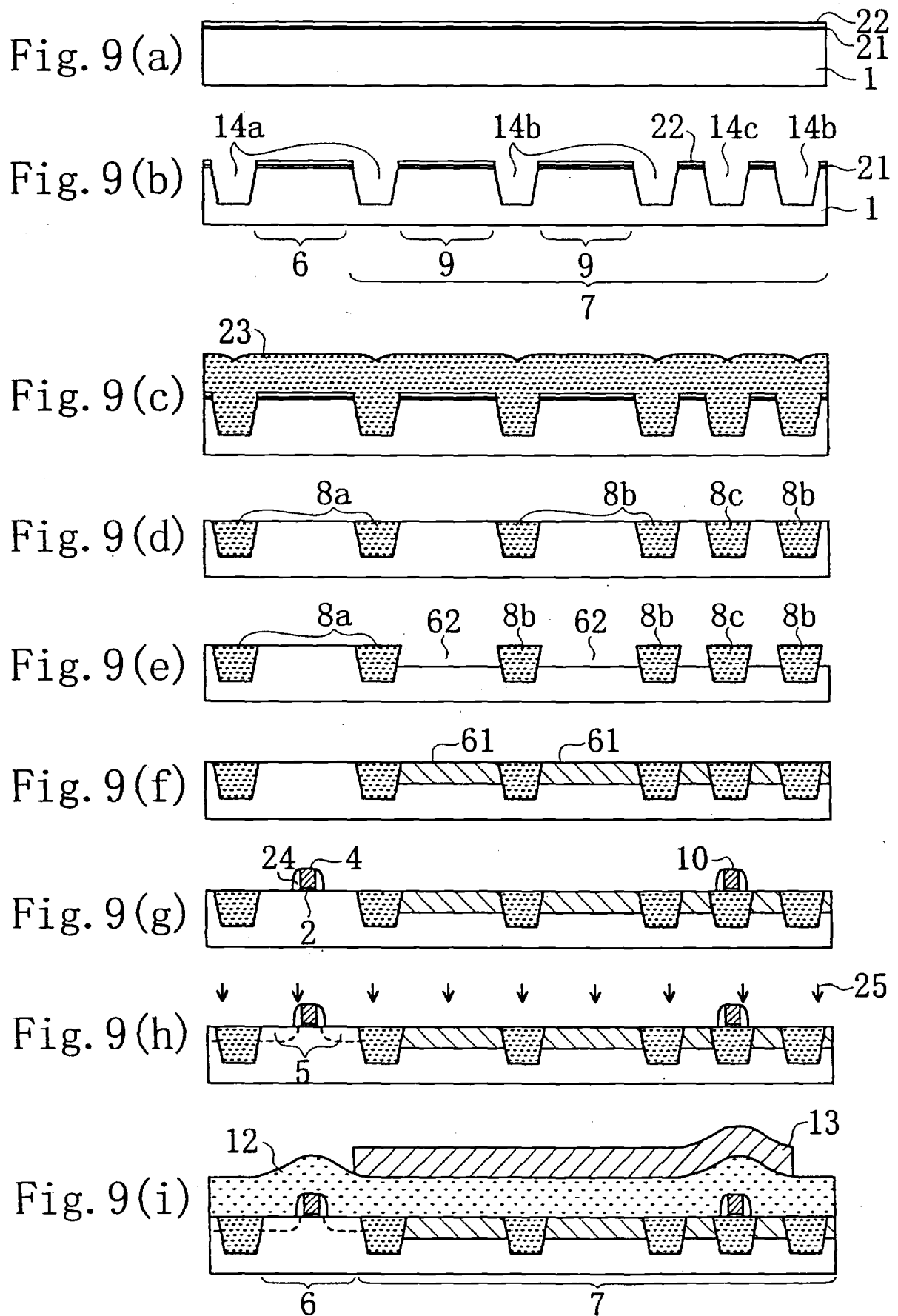
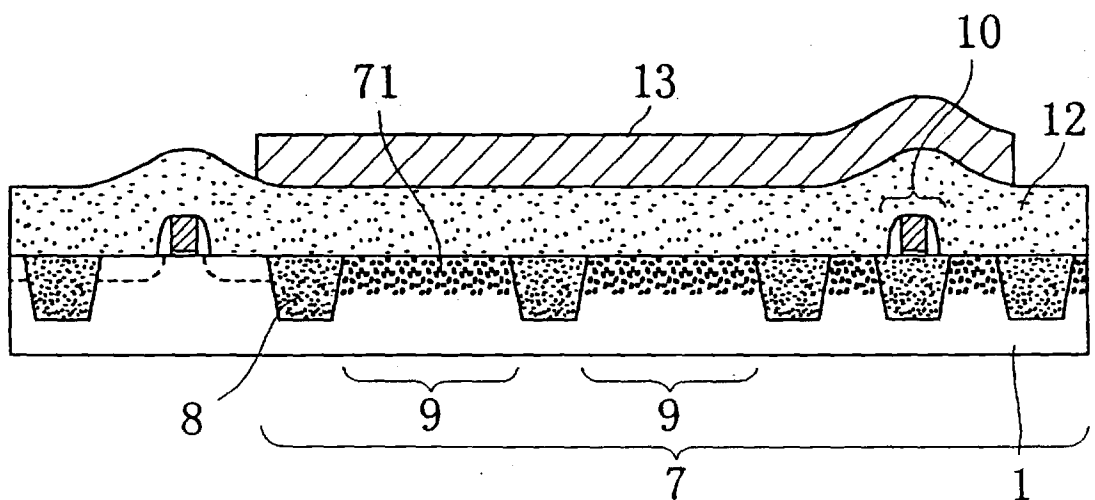


Fig. 10



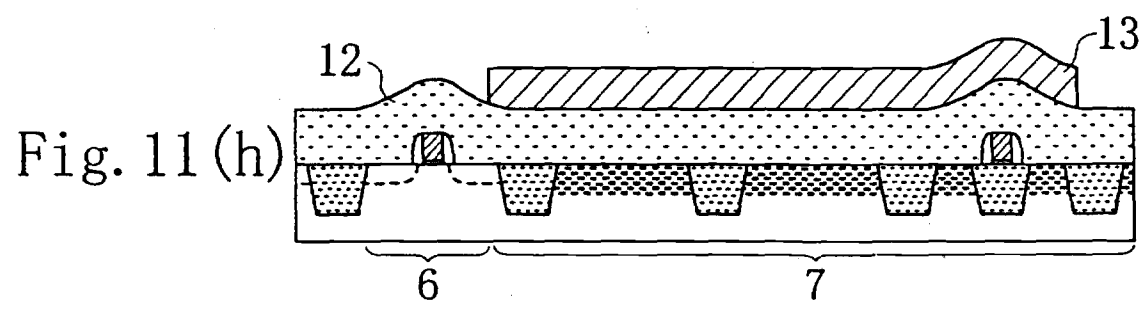
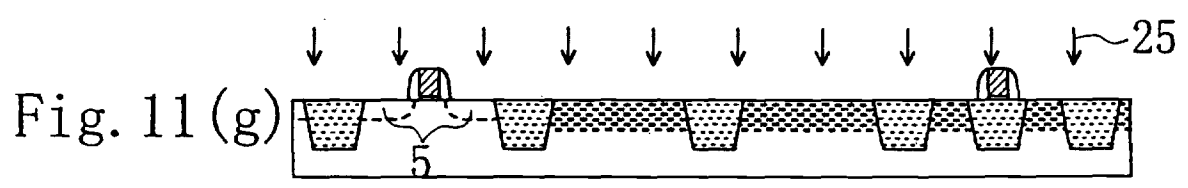
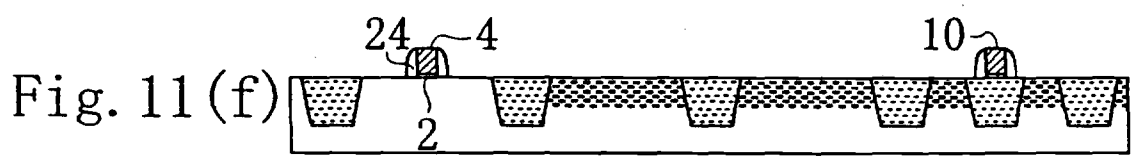
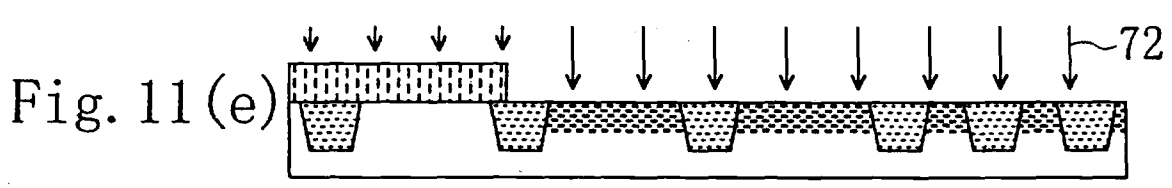
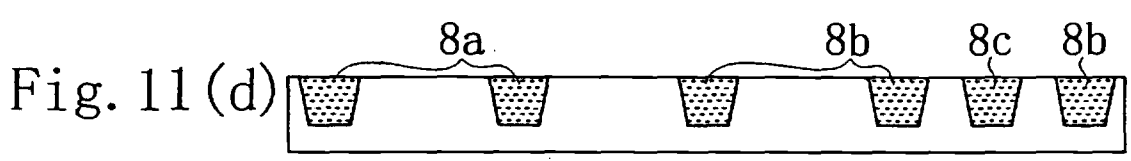
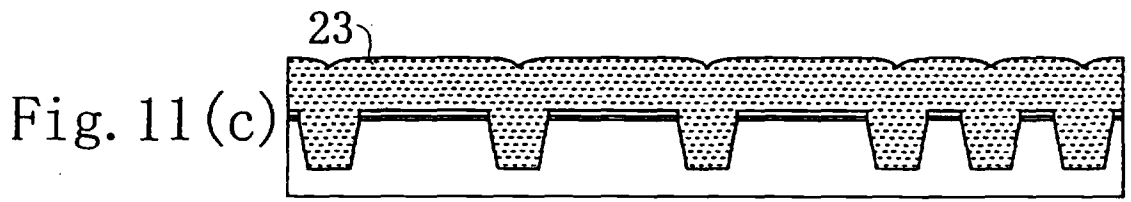
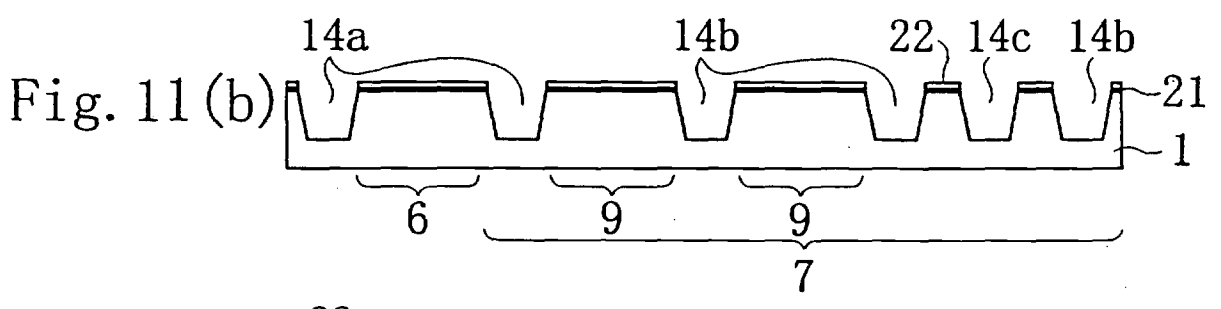
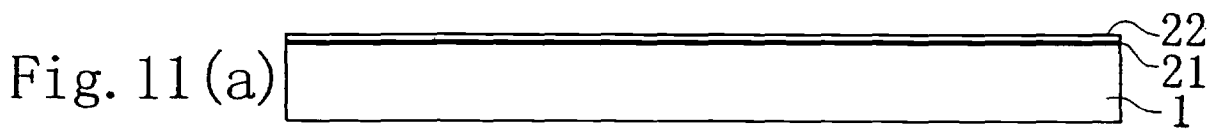
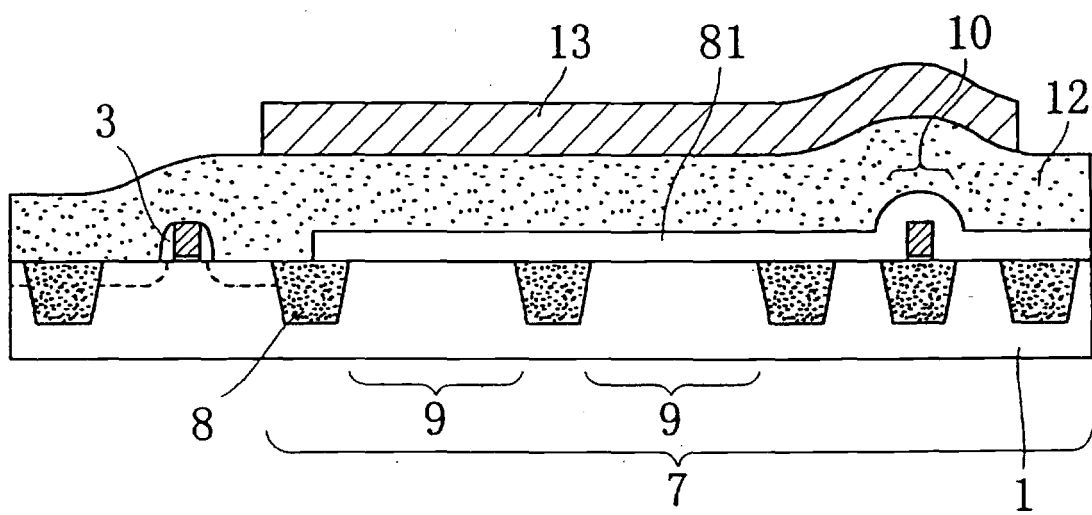


Fig. 12



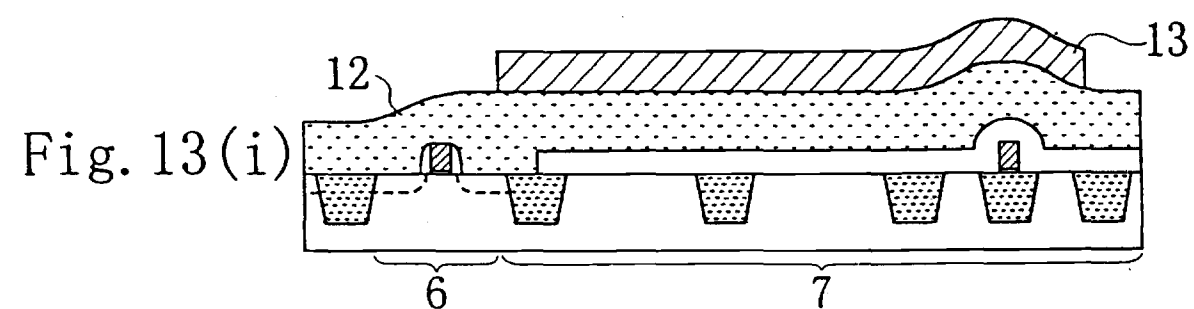
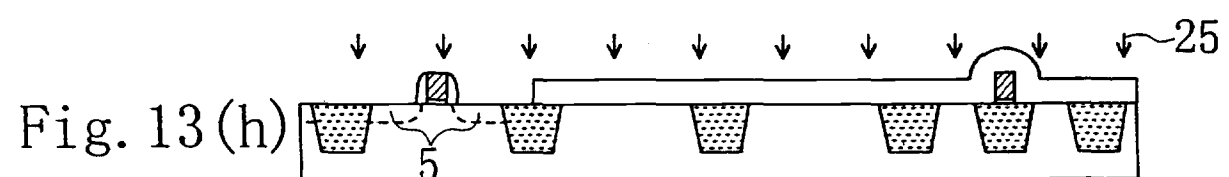
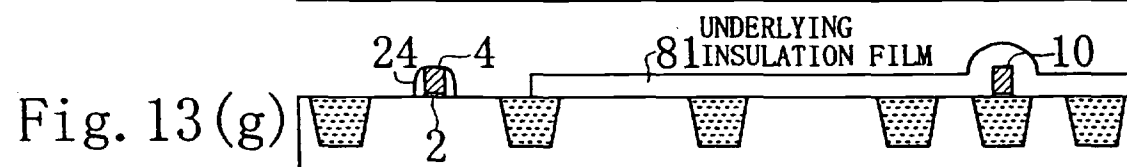
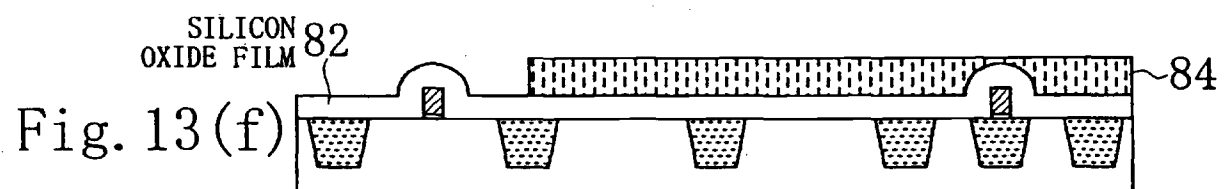
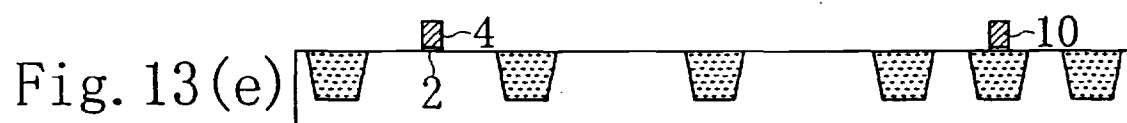
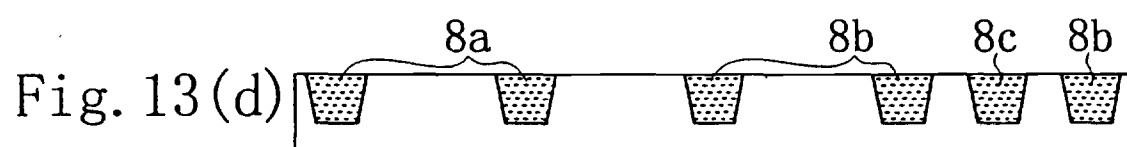
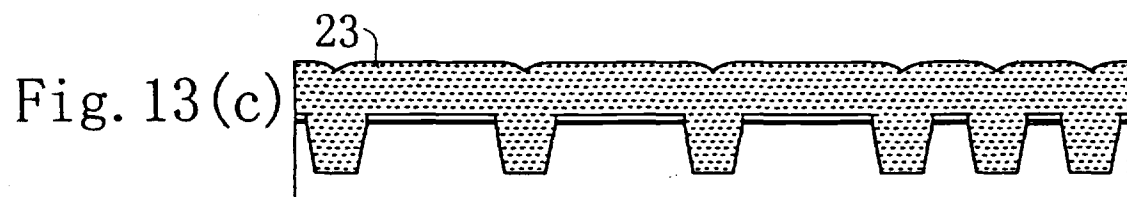
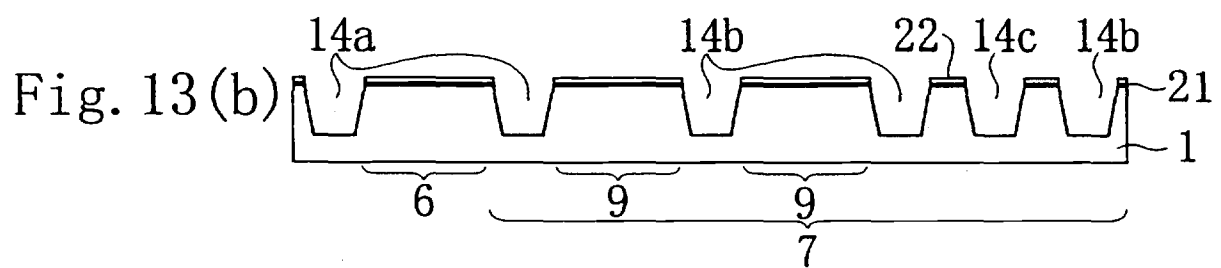
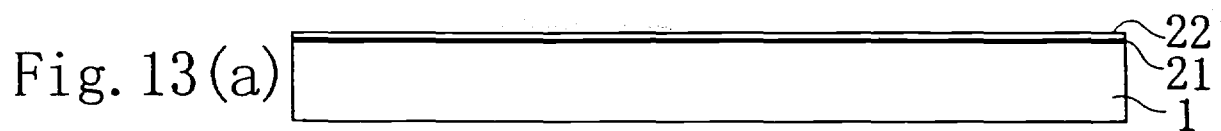


Fig. 14(a)

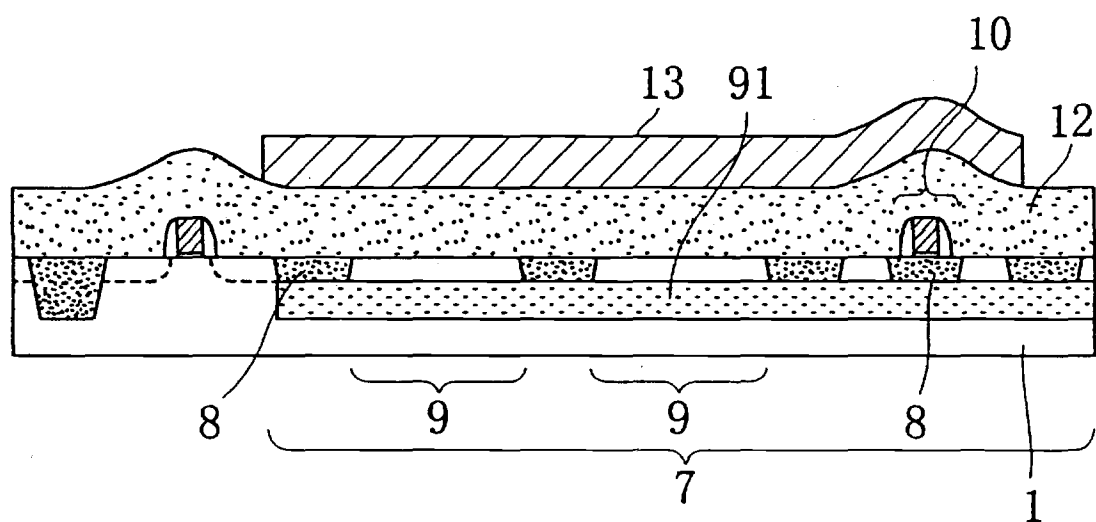
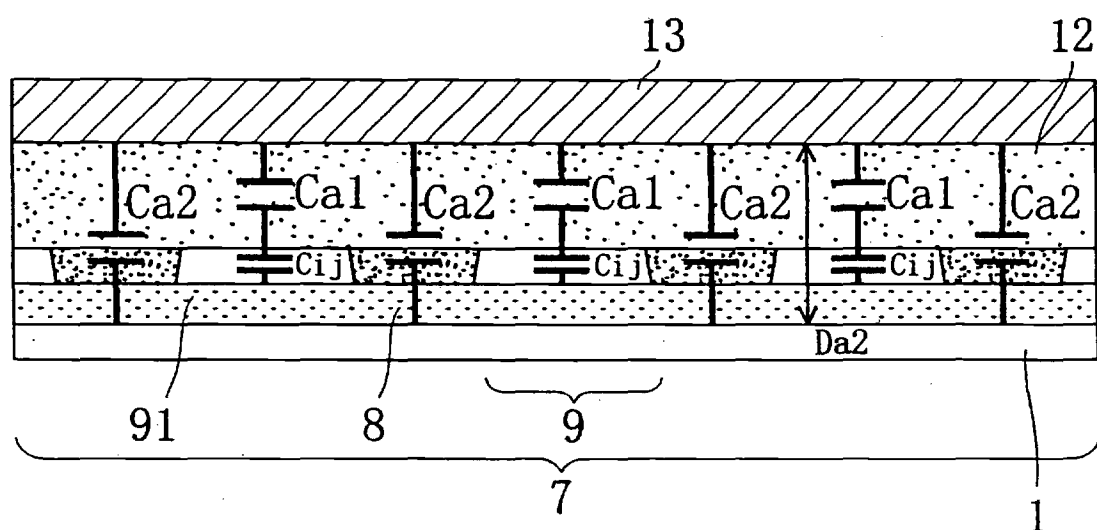
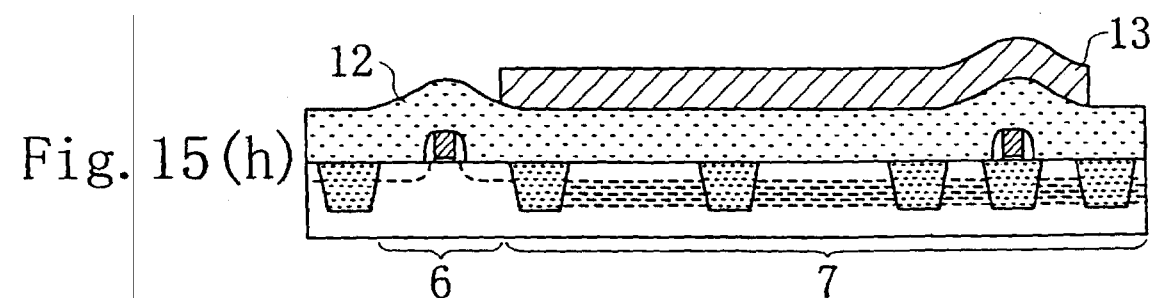
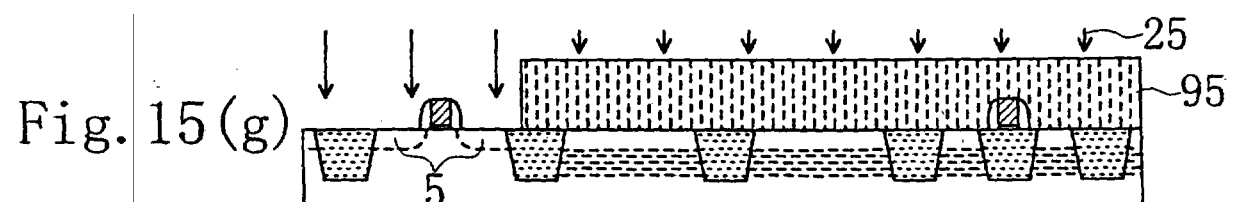
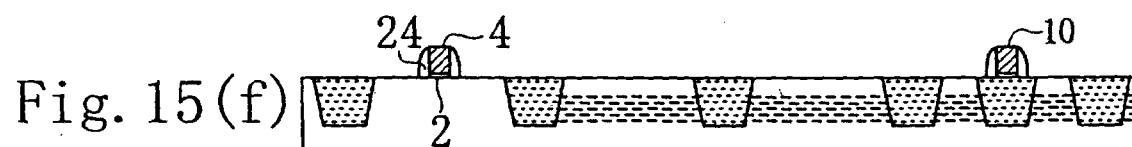
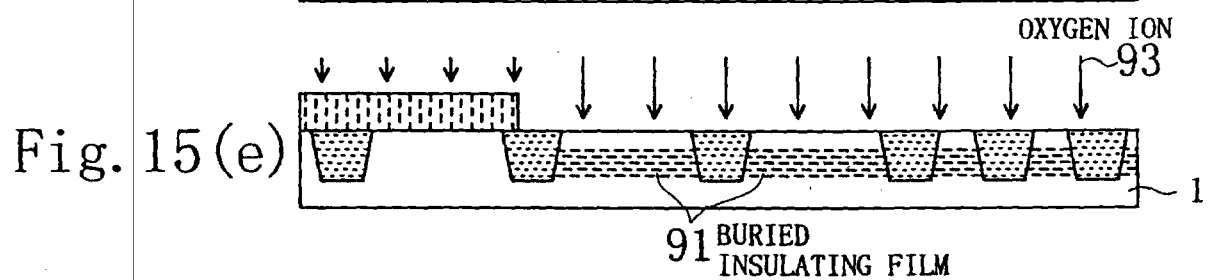
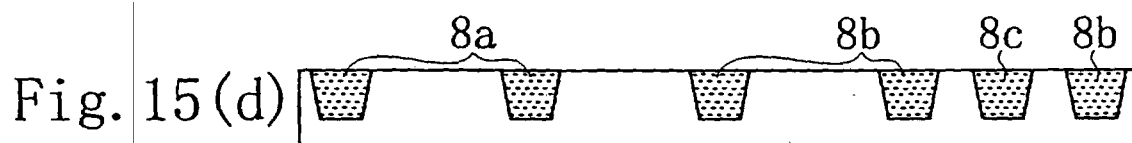
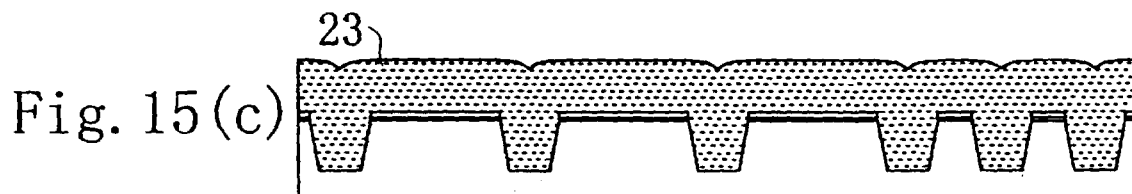
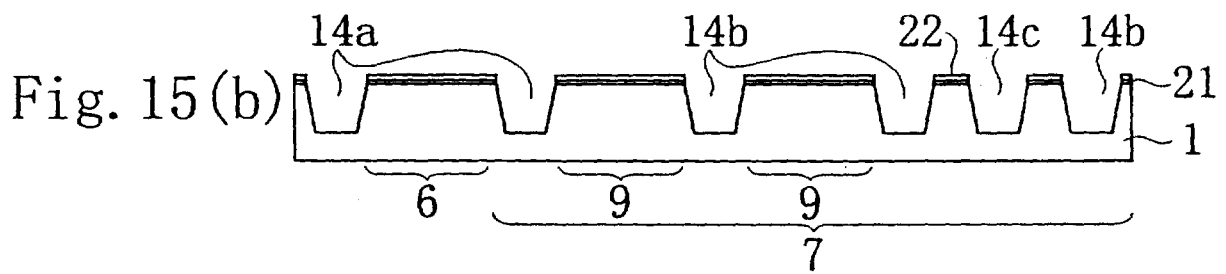
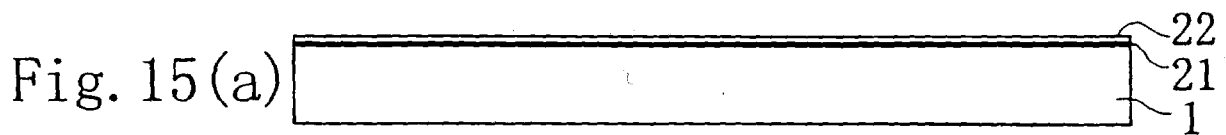
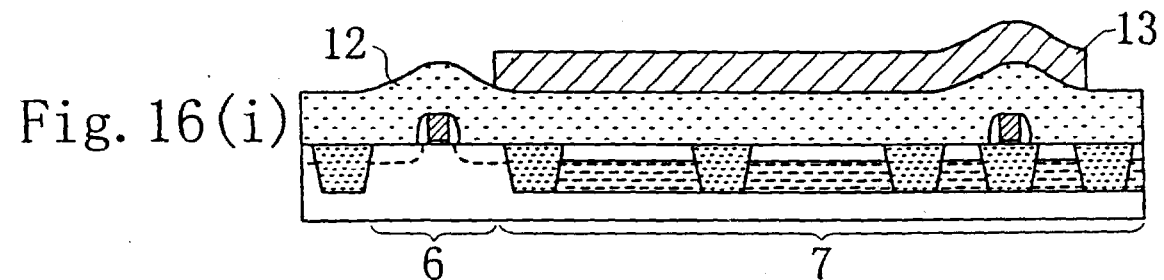
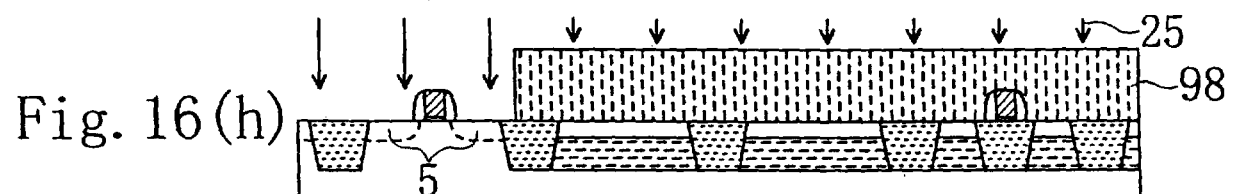
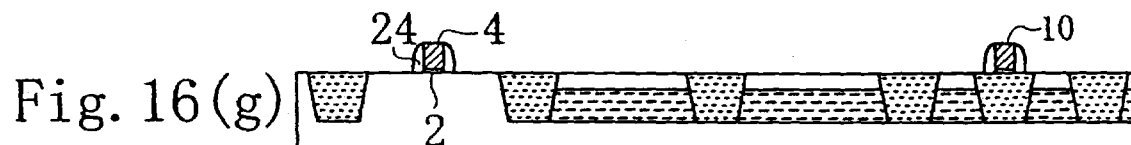
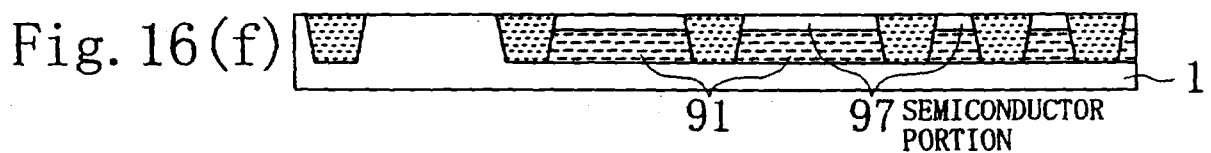
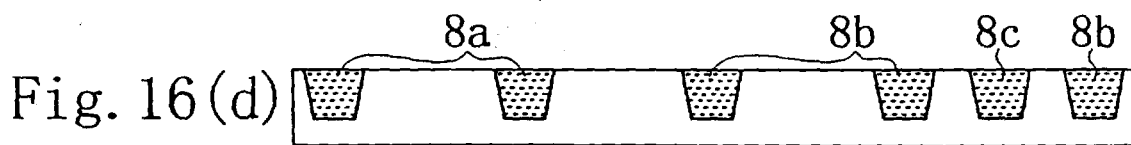
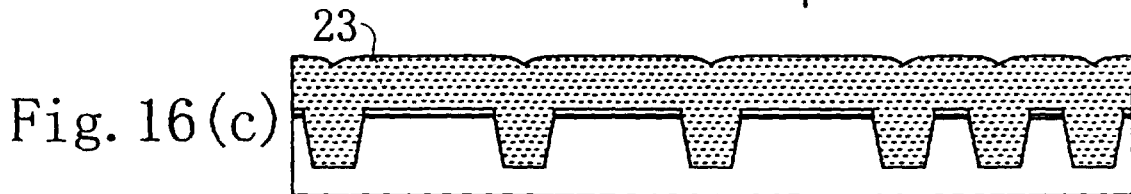
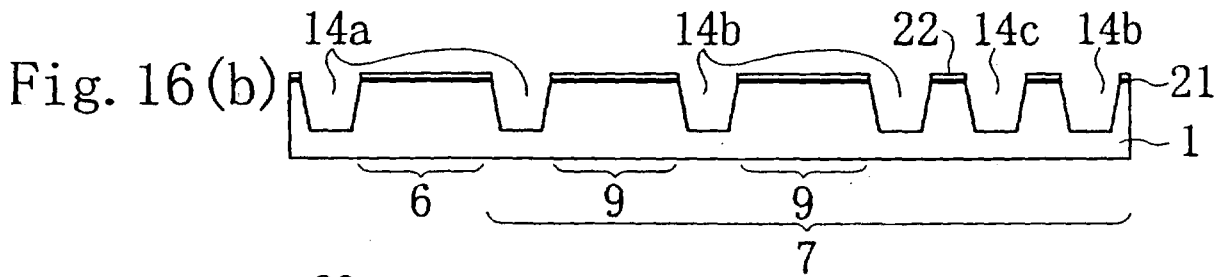
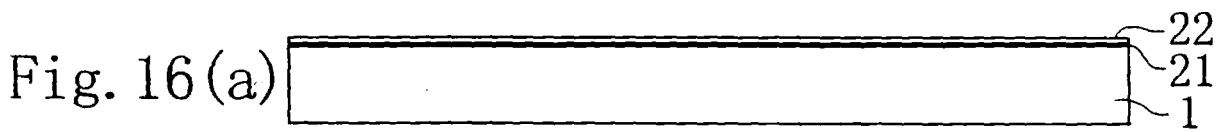
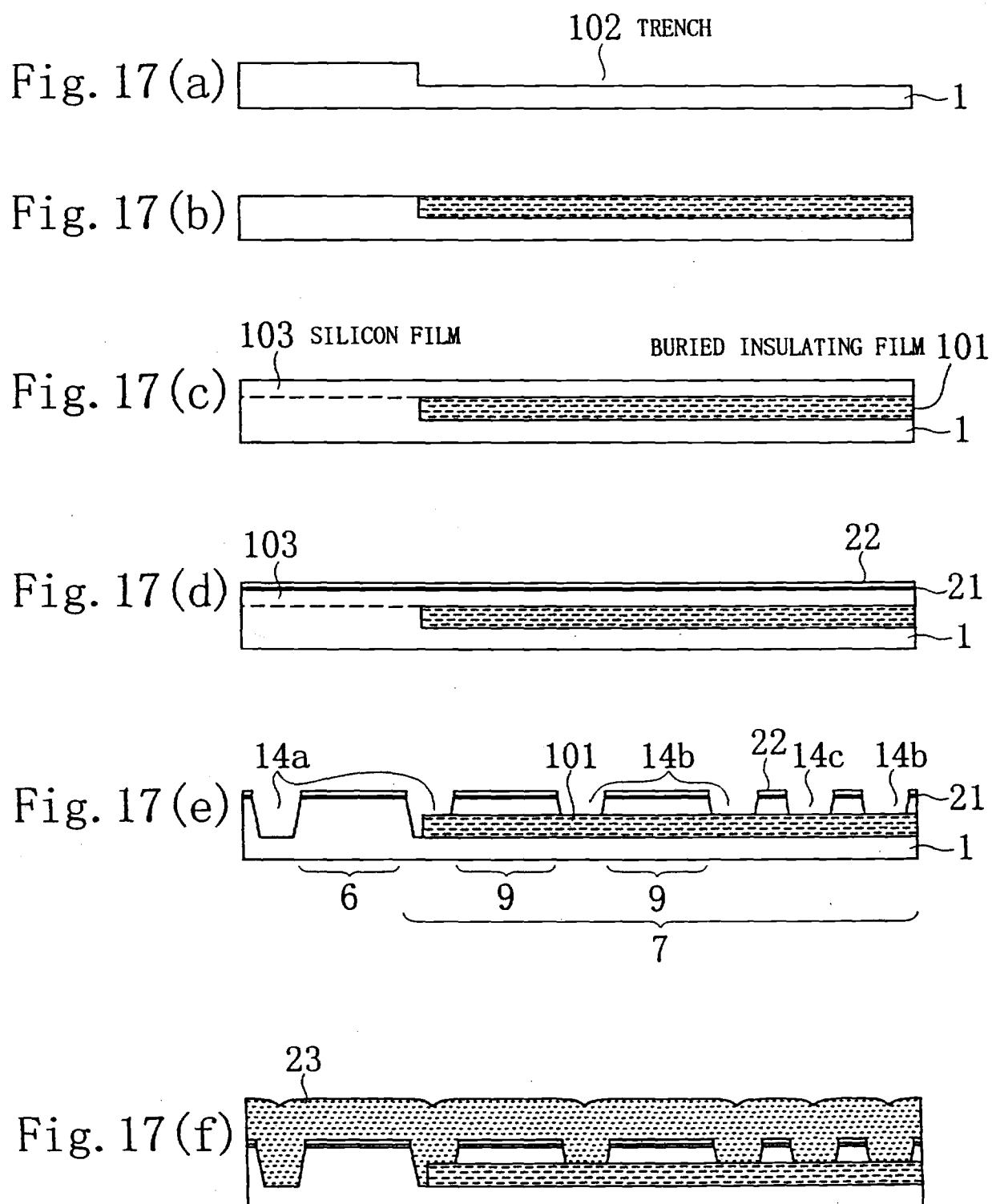


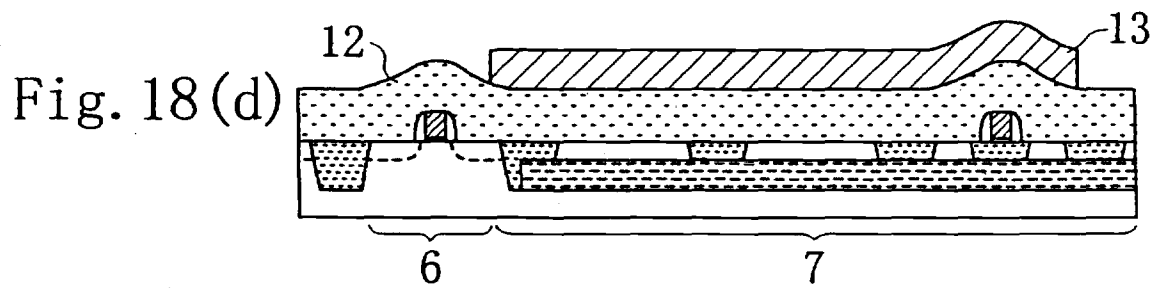
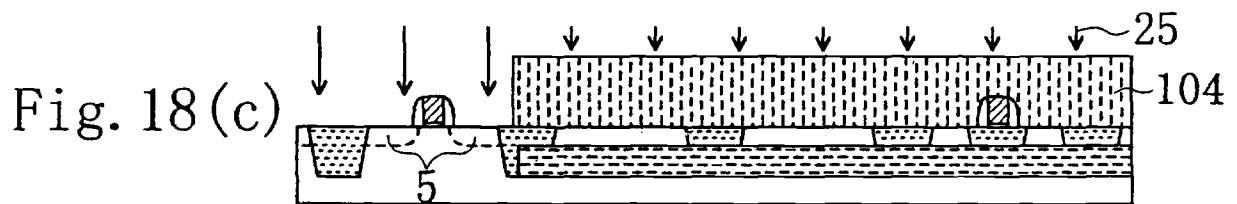
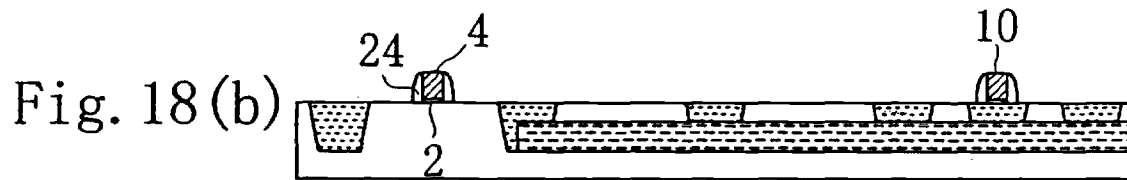
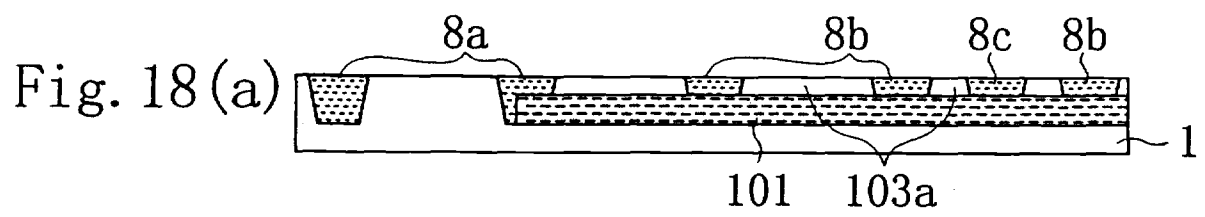
Fig. 14(b)



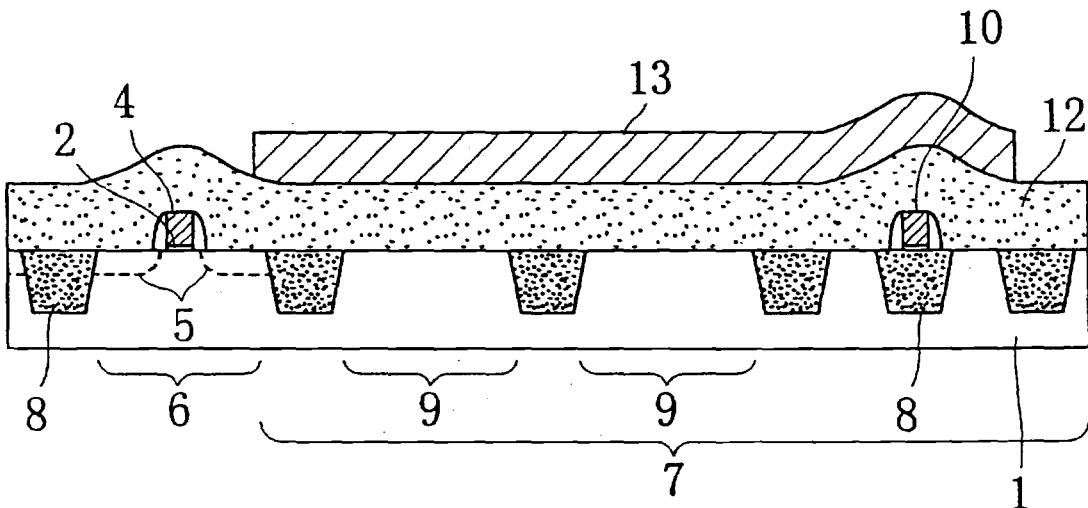








PRIOR ART



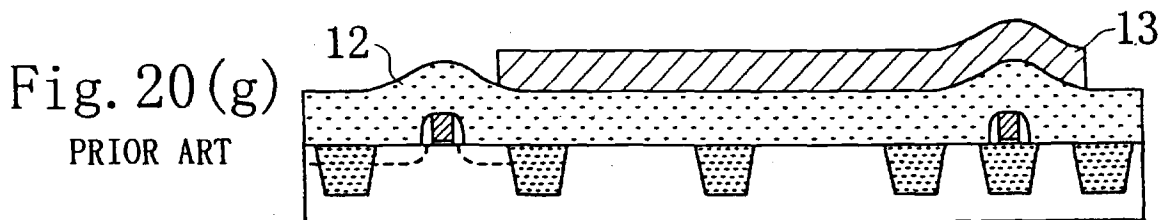
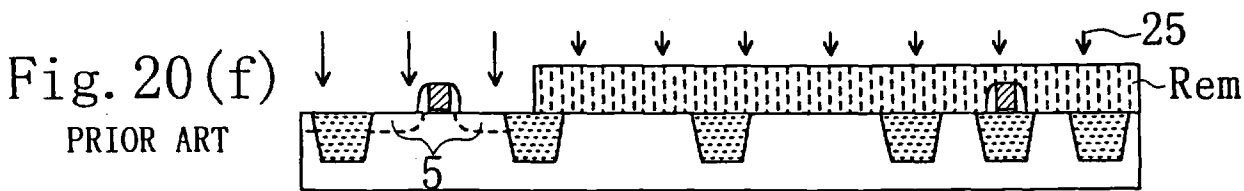
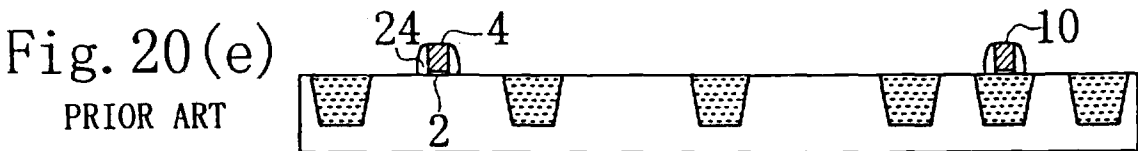
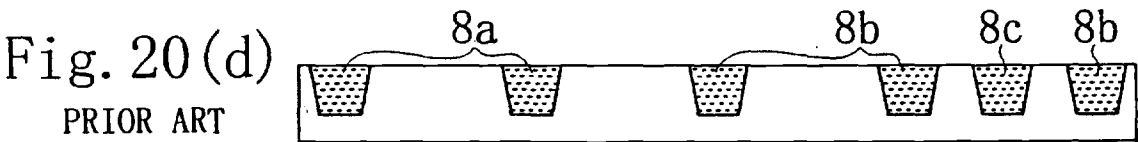
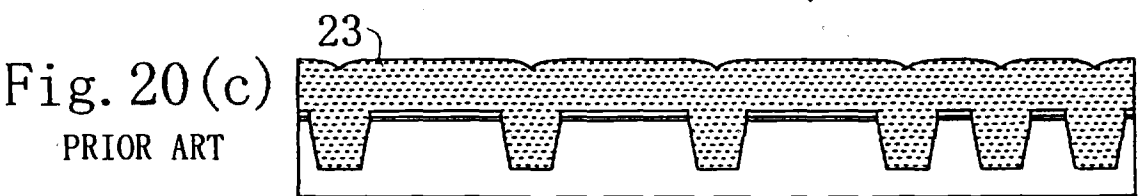
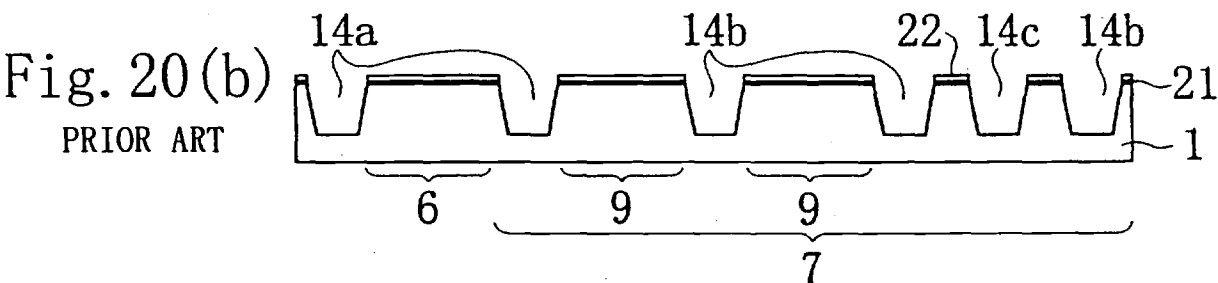
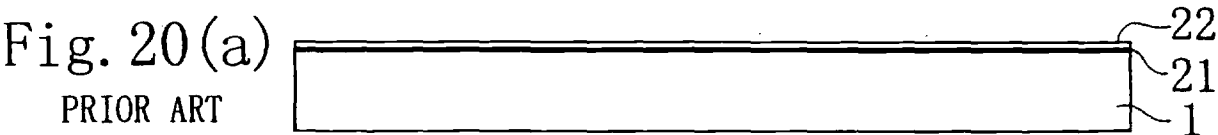


Fig. 21(a)

PRIOR ART

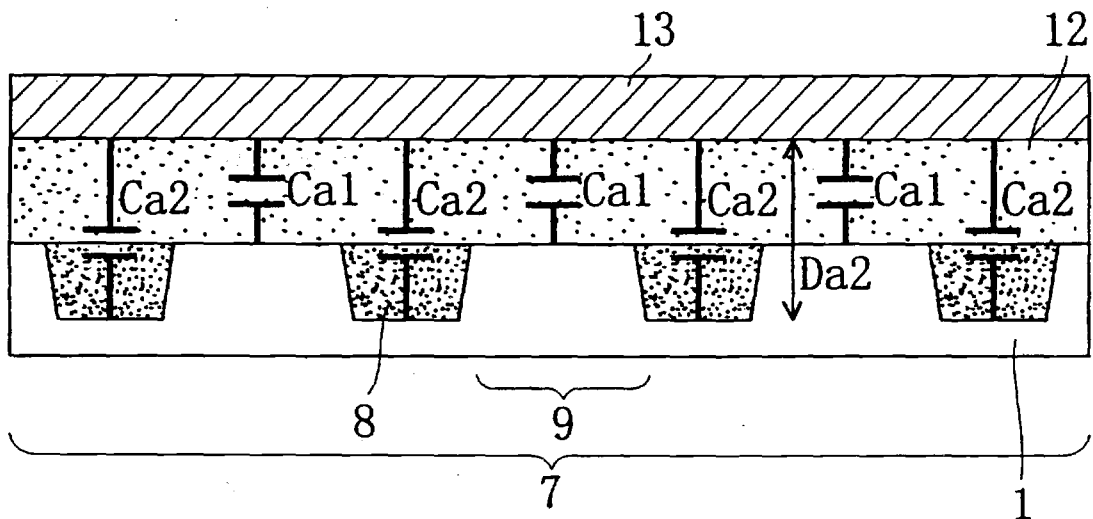
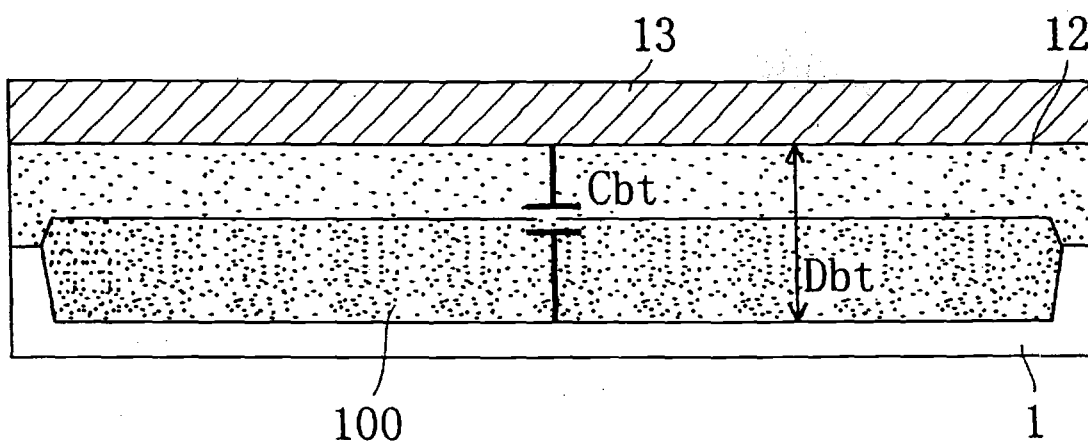


Fig. 21(b)

PRIOR ART



PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

01/11/2000 DBUTLER 00000003 130203 09469498

01 FC:101	760.00 CH
02 FC:102	78.00 CH

PTO-1556
(5/87)

*U.S. GPO: 1999-459-082/19144

PATENT APPLICATION FEE DETERMINATION RECORD

Effective November 10, 1998

Application or Docket Number

429498

CLAIMS AS FILED - PART I

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	18 minus 20= *	
INDEPENDENT CLAIMS	4 minus 3= *	
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	* 18	Minus	** 20	=
	Independent	* 4	Minus	*** 4	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	* 20	Minus	** 20	= 0
	Independent	* 4	Minus	*** 4	= 0
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY
TYPE ☐

OR
OTHER THAN
SMALL ENTITY

RATE	FEE
	380.00
X\$ 9=	
X39=	
+130=	
TOTAL	

RATE	FEE
	760.00
X\$18=	
X78=	28
+260=	
TOTAL	288

SMALL ENTITY

OR
OTHER THAN
SMALL ENTITY

RATE	ADDI- TIONAL FEE
X\$ 9=	
X39=	
+130=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$18=	
X78=	
+260=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$ 9=	
X39=	
+130=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$18=	
X78=	
+260=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$ 9=	
X39=	
+130=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$18=	
X78=	
+260=	
TOTAL ADDIT. FEE	

ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	B.B.	10500	1-10-00
O.I.P.E. CLASSIFIER		59	12/00
FORMALITY REVIEW			
RESPONSE FORMALITY REVIEW		10500	2-2

INDEX OF CLAIMS

Feb 21
071

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Rejected
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Allowed
- (Through numeral)...

Canceled
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Restricted
- N

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Non-elected
- I

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Interference
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Appeal
- O

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Objected

Claim		Date			
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If more than 150 claims or 10 actions
staple additional sheet here

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SEARCHED			
Class	Sub.	Date	Exmr.
257	504	Feb 02 01'	CJ
↓	506	↓	↓
	545		
	598		
↓		Feb 15 01'	CJ

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	Date	Exmr.
USPAT	Feb	CJ
↓	02-01'	↓
	Feb 15 01'	
USPAT		CJ

INTERFERENCE SEARCHED			
Class	Sub.	Date	Exmr.
257	509 545	10/4/01	~

(RIGHT OUTSIDE)

Patent Proof Copy Pilot Project



UNITED STATES
PATENT AND
TRADEMARK OFFICE

An Agency of the United States
Department of Commerce

Return Fax Sheet

Fax No. 215-682-8284

Application No. **09/469,498**

Corrections to Copy—Please check corrections required.

- ☐ Incorrect, duplicated, omitted words
- ☐ Incorrect, omitted punctuation
- ☐ Incorrect, omitted spacing
- ☐ Other: _____
- ☐ Check here if there were no errors on the proof copy
- ☐ Apply unentered/entered but missing/to be filed papers

	<u>Date</u>		<u>Date</u>
<input type="checkbox"/> CPA	_____	<input type="checkbox"/> Claim for Priority	_____
<input type="checkbox"/> RCE	_____	<input type="checkbox"/> Claim/Spec. Amendments	_____
<input type="checkbox"/> IDS	_____	<input type="checkbox"/> _____	_____
<input type="checkbox"/> Declaration	_____	<input type="checkbox"/> _____	_____
<input type="checkbox"/> Change of Attorney	_____	<input type="checkbox"/> _____	_____
<input type="checkbox"/> Small Entity Statement	_____	<input type="checkbox"/> Other: _____	_____
<input type="checkbox"/> Change of Address	_____	<input type="checkbox"/> _____	_____

POINT OF CONTACT FOR THIS APPLICATION: LORNA MULLENEX-CUSTOMER NO. 20277-FAX NO. 202-756-9087

Reviewer: _____

Comments:

CODE SHEET FOR CONTINUING DATA

LINE	CODE	SERIAL NO.	FILING DATE	STATUS	DOCUMENT NO.	ISSUE DATE
104	74	08/978,137	11/25/97	01	6,130,139	
105						
106						
107						
108						
109						
110						
111						
112						
113						
114						
115						
116						
117						

CONDITION AND STATUS CODES FOR CONTINUING DATA

CONDITION CODE

- 71 Continuation of application No.
- 81 which is a continuation of application No.
- 91 and a continuation of application No.

- 72 Continuation-in-part of application No.
- 82 which is a continuation-in-part of application No.
- 75 and a continuation-in-part of application No.

- 74 Division of application No.
- 84 which is a division of application No.
- 76 and a division of application No.

- 86 , said application No.
- 89 Application No.
- 90 and application No.
- 92 each

- 65 filed as application No.
- 66 Substitute for application No.
- 68 Provisional application No.

STATUS CODE

- 01 Patent No.
- 03 abandoned
- 04 SIR No.

NOTE I: When the codes 86 and 92 are used, they must be followed by 81, 82 or 84 – conditions beginning with “which is”

NOTE II: Codes 71, 72 and 74 may be used only on the first line; one of them must be used on the first line in regular continuing data, 66 or 68 may be used on the first line in Substitute or Provisional cases. Remember, however, that if there is Provisional and other continuing data, the Provisional is always listed last.