



SOLID-STATE CIRCUITS

APRIL 1982

VOLUME SC-17

NUMBER 2

(ISSN 0018-9200)

A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS COUNCIL

JOINT SPECIAL ISSUE ON VERY LARGE SCALE INTEGRATION
(Also published in IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-29, Number 4, April 1982)

H. Friedrich, W. F. Kosonocky, and
T. Yokuyama

FOREWORD 103

PAPERS

VLSI Device Processing and Patterning

- | | | |
|---|--|-----|
| <i>L. Jastrzebski</i> | Origin and Control of Material Defects in Silicon VLSI Technologies: An Overview .. | 105 |
| <i>V. Q. Ho and T. Sugano</i> | Fabrication of Si MOSFET's Using Neutron-Irradiated Silicon as Semi-Insulating Substrate | 117 |
| <i>E. Krullmann and W. L. Engl</i> | Low-Pressure Silicon Epitaxy | 121 |
| <i>T. Ito, T. Nakamura, and H. Ishikawa</i> | Advantages of Thermal Nitride and Nitroxide Gate Films in VLSI Process | 128 |
| <i>M. Hirayama, H. Miyoshi,</i> | High-Pressure Oxidation for Thin Gate Insulator Process | 133 |
| <i>N. Tsubouchi, and H. Abe</i> | | |
| <i>F. Neppel and U. Schwabe</i> | | |
| <i>Y. Homma, A. Yajima, and S. Harada</i> | Properties of Evaporated and Sputtered TaSi ₂ Films and the Influence of the Residual Gas Composition | 138 |
| <i>K. Harada, O. Kogure, and K. Murase</i> | Feature Size Limit of Liftoff Metalization Technology | 142 |
| | Poly (Phenyl Methacrylate-Co-Methacrylic Acid) as a Dry-Etching Durable Positive Electron Resist | 148 |
| <i>T. D. Berker and D. D. Casey</i> | Characterization of AZ-2415 as a Negative Electron Resist | 154 |

VLSI Technologies

- | | | |
|---|--|-----|
| <i>T. Shibata, K. Hieda, M. Sato,</i> | An Optimally Designed Process for Submicrometer MOSFET's | 161 |
| <i>M. Konaka, R. L. M. Dang, and</i> | | |
| <i>H. Iizuka</i> | | |
| <i>K. Y. Chiu, J. L. Moll, and J. Manoliu</i> | A Bird's Beak Free Local Oxidation Technology Feasible for VLSI Circuits Fabrication | 166 |
| | Direct Moat Isolation for VLSI | 171 |
| <i>K. L. Wang, S. A. Saller,</i> | | |
| <i>W. R. Hunter, P. K. Chatterjee, and</i> | | |
| <i>P. Yang</i> | | |
| <i>K. L. Wang, T. C. Holloway,</i> | Composite TiSi ₂ /n ⁺ Poly-Si Low-Resistivity Gate Electrode and Interconnect for VLSI Device Technology | 177 |
| <i>R. F. Pinizzotto, Z. P. Sobczak,</i> | | |
| <i>W. R. Hunter, and A. F. Tasch, Jr.</i> | | |
| <i>J. C.-H. Hui, T.-Y. Chiu,</i> | Sealed-Interface Local Oxidation Technology | 184 |
| <i>S.-W. S. Wong, and W. G. Oldham</i> | | |
| <i>N. Matsukawa, H. Nozawa,</i> | Selective Polysilicon Oxidation Technology for VLSI Isolation | 191 |
| <i>J. Matsunaga, and S. Kohyama</i> | | |

VLSI Device Structures and Characteristics

- | | | |
|---|---|-----|
| <i>Y. El-Mansy</i> | MOS Device and Technology Constraints in VLSI | 197 |
| <i>Y. Okuto, M. Fukuma, and Y. Ohno</i> | SOS/CMOS as a High-Performance LSI Device | 204 |
| <i>M. H. White</i> | Characterization of CMOS Devices for VLSI | 208 |
| <i>J.-P. Colinge, E. Demoulin, and</i> | Stacked Transistors CMOS (ST-CMOS), an NMOS Technology Modified to CMOS | 215 |
| <i>M. Lobet</i> | | |
| <i>P. J. Tsang, S. Ogura, W. W. Walker, J. F.</i> | Fabrication of High-Performance LDDFET's with Oxide Sidewall-Spacer Technology | 220 |
| <i>Shepard, and D. L. Critchlow</i> | | |
| <i>T. Nakamura, T. Miyazaki,</i> | Self-Aligned Transistor with Sidewall Base Electrode | 226 |
| <i>S. Takahashi, T. Kure, T. Okabe, and</i> | | |
| <i>M. Nagata</i> | | |
| <i>L. Risch, C. Werner, W. Müller, and A. W.</i> | Deep-Implant 1- μ m MOSFET Structure with Improved Threshold Control for VLSI Circuitry | 231 |
| <i>Wieder</i> | | |
| <i>H. Sunami, K. Shimohigashi, and</i> | Characteristics of a Buried-Channel Graded Drain with Punchthrough Stopper(BGP) MOS Device | 237 |
| <i>N. Hashimoto</i> | | |
| <i>E. Takeda, H. Kume, T. Toyabe, and S. Asai</i> | Submicrometer MOSFET Structure for Minimizing Hot-Carrier Generation | 241 |

<i>VLSI Device/Circuit Modeling</i>	
A. C. Ipri, L. B. Medwin, N. Goldsmith, and F. W. Brehm H. Iwai, K. Taniguchi, M. Konaka, S. Maeda, and Y. Nishi A. Husain and S. G. Chamberlain	
H.-T. Yuan, Y.-T. Lin, and S.-Y. Chiang K. C. Saraswat and F. Mohammadi D. B. Scott, W. R. Hunter, and H. Shichijo B.-S. Song and P. R. Gray Y. Ikawa, W. R. Eisenstadt, and R. W. Dutton J. Lohstroh and R. M. Pluta N. C.-C. Lu, L. Gerzberg, and J. D. Meindl	
Two-Dimensional Dynamic Analysis of Short-Channel Thin-Film MOS Transistors Using a Minicomputer	248
Two-Dimensional Nature of Diffused Layers and Certain Limitations in Scaling-Down Coplanar Structure	255
Three-Dimensional Simulation of VLSI MOSFET's: The Three-Dimensional Simulation Program WATMOS	261
Properties of Interconnection on Silicon, Sapphire, and Semi-Insulating Gallium Arsenide Substrates	269
Effect of Scaling of Interconnections on the Time Delay of VLSI Circuits	275
A Transmission Line Model for Silicided Diffusions: Impact on the Performance of VLSI Circuits	281
Threshold-Voltage Temperature Drift in Ion-Implanted MOS Transistors	291
Modeling of High-Speed, Large-Signal Transistor Switching Transients from <i>s</i> -Parameter Measurements	299
First-Order Modeling of Oxide-Isolated ISL	305
Scaling Limitations of Monolithic Polycrystalline-Silicon Resistors in VLSI Static RAM's and Logic	312
<i>VLSI Circuits</i>	
C. D. Hartgring, B. A. Rosario, and J. M. Pickett Y. Inabe, T. Hayashi, K. Kawarada, H. Miwa, and K. Ogiue P. K. Chatterjee, A. H. Shah, Y.-T. Lin, W. R. Hunter, E. A. Walker, C. C. Rhodes, and W. C. Bruncke J. E. Leiss, P. K. Chatterjee, and T. C. Holloway K. Shimohigashi, H. Masuda, Y. Kamigaki, K. Itoh, N. Hashimoto, and E. Arai D. W. Greve G. A. Sai-Halas, M. R. Wordeman, and R. H. Dennard T. Toyabe, T. Shinoda, M. Aoki, H. Kawamoto, K. Mitsusada, T. Masuhara, and S. Asai R. J. Bayruns, P. I. Suciu, N. C. Wittwer, D. L. Fraser, Jr., E. N. Fuls, R. A. Kushner, F. R. Ashley, and E. A. Gere M. Aoki, H. Ando, S. Ohba, I. Takemoto, S. Nagahara, T. Nakano, M. Kubo, and T. Fujita	
High-Speed Low-Power Silicon MESFET 1 × 1K Bit Static Shift Register	321
A 16K-Bit Static IIL RAM with 25-ns Access Time	325
Enhanced-Performance 4K × 1 High-Speed SRAM Using Optically Defined Submi- crometer Devices in Selected Circuits	330
dRAM Design Using the Taper-Isolated Dynamic RAM Cell	337
An n-Well CMOS Dynamic RAM	344
Programming Mechanism of Polysilicon Resistor Fuses	349
Alpha-Particle-Induced Soft Error Rate in VLSI Circuits	355
A Soft Error Rate Model for MOS Dynamic RAM's	362
A Fine-Line nMOS IC for Raster-Scan Control of a 500-MHz Electron-Beam Deflection System	367
2/3-Inch Format MOS Single-Chip Color Imager	375
<i>VLSI Circuit/System Design</i>	
A. Masaki and T. Chiba J. Khakbaz and E. J. McCluskey K. F. Smith, T. M. Carter, and C. E. Hunt	
Design Aspects of VLSI for Computer Logic	381
Concurrent Error Detection and Testing for Large PLA's	386
Structured Logic Design of Integrated Circuits Using the Storage/Logic Array (SLA)	395
BRIEFS	
L. A. Akers and C. S. Chao M. I. Elmasry M. I. Elmasry	
A Closed-Form Threshold Voltage Expression for a Small-Geometry MOSFET	406
Multidrain NMOS for VLSI Logic Design	409
Nanosecond NMOS VLSI Current Mode Logic	411
CONTRIBUTORS	
	415



IEEE JOURNAL OF SOLID-STATE CIRCUITS

IEEE JOURNAL OF SOLID-STATE CIRCUITS is published by the IEEE Solid-State Circuits Council on behalf of the following Groups/Societies, S-Circuits and Systems, S-Communications, S-Computer, S-Electron Devices, S-Microwave Theory and Techniques, S-Components, Hybrids, and Manufacturing Technology, G-Sonics and Ultrasonics, and S-Quantum Electronics and Applications. For information on receiving this JOURNAL, write to the IEEE Service Center at the address below.

SOLID-STATE CIRCUITS COUNCIL

President

R. G. MEYER
E.E.C.S.—Cory Hall
Univ. California
Berkeley, CA 94720

Vice President (open)

Treasurer

C. W. GWYN
Sandia Lab., Org. 2110
Albuquerque, NM 87185

Secretary

F. K. BUELOW
STC Microtechnology
224 N. Wolfe Rd.
Sunnyvale, CA 94086

Representatives

S-CAS

B. A. WOOLEY
Bell Lab.
Holmdel, NJ 07733

S-COM

S. L. FREENY
Signal Processing Res. Dep.
Bell Lab., Rm. 4D-637
Holmdel, NJ 07733

G-SU

L. T. CLAIBORNE
Texas Instruments, Inc.
13500 N. Central Exp.
P.O. Box 5936
Dallas, TX 75222

S-C

D. W. CROCKETT
Hewlett-Packard
1504 Page Mill Rd.
Palo Alto, CA 94304

S-ED

W. G. OLDHAM
Univ. California
Berkeley, CA 94720

D. O. PEDERSON
E.E.C.S.—Cory Hall
Univ. California
Berkeley, CA 94720

F. IVANEK
Farinon Electric
1691 Bayport Ave
San Carlos, CA 94070

T. R. MEEKER
Bell Lab.
555 Union Blvd.
Allentown, PA 18103

S. TRIEBWASSER
IBM T. J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

B. L. GREGORY
Sandia Lab., Org. 2140
Albuquerque, NM 87115

S-MTT

S. F. ADAM
Hewlett-Packard
Microwave Semiconductor Div.
350 W. Trimble Rd.
San Jose, CA 95131

B. E. BERSON
Consulting In Tech
1011 Suffolk Way
Los Altos, CA 94022

V. G. GELNOVATCH
U.S. Army Electron. Command
Attn: DRSEL-TL-IM
Fort Monmouth, NJ 07703

S-CHMT

JOHN E. KNOYAN
Texas A & M Univ.
Elec. Eng. Dep.
College Station, TX 77843

S-QEA

R. C. EDEN
Science Center
Rockwell Int.
P.O. Box 1085
Thousand Oaks,
CA 91360

EXEC. COMM.,
ISSCC CHAIRMAN
J. A. A. RAPER
Electron. Lab
General Electric Co.
Electronics Park
Box 1122
Syracuse, NY 13201

IEEE JOURNAL OF SOLID-STATE CIRCUITS

Editor

G. L. BALDWIN
Hewlett-Packard Lab
1501 Page Mill Road
Bldg. 1-U
Palo Alto, CA 94304

H. J. BOLL
Bell Lab.
Murray Hill, NJ 07974

R. HEWES
Central Research Lab
Texas Instruments, Inc.
Dallas, TX 75222

R. G. MEYER
E.E.C.S.—Cory Hall
Univ. California
Berkeley, CA 94720

Associate Editors

O. W. MEMELINK
Technische Hogeschool Twente
Enschede Drienerio
Postbus 217
The Netherlands

R. MULLER
Siemens AG, Dep. BAT
Balanstr. 73
D-8000 Munich 80
West Germany

B. L. GREGORY
Dep. 2140
Sandia Lab.
Albuquerque, NM 87115

M. NAGATA
Central Research Lab.
Hitachi Ltd.
Tokyo, Japan

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

Officers

ROBERT E. LARSON, *President*
JAMES B. OWENS, *President-Elect*
THELMA A. ESTRIN, *Executive Vice President*
DICK C. J. POORTVLIET, *Secretary*
CHARLES A. ELTON, *Treasurer*

HANS C. CHERNEY, *Vice President, Regional Activities*
JOSE B. CRUZ, JR., *Vice President, Technical Activities*
EDWARD J. DOYLE, *Vice President, Professional Activities*
EDWARD W. ERNST, *Vice President, Educational Activities*
G. P. RODRIGUE, *Vice President, Publication Activities*

STEPHEN KAHNE, *Division I Director*

Headquarters Staff

ERIC HERZ, *Executive Director and General Manager*
ELWOOD K. GANNETT, *Deputy General Manager*

THOMAS W. BARTLETT, *Controller*
DONALD CHRISTIANSEN, *Editor of Spectrum*
IRVING ENGELSON, *Staff Director, Technical Activities*
LEO FANNING, *Staff Director, Professional Activities*
ELWOOD K. GANNETT, *Acting Staff Director, Publishing Services*

SAVA SHERR, *Staff Director, Standards*
CHARLES F. STEWART, JR., *Staff Director, Administration Services*
DONALD L. SUPPERS, *Staff Director, Field Services*
JOHN F. WILHELM, *Staff Director, Educational Services*

Publications Department

H. JAMES CARTER, *Associate Staff Director*

Production Managers: ANN H. BURGMAYER, CAROLYNE ELENOWITZ*, GAIL S. FERENC, ISABEL NAREA
Associate Editors: MONA GHOSH, MARY E. GRANGEIA, THOMAS R. GRECO, JEFFREY B. MARTIN,
EVELYN C. NORMAN, NELA RYBOWICZ, BARBARA A. SOMOGYI

*Responsible for this Journal

IEEE JOURNAL OF SOLID-STATE CIRCUITS is published bimonthly by The Institute of Electrical and Electronics Engineers, Inc. **Headquarters:** 345 East 47th Street, New York, NY 10017. Responsibility for the contents rests upon the authors and not upon the IEEE, the Group/Society, or its members. **IEEE Service Center** (for orders, subscriptions, address changes, Region/Section/Student Services) 445 Hoes Lane, Piscataway, NJ 08854. **Telephones:** Headquarters 212-705 + extension: Information -7900, General Manager -7910, Controller -7748, Educational Services -7860, Publishing Services -7560, Standards -7960, Technical Services -7890, IEEE Service Center 201-981-0060, Professional Services: Washington Office 202-785-0017. **NY Telecopier:** 212-752-4929. **Telex:** 236-411 (International messages only). Individual copies: IEEE members \$6.00 (first copy only), nonmembers \$12.00 per copy. Annual subscription price: IEEE members, dues plus Group/Society fee. Price for nonmembers on request. Available in microfiche and microfilm. **Copyright and Reprint Permissions:** Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limits of U.S. Copyright law for private use of patrons. (1) those post-1977 articles that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 21 Congress St., Salem, MA 01970; (2) pre-1978 articles without fee. Instructors are permitted to photocopy isolated articles for noncommercial classroom use without fee. For other copying, reprint, or republication permission, write to Director, Publishing Services at IEEE Headquarters. All rights reserved. Copyright © 1982 by the Institute of Electrical and Electronics Engineers, Inc. Printed in U.S.A. Second-class postage paid at New York, NY and at additional mailing offices. **Postmaster:** Send address changes to IEEE, 445 Hoes Lane, Piscataway, NJ 08854.

Effect of Scaling of Interconnections on the Time Delay of VLSI Circuits

KRISHNA C. SARASWAT, MEMBER, IEEE, AND FARROKH MOHAMMADI, MEMBER, IEEE

Abstract—Effect of scaling of dimensions, i.e., increase in chip size and decrease in minimum feature size, on the RC time delay associated with interconnections in VLSI's has been investigated. Analytical expressions have been developed to relate this time delay to various elements of technology, i.e., interconnection material, minimum feature size, chip area, length of the interconnect, etc. Empirical expressions to predict the trends of the technological elements as a function of chronological time have been developed. Calculations of time delay for interconnections made of poly-Si, WSi_2 , W, and Al have been done and they indicate that as the chip area is increased and other device-related dimensions are decreased the interconnection time delay becomes significant compared to the device time delay and in extreme cases dominates the chip performance.

I. INTRODUCTION

WITH THE ADVANCES in technology, the integrated-circuit (IC) chip size, complexity, and device packing density is continuously increasing. New developments in lithographic and etching techniques have resulted in reduction in the minimum feature size used in the IC's. At the same time, improvements in materials technology have allowed integration of more and more devices on the same chip, resulting in increased area. According to theory of scaling [1], the smaller dimensions of an MOS transistor should enhance its speed. As a first-order approximation, therefore, this should proportionally increase the circuit speed. Indeed, for smaller circuits it does happen. However, for larger circuits, the time delays associated with the interconnections can play a significant role in determining the performance of the circuit. As the minimum feature size is made smaller, the area of cross section of the interconnection also reduces. At the same time, a higher integration level allows the chip area to increase, causing the length of the interconnections to increase. The net effect of this "scaling of interconnections" is reflected into an appreciable RC time delay. For a very large chip with extremely small geometries, the time delay associated with interconnections could become an appreciable portion of the total time delay, and hence the circuit performance could no longer be decided by the device performance.

The time delay associated with the interconnections is dependent upon two factors; the resistance of the interconnections,

and the capacitance controlled by the dielectric media. Generally, silicon dioxide is used as the dielectric. The success of silicon in microelectronics can be largely attributed to excellent properties of Si/SiO₂ interface and ease of thermal oxidation of silicon to produce a passivating layer of SiO₂. Therefore, as far as the dielectric material is concerned, our choice is somewhat limited to SiO₂. Fortunately for interconnections, a variety of materials have been used which can be broadly classified into three categories; metals, polycrystalline silicon (polysilicon), and metal silicides. A big variation of resistivity is available in this case, e.g., the resistivities of heavily doped polysilicon and aluminum are 5×10^{-4} and $2.25 \times 10^{-6} \Omega \cdot \text{cm}$, respectively. Obviously, the proper choice of the material within the constraints placed by the fabrication technology can result in minimization of the RC delay time. The materials which have been used or proposed to form interconnections can be broadly classified into four categories, heavily doped polysilicon, low-temperature metals, high-temperature refractory metals, and metal silicides. Here, we will consider N⁺ polysilicon, Al, W, and WSi_2 as the representatives of each group.

In this work, the effect of increase in chip area and decrease in the minimum feature size on the performance of the circuit has been investigated. A theory of *scaling of interconnections* has been developed. From the information available in the literature, empirical equations have been developed to predict the various elements of the technology, i.e., minimum feature size, maximum chip area, maximum interconnection length, etc., at a given point in time. Time delays associated with interconnections made of different materials have been calculated. Utilizing the theory of scaling of interconnections and scaling of MOS transistors [1] the time delay associated with interconnections and devices have been compared.

II. MODELING OF DISTRIBUTED RC TIME DELAY

The time delay associated with the interconnection is dependent upon two parameters; the resistance and the capacitance associated with the interconnections. Fig. 1 shows a schematic diagram of closely packed interconnections in an IC. The resistance of an interconnection line of length L , width W , thickness H , and resistivity ρ is given by

$$R = \rho \frac{L}{WH}. \quad (1)$$

Assuming a parallel-plate capacitance model, the capacitance between the interconnection and the silicon substrate is given by

Manuscript received July 31, 1981; revised December 15, 1981. This work was supported by the Defense Advanced Research Projects Agency under Contract MDA 903-79-C-0680 and was performed at Stanford University, Stanford, CA.

K. C. Saraswat is with the Integrated Circuits Laboratory, Stanford University, Stanford, CA 94305.

F. Mohammadi is with National Semiconductors, Santa Clara, CA.

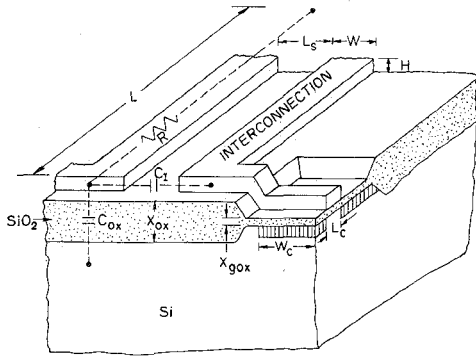


Fig. 1. Cross section of MOS transistors and parasitics associated with the interconnections.

$$C_{ox} = K_{ox} \epsilon_0 \frac{WL}{X_{ox}} \quad (2)$$

where X_{ox} and K_{ox} are the SiO_2 thickness and dielectric constant, respectively, and ϵ_0 is the permittivity of free space. The capacitance between the two adjacent interconnections separated by a distance of L_s is

$$C_I = K_{ox} \epsilon_0 \frac{HL}{L_s} \quad (3)$$

where it has been assumed that the dielectric between them is SiO_2 . The total line capacitance is given by

$$C = C_{ox} + C_I = K_{ox} \epsilon_0 L \left\{ \frac{W}{X_{ox}} + \frac{H}{L_s} \right\} \quad (4)$$

In the calculation of C_{ox} and C_I , a simple model of parallel-plate capacitance has been assumed and the effect of fringing field and finite electrode thickness [2], [3] has been ignored to maintain simplicity. By doing elaborate numerical analysis, it is possible to take these factors into account, however, the analytical nature of the calculations to follow will be lost. Dang and Shigyo have shown [2] that the above assumption is more erroneous only for small ratio of W to X_{ox} . For W/X_{ox} higher than 3, the error caused by this simple model is within a factor of two. In general, the line capacitance could be approximated by the relationship [2]

$$C = K_1 (C_{ox} + C_I) \quad (5)$$

where K_1 is the factor which takes into account the fringing fields and its value can be calculated using the two-dimensional analysis of Dang and Shigyo [2].

An interconnection should be treated as a distributed-parameter transmission line in order to calculate the accurate value of time delay. Fig. 2 shows a lumped value form of the RC distributed line which can be used to derive approximate pulse-response time [4], [5]. The transient response to a step input to the distributed RC network of Fig. 2 has been shown by Kaufman and Garrett [4] to be

$$V_o(t) = 1 - \frac{4}{n} \sum_{n=0}^{\infty} \frac{(-1)^n}{2n+1} \exp \left[- \left(\frac{2n+1}{2} \right)^2 \frac{t}{RC} \right] \quad (6)$$

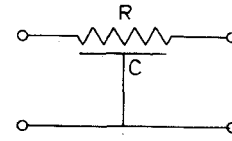


Fig. 2. Schematic of a distributed RC network representing an interconnection.

TABLE I
MOS DEVICE SCALING FOR A CONSTANT FIELD

Device/Circuit Parameter	Scaling Factor* (S)
Device dimensions L_c, W_c, X_{gox}	$1/S$
Doping concentration	S
Voltage	$1/S$
Field	1
Current	$1/S$
Gate Delay	$1/S$
Power dissipation/device	$1/S^2$
Power density	1
Speed power product/device	$1/S^3$

*Scaling factor $S > 1$.

The time it takes the output to reach from 10 to 90 percent of its final value, defined as rise time τ , is $0.89 RC$ according to (6). Compared to that, rise time of a corresponding one-lump RC circuit is $2.2 RC$. Similar analysis of distributed RC line has been done by Wilnai [5] with identical results. Therefore, in the analysis to follow, $\tau_L = 0.89 RC$ will be used as a figure of merit of the interconnection line. From (1) and (5) we obtain

$$\tau_L = 0.89 K_1 K_{ox} \epsilon_0 \rho \frac{L^2}{WH} \left(\frac{W}{X_{ox}} + \frac{H}{L_s} \right) \quad (7)$$

It is obvious that the figure of merit or rise time τ_L is heavily dependent upon various dimensions involved in a chip, i.e., L , W , H , X_{ox} , and L_s . Therefore, in order to obtain more information about τ_L , first we have to relate the above dimensions to various elements of the VLSI technology. In the next section, a theory of "scaling of interconnections" will be developed analogous to the theory of MOS device scaling [1], where various dimensions involved with devices and interconnections will be related to various elements of the technology and the time frame.

III. SCALING OF DEVICE AND INTERCONNECTION LINES

The area occupied by an MOS transistor can be made smaller by shortening its channel width and length leading to a faster device. Substrate doping plus the junction built-in potential determine the minimum depletion-region thickness of an operable device which, in turn, establishes the minimum device size. Based on the above observations, the linear transformation (device scaling) in Table I has been suggested [1]. According

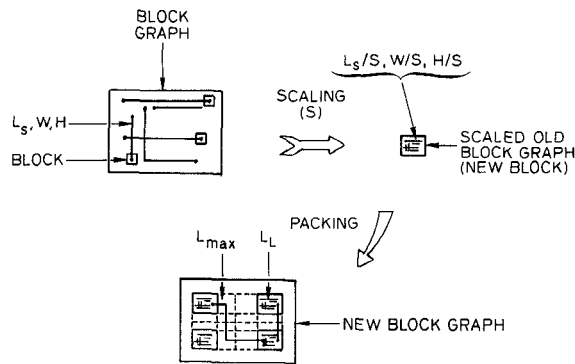


Fig. 3. Integration of scaled circuits.

to Table I, as the average feature size drops by a scaling factor of $1/S$, device performance is enhanced; as gate delay is reduced by a factor of $1/S$, and power dissipation/device by a factor of $1/S^2$, more devices can be packed on a chip.

Smaller dimensions, larger chip size, and circuit innovations all contribute to the progress of integration and the generation of a larger number of components on a single chip. Increasing these components raises the number of connections required for signal transmission. To clarify the problem of interconnections, the following terms are defined [6]:

A "block graph" is a structure consisting of interconnected blocks; a logic design is an example.

A "block" is an undefined primitive. In a logic design, for example, it can be a NOR circuit, a storage element, register, or an IC chip.

In the following discussion, only planar transistors with a silicon substrate and silicon-dioxide dielectric are considered, and the interconnections are assumed to be in a single plane isolated by a silicon-dioxide layer. It is assumed that a specific block graph can be scaled down and miniaturized so that it can be packed with the others on the same chip, thereby generating a super-block graph containing the old scaled-down block graphs as illustrated in Fig. 3. The interconnections within a block are defined as local interconnections and between blocks are termed as long-distance interconnections.

The concept of scaling the local interconnection lines can be understood by examining Figs. 1, 3, and Table II. It can be seen in Table II that, after scaling, the line response time remains constant and the line voltage drop stays the same; however, current density increases which can introduce severe device-performance problems, such as electromigration. A comparison between Tables I and II reveals that the total delay time of a scaled block graph is a function of gate delay only because the scaling rule dictates the gate-delay reduction (by a factor of $1/S$) with a constant line response time. Because of the short lines in a scaled block graph, gate delay is typically one order of magnitude higher than the local line response. The effect of long-distance interconnection lines on total delay time for the transmission of signals from block to block is discussed in the following sections.

The communication between blocks in a super-block graph is accomplished via long-distance interconnections. In the design of a complex system with a large number of functions on a chip, optimization of length of the interconnections is of major importance. The average wire length can be estimated

TABLE II
SCALING OF LOCAL INTERCONNECTION LINES FOR CONSTANT RESPONSE TIME AND CONSTANT FIELD

Interconnection Parameter	Scaling Factor* (S)
Interconnection dimensions L_L, H, W, L_S, X_{ox}	$1/S$
Line resistance $R = \rho L_L / WH$	S
Line capacitance $C_{ox} = K_{ox} \epsilon_0 L_S W / X_F$	$1/S$
Interelectrode capacitance $C_i = K_{ox} \epsilon_0 L H / L_S$	$1/S$
Line response time $0.89 RC$	1
Line voltage drop IR	1
Line current density	S

*Scaling factor $S > 1$.

by a very useful statistical formula [7]

$$L_{max} = KA^g \quad (8)$$

where

L_{max} maximum wire length
 A chip area
 K, g constants.

A good rule of thumb is $K = g = 1/2$ [7]. With these values, the average length of the long-distance interconnections is given by

$$L_{max} = \frac{\sqrt{\text{chip area}}}{2}. \quad (9)$$

Assuming that chip area will increase with the continuing development of IC processing, the effect of scaling of transistors and local interconnections on the scaling of long-distance interconnection lines can be determined. The results are summarized in Table III where it is assumed that the maximum long-distance or block-to-block interconnection line increases by a factor of $S_c > 1$. It can be concluded, therefore, that the long-distance line voltage drop will increase with scaling. Because the long-distance line response time rises drastically as a result of scaling, a substantial amount of delay and energy is dissipated during communication across the interconnection lines, and therefore, the performance of the circuits can suffer from technological advancement.

IV. ESTIMATION OF AVERAGE INTERCONNECTION LENGTH

The systematic approach taken to anticipate the problems that will arise in future VLSI can be optimized by introducing realistic data. Fig. 4 is an extrapolation of the basic capabilities of semiconductor technology as measured by chip size and minimum dimension resulting from the lithographic process. The data for this plot were obtained by many investigators of bipolar and MOS technologies. The prediction of a $0.5\text{-}\mu\text{m}$ feature size and 200-mm^2 chip size by the late 1980's appears to be reasonable. Applying (9) and the data in Fig. 4, the

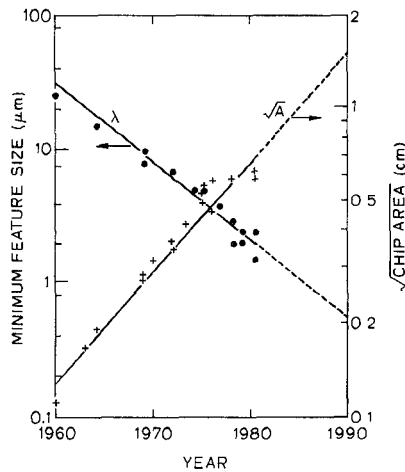


Fig. 4. Variation of minimum feature size and chip size versus year of fabrication for the state-of-the-art chip fabricated that year.

TABLE III
SCALING OF LONG-DISTANCE INTERCONNECTION LINES FOR CONSTANT
LOCAL RESPONSE TIME AND CONSTANT FIELD

Interconnection Parameter	Scaling Factor* (S)
Long-distance interconnection dimensions H, W, L_s, X_F	$1/S$
Long-distance interconnection dimension L_{max}^\dagger	S_c
Line resistance $R = \rho L_{max}/WH$	$S_c^2 S_c$
Line capacitance $C_{ox} = K_{ox} \epsilon_0 L_{max} W/X_{ox}$	S_c
Interelectrode capacitance $C_I = K_{ox} \epsilon_0 L_{max} H/L_s$	S_c
Line response time $0.89 RC$	$S_c^2 S_c^2$
Line voltage drop IR	$S S_c$
Line current density	S

* $S, S_c > 1$.

$^\dagger L_{max} = \frac{\sqrt{\text{chip area}}}{2} \rightarrow \text{scaling factor } S_c$.

maximum average long-distance wire length is estimated to be one-half the size of the chip edge. An exponential fitting to these data reveals the following relationships:

$$\lambda = 10^{-5} \exp [-0.135 (t - 1900)] \quad (10)$$

where λ is the minimum feature size (μm), t = year (1968, 1975, 1990), and, for long-distance interconnection length (block to block)

$$L_{max} = \frac{\sqrt{A}}{2} = 2.5 \times 10^{-5} \exp [0.089 (t - 1900)] \text{ cm.} \quad (11)$$

V. ESTIMATION OF AVERAGE DELAY TIME FOR SIGNAL TRANSMISSION

In this section, the long-distance interconnection line delay has been addressed as an unavoidable limit on a system performance. A model for interconnection delay time was devel-

oped in Section III. Equation (7) relates the delay time to various technological elements. We will further develop this equation in this section.

According to the theory of scaling [1], vertical as well as horizontal dimensions should be scaled down to reduce the device size and thus improve the device performance. Therefore, most of the device dimensions are controlled by the minimum feature size λ , allowed by the technology. For a large chip, the major fraction of the area is occupied by the interconnections and not by the device [7]. Therefore, to minimize the chip area, the width and spacing between the interconnections should be kept at the minimum feature size, i.e.,

$$L_s = W = \lambda. \quad (12)$$

We can also assume that the thickness of the oxide and the interconnection scale with the minimum feature size. A good assumption is

$$\begin{aligned} X_{ox} &= 0.35 \lambda \\ H &= 0.25 \lambda. \end{aligned} \quad (13)$$

For the relationships predicted by (12) and (13), the value of K_1 from the model of Dang and Shigyo [2] is approximately 2. By combining (7), (9), (12), and (13), a simple relationship is obtained to calculate τ_L

$$\tau_L = 5.53 \epsilon_0 K_{ox} \rho \frac{A}{\lambda^2}. \quad (14)$$

The above equation relates τ_L to some key technological parameters. The product $K_{ox} \rho$ is a purely physical measure determined by the electrode material and the property of its surrounding ambient (SiO_2); on the other hand, A/λ^2 is a measure of the technology and number of components on the chip (bits of memory, logic gates). Because the objective for improving IC fabrication technology is to pack more components on a single chip, the target is to increase the value of A/λ^2 ; however, $K_{ox} \rho$ must be reduced to minimize τ_L . This can be achieved by lowering electrode resistivity by the selection of low-resistance materials as the interconnection electrode.

By substituting the values of λ and A from (10) and (11), respectively, in (14), τ_L can be predicted as a function of time

$$\tau_L = 1.3 \times 10^8 \epsilon_0 K_{ox} \rho \exp [0.448 (t - 1900)]. \quad (15)$$

The above equation predicts the interconnection delay time as a function of time for the largest chip fabricated that year using the state-of-the-art technology as predicted by Fig. 4. The estimated values of τ_L as a function of time are plotted in Fig. 5 for polysilicon, tungsten silicide, tungsten, and aluminum with thin-film resistivities of 500, 30, 10, and $3 \mu\Omega \cdot \text{cm}$, respectively. Also plotted are the values of gate delay obtained from the literature.¹ It is evident that as time is progressing, the delay is decreasing, however, the interconnection delay is increasing. Depending upon the interconnection materials, at certain times the speed of the state-of-the-art chip will be

¹The data shown here were collected from various publications, conference proceedings, and product announcements by various manufacturers. The gate delay does not scale here by the scaling factor S mainly because not all of the scaling rules were followed in manufacturing these IC's.

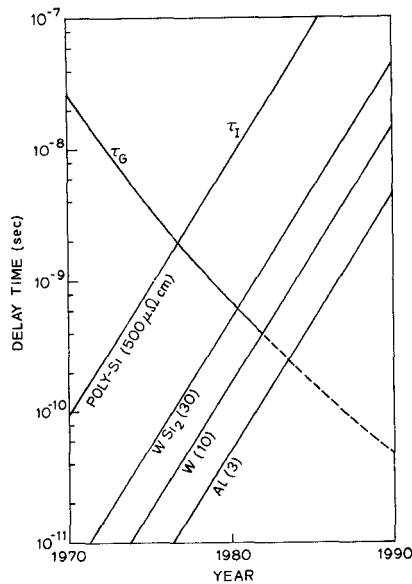


Fig. 5. Interconnection time delay and average gate delay versus year of fabrication for the state-of-the-art chip fabricated that year.

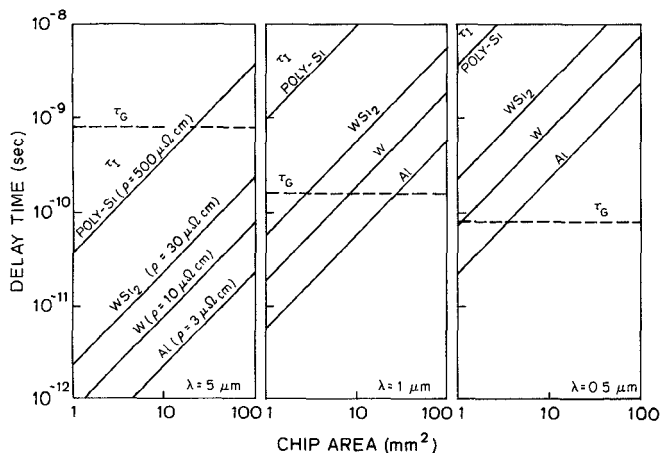


Fig. 6. Interconnection time delay versus the chip area for heavily doped polysilicon, WSi_2 , W, and Al for minimum feature sizes of 5, 1, and $0.5 \mu m$.

limited by the interconnections and not by the devices. This is a serious implication and could become a major factor in the evolution of integrated electronics.

The preceding analysis was done only for the state-of-the-art chip with biggest area and smallest feature size, to show the technological trends. In general, one would like to know the values of τ_g and τ_L for all values of λ and A , because most of the chips manufactured at a certain time do not necessarily follow the state-of-the-art technology. Using (14), τ_L has been calculated as a function of A and λ and the results are plotted in Fig. 6. It is seen that τ_L increases as A is increased and λ is decreased, which are trends for future technology. Also shown are values of τ_g which are dependent only upon λ and not upon A . Ideal scaling rules [1] have been assumed to estimate these values of τ_g . It is seen clearly that for $5\text{-}\mu m$ technology, except for very-large-area chips, the performance is mainly device controlled. For $1\text{-}\mu m$ technology, the higher resistivity materials combined with large chip area make the performance interconnection controlled. For the lower resistivity material like W and Al, the chip performance is still controlled by the

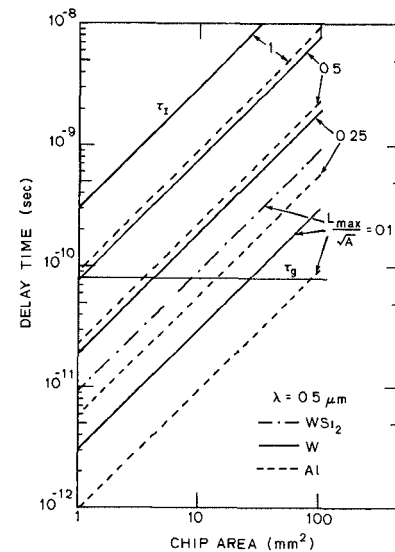


Fig. 7. Interconnection time delays versus chip area for $L_{max} = \sqrt{A} = 1.0, 0.5, 0.25, \text{ and } 0.1$.

devices. For $0.5\text{-}\mu m$ technology, the chip performance is largely controlled by the interconnections.

In the analysis leading to Figs. 5 and 6 it was assumed that $L_{max} = 0.5\sqrt{A}$. This might not always be correct. In many circuits, L_{max} might be either larger or smaller than $0.5\sqrt{A}$. Fig. 7 shows the effect of this variation. It is evident that for the same chip area substantial reduction in τ_L can be obtained by keeping the length of interconnections smaller.

VI. MATERIALS FOR MULTILAYER INTERCONNECTIONS

It has been demonstrated in this work that, as device dimensions are becoming increasingly smaller, severe requirements are being imposed on the electrode material. The basic demand is conductivity because it can substantially improve the resistances and delay times of the electrical interconnection lines used for VLSI structures. In general, several other requirements are imposed on interconnection materials by the fabrication technology. In a multilayer interconnection structure, the layers incorporated early in the process sequence might be subjected to several fabrication steps, yet other layers incorporated much later might not be subjected to that many steps. The most rigorous set of requirements can be summarized as

- low resistivity,
- ability to withstand the chemicals and high temperatures required in the fabrication process,
- ability to be thermally oxidized,
- stability of contacts to other layers,
- good MOS properties,
- resistance to electromigration,
- capability to be defined into fine patterns.

Not all of the requirements will be applicable to all of the layers, however, the selection of a material becomes easier if it meets more requirements.

Historically, metals like aluminum and gold have been used in bipolar and MOS IC's. With the advent of silicon-gate MOS technology, polysilicon has been extensively used to form gate electrodes and interconnections. Refractory metals such as tungsten (W), molybdenum (Mo), titanium (Ti), and tantalum

(Ta) and their silicides are receiving increased attention as a replacement/compliment of polysilicon. Table IV gives a comparison of the properties of polysilicon, metals, and silicides. Polysilicon meets all of the requirements addressed above, however, its high resistivity is beginning to limit the performance of the larger area circuits. Its use is, therefore, limited to the interconnections in those parts of the circuit where RC delay times are not critical and where cleanliness and other good properties of polysilicon are badly needed; for example, to form gate electrodes in MOS transistors and the local interconnections of relatively small length. Aluminum does not meet all of the requirements. Because of its poor high-temperature capabilities, it can be incorporated in the process only after all of the high-temperature steps have been finished. Very fine lines of Al are questionable because of its poor electromigration properties [8]. Since the oxides of W and Mo are volatile at high temperatures, these metals can be used only when all of the steps where exposure to high-temperature oxidizing ambient might occur are over but high-temperature steps in inert ambient are still remaining. Silicides of W, Mo, and Ta have reasonably good compatibility with the IC fabrication technology [9]–[12]. They have fairly high conductivity; they can withstand all of the chemicals normally encountered during the fabrication process. Therefore, they can be used in all of the applications where polysilicon has been used so far. $TiSi_2$ is also very attractive for this application, except its etch rate in hydrofluoric acid (HF) is very large. If the use of HF can be avoided during the fabrication by employing dry-etching techniques, $TiSi_2$ can also be used successfully [13]. A combination of silicides and polysilicon (usually known as polycide) can also be used in such situations [11]. Since the conductivity of such a sandwich layer is dominated by the silicide, in this study we have not tried to differentiate between polycides and silicides.

One factor which has not been discussed in this work is the use of a dielectric material with lower dielectric constant than SiO_2 . This will result in lower capacitance as predicted by (4). Not much work has been done in this area, however, this could become an important area of future research.

VII. CONCLUSION

From the results presented here it is evident that RC time delay associated with interconnections can be a significant portion of the total circuit time delay, especially for VLSIC. If the device dimensions are scaled down following the laws of ideal scaling [1] and the circuit size and complexity keeps growing as it has been in the past, this problem becomes even more serious, as is evident from Figs. 4 and 5. If the design rules are not altered drastically, e.g., the length of the interconnections bears the relationship governed by (9), the overall performance of the future VLSI circuits will be totally controlled by the properties of interconnection material, as shown in Figs. 5 and 6. Eventually for very large circuits, even Al may not prove to be a low-resistivity material. By changing the design rules, e.g., by making the length of the interconnection smaller, the circuit performance could be significantly improved as shown in Fig. 7. A combination of several mate-

TABLE IV
PROPERTIES OF INTERCONNECTION MATERIALS

MATERIALS	BULK RESISTIVITY ($\mu\Omega\text{ cm}$)	THIN-FILM RESISTIVITY ($\mu\Omega\text{ cm}$)	MELTING POINT ($^{\circ}\text{C}$)	CHEMICAL COMPATIBILITY	THERMAL OXIDATION
POLY-Si	250	500	1410	YES	YES
AL	2.26	3	660	?	NO
W	5.5	10	3410	?	NO
Mo	5.0	10	2610	?	NO
WSi_2	12.5	30	2165	YES	YES
$MoSi_2$	21.6	40	2050	YES	YES
$TaSi_2$	8.5	35	2170	YES	YES
$TiSi_2$	13	15	1540	?	YES

* $TiSi_2$ is etched severely in HF

rials will have to be used to optimize the circuit performance. The selection of the materials will be dictated by the requirements of the circuits and conditions imposed by fabrication technology.

ACKNOWLEDGMENT

The authors wish to thank J. D. Meindl for valuable discussions.

REFERENCES

- [1] R. H. Dennard, F. H. Gaensslen, H. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlank, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 256–268, 1974.
- [2] R. L. M. Dang and N. Shigyo, "A two-dimensional simulation of LSI interconnect capacitance," *IEEE Electron Device Lett.*, vol. EDL-2, pp. 196–197, Aug. 1981.
- [3] W. H. Chang, "Analytical IC metal-line capacitance formulas," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 608–611, Sept. 1976.
- [4] W. M. Kaufman and S. J. Garrett, "Tapered distributed filters," *IRE Trans. Circuit Theory*, vol. CT-9, pp. 329–336, Dec. 1962.
- [5] A. Wilnai, "Open-ended RC line model predicts MOSFET IC response," *EDN*, pp. 53–54, Dec. 15, 1971.
- [6] B. S. Landman and R. L. Russo, "On a pin versus block relationship for partitions of logic graphs," *IEEE Trans. Comput.*, vol. C-20, p. 1469, 1971.
- [7] R. W. Keyes, "The evolution of digital electronics towards VLSI," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 271–278, 1979.
- [8] F. M. d'Heurle and J. M. Poate, "Electromigration in thin films," in *Thin Films—Interdiffusion and Reactions*, J. M. Poate, K. N. Tu, and J. W. Meyer, Eds. New York: Wiley, 1978.
- [9] T. Mochizuki, K. Shibata, T. Inoue, and K. Ohuchi, "A new MOS process using $MoSi_2$ as a gate material," *Japan. J. Appl. Phys.*, Suppl., vol. 17, pp. 37–42, 1977.
- [10] F. Mohammadi and K. C. Saraswat, "Properties of sputtered tungsten silicide for MOS integrated circuit applications," *J. Electrochem. Soc.*, vol. 127, pp. 450–454, 1980.
- [11] B. L. Crowder and S. Zirinsky, "1- μm MOSFET VLSI technology. Part VII: Metal silicide interconnection technology—A future perspective," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 369–371, 1979.
- [12] H. J. Geipel, Jr., N. Hsieh, M. H. Ishaq, C. W. Koburger, and F. R. White, "Composite silicide gate electrodes—Interconnections for VLSI device technologies," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1417–1424, 1980.
- [13] S. P. Murarka, D. B. Fraser, A. K. Sinha, and H. J. Levinstein, "Refractory silicides of titanium for low-resistivity gates and interconnects," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1425–1430, 1980.