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ABOUT THE COVER

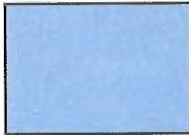
In the background is a processed wafer of silicon on which a large number of identical circuit chips are fabricated. When cut from such a wafer, a chip can be housed in a package such as the one shown here with its cover removed. This single chip is a segmented memory array with a very large number of active devices in a variety of intricate circuit structures. The growing need for efficient and reliable low-cost components such as these underlies the importance of the various circuit design and circuit analysis techniques discussed in this text.

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There are two major types of three-terminal semiconductor devices: the bipolar junction transistor (BJT), which is the subject of this chapter, and the field-effect transistor (FET), which we shall study in Chapter 5. The two transistor types are equally important, and each offers distinct advantages and has unique areas of application.

The bipolar transistor consists of two *pn* junctions constructed in a special way and connected in series, back to back. Current is conducted by both electrons and holes, hence the name bipolar.

The BJT, often referred to simply as “the transistor,” is widely used in discrete circuits as well as in IC design, both analog and digital. The device characteristics are so well understood that one is able to design transistor circuits whose performance is remarkably predictable and quite insensitive to variations in device parameters.

We shall start by presenting a simple qualitative description of the operation of the transistor. Though simple, this physical description provides considerable insight into the performance of the transistor as a circuit element. We will quickly move from describing current flow in terms of holes and electrons to a study of transistor terminal characteristics. First-order models for transistor operation in different modes will be developed and utilized in the analysis of transistor circuits. One of the main objectives of this chapter is to develop in the reader a high degree of familiarity with the transistor. Thus by the end of the chapter the reader should be able to perform rapid first-order analysis of transistor circuits, as well as design single-stage transistor amplifiers.

4.1 PHYSICAL STRUCTURE AND MODES OF OPERATION

Figure 4.1 shows a simplified structure for a BJT. A practical transistor structure will be shown later (see also Appendix A, which deals with fabrication technology).

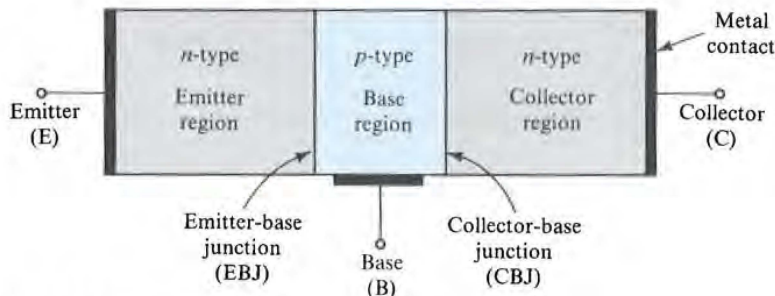


Fig. 4.1 A simplified structure of the *npn* transistor.

As shown in Fig. 4.1, the BJT consists of three semiconductor regions: the emitter region (*n* type), the base region (*p* type), and the collector region (*n* type). Such a transistor is called an *npn* transistor. Another transistor, a dual of the *npn* as shown in Fig. 4.2, has a *p*-type emitter, an *n*-type base, and a *p*-type collector and is appropriately called a *pnp* transistor.

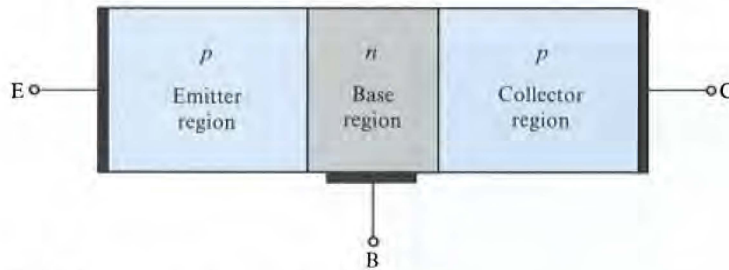


Fig. 4.2 A simplified structure of the *pnp* transistor.

A terminal is connected to each of the three semiconductor regions of a transistor, with the terminals labeled **emitter (E)**, **base (B)**, and **collector (C)**.

The transistor consists of two *pn* junctions, the emitter–base junction (EBJ) and the collector–base junction (CBJ). Depending on the bias condition (forward or reverse) of each of these junctions, different modes of operation of the BJT are obtained, as shown in Table 4.1.

The active mode is the one used if the transistor is to operate as an amplifier. Switching applications (for example, logic circuits) utilize both the cutoff and the saturation modes.

Table 4.1 BJT MODES OF OPERATION

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

4.2 OPERATION OF THE *n*pn TRANSISTOR IN THE ACTIVE MODE

Let us start by considering the physical operation of the transistor in the active mode. This situation is illustrated in Fig. 4.3 for the *n*pn transistor. Two external voltage sources (shown as batteries) are used to establish the required bias conditions for active-mode operation. The voltage V_{BE} causes the *p*-type base to be higher in potential than the *n*-type emitter, thus forward-biasing the emitter–base junction. The collector–base voltage V_{CB} causes the *n*-type collector to be higher in potential than the *p*-type base, thus reverse-biasing the collector–base junction.

Current Flow

In the following description of current flow only diffusion-current components are considered. Drift currents due to thermally generated minority carriers are usually very small and can be neglected. We will have more to say about these reverse-current components at a later stage.

Field-Effect Transistors (FETs)

Introduction

- | | | | |
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| 5.1 | Structure and Physical Operation of the Enhancement-Type MOSFET | 5.7 | Biasing the FET in Discrete Circuits |
| 5.2 | Current-Voltage Characteristics of the Enhancement MOSFET | 5.8 | Basic Configurations of Single-Stage FET Amplifiers |
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INTRODUCTION

In this chapter we study the other major type of transistor, the field-effect transistor (FET). As in the case of the BJT (Chapter 4), the voltage between two terminals of the FET controls the current flow in the third terminal. Correspondingly, the FET can be used both as an amplifier and as a switch.

The field-effect transistor derives its name from the essence of its physical operation. Specifically, it will be shown that the current-control mechanism is based on an electric field established by the voltage applied to the control terminal. It will also be shown that current is conducted by only one type of carrier (electrons or holes) depending on the type of FET (n channel or p channel), which gives the FET another name, the **unipolar transistor**.

Although the basic concept of the FET has been known since the 1930s, the device became a practical reality only in the 1960s. Since the late 1970s, a particular kind of FET, the **metal-oxide semiconductor field-effect transistor (MOSFET)**, has been ex-

tremely popular. Compared to BJTs, MOS transistors can be made quite small (that is, occupying a small silicon area on the IC chip), and their manufacturing process is relatively simple (see Appendix A). Furthermore, digital logic and memory functions can be implemented with circuits that exclusively use MOSFETs (that is, no resistors or diodes are needed). For these reasons, most very-large-scale integrated (VLSI) circuits are made at the present time using MOS technology. Examples include microprocessor and memory chips. MOS technology has also been applied extensively in the design of analog integrated circuits.

Although the FET family of devices has many different types, and we shall discuss a few, most of the chapter is devoted to the enhancement-type MOSFET, which is by far the most significant field-effect transistor. Its significance is on par with that of the bipolar junction transistor, with each having its own areas of application.

Field-effect transistors are available in discrete form, and we shall study their application in discrete circuit design. Their most important use, however, is in the design of integrated circuits. The study of MOS integrated circuits begins in this chapter and is continued in subsequent chapters.

5.1 STRUCTURE AND PHYSICAL OPERATION OF THE ENHANCEMENT-TYPE MOSFET

The enhancement-type MOSFET is the most widely used field-effect transistor. In this section we shall study its structure and physical operation. This will lead to the current-voltage characteristics of the device, studied in the next section.

Device Structure

Figure 5.1 shows the physical structure of the n -channel enhancement-type MOSFET. The meaning of the names “enhancement” and “ n -channel” will become apparent shortly. The transistor is fabricated on a p -type substrate, which is a single-crystal silicon wafer that provides physical support for the device (and for the entire circuit in the case of an integrated circuit). Two heavily doped n -type regions, indicated in the figure as the n^+ source¹ and the n^+ drain regions, are created in the substrate. A thin (about $0.1\ \mu\text{m}$) layer² of silicon dioxide (SiO_2), which is an excellent electrical insulator, is grown on the surface of the substrate, covering the area between the source and drain regions. Metal is deposited on top of the oxide layer to form the gate electrode of the device. Metal contacts are also made to the source region, the drain region, and the substrate, also known as the body. Thus, four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

At this point it should be clear that the name of the device (metal-oxide-semiconductor FET) is derived from its physical structure. The name, however, has become a general one and is used also for FETs that do not use metal for the gate electrode. In fact, most

¹The notation n^+ indicates heavily doped n -type silicon. Conversely, n^- is used to denote lightly doped n -type silicon. Similar notation applies for p -type silicon.

²A micrometer (μm), also called micron, is $10^{-6}\ \text{m}$.

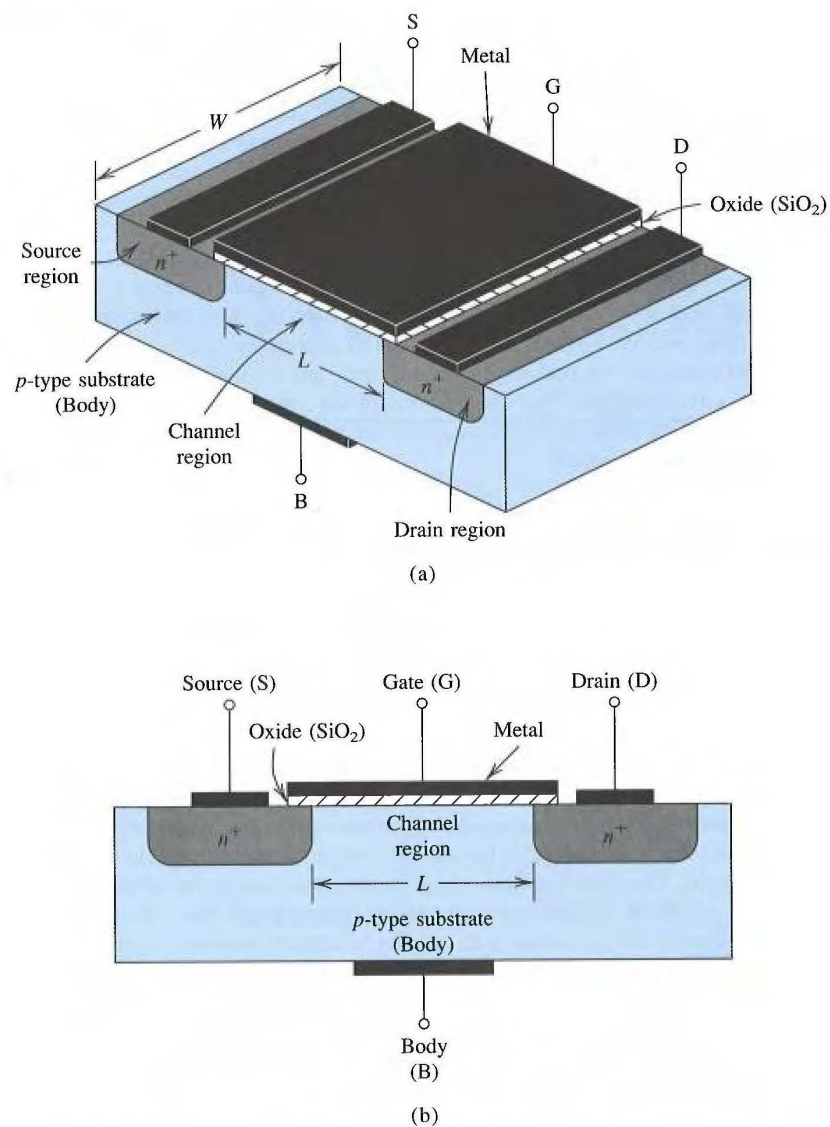


Fig. 5.1 Physical structure of enhancement-type NMOS transistor: (a) perspective view; (b) cross section. Typically $L = 1$ to $10\ \mu\text{m}$, $W = 2$ to $500\ \mu\text{m}$, and the thickness of the oxide layer is of the order of $0.1\ \mu\text{m}$.

modern MOSFETs are fabricated using a process known as silicon-gate technology, in which a certain type of silicon, called polysilicon, is used to form the gate electrode (see Appendix A). Our description of MOSFET operation and characteristics apply irrespective of the type of gate electrode.

Another name for the MOSFET is the **insulated-gate FET** or **IGFET**. This name also arises from the physical structure of the device, emphasizing the fact that the gate electrode is electrically insulated from the device body (by the oxide layer). It is this insulation that causes the current in the gate terminal to be extremely small (of the order of 10^{-15} A).

Observe that the substrate forms *pn* junctions with the source and drain regions. In normal operation these *pn* junctions are kept reverse-biased at all times. Since the drain will be at a positive voltage relative to the source, the two *pn* junctions can be effectively cut off by simply connecting the substrate terminal to the source terminal. We shall assume this to be the case in the following description of MOSFET operation. Thus, here, the substrate will be considered as having no effect on device operation, and the MOSFET will be treated as a three-terminal device, with the terminals being the gate (G), the source (S), and the drain (D). It will be shown that a voltage applied to the gate controls current flow between source and drain. This current will flow in the longitudinal direction from drain to source in the region labeled "channel region." Note that this region has a length L and a width W , two important parameters of the MOSFET. Typically, L is in the range 1 to 10 μm , and W is in the range 2 to 500 μm . Finally note that, unlike the BJT, the MOSFET is normally constructed as a symmetrical device. Thus its source and drain can be interchanged with no change in device characteristics.

Operation with No Gate Voltage

With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the *pn* junction between the n^+ drain region and the *p*-type substrate, and the other diode is formed by the *pn* junction between the *p*-type substrate and the n^+ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage v_{DS} is applied. In fact, the path between drain and source has a very high resistance (of the order of $10^{12} \Omega$).

Creating a Channel for Current Flow

Consider next the situation depicted in Fig. 5.2. Here we have grounded the source and the drain and applied a positive voltage to the gate. Since the source is grounded, the gate voltage appears in effect between gate and source and thus is denoted v_{GS} . The positive voltage on the gate causes in the first instance the free holes (which are positively charged) to be repelled from the region of the substrate under the gate (the channel region). These holes are pushed downward into the substrate, leaving behind a carrier-depletion region. The depletion region is populated by the bound negative charge associated with the acceptor atoms. These charges are "uncovered" because the neutralizing holes have been pushed downward into the substrate.

As well, the positive gate voltage attracts electrons from the n^+ source and drain regions (where they are in abundance) into the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an *n* region is in

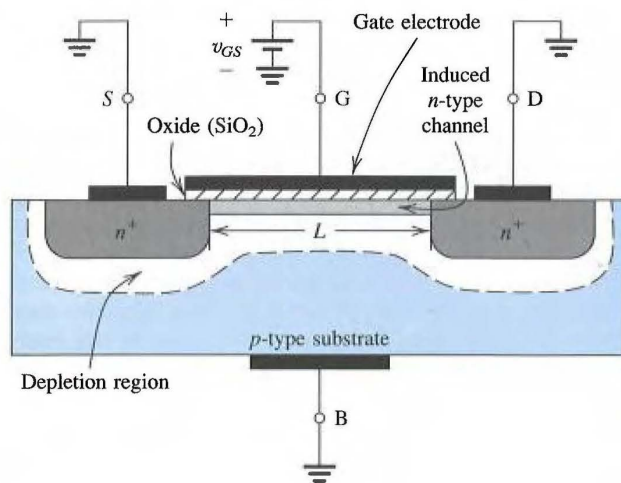


Fig. 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate.

effect created, connecting the source and drain regions, as indicated in Fig. 5.2. Now if a voltage is applied between drain and source, current flows through this induced n region, carried by the mobile electrons. The induced n region thus forms a **channel** for current flow from drain to source and is aptly called so. Correspondingly, the MOSFET of Fig. 5.2 is called an **n -channel MOSFET** or, alternatively, an **NMOS transistor**. Note that an n -channel MOSFET is formed in a p -type substrate: The channel is created by inverting the substrate surface from p type to n type. Hence the induced channel is called an **inversion layer**.

The value of v_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage** and is denoted V_t .³ Obviously, V_t for an n -channel FET is positive. The value of V_t is controlled during device fabrication and typically lies in the range 1 to 3 V.

The gate and body of the MOSFET form a parallel-plate capacitor with the oxide layer acting as the capacitor dielectric. The positive gate voltage causes positive charge to accumulate on the top plate of the capacitor (the gate electrode). The corresponding negative charge of the bottom plate is formed by the electrons in the induced channel. An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, and thus it determines the channel conductivity and, in turn, the current that will flow through the channel when a voltage v_{DS} is applied.

Applying a Small v_{DS}

Having induced a channel, we now apply a positive voltage v_{DS} between drain and source, as shown in Fig. 5.3. We first consider the case where v_{DS} is small (say, 0.1 or 0.2 V).

³Many texts use V_T to denote the threshold voltage. We use V_t to avoid confusion with the thermal voltage V_T .

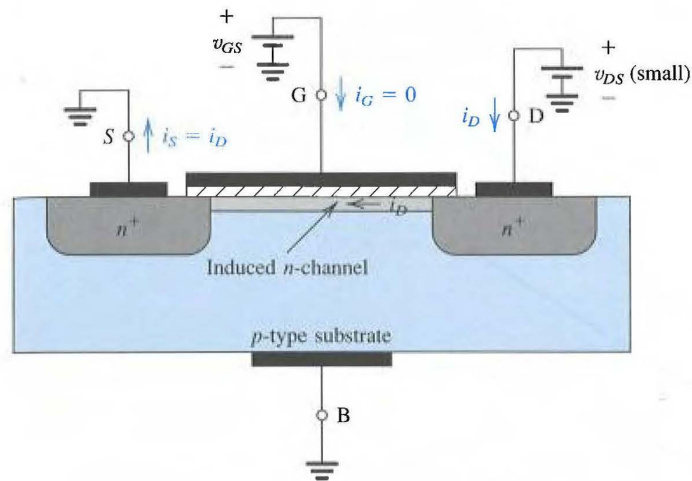


Fig. 5.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a conductance whose value is determined by v_{GS} . Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)v_{DS}$. Note that the depletion region is not shown (for simplicity).

The voltage v_{DS} causes a current i_D to flow through the induced n channel. Current is carried by free electrons traveling from source to drain (hence the names source and drain). The magnitude of i_D depends on the density of electrons in the channel, which in turn depends on the magnitude of v_{GS} . Specifically, for $v_{GS} = V_t$ the channel is just induced and the current conducted is still negligibly small. As v_{GS} exceeds V_t , more electrons are attracted into the channel. We may visualize the increase in charge carriers in the channel as an increase in the channel depth. The result is a channel of increased conductance or equivalently reduced resistance. In fact, the conductance of the channel is proportional to the **excess gate voltage** ($v_{GS} - V_t$). It follows that the current i_D will be proportional to $v_{GS} - V_t$ and, of course, to the voltage v_{DS} that causes i_D to flow.

Figure 5.4 shows a sketch of i_D versus v_{DS} for various values of v_{GS} . We observe that the MOSFET is operating as a linear resistance whose value is controlled by v_{GS} . The resistance is infinite for $v_{GS} \leq V_t$, and its value decreases as v_{GS} exceeds V_t .

The description above indicates that for the MOSFET to conduct, a channel has to be induced. Then, increasing v_{GS} above the threshold voltage V_t enhances the channel, hence the names **enhancement-mode operation** and **enhancement-type MOSFET**. Finally, we note that the current that leaves the source terminal (i_S) is equal to the current that enters the drain terminal (i_D), and the gate current $i_G = 0$.

Operation as v_{DS} is Increased

We next consider the situation as v_{DS} is increased. For this purpose let v_{GS} be held constant at a value greater than V_t . Refer to Fig. 5.5, and note that v_{DS} appears as a voltage drop across the length of the channel. That is, as we travel along the channel from source

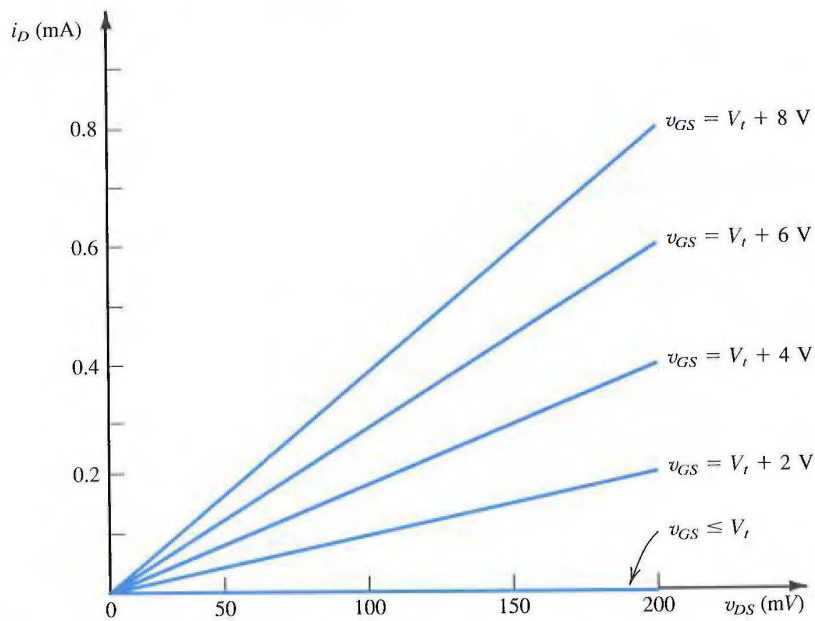


Fig. 5.4 The i_D - v_{DS} characteristics of the MOSFET in Fig. 5.3. Note that v_{DS} is small. The device operates as a linear resistor whose value is controlled by v_{GS} .

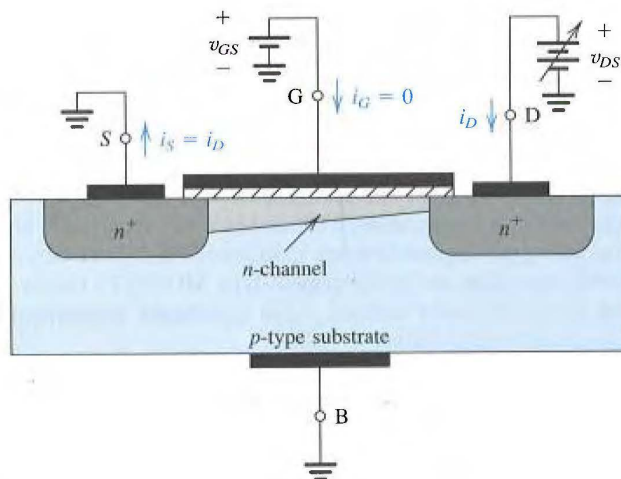


Fig. 5.5 Operation of the enhancement NMOS' transistor as v_{DS} is increased. The induced channel acquires a tapered shape and its resistance increases as v_{DS} is increased. Here v_{GS} is kept constant at a value $> V_t$.

to drain, the voltage (measured relative to the source) increases from 0 to v_{DS} . Thus the voltage between the gate and points along the channel decreases from v_{GS} at the source end to $v_{GS} - v_{DS}$ at the drain end. Since the channel depth depends on this voltage, we find that the channel is no longer of uniform depth; rather, the channel will take the tapered form shown in Fig. 5.5, being deepest at the source end and shallowest at the drain end. As v_{DS} is increased, the channel becomes more tapered and its resistance increases correspondingly. Thus the i_D - v_{DS} curve does not continue as a straight line but bends as shown in Fig. 5.6. Eventually, when v_{DS} is increased to the value that reduces

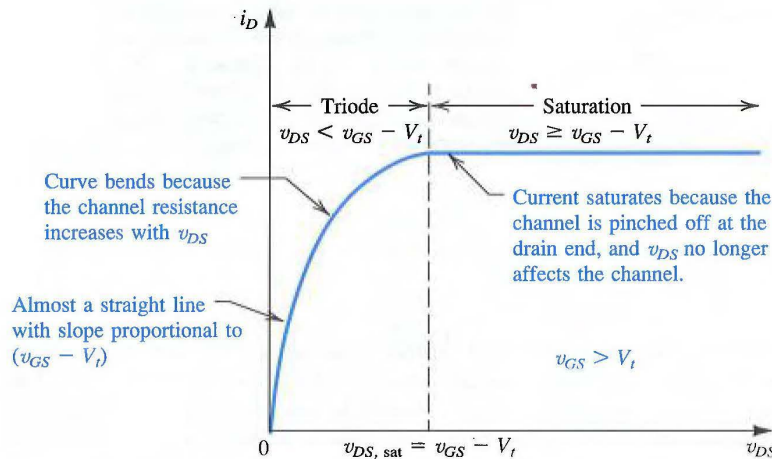


Fig. 5.6 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

the voltage between gate and channel at the drain end to V_t —that is, $v_{GS} - v_{DS} = V_t$ or $v_{DS} = v_{GS} - V_t$ —the channel depth at the drain end decreases to almost zero, and the channel is said to be **pinched off**. Increasing v_{DS} beyond this value has little effect (theoretically, no effect) on the channel shape, and the current through the channel remains constant at the value reached for $v_{DS} = v_{GS} - V_t$. The drain current thus **saturates** at this value, and the MOSFET is said to have entered the **saturation region**⁴ of operation. The voltage v_{DS} at which saturation occurs is denoted $v_{DS,sat}$,

$$v_{DS,sat} = v_{GS} - V_t \quad (5.1)$$

Obviously, for every value of $v_{GS} \geq V_t$, there is a corresponding value of $v_{DS,sat}$. The device operates in the saturation region if $v_{DS} \geq v_{DS,sat}$. The region of the i_D - v_{DS} charac-

⁴ Saturation in a MOSFET means a very different thing than in a BJT. This is a rather unfortunate situation but cannot be changed at this time: Virtually the entire electronics literature uses this terminology!

teristic obtained for $v_{DS} < v_{DS,sat}$ is called the **triode region**, a carryover from the days of vacuum-tube devices whose operation an FET resembles.

To help further in visualizing the effect of v_{DS} , we show in Fig. 5.7 sketches of the channel as v_{DS} is increased while v_{GS} is kept constant. Theoretically, any increase in v_{DS} above $v_{DS,sat}$ (which is equal to $v_{GS} - V_t$) has no effect on the channel shape and simply appears across the depletion region surrounding the channel and the n^+ drain region.

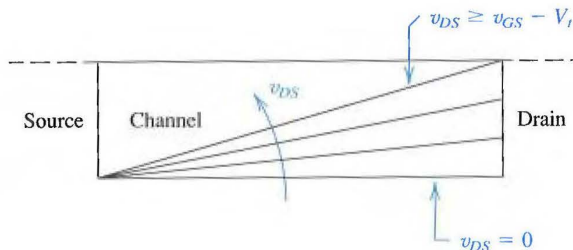


Fig. 5.7 Increasing v_{DS} causes the channel to acquire a tapered shape. Eventually, as v_{DS} reaches $v_{GS} - V_t$, the channel is pinched off at the drain end. Increasing v_{DS} above $v_{GS} - V_t$ has little effect (theoretically, no effect) on the channel's shape.

The *p*-channel MOSFET

A *p*-channel enhancement-type MOSFET (PMOS transistor) is fabricated on an *n*-type substrate with p^+ regions for the drain and source, and holes as charge carriers. The device operates in the same manner as the *n*-channel device except that v_{GS} and v_{DS} are negative and the threshold voltage V_t is negative. Also the current i_D enters the source terminal and leaves through the drain terminal.

PMOS technology was originally the dominant one. However, because NMOS devices can be made smaller and thus operate faster, and because NMOS requires lower supply voltages than PMOS, NMOS technology has virtually replaced PMOS. Nevertheless, it is important to be familiar with the PMOS transistor for two reasons: PMOS devices are still available for discrete-circuit design, and more importantly, both PMOS and NMOS transistors are utilized in **complementary MOS** or **CMOS** circuits.

Complementary MOS or CMOS

As the name implies, complementary MOS technology employs MOS transistors of both polarities. Although CMOS circuits are somewhat more difficult to fabricate than NMOS, the availability of complementary devices makes possible many powerful circuit-design possibilities. Indeed, at the present time CMOS is the most useful of all the integrated-circuit MOS technologies. This statement applies to both analog and digital circuits. Throughout this book we will study many CMOS circuit techniques.

Figure 5.8 shows a cross section of a CMOS chip illustrating how the PMOS and NMOS transistors are fabricated. Observe that while the PMOS transistor is implemented directly in the *n*-type substrate, the NMOS transistor is fabricated in a specially created *p* region, known as a *p* well. The two devices are isolated from each other by a thick region of oxide that functions as an insulator.

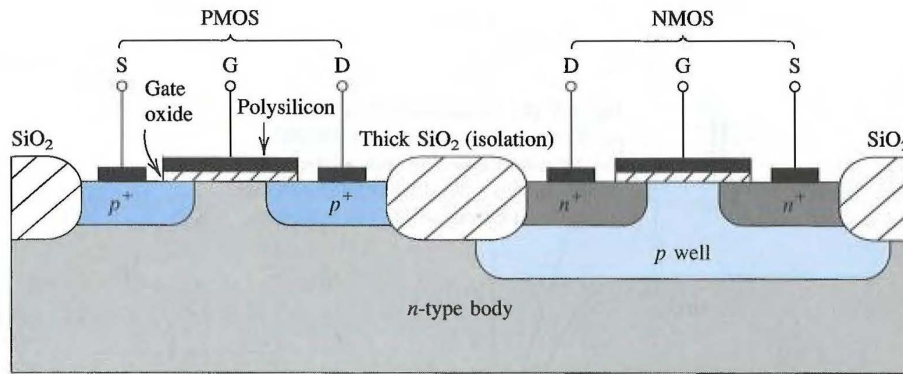


Fig. 5.8 Cross section of a CMOS integrated circuit. Note that the NMOS transistor is formed in a separate p -type region, known as a p well. Another arrangement is also possible in which a p -type body is used and the p device is formed in an n well.

Operating the MOS Transistor in the Subthreshold Region

The above description of MOSFET operation implies that for $v_{GS} < V_t$, no current flows and the device is cut off. This is not entirely true for it has been found that for values of v_{GS} smaller but close to V_t , a small drain current flows. In this **subthreshold region** of operation the drain current is exponentially related to v_{GS} , much like the i_C - v_{BE} relationship of a BJT.

Although in most applications the MOS transistor is operated with $v_{GS} > V_t$, there are special, but a growing number of, applications that make use of subthreshold operation. In this book we will not consider subthreshold operation any further and refer the reader to the references listed at the end of the chapter [see in particular Mead (1988) and Tsividis (1987)].

5.2 CURRENT-VOLTAGE CHARACTERISTICS OF THE ENHANCEMENT MOSFET

Building on the physical foundation established in the previous section for the operation of the enhancement MOS transistor, we present in this section its complete current-voltage characteristics. These characteristics can be measured at dc or at low frequencies and thus are called static characteristics. The dynamic effects that limit the operation of the MOSFET at high frequencies and high switching speeds will be discussed in Chapter 7 for amplifier circuits, and in Chapter 13 for digital circuits.

Circuit Symbol

Figure 5.9(a) shows the circuit symbol for the n -channel enhancement-type MOSFET. The symbol is very descriptive: The vertical solid line denotes the gate electrode; the vertical broken line denotes the channel—the line is broken to indicate that the device is of the enhancement type whose channel does not exist without the application of an