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# PHILIPS TECHNICAL REVIEW

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MOS TRANSISTORS



## PHILIPS TECHNICAL REVIEW

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## Some problems of MOS technology

J. A. Appels, H. Kalter and E. Kooi

### Introduction

Scientists and engineers working in MOS transistor technology are charged with the production of MOS transistors and integrated circuits that possess certain specified characteristics, are stable in behaviour, and give high production yields. The specified requirements determine the various steps in the production process: from the design geometry to the choice and techniques of oxidation, etching, diffusion and other processes in the manufacture of a MOS transistor<sup>[1]</sup>. Some of the problems which this involves are described in this article; the structure and operation of the MOS transistor, which are dealt with elsewhere in this issue<sup>[2]</sup>, are assumed to be generally familiar to the reader.

A typical example of a quantity that is determined by design geometry and technological processes is the transconductance of the MOS transistor. In the article just noted<sup>[2]</sup> it is shown that the transconductance — and hence the current that the transistor can carry at the maximum permissible gate voltage — is proportional to

$$\beta = \mu C_{ox} w / l. \quad \dots \dots (1)$$

Here  $\mu$  is the mobility of the charge carriers in the channel,  $C_{ox}$  the capacitance of the gate per unit area,  $w$  is the width and  $l$  the length of the channel (fig. 1).

The mobility  $\mu$  depends on the semiconductor material of which the MOS transistor is made. For practical reasons this is almost invariably silicon. One of these reasons is that it is relatively simple to apply effective isolating layers to silicon by oxidation. Although impurity centres or defects may be present at the Si/SiO<sub>2</sub> interface, the nature and concentrations of these impurities can now be controlled, and they can in fact be used to alter the behaviour of a MOS transistor in a desired direction. Much of this article will be concerned with the Si/SiO<sub>2</sub> interface.

In the bulk of the silicon the mobility  $\mu$  may be regarded as a constant of the material. At the surface the mobility is usually appreciably lower than in the bulk. Not only may it be affected here by the impurities or defects, but it is also found that  $\mu$  decreases with increasing gate voltage, and therefore depends on the

magnitude of the charge induced in the channel. A theoretical analysis based on detailed physical considerations has shown that this is to be expected<sup>[3]</sup>.

It has also been found that the surface mobility is dependent on the crystal orientation at the surface. For electrons the mobility is greatest for the (100) plane of silicon; the surface mobility in this plane can even approach the value of  $\mu$  in the bulk. For the holes the

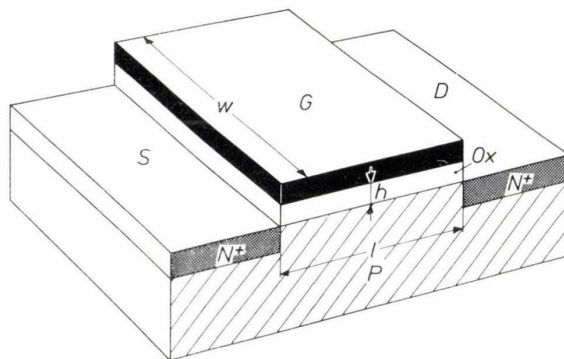


Fig. 1. Schematic diagram of a MOS transistor, made on a *P*-type silicon substrate. Two diffused zones of *N*<sup>+</sup> silicon constitute the source *S* and the drain *D*. Between them, isolated by an oxide layer *Ox*, is a metal control electrode, the gate *G*. If *G* is sufficiently positive, a concentration of free electrons occurs under the gate, forming an *N*-type conducting channel between source and drain. The length *l* and width *w* of the channel, and the thickness *h* of the oxide are the chief factors that determine the characteristics of the MOS transistor.

mobility is greatest for the (111) orientation, but hole mobility is substantially less than electron mobility. To achieve the maximum carrier mobility, and hence the maximum transconductance, the best choice is an *N*-channel transistor on a silicon chip whose surface is oriented in the (100) plane.

If a high value of  $\beta$  is desired it is also necessary to have a high  $C_{ox}$  (see equation 1), and for this purpose the oxide layer under the gate is made as thin as possible. The minimum thickness is mainly determined by

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[1] A description of the photo-etching and diffusion processes is given in: A. Schmitz, *Solid circuits*, Philips tech. Rev. **27**, 192-199, 1966.

[2] J. A. van Nielen, *Operation and d.c. behaviour of MOS transistors*; this issue, page 209.

[3] N. St. J. Murphy, F. Berz and I. Flinn, *Carrier mobility in MOS transistors*; this issue, page 237.

the breakdown field-strength (about  $10^3$  V/ $\mu$ m); practical values frequently lie between 0.05 and 0.25  $\mu$ m.

The dimensions of the silicon chips set an upper limit to the width  $w$  of the channel, and of course the chance of a defect increases with increasing  $w$ . A width of a few millimetres is fairly easy to achieve, and special techniques can be applied to give a channel with a width of a few centimetres [4].

The length  $l$  of the channel cannot be made very small without running the risk of "punch-through", i.e. a flow of current between source and drain outside the channel. The length  $l$  is usually a few microns, but special methods can be used to bring it down to about 1 micron. A very short channel is particularly important in MOS transistors for the UHF band [5].

In addition to the transconductance  $\beta$ , the parasitic capacitances play an important part in fast transistors. The most detrimental one is usually the feedback capacitance between drain and gate [6]. This capacitance depends on the amount of overlap between drain and gate: it can be reduced by bringing the gate into accurate register with the channel region. Various useful methods that we have developed for this will be discussed in this article.

The speed of integrated circuits made with MOS transistors is mainly limited by the parasitic capacitance between wiring and substrate. MOS transistors are therefore made with thick oxide layers under the wiring but with thin oxide layers at the active regions. This approach also tends to prevent the formation of parasitic MOS transistors; these can be formed when a voltage applied to a conductor induces a conducting channel in the substrate underneath the conductor. In the transition from the thick oxide to the thin oxide there has to be a step in the metallization; this has often proved to be a weak spot. We have therefore developed a process in which the thicker oxide is embedded deeper in the silicon substrate, so that any steps above the surface are smaller. This is known as the LOCOS process (local oxidation of silicon), and will also be described in this article.

First of all we shall take a closer look at the silicon/silicon-dioxide interface. The surface defects present there and the contact potential of the gate metal and the substrate doping all have an important effect on the threshold voltage, i.e. the minimum gate voltage needed to form a channel [2]. In fact these defects can have a much greater influence than the contact potential and substrate doping. They can change the threshold voltage by tens of volts, whereas the changes due to differences in contact potential between dissimilar metals and the variation of substrate doping that occurs in practice amount to only a few volts. The presence of mobile ions can result in a slow change

in the threshold voltage. Control of the threshold voltage and making sure that it is stable are the main factors that decide which technology should be followed.

### The silicon/silicon-dioxide interface

The theoretical treatment given here of the silicon/silicon-dioxide interface makes no pretence at being complete, but is a simple model that is nevertheless capable of explaining many experimental results, and one that has also been found useful for qualitatively predicting the behaviour of the Si/SiO<sub>2</sub> system from the processing conditions that were used when it was made. In this model we distinguish between defects of two kinds:

- Surface states — states that can exchange charge with the silicon, and which can be described in physical terms as quantum states with an energy level between the valence and conduction band;
- Oxide charge — fixed positive charges (ionized donors) near the interface and presumably in the oxide.

We shall now consider both types of defect in turn.

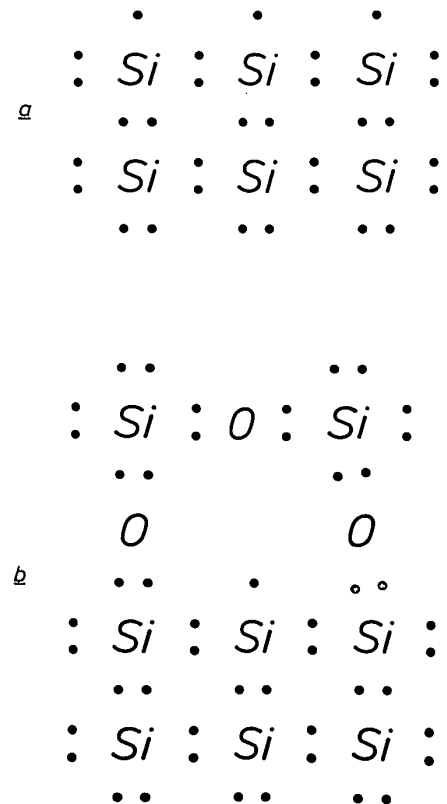


Fig. 2. *a*) Crystal lattice of silicon. At the surface of the crystal (top of the figure) each atom has an unpaired electron. *b*) Where the surface of the silicon crystal is covered with silicon dioxide, the lattices of the two substances do not exactly match. As a result silicon bonds remain unsaturated in places.

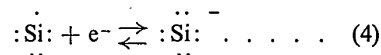


### Surface states

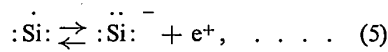
If the crystal lattice terminates abruptly at the surface of a silicon chip, then a large number of unsaturated silicon bonds are to be expected, i.e. each atom in the outside layer of silicon atoms should have an unpaired electron (fig. 2a). Since there are about  $10^{15}$  Si atoms per  $\text{cm}^2$  at the surface, one would expect about the same number of unsaturated bonds on a "clean" surface. If the silicon is oxidized, as it is in the case under consideration, then the number of unsaturated bonds is of course lower, but it is not equal to zero because there will probably not be an exact fit between the Si and  $\text{SiO}_2$  networks (fig. 2b). We shall now consider what electrical effects can result from the unsaturated silicon bonds.

It is very probable that it will take less energy to raise an unpaired electron into the conduction band than to raise a paired valence electron; in other words, the un-

bonds may act not only as electron donors or traps for holes, but also as traps for electrons, since trapping an electron changes a silicon atom with an unpaired electron into an atom with eight electrons in its outer shell. This is the inert-gas configuration:



The effect may also be seen as the giving-up of a hole:



and we may then conclude that the relevant energy level must lie in the forbidden band.

From a wide variety of measurements [7] it has been found that energy levels do in fact occur in the forbidden band, and that broadly two groups may be distinguished: a group near the conduction band

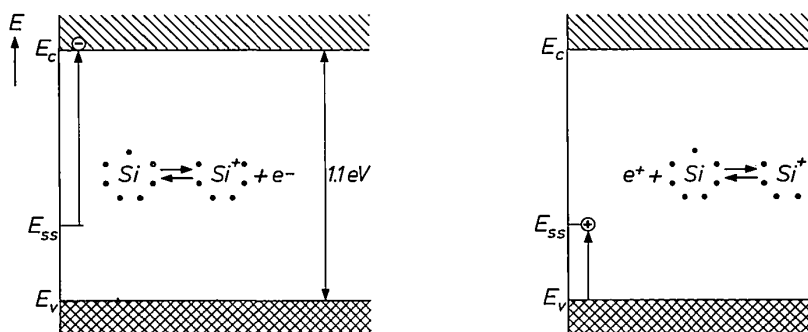
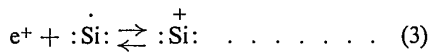
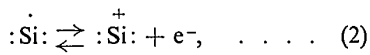


Fig. 3. The unpaired electron of a silicon atom with an unsaturated bond has an energy  $E_{ss}$  which lies in the forbidden band between valence band (energy  $E_v$ ) and conduction band (energy  $E_c$ ). The atom may occur as a donor; by giving up an electron (on the left) or taking up a hole (on the right) it then acquires a positive charge. If there is a high electron concentration the atom may also occur as an acceptor and acquire a negative charge.

paired electron possesses an energy level that lies in the forbidden band. A silicon atom to which such an electron is bound may give up this electron or take up a hole, but in both cases the atom itself becomes positively charged (fig. 3):



If we are dealing, for example, with *P*-type silicon, then there are many holes and the equilibria (2) and (3) shift to the right. If moreover the energy gap  $E_{ss} - E_v$  is small, a number of holes from the silicon may be trapped, and therefore the hole conduction near the surface of the crystal is not so good as in the bulk of the material.

It is also conceivable that the unsaturated silicon

— these are probably acceptor levels — and a group near the valence band — probably donor levels. Depending on the voltages applied in the measurements, there is a tendency for electrons or holes to concentrate at the Si/ $\text{SiO}_2$  interface; if there is a high electron concentration the defects act mainly as acceptor levels, but at a high hole concentration mainly as donor levels. On the same sample the number of acceptor levels found in one measurement is invariably almost equal

[4] R. D. Josephy, MOS transistors for power amplification in the HF band; this issue, page 251.

[5] R. J. Nienhuis, A MOS tetrode for the UHF band with a channel  $1.5 \mu\text{m}$  long; this issue, page 259.

[6] P. A. H. Hart and F. M. Klaassen, The MOS transistor as a small-signal amplifier; this issue, page 216.

[7] E. Kooi, The surface properties of oxidized silicon, Thesis, Eindhoven 1967.

M. V. Whelan, Influence of charge interactions on capacitance versus voltage curves in MOS structures, Philips Res. Repts. 20, 562-577, 1965; Electrical behaviour of defects at a thermally oxidized silicon surface, Thesis, Eindhoven 1970.

to the number of donor levels found in another measurement; this lends plausibility to our assumption that the same trapping centres are involved in both cases.

The assumption that the centres are related to unsaturated silicon bonds explains why the number of surface states depends on the crystal orientation of the silicon surface. If this is a (111) plane, then there are usually 3 to 5 times as many surface states as on a (100) plane. This suggests that the oxide network fits better on a (100) crystal plane than on a (111) plane. Other crystal orientations give various numbers of surface states that lie between those of the (100) and (111) planes.

The way in which the surface states can affect the characteristics of a MOS transistor will be demonstrated by means of a number of experimental transistors on a *P*-type silicon substrate, i.e. with an *N*-type channel. This channel would have to be induced by applying a positive voltage to the gate. Since the effect of this is a decrease in the concentration of holes near the silicon surface and an increase in the electron concentration, the equilibria (2) and (3) shift to the left and the equilibria (4) and (5) to the right. This means that the donor states tend to become neutral (if they were not neutral already) and the acceptor states negative. The build-up of negative charge in the surface states means that the mobile charge entering the bulk of the silicon is less than the total induced charge. Consequently the threshold voltage, required for inversion, is higher than expected, and on increasing the gate voltage the subsequent increase in the inversion charge (and hence in the current through the transistor) is lower, and the transconductance is therefore affected.

The effect of the surface states is illustrated in fig. 4, which shows the  $I_d$ - $V_{gs}$  curves for the experimental MOS transistors that all have the same dimensions but were annealed in different gas atmospheres after forming the gate oxide in an extremely dry atmosphere at about 1100 °C. During the anneal, the temperature was kept low (450 °C) compared with the normal growth temperature of SiO<sub>2</sub> on Si (1000 °C or higher), so that the processing steps could cause no difference in oxide thickness. They did, however, give rise to differences in the numbers of surface states, as may be shown from the threshold voltages and transconductances. In fact a hydrogen atmosphere and water vapour in an atmosphere of wet nitrogen even lead to negative threshold voltages and thus appear to remove the surface states for the most part. Water vapour in an oxygen atmosphere has considerably less effect. This suggests that a reduction of water to hydrogen plays an important part in the process. This hypothesis seems to be confirmed by the experience

that the treatment in wet nitrogen is most effective when the chip is heated to a high temperature in an inert gas immediately after the silicon is oxidized. This treatment reduces the oxygen content of the SiO<sub>2</sub> through the influence of the silicon beneath it.

The simplest explanation for the disappearance of the surface states is a chemical reaction of hydrogen with the centres involved, i.e. the formation of SiH groups in our model. This explanation has been confirmed by infra-red absorption measurements [8]. With the aid of a sensitive method of measurement it has been shown that the SiO<sub>2</sub> almost invariably contains a certain number of SiH groups, whose concentration is particularly high when the oxidized surface is subjected to operations which reduce the number of surface states.

Often very little water vapour is sufficient to reduce the number of surface states; a heat treatment in an inert gas (e.g. nitrogen or helium) which is not extremely dry (containing a few ppm of water) may be effective. It is also found that treatment in a fairly dry environment may also be highly effective if there is a base-metal electrode (e.g. of aluminium) on the silicon surface. Here again the surface states under the electrode disappear upon heating. It is assumed that in this case a reaction of the metal with traces of water produces sufficient hydrogen.

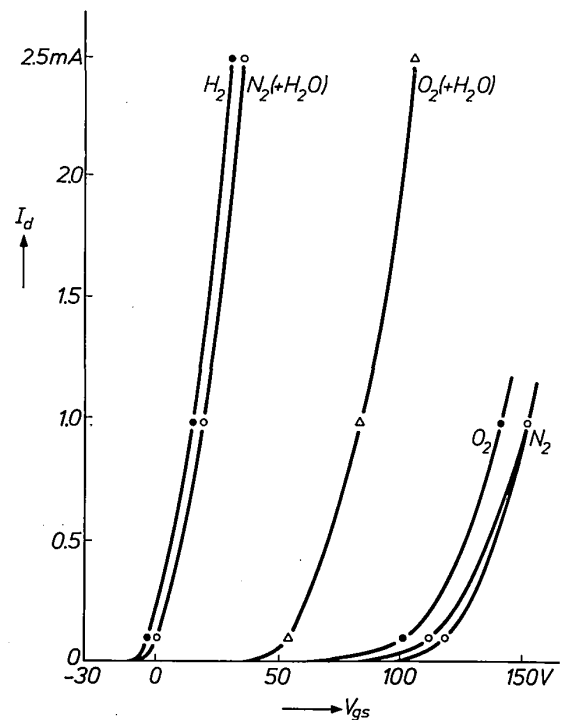


Fig. 4. The  $I_d$ - $V_{gs}$  characteristics of a number of geometrically identical MOS transistors which have been processed in different gas atmospheres after the chips had been oxidized.

We may therefore conclude that the structure of the interface is generally very dependent on the crystal orientation of the silicon, on the method of growing the oxide and on the subsequent treatments. Many experiments can be explained on the assumption that the silicon bonds are or are not saturated with hydrogen. We can be certain, however, that this does not give a complete description of the interface. A more exact theory would have to take into account, for example, the occurrence of SiOH groups and particularly the influence of other impurities (whether deliberately introduced or not) on the interface structure. We shall return to this in the next section.

#### Positive charge at the oxide/silicon interface

Anyone assuming that all the difficulties are resolved by a suitable after-treatment that reduces the number of surface states to a negligible value will be surprised by the result that, although the  $I_d-V_{gs}$  curve has approximately the theoretically expected shape after such a treatment, the threshold voltage often has a value less positive (or more negative) than was expected.

Indeed, the *N*-channel MOS transistors of fig. 4 have a negative threshold voltage after treatment in hydrogen or wet nitrogen; in other words, they already have an inversion channel when the gate voltage is zero. This effect cannot be explained in terms of the surface states, since they have the very effect of opposing the inversion.

We must therefore assume that there are other centres present in addition to the ones we have mentioned. It is usually supposed that the effect is caused by the presence of positively charged centres in the oxide immediately adjacent to the silicon surface, although these are difficult to distinguish experimentally from ionized donor centres in the silicon near the surface. The amount of oxide charge, like the number of surface states described above, is connected with the interface structure. Again, with identical processing, the oxidized (100) plane is found to give the lowest oxide charge, and the (111) plane the highest. Impurities have an important effect, particularly sodium. It has been clearly demonstrated<sup>[7]</sup> that the presence of sodium during oxidation can have a marked effect on the amount of charge, although the crystal orientation still remains important. It has been shown by neutron-activation analysis that the sodium has a distribution in the oxide like that illustrated in fig. 5. Most of the sodium can be seen to lie in the top layer of the oxide, but there is also an accumulation at the interface with the silicon. The position of sodium in the oxide structure may perhaps best be represented as in fig. 6a. This structure may be regarded as a somewhat reduced oxide structure, which is also to be expected on the silicon side of

the oxide layer. The sodium atom breaks the bond between an oxygen and a silicon atom, and itself forms a bond with the oxygen atom. As a result, one of the valence electrons of the silicon loses its bond, and as this electron is easily released, a positively charged centre is formed.

The sodium at the interface may conceivably be replaced by other alkali metals and even by hydrogen. This may perhaps explain why, even under fairly clean conditions, oxidation in steam gives rise to more oxide charge than oxidation in dry oxygen. On the other hand, it has also been observed that heating in hydro-

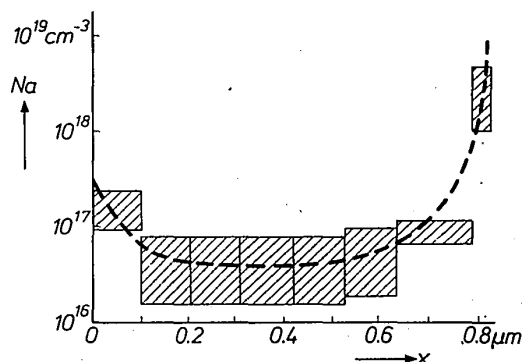


Fig. 5. Distribution of the concentration of Na atoms in the oxide as a function of the distance  $x$  from the silicon; the hatched area indicates the scatter of the measuring results.

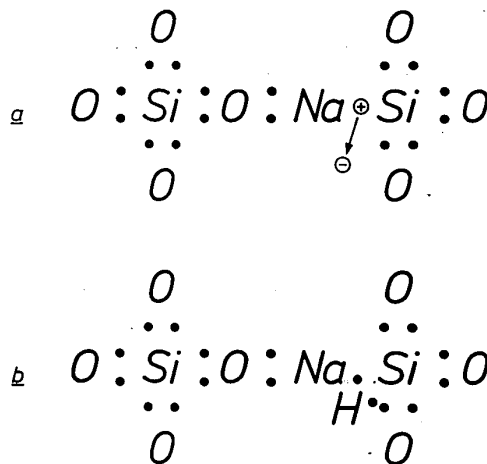


Fig. 6. a) The location of a sodium atom in  $\text{SiO}_2$ . The sodium atom breaks the bond between a silicon and an oxygen atom, and as a result one of the valence electrons of the silicon loses its bond; this electron is easily released and leaves behind a positive charge. b) A hydrogen atom can introduce an SiH group in  $\text{SiO}_2$ . In this group the hydrogen atom forms a homopolar bond with the silicon and there is no longer an unpaired electron.

[8] These measurements were carried out by Dr. K. H. Beckmann and T. Tempelmann of the Philips Hamburg laboratories; see K. H. Beckmann and N. J. Harrick, *J. Electrochem. Soc.* **118**, 614-619, 1971 (No. 4).



gen or in water vapour — particularly at less elevated temperature (600 °C) — may cause the charge to decrease. Here again, the formation of SiH may be expected, resulting for example in the structure illustrated in fig. 6b. The hydrogen atom now forms a homopolar bond with the silicon atom, and this no longer has an unpaired electron.

Fixed negative charge has sometimes been found. It can be caused by at least one impurity — gold, which is often present in small quantities. Gold is also readily made radioactive by neutron activation and its presence demonstrated in this way.

The presence of sodium and of other impurities may have a variety of causes. The impurities may come from the chemicals used or from the quartz glass tubes in which the oxidations are carried out. Another important source may be dust; if this settles on hot quartz tubes, sodium ions may easily enter the tube by diffusion and thus mix with the oxidizing gas. To achieve good process control it is therefore important to use pure chemicals and to protect the quartz tube from dust. Where extremely clean oxides are required, water-cooled quartz tubes may be used, and the silicon chip may then be heated by induction heating.

For the control of the oxide charge, cleanliness is not the only important consideration, and indeed it may not always be necessary; what is particularly important, as in the case of the surface states, is the gas atmosphere. An oxidizing atmosphere increases the oxide charge, especially when the temperature is relatively low (the effect is shown for example in fig. 4, where heating at 450 °C in oxygen does not in fact give a transistor of the depletion type — because there are so many surface states opposing inversion — but it does clearly alter the threshold voltage in the negative direction, by 15 volts). This effect of oxygen is not yet sufficiently understood. It is undoubtedly related to the oxidation mechanism: perhaps the oxygen at the upper surface attracts electrons which are then generated by structural change of the oxide/silicon interface. It is also conceivable that traces of impurities again play an important part: the transport of hydrogen from the interface towards the supplied oxygen is a likely possibility, which could cause the structure in fig. 6b to change for example to that in fig. 6a. In any case the significance for the technologist is that to obtain a low oxide charge he will have to end the oxidation in one way or another by tempering in a non-oxidizing gas.

Depending on the process used, the oxide charge is found to have a value ranging from less than  $10^{10}$  to more than  $10^{13}$  unit charges per  $\text{cm}^2$ . At an oxide thickness of say 0.2  $\mu\text{m}$ , this means a change in the threshold voltage with respect to the theoretical value ranging from less than 0.1 V to more than 100 V. Process control has now advanced to a stage where variation of the oxide charge with a tolerance of  $10^{10}$  charges per  $\text{cm}^2$  is quite feasible. One of the results of the presence of the positive oxide charge was that it was

originally very difficult to make *N*-channel MOS transistors that did not already have an inversion channel at zero gate voltage in the absence of surface states. This is the main reason why most MOS circuits have been (and still are) made with transistors of the *P*-channel type: here of course the presence of oxide charge only means that the threshold voltage is rather more negative, since *P*-channel transistors are always of the enhancement type.

#### Determination of oxide charge and surface states by measurement of the MOS capacitance

Information about the nature and number of the surface states can be obtained by a.c. circuit measurements that determine how the effective capacitance of the capacitor formed by gate, oxide layer and substrate depends on the applied d.c. voltage. A number of measurements have been made on MOS configurations specially designed for the purpose, with the metal contact on the oxide much greater than the gate of a transistor but small with respect to the dimensions of the silicon wafer, which was entirely covered on the other side by a metal substrate contact. These configurations might be referred to as MOS capacitors (fig. 7). The

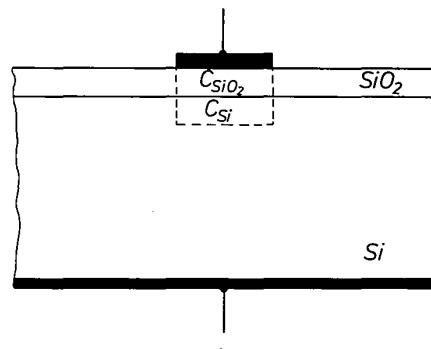


Fig. 7. MOS capacitor. The capacitance measured at the terminals is that of the series arrangement of  $C_{\text{SiO}_2}$  and  $C_{\text{Si}}$ . The magnitude of  $C_{\text{Si}}$  depends on the applied d.c. voltage.

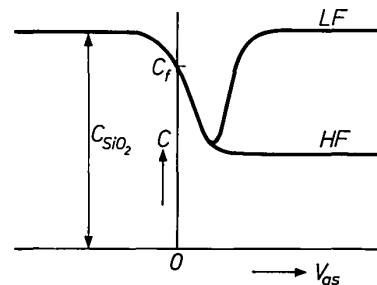


Fig. 8. Variation of the capacitance  $C$  of a MOS capacitor (on *P*-type silicon) with the applied d.c. voltage  $V_{\text{gs}}$  in the theoretical case where there are no surface states and no oxide charge. In this case the energy bands at  $V_{\text{gs}} = 0$  are not bent and the capacitance measured is the flat-band capacitance  $C_f$ . The MOS capacitor has a capacitance equal to  $C_{\text{SiO}_2}$  when the silicon directly beneath the oxide is a good conductor. This can be demonstrated quite clearly with low-frequency a.c. voltages (curve LF), but at higher frequencies the agreement is not so good (HF).

capacitance  $C$  measured at a particular frequency may be regarded as the resultant of the series configuration of a capacitance  $C_{SiO_2}$  across the oxide layer and a capacitance  $C_{Si}$ , which is related to the fact that the charge on the lower "plate" of the capacitor has the form of a space-charge cloud in the silicon. We may write:

$$\frac{1}{C} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{Si}}.$$

If  $C_{SiO_2} \gg C_{Si}$ , then  $C \approx C_{Si}$ ; if  $C_{Si} \gg C_{SiO_2}$ , then  $C \approx C_{SiO_2}$ . In these equations  $C_{SiO_2}$  is a constant, but  $C_{Si}$  depends on the thickness of the depletion layer, that is to say on the applied voltage and on the doping concentration of the silicon.

If there is no oxide charge and there are no surface states, we may expect the relation between  $C$  and  $V_{gs}$  in a MOS configuration on a  $P$ -type substrate to be represented by curves like those in fig. 8. This figure also applies to  $N$ -type material, provided the positive and negative  $V_{gs}$  scales are interchanged.

to about  $C_{SiO_2}$ , but at higher frequencies  $C$  remains small. This is because the supply and removal of charge carriers in the inverted layer of an MOS capacitor cannot take place fast enough at such high frequencies. In MOS transistors this effect is not so pronounced, the inverted layer here being connected with source and drain diffusion.

Two typical examples of the results of capacitance measurements can be seen in fig. 9a and b. These measurements were not made on MOS capacitors but on MOS transistors specially made for the purpose, since it was also required to measure the drain current  $I_d$ . This is also included in the figures. The transistors on which the measurements represented in fig. 9a and fig. 9b were carried out had the same shape and dimensions and were made on  $P$ -type substrates having the same conductivity ( $50 \Omega\text{cm}$ ). There was only a slight difference in the production process: after oxidation (16 hours at  $1200^\circ\text{C}$  in oxygen) and a phosphorus diffusion (4 hours at  $1150^\circ\text{C}$  in dry nitrogen) the transistor of

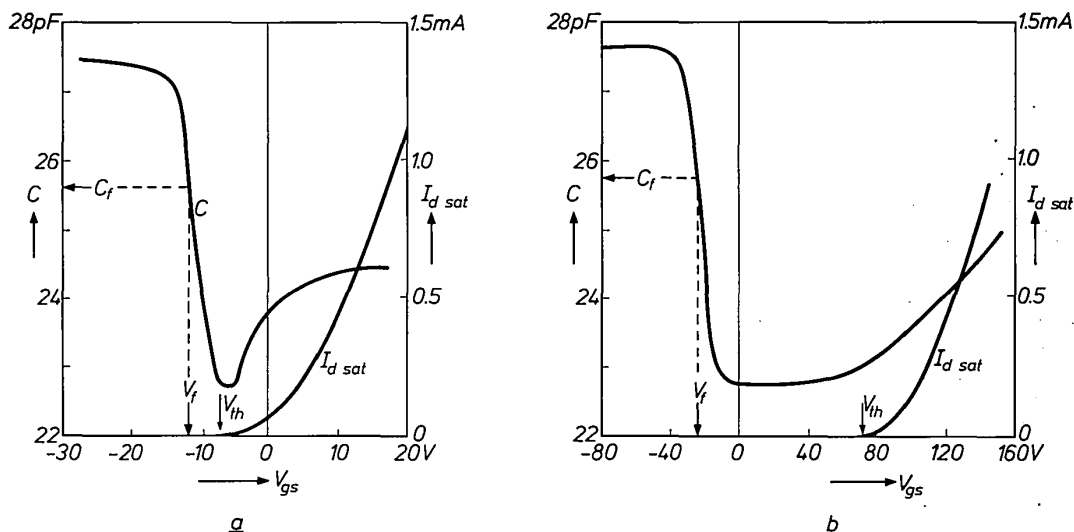


Fig. 9. Variation of the gate capacitance  $C$  with the d.c. voltage  $V_{gs}$  in an  $N$ -channel MOS transistor. a) After oxidation, the transistor was processed in wet nitrogen. From the calculated flat-band capacitance  $C_f$  it follows that the flat-band voltage  $V_f$  is  $-12$  V. The threshold voltage  $V_{th}$  of this transistor is  $-6$  V, as appears from the  $I_{d\text{ sat}}-V_{gs}$  characteristic. b) Here the transistor has not undergone treatment in wet nitrogen, and consequently surface states are present at the  $SiO_2/Si$  interface. The flat-band voltage  $V_f$  is  $-30$  V, the threshold voltage  $V_{th}$  is  $+80$  V.

The nature of the curves may be explained in qualitative terms as follows. In the case of a  $P$ -type substrate a negative charge on the measuring electrode of the MOS capacitor would increase the hole concentration at the surface. Charge variations caused by the a.c. signal used for measurement then occur so close to the interface that  $C_{Si}$  is relatively large and  $C$  is approximately equal to  $C_{SiO_2}$ . If the negative voltage on the electrode is allowed to approach zero, then these charge variations gradually occur less close to the interface and  $C_{Si}$  becomes smaller. As a result the measured capacitance is also lower. If  $V_{gs}$  is raised to positive values, this process continues until the threshold voltage is reached and inversion takes place at the surface.

The values of  $C$  found when  $V_{gs}$  is raised still further depend on the frequency at which the measurement is made. At low frequencies (below about 100 Hz)  $C$  increases with rising  $V_{gs}$  up

fig. 9a was subjected to heat treatment at  $450^\circ\text{C}$  for a further 30 minutes in wet nitrogen before the electrode metal was deposited.

The oxide layer was  $1.2 \mu\text{m}$  thick in both transistors, and for the substrate conductivity of  $50 \Omega\text{cm}$  the threshold voltage  $V_{th}$  should be  $+6$  V when all other effects are neglected. As can be seen in fig. 9a, the threshold voltage is  $-6$  V, i.e. 12 V lower. If the sum of the oxide charge and the charge present in the surface states at the threshold voltage is put at  $N_t$  elementary charges  $e$  per  $\text{cm}^2$ , we can calculate  $N_t$  from the expression:

$$N_t e = -C_{ox} \Delta V_{th},$$

where  $\Delta V_{th}$  is the change in  $V_{th}$  caused by the positive charge, i.e.  $-12$  V in the present case. We then arrive at  $N_t = 2 \times 10^{11}$  positive charges per  $\text{cm}^2$ .

From the shape of the curves of fig. 9a it can be shown that the positive charge in this transistor must be situated almost entirely in the oxide, and that the charge in the surface states is negligible in this case. Now let us return for a moment to fig. 8. This shows the variation of  $C$  with  $V_{gs}$  for the theoretical case in which there are no surface states and no oxide charges. In this case, for a gate voltage of  $V_{gs} = 0$  the energy bands in the energy-band diagram of the MOS transistor are not curved<sup>[2]</sup>, and  $C$  has a value  $C_f$  that can be calculated from the oxide thickness and the substrate doping. If oxide charges do exist, they cause band curvature at zero gate voltage, and a negative gate voltage  $V_t$  is then required to remove the band curvature and obtain the flat-band capacitance  $C_f$ . If we calculate this for a given transistor we can use the measured  $C$ - $V_{gs}$  curve to find the magnitude of  $V_t$  for that transistor. The voltage  $V_t$  is a measure of the oxide charge without the charge in the surface states, because it is measured when there is as yet no question of inversion and the associated electron trapping. In fig. 9a,  $V_t = -12$  V, which is therefore the same as  $\Delta V_{th}$ . It is apparent, that  $\Delta V_{th}$  is then entirely due to the oxide charge, and the surface states are negligible. The calculated number  $N_t = 2 \times 10^{11}/\text{cm}^2$  therefore consists entirely of oxide charge.

In fig. 9b we have a different case. Here the value of  $V_t$  is about  $-30$  V, and we see from the curve for  $I_d$  that  $V_{th}$  is about  $+80$  V. If we compare the measured  $C$ - $V_{gs}$  curve with the theoretical curve of fig. 8, we find that the fairly sharp minimum there has now become a broad region: the left-hand part of the curve has been displaced to the left (by 30 V) and the right-hand part to the right. The displacement to the left corresponds to  $V_t$  and is attributable to positive charge in the oxide, the displacement to the right must be due to the trapping of charge carriers, for the  $V_{gs}$  value at which  $C$  begins to increase coincides exactly with the value of the threshold voltage, as can be seen from the  $I_d$  curve.

### Stability of the threshold voltage

It is found in practice that the threshold voltage of a MOS transistor may drift in use. This instability of the threshold voltage may be the result not only of a change in the number of surface states but also of a change in the oxide charge; in practice the change in the oxide charge is usually the cause<sup>[9]</sup>.

A change can occur in the oxide layer through charge transport becoming possible in one way or another in the MOS system. There may for example be a transport of holes or electrons from the silicon to the oxide, where the carriers become trapped in defect centres. This effect is particularly noticeable at elevated temperatures ( $200^\circ\text{C}$  to  $300^\circ\text{C}$ ); it can be reduced to negligible proportions provided every effort is made to make a perfect interface structure (a (100) plane with a clean oxide and appropriate heat treatments).

A more serious effect is the transport of ions to the oxide. This occurs when the gate is positive with respect to the silicon. If no precautions are taken, this effect may be particularly marked at elevated temperature (e.g.  $100^\circ\text{C}$ - $300^\circ\text{C}$ ). The threshold voltage may change by many volts, and always in the negative direction. This points to the build-up of a positive oxide charge

near the interface. It is known that electric conduction in vitreous materials, such as  $\text{SiO}_2$ , is often due to alkali ions. Turning again to fig. 5, we see that there is a relatively large amount of sodium present in the oxide, particularly in the top layer. If all this sodium were to be driven towards the oxide/silicon interface when a positive voltage was applied, this would give rise to a concentration of about  $10^{13}$  positive elementary charges per  $\text{cm}^2$  (at an oxide thickness of  $0.2\ \mu\text{m}$  this would mean a change of 100 V in the threshold voltage). Such large changes are not generally found, however, and also the absence of any significant instability when the gate voltage is negative indicates that most of the sodium ions present in the oxide do not take part in the conduction. It is probable that reaction between the metal electrode and the oxide causes the release of ions at the oxide surface (not necessarily sodium ions alone), which then easily migrate through the oxide under the influence of the electric field.

This again demonstrates the need for clean conditions during oxide growth, but this alone is not sufficient. In the photo-etching techniques used after oxidation the oxide surface can again easily become contaminated, and contamination can also occur in the metallization stage. If all these operations are carried out with scrupulous care, MOS transistors can be made whose threshold voltage drifts by no more than a fraction of a volt when a field of  $100\ \text{V}/\mu\text{m}$  is applied, even at a temperature of  $300^\circ\text{C}$ . The chance of something going wrong is however so great that another solution is usually adopted, which is to cover the  $\text{SiO}_2$  layer with another dielectric that is far more difficult for the ions to penetrate.

### Other dielectrics

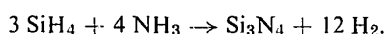
The main purpose of covering oxidized silicon with a second isolating layer is to prevent the migration of ions from the metal electrode into the oxide. A widely used procedure is to heat the oxidized silicon chip in a vapour of  $\text{P}_2\text{O}_5$ . This reacts with the  $\text{SiO}_2$ , whose top layer is converted into a vitreous mixed oxide (usual composition  $\text{SiO}_2 : \text{P}_2\text{O}_5 \approx 10 : 1$ ). This phosphate glass prevents the migration of sodium ions very effectively, so that up to about  $200^\circ\text{C}$  the instabilities can be kept to a fraction of a volt. On the other hand, it may itself introduce a slight instability, due to the occurrence of a polarization effect, which may cause some instability even at room temperature<sup>[10]</sup>. The magnitude of the effect depends on the composition and thickness of the phosphate glass in relation to the silicon dioxide beneath it. Given favourable ratios, the effect of the polarization can be restricted to a threshold voltage change of less than 0.1 V. It becomes more difficult when the oxide layers are very thin, because if



the phosphate glass is too thin (less than about 20 nm) there is a danger that the metal will react through the layer in places.

An interesting side effect of the application of phosphate glass is that at high temperature it absorbs impurities, such as sodium, from the  $\text{SiO}_2$ , which can be an advantage. A disadvantage of phosphate glass for thin layers is that the oxide charge is found to be a little higher after application of the layer, this resembles the effect found after heating in oxygen.

The best isolating layer known so far for blocking ion conduction is probably silicon nitride. This can be applied to the  $\text{SiO}_2$  layer by reacting silane or silicon chloride with ammonia at a temperature of 800 to 1000 °C:

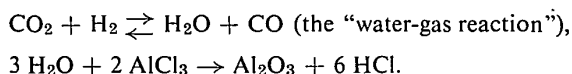


If the reaction is made to take place in a hydrogen atmosphere, the immediate result is a radical reduction of surface states on the silicon. Traces of impurities are very important in this process also and cleanliness in processing is therefore necessary to keep the oxide charge low.

Since silicon nitride gives such effective masking, a thin layer is sufficient (10 nm to 20 nm). A disadvantage of silicon nitride is that there can be a small amount of electron conduction in it, which can give rise to slow instability effects (drift due to charge build-up at the nitride/oxide interface). The effect is more pronounced at high field strengths. To minimize the effect it is necessary to make the nitride much thinner than the oxide underneath it.

The effect can also be utilized to bring about a change in the threshold voltage: it then constitutes a storage effect<sup>[11]</sup>, which can be made to last for days or weeks. The nitride should then be thick compared with the oxide. When the oxide is very thin (a few nanometres) charge can also be transferred from the silicon to the centres at the nitride/oxide interface by the tunnelling of carriers. This is also most effective at high field strengths: the momentary application of a high gate voltage (e.g. about  $10^3 \text{ V}/\mu\text{m}$  for 1  $\mu\text{s}$ ) causes a change in the threshold voltage that is maintained for a long time.

Aluminium oxide ( $\text{Al}_2\text{O}_3$ ) is another good insulator which effectively blocks alkali ions. It is made at about 900 °C from  $\text{AlCl}_3$  and  $\text{CO}_2$  in a hydrogen atmosphere by the reaction:



Since the atmosphere is again hydrogen, the result is an  $\text{SiO}_2$  interface with very few surface states. It has been reported that the application of the  $\text{Al}_2\text{O}_3$  layer causes a change of about 1.5 volts in the positive direction in the threshold voltage<sup>[12]</sup>. This is an interesting

effect because it can be used in certain cases to counteract the unwanted effect of positive oxide charge.

To learn more about this effect we measured the flat-band voltage  $V_f$  in a MOS capacitor, by the method described on page 232. The insulation of the measuring electrode consisted of a coating of  $\text{Al}_2\text{O}_3$  on a layer of  $\text{SiO}_2$ . The measuring electrode itself was a globule of mercury. After every measurement a thin layer of the insulating double layer was etched away and the measurement repeated. In this way we hoped to establish the distribution of the oxide charges over the thickness of the oxide. The results of the measurements are shown in fig. 10, in which the measured flat-band voltage  $V_f$  is plotted as a function of the oxide thickness  $h_{ox}$ . The flat sections of the curve indicate that there is no oxide charge present there (or at least less than  $10^{10}$  charges per  $\text{cm}^2$ ). The potential jump in the transition region from  $\text{Al}_2\text{O}_3$  to  $\text{SiO}_2$  might be explained by assuming the presence of an electric double layer of positive charges in the  $\text{Al}_2\text{O}_3$  and

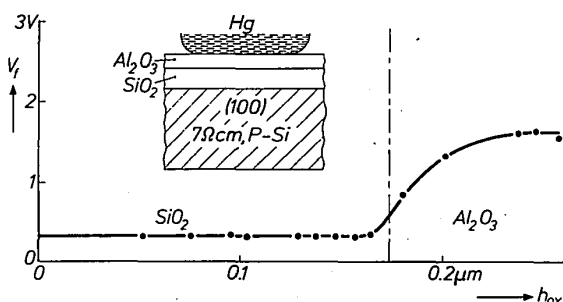


Fig. 10. The flat-band voltage  $V_f$ , measured for a MOS capacitor whose dielectric consisted of a layer of  $\text{Al}_2\text{O}_3$  on a layer of  $\text{SiO}_2$ . During the experiment thin layers of the dielectric were etched away; after each etching operation renewed contact was made with a mercury globule and the magnitude of  $V_f$  was measured. The potential jump may be due to an electric double-layer in the junction between  $\text{Al}_2\text{O}_3$  and  $\text{SiO}_2$ .

negative charges in the  $\text{SiO}_2$ . From measurements with other contact metals than mercury we found that the magnitude of the potential jump in fig. 10 depends on the metal used. To give a complete description of the metal/ $\text{Al}_2\text{O}_3$ / $\text{SiO}_2$ /Si system we must therefore take into account not only the charge at the junction between the  $\text{Al}_2\text{O}_3$  and the  $\text{SiO}_2$  but also an exchange of charge between the metal and the isolating layer. This exchange causes a change in the effective contact potential of the metal.

Besides those in the  $\text{Al}_2\text{O}_3$ / $\text{SiO}_2$  system, potential jumps were also found at the interfaces of various other combinations of  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , phosphate glass and  $\text{Al}_2\text{O}_3$ . The potential jump at the  $\text{Al}_2\text{O}_3$ / $\text{SiO}_2$  interface was found to be the best for obtaining the highest positive value of  $V_f$ .

[9] The sensitivity of the MOS transistor to ionizing radiation, which generates free electrons and holes in the oxide, is not dealt with here; see chapters 5 and 6 of the thesis by E. Kooi<sup>[7]</sup>.

[10] E. H. Snow and B. E. Deal, Polarization phenomena and other properties of phosphosilicate glass films on silicon, J. Electrochem. Soc. 113, 263-269, 1966.

[11] J. T. Wallmark and J. H. Scott, Switching and storage characteristics of MIS memory transistors, RCA Rev. 30, 335-365, 1969 (No. 2).

[12] H. E. Nigh, Some properties of vapour deposited aluminium oxide, Proc. Int. Conf. on the properties and use of M.I.S. structures, Grenoble 1969, pp. 77-87.

The use of  $\text{Si}_3\text{N}_4$  or  $\text{Al}_2\text{O}_3$  offers the additional advantage of a higher dielectric constant than that of  $\text{SiO}_2$  ( $\epsilon_{\text{Si}_3\text{N}_4} = 6.5$ ;  $\epsilon_{\text{Al}_2\text{O}_3} = 9.5$ ;  $\epsilon_{\text{SiO}_2} = 3.8$ ). One can profit from this, for example, by making the isolating layer somewhat thicker for the same value of capacitance, which increases the breakdown voltage. In practice, however, the  $\text{SiO}_2$  layer beneath the  $\text{Si}_3\text{N}_4$  or  $\text{Al}_2\text{O}_3$  is made relatively thick, in order to avoid the storage effects we mentioned earlier. The advantage of the dielectric constant is then minimal.

Silicon nitride and aluminium oxide are both difficult to etch with hydrofluoric acid, the etchant generally used in photo-etching techniques for  $\text{SiO}_2$  layers, and have to be etched with hot phosphoric acid. However, this attacks most photo-lacquers. To overcome the difficulty, a layer of  $\text{SiO}_2$  is grown (e.g. from  $\text{SiH}_4$ ,  $\text{CO}_2$  and  $\text{H}_2$ ) on the  $\text{Si}_3\text{N}_4$  or  $\text{Al}_2\text{O}_3$ , and a pattern is etched in this  $\text{SiO}_2$  by the usual etching techniques. The pattern serves as a mask during the etching of the  $\text{Si}_3\text{N}_4$  or  $\text{Al}_2\text{O}_3$  layer by hot phosphoric acid.

#### Parasitic inversion channels; the LOCOS technique

Even when all charge transport through the isolating layer is avoided, MOS transistors can still give very troublesome instability effects. This is the case when charge is able to leak from the gate across the insulator surface. The surrounding area then acquires the same potential as the gate, and an inversion channel may also appear beside the gate. The result is that the drain current  $I_d$  gradually increases. When the current in the MOS transistor is switched off by a change in the gate voltage, the parasitic channel remains for some time and therefore  $I_d$  does not immediately go to zero.

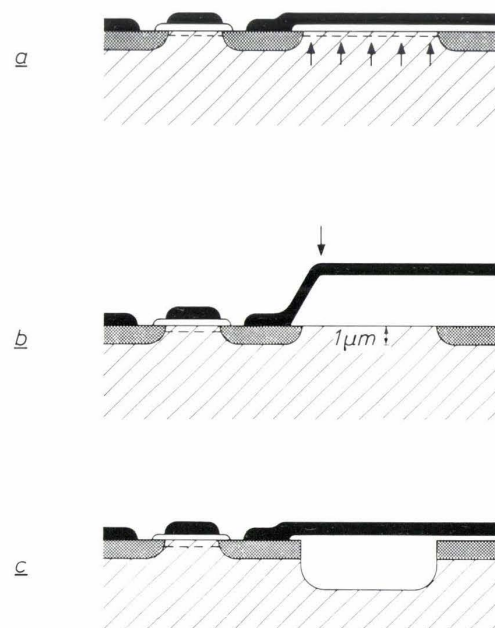
In discrete devices this unwanted effect can easily be avoided by making the transistors in such a way that the drain region is entirely surrounded by the source region and the channel region is entirely covered by the gate. In integrated circuits, however, this is an undesirable arrangement, because the various electrodes have to be interconnected to other elements across the isolating layer. Another consequence of this may be the occurrence of inversion channels under the wiring. The way in which such parasitic transistors may occur is illustrated in *fig. 11a*.

The remedy is to ensure that at those places where parasitic channels are likely to occur the threshold voltage is higher than the potential that can appear across the oxide. It may be sufficient for this purpose to apply a thick isolating layer in the region concerned. This has the additional advantage of keeping down the capacitance of the wiring to the silicon. An unduly thick layer, however, also has serious disadvantages. Shallow windows have to be etched in the thick layer, and at the edge of these the metallization must make a fairly large

step (*fig. 11b*). This has been found to be a weak spot in the metallization, which is detrimental to the yield and reliability.

We have developed a method which almost entirely overcomes this difficulty. The method is based on the local oxidation of a silicon surface masked with a layer of silicon nitride<sup>[13]</sup>. With this method, which we have called the LOCOS technique (local oxidation of silicon), structures can be made in the way shown in *fig. 11*. It also offers advantages for other MOS circuits.

The way in which the sunken layer of oxide is produced is shown in *fig. 12*. A silicon-nitride mask of the appropriate pattern is applied to the silicon (*fig. 12a, b, c*). Silicon is etched away from the parts not covered to a depth of about  $1\text{ }\mu\text{m}$  (*fig. 12d*). Oxidation is now



*Fig. 11. a)* In an integrated circuit with MOS transistors a parasitic inversion channel may form under the wiring (see arrows). *b)* To prevent this, the oxide beneath the wiring is generally made thick. The step which the metallization then has to make to the silicon surface forms a weak spot. *c)* By using the LOCOS technique with local oxidation the thick oxide (e.g.  $2\text{ }\mu\text{m}$ ) can be partly buried in the silicon, thus eliminating the large step in the metallization.

carried out until the recesses are completely filled with  $\text{SiO}_2$ . The oxide growth takes place at the expense of the silicon beneath it and the oxide layer formed is almost  $2\text{ }\mu\text{m}$  thick (*fig. 12e*). Oxidation of the silicon nitride during this process is very slight, and the silicon nitride can be removed by etching in hot phosphoric acid (*fig. 12f*). The MOS transistors can now be made in the silicon islands formed on the surface.

Another method of avoiding parasitic inversion channels, or of at least splitting them up, is to increase the  $N$ -type or  $P$ -type doping of the substrate in the vulnerable zones. This has the effect of locally increasing the threshold voltage<sup>[2]</sup> [14]. The method is also used in combination with thick oxide in cases where the latter still offers insufficient protection.

We have already seen that the presence of surface states tends to prevent inversion (page 228). The parasitic channels might therefore also be avoided by incorporating a sufficient number of surface states at these places. This must be done locally, however, otherwise they would cause trouble in the MOS transistors. We have devised a simple method of doing this. Here again, use is made of the effective masking action of silicon nitride, although in a quite different way. The oxide is then covered with the nitride at the places where there is a risk of parasitic channels forming. A high-temperature heat treatment follows, which causes a large number of surface states to be formed because of the out-diffusion of hydrogen. In a second stage the surface states under the oxide can be removed by means of a treatment with water vapour, while those under the nitride/oxide system are maintained.

#### Parasitic capacitances

We have already mentioned the parasitic capacitances due to the wiring. The LOCOS technique provides a very effective means of reducing these.

In the MOS transistor a parasitic capacitance is often formed by the overlap of the gate metal across the drain region, setting a limit to the speed of the transistor. Fig. 13 shows a number of methods that can be used for minimizing this capacitance.

For comparison, fig. 13a illustrates a conventional method for making an  $N$ -channel MOS transistor. After the  $N^+$  diffusions the gate isolation is applied, and the metallization is then brought into register by means of photoetching techniques. An overlap of a few microns is difficult to avoid.

In fig. 13b the metal electrode is applied before the  $N^+$  regions are made. These can be made either by diffusion or by ion implantation<sup>[15]</sup>, using the masking effect of the metal (polycrystalline silicon can also be used in this case).

Often a thick oxide layer is used to reduce parasitic capacitances. The structure shown in fig. 13c was obtained by covering the whole surface with a thick layer of oxide after the  $N^+$  diffusion. The thick oxide was then removed from the channel region and the thin gate isolation deposited in its place. The gate metal now lies partly on thick oxide, and the contribution of this part to the parasitic capacitance is therefore slight.

In fig. 13d the source and drain regions are diffused from a phosphorus-doped layer of silicon dioxide. During the diffusion a thin oxide film forms on the channel region<sup>[5]</sup>. Compared with fig. 13c, this has the

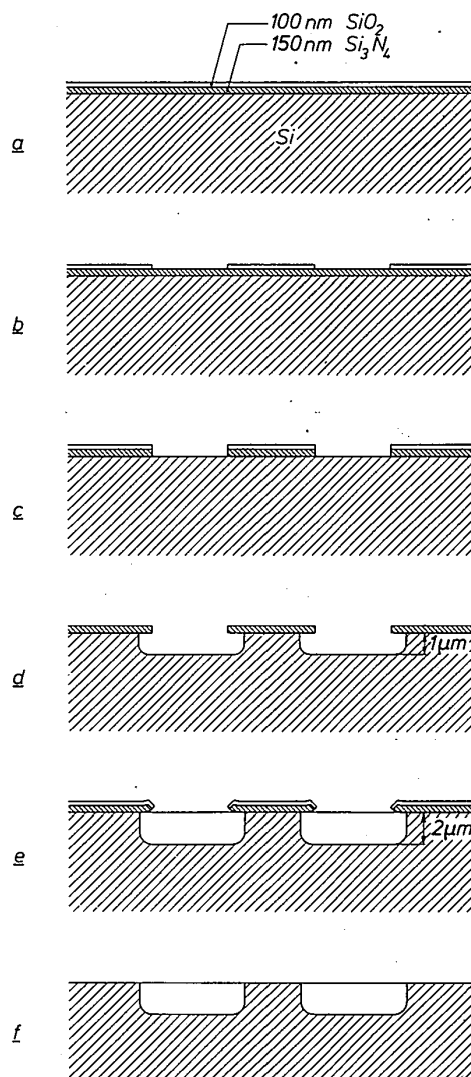


Fig. 12. The LOCOS technique.

a) A layer of silicon nitride and a layer of silicon dioxide are successively formed on the silicon.

b) A pattern of holes is etched in the  $\text{SiO}_2$  using the conventional photo-etching technique.

c) The pattern is etched into the  $\text{Si}_3\text{N}_4$  with hot phosphoric acid, the  $\text{SiO}_2$  serving as a mask.  $\text{SiO}_2$  masking is required because the photo-lacquers normally used for masking are attacked by hot phosphoric acid.

d) The silicon is etched away at the holes in the pattern to a depth of about  $1 \mu\text{m}$ .

e) The silicon in the  $1 \mu\text{m}$  deep holes is oxidized to a depth of about  $2 \mu\text{m}$ . The holes are completely filled with the  $\text{SiO}_2$  thus formed. The  $\text{Si}_3\text{N}_4$  is only superficially oxidized.

f) All  $\text{Si}_3\text{N}_4$  is etched away with hot phosphoric acid.

[13] J. A. Appels, E. Kooi, M. M. Paffen, J. J. H. Schatorjé and W. H. C. G. Verkuylen, Local oxidation of silicon and its application in semiconductor-device technology, Philips Res. Repts. 25, 118-132, 1970 (No. 2).

J. A. Appels and M. M. Paffen, Local oxidation of silicon; new technological aspects, *ibid.*, in press.

E. Kooi *et al.*, LOCOS devices, *ibid.*, in press.

[14] L. M. van der Steen, Digital integrated circuits with MOS transistors; this issue, page 277.

[15] J. M. Shannon, Ion-implanted high-frequency MOS transistors; this issue, page 267.



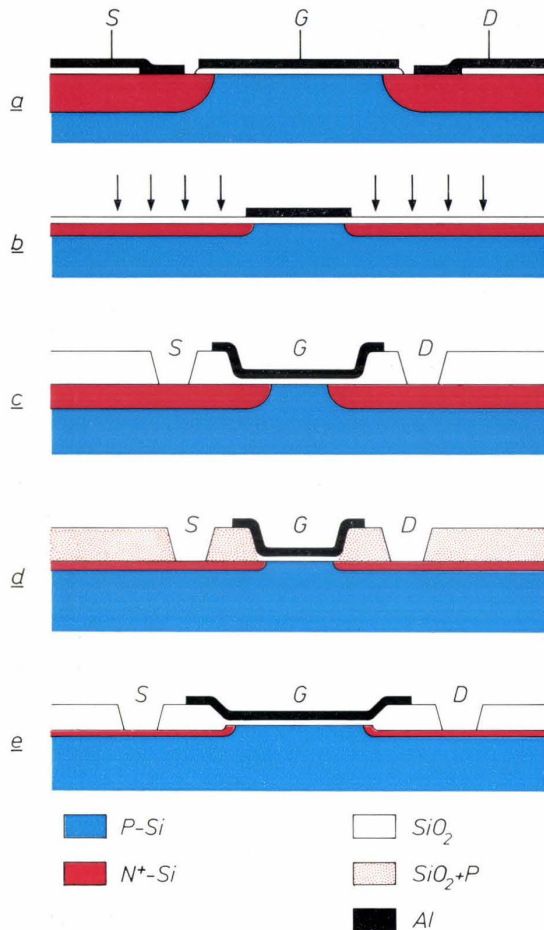


Fig. 13. *a*) Conventional MOS structure, in which the overlapping of the gate *G* causes fairly large parasitic capacitances to source *S* and drain *D*. *b*) to *e*) MOS structures with low parasitic capacitances. *b*) The overlap is small because the gate serves as a mask in the formation of the source and drain regions, formed by diffusion or ion implantation. *c*) Outside the channel region the gate lies on thick oxide. *d*) As *c*), but here the source and drain regions have been produced by diffusion from a doped oxide, so that their position in relation to the gate is more accurately determined. *e*) The thick oxide has been half buried in the silicon by the LOCOS technique. Exact control of the diffusion and oxidation processes gives diffusion regions that are only a fraction of a micron deep, thus minimizing the capacitance of the raised edges to the gate.

great advantage that it is not necessary to etch a hole at exactly the right place in thick oxide. The overlapping part of the metal electrode now lies almost entirely on thick oxide, and therefore makes very little contribution to the parasitic capacitance.

Fig. 13*e* illustrates how the LOCOS technique can be used with advantage here. After etching the channel-region pattern in the nitride layer, the diffusion of the source and drain regions is carried out, combined with oxidation, by briefly exposing the silicon chip to an atmosphere that contains the *N*-type dopant (arsenic or antimony) and then exposing it to an oxidizing atmosphere. During the oxidation process the *N*-type dopant diffuses further into the silicon. In the source and drain regions this results in a half-buried layer of oxide with a shallow *N*<sup>+</sup> diffused zone under it. Finally the nitride on the channel region is replaced by another insulator. Here again the overlapping part of the gate lies mainly on thick oxide, so that the parasitic capacitance to the drain remains small. The technique of diffusion and oxidation that we have described also helps to keep this capacitance small by limiting the diffusion depth to a fraction of a micron, which keeps the raised edges of the *N*<sup>+</sup> regions opposite the gate very narrow.

**Summary.** The threshold voltage of a MOS transistor depends critically on the surface states (silicon atoms with unsaturated bonds) at the Si/SiO<sub>2</sub> interface, and on positive charges in the SiO<sub>2</sub>. The number of surface states is reduced by treatment in a gas atmosphere that promotes the formation of SiH groups. The positive oxide charge is mainly connected with the presence of Na<sup>+</sup> ions in the oxide. The oxide charge can also be reduced by the same treatment. Sodium ions in the oxide can cause positive oxide charge.

Migration of alkali ions through the oxide can cause slow drift of the threshold voltage. To avoid this, a layer of phosphor-silicate glass, silicon nitride or aluminium oxide is applied to the silicon dioxide. The electric charge at the interface, particularly that of Al<sub>2</sub>O<sub>3</sub> and SiO<sub>2</sub>, is sometimes utilized for controlling the threshold voltage.

Thick oxide is used for keeping down parasitic capacitances and for preventing the formation of parasitic channels under the wiring of integrated MOS circuits. The LOCOS technique developed by the authors makes it possible to embed the thicker oxide in the silicon, thus avoiding the steps or ridges in the metallization, which have been found to be weak spots.