

UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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INTEL CORPORATION  
Petitioner

v.

GODO KAISHA IP BRIDGE 1  
Patent Owner

**PETITION FOR *INTER PARTES* REVIEW OF  
U.S. PATENT NO. 6,346,736**

**TABLE OF CONTENTS**

I.	Introduction.....	1
II.	Mandatory Notices.....	1
A.	Real Party-in-Interest .....	1
B.	Related Matters.....	1
C.	Counsel .....	2
III.	Payment of Fees Under 37 C.F.R. § 42.103 .....	2
IV.	Certification of Grounds for Standing .....	3
V.	Overview of Challenge and Relief Requested.....	3
A.	37 C.F.R. § 42.104(b)(1): Claims for Which IPR Is Requested .....	3
B.	37 C.F.R. § 42.104(b)(2): Grounds for Challenge .....	3
C.	37 C.F.R. § 42.104(b)(3): Claim Construction .....	6
D.	37 C.F.R. § 42.104(b)(4): How the Claims Are Unpatentable .....	6
E.	37 C.F.R. § 42.104(b)(5): Evidence Supporting Challenge.....	6
VI.	Brief Description of Technology .....	6
A.	Semiconductor Devices .....	6
B.	Isolation Methods .....	10
C.	Wiring-to-Substrate Capacitance .....	15
D.	Overview of the '736 Patent.....	25
1.	Summary of Alleged Invention of the '736 Patent .....	25
2.	Prosecution History .....	31
VII.	Level of Ordinary Skill in the Art.....	33
VIII.	Claim Construction .....	34
IX.	Overview of the Primary Prior Art References .....	34
A.	Overview of Admitted Prior Art .....	34
B.	Overview of Oshima .....	38
X.	Specific Grounds for Petition.....	40
A.	Ground 1: Claims 6-9, 11, 13, 14, 16, and 20 Are Obvious in View of APA and Oshima .....	40
1.	Independent Claims 6 and 13.....	41

Petition for *Inter Partes* Review of U.S. Patent No. 6,346,736

2. Dependent Claim 7.....	68
3. Dependent Claim 8.....	70
4. Dependent Claim 9.....	75
5. Dependent Claim 11.....	77
6. Dependent Claim 14.....	77
7. Dependent Claim 16.....	78
8. Dependent Claim 20.....	80
XI. Conclusion .....	81

## TABLE OF AUTHORITIES

	<b>Page(s)</b>
<b>Cases</b>	
<i>Berk-Tek LLC v. Belden Techs. Inc.</i> , IPR2013-00059, Paper 12 (PTAB May 2, 2013) .....	4
<i>Canon Inc. et al. v. Papst Licensing GmbH &amp; Co. KG</i> , IPR2016-01212, Paper 11 (PTAB Dec. 15, 2016) .....	4
<i>Chimei Innolux Corp. v. Semiconductor Energy Lab. Co.</i> , IPR2013-00038, Paper 9 (PTAB Mar. 21, 2013) .....	4
<i>Ford Motor Co. et al. v. Cruise Control Techs. LLC</i> , IPR2014-00281, Paper 55 (PTAB June 29, 2015) .....	4
<i>Ford Motor Co. v. Paice LLC et al.</i> , IPR2015-00790, Paper 13 (PTAB Nov. 9, 2015) .....	4
<i>Godo Kaisha IP Bridge 1 v. Intel Corporation</i> , Case No. 2:17-cv-00676 (E.D. Tex.) .....	1
<i>Intri-Plex Techs., Inc. et al. v. Saint-Gobain Performance Plastics Rencol Ltd.</i> , IPR2014-00309, Paper 83 (PTAB Mar. 24, 2014) .....	4, 5
<i>Invensense Inc. v. STMicroelectronics, Inc.</i> , IPR2013-00254, Paper 11 (PTAB Oct. 11, 2013) .....	4
<i>Kingbright Elecs. Co. et al. v. Cree, Inc.</i> , IPR2015-00743, Paper 8 (PTAB Sept. 9, 2015) .....	5
<i>LG Elecs, Inc. v. ATI Techs. ULC</i> , IPR2015-00325, Paper 62 (PTAB Apr. 14, 2016) .....	4
<i>Nichia Corp. v. Emcore Corp.</i> , IPR2012-00005, Paper 13 (PTAB Feb. 12, 2013) .....	4
<i>Omron Oilfield &amp; Marine, Inc. v. MD/TOTCO, A Division of VARCO, L.P.</i> , IPR2013-00265, Paper No. 11 (PTAB Oct. 31, 2013) .....	34

Petition for *Inter Partes* Review of U.S. Patent No. 6,346,736

<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005) .....	34
------------------------------------------------------------------------	----

<i>QSC Audio Prods., LLC v. Crest Audio, Inc.</i> , IPR2014-00131, Paper 41 (PTAB May 1, 2015) .....	4
---------------------------------------------------------------------------------------------------------	---

<i>In re Rambus Inc.</i> , 694 F.3d 42 (Fed. Cir. 2012) .....	34
------------------------------------------------------------------	----

<i>Toshiba Corp. et al. v. Gold Charm Ltd.</i> , IPR2015-01525, Paper 12 (PTAB Dec. 28, 2015) .....	4
--------------------------------------------------------------------------------------------------------	---

**Statutes**

35 U.S.C. § 102(e) .....	3
35 U.S.C. § 103(a) .....	5
35 U.S.C. § 311(b) .....	4, 5
35 U.S.C. § 315(e)(1).....	3

**Rules**

37 C.F.R. § 1.68 .....	6
37 C.F.R. § 42.10(b) .....	2
37 C.F.R. § 42.15(a)(1).....	2
37 C.F.R. § 42.103 .....	2
37 C.F.R. § 42.104 .....	3, 6

Intel Corporation (“Intel” or “Petitioner”) requests *inter partes* review (“IPR”) of claims 6-9, 11, 13, 14, 16, and 20 (“the Challenged Claims”) of U.S. Patent No. 6,346,736 (the “’736 patent”) (Ex. 1103).

## **I. INTRODUCTION**

The ’736 patent claims a semiconductor device that reduces so-called “wiring-to-substrate capacitance” by introducing certain structural elements between the wire and the substrate or within the substrate itself. Before the alleged invention, however, the wiring-to-substrate capacitance problem was well known, and, as explained in detail below, the solutions claimed in the ’736 patent would have been obvious to a person of ordinary skill in the art (“POSITA”) at the time of the alleged invention. The Challenged Claims should therefore be cancelled. Declaration of Dr. Bravman (“Bravman Decl.”) ¶ 26 (Ex. 1101).

## **II. MANDATORY NOTICES**

### **A. Real Party-in-Interest**

Intel is the real party-in-interest for the Petitioner.

### **B. Related Matters**

Godo Kaisha IP Bridge 1 (“IP Bridge”) has asserted the ’736 patent in *Godo Kaisha IP Bridge 1 v. Intel Corporation*, Case No. 2:17-cv-00676 (E.D. Tex.) (“Intel litigation”). This matter may affect, or be affected by, decisions in this proceeding.

**C. Counsel**

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Intel concurrently submits a Power of Attorney, 37 C.F.R. § 42.10(b), and consents to electronic service directed to the following email address:  
  
Intel\_IPBRIDGE\_IPR@kirkland.com

**III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.103**

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. § 42.15(a)(1) for this Petition to Deposit Account No. 506092. Review of nine (9) claims is requested, so no claim excess fee is paid. The undersigned further

authorizes payment for any additional fees that may be due in connection with this Petition to be charged to this deposit account.

#### **IV. CERTIFICATION OF GROUNDS FOR STANDING**

Intel certifies that the '736 patent is available for IPR and that Intel is not barred or estopped from requesting an IPR of the Challenged Claims on the grounds identified in this Petition. Intel certifies that: (1) Intel is not the owner of the '736 patent; (2) Intel (or any real party-in-interest) has not filed a civil action challenging the validity of any claim of the '736 patent; (3) Intel files this Petition within one year of the date it was served with a complaint asserting infringement of the '736 patent; (4) the estoppel provisions of 35 U.S.C. § 315(e)(1) do not prohibit this IPR; and (5) this Petition is filed after the '736 patent was granted.

#### **V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED**

##### **A. 37 C.F.R. § 42.104(b)(1): Claims for Which IPR Is Requested**

Petitioner challenges claims 6-9, 11, 13, 14, 16, and 20 of the '736 patent.

##### **B. 37 C.F.R. § 42.104(b)(2): Grounds for Challenge**

The Challenged Claims are unpatentable based on the following:

1. U.S. Patent No. 5,814,848 ("Oshima") (Ex. 1118); filed on May 31, 1996, issued on September 29, 1998, prior art under §102(e).

2. Admitted Prior Art ("APA") from the '736 patent (Ex. 1103). The Board has determined that "statements within the four corners of the challenged patent that constitute admissions may be considered '*prior art consisting of patents*'



for purposes of Section 311(b).” *See Intri-Plex Techs., Inc. et al. v. Saint-Gobain Performance Plastics Rencol Ltd.*, IPR2014-00309, Paper 83, \*at 21 n.8 (PTAB Mar. 24, 2014). There have been numerous decisions by the Board that instituted and/or found claims to be unpatentable based on admitted prior art in combination with other patents and/or printed publications. *See, e.g., Nichia Corp. v. Emcore Corp.*, IPR2012-00005, Paper 13, \*at 4 (PTAB Feb. 12, 2013); *Chimei Innolux Corp. v. Semiconductor Energy Lab. Co.*, IPR2013-00038, Paper 9, \*at 5 (PTAB Mar. 21, 2013); *Berk-Tek LLC v. Belden Techs. Inc.*, IPR2013-00059, Paper 12, \*at 4 (PTAB May 2, 2013); *Invensense Inc. v. STMicroelectronics, Inc.*, IPR2013-00254, Paper 11, \*at 2-3 (PTAB Oct. 11, 2013); *Ford Motor Co. et al. v. Cruise Control Techs. LLC*, IPR2014-00281, Paper 55, \*at 5 (PTAB June 29, 2015); *LG Elecs, Inc. v. ATI Techs. ULC*, IPR2015-00325, Paper 62, \*at 4 (PTAB Apr. 14, 2016); *QSC Audio Prods., LLC v. Crest Audio, Inc.*, IPR2014-00131, Paper 41, \*at 3 (PTAB May 1, 2015); *Ford Motor Co. v. Paice LLC et al.*, IPR2015-00790, Paper 13, \*at 5 (PTAB Nov. 9, 2015); *Toshiba Corp. et al. v. Gold Charm Ltd.*, IPR2015-01525, Paper 12, \*at 6 (PTAB Dec. 28, 2015); *Canon Inc. et al. v. Papst Licensing GmbH & Co. KG*, IPR2016-01212, Paper 11, \*at 7 (PTAB Dec. 15, 2016). As in *Intri-Plex*, the APA in the ’736 patent is wholly-contained within the four corners of the challenged patent, forms part of the ’736 patent, and is an admission that is considered prior art under Section 311(b). In *Intri-Plex*, the patentee labelled figures

as “Prior Art” and stated in the specification that the prior art figures showed “known” features and methods. *See Intri-Plex*, IPR2014-00309, Paper 83 at 19-20. In the ’736 patent, the patentee labelled FIGS. 19, 20(a)-20(g), 21(a), and 21(b) as “PRIOR ART,” and the ’736 patent describes these figures as showing conventional features or process steps. ’736 patent at 1:35-37 (“FIG. 19 shows an example of the *conventional* trench-isolated semiconductor device having the dummy island semiconductor portions.”),<sup>1</sup> 1:60-62 (“FIGS. 20(a) to 20(g) are cross-sectional views illustrating a process of manufacturing the *conventional* trench-isolated semiconductor device having an NMOS transistor.”) (Ex. 1103). Moreover, the APA in the ’736 patent is unlike (1) statements in a patent specification taken in combination with statements of experts and inventors in other proceedings, or (2) statements in a patent specification not identified as prior art, both of which the Board has held was not an allowable statutory basis on which to institute an IPR proceeding. *See Kingbright Elecs. Co. et al. v. Cree, Inc.*, IPR2015-00743, Paper 8, \*at 6-11 (PTAB Sept. 9, 2015). Petitioner therefore submits that the APA in the ’736 qualifies as a patent or printed publication and forms a sufficient basis for finding the claims of the ’736 unpatentable under 35 U.S.C. § 311(b).

Ground	Proposed Statutory Rejection
1	Claims 6-9, 11, 13, 14, 16, and 20 are obvious in view of the APA and Oshima under §103(a)

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<sup>1</sup> All emphases and annotations added unless otherwise noted.

**C. 37 C.F.R. § 42.104(b)(3): Claim Construction**

See Section VIII.

**D. 37 C.F.R. § 42.104(b)(4): How the Claims Are Unpatentable**

A detailed explanation of how the Challenged Claims are unpatentable is provided below in Section X.

**E. 37 C.F.R. § 42.104(b)(5): Evidence Supporting Challenge**

A list of exhibits is provided below. The relevance of this evidence and the specific portions supporting the challenge are provided below in Section X. Intel also submits the declaration of Dr. John Bravman, Ex. 1101, in support of this Petition under 37 C.F.R. § 1.68.

**VI. BRIEF DESCRIPTION OF TECHNOLOGY**

The '736 patent relates to “reducing the capacitance between the wiring and substrate of the semiconductor device.” '736 patent at 1:8-9 (Ex. 1103).

**A. Semiconductor Devices**

A semiconductor device is an electronic device that is designed to operate in accordance with certain properties of a semiconductor material<sup>2</sup>—most commonly silicon. An “integrated circuit” (or “IC”) is a group of electrical circuits formed together over a semiconducting base layer—or “substrate”—such as silicon.

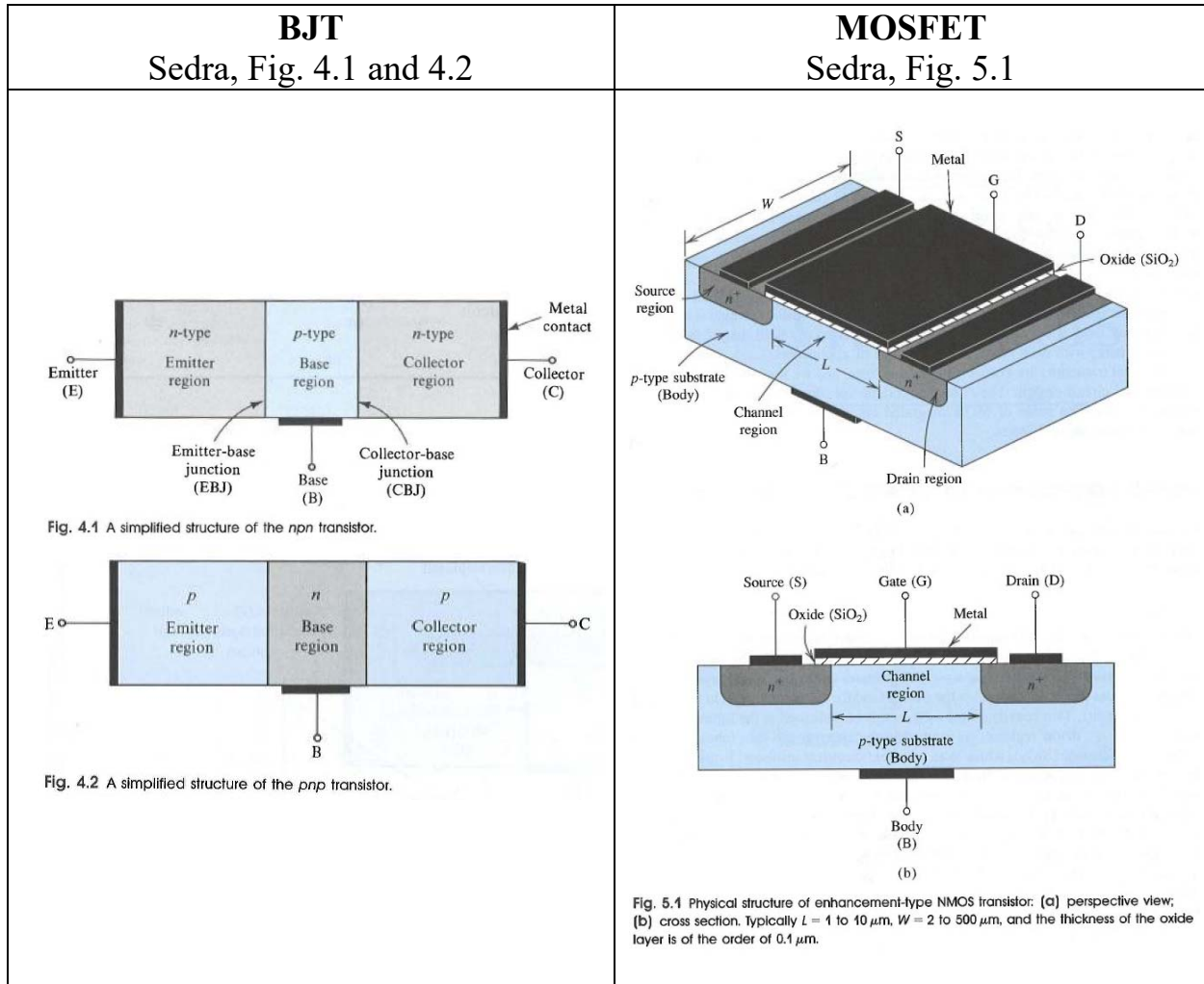
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<sup>2</sup> Semiconductor material has a conductivity somewhere between a conductor (high conductivity) and an insulator (no conductivity).

Modern integrated circuits typically include building-block components called transistors, which are fabricated in part by implanting charge-carrying ions—called “dopants”—into the semiconductor substrate to make certain regions more conductive. The dopants can be predominantly negative (“n-type”) or predominantly positive (“p-type”). The combination of these different implanted regions, along with other nearby structures, forms a transistor in the substrate. Bravman Decl. ¶¶ 28-29 (Ex. 1101).

There are different types of transistors. One well-known type is a metal oxide semiconductor field effect transistor (“MOSFET”). As illustrated below, MOSFETs use a “gate oxide film,” a “gate electrode,” and “source” and “drain” implanted regions on either side of the gate electrode. Another commonly utilized transistor is a bipolar junction transistor (“BJT”), which uses different oppositely doped regions in “npn” or “pnp” configurations. *See* Sedra, Adel S., Microelectronics Circuits, (3rd ed., 1991) (“Sedra”) at 11 (“As shown in Fig. 4.1, the BJT consists of three semiconductor regions: the emitter region (n type), the base region (p type), and the collector region (n type). Such a transistor is called an npn transistor. Another transistor, a dual of the npn as shown in Fig. 4.2, has a p-type emitter, an n-type base, and a p-type collector, and is appropriately called a pnp transistor.”), 14 (“Figure 5.1 shows the physical structure of the n-channel enhancement-type MOSFET . . . . At this point it should be clear that the name of the device (metal-oxide-semiconductor

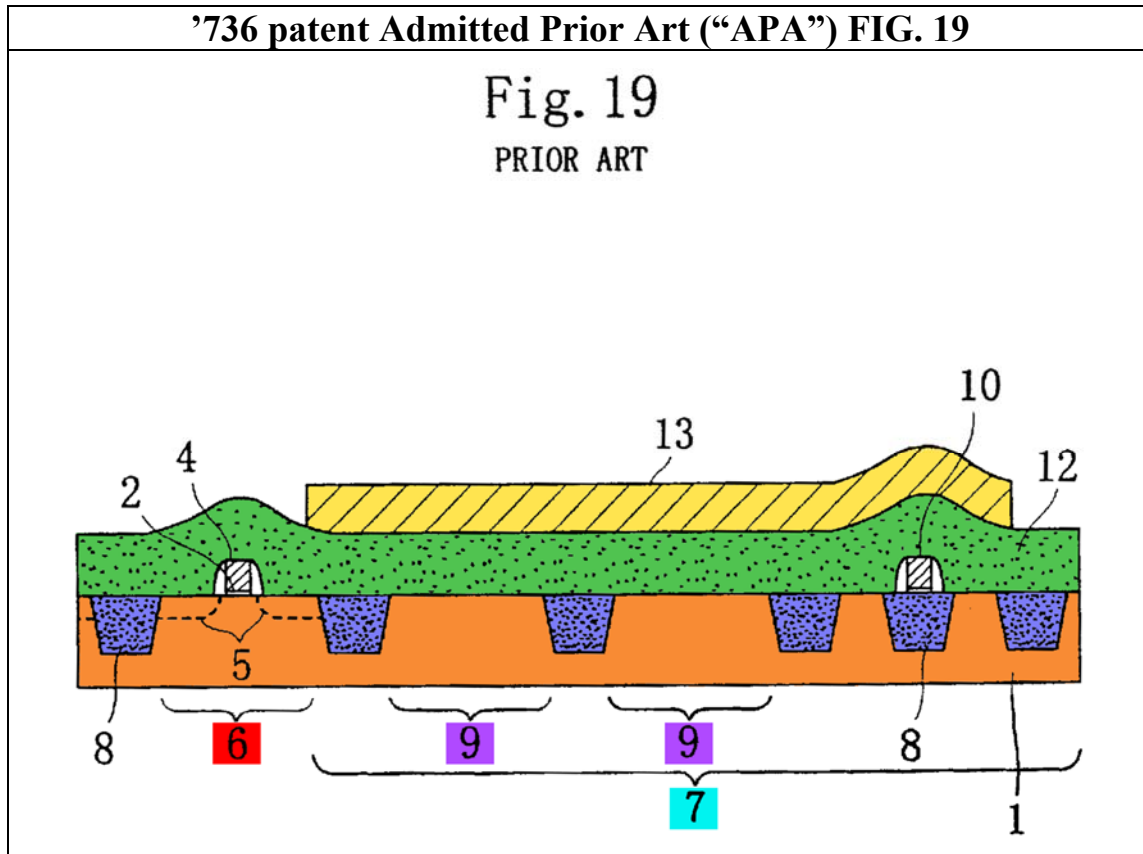
FET) is derived from its physical structure. The name, however, has become a general one . . . .”) (Ex. 1107). Bravman Decl. ¶¶ 30-31 (Ex. 1101).



Generally, a network of metal, electrically conductive pathways is formed above the semiconducting substrate to connect the various transistors together in a desired circuit configuration. These pathways function like wires and are typically called “interconnects.” Bravman Decl. ¶ 35 (Ex. 1101).

APA FIG. 19 of the '736 patent, reproduced below, shows an exemplary semiconductor device having a MOSFET and an **interconnect metal wire**. An

**active region 6** that includes a MOSFET transistor—having a gate oxide film 2, gate electrode 4, and source/drain regions 5—is formed in and over the **silicon substrate 1**. This **active region 6** is surrounded by an **isolation region 7** that contains several **trench portions 8** and **dummy semiconductor portions 9**. A non-conducting dielectric material (*i.e.*, “**interlayer insulating film 12**”) is formed above the entire **substrate** (*i.e.*, over the entire **active region 6** and **isolation region 7**) and metal interconnects (*i.e.*, “**metal wire 13**”) are formed thereon over the **isolation region 7**. Isolation regions electrically isolate active regions that include MOSFET transistors. *See* John Uyemura, *Fundamentals of MOS Digital Integrated Circuits* (Addison-Wesley Publishing Company 1988) (“Uyemura”) (Ex. 1110). Such isolation ensures proper circuit operation by preventing unwanted conduction paths between the active regions. *Id.* Bravman Decl. ¶¶ 32-34 (Ex. 1101).

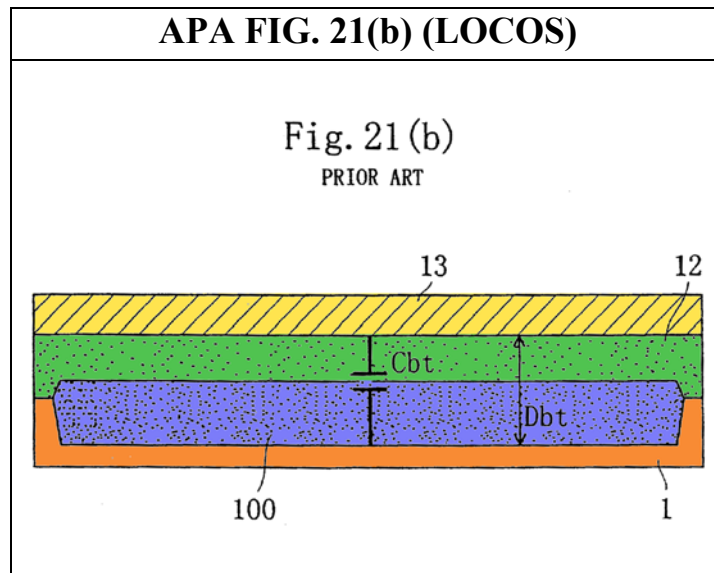


## B. Isolation Methods

With the rapid developments in semiconductor technologies over the past several decades, the industry was able to place a greater number of transistors into the same space on the semiconductor substrate. This phenomenon gave rise to Moore's Law. But as transistor density increased, it created an unwanted side effect of increased leakage current between different transistors. To counteract this effect, the semiconductor industry began electrically isolating transistors from each other. Bravman Decl. ¶¶ 36-37 (Ex. 1101).

LOCOS (local oxidation of silicon) was a popular method for isolating transistors that was developed in the 1970s. In devices that used LOCOS isolation,

a wide isolation oxide was grown in specified regions of the substrate to electrically separate transistors. The '736 patent illustrates a semiconductor with LOCOS isolation in APA FIG. 21(b), reproduced below. *See also* '736 patent at 2:59-62 (“FIG. 21(b) is a . . . semiconductor device having a LOCOS isolation film 100 . . .”) (Ex. 1103); Uyemura at 46-48 (Ex. 1110). Bravman Decl. ¶ 38 (Ex. 1101).

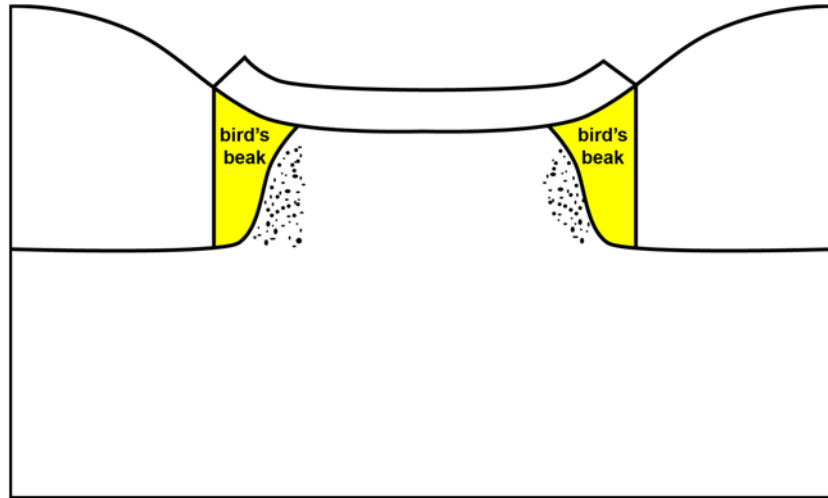


In FIG. 21(b), the LOCOS film 100 is grown in the substrate 1, and serves to isolate transistors on the left and right sides of it (not shown). The figure also shows wire 13 above interlayer insulating film 12. Bravman Decl. ¶ 39 (Ex. 1101).

But LOCOS isolation had drawbacks, including the so-called “bird’s beak” structural problem. Bird’s beaks grow during formation of the LOCOS structure and reduce the area available for the formation of the transistors. This problem was well-known at the time of the '736 patent (Uyemura at 46-48 (Ex. 1110); U.S. Patent No. 5,702,976 (“Schuegraf”) at 1:31-59 (Ex. 1113)) and is illustrated above as sloped



edges of LOCOS film 100 in APA FIG. 21(b), and in the figure below. Bravman Decl. ¶¶ 40-41 (Ex. 1101).



A second issue with LOCOS was the lack of planarity that resulted during photolithographic operations, in which layers of material are deposited on top of each other. *See, e.g.*, U.S. Patent No. 4,571,819 (“Rogers”) at 1:32-38 (Ex. 1112); Schuegraf at 1:55-59 (Ex. 1113). Bravman Decl. ¶ 42 (Ex. 1101).

A third issue with LOCOS (and with wide areas of oxide more generally) was that LOCOS films, when polished, suffered from “pattern dependence,” which, as the APA explains, “causes polishing properties to vary depending on the area of a region to be planarized.” ’736 patent at 1:28-29 (Ex. 1103). For example, over-polishing may result in the thinning of the wide oxide region—a phenomenon called “dishing.” Bravman Decl. ¶ 43 (Ex. 1101).

The shallow trench isolation (STI) method of isolating transistors was developed in the early-to-mid 1980s (U.S. Patent No. 4,519,128 (“Chesebro”) at

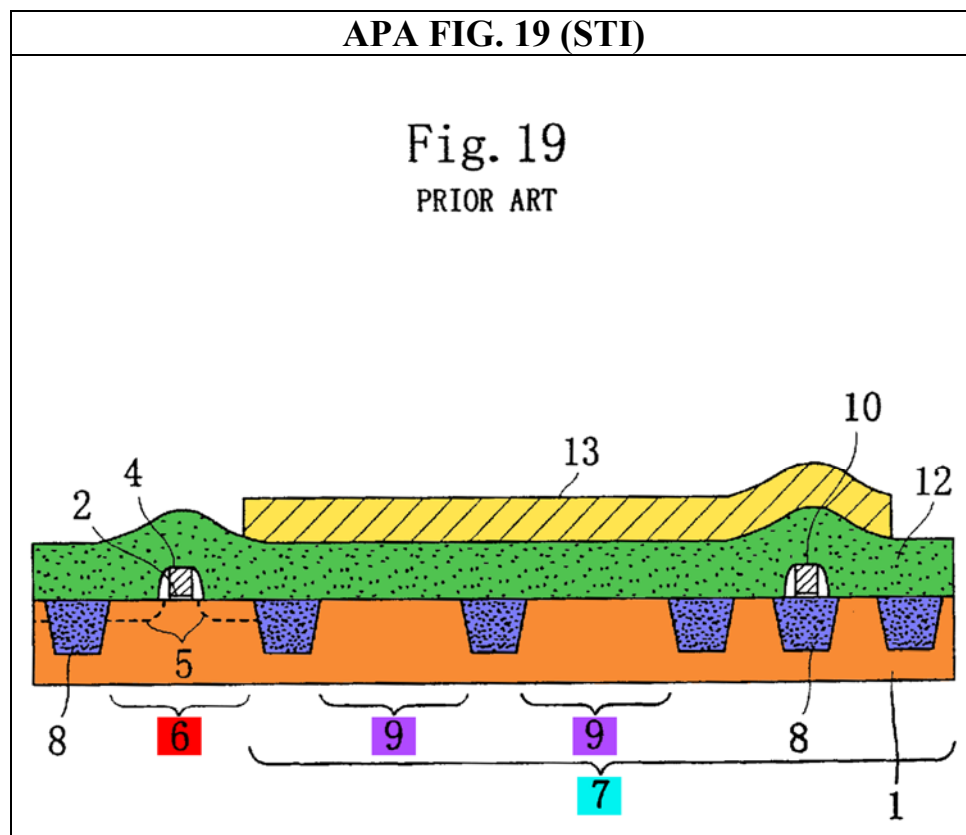
Abstract (Ex. 1111); Rogers at Abstract (Ex. 1112)) to address and improve upon the shortcomings of LOCOS.<sup>3</sup> In devices that use STI, shallow trenches are etched into the silicon substrate and filled with insulating material to isolate the transistors. Uyemura at 46-48 (Ex. 1110); Schuegraf at 1:60-2:24 (Ex. 1113). STI allows much greater transistor density than LOCOS does because it avoids the bird's beak problem and thus allows for smaller isolation regions. By the mid-1990s, market pressures to increase transistor density had incentivized the semiconductor industry to switch from LOCOS to the more-complex STI process. Bravman Decl. ¶¶ 44-46 (Ex. 1101).

STI also addressed the “planarity” and “pattern dependence” issues described above. With respect to the former, the surface of a substrate with STI trenches was relatively more planar owing to the use of CMP polishing as part of the STI trench formation process; with respect to the latter, because STI trenches were typically narrower than LOCOS regions, the surface of an STI trench would not deform when polished to the extent the surface of a LOCOS region would. Bravman Decl. ¶¶ 47-48 (Ex. 1101).

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<sup>3</sup> Isolation regions in both LOCOS and STI can also be called “field oxide.” See Uyemura at 48-52 (Ex. 1110).

The '736 patent acknowledges that STI was well known in the prior art, as illustrated below in APA FIG. 19, and the '736 patent even describes the industry shift from LOCOS to STI: “As higher-density and increasingly miniaturized semiconductor devices have been implemented in recent years, repeated attempts have been made to substitute a trench isolation [or STI] technique for a LOCOS technique...” '736 patent at 1:10-13; *see also id.* at 1:35-37 (“FIG. 19 shows an example of the **conventional** trench isolated semiconductor device . . .”) (Ex., 1101); Uyemura at 48-52 (Ex. 1110).



STI's increased manufacturing complexity compared to LOCOS was outweighed by the benefits of solving the bird's beak, planarity, and pattern

dependence problems, and the fact that LOCOS and STI were able to be used for the same purpose.<sup>4</sup> This drove the industry to widely adopt STI in the 1990s. Bravman Decl. ¶¶ 45, 49 (Ex. 1101).

### **C. Wiring-to-Substrate Capacitance**

As noted in the '736 patent, however, the STI method is not without its own drawbacks. The '736 patent's description of the APA notes that as STI allows miniaturization to occur, capacitance between the **interconnects** and the **substrate** increases, leading to undesirable reduction in the operating speed of the

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<sup>4</sup> Schuegraf at 2:20-22 ("Shallow Trench Isolation (STI) is used primarily for isolating devices of the same type and is often considered an alternative to LOCOS isolation") (Ex. 1113); U.S. Patent No. 4,957,590 ("Douglas") at 4:10-16 (Ex. 1114); U.S. Patent No. 5,976,939 ("Thompson") at 3:8-10 (Ex. 1115); U.S. Patent No. 6,165,826 ("Chau") at 5:56-67 (Ex. 1116); U.S. Patent No. 5,733,812 ("Ueda") at 22:49-52 (Ex. 1117).

semiconductor device.<sup>5</sup> See '736 patent at 3:1-29 (“Although the formation of the island pattern composed of the dummy semiconductor portions in the isolation region has the advantage of achieving planarization with excellent in-plane uniformity, it also has the possibility of increasing the **wiring-to-substrate** capacitance and resultantly reducing the operating speed of the semiconductor device.”) (Ex. 1103). The “**wiring-to-substrate** capacitance” refers to the physical phenomenon in which opposite charges accumulate on the wire and the substrate of

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<sup>5</sup> As Saraswat explains, “[a]s the minimum feature size is made smaller, the area of cross section of the interconnection also reduces. At the same time, a higher integration level allows the chip area to increase, causing the length of the interconnections to increase. The net effect of this ‘scaling of interconnections’ is reflected into an appreciable RC time delay. For a very large chip with extremely small geometries, the time delay associated with interconnections could become an appreciable portion of the total time delay, and hence the circuit performance could no longer be decided by the device performance.” Saraswat and Mohammadi, “Effect of scaling of interconnections on the time delay of VLSI circuits,” IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 2, April 1982 (“Saraswat”) at Introduction (Ex. 1106).

a semiconductor; this build-up of charge creates an electric field that can impede current flow in the wire. Bravman Decl. ¶¶ 50, 53 (Ex. 1101).

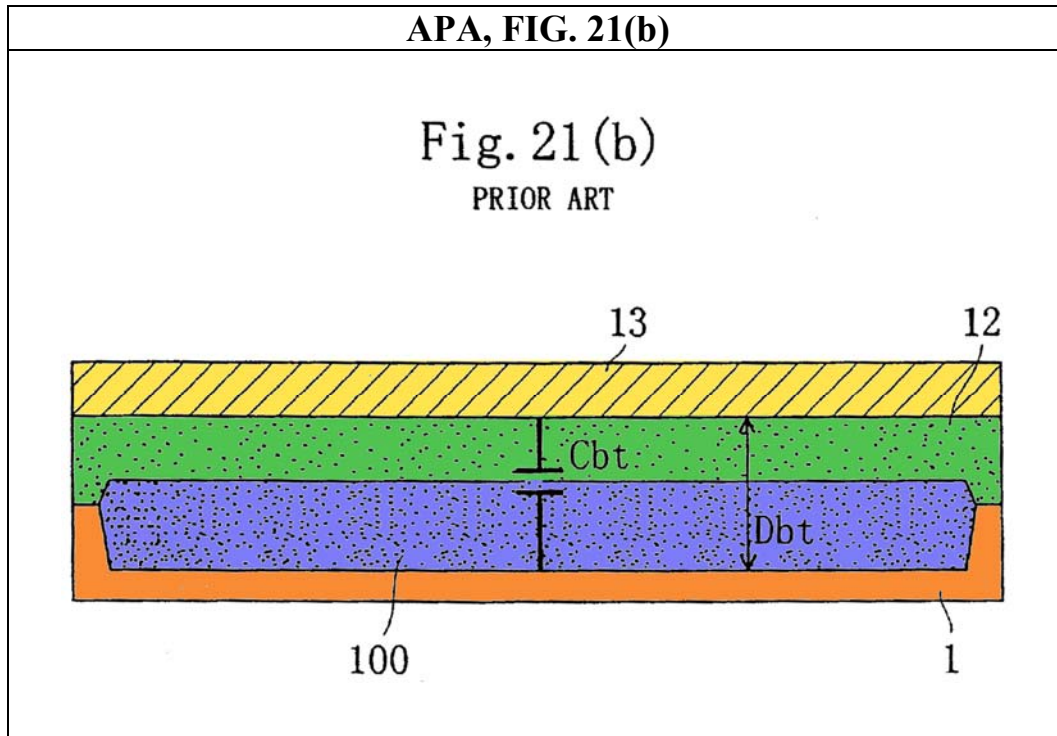
In fact, this “wiring-to-substrate capacitance” problem was well known long before the effective filing date of the ’736 patent. *See* U.S. Patent No. 5,107,320 (“Iranmanesh”) at 1:37-39 (“It is well known that device performance is impacted by the capacitance between the interconnect and the underlying substrate.”) (Ex. 1108); *see also* Oshima at 1:14-23 (“With the steady advance of the integration rate of semiconductor integrated circuits, the integrated circuits have become more and more microminiaturized . . . . As a result, the proportion of the wiring capacitance to the capacitance load of the respective circuit signals has increased.”) (Ex. 1118); U.S. Patent No. 4,960,725 (“Noguchi”) at 1:41-54 (“[I]t is considered that there are three different types of capacitance elements . . . . When the size of a transistor becomes smaller . . . the above mentioned capacitances (i) and (ii) are reduced. However, the capacitance (iii) [a capacitance between the substrate 1 and the conductive layer 10] tends to increase . . . .”) (Ex. 1121). Bravman Decl. ¶¶ 54-55 (Ex. 1101).

As shown in the ’736 patent’s description of the APA (*e.g.*, in FIG. 21(b)), the capacitance between the metal wire 13 and the substrate 1 with a LOCOS oxide film 100 is represented by the variable C<sub>bt</sub>. The APA models the metal wire 13

and the **substrate 1** as parallel conductive plates separated by a dielectric material<sup>6</sup> (*i.e.*, in which the dielectric material is the combination of interlayer insulating film 12 and LOCOS oxide film 100). *See* '736 patent at 3:7-12 (“In the case where a member interposed between the wiring and substrate is composed of a homogeneous material, the wiring-to-substrate capacitance per unit area is inversely proportional to the distance between the wiring and substrate, so that the capacitance is larger as the distance is shorter.”), 3:32-40 (Ex. 1103). In other words, the wire is treated as one plate, and the substrate is treated as a second plate a set distance away. As the distance between the plates increases, capacitance decreases (assuming all other factors remain the same). Bravman Decl. ¶¶ 51-52, 56 (Ex. 1101).

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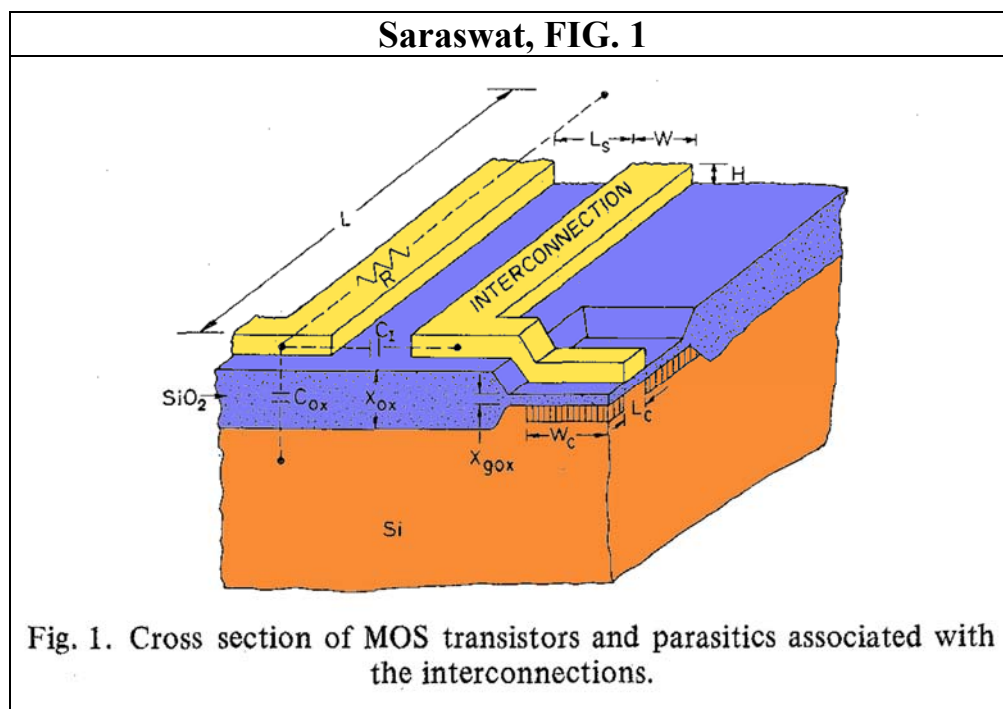
<sup>6</sup> A dielectric material is an electric insulator that, when placed in an electric field (such as exists between the plates of a capacitor), prevents charge from flowing through the material.



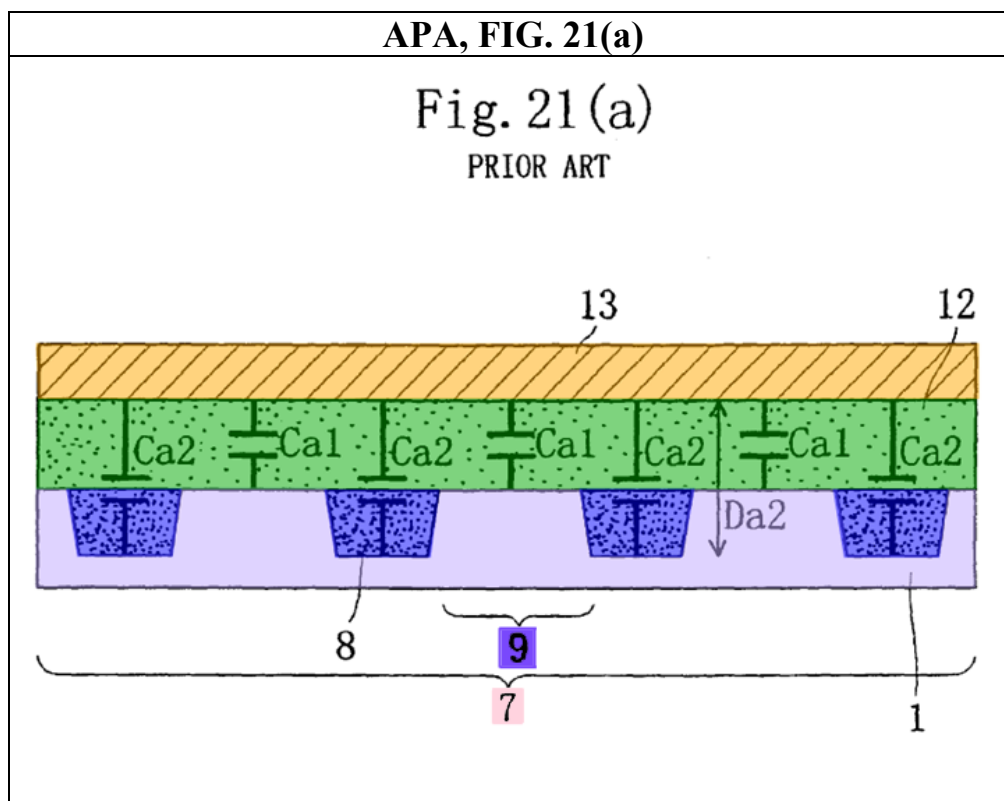
Engineers used this parallel-plate model to describe the capacitance of interconnects more than a decade before the alleged priority date of the '736 patent. *See* Saraswat at 4-5 (“interconnection line of length  $L$ , width  $W$  . . . . Assuming a ***parallel-plate capacitance model***, the capacitance between the **interconnection** and the **silicon**

**substrate** is given by  $C_{ox} = K_{ox} \epsilon_0 \frac{WL}{X_{ox}}$ , where  $X_{ox}$  and  $K_{ox}$  are the  $\text{SiO}_2$  thickness and dielectric constant, respectively, and  $\epsilon_0$  is the permittivity of free space.”) (Ex. 1106). Bravman Decl. ¶ 57 (Ex. 1101).

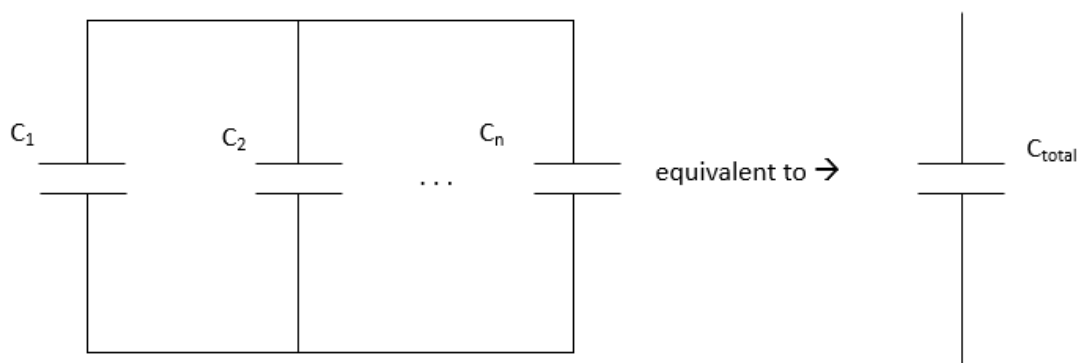




Notably, while the '736 patent models capacitance between wire and substrate in a LOCOS semiconductor device as a single, parallel-plate capacitor (as shown in FIG. 21(b) of the '736 patent), the '736 patent uses a different model for devices formed using STI. Specifically, when multiple trench portions are created in STI devices—as depicted in FIG. 21(a) below—the '736 patent models the total capacitance between wire and substrate as a set of parallel-plate capacitors connected “in parallel” to one another. Bravman Decl. ¶ 58 (Ex. 1101).

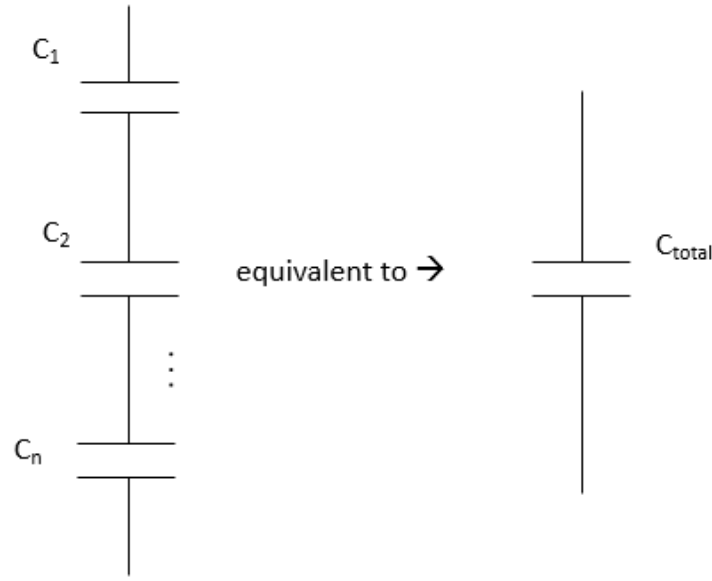


The cumulative behavior of capacitors connected “in series” and “in parallel” is described in introductory textbooks dealing with electronic circuits. For capacitors connected in parallel:



$$C_{total} = C_1 + C_2 + \cdots C_n$$

And for capacitors connected in series:



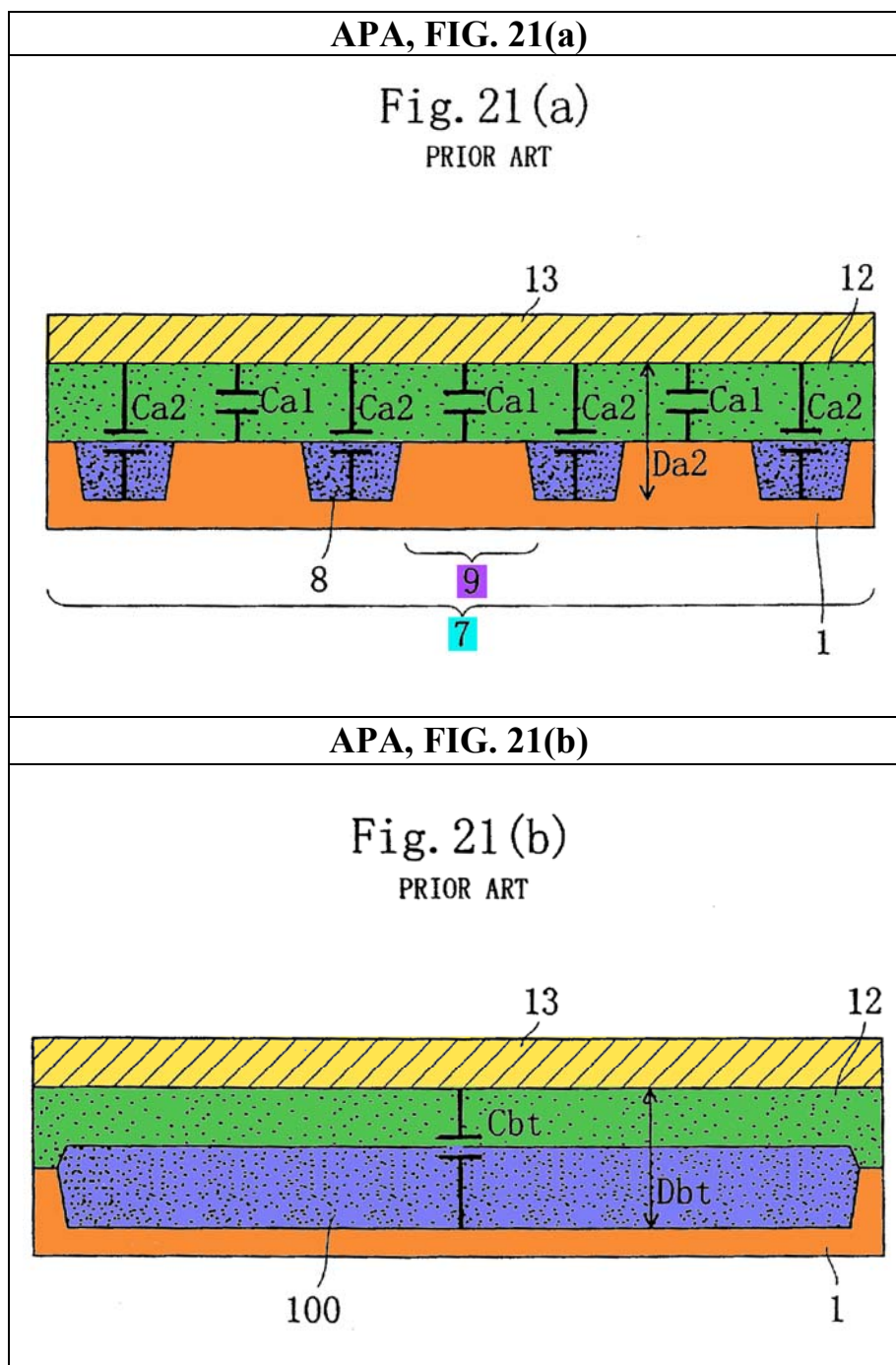
$$C_{total} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \dots \frac{1}{C_n}}$$

See Dorf and Tallarida, *Pocket Book of Electrical Engineering Formulas*, CRC Press (1993) at 9 (Ex. 1109). Thus, capacitors arranged in parallel tend to increase overall capacitance, whereas capacitors arranged in series tend to decrease overall capacitance. Bravman Decl. ¶¶ 58-59 (Ex. 1101).

The '736 patent APA describes the total capacitance of the STI device in FIG. 21(a)—assigned the variable  $Cat$ —as the sum of all the parallel capacitances between wire and substrate *without* an interposed STI (indicated with variable  $Ca1$ ) and between wire and substrate *with* an interposed STI (indicated with variable  $Ca2$ ):

$$Cat = \Sigma Ca1 + \Sigma Ca2$$

*See* '736 patent at 3:1-6 (Ex. 1103). If the distance  $Da2$  in FIG. 21(a) is equal to the distance  $Dbt$  in FIG. 21(b), the total capacitance in FIG. 21(a) (*i.e.*,  $Cat$ ) is larger than the capacitance in FIG. 21b (*i.e.*,  $Cbt$ ). *See* '736 patent at 3:13-23 ("If the total wiring-to-substrate of the semiconductor device shown in FIG. 21(b) is represented by  $Cbt$  when the dimension  $Da2$  shown in FIG. 21(a) is equal to the dimension  $Dbt$  shown in FIG. 21(b) . . . the wiring-to-substrate capacitance  $Cat$  in the structure shown in FIG. 21(a) is larger than the wiring-to-substrate capacitance  $Cbt$  in the structure shown in FIG. 21(b).") (Ex. 1103). This has the undesirable effect of "reducing the operating speed of the semiconductor device." '736 patent at 3:24-29 (Ex. 1103). Bravman Decl. ¶ 60-61 (Ex. 1101).



The '736 patent purports to solve the **wire-to-substrate** capacitance problem in STI semiconductor devices. As explained more fully below, however, the claim elements recited in the '736 patent were already well-known in the art, and a

POSITA would have been motivated to combine them to yield the claimed invention long before the effective filing date of the patent.

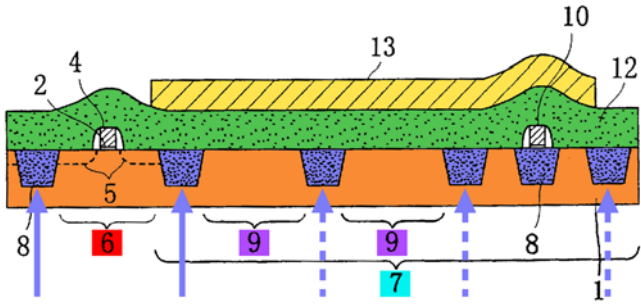
#### **D. Overview of the '736 Patent**

The '736 patent issued from U.S. App. No. 09/469,498, filed on December 22, 1999, which is a divisional of U.S. Patent No. 6,130,139, filed on November 25, 1997, which, in turn, claims priority to Japanese applications JP 09-023844, filed on February 6, 1997, and JP 08-314762, filed on November 26, 1996. The purported invention of the '736 patent is a “semiconductor device having lower total **wiring-to-substrate** capacitance and a higher operating speed.” '736 patent at Abstract (Ex. 1103).

##### 1. Summary of Alleged Invention of the '736 Patent

The '736 patent purports to reduce the **wiring-to-substrate** capacitance in a STI semiconductor device by treating the **metal wire 13** and the **substrate 1** as two parallel plates of a capacitor separated by a dielectric material (*i.e.*, interlayer insulating film 12) and then varying the properties of that material to control total capacitance. *See* '736 patent at 3:32-39 (Ex. 1103). In other words, the '736 patent relies on one of the most basic capacitance models in electronics and claims obvious, well-known variations of that model to yield predictable results. Bravman Decl. ¶¶ 62, 66 (Ex. 1101).

Challenged *independent claims 6 and 13* recites the limitations below, and all but the last of each are indisputably disclosed in the APA (*e.g.*, FIG. 19). Bravman Decl. ¶¶ 67-68 (Ex. 1101).

Independent claims 6 and 13	APA, FIG. 19
<p>A semiconductor device comprising:</p> <p>a semiconductor <b>substrate</b> having an <b>active region</b> and an <b>isolation region</b> surrounding said <b>active region</b>;</p> <p>a <b>first trench portion</b> [solid blue arrows] filled with an insulating material formed to separate said <b>active region</b> from said <b>isolation region</b>;</p> <p>a <b>second trench portion</b> [dotted blue arrows] filled with an insulating material formed to separate a plurality of <b>dummy semiconductor portions</b> in said <b>isolation region</b>;</p> <p>an <b>interlayer insulating film</b> formed to extend continuously over said <b>active region</b> and said <b>isolation region</b>;</p> <p>a <b>wire</b> formed on said <b>interlayer insulating film</b> covering said <b>dummy semiconductor portions</b> and said <b>second trench portion</b> in said <b>isolation region</b>; and</p> <p>[Claim 6 only] a <b>dielectric film</b> interposed between at least said <b>dummy semiconductor portions</b> of</p>	<p>Fig. 19 PRIOR ART</p>  <p>The diagram shows a cross-section of a semiconductor device. At the bottom is a substrate (1) with an active region (2) and isolation regions (3). A first trench portion (4) is filled with insulating material (5) to separate the active region from the isolation regions. A second trench portion (6) is filled with insulating material (7) to separate dummy semiconductor portions (8) in the isolation region. An interlayer insulating film (9) covers the active region and the isolation region. A wire (10) is formed on the interlayer insulating film, covering the dummy semiconductor portions and the second trench portion. A dielectric film (12) is interposed between the dummy semiconductor portions. Labels 1 through 13 identify various components and regions.</p>

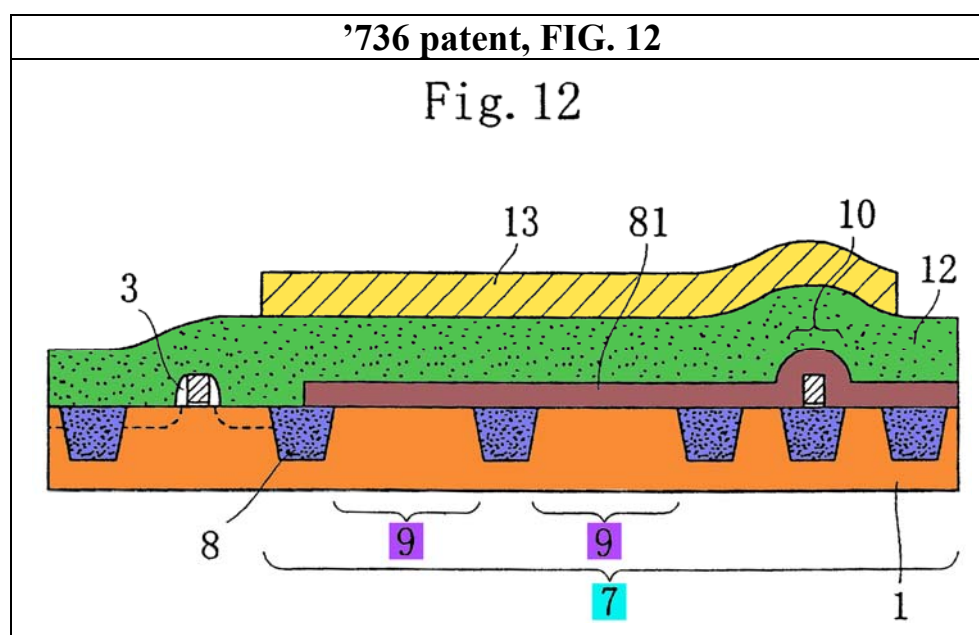
Independent claims 6 and 13	APA, FIG. 19
<p>said <b>isolation region</b> and said <b>interlayer insulating film</b>.</p> <p>[Claim 13 only] a <b>resistor film</b> formed under said <b>wire</b>, and between said <b>interlayer insulating film</b> and at least said <b>dummy semiconductor portions</b> of said <b>isolation region</b>.</p>	

The last limitations of each of the independent claims—which is the *only* purported novel part of each claim—are directed to structures that the patent says reduces the negative effects of increased wiring-to-substrate capacitance and increases operating speed for the semiconductor device. *See* ’736 patent at Abstract (“What results is a semiconductor device having lower total wiring-to-substrate capacitance and a higher operating speed.”); 3:32-48 (“the present invention has been achieved based on the principle that, if each electrode of a parallel-plate capacitor occupies an equal area, the capacitance of the capacitor is generally smaller as the distance between the electrodes is larger or on the physical phenomenon that, even when the capacitor has equal capacitance, the amount of charge accumulated therein is smaller as the voltage between the electrodes is lower. It is therefore an object of the present invention to increase the operating speed . . . [by] reducing the wiring-to-substrate capacitance in the isolation region or means for reducing the amount of charge accumulated in the capacitance present between the wiring and substrate in the isolation region.”) (Ex. 1103). As more fully summarized below,



claim 6 is directed to adding a dielectric film, and claim 13 is directed to providing a resistor film, both of which purportedly reduce the negative effects of increased wiring-to-substrate capacitance. Bravman Decl. ¶¶ 68-69 (Ex. 1101).

As shown in FIG. 12 below, a **dielectric film** is provided in accordance with claim 6. *See* '736 patent at 23:1-27 (Ex. 1103).



The '736 patent states that the insertion of this **dielectric film 81** increases the distance between the capacitor plates, which in turn decreases the capacitance value. More specifically, each of the Ca1 and Ca2 values decrease from the capacitance values shown in FIG. 21(a). *See* '736 patent at 24:34-43 (“the underlying film 81 . . . is present over the isolation region 7, so that the distance between the wiring and the substrate is longer than in the conventional semiconductor device shown in FIG. 19. Since the wiring-to-substrate capacitance decreases in inverse proportion to the

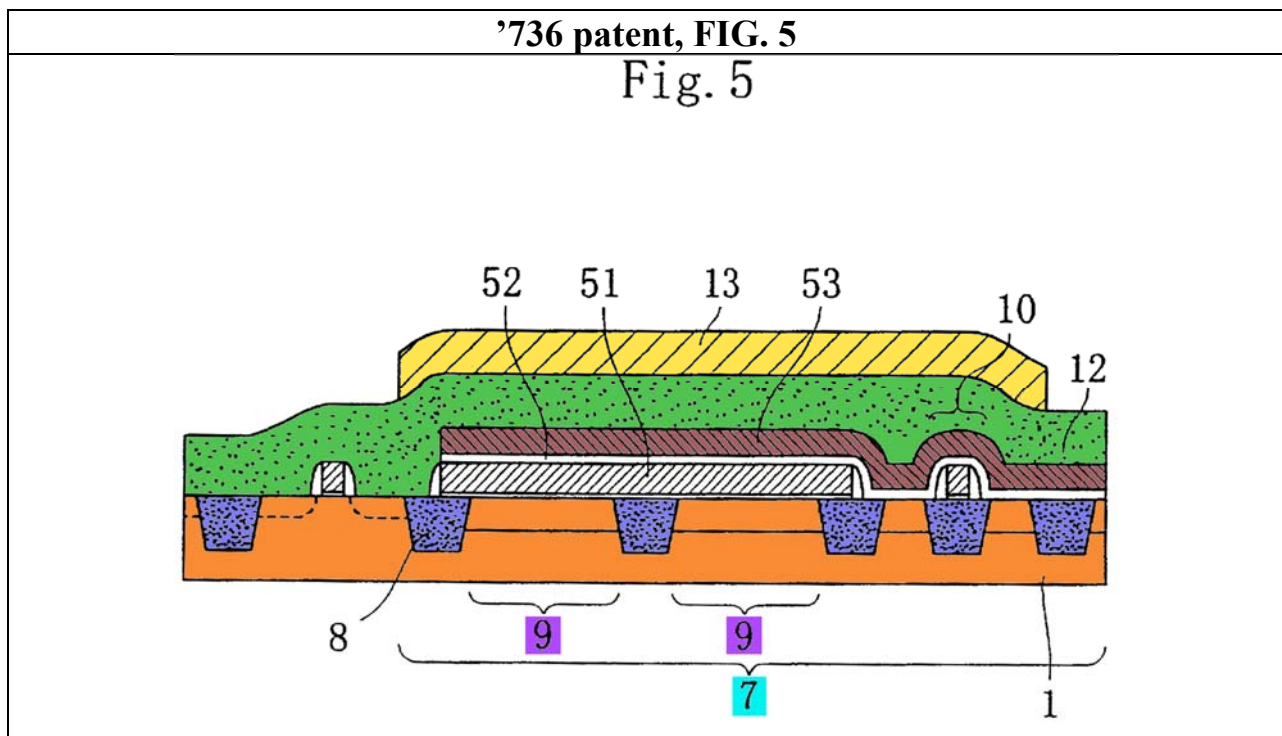
distance, the wiring-to-substrate capacitance is reduced in the semiconductor device according to the present embodiment, resulting in a higher operating speed.”) (Ex. 1103). The ’736 patent also states that overall capacitance is reduced since a second capacitance (the capacitance of the dielectric film) is added in series with the capacitance of the interlayer insulating film. ’736 patent at 4:28-35 (Ex. 1103). Bravman Decl. ¶ 63 (Ex. 1101).

As shown in FIG 5 below, a **resistor film** is provided in accordance with claim 13. *See* ’736 patent at 15:53-16:18 (Ex. 1103). A silicon oxide film 52 and a **high resistor film 53** is formed over dummy gate 51, polysilicon wire 10, and **substrate 1**. The ’736 patent describes the high resistor film 53 as being composed of polysilicon film and having “a sheet resistance film higher than that of the first-layer polysilicon film composing the gate electrode 4 . . . .” ’736 patent at 16:6-15 (Ex. 1103). The ’736 patent further indicates that

it is sufficient to consider the capacitance between the wiring and high resistor film instead of the capacitance between the wiring and substrate. In this case, since the resistance of the polysilicon film composing the high resistor film 53 is high, a voltage drop occurs between the top face of the high resistor film 53 and the surface of the semiconductor substrate 1. Accordingly, the voltage applied to the top and bottom faces of the interlayer insulating film is reduced, though the capacitance of the

interlayer insulating film 12 remains unchanged. Since the amount of charge accumulated in the top and bottom faces of the interlayer insulating film 12 decreases in direct proportion to the voltage applied thereto, the time required for charging or discharging between the wiring and high resistor is reduced . . . .

'736 patent at 16:20-34 (Ex. 1103). In other words, because the wire and the resistor film, separated by the interlayer insulating film, acts as a capacitor in series with a second capacitor comprising the resistor film and the substrate, the overall wire-to-substrate capacitance decreases. This means that the charge collected on the top and bottom faces of the interlayer insulating film decreases. Bravman Decl. ¶¶ 64-65 (Ex. 1101).



As explained in greater detail below, however, the claims covering these embodiments present little more than a routine modification of APA semiconductor devices using well-known techniques to reduce overall capacitance. There is nothing novel or inventive about the structures, materials, configurations, or methods to reduce overall capacitance in any of the challenged claims of the '736 patent. Bravman Decl. ¶ 70 (Ex. 1101).

## 2. Prosecution History

U.S. Application No. 09/469,498 (“the ’498 application”)—which issued as the ’736 patent—was filed on December 22, 1999, as a “division of application No. 08/987,137, filed on Nov. 25, 1997, now Pat. No. 6,130,139” (’736 patent at Related U.S. Application Data (62) (Ex. 1103)), and claims priority to JP 08-314762, filed on November 26, 1996, and JP 09-023844, filed on February 6, 1997. *See id* at Foreign Application Priority Data (30). (Ex. 1103).

On February 26, 2001, the claims of the ’498 application were rejected as being anticipated over prior art references not relied upon in this petition. *See* File History of U.S. Patent No. 6,346,736 (“’736 patent File History”) at Non-Final Rejection, 161-200, dated Feb. 26, 2001 (Ex. 1104). On July 17, 2001, Applicants amended the claims and argued that the prior art references do not teach the amended claims. *Id.* at Amendment, 178-97, dated July 17, 2001 (Ex. 1104).

In the process, Applicants confirmed that the APA structures and the **wiring-to-substrate** capacitances arising from those structures were well-known in the art. *See* '736 patent File History at Response, 185, dated July 17, 2001 (“More specifically, it is a known technique to form dummy semiconductor portions in an isolation region in order to obtain an isolation region having a planarized surface. Indeed, without such dummy semiconductor portions, it would be difficult to obtain a planarized surface of the isolation region. However, prior to the present invention there has been the problem that the formation of the dummy semiconductor portions increases the wiring-to-substrate capacitance in the isolation region, as is described in the “BACKGROUND OF THE INVENTION” portion of the specification and Figs. 21(a) – 21(c).”) (Ex. 1104).

Applicants further argued that the cited prior art references do not teach or suggest the amended claims. The table below summarizes the amendments that were made to the final limitations of the challenged independent claims, where underlining represents an added limitation. Bravman Decl. ¶ 74 (Ex. 1101).

Claim	Limitation	Corresponding Figures
6	“a <b>dielectric film</b> interposed between at least said <b>dummy semiconductor portions</b> of said <b>isolation region</b> and said <b>interlayer insulating film</b> ”	<p>Fig. 12</p> <p>'736 patent, FIG. 12</p>
13	“a <b>resistor film</b> formed <u>under</u> said <b>wire</b> , and between said <b>interlayer insulating film</b> and at least said <b>dummy semiconductor portions</b> of said <b>isolation region</b> ”	<p>Fig. 5</p> <p>'736 patent, FIG. 5</p>

## VII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA at the time of the alleged invention would have had at least a B.S. degree in electrical engineering, materials science or engineering, or chemical engineering (or equivalent education), and would have two or three years of experience with integrated circuit manufacturing, fabrication, and structures. This was the typical level of experience of persons working with processes for manufacturing semiconductor device structures at the time of the alleged invention. Bravman Decl. ¶¶ 75-76 (Ex. 1101).

## VIII. CLAIM CONSTRUCTION

As noted above, the '736 patent is a divisional application of U.S. Patent No. 6,130,139, which was filed on November 25, 1997. The '736 patent therefore expired on November 25, 2017. Accordingly, this petition applies a district court-type claim construction. *See, e.g., Omron Oilfield & Marine, Inc. v. MD/TOTCO, A Division of VARCO, L.P.*, IPR2013-00265, Paper No. 11, \*at 7 (PTAB Oct. 31, 2013) (“The Board’s review of the claims of an expired patent is similar to that of a district court’s review.”) (citing *In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012)); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005).

## IX. OVERVIEW OF THE PRIMARY PRIOR ART REFERENCES

### A. Overview of Admitted Prior Art

The '736 patent admits that most aspects of the claimed structures were well known. For example, comparing FIG. 1 with admitted prior art (APA) FIG. 19 shows that the following claimed elements were all admittedly well-known:

“a **semiconductor substrate** having an **active region** and an **isolation region** surrounding said **active region**,”

“a **first trench portion** [solid blue arrow] filled with an insulating material formed to separate said **active region** from said **isolation region**,”

“a **second trench portion** [dotted blue arrows] filled with an insulating material formed to separate a plurality of **dummy semiconductor portions** in said **isolation region**,”

“an **interlayer insulating film** formed to extend continuously over said **active region** and said **isolation region**,” and

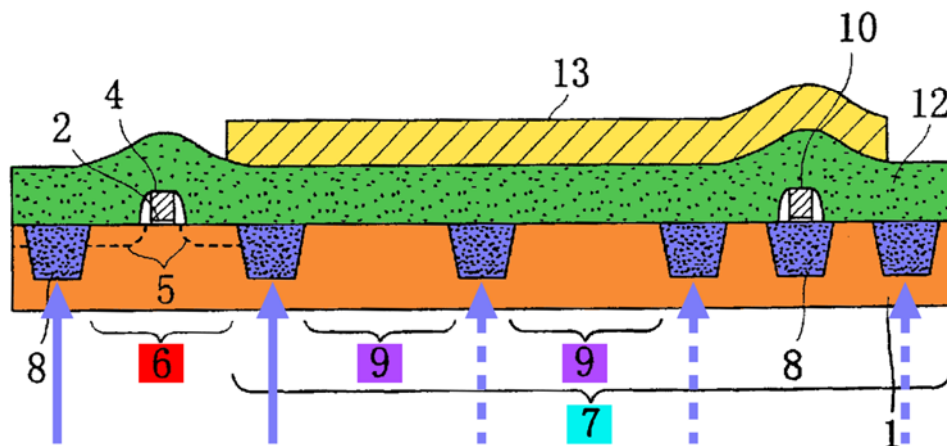
“a **wire** formed on said **interlayer insulating film** covering said **dummy semiconductor portions** and said **second trench portion** in said **isolation region**”



**APA, FIG. 19**

Fig. 19

PRIOR ART



**APA, FIG. 12 (claim 6)**

**APA, FIG. 5 (claim 13)**

Fig. 12

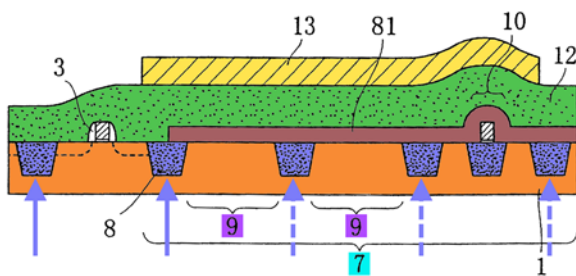
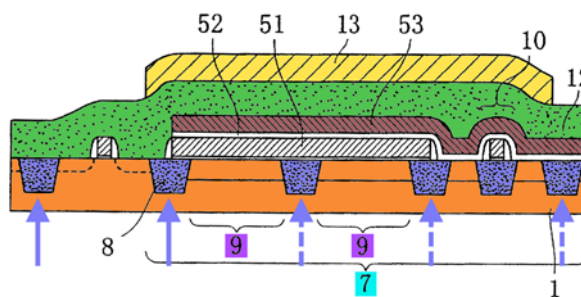


Fig. 5



Moreover, the '736 patent admits that a POSITA recognized the increased **wiring-to-substrate** capacitance problem that the claims purport to solve. *See* '736 patent at 3:1-30 (describing, as part of the APA and with respect to Figures 21(a) and (b), that LOCOS-isolated devices had lower wiring-to-substrate capacitance than STI-isolated devices) (Ex. 1103). The patent therefore effectively admits that there was a motivation to find solutions to reduce the increased **wiring-to-substrate** capacitance in semiconductor devices formed using trench isolations so as to increase the operating speed. *See e.g.*, Noguchi at 1:12-16 (“[t]he invention relates . . . to a semiconductor device in which a reduction of a parasitic capacitance between a substrate and a conductive layer utilized for wiring is needed in order to improve the operation speed.”) (Ex. 1121); '736 patent File History at Remarks, 185, dated July 17, 2001 (“More specifically, it is a known technique to form dummy semiconductor portions in an isolation region in order to obtain an isolation region having a planarized surface. Indeed, without such dummy semiconductor portions, it would be difficult to obtain a planarized surface of the isolation region. However, prior to the present invention there has been the problem that the formation of the dummy semiconductor portions deleteriously increases the wiring-to-substrate capacitance in the isolation region, as is described in the “BACKGROUND OF THE INVENTION” portion of the specification and Figs. 21(a) – 21(c).”) (Ex. 1104). Bravman Decl. ¶ 83 (Ex. 1101).

## B. Overview of Oshima

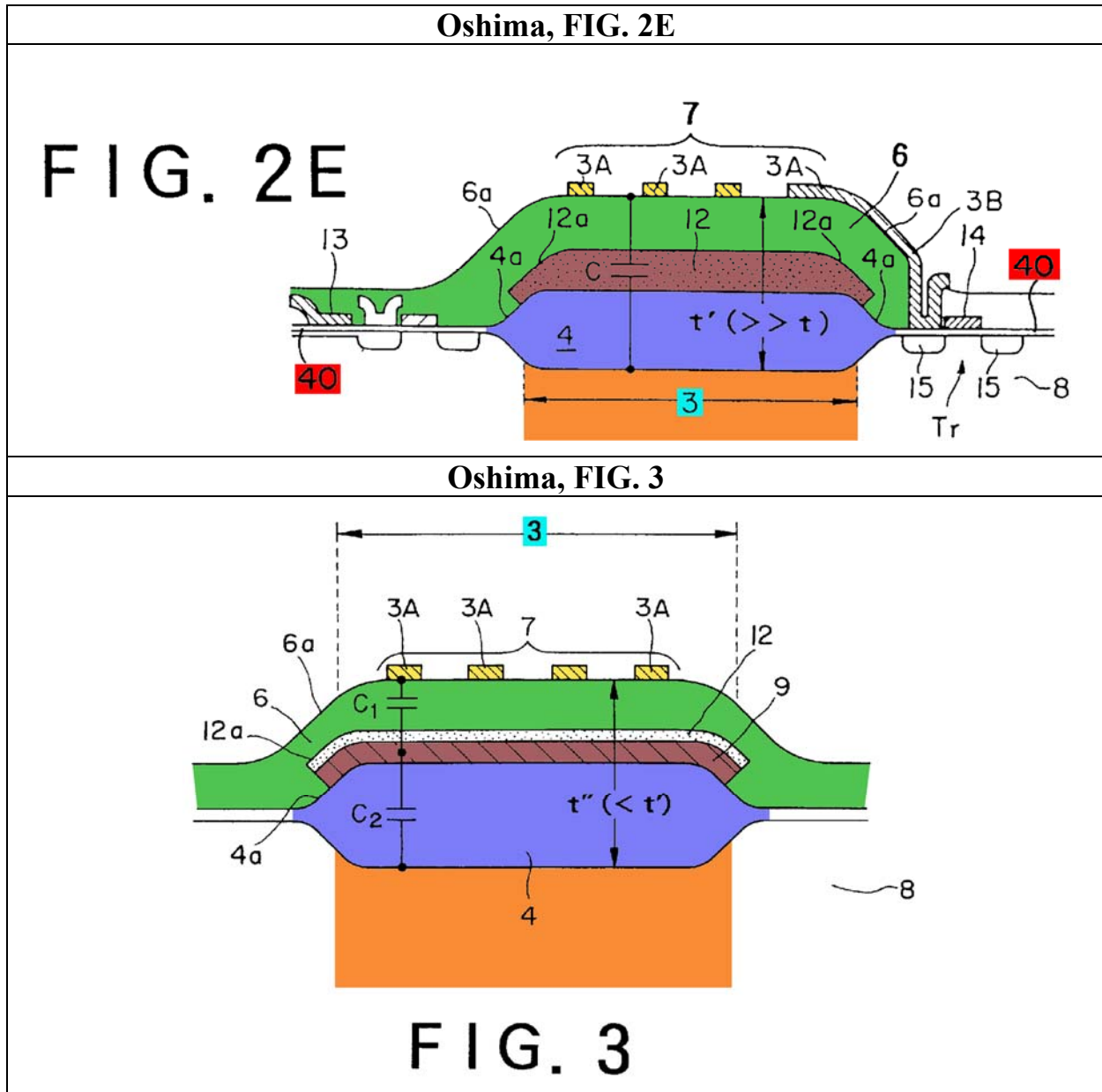
Oshima was not considered during the prosecution of the '736 patent.

Oshima is directed to a “semiconductor integrated circuit having reduced wiring capacitance.” Oshima at Title (Ex. 1118). Oshima teaches “**circuit block regions [i.e., active region] 2**,” “indicated by reference numeral 40,” Oshima at 4:57-5:3 (Ex. 1118), next to the **bus line region 3** that contain “**bus lines 3A and wires 3B**.” Oshima at 4:50-56 (Ex. 1118). Bravman Decl. ¶¶ 85-87 (Ex. 1101).

Oshima teaches different methods to reduce the wiring-to-substrate capacitance in the **isolation regions**.<sup>7</sup> Oshima at Abstract (“the wiring capacitance of the bus line region is reduced, so that the operation speed can be increased, the power consumption can be decreased, and the chip size can be reduced.”); *see also id.* at 2:37-43 (Ex. 1118). First, as shown in FIG. 2E, Oshima reduces wiring capacitance “by selectively increasing the interlayer film thickness markedly under the bus line region.” Oshima at 2:42-44 (Ex. 1118). Oshima states that “[i]n order to reduce the wiring capacitance, the thicker the **oxide film 12** is, the better will be the result.” Oshima at 5:17-18 (Ex. 1118). Bravman Decl. ¶¶ 85-87 (Ex. 1101).

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<sup>7</sup> Oshima calls these isolation regions “bus line” or “wiring” regions. *See, e.g.,* Oshima at 1:16-20, 2:5-12, 4:57-62, 5:33-44; FIGS. 1, 2A, 3, 4A, 5A, 6, 7 (identifying bus line region 3).



In a second embodiment, as shown in FIG. 3, Oshima teaches providing a “poly silicon layer 9 . . . under the bus line region 3.” Oshima at 6:37-42 (Ex. 1118). Oshima explains that “the capacitance  $C$  between the bus line region wiring layer 7 and the semiconductor substrate 7 [sic] can be reduced as  $\frac{1}{C} = \left(\frac{1}{C_1}\right) +$

$\left(\frac{1}{C2}\right)$  where C1 denotes the capacitance between the **poly silicon layer 9** and the bus line region **wiring layer 7**, and C2 denotes the capacitance between the **poly silicon layer 9** and the semiconductor **substrate 8**.” Oshima at 6:45-54 (Ex. 1118). In other words, Oshima explains that the **poly silicon layer 9** adds capacitance in series, as shown in FIG. 3. Bravman Decl. ¶ 88 (Ex. 1101).

## **X. SPECIFIC GROUNDS FOR PETITION**

Intel demonstrates below how the prior art discloses each and every limitation of the Challenged Claims.

Secondary considerations do not support a finding of nonobviousness. There is no evidence of commercial success, long felt need, failure of others, skepticism, praise, teaching away, recognition of a problem, or copying by competitors. Bravman Decl. ¶¶ 149-157 (Ex. 1101). Should IP Bridge hereafter put forth allegations regarding secondary considerations, Intel requests an opportunity to respond.

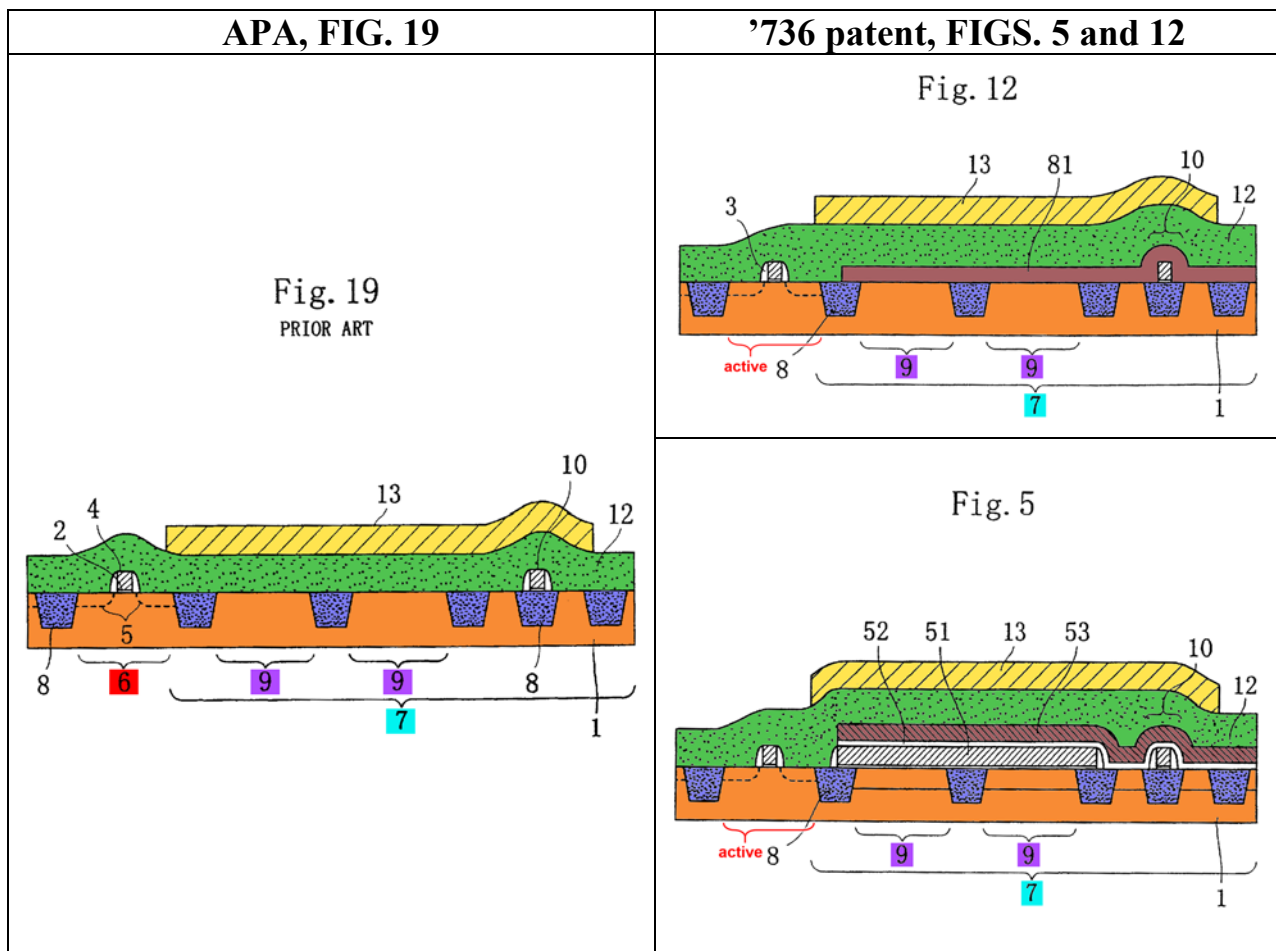
### **A. Ground 1: Claims 6-9, 11, 13, 14, 16, and 20 Are Obvious in View of APA and Oshima**

Intel demonstrates below how the prior art discloses each and every limitation of claims 6-9, 11, 13, 14, 16, and 20.

1. Independent Claims 6 and 13

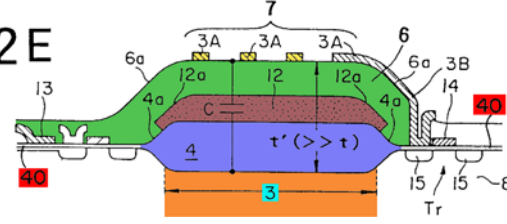
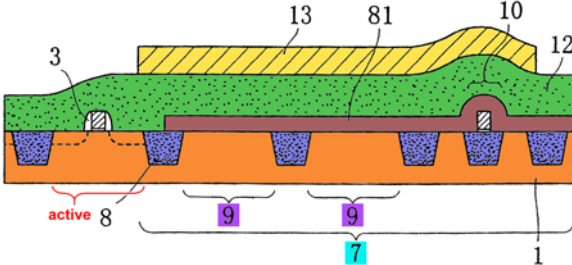
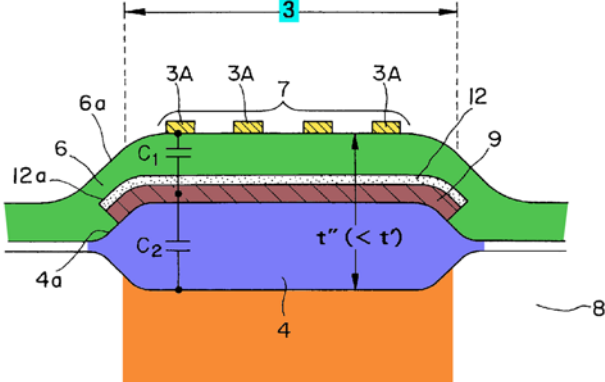
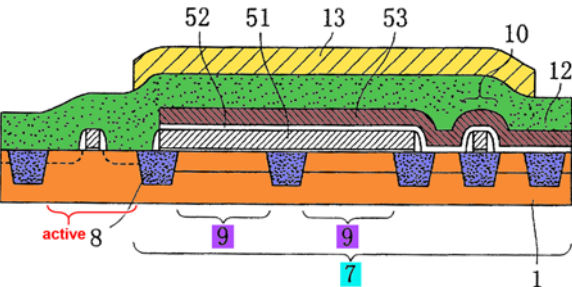
a) **“A semiconductor device, comprising”**

To the extent that the preamble of the '736 patent is limiting, the '736 patent acknowledges that the preamble was already well-known. APA “FIG. 19 shows an example of the conventional trench-isolated *semiconductor device* having the dummy island semiconductor portions.” '736 patent at 1:35-37 (Ex. 1103). Bravman Decl. ¶ 90 (Ex. 1101).



Oshima also discloses a “*semiconductor integrated circuit* having reduced wiring capacitance.” Oshima at Title; *see also id.* at Abstract, 1:6-10, 2:38-43, 2:66-

3:20, 4:63-5:3, 7:46-59 (Ex. 1118). Exemplary semiconductor devices are shown in FIGs. 2E and 3. *See* Oshima at 2:32-65 (Ex. 1118). Accordingly, Oshima teaches this limitation. Bravman Decl. ¶ 91 (Ex. 1101).

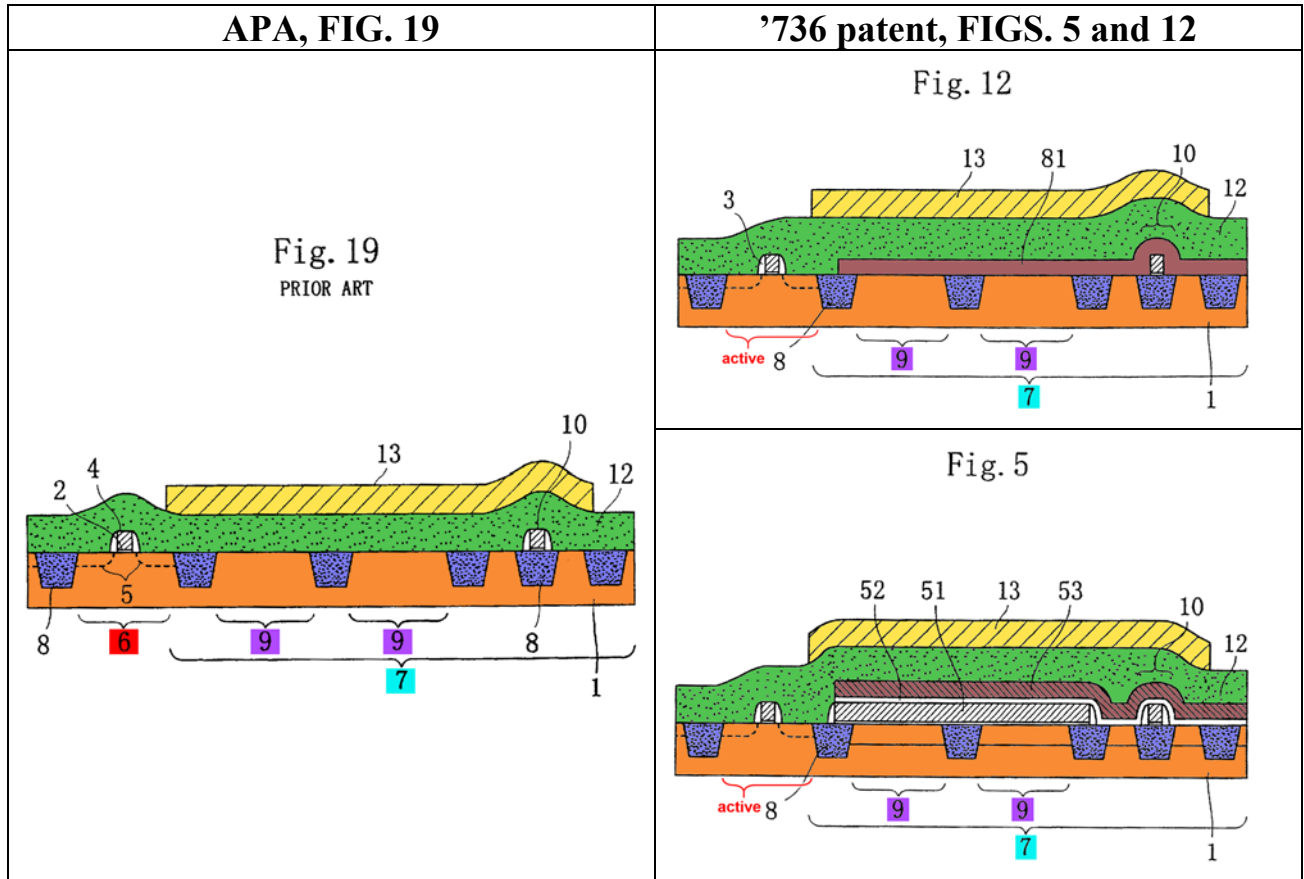
Oshima, FIGs. 2E and 3	'736 patent, FIGS. 5 and 12
<p><b>FIG. 2E</b></p> 	<p><b>Fig. 12</b></p> 
 <p><b>FIG. 3</b></p>	<p><b>Fig. 5</b></p> 

b) “a **semiconductor substrate** having an **active region** and an **isolation region** surrounding said **active region**”

The '736 patent admits that this limitation was well-known. APA FIG. 19 shows “an **active region 6** of a P-type **silicon substrate 1** . . . .” '736 patent at 1:38-41 (Ex. 1103). APA further notes that an “**isolation region 7** surrounding the **active region 6** is formed . . . .” '736 patent at 1:41-43 (Ex. 1103). APA discloses that



“[t]he semiconductor portions 9 [in the isolation region] may be considered as dummy active regions which do not function as active regions.” ’736 patent at 2:10-12 (Ex. 1103). Bravman Decl. ¶ 92 (Ex. 1101).



Oshima also teaches this limitation. Oshima discloses a **semiconductor substrate 8**. Oshima at 5:23-30 (“Successively, various circuit elements . . . are formed in the circuit block region 2 of the semiconductor substrate 8 . . .”), 6:61-64 (“Therefore, it is possible to reduce the capacitance C, as compared with the conventional structure having no floating terminal between the bus line region wiring layer 7 and the semiconductor substrate 8.”); *see also id.* at Abstract, 1:41-



55, 2:2-12, 2:45-54, 2:55-65, 4:57-62, 5:37-44, 6:43-64 (Ex. 1118). Bravman Decl. ¶ 93 (Ex. 1101).

Oshima further discloses “**circuit block region 2**” that contain transistors. *See* Oshima at 4:63-5:3 (“[A] poly silicon layer 9 is formed are [sic] all over the surface of the entire field oxide film 4, in order to form plate electrodes 13 of memory cells and gate electrodes 14 *of the transistors . . . in the circuit block region (i.e., active region) 2 . . .*”) (Ex. 1118). These “**circuit block regions 2** [are] indicated by **reference numeral 40**” in FIG. 2E below. *See* Oshima at 4:57-62 (Ex. 1118). Bravman Decl. ¶ 94 (Ex. 1101).

Oshima also teaches an **isolation region**. In the ’736 patent, an **isolation region** is contrasted with an **active region** and is referred to as a structure or region that electrically isolates transistors (*e.g.*, MOSFETs) found within neighboring active regions. *See* ’736 patent at 11:34-43 (“As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with *an element functioning as a MOSFET* composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An *isolation region 7 for electrically isolating the individual elements* is formed with a plurality of trench portions 8 filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 *and not serving as active regions.*”); *see also id.* at 13:36-45, 14:37-46, 15:55-64, 18:16-24,

21:13-22, 23:4-15, 24:63-25:5 (Ex. 1103); *see also* Uyemura at 42 (isolation regions are used to electrically isolate “neighboring devices”). Bravman Decl. ¶¶ 95-96 (Ex. 1101).

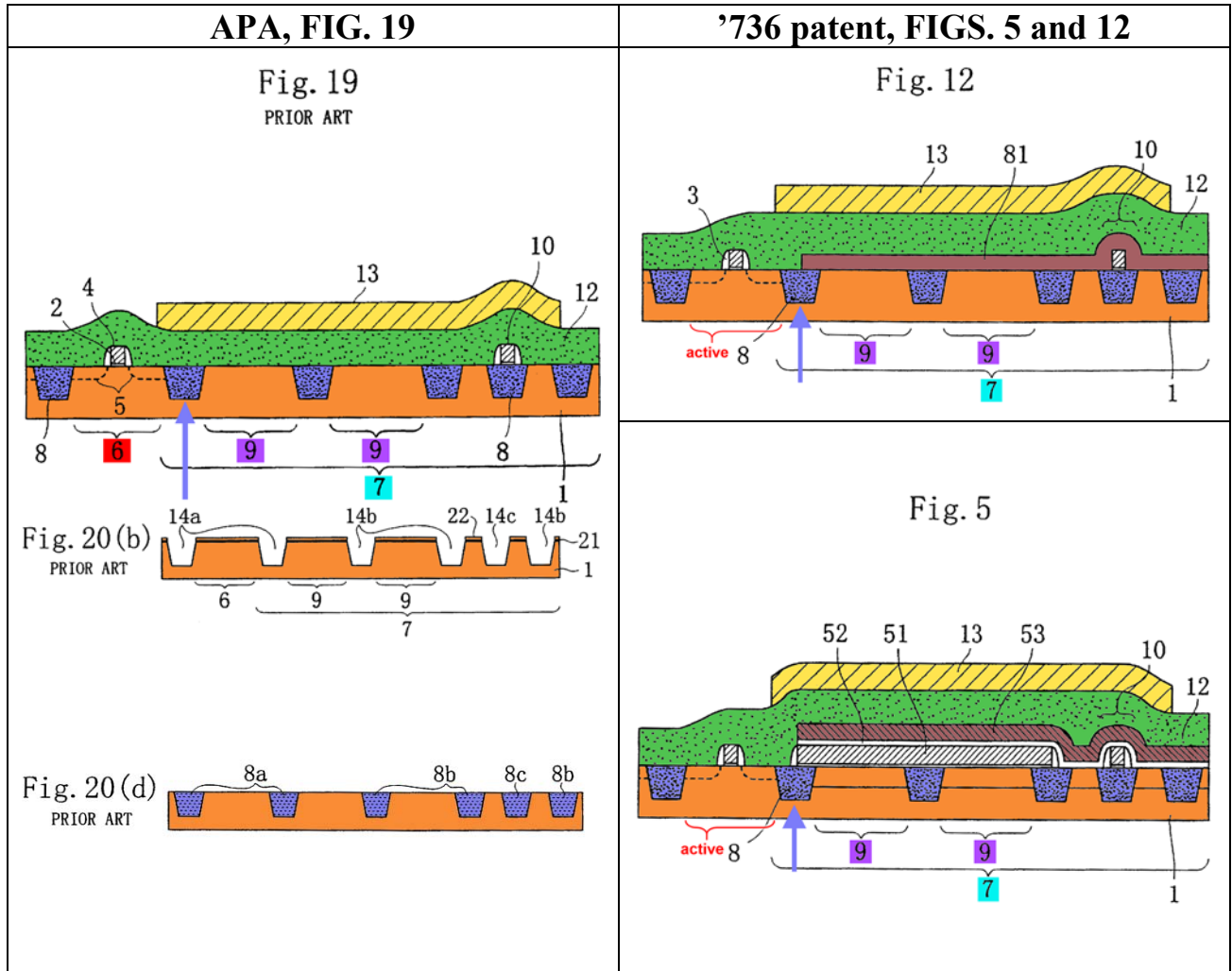
In Oshima, “an element separating **field oxide film 4** is formed all over the surface of the **semiconductor substrate 8** in such a way as to become selectively thick at only the region where the **bus line regions 3** are to be formed . . . .” Oshima at 4:57-62; *see also id.* at 1:16-20, 4:57-62, 5:33-44, 6:34-64 (Ex. 1118). The **bus line regions 3** isolate and surround the **circuit block region 2**. *Id.* at 2:5-6 (contrasting bus line region from active region); FIGS. 1, 2A, 3, 4A, 5A, 6, 7 (identifying bus line region 3). Accordingly, Oshima teaches this limitation. Bravman Decl. ¶ 95 (Ex. 1101).

<p><b>Oshima, FIGS. 2E and 3</b></p> <div style="text-align: center;"> <p><b>FIG. 2E</b></p> </div> <div style="text-align: center;"> <p><b>FIG. 3</b></p> </div>	<p><b>'736 patent, FIGS. 5 and 12</b></p> <div style="text-align: center;"> <p><b>Fig. 12</b></p> </div> <div style="text-align: center;"> <p><b>Fig. 5</b></p> </div>
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- c) “a **first trench portion** filled with an insulating material formed to separate said **active region** from said **isolation region**”
- “a **first trench portion** filled with an insulating material formed to separate a plurality of **dummy semiconductor portions** in said **isolation region**”

APA admits these elements were well-known. The APA discloses that an “**isolation region 7** surrounding the **active region 6** is formed with a plurality of **trench portions 8** each filled with a silicon oxide film.” ’736 patent at 1:41-44 (Ex. 1103). Silicon oxide is a type of insulating material. As shown, the second-to-left

**trench portion 8**, highlighted with a blue arrow, separates the **active region 6** and the **isolation region 7**. Bravman Decl. ¶ 97 (Ex. 1101).



APA further discloses that “[b]etween the individual **trench portions 8**, there are provided **semiconductor portions 9** having top surfaces at the same level as the top surfaces of the **trench portions**.” ’736 patent at 1:44-47 (Ex. 1103). APA further notes that “[i]n the **isolation region 7** also, the **semiconductor portions 9** have been provided to form at least one projecting portion surrounded by the trenches 14 [which correspond to **trench portions 8**, as shown above in FIGS. 20(b)

and 20(d)]. The **semiconductor portions 9** may be considered as dummy active regions which do not function as active regions.” ’736 patent at 2:7-25 (Ex. 1103). As such, APA discloses this limitation. Bravman Decl. ¶ 98 (Ex. 1101).

Oshima discloses a **field oxide film 4** that is selectively thicker only at the **bus line regions 3**. Oshima at 4:57-62 (“an element separating field oxide film 4 is formed all over the surface of the semiconductor substrate 8 in such a way as to become selectively thick at only the region where the bus line regions 3 are to be formed . . . .”) (Ex. 1118). As shown in FIG. 2E of Oshima, the **field oxide film 4** in the **bus line regions 3** separates the “**circuit block regions 2, indicated by reference numeral 40.**” *Id.* (Ex. 1118). Bravman Decl. ¶ 99 (Ex. 1101).

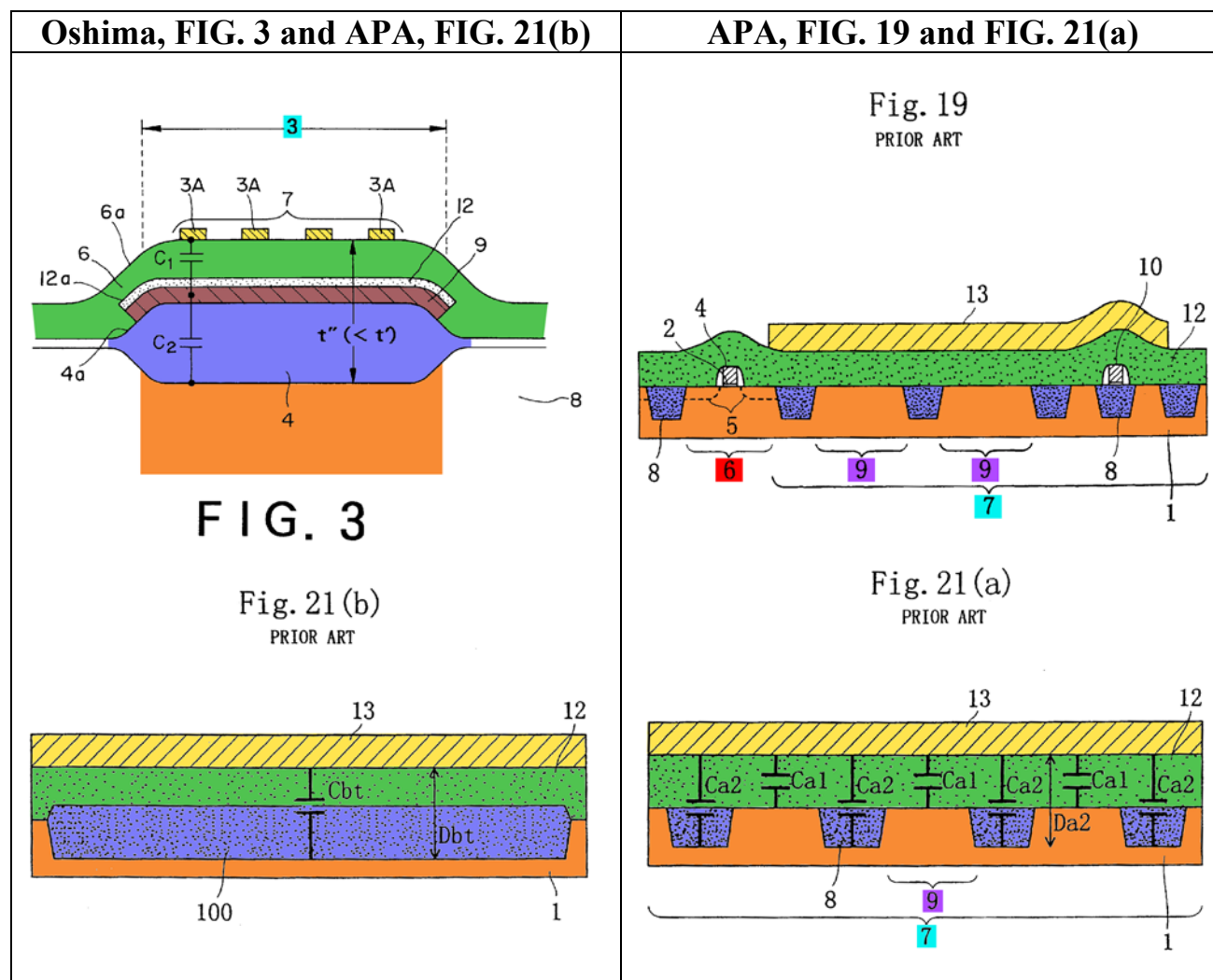
Oshima, FIGS. 2E and 3	'736 patent, FIGS. 5 and 12
<p data-bbox="321 457 401 504"><b>FIG. 2E</b></p>	<p data-bbox="1127 352 1232 386">Fig. 12</p>
<p data-bbox="401 1274 599 1320"><b>FIG. 3</b></p>	<p data-bbox="1166 877 1258 913">Fig. 5</p>

### i) Reasons to Combine

Replacing Oshima's **field oxide film 4** with **trench portions** and **dummy semiconductor portions** would have been obvious in view of the APA. APA FIGS. 19, 21(a), and 21(b) show that as transistor dimensions shrink, large oxide regions, such as disclosed in Oshima as **field oxide film 4** and illustrated in Figure 21(b) as **LOCOS isolation film 100**, are replaced with a combination of **trench portions 8**

and **dummy semiconductor portions 9**, such as illustrated in Figures 19 and 21(a) because, *inter alia*, large areas of oxide cause polishing/fabrication problems—problems that were well-known in the art prior to the '736 patent. *See* '736 patent at 1:10-34 (“As higher-density and increasingly miniaturized semiconductor devices have been implemented in recent years, repeated attempts have been made to substitute a trench isolation technique for a LOCOS technique . . . the provision of dummy island semiconductor portions has been proposed to avoid trouble resulting from so-called pattern dependence, which causes polishing properties to vary depending on the area of a region to be planarized.”) (Ex. 1103); *see also supra* § VI.B (describing advantages of STI over LOCOS). Bravman Decl. ¶ 100 (Ex. 1101).

The result of such miniaturization and use of **trench isolation** techniques is shown in APA FIG. 19. '736 patent at 1:35-37 (“FIG. 19 shows an example of the conventional trench-isolated semiconductor device having the dummy island semiconductor portions.”) (Ex. 1103). Bravman Decl. ¶ 100 (Ex. 1101).



Oshima is likewise directed to reducing transistor sizes and mitigating the problems that arise from such miniaturization. *See* Oshima at 1:14-23 (“the integrated circuits have become more and more microminiaturized . . . so that space required for a wiring region (a bus line region) for connecting the circuit blocks to one another has increase. As a result, the proportion of the wiring capacitance to the capacitance load of the respective circuit signals has increased.”); 1:41-2:34 (Ex. 1118). A POSITA would have been motivated to employ the admittedly well-known

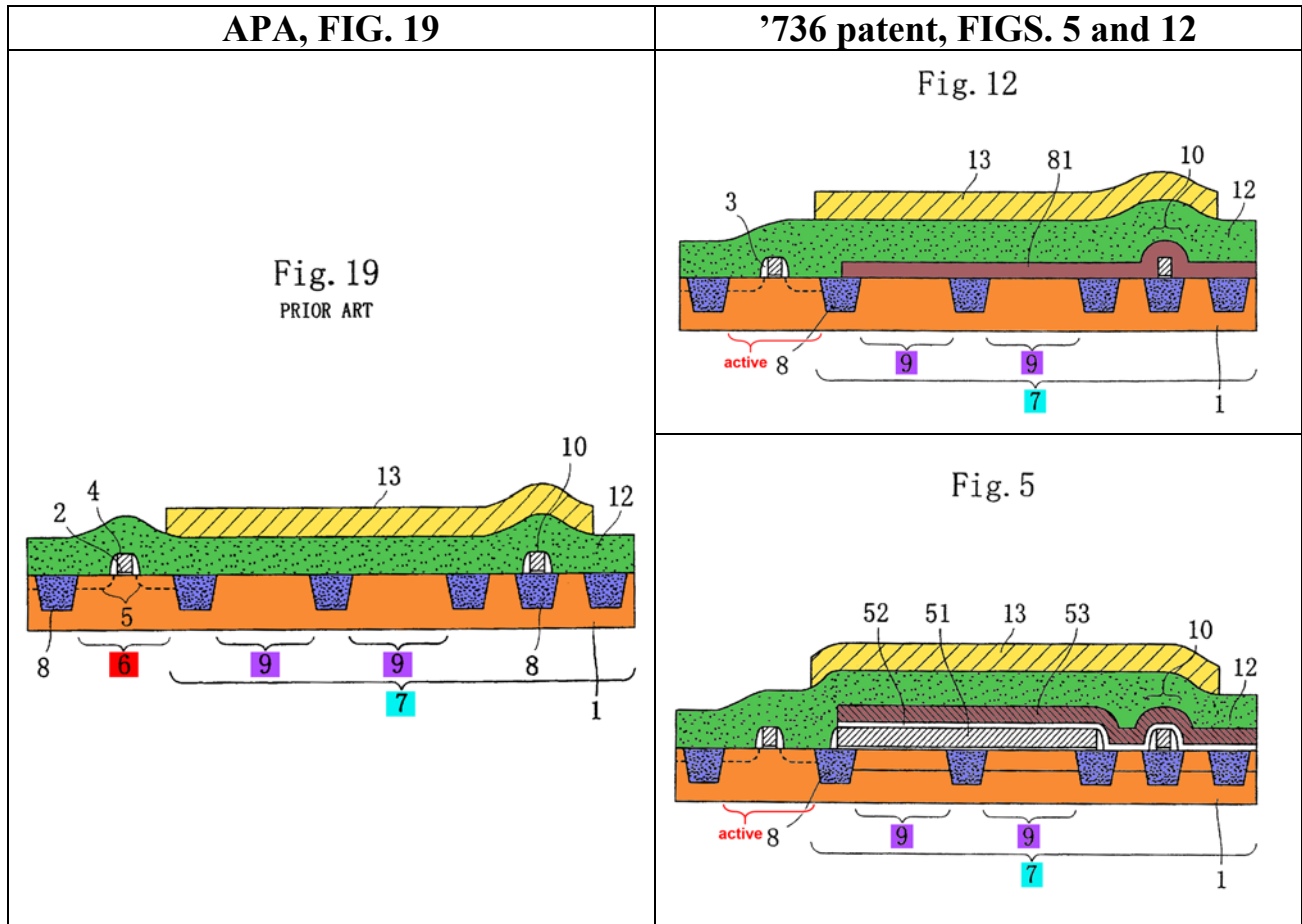


scheme of replacing a large **field oxide film 4** with a combination of **trench portions 8** and **dummy semiconductor portions 9** in an attempt to avoid the problems associated with such large **oxide regions** when fabricating the devices. Indeed, by the time of the filing of the '736 patent, the industry was already shifting to replacing LOCOS with STI due to the latter's benefits, including, for example, the lack of the "bird's beak," increased planarization, and decreased pattern dependence. *See supra* § VI.B. Bravman Decl. ¶ 101 (Ex. 1101).

*See also Taiwan Semiconductor Mfg. Co. et al. v. Godo Kaisha IP Bridge 1*, IPR2016-01246, Paper 49, \*at 21-36, 65 n.18 (PTAB Jan. 3, 2018) (finding that it would have been obvious to replace LOCOS with STI at least as of July 1996—four months before the priority date of the '736 patent).

d) “an **interlayer insulating film** formed to extend continuously over said **active region** and said **isolation region**”

APA admits that this limitation was known in the art. APA discloses that an “**interlayer insulating film 12** is deposited over the *entire surface of the* **substrate**, followed by a **metal wire 13** provided thereon.” '736 patent at 1:49-51 (Ex. 1103). Bravman Decl. ¶ 102 (Ex. 1101).

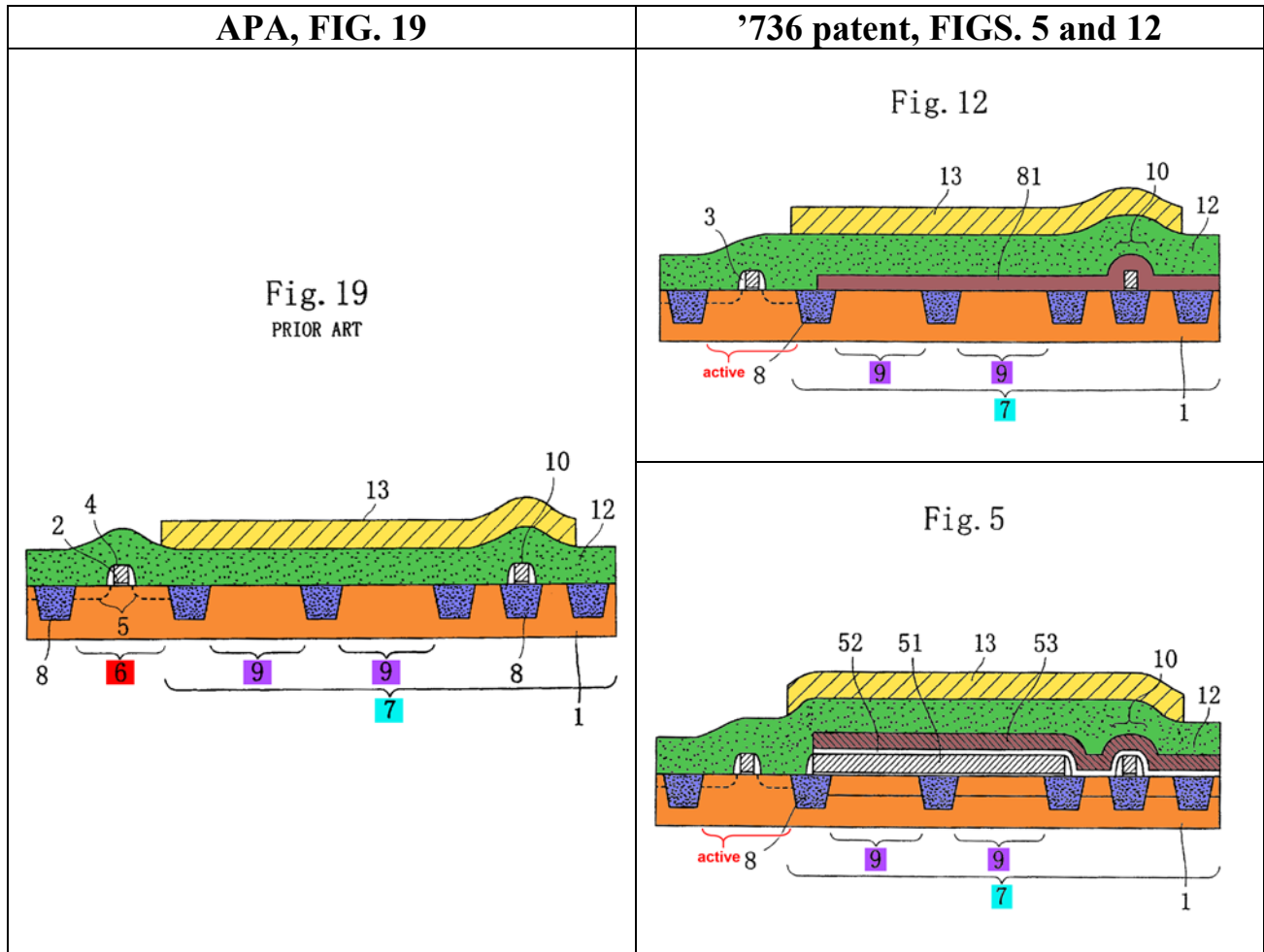


Oshima also discloses this element. Oshima discloses that after the **circuit block regions 2**, indicated by **reference numeral 40**, and **field oxide film 4** and **oxide film 12** in the **bus line regions 3** are formed, “an **interlayer insulating film 6** is formed over the entire surface of the integrated circuit 1.” Oshima at 5:31-32; *see also id.* at 4:57-5:3, 6:34-64 (Ex. 1118). Accordingly, Oshima teaches this limitation. Bravman Decl. ¶ 103 (Ex. 1101).

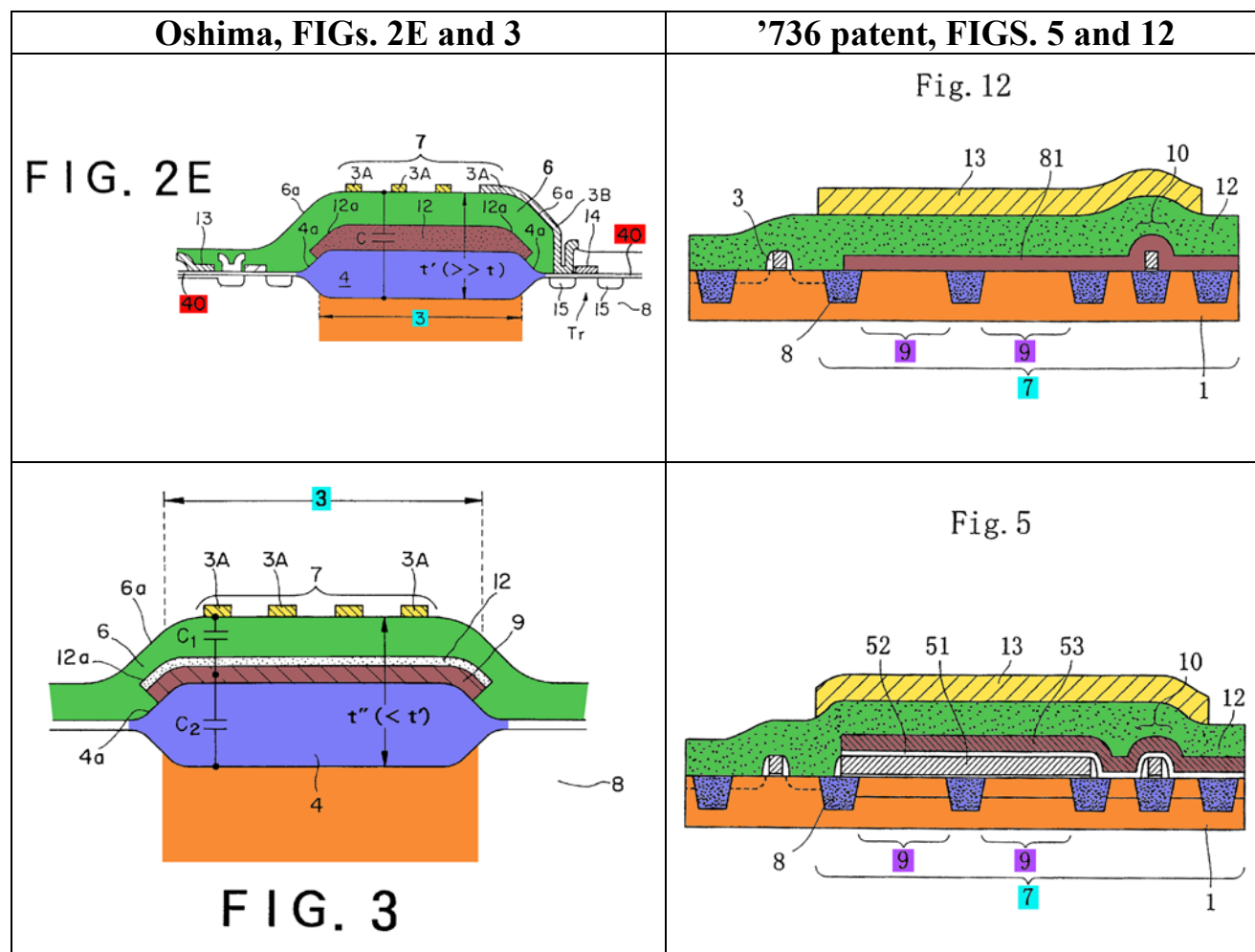
<p><b>Oshima, FIGS. 2E and 3</b></p>	<p><b>'736 patent, FIGS. 5 and 12</b></p>
<div style="text-align: center;"> <p><b>FIG. 2E</b></p> </div>	<div style="text-align: center;"> <p><b>Fig. 12</b></p> </div>
<div style="text-align: center;"> <p><b>FIG. 3</b></p> </div>	<div style="text-align: center;"> <p><b>Fig. 5</b></p> </div>

e) “a **wire** formed on said **interlayer insulating film** covering said **dummy semiconductor portions** and said **second trench portion** in said **isolation region**; and”

The APA acknowledges that this limitation was known. APA discloses that an “interlayer insulating film 12 is deposited over the entire surface of the substrate, followed by a metal wire 13 provided thereon.” ’736 patent at 1:49-51 (Ex. 1103). As shown in APA FIG. 19, the metal wire 13 covers the dummy semiconductor portions 9 and the second trench portion 8 in the isolation region 7, in the same manner as the embodiments in FIGS. 5, 7, and 12 that correspond to this limitation of claim 6. Bravman Decl. ¶ 104 (Ex. 1101).



Oshima discloses that “a bus line region **wiring layer 7** is formed on the **interlayer insulating film layer 6** at the area corresponding to the **bus line region 3.**” Oshima at 5:33-35 (Ex. 1118). As Oshima explains, “there are arranged **bus lines 3A and wires 3B** for connecting the **bus line 3A** to circuits formed in the **circuit block region 2.**” Oshima at 4:50-56 (Ex. 1118). Bravman Decl. ¶ 105 (Ex. 1101).



i) Reasons to Combine

As explained in Section X.A.1.c)i), it would have been obvious to replace the **field oxide film 4** with a combination of **trench portions 8** and **dummy semiconductor portions 9**.

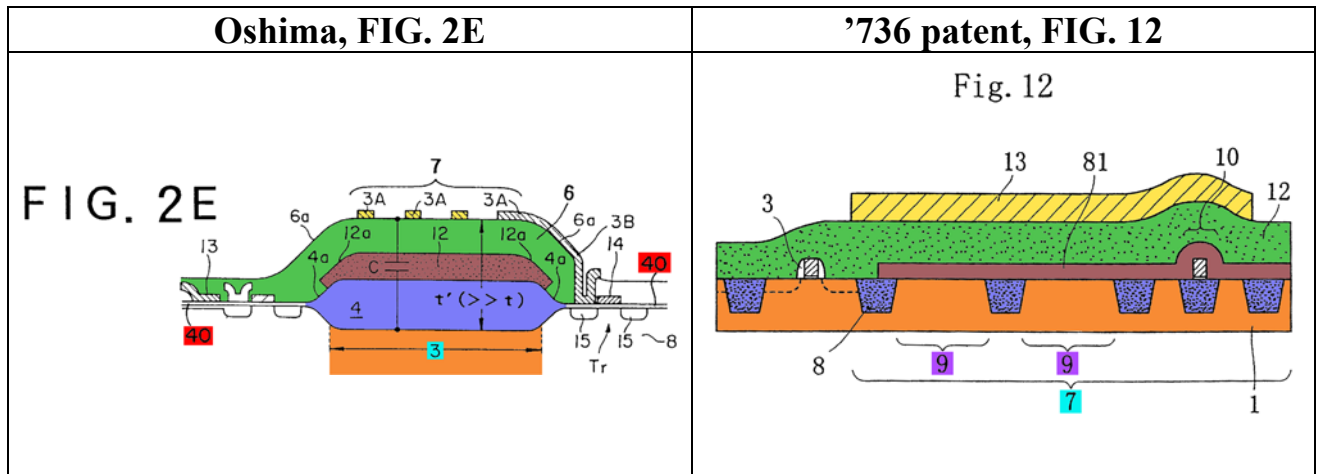
It would also have been obvious to provide a **metal wire** covering the **trench portions 8** and **dummy semiconductor portions 9**, as shown in APA FIG. 19. Oshima's **wiring layer 7** provides connections between different components of the integrated circuit. In the particular configuration shown, the **bus lines 3A** and **wires**

**3B** run into and out of the page. However, a POSITA would recognize that other configurations are possible, depending on the particular needs of the connections needed. One such configuration is shown in APA FIG. 19, where the **metal wire** runs across the page. In other words, if the **wires** in Oshima were rotated 90 degrees from the orientation shown in Oshima, the **wires** would appear similar to the configuration shown in APA FIG. 19. Accordingly, the differences between Oshima and the APA amount to minor modification of wire layout and would lead to expected behavior of delivering the desired signal or power in a manner desired by a layout engineer. *See, e.g.*, Oshima at FIGS. 1, 2E (showing different orientations for wires 3A, which run into the page, and wires 3B, which run across the page). These are merely different configurations that would be found in different parts of a semiconductor device, and such a modification is merely a simple substitution of a known element for another to obtain predictable results. It thus would have been obvious to a POSITA to rotate Oshima's **wiring layer 7**, or replace it with the **metal wire 13** shown in APA FIG. 19. Bravman Decl. ¶ 106 (Ex. 1101).

f) *Claim 6 only: “a **dielectric film** interposed between at least said **dummy semiconductor portions** of said **isolation region** and said **interlayer insulating film**.”*

Oshima teaches this limitation of claim 6 via its **oxide film 12**. As shown in FIG. 2E of Oshima, the **oxide film 12** is interposed between the **field oxide film 4** of the **bus line region 3** and the **interlayer insulating film 6**. Oshima at 4:47-6:33

(Ex. 1118). Oshima discloses that “the **oxide film 12** can be grown by thermal oxidation . . . . In order to reduce the wiring capacitance, the thicker the **oxide film 12** is, the better will be the result.” Oshima at 5:13-20; *see also* 1:56-62 (showing relationship between thickness and capacitance) (Ex. 1118). Oshima explains that “[a]s a result of the above-mentioned process, the thickness of the **interlayer film 6** formed between the semiconductor **substrate 8** and the **bus line region wiring layer 7** can be increased . . . . Therefore, it is possible to markedly reduce the wiring capacitance . . . .” Oshima at 5:37-44 (Ex. 1118). Bravman Decl. ¶¶ 107-08 (Ex. 1101).

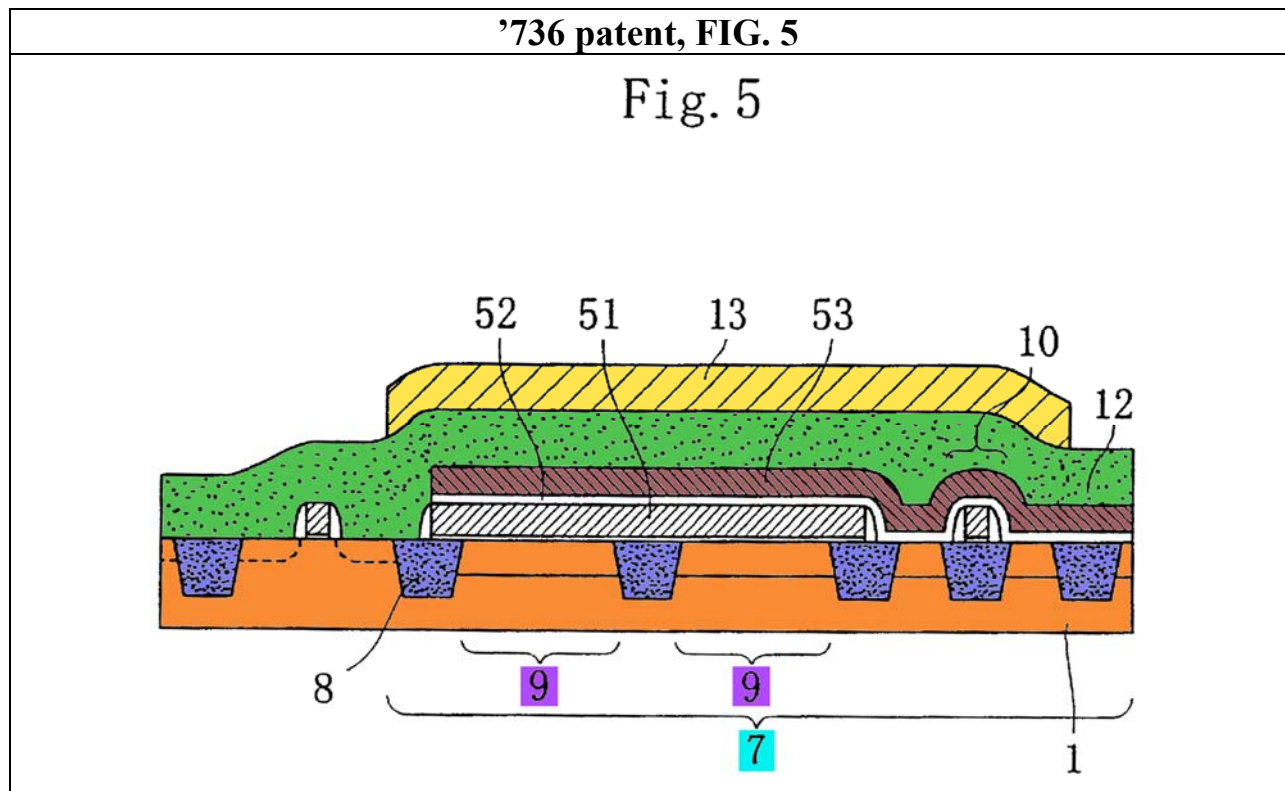


It would have been obvious for a POSITA to integrate Oshima’s **oxide film 12** into the APA. This is explained *infra* in Section X.A.1.g)i). Alternatively, it would have been obvious to a POSITA to replace Oshima’s **field oxide film 4** with a combination of **trench portions 8** and **dummy semiconductor portions 9**, as was discussed above. *See supra* § X.A.1.c)i). Bravman Decl. ¶ 109 (Ex. 1101).



- g) *Claim 13 only: “a resistor film formed under said wire, and between said interlayer insulating film and at least said dummy semiconductor portions of said isolation region.”*

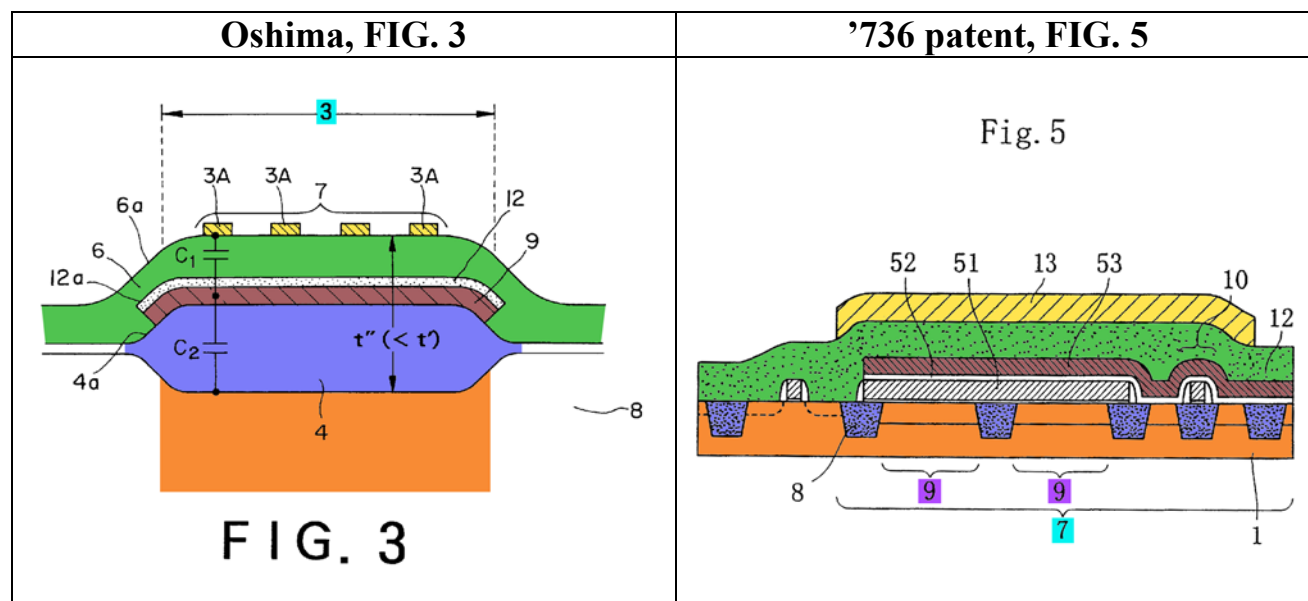
Oshima teaches this limitation of claim 6 via its **silicon layer 9**. As explained above in Section VI.D.1, the '736 patent discloses that a “**high resistor film 53** [shown below in FIG. 5] *composed of a polysilicon.*” '736 patent at 16:3-7 (Ex. 1103). “The polysilicon film composing the high resistor film 53 has a sheet resistance film higher than that of the first-layer polysilicon film composing the gate electrode 4 and the like and an impurity concentration of  $1 \times 10^{20} \text{ cm}^{-3}$  or less.” *Id.* at 16:12-15; *see also id.* at 18:28-19:12 (stating, in another embodiment, that the resistor film may be a “low-resistor film composed of silicide or the like”) (Ex. 1103).





Oshima discloses that in the process of forming the oxide film 12, “a **poly silicon layer 9** is formed . . . all over the surface of the entire field oxide film 4 . . . . [and] the **poly silicon layer 9** is oxidized into an oxide film 12.” Oshima at 4:47-5:21 (Ex. 1118). This is shown in FIGS. 2A-2E. In this embodiment, Oshima teaches that the poly silicon layer 9 is doped to facilitate its complete conversion into the interlayer oxide film 12. *See* Oshima at 6:16-27 (“Further, since the poly silicon layer 9 of high impurity concentration has such a nature that the thermal oxidization is accelerated, after the insulating film 10 has been etched, it is preferable to implant impurities onto the poly silicon layer 9 at the exposed bus line region 3. In this case, it is possible to thermo-oxidize the poly silicon layer 9 into the oxide film 12 as the perfect interlayer insulating film . . . .”) (Ex. 1118). Bravman Decl. ¶ 110 (Ex. 1101).

Oshima’s second embodiment teaches that “[i]n the case where the additional thermal process is limited due to the restriction of the processing conditions, it is impossible to perfectly oxidize the **poly silicon layer 9** formed under the bus line region 3. Therefore, the **poly silicon layer 9 inevitably remains** under the oxide film 12 formed by thermal oxidization.” Oshima at 6:34-42 (Ex. 1118). This is shown in FIG. 3. Bravman Decl. ¶ 110 (Ex. 1101).



Like the '736 patent's **polysilicon resistor film 53**, Oshima also discloses a “poly silicon film 9.” Oshima at 6:37-42 (Ex. 1118); *see also* '736 patent at 16:3-7, 16:12-15, 18:28-19:12 (allowing varying levels of resistivity). Oshima's **polysilicon film 9** also meets the claimed “**resistor film**” limitation. Bravman Decl. ¶ 111 (Ex. 1101).

Moreover, Oshima's FIG. 3 shows that the **polysilicon film 9** is formed under said **wiring layer 7**. As explained above in Section X.A.1.e), it would also have been obvious to a POISTA to provide a **metal wire** that covers the **trench portions 8** and **dummy semiconductor portions 9**, just as it was shown in APA FIG. 19. Accordingly, the **polysilicon film 9** is formed under the **metal wire** that covers the **trench portions 8** and **dummy semiconductor portions 9**. Bravman Decl. ¶ 112 (Ex. 1101).

The **polysilicon film 9** is also between said **interlayer film 6** and **field oxide film 4** of the **bus line region 3**. As explained above in Section X.A.1.c) and further below in Section X.A.1.h), it would have been obvious to replace the long **field oxide film 4** with a combination of **trench portions 8** and **dummy semiconductor portions 9**. Accordingly, the **polysilicon film 9** would have been between at least the **dummy semiconductor portions** and the **interlayer insulating film**. Bravman Decl. ¶ 113 (Ex. 1101).

i) Reasons to Combine

It would have been obvious to a POSITA to integrate Oshima's **oxide film 12** (claim 6) or **poly silicon layer 9** (claim 13) into the APA, which, as explained above (*see supra* § IX.A), expressly discloses all other elements of this claim. The APA notes that utilizing the trench isolation technique can lead to problems associated with increased capacitance. Specifically, APA explains that the wire-to-substrate capacitance ends up being higher for the miniaturized structure containing **trench portions 8** and **dummy semiconductor portions 9** than the structures that utilize **LOCOS** structures. *See* '736 patent at 2:50-3:30 (referring to APA Fig. 19 and noting that, "[a]lthough the formation of the island pattern composed of the dummy semiconductor portions in the isolation region has the advantage of achieving planarization with excellent in-plane uniformity, it also has the possibility of

increasing the wiring-to-substrate capacitance and resultantly reducing the operating speed of the semiconductor device.”) (Ex. 1103). Bravman Decl. ¶ 114 (Ex. 1101).

Oshima teaches a scheme that mitigates such increased capacitance and therefore is specifically directed to the very problem that the APA highlights. *See* Oshima at 1:14-23 (“With the steady advance of the integration rate of semiconductor integrated circuits, the integrated circuits have become more and more microminiaturized . . . . As a result, the proportion of the wiring capacitance to the capacitance load of the respective circuit signals has increased.”) (Ex. 1118). Oshima explains that “since the suppression of an increase of the wiring capacitance relates to a problem of the manufacturing cost . . . this problem is particularly serious in the field of complicated logic circuits, and specially ordered memory circuits which require high speed operation.” Oshima at 2:29-34 (Ex. 1118). Bravman Decl. ¶ 114 (Ex. 1101).

To address this problem, Oshima teaches one skilled in the art how to achieve decreased capacitance. Oshima is primarily directed to “a semiconductor integrated circuit suitable for high operation speed through a reduction of the wiring capacitance.” Oshima at 1:5-10 (Ex. 1118). Oshima teaches that providing the **oxide film 12** (the “dielectric film” of claim 6) or the **polysilicon film 9** (the “resistor film” of claim 13) can lead to a reduction in the overall capacitance. *See* Oshima at 5:37-44 (“As a result . . . the thickness of the interlayer film 6 formed between the

semiconductor substrate 8 and the bus line region wiring layer 7 can be increased . . . . Therefore, it is possible to markedly reduce the wiring capacitance . . . .”), 6:43-64 (“it is possible to reduce the capacitance C, as compared with the conventional structure having no floating terminal between the bus line region wiring layer 7 and the semiconductor substrate 8.”) (Ex. 1118). Bravman Decl. ¶ 114 (Ex. 1101).

Oshima utilizes a particular arrangement of the **oxide film 12** to lower the overall capacitance using fundamental, well-known characteristics of a capacitor—*e.g.*, increasing the distance between electrodes, or reducing the charge collected on the “plates” of a capacitor, leads to a reduction in capacitance. *See supra* § VI.C. A POSITA therefore would have understood combining the **oxide film 12** or **polysilicon film 9** disclosed in Oshima with the structures disclosed in APA to be a routine modification, leading to expected results. Bravman Decl. ¶ 115 (Ex. 1101).

Alternatively to integrating Oshima’s **oxide film 12** (claim 6) or **poly silicon layer 9** (claim 13) into the APA, as explained in Section X.A.1.c), it also would have been obvious to a POSITA at the time of the invention of the ’736 patent to replace Oshima’s **field oxide film 4** with a combination of **trench portions 8** and **dummy semiconductor portions 9** because, *inter alia*, it avoids the “bird’s beak” effect, improves planarization, and reduces pattern dependence. Bravman Decl. ¶ 116 (Ex. 1101).

*h) Additional Reasons to Combine*

As explained above, the APA teaches *all* of the claim limitations *except* for “a **dielectric film** interposed between at least said **dummy semiconductor portions** of said **isolation region** and said **interlayer insulating film**” (claim 6) and “a **resistor film** formed under said **wire**, and between said **interlayer insulating film** and at least said **dummy semiconductor portions** of said **isolation region**” (claim 13). *See supra* § IX.A. Oshima provides disclosure of these final limitations. As explained above, Oshima teaches that providing the **oxide film 12** or the **polysilicon film 9** can lead to a reduction in the overall capacitance. *Compare, e.g.*, Oshima at 5:37-44 (“As a result . . . the thickness of the interlayer film 6 formed between the semiconductor substrate 8 and the bus line region wiring layer 7 can be increased . . . . Therefore, it is possible to markedly reduce the wiring capacitance . . . .”), 6:43-64 (“it is possible to reduce the capacitance C, as compared with the conventional structure having no floating terminal between the bus line region wiring layer 7 and the semiconductor substrate 8.”) (Ex. 1118) *with* ’736 patent at 3:7-13 (“In the case where a member interposed between the wiring and substrate is composed of a homogenous material, the wiring-to-substrate capacitance per unit area is inversely proportional to the distance between the wiring and the substrate . . . .”), 24:34-43 (“[T]he distance between the wiring and the substrate is longer than in the conventional semiconductor device shown in FIG. 19. Since the wiring-to-substrate

capacitance decreases in inverse proportion to the distance, the wiring-to-substrate capacitance is reduced . . . .”) (Ex. 1103). A POSITA would have been motivated to add either the **oxide film 12** or the **polysilicon film 9** described in Oshima to the APA structure to achieve a significant reduction in capacitance. Bravman Decl. ¶ 117 (Ex. 1101).

Both APA and Oshima discuss the undesirable effects of increased capacitance as miniaturization occurs, which leads to slower operating frequency. The APA explains that one side-effect of such miniaturized structures shown in FIG. 19 is that the **wire-to-substrate** capacitance ends up being higher than the structures that utilize LOCOS. *See* ’736 patent at 2:50-3:30 (“Although the formation of the island pattern composed of the dummy semiconductor portions in the isolation region has the advantage of achieving planarization with excellent in-plane uniformity, it also has the possibility of increasing the **wiring-to-substrate** capacitance and resultantly reducing the operating speed of the semiconductor device.”) (Ex. 1103). In other words, APA admits that the undesirable effect of increasing **wiring-to-substrate** capacitance as a result of miniaturization was well-known. Moreover, the other benefits of using STI over LOCOS were also well-known to persons of ordinary skill at the time of the invention of the ’736 patent. *See supra* § VI.B. Bravman Decl. ¶ 118 (Ex. 1101).

Likewise, Oshima states that “the wiring capacitance of the **bus line region** is reduced, so that operation speed can be increased, the power consumption can be decreased, ***and the chip size can be reduced.***” Oshima at Abstract; *see also id.* at 2:19-28 (Ex. 1118). It was thus well-known that an “the suppression of an increase of the wiring capacitance” was “particularly serious.” Oshima at 2:29-34 (Ex. 1118). Indeed, Oshima states that its invention makes it possible “to markedly reduce the wiring capacitance down to about 12 to 25% of that of the conventional integrated circuit . . . .” Oshima at 5:41-44 (Ex. 1118). Bravman Decl. ¶ 119-20 (Ex. 1101).

As such, a POSITA would have been motivated to employ the capacitance-reducing scheme of Oshima in the APA structure. Oshima utilizes a particular arrangement of a **oxide film 12** or **polysilicon film 9** in the **substrate** to either increase the distance between the wire and the substrate, or reduce charge collected by adding a capacitance in series, respectively—well-known capacitance models—to negate the negative effects associated with increased wiring-to-substrate capacitance. Combining Oshima’s **oxide film 12** or **polysilicon film 9** with the structures disclosed in APA would thus have been a routine modification leading to expected results in line with basic principles of electrical engineering. Bravman Decl. ¶ 121-22 (Ex. 1101).



2. Dependent Claim 7

Claim 7 is dependent on claim 6 and further requires that “said dielectric film is an underlying insulating film interposed between said interlayer insulating film and said dummy semiconductor portions and said second trench portion.” As explained above in Section X.A.1, the APA and Oshima disclose every element of claim 6. Bravman Decl. ¶ 123 (Ex. 1101).

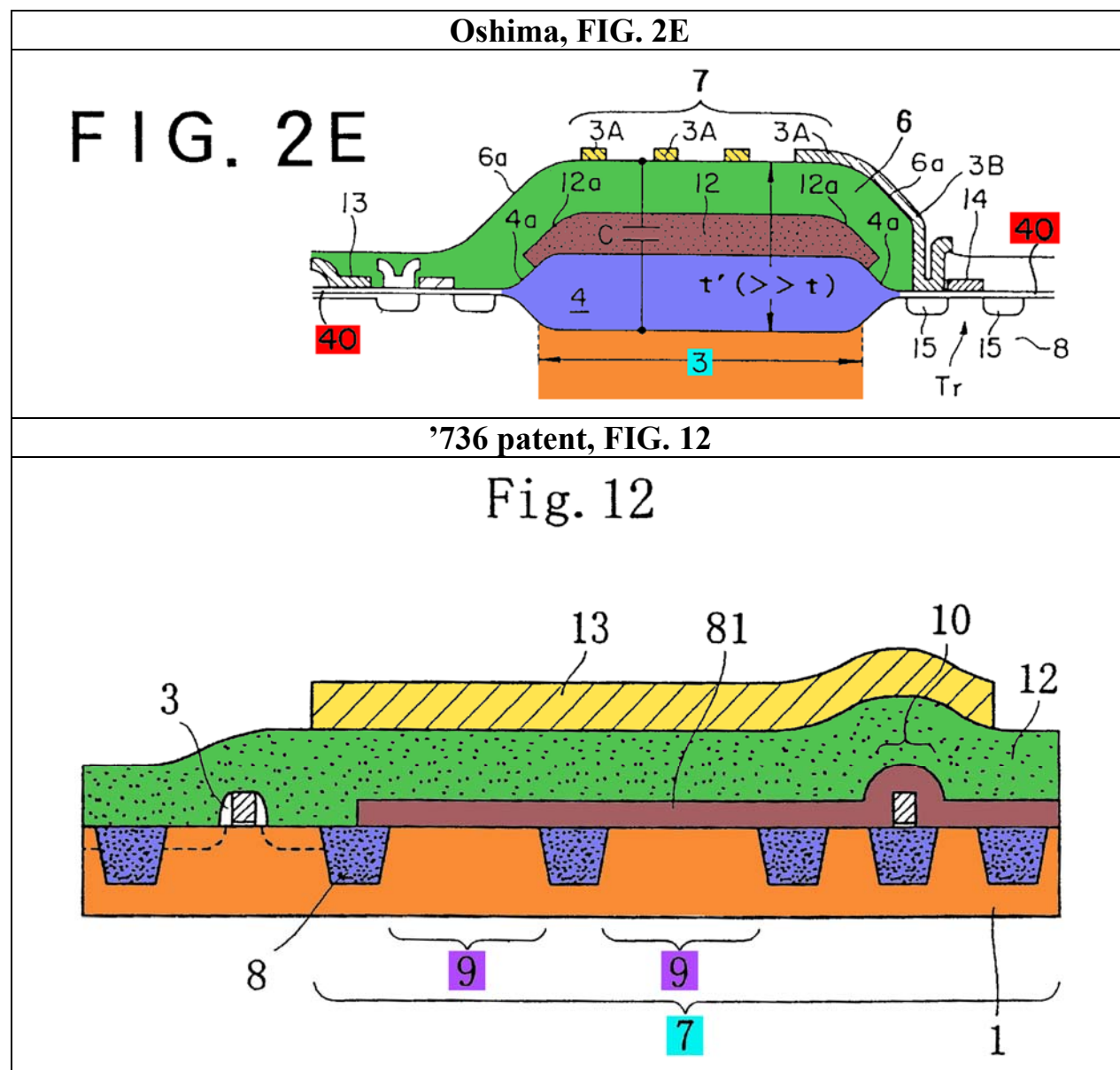
The ’736 patent specification notes that “FIG. 12 is a cross-sectional view of a semiconductor device . . . having . . . an **underlying insulating film** formed beneath an **interlayer insulating film**.” ’736 patent at 10:58-61 (Ex. 1103). As shown, the “**underlying insulating film 81**” is lying under the **interlayer insulating film 12** and is interposed between the **interlayer insulating film 12** and the **isolation region 7**, which includes the **dummy semiconductor portions 9** and the **trench portions 8**.

Just like the ’736 patent, Oshima discloses an **oxide film 12** that lies under the **interlayer film 6** and is interposed between the **interlayer film 6** and the **field oxide film 4** in the **bus line region 3**. Oshima at 4:47-6:33; 5:13-20 (Ex. 1118). A POSITA would have found it obvious to incorporate Oshima’s **oxide film 12** into the APA, as discussed above. Such an incorporation would have the oxide film 12 be an underlying film between the **interlayer insulating film 12** and the **dummy**

**semiconductor portions** and **second trench portions**, as this claim element requires. Bravman Decl. ¶ 124 (Ex. 1101).

Or, as explained above with respect to claim 6, replacing Oshima's **field oxide film 4** in the **bus line regions 3** with **trench portions 8** and **dummy semiconductor portions 9** would have been obvious to a POSITA. *See supra* § X.A.1.c)i). Bravman Decl. ¶ 125 (Ex. 1101).

The APA combined with Oshima thus discloses claim 7 of the '736 patent. Bravman Decl. ¶ 126 (Ex. 1101).

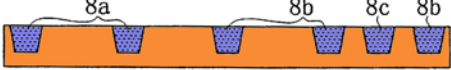

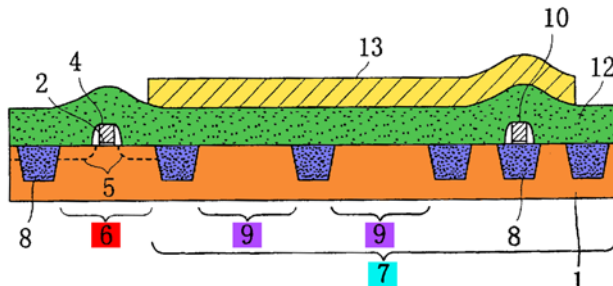

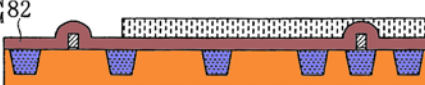
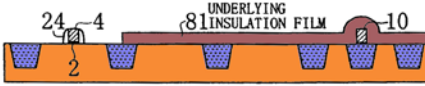
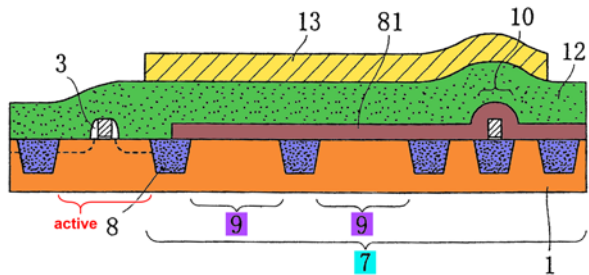


### 3. Dependent Claim 8

Claim 8 is dependent on claim 7 and further requires “a gate electrode formed on the semiconductor substrate within said active region and sidewalls made of an insulating material and formed on both side faces of said gate electrode, wherein said underlying insulating film is formed of the same film as forming said sidewalls.”

As explained above in Section X.A.2, the APA and Oshima disclose every element of claim 7. Bravman Decl. ¶ 127 (Ex. 1101).

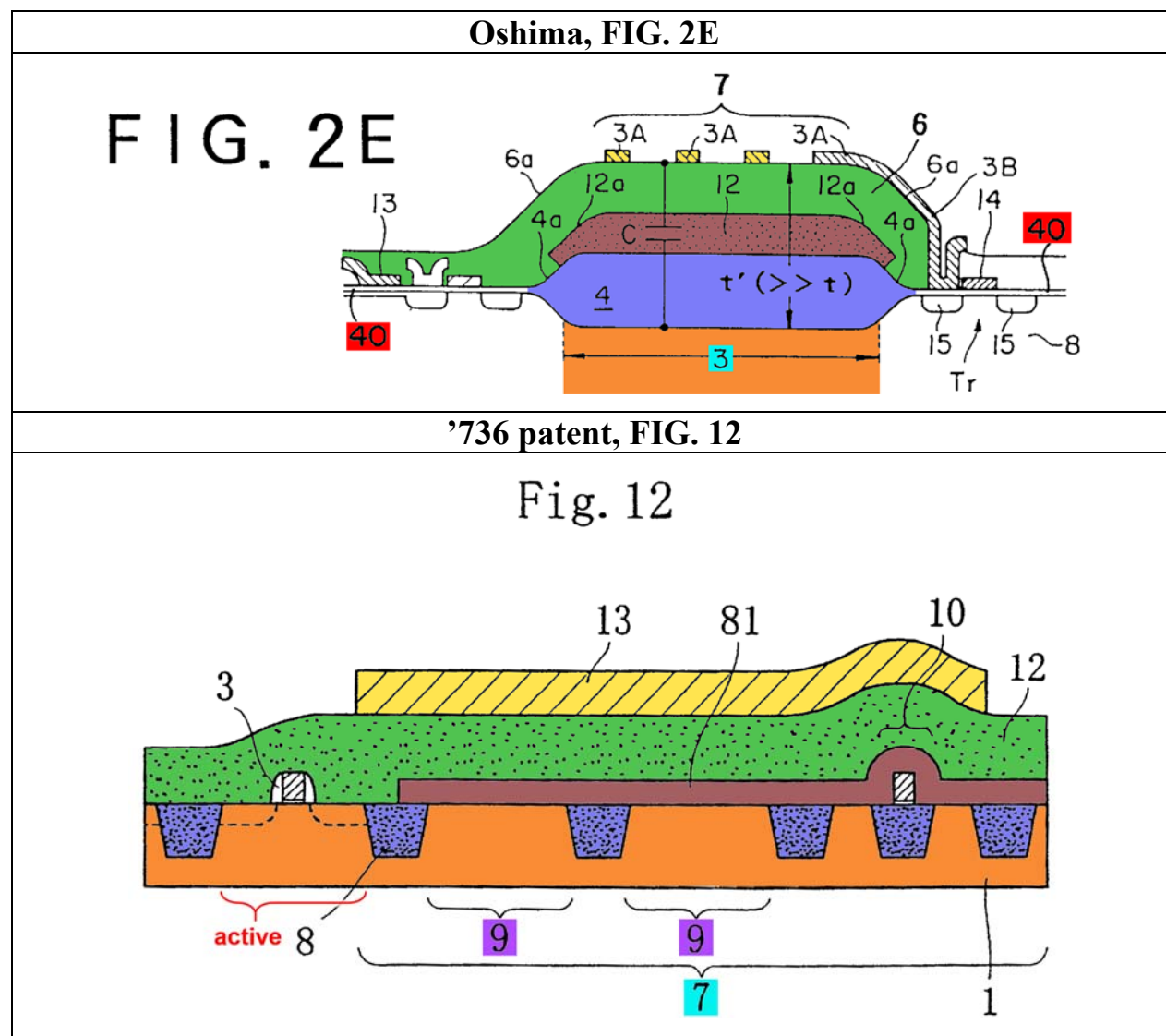
The APA discloses a gate electrode in the active region formed with sidewalls on both side faces. The '736 patent refers to “a gate electrode 4” in the active region of the semiconductor device of APA FIG. 19. *See* '736 patent at 1:38-40 (Ex. 1103). The APA also includes sidewalls on both side faces of the gate electrode; the sidewalls are unlabeled in APA FIG. 19, but they are labeled using numeral 24 in APA FIG. 20(g), which is a step in the manufacturing process of the semiconductor device in APA FIG. 19. *See* '736 Patent at FIG. 19, 20(e) (describing “sidewalls 24” during the manufacturing process of APA FIG. 19 “using a known technique”), 2:26-29. Such a “known technique” of creating sidewalls 24 included creating them from a silicon oxide. Bravman Decl. ¶¶ 128-29 (Ex. 1101).

APA, FIGS. 19, 20(d) and 20(e)	'736 patent, FIGS. 12, 13(e), 13(f) and 13(g)
<p>Fig. 20(d) PRIOR ART</p>  <p>Fig. 20(e) PRIOR ART</p>  <p>Fig. 19 PRIOR ART</p> 	<p>Fig. 13(e)</p>  <p>Fig. 13(f)</p>  <p>Fig. 13(g)</p>  <p>Fig. 12</p> 

The semiconductor device of APA FIG. 19, however, does not disclose the underlying insulating film 81. But combining such an underlying insulating film into the semiconductor structure of APA would have been known. *See supra* §§ X.A.1.f), X.A.1.h) and X.A.2. Bravman Decl. ¶ 130 (Ex. 1101).

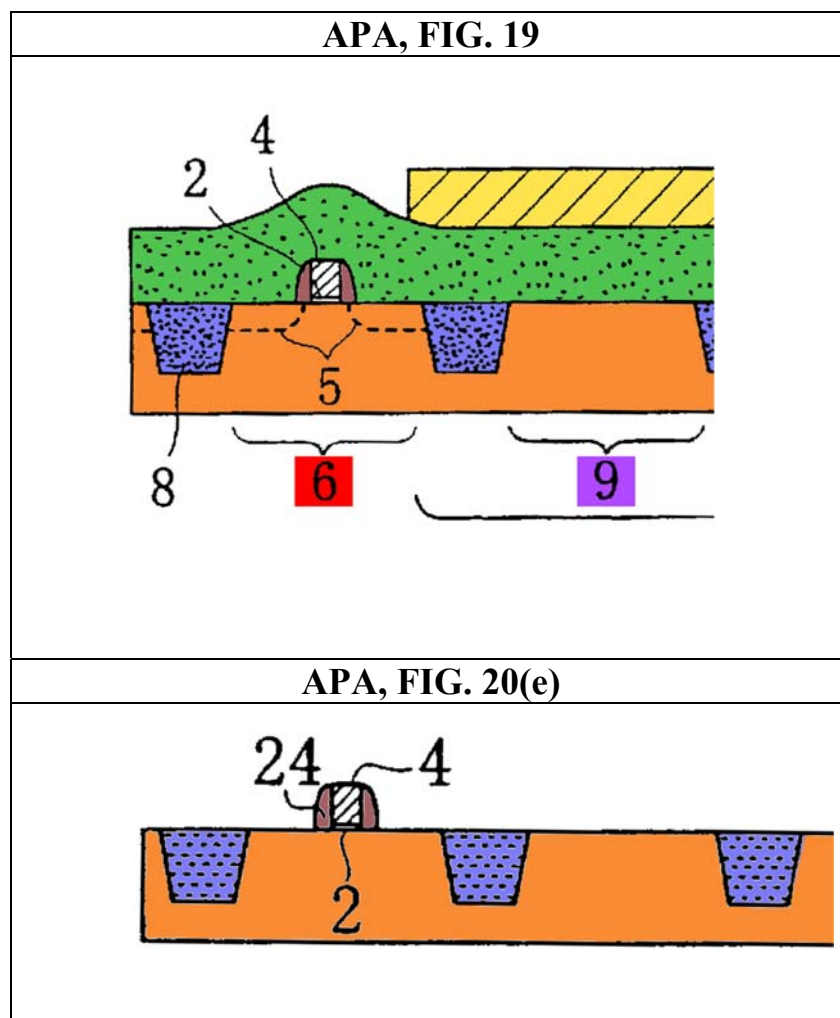
Alternatively, it would have been obvious to modify Oshima to disclose this claim element. As explained above with respect to claim 6, Oshima teaches an active region by disclosing “**circuit block regions 2, indicated by reference numeral 40.**” *See* Oshima at 4:63-5:3 (Ex. 1118). Oshima further discloses a gate electrode. Oshima at 4:63-5:3 (Ex. 1118) (“gate electrodes 14 of transistors . . . in

the **circuit block region (i.e., active region) 2 . . . .**”). Bravman Decl. ¶ 131 (Ex. 1101).



Although sidewalls are not explicitly shown in Oshima, such structures were well known to a POSITA. For example, APA discloses that “an **active region 6** of a P-type silicon substrate 1 is formed with . . . a gate electrode 4 made of a polysilicon film . . . .” ’736 patent at 1:38-41 (Ex. 1103). Sidewalls are shown in APA FIG. 19 as elements positioned to the left and right of gate electrode 4. The **sidewalls** of

APA FIG. 19 are not labelled by a reference numeral. APA FIG. 20(e), however, shows that these elements positioned to the left and right of gate electrode 4 are **sidewalls 24**. '736 patent at 2:26-29 (“there are formed . . . the gate electrode 4 having **sidewalls 24** on the side faces thereof . . . *by using a known technique.*”) (Ex. 1103). Including sidewalls was standard practice at the time of the invention of the '736 patent, and it would not have materially contributed to the complexity of manufacturing semiconductors. A POSITA would have been aware of the benefits of including sidewalls, such as allowing fabrication of “lightly doped drain” regions, and thus contributing to the reliability of semiconductors through the reduction of “hot carrier” effects. *See also* U.S. Patent No. 4,786,609 (“Chen”) at Abstract, FIG. 1j, 1:13-58 (describing sidewalls and reasons for implementing them) (Ex. 1122). Bravman Decl. ¶ 132-33 (Ex. 1101).



Therefore, the APA and Oshima disclose this element and invalidate claim 8.

Bravman Decl. ¶ 134 (Ex. 1101).

#### 4. Dependent Claim 9

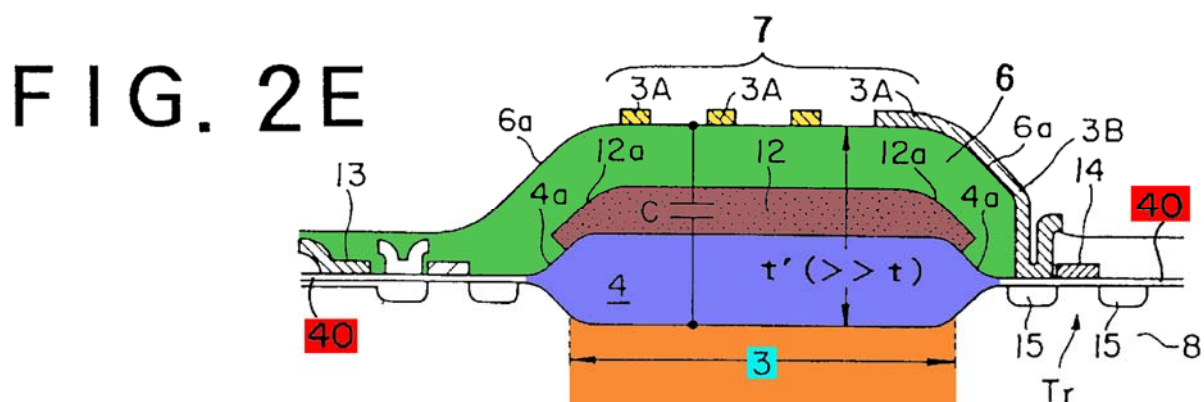
Claim 9 is dependent on claim 8, which is dependent on claim 7. Claim 9 further requires that “said underlying insulating film is composed of a multilayer film.” As explained above in Section X.A.3, the APA and Oshima disclose every element of claim 8. Bravman Decl. ¶ 135 (Ex. 1101).



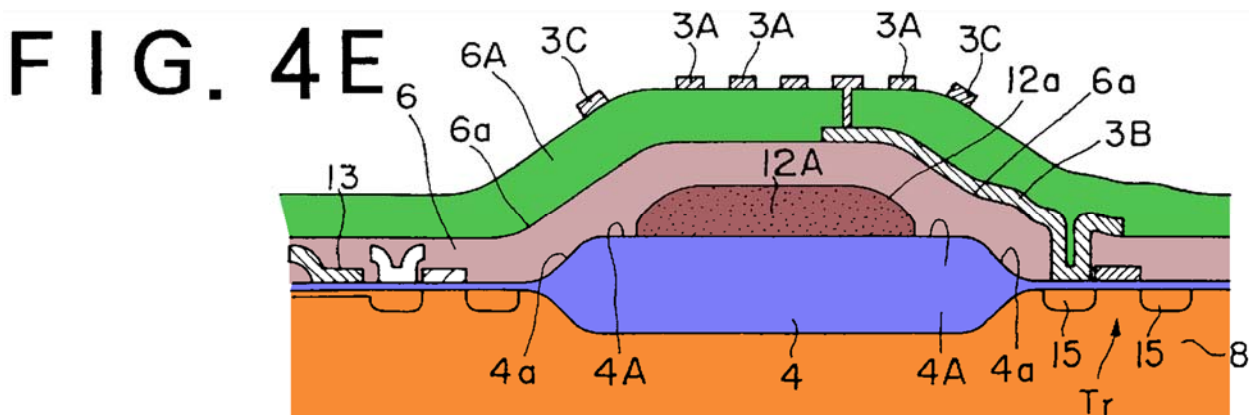
As shown in FIG. 4E, Oshima discloses another embodiment where an *additional insulating film 6* is added above the **oxide film 12A**. Oshima at 7:7-9 (Ex. 1118). This *additional insulating film*, in conjunction with **oxide film 12A**, corresponds to the claimed multilayer film. Oshima thus discloses this limitation, and the APA in combination with Oshima discloses claim 9 of the '736 patent.

Bravman Decl. ¶ 136 (Ex. 1101).

**Oshima, FIG. 2E**



Oshima, FIG. 4E



5. Dependent Claim 11

Claim 11 is dependent on claim 6 and further requires that “said dielectric film is composed of at least one of a silicon oxide film and a silicon nitride film.” As explained above in Section X.A.1, the APA and Oshima disclose every element of claim 6. Bravman Decl. ¶ 137 (Ex. 1101).

Oshima discloses “the **poly silicon layer 9** is oxidized into an **oxide film 12**.” Oshima at 5:13-14 (Ex. 1118). In other words, because **oxide film 12** is formed by the reaction of oxygen and silicon, it is a silicon oxide film. Oshima thus discloses this limitation, and the APA in combination with Oshima discloses claim 11 of the ’736 patent. Bravman Decl. ¶¶ 138-39 (Ex. 1101).

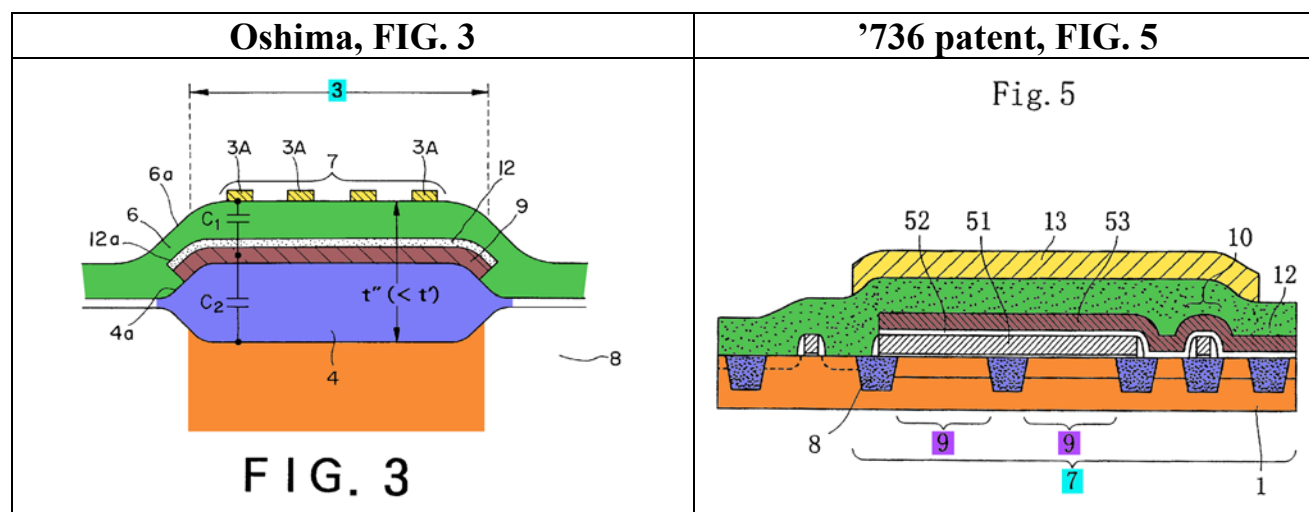
6. Dependent Claim 14

Claim 14 is dependent on claim 13 and further requires that “said resistor film is an underlying resistor film formed to extend continuously over said dummy semiconductor portions and said second trench portions.” As explained above in Section X.A.1, the APA and Oshima disclose every element of claim 13. Bravman Decl. ¶ 140 (Ex. 1101).

Just like claim 14 of the ’736 patent, Oshima discloses a **poly silicon layer 9** that is beneath the **interlayer film 6** in Fig. 3. *See* Oshima at 6:34-64 (Ex. 1118). Moreover, the **poly silicon layer 9** in Fig. 3 extends continuously over the **field oxide film 4** in the **bus line regions 3**. A POSITA would have found it obvious to

incorporate Oshima's **poly silicon layer 9** into the APA, as discussed above. Such an incorporation would have the poly silicon layer 9 extend continuously over the **dummy semiconductor portions** and **second trench portions**, as this claim element requires. Bravman Decl. ¶ 141 (Ex. 1101).

Or, as explained above with respect to claim 13, it would have been obvious to a POSITA to replace Oshima's **field oxide film 4** in the **bus line region 3** with **trench portions 8** and **dummy semiconductor portions 9**, or to incorporate Oshima's **polysilicon film 9** into the APA. *See supra* §§ X.A.1.g)i), X.A.1.h). Accordingly, the APA in combination with Oshima discloses claim 14 of the '736 patent. Bravman Decl. ¶¶ 142-43 (Ex. 1101).



## 7. Dependent Claim 16

Claim 16 is dependent on claim 14 and further requires “an element having an electrode member composed of a conductor film formed on the semiconductor substrate within said active region, wherein said resistor film is composed of the

same material as composing said electrode member.” As explained above in Section X.A.6, the APA and Oshima disclose every element of claim 14. Bravman Decl. ¶¶ 144 (Ex. 1101).

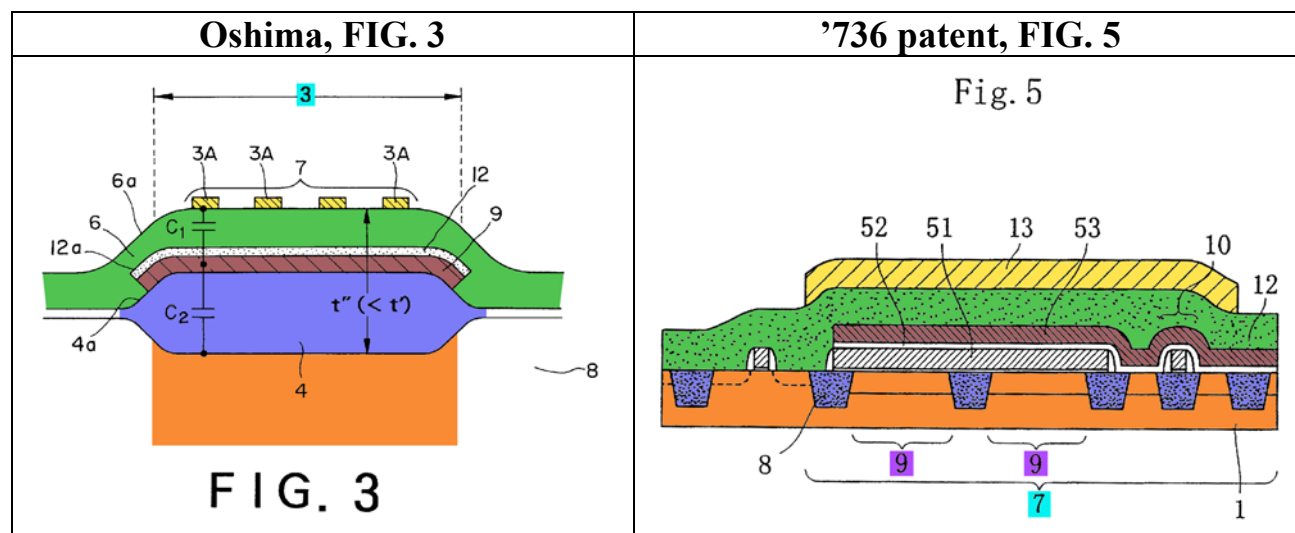
As explained above with respect to claim 13, Oshima teaches that “a **poly silicon layer 9** is formed . . . all over the surface of the entire **field oxide film 4**, in order to form *plate electrodes 13* of memory cells and *gate electrodes 14* of the transistors (both shown in FIG. 2(E)) in the **circuit block region (i.e., active region) 2 . . . .**” Oshima at 4:63-5:3 (Ex. 1118). In other words, Oshima teaches “**circuit block regions 2, indicated by reference numeral 40**” that include electrode 13 or 14. *See id.* at FIG. 2E (Ex. 1118). These electrodes 13 or 14 are formed from the same material as the **poly silicon layer 9** shown in FIG. 3 of Oshima. *Id.* at 4:63-5:3. Accordingly, Oshima teaches this limitation, and the APA in combination with Oshima discloses claim 16 of the ’736 patent. Bravman Decl. ¶¶ 145-46 (Ex. 1101).

[illegible]

## 8. Dependent Claim 20

Claim 20 is dependent on claim 13 and further requires that “said resistor film is composed of at least one of a polysilicon film and an amorphous silicon film.” As explained above in Section X.A.1, the APA and Oshima disclose every element of claim 13. Bravman Decl. ¶ 147 (Ex. 1101).

Oshima discloses a “**poly silicon film 9.**” Oshima at 6:37-42 (Ex. 1118). Accordingly, Oshima teaches the resistor film to be “composed of at least . . . a polysilicon film,” and thus Oshima discloses this limitation, and the APA in combination with Oshima discloses claim 20 of the ’736 patent. *Id.* Bravman Decl. ¶ 148 (Ex. 1101).



## XI. CONCLUSION

The Petitioner requests institution of an IPR and cancellation of the Challenged Claims.

Dated: March 7, 2018

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Petition for *Inter Partes* Review of U.S. Patent No. 6,346,736

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**Table of Exhibits for U.S. Patent 6,346,736 Petition  
for Inter Partes Review**

<b>Exhibit</b>	<b>Description</b>
1101	Declaration of Dr. John C. Bravman
1102	<i>Curriculum Vitae</i> of Dr. John C. Bravman
1103	U.S. Patent No. 6,346,736
1104	File History of U.S. Patent No. 6,346,736 (“File History”)
1105	Assignment History U.S. Patent No. 6,346,736
1106	Saraswat and Mohammadi, “Effect of scaling of interconnections on the time delay of VLSI circuits,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. SC-17, No. 2, April 1982, pp. 275-280 (“Saraswat”)
1107	Sedra, Adel S., <i>Microelectronics Circuits</i> , Oxford University Press, Inc. (3 <sup>rd</sup> 3d., 1991)
1108	U.S. Patent No. 5,107,320 (“Iranmanesh”)
1109	Dorf and Tallarida, <i>Pocket Book of Electrical Engineering Formulas</i> , CRC Press, p. 148 (1993)
1110	Uyemura, <i>Fundamentals of MOS Digital Integrated Circuits</i> , Addison-Wesley Publishing Co, pp. 263-273 (1988)
1111	U.S. Patent No. 4,519,128 (“Chesebro”)
1112	U.S. Patent No. 4,571,819 (“Rogers”)
1113	U.S. Patent No. 5,702,976 (“Schuegraf”)
1114	U.S. Patent No. 4,957,590 (“Douglas”)
1115	U.S. Patent No. 5,976,939 (“Thompson”)
1116	U.S. Patent No. 6,165,826 (“Chau”)
1117	U.S. Patent No. 5,733,812 (“Ueda”)
1118	U.S. Patent No. 5,814,848 (“Oshima”)
1119	Moore, Gordon E. “Cramming More Components Onto Integrated Circuits.” <i>Electronics</i> , vol. 38, no. 8, Apr. 19, 1965 (“Moore”)
1120	Appels, J. A., et al. “Some Problems of MOS Technology.” <i>Philips Technical Review</i> , vol. 31, nos. 7/8/9, 1970 (“Appels”)



Petition for *Inter Partes* Review of U.S. Patent No. 6,346,736

<b>Exhibit</b>	<b>Description</b>
1121	U.S. Patent No. 4,960,725 (“Noguchi”)
1122	U.S. Patent No. 4,786,609 (“Chen”)
1123	Panasonic Press Release, “Matsushita Electric Becomes Panasonic Corporation” October 1, 2008, Available at <a href="http://news.panasonic.com/global/press/data/en081001-4/en081001-4.html">http://news.panasonic.com/global/press/data/en081001-4/en081001-4.html</a>

**CERTIFICATE OF COMPLIANCE**

I hereby certify that the foregoing, Petition for Inter Partes Review of U.S. Patent No. 6,346,736, contains **12,543** words as measured by the word processing software used to prepare the document, in compliance with 37 C.F.R. § 42.24(d).

Dated: March 7, 2018

Respectfully submitted,

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**CERTIFICATE OF SERVICE**

The undersigned hereby certifies that a copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,346,736 was served on March 7, 2018, via FedEx delivery directed to counsel of record for the patent at the following address:

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