

FILE HISTORY

US 6,130,139

PATENT: 6,130,139

INVENTORS: Ukeda, Takaaki

Kudo, Chiaki

Yabu, Toshiki

TITLE: Method of manufacturing trench-isolated
semiconductor device

APPLICATION
NO: US1997978137A

FILED: 25 NOV 1997

ISSUED: 10 OCT 2000

COMPILED: 29 AUG 2014

70579 U.S. PTO
08/978137

11/25/97	425	426
Class	Subclass	Issue Classification

SCANNED

6130139

UTILITY SERIAL NUMBER	PATENT DATE OCT 10 1998	PATENT NUMBER 6130139
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SERIAL NUMBER 08/978,137	FILING DATE 11/25/97	CLASS 257 438	SUBCLASS 724	GROUP ART UNIT 2826	EXAMINER K. D. [Signature]
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APPLICANTS TAKAOKI UKEDA, OSAKA, JAPAN; CHIAKI KUDO, KYOTO, JAPAN; TOSHIKI YABU, OSAKA, JAPAN.

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CONTINUING DATA
VERIFIED
KBD

FOREIGN APPLICATIONS
VERIFIED JAPAN 8-314762 11/26/96
JAPAN 9-023844 02/06/97
KBD

Foreign priority claimed 35 USC 119 conditions met	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no	AS FILED	STATE OR COUNTRY JPN	SHEETS DRWGS. 21	TOTAL CLAIMS 38	INDEP. CLAIMS 12	FILING FEE RECEIVED \$1,924.00	ATTORNEY'S DOCKET NO. 43889-677
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VERIFIED AND ACKNOWLEDGED
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Edward E. Kubasiewicz, ESQ
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Washington DC 20005-3096

TITLE
REPRODUCIBLE DEVICE AND METHOD OF MANUFACTURING THE SAME
METHOD OF MANUFACTURING TRENCH-ISOLATED SEMICONDUCTOR DEVICE
U.S. DEPT. OF COMM./PAT. & TM - PTO-436L (Rev. 12-98)

PARTS OF APPLICATION FILED SEPARATELY		Applications Examiner [Signature]	
NOTICE OF ALLOWANCE MAILED 10-1-99		CLAIMS ALLOWED Total Claims 20 Print Claim 19	
ISSUE FEE Amount Due 1200 Date Paid 12/10/99		DRAWING Sheets Drwg. 21 Figs. Drwg. 89 Print Fig. 11a)	
Label Area		ISSUE BATCH NUMBER C61	
PREPARED FOR ISSUE			
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Form PTO-436A
(Rev. 8/92)

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Formal Drawings (5 sheets)

ISSUE FEE IN FILE

(FACE)

6,130,139

METHOD OF MANUFACTURING TRENCH-ISOLATED SEMICONDUCTOR DEVICE

Transaction History

Date	Transaction Description
12-14-1997	Initial Exam Team nn
01-06-1998	Request for Foreign Priority (Priority Papers May Be Included)
03-04-1998	IFW Scan & PACR Auto Security Review
03-17-1998	Application Dispatched from OIPE
03-26-1998	Case Docketed to Examiner in GAU
05-22-1998	Information Disclosure Statement (IDS) Filed
05-22-1998	Information Disclosure Statement (IDS) Filed
01-21-1999	Mail Restriction Requirement
01-21-1999	Restriction/Election Requirement
02-01-1999	Correspondence Address Change
02-16-1999	Response to Election / Restriction Filed
02-18-1999	Date Forwarded to Examiner
03-04-1999	Case Docketed to Examiner in GAU
05-05-1999	Non-Final Rejection
05-10-1999	Mail Non-Final Rejection
09-09-1999	Response after Non-Final Action
09-09-1999	Request for Extension of Time - Granted
09-15-1999	Date Forwarded to Examiner
10-01-1999	Mail Notice of Allowance
10-01-1999	Notice of Allowance Data Verification Completed
11-03-1999	Workflow - Drawings Finished
11-03-1999	Workflow - Drawings Matched with File at Contractor
11-03-1999	Workflow - Drawings Received at Contractor
11-03-1999	Workflow - Drawings Sent to Contractor
11-04-1999	Workflow - Drawings Received at Contractor
11-17-1999	Workflow - File Sent to Contractor
12-10-1999	Issue Fee Payment Verified
12-10-1999	Workflow - Incoming Correspondence - Finish
12-10-1999	Workflow - Incoming Correspondence - Begin
12-10-1999	UnMatched Papers in Pubs
12-10-1999	Workflow - Drawings Sent to Contractor
04-27-2000	Correspondence Address Change
08-10-2000	Workflow - Complete WF Records for Drawings
09-14-2000	Application Is Considered Ready for Issue
09-21-2000	Issue Notification Mailed
10-10-2000	Recordation of Patent Grant Mailed

70579 U.S. PTO
08/978137



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PATENT APPLICATION



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CONTENTS

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INITIALS _____

Date
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Mailed

1.	Application	21	papers.	
2.	Priority Document			1-6-98
3.	OPR			4-17-98
4.	IDS			5-22-98
1-21-99 TIT	5.	restriction		1-21-99
2/18/99	6.	Election		2-10-99
FS 5-5	7.	Non-Final Rpt (3 mos)		5-10-99 TIT
9-15-99	8.	EXT OF TIME		9-9-99
9-15-99	9.	Amend A / drawings		9-9-99
10/1/99	10.	PTOL-37		10-1-99
10/13/99	11.	Change of Address		2/1/99
4/14/00	12.	Formal Drawings (21 sheets) set		1/3/99
4-27-00	13.	Change of Address		4-27-00 12/10/99
9-7-00	14.	Rule 312 amend B		11/4/99
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STAPLE AREA

U.S. GOVERNMENT PRINTING OFFICE: 1987-430-220

PATENT NUMBER

ORIGINAL CLASSIFICATION

CLASS 438 SUBCLASS 424

APPLICATION SERIAL NUMBER

08/978,137

CROSS REFERENCE(S)

CLASS 438 SUBCLASS 414 353 360 425

APPLICANT'S NAME (PLEASE PRINT)

UKEDA ET AL.

IF REISSUE, ORIGINAL PATENT NUMBER

INTERNATIONAL CLASSIFICATION

H 01 L 21 / 76

GROUP ART UNIT

2822

ASSISTANT EXAMINER (PLEASE STAMP OR PRINT FULL NAME)

KHANH DUONG

PRIMARY EXAMINER (PLEASE STAMP OR PRINT FULL NAME)

Carl Whitehead Jr.

PTO 270 (REV. 5-81)

ISSUE CLASSIFICATION SLIP

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

Claim	Date
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SYMBOLS
 ✓ Rejected
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 I Interference
 A Appeal
 D Obsolete

Claim	Date
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POSITION	ID NO.	DATE
CLASSIFIER	11	2/11/98
EXAMINER	69482	3-11-98
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INDEX OF CLAIMS

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Claim	Date
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SYMBOLS

✓ Rejected
 ✗ Allowed
 (Through number) Contested
 N Restricted
 I Non-elected
 A Interference
 O Appeal
 O Objected

SEARCHED			
Class	Sub.	Date	Exmr.
438	414	4/24/99	KBD
↓	424	↓	↓
	423		
	427		
438	353	4/28/99	KBD
↓	354	↓	↓
	355		
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	360		
	370		
	404 ✓		
	412		
	413		
	405		
↓	425	↓	↓
Update		9/30/99	KBD

SEARCH NOTES		
	Date	Exmr.
USPAT IS & R	4/26/99 4/27/99 4/28/99	KBD ↓ KBD
USPAT	4/29/99	KBD

INTERFERENCE SEARCHED			
Class	Sub.	Date	Exmr.
438	414	9/30/99	KBD
↓	424	↓	↓
	353		
	404		
	425		

(FILE 'USPAT' ENTERED AT 10:05:52 ON 29 APR 1999)

L1 8 S IMPLANT? (5A) SUBSTRATE (5A) HIGH (W) RESIST?
L2 390121 S NITROGEN OR OXYGEN
L3 0 S L1 (P) L2
L4 2 S L1 AND L2
L5 802 S (IMPLANT? OR DOP?) (10A) HIGH (W) RESIST?
L6 69 S L5 (P) L2
L7 324016 S OXIDE
L8 8 S L6 (P) L7
L9 3646 S ISOLATION (W) (REGION OR PORTION)
L10 13 S L5 (P) L9
L11 2 S L10 AND L2
L12 3 S L6 AND L9
L13 274 S (IMPLANT? OR DOP?) (5A) L2 (8A) RESIST?
L14 11 S L9 AND L13
L15 52497 S NITROGEN (5A) OXYGEN
L16 325 S (IMPLANT? OR DOP?) (5A) L15
L17 176090 S (INCREAS? OR HIGH) (3A) RESIST?
L18 30 S L16 (P) L17
L19 5940 S L2 (P) L17
L20 8 S L19 (P) L9
L21 162977 S SEMICONDUCTOR
L22 22 S L16 (5A) L21.
L23 104 S L17 (10A) L15
L24 73 S L17 (7A) L15
L25 111 S L16 (5A) (SUBSTRATE OR SILICON)
L26 5 S L25 (7A) (RESIST?)

(FILE 'USPAT' ENTERED AT 13:11:55 ON 28 APR 1999)

L1	9	S	(IMPLANT? OR DOP?) (20A) (HIGH RESISTOR)
L2	2546	S	(POLYSILICON OR RESISTOR) (W) FILM
L3	119320	S	ISOLATION
L4	76	S	L2 (10A) L3
L5	501514	S	(INSULATING OR DIELECTRIC OR OXIDE)
L6	0	S	DUMMY SEMICONDUCTOR PORTION#
L7	8846	S	L5 (10A) L3
L8	1104	S	L5 (10A) L3 (W) REGION
L9	12987	S	TRENCH?
L10	189	S	L8 (P) L9
L11	12	S	L2 (10A) L3 (W) REGION
L12	7908	S	L5 (7A) L3
L13	1428	S	L12 (P) L9
L14	1013	S	L5 (8A) L3 (W) REGION
L15	173	S	L14 (P) L9
L16	109	S	L14 (10A) L9

(FILE 'USPAT' ENTERED AT 16:04:48 ON 27 APR 1999)

L1	12947 S TRENCH?
L2	390 S DUMMY(W) (GATE# OR ELECTRODE#)
L3	0 S INTER(W) TRENCH(W) INSULAT?
L4	2609 S (IMPLANT? OR DOP?) (5A) OXYGEN
L5	1122 S BURIED(5A) INSULATING
L6	10 S L1(P) L2
L7	63 S L1(P) L4
L8	5 S L7(P) L5

{FILE 'USPAT' ENTERED AT 10:04:23 ON 26 APR 1999}

L1 1311 S (IMPLANT? OR DOP?) (7A) (P(W)N)
L2 12923 S TRENCH?
L3 24 S L1(P)L2
L4 13341 S SOURCE(W)DRAIN
L5 4 S L1(10A)L4
L6 8 S L1(20A)L4
L7 8683 S P(W)N(W)JUNCTION#
L8 178 S L2(P)L7
L9 32 S BURIED(P)L8
L10 2113 S INTERLAYER(W)INSULATING
L11 2 S L8(P)L10
L12 (215792)S GATE
L13 144 S L12(P)L1
L14 1 S L13 AND L10



US006130139A

United States Patent [19][11] **Patent Number:** **6,130,139****Ukeda et al.**[45] **Date of Patent:** **Oct. 10, 2000**[54] **METHOD OF MANUFACTURING TRENCH-ISOLATED SEMICONDUCTOR DEVICE**

5,877,066 3/1999 Stolmeijer et al. 438/424

FOREIGN PATENT DOCUMENTS[75] Inventors: **Takaaki Ukeda**, Osaka; **Chiaki Kudo**, Kyoto; **Toshiki Yabu**, Osaka, all of Japan

0220500	9/1986	European Pat. Off. .
0538807	10/1992	European Pat. Off. .
58-200554	11/1983	Japan .
60-015944	1/1985	Japan .
63-246842	10/1988	Japan .
02272745	11/1990	Japan .
05013565	1/1993	Japan .

[73] Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka, Japan[21] Appl. No.: **08/978,137**[22] Filed: **Nov. 25, 1997**[30] **Foreign Application Priority Data**

Nov. 26, 1996	[JP]	Japan	8-314762
Feb. 6, 1997	[JP]	Japan	9-023844

[51] **Int. Cl.⁷** **H01L 21/76**[52] **U.S. Cl.** **438/424; 438/414; 438/353; 438/360; 438/425**[58] **Field of Search** 438/414, 424, 438/423, 427, 353, 354, 355, 356, 357, 359, 360, 370, 404, 412, 413, 405, 425[56] **References Cited****U.S. PATENT DOCUMENTS**

3,622,382	11/1971	Brack et al.	428/448
4,929,566	5/1990	Beitman	438/423
4,948,742	8/1990	Nishimura et al.	438/423
5,270,265	12/1993	Hemmenway et al.	438/404
5,426,062	6/1995	Ilwang	438/423
5,663,588	9/1997	Suzuki et al.	257/350
5,665,633	9/1997	Meyer	438/427
5,760,444	6/1998	Okumura	257/350
5,856,218	1/1999	Kinoshita et al.	438/414

Primary Examiner—Carl Whitehead, Jr.*Assistant Examiner*—Khanh Duong*Attorney, Agent, or Firm*—McDermott, Will & Emery[57] **ABSTRACT**

The top surface of a P-type semiconductor substrate is partitioned into an active region to be formed with an element and an isolation region surrounding the active region. The isolation region is composed of trench portions and dummy semiconductor portions. An interlayer insulating film is deposited on the substrate, followed by a wire formed thereon. In each of the semiconductor portions, an impurity diffusion layer is formed simultaneously with the implantation of ions into the element so that a PN junction is formed between the impurity diffusion layer and the silicon substrate. A capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions is obtained by adding in series the capacitance in the impurity diffusion layer to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the inter layer insulating film. What results is a semiconductor device having lower total wiring-to-substrate capacitance and a higher operating speed.

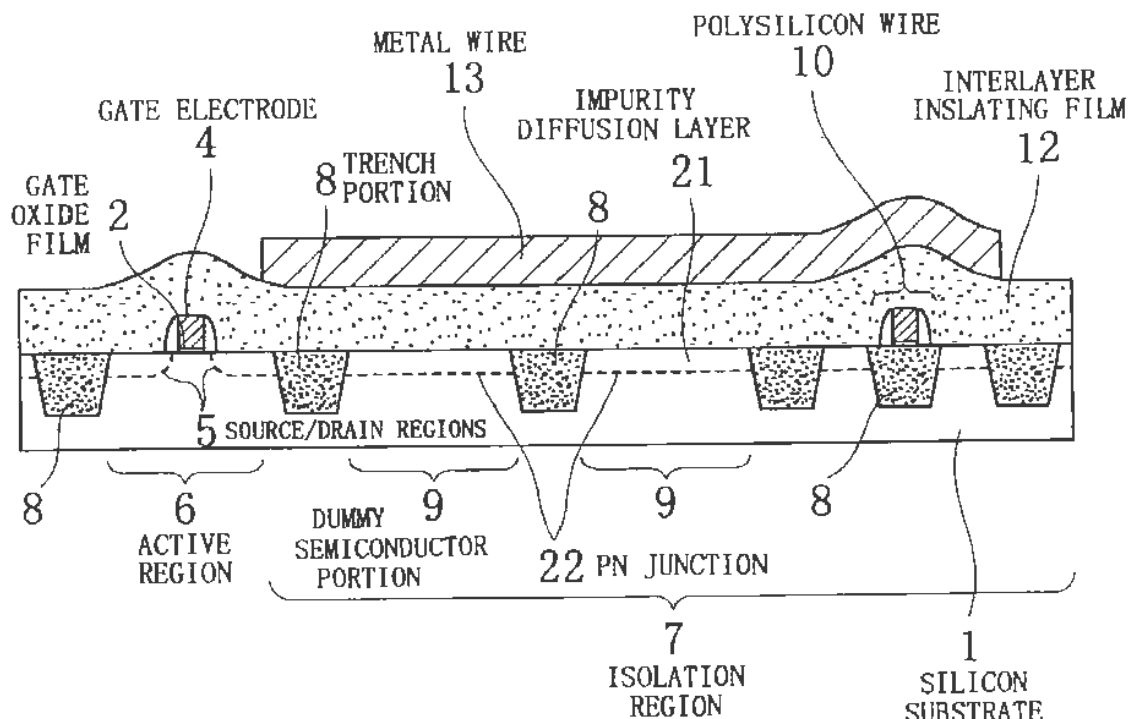
20 Claims, 21 Drawing Sheets

Fig. 1(a)

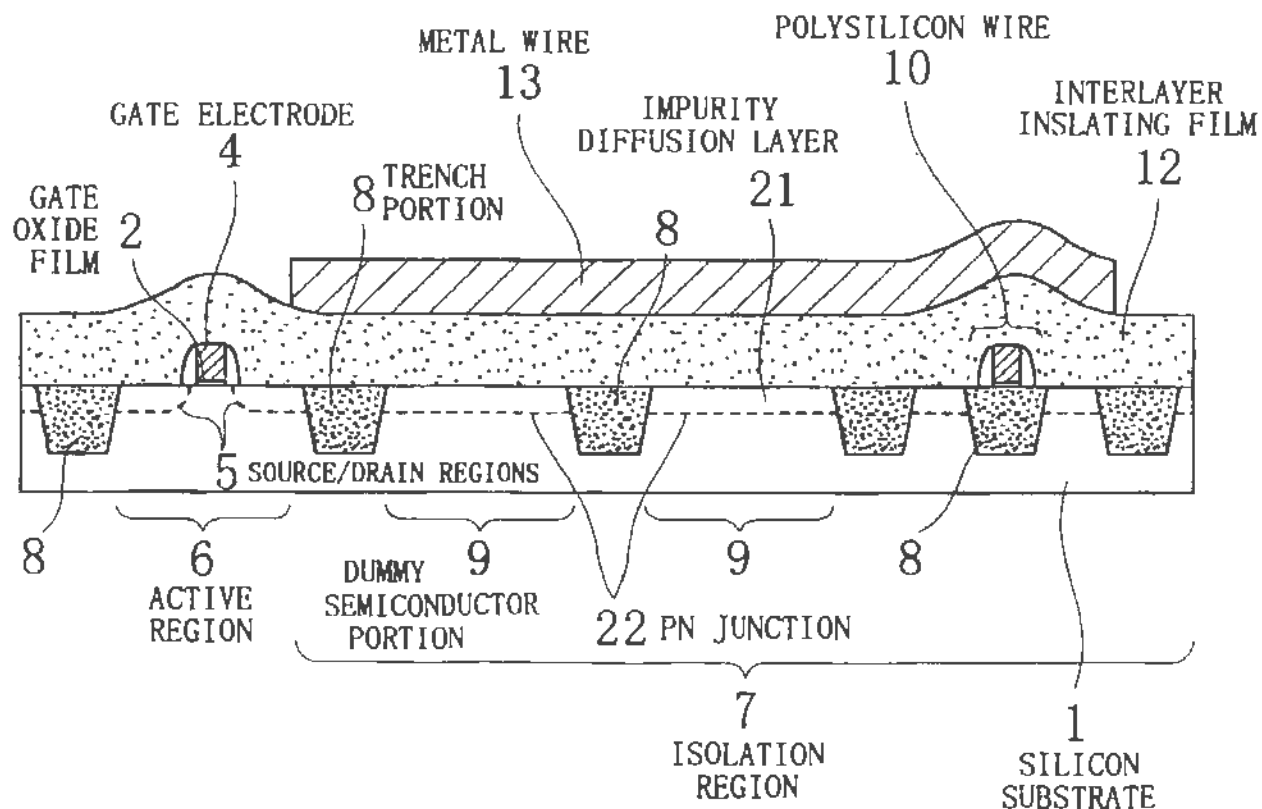
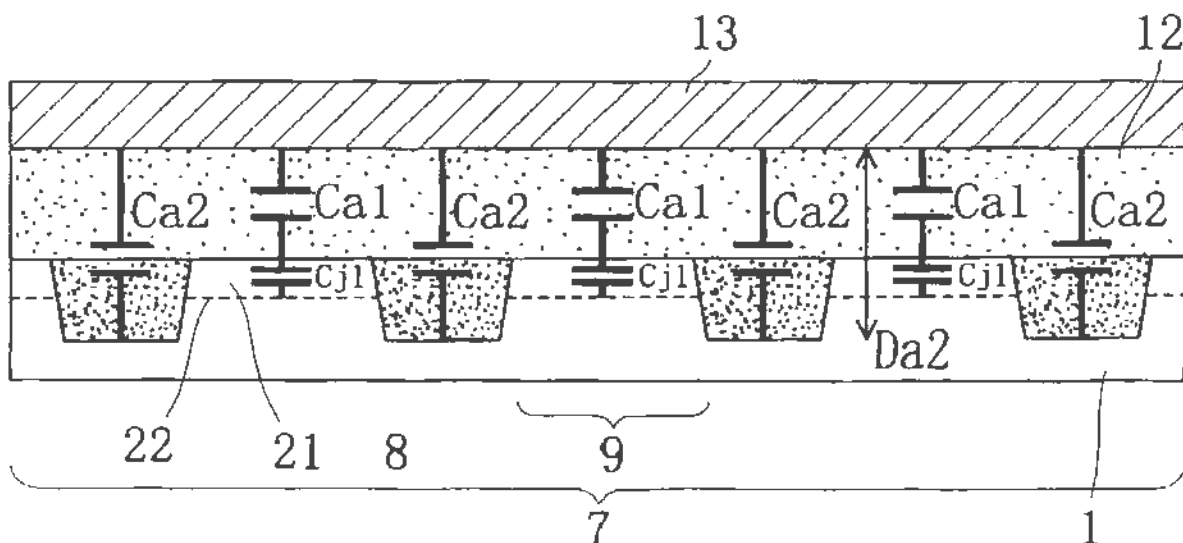


Fig. 1(b)



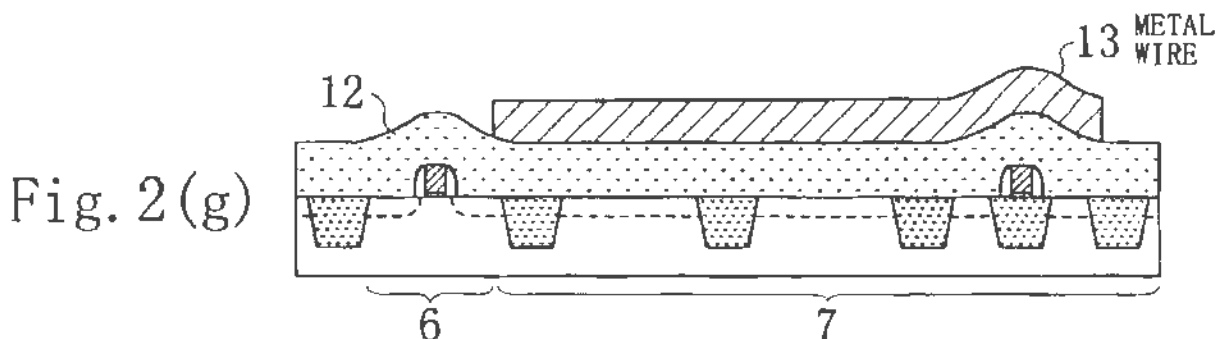
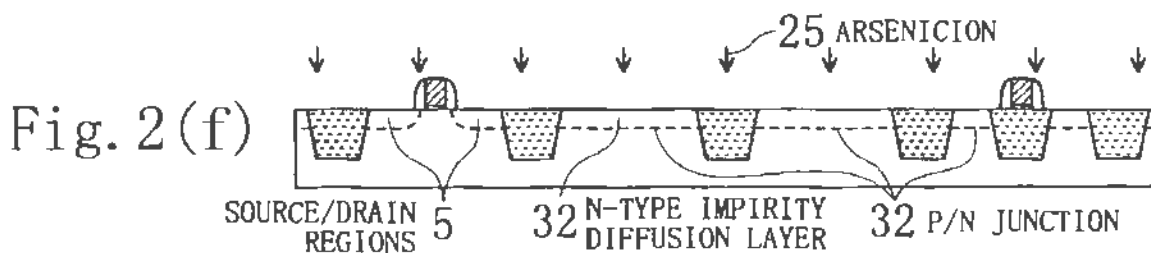
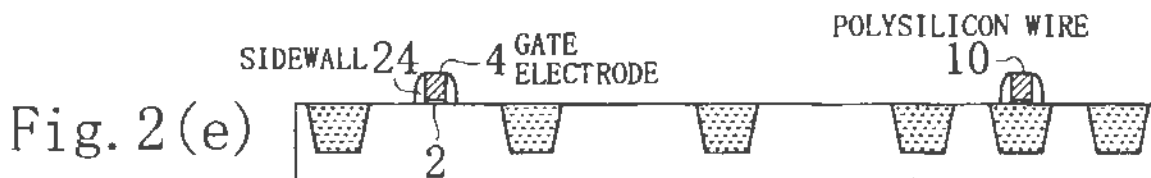
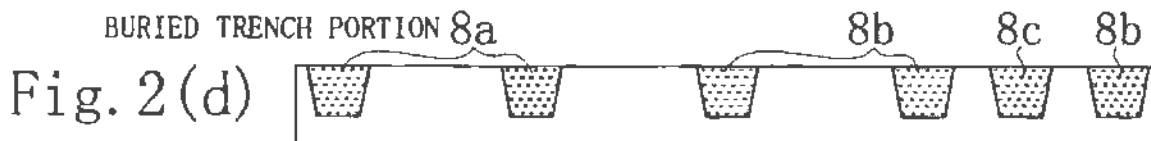
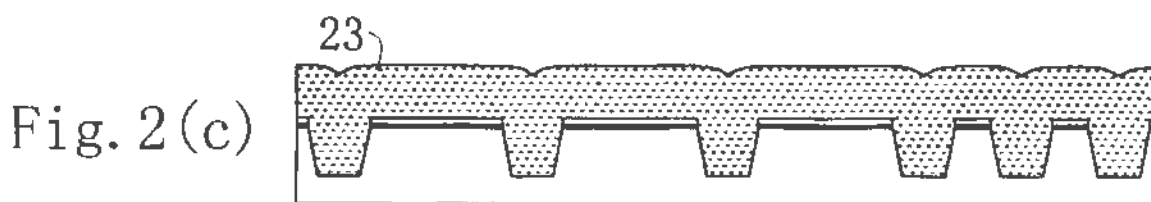
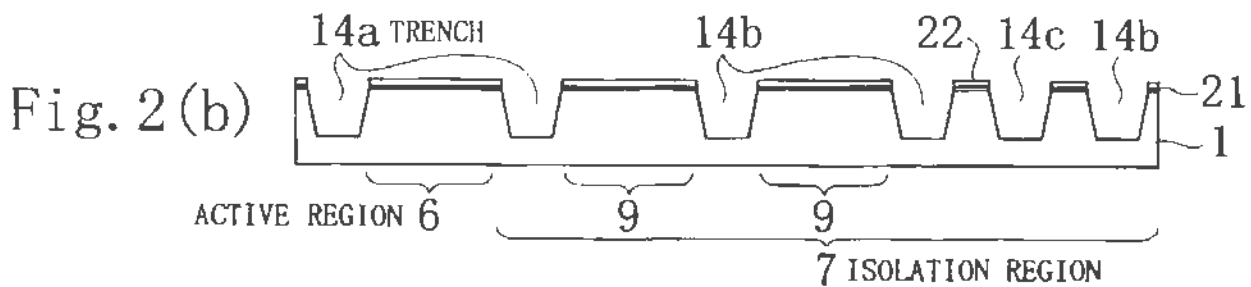
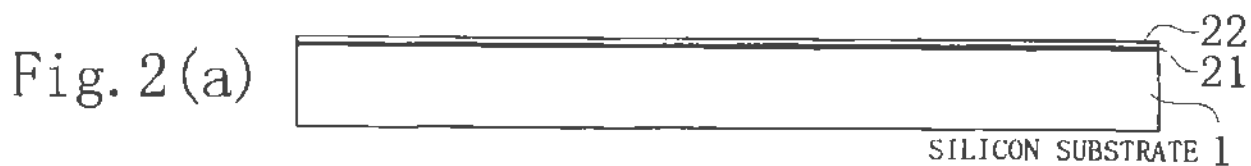


Fig. 3

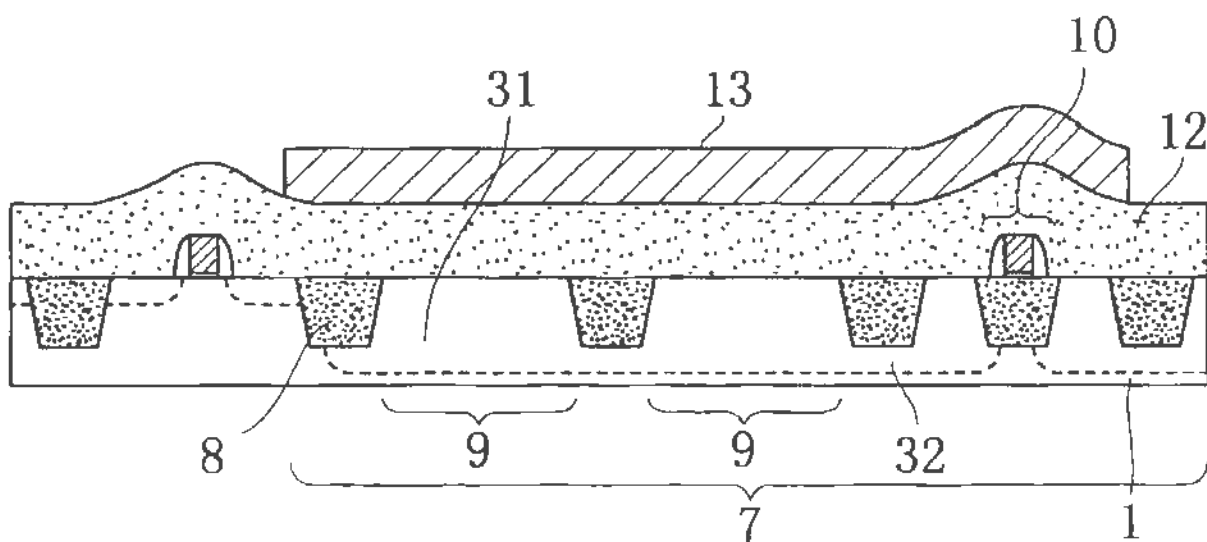


Fig. 4

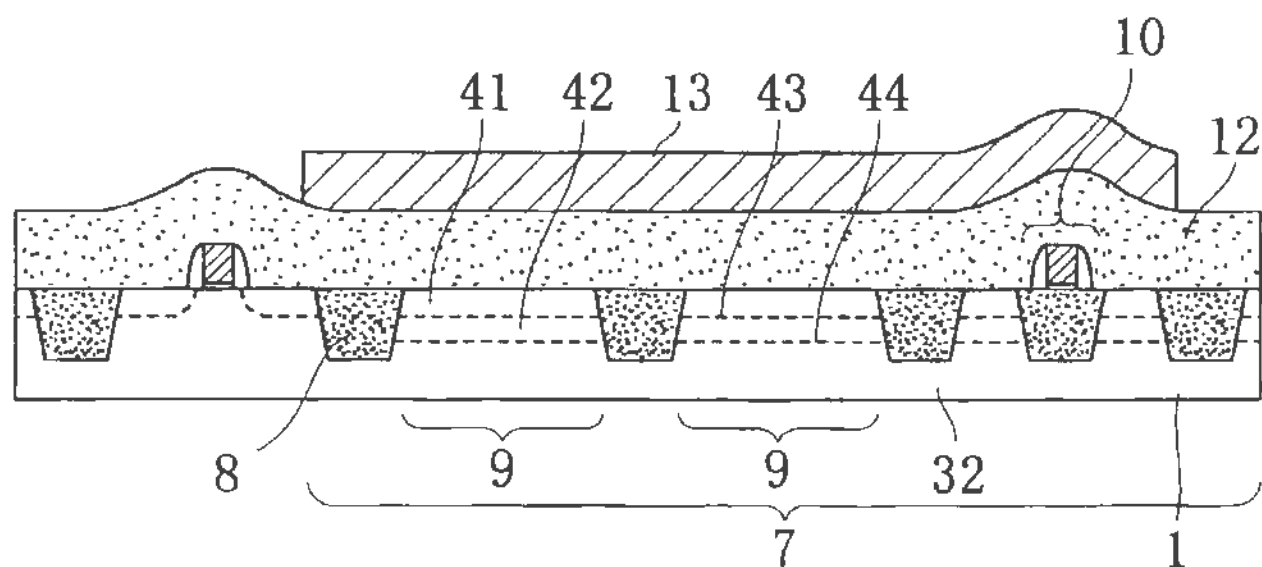


Fig. 5

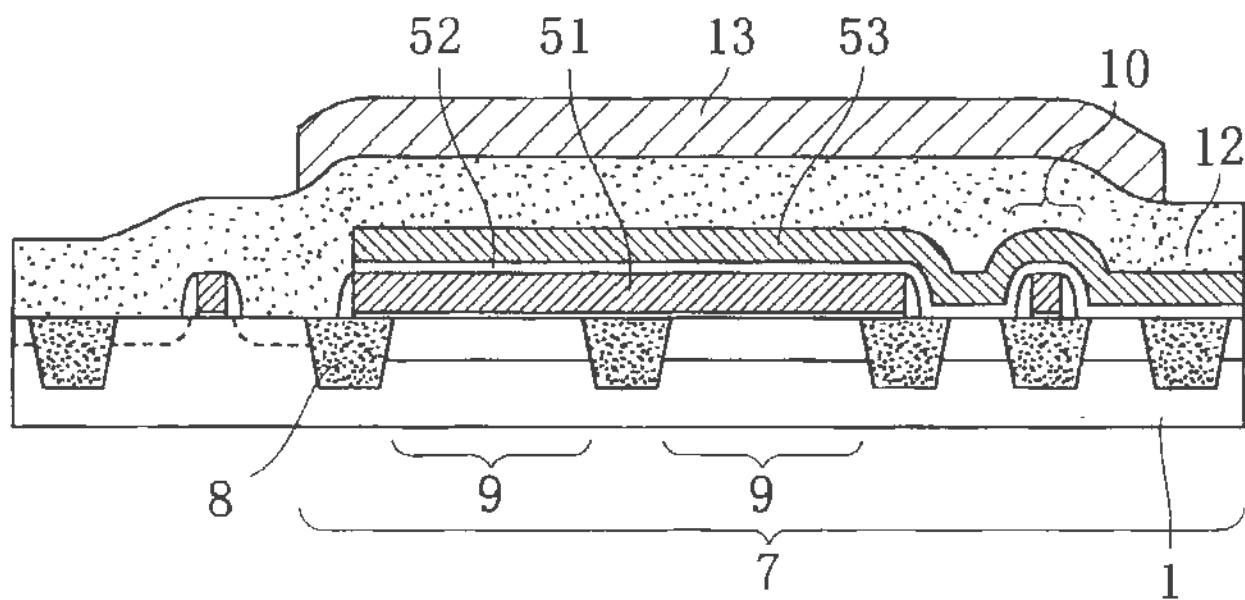


Fig. 6(a)



Fig. 6(b)

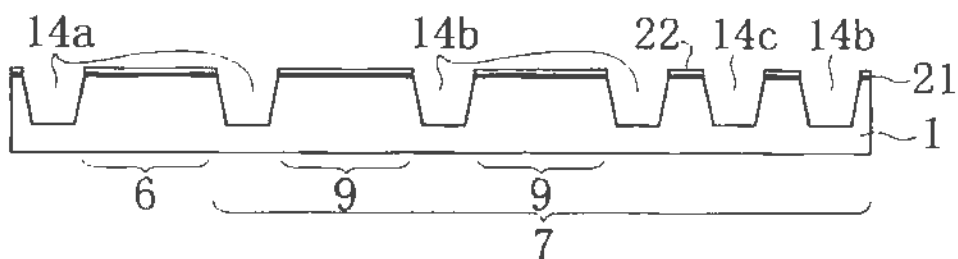


Fig. 6(c)

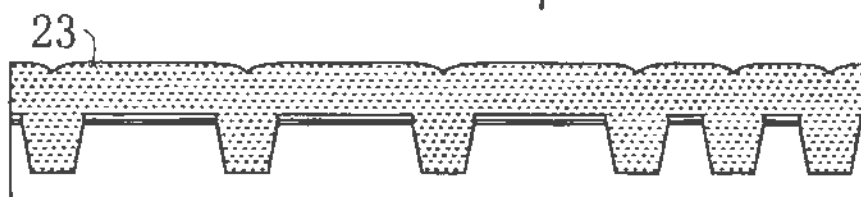


Fig. 6(d)

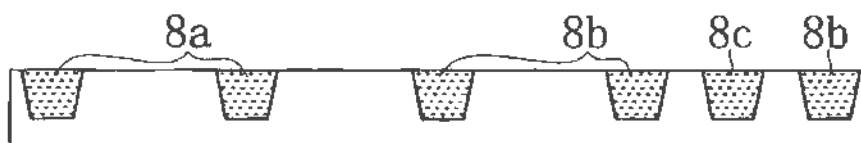


Fig. 6(e)



Fig. 6(f)

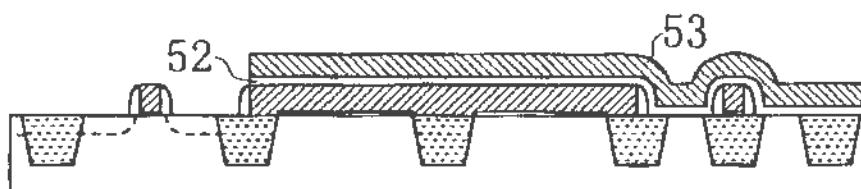


Fig. 6(g)

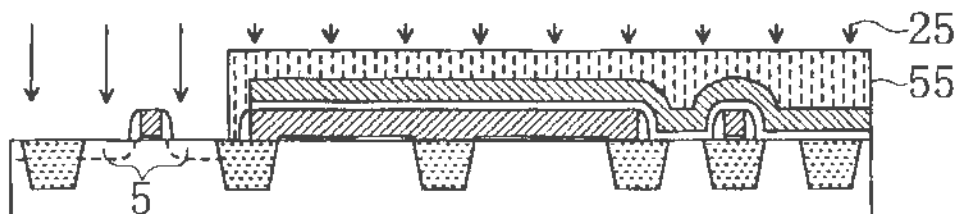


Fig. 6(h)

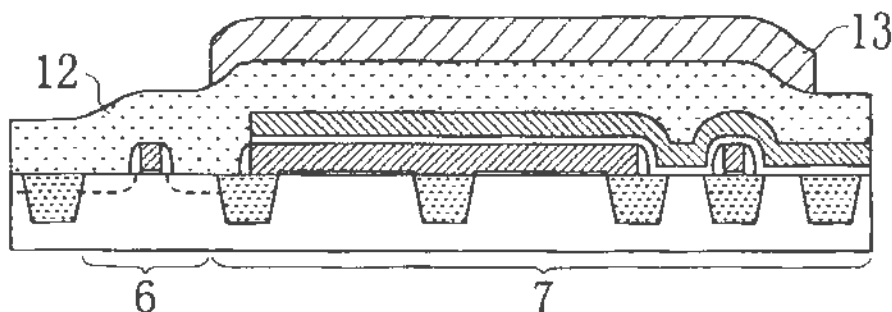


Fig. 7

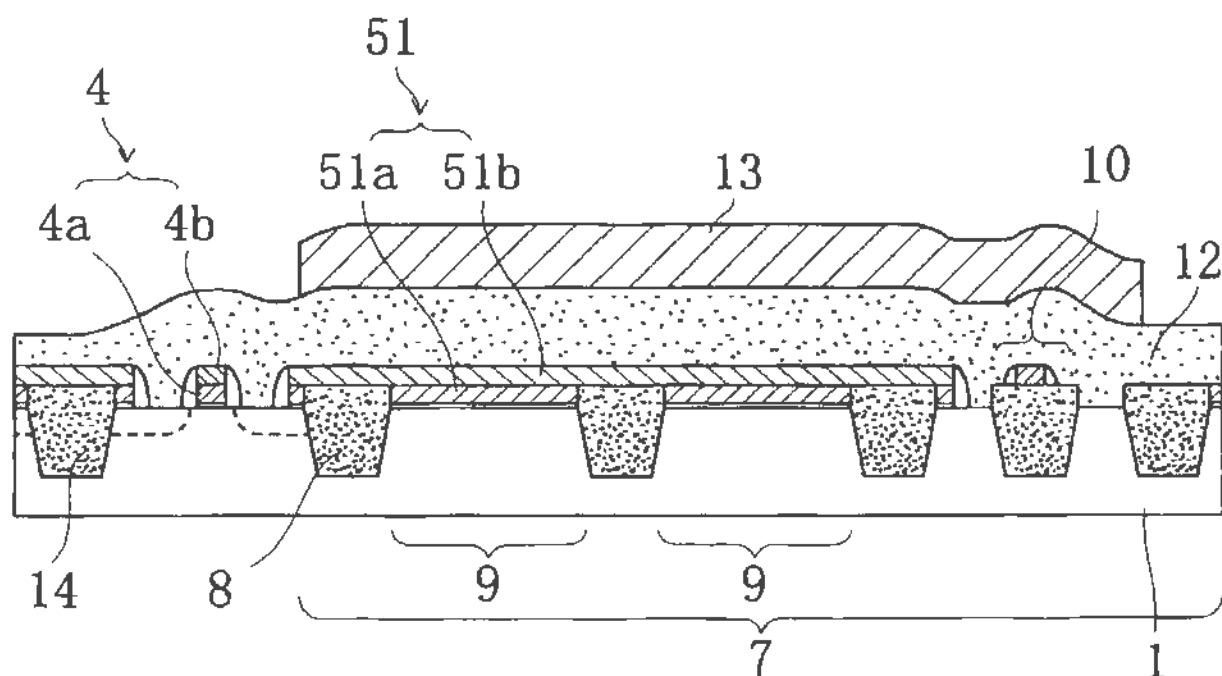
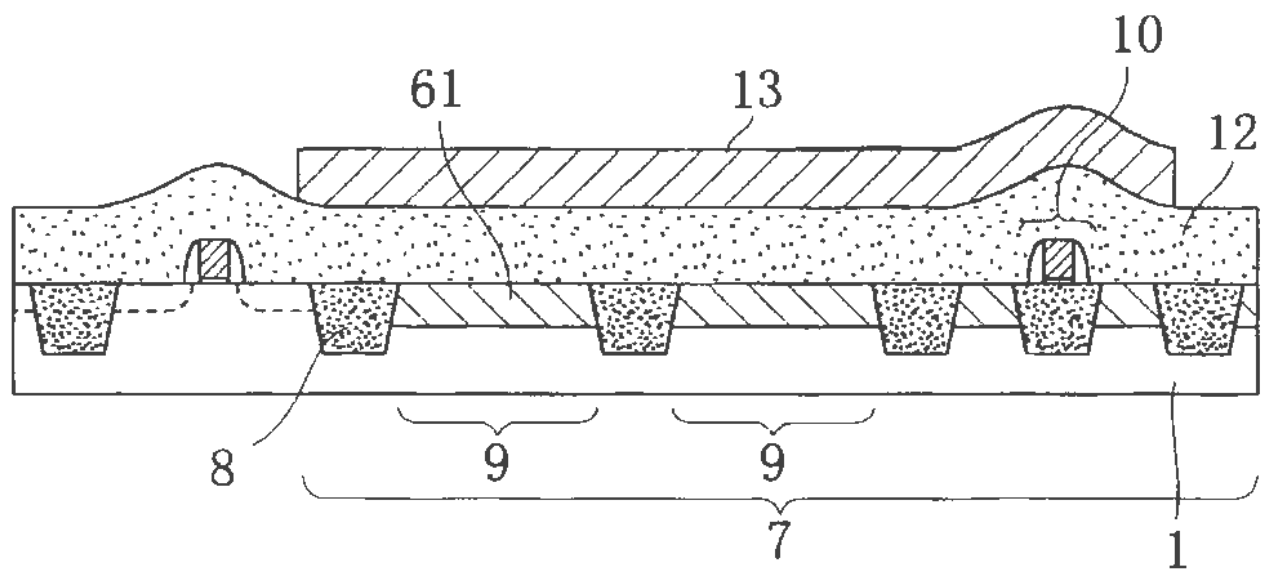


Fig. 8



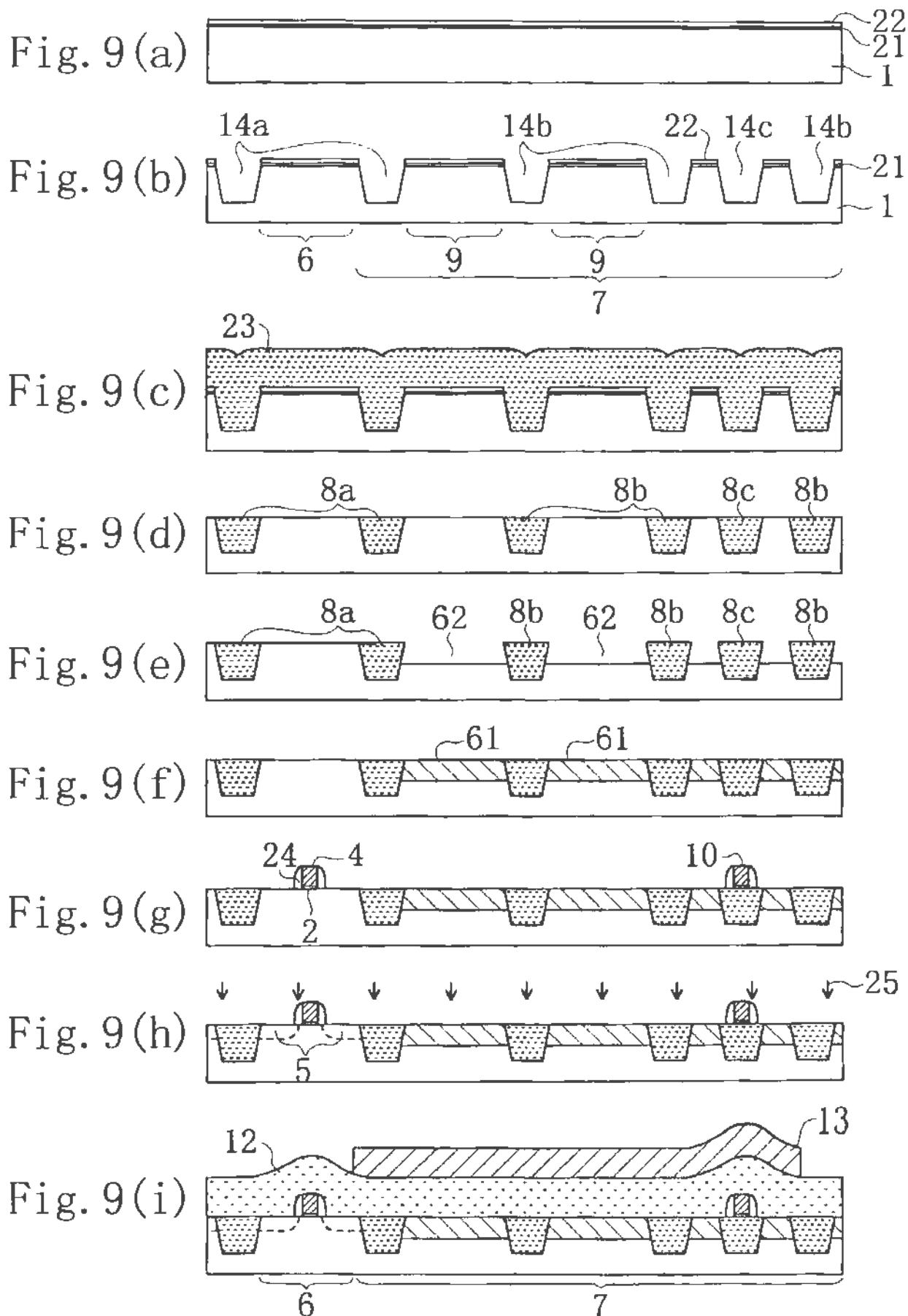
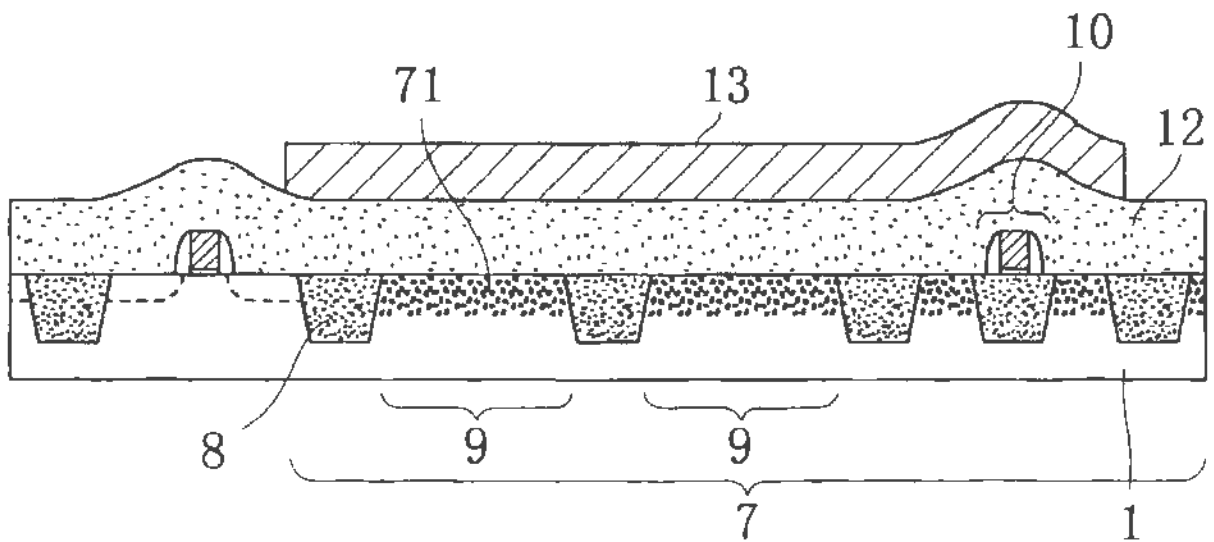


Fig. 10



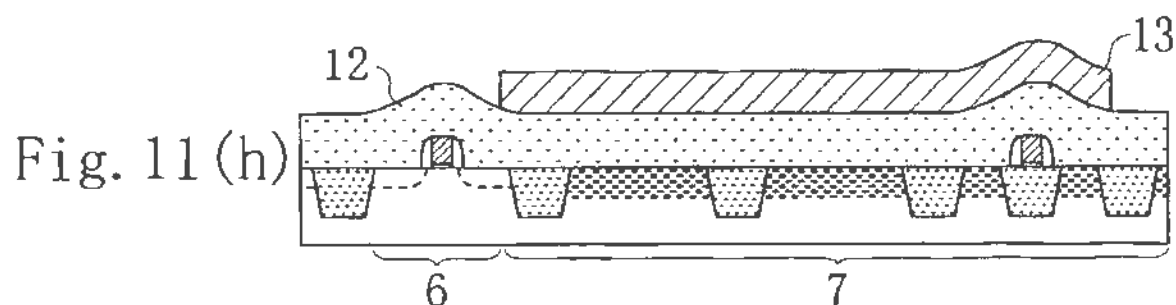
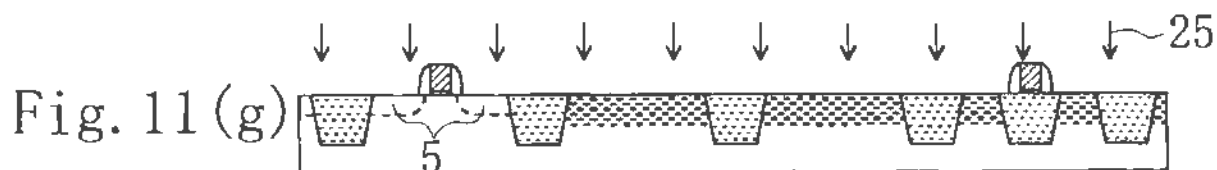
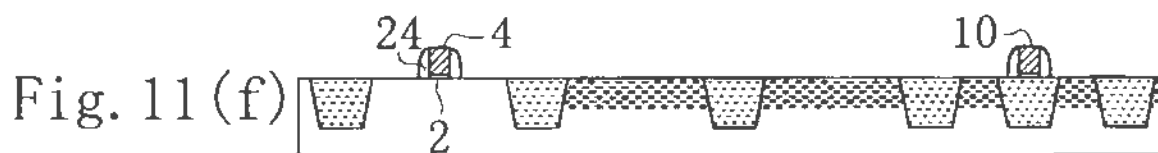
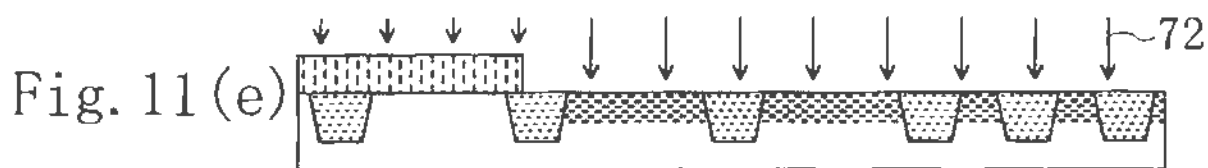
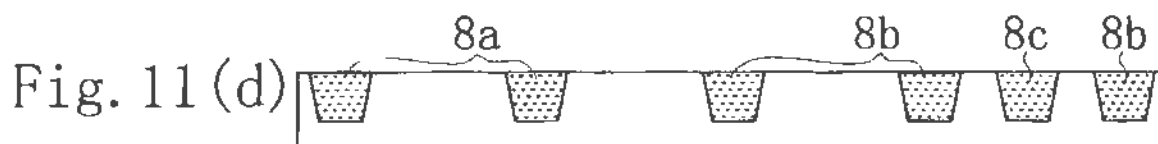
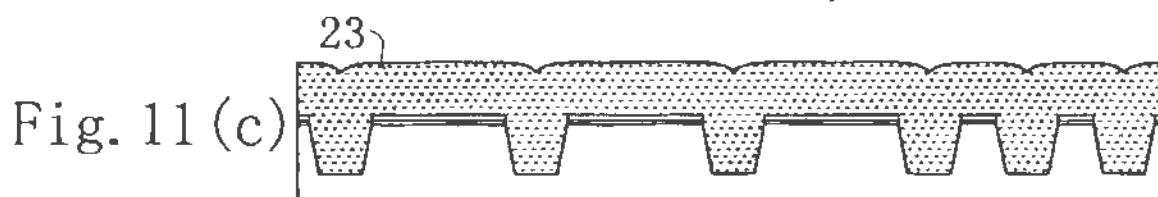
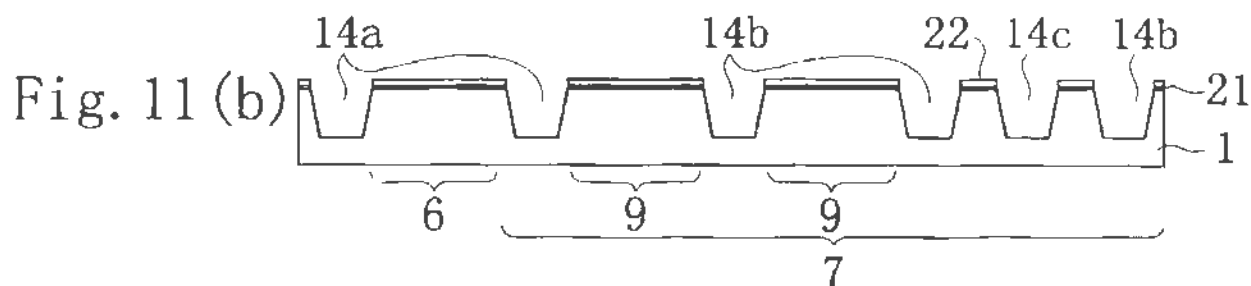
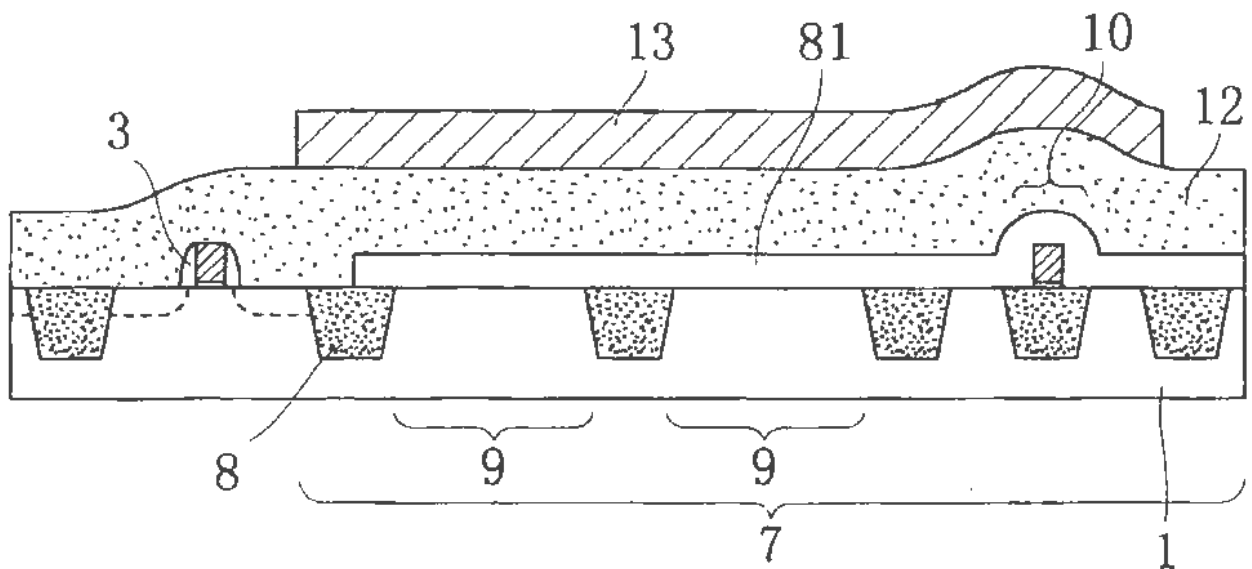


Fig. 12



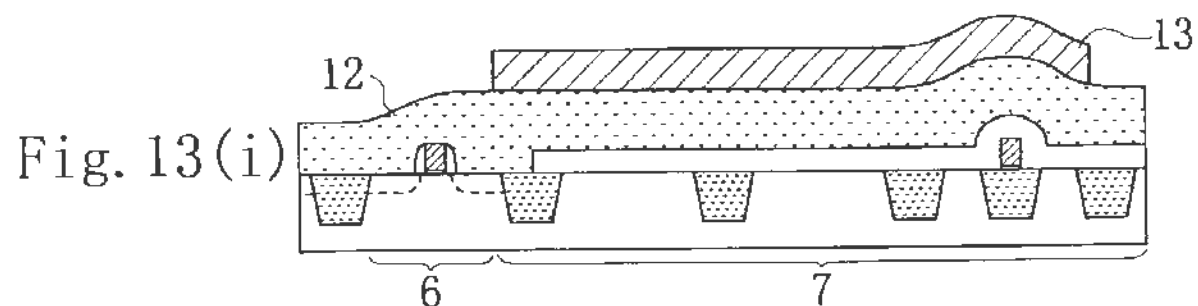
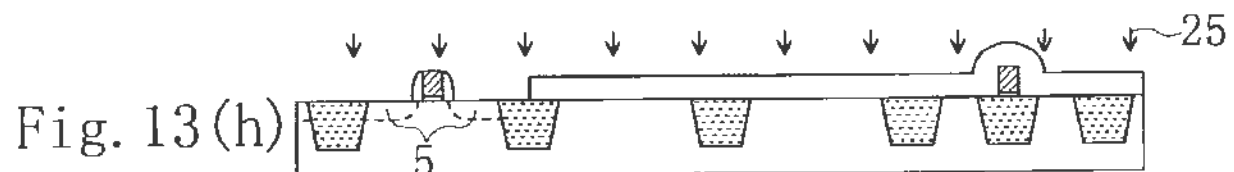
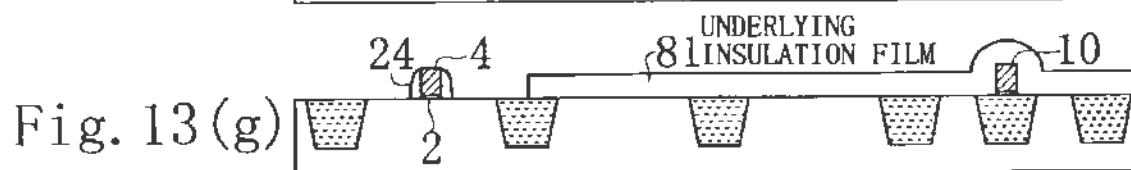
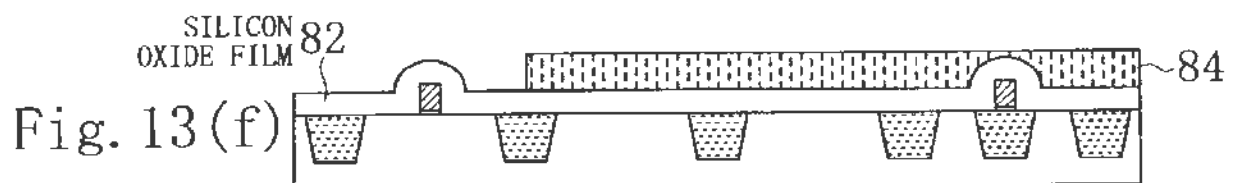
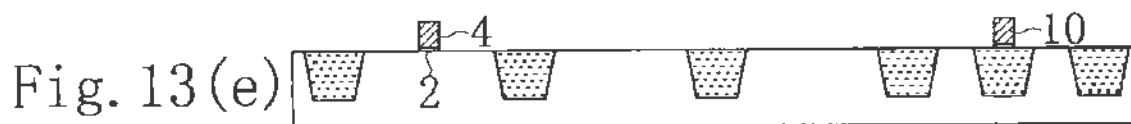
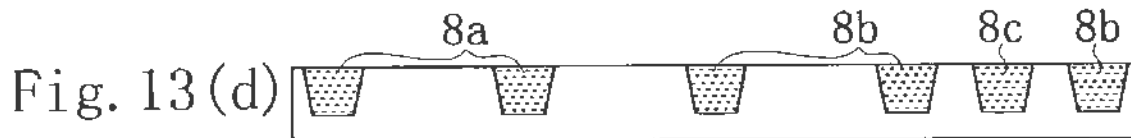
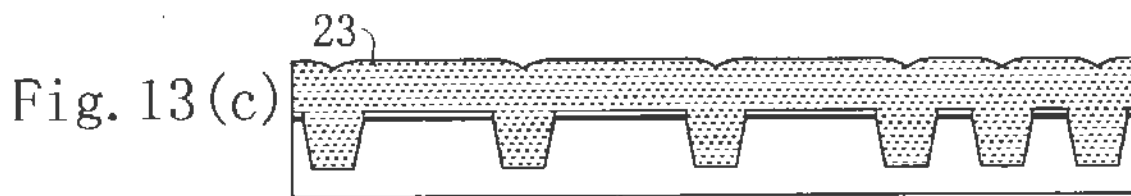
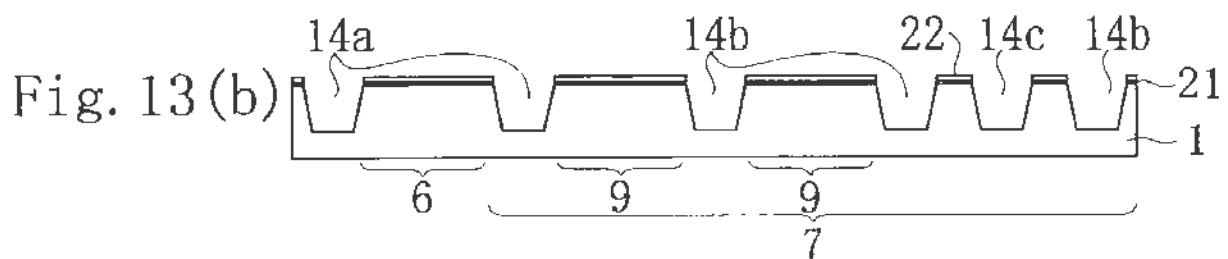
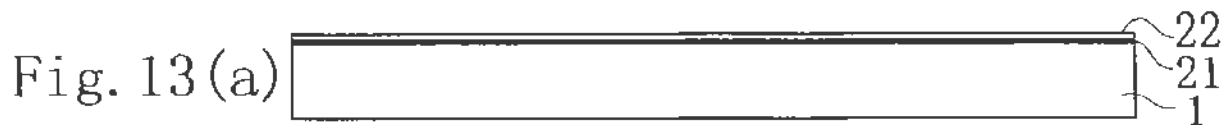


Fig. 14(a)

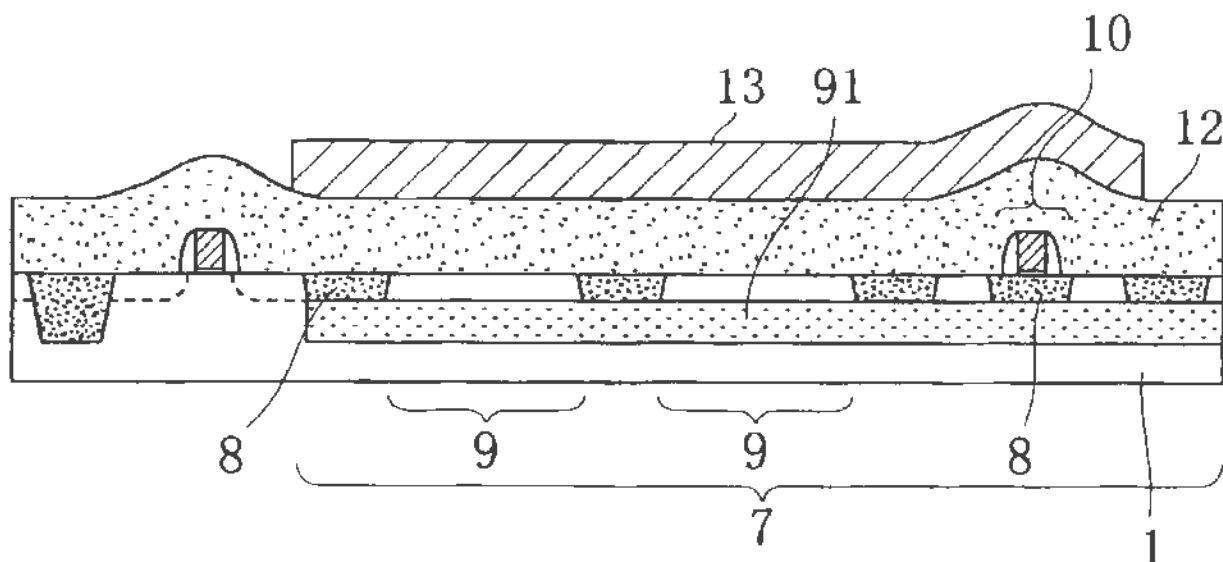
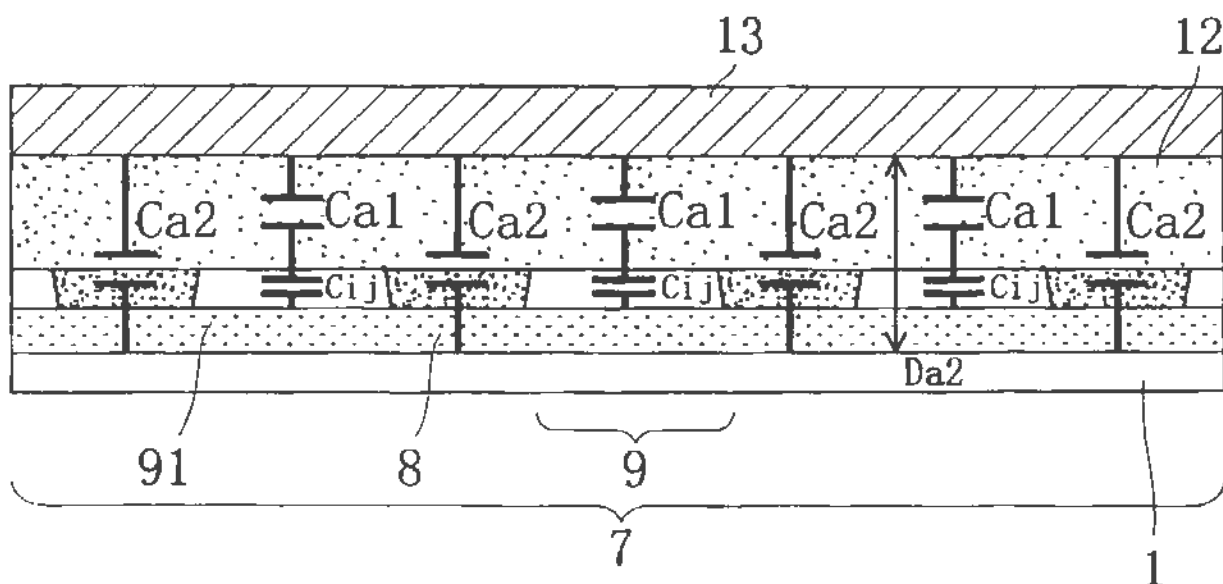
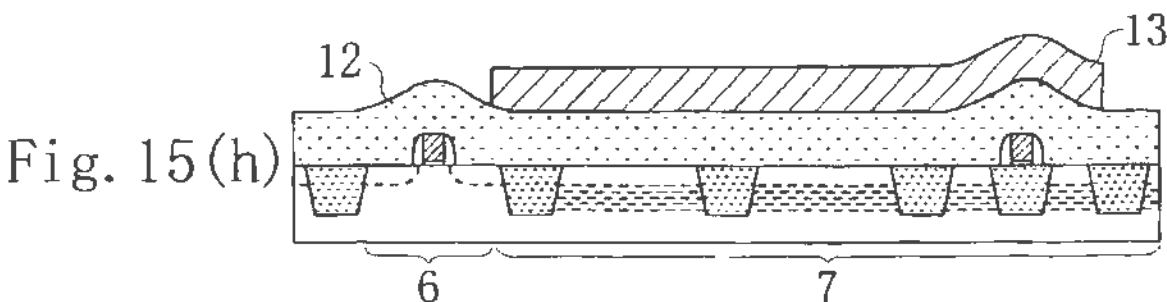
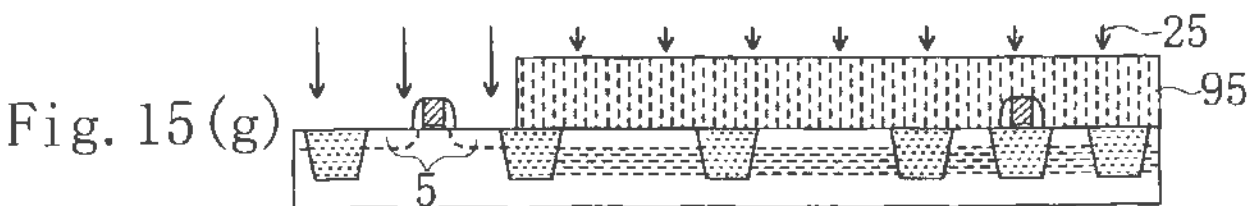
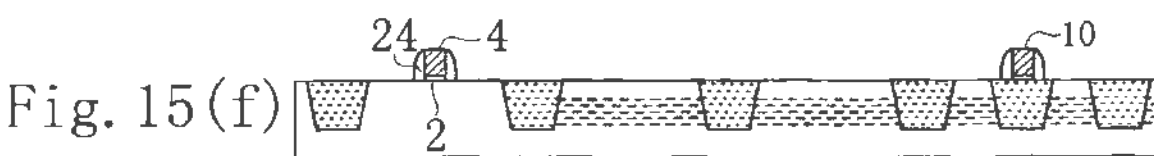
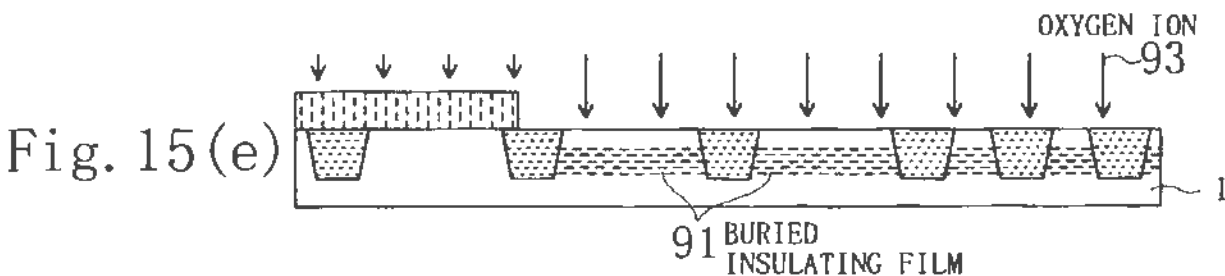
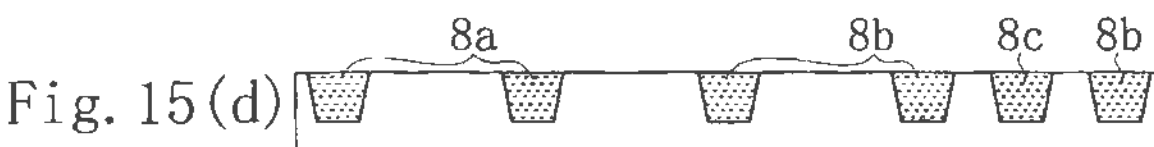
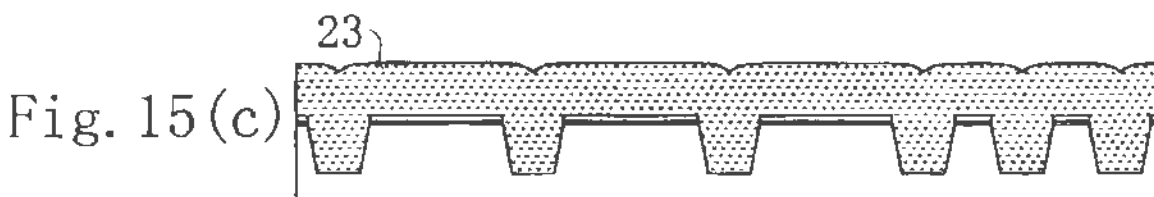
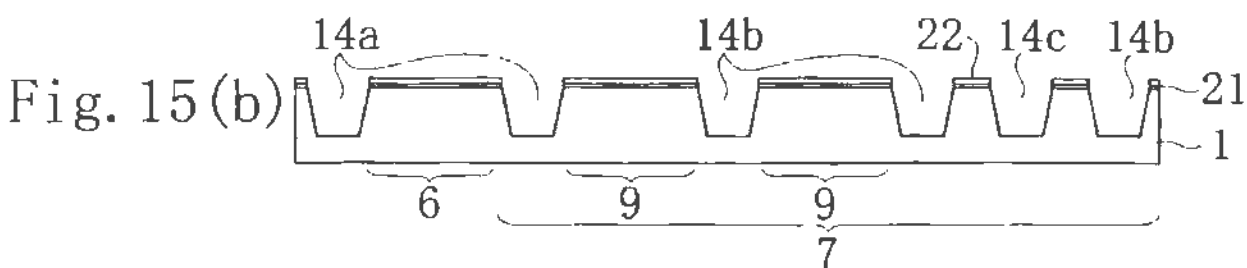
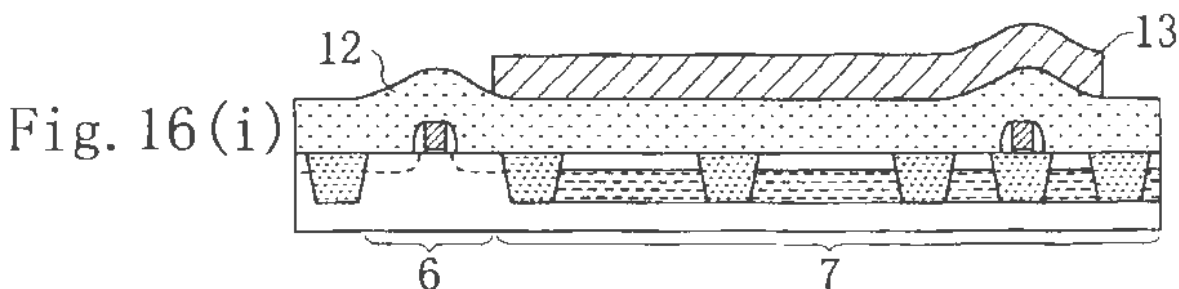
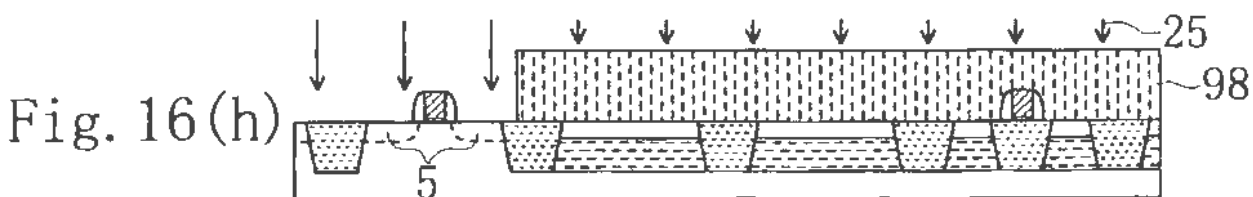
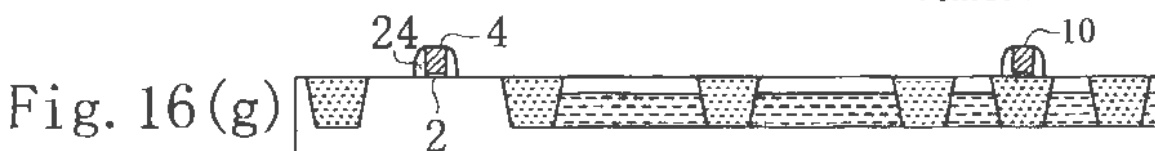
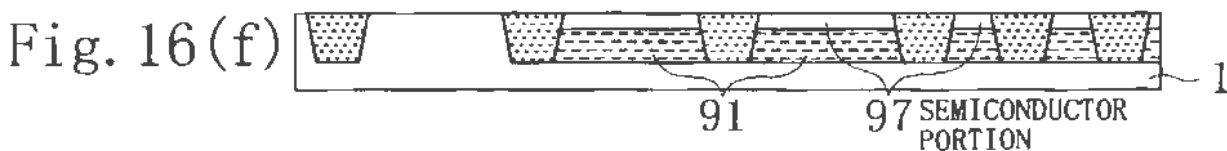
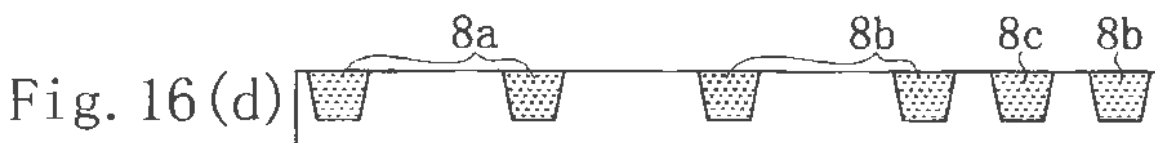
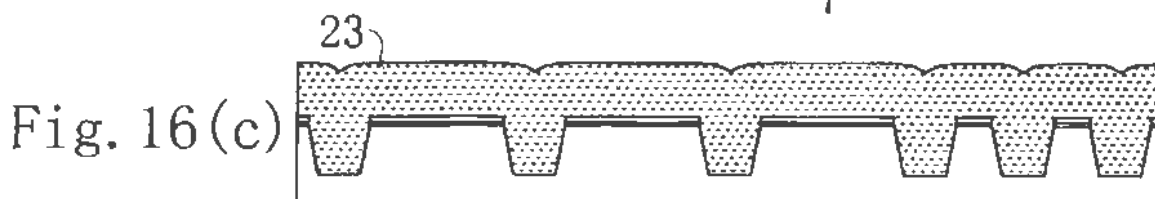
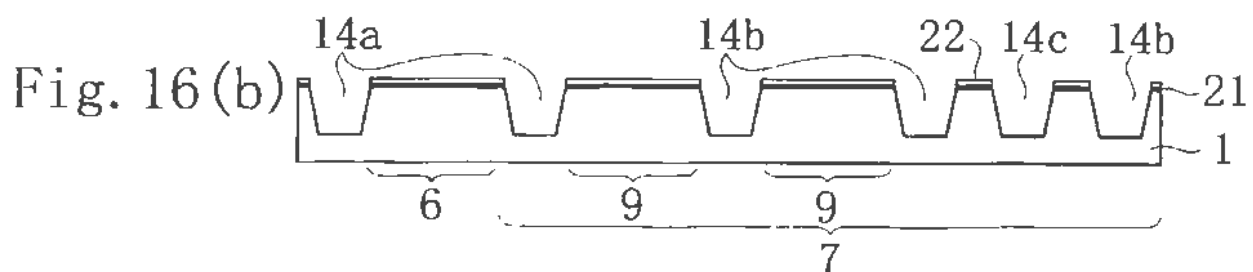
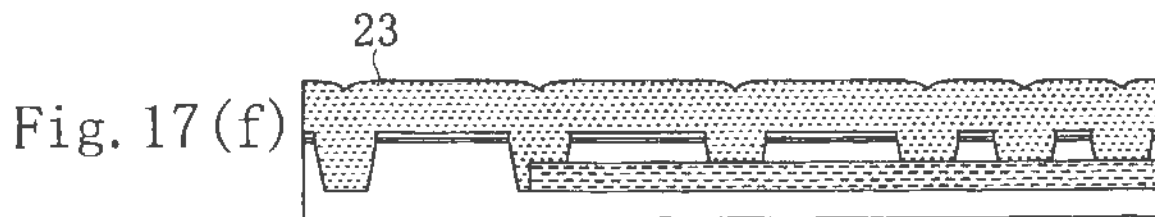
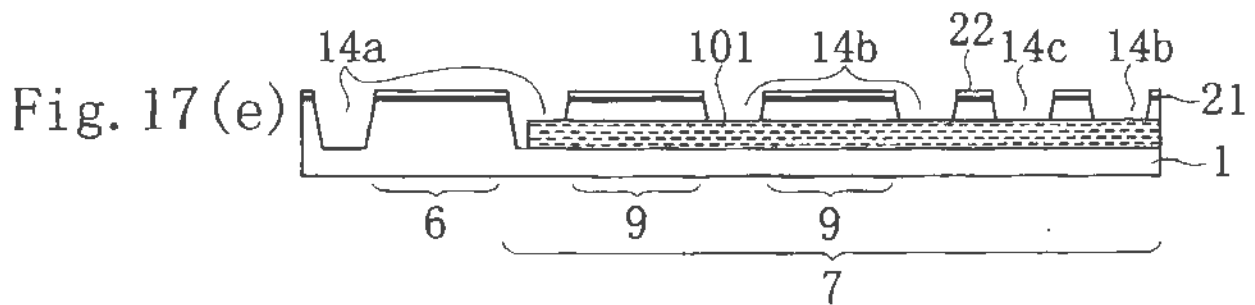
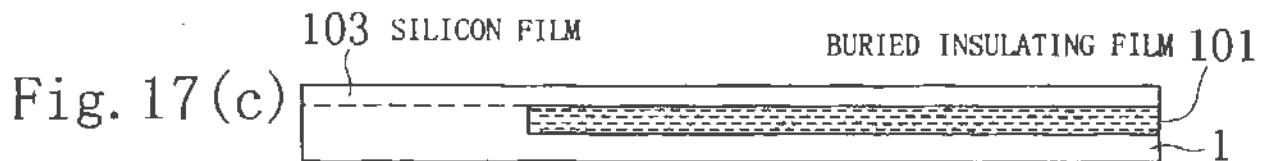
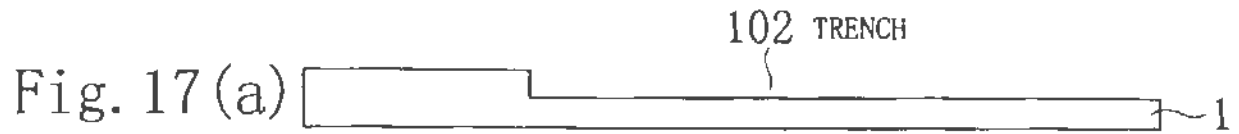


Fig. 14(b)









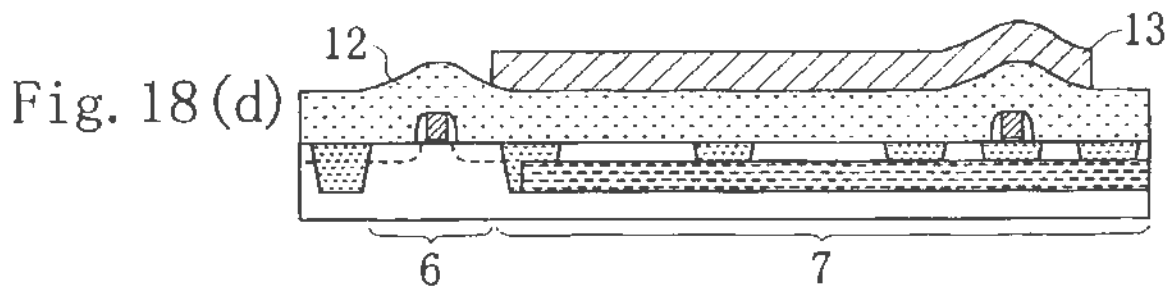
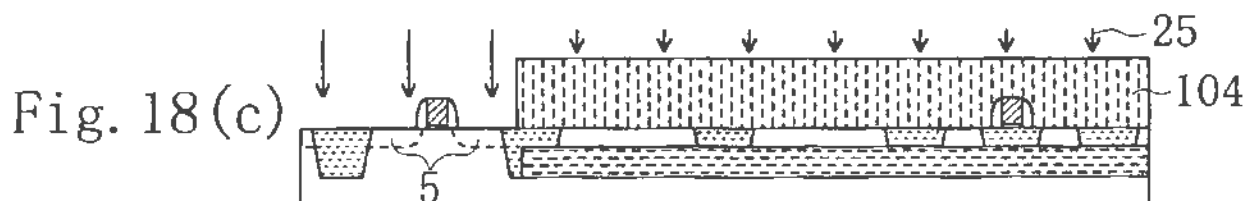
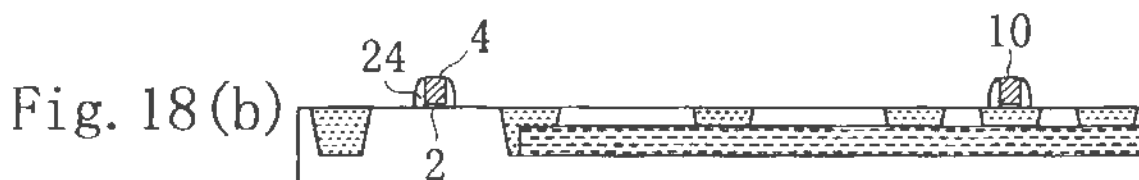
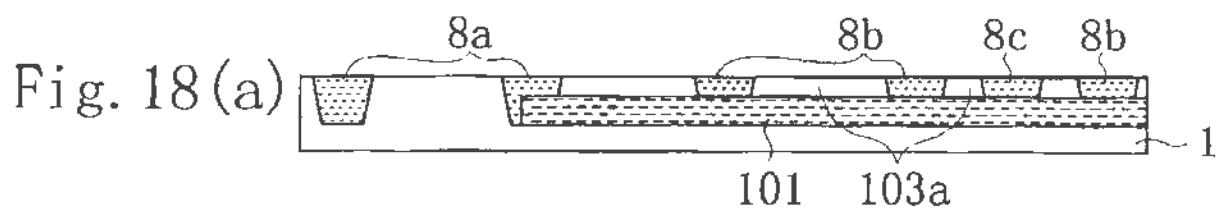


Fig. 19
PRIOR ART

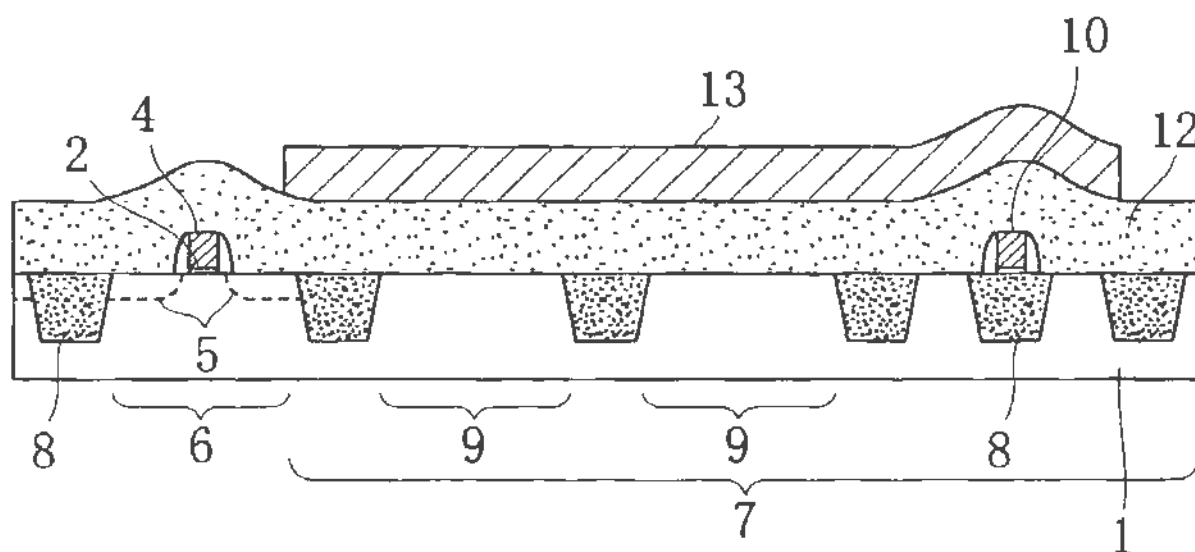


Fig. 20(a)

PRIOR ART



Fig. 20(b)

PRIOR ART

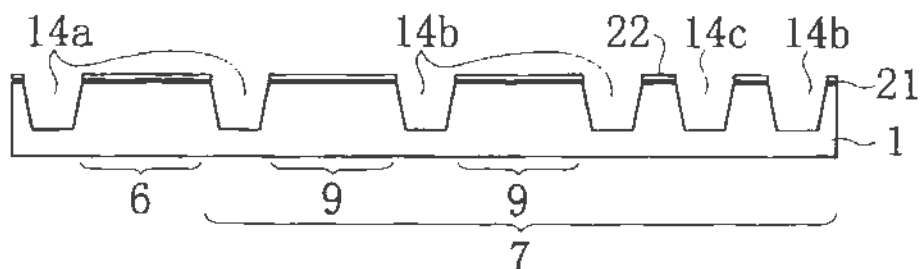


Fig. 20(c)

PRIOR ART

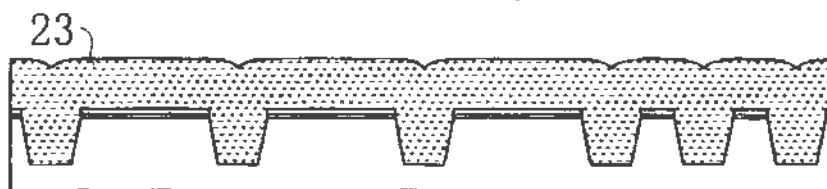


Fig. 20(d)

PRIOR ART

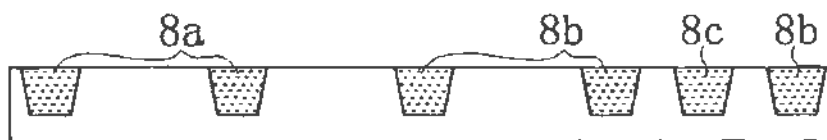


Fig. 20(e)

PRIOR ART

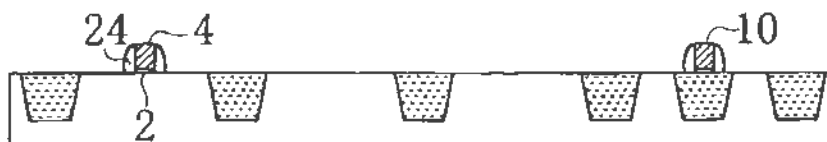


Fig. 20(f)

PRIOR ART

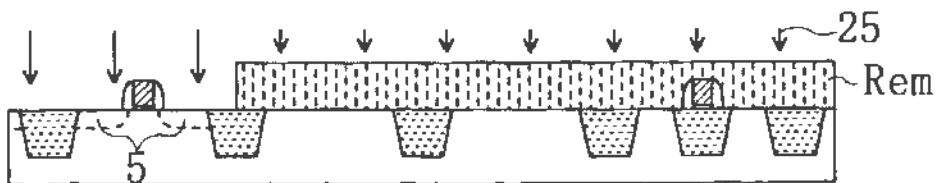


Fig. 20(g)

PRIOR ART

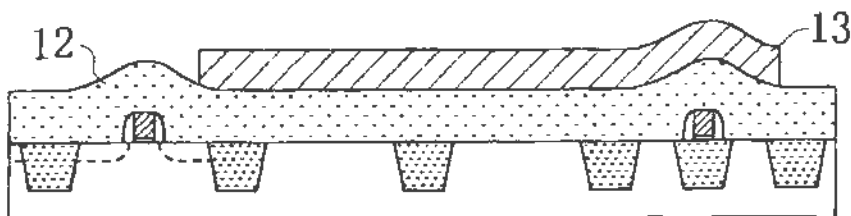


Fig. 21(a)

PRIOR ART

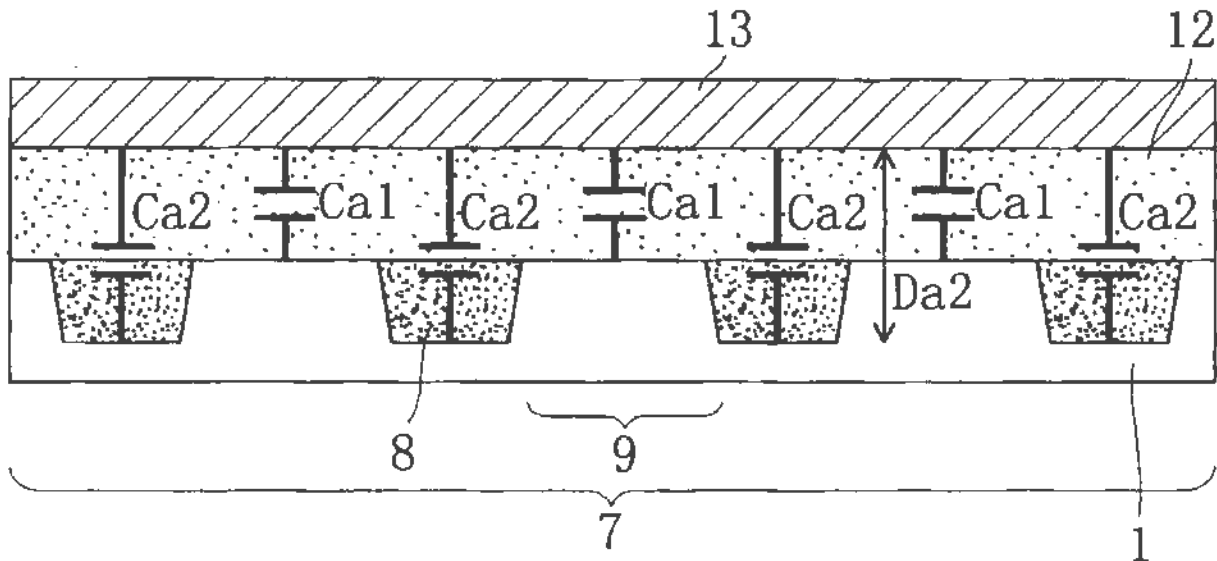
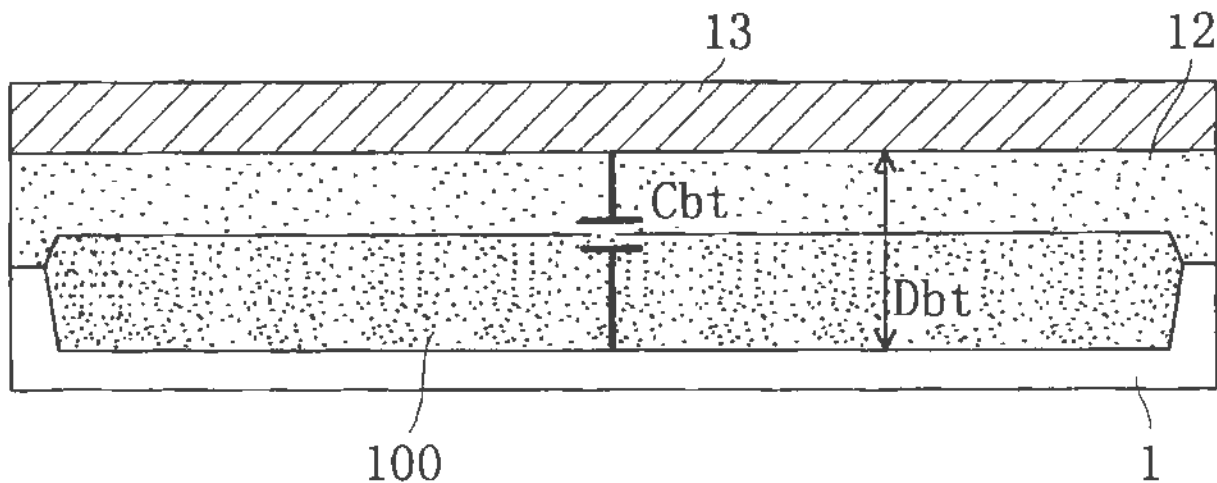


Fig. 21(b)

PRIOR ART



METHOD OF MANUFACTURING TRENCH-ISOLATED SEMICONDUCTOR DEVICE

The present invention relates to a semiconductor device having a trench-isolated structure and, more particularly, to a method of reducing the capacitance between the wiring and substrate of the semiconductor device.

As higher-density and increasingly miniaturized semiconductor devices have been implemented in recent years, repeated attempts have been made to substitute a trench isolation technique for a LOCOS technique which is most prevalently used to form isolation for providing insulation between individual elements of the semiconductor devices. In accordance with the trench isolation technique, an insulating material is filled in a trench formed in a semiconductor substrate to form isolation.

Since planarization of a surface of a semiconductor substrate including the insulating material filled in the trench is important to the trench isolation technique, chemical mechanical polishing (CMP) has been used as a planarizing technique which achieves excellent in-plane uniformity free from pattern dependence. In the case where the trench occupies a large area in a CMP process for planarization, the provision of dummy island semiconductor portions has been proposed to avoid trouble resulting from so-called pattern dependence, which causes polishing properties to vary depending on the area of a region to be planarized. In other words, the trench is divided into a plurality of narrow trenches so that the surface of the semiconductor substrate is exposed between the individual trenches to form the dummy semiconductor portions which do not serve as active regions.

FIG. 19 shows an example of the conventional trench-isolated semiconductor device having the dummy island semiconductor portions.

As shown in FIG. 19, an active region 6 of a P-type silicon substrate 1 is formed with: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5 into which an impurity has been introduced. An isolation region 7 surrounding the active region 6 is formed with a plurality of trench portions 8 each filled with a silicon oxide film. Between the individual trench portions 8, there are provided semiconductor portions 9 having top surfaces at the same level as the top surfaces of the trench portions 8. On the trench portions 8 also, there is provided a polysilicon wire 10 formed simultaneously with the gate oxide film 2 and the gate electrode 4 of an element. An interlayer insulating film 12 is deposited over the entire surface of the substrate, followed by a metal wire 13 provided thereon.

In this case, if the trench portions have such large widths as shown in FIG. 21(b), a silicon oxide film filled in each of the trench portions is polished during the CMP process for planarizing the whole substrate so that the surface thereof is depressed due to pattern dependence, which leads to the trouble of degraded planarity or the like. The isolation structure as shown in FIG. 19 has been proposed to prevent such trouble resulting from pattern dependence.

FIGS. 20(a) to 20(g) are cross-sectional views illustrating a process of manufacturing the conventional trench-isolated semiconductor device having an NMOS transistor.

In the step shown in FIG. 20(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 20(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. However, the trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element;

trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions.

In the step shown in FIG. 20(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 20(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wires and the silicon substrate.

In the step shown in FIG. 20(e), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 and the polysilicon wire 10 are formed simultaneously.

In the step shown in FIG. 20(f), arsenic ions 25 are implanted into the active region 6 of the NMOSFET region by using a resist mask Rem covering the PMOSFET region and the isolation region to form the source/drain regions 5. The NMOSFET is formed by the foregoing process steps.

In the step shown in FIG. 20(g), the silicon oxide film is deposited to form the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

In the foregoing step shown in FIG. 20(f), ions of such an impurity as phosphorus or arsenic have been implanted into the gate electrode 4 and source/drain regions 5 of the active region 6 in the step shown in FIG. 20(f). However, impurity ions are not implanted in principle in the region other than the active region 6, though they may be introduced slightly extensively into the periphery of the isolation region in considerations of mask displacement. Hence, impurity ions are not implanted in the dummy semiconductor portions 9 between the individual trench portions 8.

A description will be given to the wiring-to-substrate capacitance of the trench-isolated semiconductor device having the small trench portions 8 which are discretely located and the dummy semiconductor portions 9 as shown in FIG. 19 and in a semiconductor device having a wide isolating/insulating film such as a LOCOS film. FIG. 21(a) is a cross-sectional view for illustrating, by way of example, the wiring-to-substrate capacitance in the isolation region 7 having the dummy semiconductor portions 9. FIG. 21(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance of the semiconductor device having a LOCOS isolation film 100 and no dummy semiconductor portion. It is assumed here that impurity ions have not been implanted in the isolation region 7 during the implantation of ions into the source/drain regions and that the area occupied by the whole isolation region 7 is equal in each of the two semiconductor devices.

In the semiconductor device shown in FIG. 21(a), a total wiring-to-substrate capacitance C_{at} corresponds to the sum of capacitances $Ca1$ and $Ca2$, which is represented by the following equation (1):

$$C_{at} = \Sigma C_{a1} + \Sigma C_{a2}$$

In the case where a member interposed between the wiring and substrate is composed of a homogeneous material, the wiring-to-substrate capacitance per unit area is inversely proportional to the distance between the wiring and substrate, so that the capacitance is larger as the distance is shorter. If the total wiring-to-substrate of the semiconductor device shown in FIG. 21(b) is represented by C_{bt} when the dimension Da_2 shown in FIG. 21(a) is equal to the dimension Db_1 shown in FIG. 21(b), the following inequality (2) is satisfied:

$$C_{at} > C_{bt} \quad (2)$$

which indicates that the wiring-to-substrate capacitance C_{at} in the structure shown in FIG. 21(a) is larger than the wiring-to-substrate capacitance C_{bt} in the structure shown in FIG. 21(b).

Although the formation of the island pattern composed of the dummy semiconductor portions in the isolation region has the advantage of achieving planarization with excellent in-plane uniformity, it also has the possibility of increasing the wiring-to-substrate capacitance and resultantly reducing the operating speed of the semiconductor device.

SUMMARY OF THE INVENTION

In view of the foregoing, the present invention has been achieved based on the principle that, if each electrode of a parallel-plate capacitor occupies an equal area, the capacitance of the capacitor is generally smaller as the distance between the electrodes is larger or on the physical phenomenon that, even when the capacitor has equal capacitance, the amount of charge accumulated therein is smaller as the voltage between the electrodes is lower.

It is therefore an object of the present invention to increase the operating speed of a trench-isolated semiconductor device comprising an isolation region consisting of trench portions and dummy semiconductor portions by providing therein means for reducing the wiring-to-substrate capacitance in the isolation region or means for reducing the amount of charge accumulated in the capacitance present between the wiring and substrate in the isolation region.

A first semiconductor device according to the present invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; and at least one PN junction formed in the semiconductor portions underlying the wire.

In the arrangement, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the upper portion of the PN junction of each of the semiconductor portions to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. Accordingly, the wiring-to-substrate capacitance of the whole semiconductor device is reduced, resulting in the semiconductor device operating at a higher speed.

The PN junction may include a plurality of PN junctions formed in the semiconductor portions.

The arrangement achieves a further reduction in wiring-to-substrate capacitance, resulting in a higher operating speed.

The active region may be formed with an impurity diffusion region and a PN junction may be formed at a bottom face of the impurity diffusion region, the PN junction of the isolation region being positioned at a level lower than the PN junction of the active region.

The arrangement further reduces the wiring-to-substrate capacitance.

A second semiconductor device according to the present invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; and a dielectric film interposed between at least the semiconductor portions of the isolation region and the interlayer insulating film.

In the arrangement, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the dielectric film to the capacitance in the interlayer insulating film, so that the total wiring-to-substrate capacitance is lowered. Consequently, the operating speed of the semiconductor device is increased.

As the dielectric film, an underlying insulating film may be provided between the interlayer insulating film and the semiconductor portions and trench portions.

There can be further provided a gate electrode formed on the semiconductor substrate within the active region and sidewalls made of an insulating material and formed on both side faces of the gate electrode such that the underlying insulating film is formed of the same film as forming the sidewalls.

The underlying insulating film may be composed of a multilayer film.

The arrangement enables the underlying insulating film for reducing the wiring-to-substrate capacitance to be composed by using the sidewalls required to form a MOSFET of so-called LDD structure. Consequently, the wiring-to-substrate capacitance can be reduced, while avoiding an increase in manufacturing cost.

The dielectric film may be formed in an upper portion of each of the semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top face of each of the trench portions.

Preferably, the dielectric film is composed of at least one of a silicon oxide film and a silicon nitride film.

A third semiconductor device according to the present invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; and a buried insulating film formed in an inner portion of each of the semiconductor portions in the isolation region.

The arrangement allows a reduction in the wiring-to-substrate capacitance of the entire isolation region, resulting in a significant reduction in operating speed.

A fourth semiconductor device according to the present invention comprises: a semiconductor substrate having an

active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; an a resistor film formed between the interlayer insulating film and at least the semiconductor portions of the isolation region.

In the arrangement, a voltage drop in the resistor film reduces the amount of charge accumulated in the wiring-to-substrate capacitance in the region of the semiconductor device containing the resistor film, though the wiring-to-substrate capacitance is not reduced in the region. Consequently, the time required for charging or discharging is reduced, resulting in the semiconductor device operating at a higher speed.

As the resistor film, an underlying resistor film may be formed to extend continuously over the semiconductor portions and trench portions.

The arrangement allows the wiring-to-substrate capacitance to be reduced by using various films having electric resistivity which are formed on the semiconductor substrate.

There can further be provided a resistor element formed on the semiconductor substrate and having a high resistor film such that the underlying resistor film is formed of the same film as composing the high resistor film of the resistor element.

In the arrangement, the underlying resistor film having the same resistance as the high resistor film used as a resistor element achieves a remarkable voltage dropping effect.

There can further be provided an element having an electrode member composed of a conductor film formed on the semiconductor substrate within the active region such that the resistor film is composed of the same material as composing the electrode member.

There can further be provided a FET having a gate electrode composed of a first conductor film formed on the semiconductor portion within the active region and a second conductor film deposited on the first conductor film such that a top surface of the first conductor film of the gate electrode is at approximately the same level as a top surface of each of the trench portions, while a region of the resistor film overlying each of the semiconductor portions is formed of the same two films as composing the first and second conductor films of the gate electrode and a region of the resistor film overlying each of the trench portions is composed of the same material as composing the first conductor film of the gate electrode.

Each of the arrangements eliminates the necessity for an additional step of forming the resistor film, so that the wiring-to-substrate capacitance is reduced, while an increase in manufacturing cost is prevented.

The resistor film may be formed in an upper portion of each of the semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top surface of each of the trench portions.

The resistor film may be composed of a silicon film containing at least one of an oxygen atom and a nitrogen atom.

The resistor film may be composed of at least one of a polysilicon film and an amorphous silicon film.

The arrangement allows the formation of the resistor film by using the polysilicon film or amorphous silicon film to

compose the gate electrode and the resistor element and thereby prevents an increase in manufacturing cost.

A first method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region of a first conductivity type, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of introducing an impurity containing at least an impurity of a second conductivity type into the dummy semiconductor portions of the isolation region to form at least one PN junction in the dummy semiconductor portions; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

The method enables the formation of the semiconductor device including the dummy semiconductor portions each having the PN junction. The capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the upper portion of the PN junction of each of the semiconductor portions to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. Accordingly, the wiring-to-substrate capacitance of the whole semiconductor device is reduced, resulting in the semiconductor device operating at a higher speed.

The third and fourth steps may include forming a gate electrode of a FET as the element on the active region, introducing the impurity of the second conductivity type into the active region and the dummy semiconductor portions, and thereby forming source/drain regions of the FET, while forming the at least one PN junction in the dummy semiconductor portions.

The method enables the formation of the semiconductor device operating at a high speed by using a typical manufacturing process for forming a FET without an additional step of forming the PN junction in each of the dummy semiconductor portions.

The third step may include forming a gate electrode of a FET as the element on the active region by using a first mask covering the isolation region and introducing the impurity of the second conductivity type into the active region to form source/drain regions of the FET and the fourth step may include introducing the impurity containing at least the impurity of the second conductivity type into the dummy semiconductor portions by using a second mask covering the active region to form the at least one PN junction in the dummy semiconductor portions.

The method enables the formation of the semiconductor device having an arbitrary number of PN junctions without placing restraints on the depth and impurity concentration of the PN junction in the active region, resulting in a semiconductor device having minimum wiring-to-substrate capacitance.

A second method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a

plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming a resistor film on each of the dummy semiconductor portions of the isolation region; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

The method enables the formation of the semiconductor device comprising the resistor film between the interlayer insulating film and dummy semiconductor portions of the isolation region. A voltage drop in the resistor film reduces the amount of charge accumulated in the wiring-to-substrate capacitance, though the wiring-to-substrate capacitance is not reduced in the region containing the resistor film of the semiconductor device. Consequently, the time required for charging or discharging is reduced, resulting in the semiconductor device operating at a higher speed.

The fourth step may include composing the resistor film of a film containing at least one of polysilicon and amorphous silicon.

The fourth step may include composing the resistor film of a multilayer film constituted by two or more conductor films with at least an insulating film interposed therebetween.

The fourth step may include introducing an impurity at a concentration of 1×10^{20} atoms/cm³ or lower into the resistor film.

A third method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of implanting ions into an upper portion of each of the dummy semiconductor portions to form a high resistor portion therein; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

The method allows the formation of the semiconductor device comprising the high resistor portion between the interlayer insulating film and dummy semiconductor portions of the isolation region. As described above, a voltage drop in the region containing the high resistor portion of the semiconductor device reduces the amount of charge accumulated in the wiring-to-substrate capacitance. What results is the semiconductor device which requires a shorter time for charging or discharging and therefore operates insulating film at a higher speed.

The fourth step may include implanting ions containing at least an atom having an oxidizing function to form the high resistor portion.

The fourth step may include implanting ions containing at least an atom having a nitriding function to form the high resistor portion.

A fourth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a

plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming an underlying insulating film over the dummy semiconductor portions of the isolation region; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

In accordance with the method, there is formed the semiconductor device including the underlying insulating film beneath the interlayer insulating film in the isolation region thereof. Consequently, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the underlying insulating film to the capacitance in the interlayer insulating film, so that the total wiring-to-substrate capacitance is reduced. What results is the semiconductor device operating at a high speed.

The third step and the fourth step may include forming a gate electrode of a FET forming the element on the active region, depositing a dielectric film on the substrate, performing anisotropic etching with respect to the dielectric film by using a mask covering the isolation region, and thereby leaving sidewalls on both side faces of the gate electrode, while leaving the underlying insulating film over the dummy semiconductor portions.

The method enables the formation of a semiconductor device operating at a high speed by using a typical manufacturing process for forming a FET without an additional step of forming the underlying insulating film.

The fourth step may include forming the underlying insulating film of a dielectric film containing at least silicon oxide.

The fourth step may include forming the underlying insulating film of a dielectric film containing at least silicon nitride.

A fifth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming depressed portions by etching the dummy semiconductor portions and filling an insulating material in the depressed portions to form inter-trench insulating films each having a top face at the same level as respective top faces of the first and second buried trench portions; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

In accordance with the method, there is formed the semiconductor device comprising the inter-trench insulating films between the interlayer insulating films and dummy semiconductor portions of the isolation region thereof. Consequently, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the inter-trench buried insulating films to the capacitance in the interlayer insulating film, so that the total wiring-to-substrate capacitance is reduced. What results is the semiconductor device operating at a high speed.

The fourth step may include forming each of the inter-trench insulating films of a dielectric film containing at least silicon oxide.

The fourth step may include forming each of the inter-trench insulating films of a dielectric film containing at least silicon nitride.

A sixth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of implanting oxygen ions into each of the dummy semiconductor portions to form a buried insulating film in an inner portion thereof; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

A seventh method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming third trenches by etching the semiconductor portions and filling an insulating material in the third trenches to form buried insulating films each having a top face at a level lower than respective top faces of the first and second buried trench portions; a fourth step of growing semiconductor films on the buried insulating films, with the active region covered with a mask member, to form dummy semiconductor portions; a sixth step of forming an interlayer insulating film over an entire surface of the substrate; a fifth step of forming an element on the active region; a seventh step of forming a wire on the interlayer insulating film.

An eighth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench extending over an entire isolation region of the substrate region, while leaving an active region of the substrate region; a second step of filling an insulating material in the first trench to form a buried insulating film having a top face at the same level as a top face of the isolation region; a third step of growing a semiconductor film over the active region and the buried insulating film; a fourth step of forming, in the semiconductor substrate, a second trench for partitioning the semiconductor film and the substrate region into the active region and the isolation region and a third trench for partitioning the portion of the semiconductor film overlying the isolation region into a plurality of dummy semiconductor portions; a fifth step of filling an insulating material in each of the second and third trenches to form a first buried trench portion and a second buried trench portion; a sixth step of forming an element on the portion of the semiconductor film overlying the active region; a seventh step of forming an interlayer insulating film over an entire surface of the substrate; and an eighth step of forming a wire on the interlayer insulating film.

In accordance with the methods, there are obtained semiconductor devices each comprising a buried insulating film at a depth of each of the dummy semiconductor portions of the isolation region. What results is the semiconductor device having smaller wiring-to-substrate capacitance and operating at a higher speed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(a) is a cross-sectional view of a semiconductor device according to a first embodiment, having shallow PN junctions formed in the semiconductor portions thereof and FIG. 1(b) is an enlarged cross-sectional view of an isolation region for illustrating the wiring-to-substrate capacitance in the semiconductor device;

FIGS. 2(a) to 2(g) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to the first embodiment;

FIG. 3 is a cross-sectional view of a semiconductor device according to a second embodiment, having shallow PN junctions formed in the semiconductor portions thereof;

FIG. 4 is a cross-sectional view of a semiconductor device according to a third embodiment, having two PN junctions in the semiconductor portions thereof;

FIG. 5 is a cross-sectional view of a semiconductor device according to a fourth embodiment, having a high resistor film formed on the semiconductor portions thereof;

FIGS. 6(a) to 6(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a fourth embodiment;

FIG. 7 is a cross-sectional view of a semiconductor device according to a fifth embodiment, having a multilayer gate provided therein;

FIG. 8 is a cross-sectional view of a semiconductor device according to an eighth embodiment, having an inter-trench film formed on each of the semiconductor portions thereof;

FIGS. 9(a) to 9(i) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to the sixth embodiment;

FIG. 10 is a cross-sectional view of a semiconductor device according to a seventh embodiment, having a high resistor portion in the upper portion of each of the semiconductor portions;

FIGS. 11(a) to 11(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a seventh embodiment;

FIG. 12 is a cross-sectional view of a semiconductor device according to an eighth embodiment, having an underlying, having an underlying insulating film formed beneath an interlayer insulating film;

FIGS. 13(a) to 13(i) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to the eighth embodiment;

FIG. 14(a) is a cross-sectional view of a semiconductor device according to a ninth embodiment, having a buried insulating film formed over the entire isolation region and FIG. 14(b) is an enlarged cross-sectional view of the isolation region for illustrating the wiring-to-substrate capacitance in the semiconductor device;

FIGS. 15(a) to 15(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to the ninth embodiment;

FIGS. 16(a) to 16(i) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a tenth embodiment;

FIGS. 17(a) to 17(f) are cross-sectional views illustrating the first half of a process of manufacturing a semiconductor device according to an eleventh embodiment;

FIGS. 18(a) to 18(d) are cross-sectional views illustrating the second half of the process of manufacturing the semiconductor device according to the eleventh embodiment;

FIG. 19 is a cross-sectional view of a conventional semiconductor device;

FIGS. 20(a) to 20(g) are cross-sectional views illustrating a process of manufacturing the conventional semiconductor device; and

FIGS. 21(a) and 21(b) are cross-sectional views for illustrating the wiring-to-substrate capacitance in each of a conventional trench-isolated semiconductor device and a conventional LOCOS-isolated semiconductor device.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to the drawings, the embodiments of the present invention will be described.
(First Embodiment)

FIG. 1(a) is a cross-sectional view of a semiconductor device having a MOSFET according to a first embodiment. As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as the MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Each of the semiconductor portions 9 formed in the isolation region 7 is provided with an impurity diffusion layer 21 into which an N-type impurity of the conductivity type opposite to that of the silicon substrate 1 has been introduced, so that a PN junction 22 is formed between the impurity diffusion layer 21 and the silicon substrate 1. The PN junction 22 is positioned at a level between those of the top and bottom faces of the trench portions 8.

FIG. 1(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance in the isolation region 7 of the semiconductor device according to the present embodiment. As shown in the drawing, the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment includes the components of capacitances Ca1 and Ca2, similarly to the wiring-to-substrate capacitance of the conventional semiconductor device shown in FIG. 21(a). Moreover, since the PN junction 22 is formed in each of the semiconductor portions 9, another capacitance Cj1 is added in series to the capacitance Ca1. Hence, the total wiring-to-substrate capacitance Cjt is represented by the following equation (3):

$$C_{jt} = \Sigma \{ (C_{at} \times C_{j1}) / (C_{at} + C_{j1}) \} + \Sigma C_{a2} \quad (3),$$

which is smaller than the total capacitance Cat represented by the equation (1). Accordingly, the following inequality (4) is satisfied (4):

Cjt < Cat

(4).

Thus, the wiring-to-substrate capacitance can be reduced in the semiconductor device according to the present embodiment owing to the PN junction 22 present in each of the dummy semiconductor portions 9 of the isolation region 7, which increases the operating speed of the semiconductor device.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 2(a) to 2(g) are cross-sectional views showing the structure of the semiconductor device having the NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 2(a), the thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 2(b), the plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active 6 region by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 2(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 2(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wires and the silicon substrate.

In the step shown in FIG. 2(e), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wires 10 by using a known technique. The gate electrode 4 and the polysilicon wires 10 can be formed simultaneously by using a common mask.

In the step shown in FIG. 2(f), arsenic ions 25 are implanted not only into the active region 6 but also into the entire isolation region 7. As a result, the NMOSFET having the source/drain regions 5 is formed in the active region 6. On the other hand, an N-type impurity diffusion layer 31 is formed in each of the dummy semiconductor portions 6 of the isolation region 7, resulting in a PN junction 32 formed between the N-type impurity diffusion layer 31 and the P-type silicon substrate 1. The present embodiment is characterized in that the PN junction 32 is positioned between the top and bottom faces of the buried trench portions 8.

In the step shown in FIG. 2(g), the silicon oxide film is deposited to form the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

In the case of providing the MOSFET in the active region as provided in accordance with the manufacturing method of

the present embodiment, the PN junction 22 in each of the semiconductor portions 9 can be formed easily through the implantation of ions for forming the source/drain regions 5, so that manufacturing cost is not increased.

Although the present embodiment has described the case of using the P-type silicon substrate, it will be appreciated that the same effects as achieved in the present embodiment are also achieved in the case of using an N-type silicon substrate by introducing a P-type impurity into the upper portions of the semiconductor portions located between the individual trench portions and thereby forming the PN junctions between the resulting P-type impurity diffusion layers and the N-type silicon substrate.

Although the formation of the PN junctions 32 in the dummy semiconductor portions 9 of the isolation region 7 has been performed simultaneously with the formation of the source/drain regions 5 in the manufacturing method of the present embodiment, the formation of the dummy semiconductor portions 9 may be preformed at any stage of the process of manufacturing the semiconductor device, provided that the PN junctions can be formed in the dummy semiconductor portions.

(Second Embodiment)

FIG. 3 is a cross-sectional view of a semiconductor device according to a second embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Each of the semiconductor portions 9 formed in the isolation region 7 is provided with an impurity diffusion layer 31 into which an N-type impurity of the conductivity type opposite to that of the impurity introduced into the silicon substrate 1 has been introduced, so that a PN junction 32 is formed between the impurity diffusion layer 31 and the silicon substrate 1. The PN junction 32 is positioned at a level lower than the bottom faces of the trench portions 8.

The wiring-to-substrate capacitance in the isolation region 7 of the present embodiment is represented by the following equation (5):

$$C_{jt} = \sum \{ (C_{a1} \times C_{j1}) / (C_{a1} + C_{j1}) \} + \sum \{ (C_{a2} \times C_{k1}) / (C_{a2} + C_{k1}) \} \quad (5)$$

which is smaller than the total capacitance C_{at} represented by the equation (1). In the foregoing equation (5), C_{k1} represents the capacitance between the bottom face of the trench portion 8 and the PN junction 32. Hence, the following inequality (6) is satisfied, similarly to the first embodiment:

$$C_{jt} < C_{at} \quad (6)$$

Thus, the wiring-to-substrate capacitance can also be reduced in the semiconductor device according to the present embodiment since the PN junction 32 is present in

each of the dummy semiconductor portions 9 of the isolation region 7, similarly to the first embodiment, so that the operating speed of the semiconductor device is increased. In particular, the present embodiment can reduce the wiring-to-substrate capacitance in the entire isolation region containing not only the semiconductor portions 9 but also the trench portions, so that the effect of increasing the operating speed is remarkable.

Although it is difficult to form the PN junction 32 as formed in the present embodiment through the implantation of impurity ions for forming the source/drain regions of the MOSFET, the impurity concentration and the depth of ionic penetration into the substrate can be controlled arbitrarily, so that a higher effect of reducing the capacitance is achieved. In particular, since the PN junction 32 is positioned at a level lower than the bottom faces of the trench portions 8, a higher effect of reducing the capacitance is achieved.

Although the present embodiment has described the case of using the P-type silicon substrate, an N-type silicon substrate may also be used instead. In this case, a PN junction can be formed by introducing a P-type impurity into the semiconductor portions and thereby forming an impurity diffusion layer, so that the same effects as achieved in the present embodiment are achieved.

(Third Embodiment)

FIG. 4 is a cross-sectional view of a semiconductor device according to a third embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Each of the dummy semiconductor portions 9 formed in the isolation region 7 is provided with a P-type impurity diffusion layer 41 and an N-type impurity diffusion layer 42, which are arranged in this order from the surface of the silicon substrate. As a result, a first PN junction 43 is formed between the P-type impurity diffusion layer 41 and the N-type impurity diffusion layer 42, while a second PN junction 44 is formed between the N-type impurity diffusion layer 42 and the P-type silicon substrate 1. The first and second PN junctions 43 and 44 are positioned at levels between the top and bottom faces of the trench portions 8.

If respective junction capacitances in the P-type and N-type impurity diffusion layers 41 and 42 are designated at C_{j1} and C_{j2} , a total wiring-to-substrate capacitance C_{jt} in the semiconductor device according to the present embodiment is represented by the following equation (7):

$$C_{jt} = \sum \{ 1 / [(1/C_{a1}) + (1/C_{j1}) + (1/C_{j2})] \} + \sum C_{a2} \quad (7)$$

which is smaller than the total capacitance C_{at} of the semiconductor device according to the first embodiment represented by the equation (1). Hence, the following equation (8) is satisfied:

$$C_{jt} < C_{at}$$

Since the present embodiment has provided the plurality of PN junctions **43** and **44** in the respective dummy semiconductor portions of the isolation region **7**, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions **9** of the semiconductor device can be represented by the capacitance obtained by connecting in series the respective capacitances in the P-type and N-type impurity diffusion layers **41** and **42** to the capacitance in the interlayer insulating film. Consequently, the wiring-to-substrate capacitance of the semiconductor device can further be reduced than in the first embodiment, resulting in the semiconductor device operating at a higher speed.

Although the present embodiment has described the case where the two PN junctions **43** and **44** are formed of the two impurity diffusion layers, if three or more PN junctions are formed of three or more impurity diffusion layers, the total wiring-to-substrate capacitance can be represented in the same fashion as represented by the equation (7). For example, if m PN junctions (m is an integer equal to or more than 3) are formed in each of the dummy active regions **9** and n PN junctions (n is an integer equal to or more than 3) are formed immediately under the trench portion **8**, the total wiring-to-substrate capacitance C_{jt} is represented by the following equation (9):

$$C_{jt} = \Sigma \{ 1 / (1/Ca1 + \Sigma (1/Cjm)) \} + \Sigma \{ 1 / (1/Ca2 + \Sigma (1/Cjn)) \} \quad (9),$$

which is smaller than the total capacitance Cat represented by the equation (1). Hence, the following inequality (10) is satisfied:

$$C_{jt} < Cat \quad (10).$$

In the case of using the structure, the wiring-to-substrate capacitance can be reduced significantly since not only the capacitance component in the region containing the semiconductor portions of the isolation region **7** but also the capacitance component in the region containing the trench portions thereof is also reduced.

(Fourth embodiment)

FIG. 5 is a cross-sectional view of a semiconductor device according to a fourth embodiment.

As shown in the drawing, a first active region **6** of a P-type silicon substrate **1** is provided with an element functioning as a MOSFET composed of: a gate oxide film **2**; a gate electrode **4** made of a polysilicon film; and source/drain regions **5**. An isolation region **7** for electrically isolating the individual elements is formed with a plurality of trench portions **8** each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions **9** provided between the individual trench portions **8** and not serving as active regions. On one of the trench portions **8** formed in the isolation region **7**, there is provided a polysilicon wire **10** formed simultaneously with the gate insulating film **2** and the gate electrode **4**. In addition, a dummy gate **51** composed of a polysilicon film formed simultaneously with the gate electrode **4** extends continuously over the semiconductor portions **9** and trench portions **8**. Over the dummy gate **51**, the polysilicon wire **10**, and a surface of the silicon substrate (except for the active region), a silicon oxide film **52** and a high resistor film **53** composed of a polysilicon film are further formed in layers. The dummy gate **51** has been formed by patterning a first-layer polysilicon film used commonly to form the gate electrode **4** and the polysilicon wire **10** so that it is at a given distance from each of the gate electrode **4** and the polysilicon wire **10**. The polysilicon film composing the high resistor film **53** has a

sheet resistance film higher than that of the first-layer polysilicon film composing the gate electrode **4** and the like and an impurity concentration of $1 \times 10^{20} \text{ cm}^{-3}$ or less. The sheet resistance of the dummy gate **51** can also be held high by covering the isolation region with a resist film or the like during the implantation of an impurity into the active region.

In the semiconductor device according to the present embodiment, it is sufficient to consider the capacitance between the wiring and high resistor film instead of the capacitance between the wiring and substrate. In this case, since the resistance of the polysilicon film composing the high resistor film **53** is high, a voltage drop occurs between the top face of the high resistor film **53** and the surface of the semiconductor substrate **1**. Accordingly, the voltage applied to the top and bottom faces of the interlayer insulating film is reduced, though the capacitance of the interlayer insulating film **12** remains unchanged. Since the amount of charge accumulated in the top and bottom faces of the interlayer insulating film **12** decreases in direct proportion to the voltage applied thereto, the time required for charging or discharging between the wiring and high resistor is reduced, resulting in the semiconductor device operating at a higher speed.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 6(a) to 6(h) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 6(a), a thin silicon oxide film **21** having a thickness of 10 nm and a silicon nitride film **22** are formed sequentially on the P-type silicon substrate **1**.

In the step shown in FIG. 6(b), a plurality of trenches **14** each having a given width are formed in the silicon substrate **1**. The trenches **14** include: trenches **14a** formed to surround the active region **6** to be formed with the element; trenches **14b** formed in the isolation region **7** separated from the active region **6** by the trenches **14a** to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches **14c** for forming the polysilicon wires. In the isolation region **7** also, the semiconductor portions **9** have been provided to form at least one projecting portion surrounded by the trenches **14**. The semiconductor portions **9** may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire **10**, which is to be formed in the subsequent step.

In the step shown in FIG. 6(c), a silicon oxide film **23** is deposited over the entire surface of the substrate to fill in the trenches **14**.

In the step shown in FIG. 6(d), the silicon oxide film **23** is polished by a CMP process. Subsequently, the silicon nitride film **22** and the silicon oxide film **21** are removed selectively to form a plurality of buried trench portions **8** each filled with a silicon oxide film and having a planarized surface. The buried trench portions **8** include: buried trench portions **8a** functioning as isolation; buried trench portions **8b** forming the dummy semiconductor portions **9**; and buried trench portions **8c** for providing insulation between the polysilicon wires and the silicon substrate.

In the step shown in FIG. 6(e), there are formed the gate oxide film **2**, the gate electrode **4** having sidewalls **24** on the side faces thereof, and the polysilicon wires **10** by using a known technique. During the process, the dummy gate **51** is formed simultaneously with the gate electrode **4** and the polysilicon wire and at a given distance from each of the

gate electrode 4 and the polysilicon wire 10, so that the dummy gate 51 neither cross nor contact the gate electrode 4 and the polysilicon wire 10. The gate electrode 4, the polysilicon wire 10, and the dummy gate 51 can be formed simultaneously by using a common semiconductor mask. The dummy gate 51 has a sheet resistance higher than those of the gate electrode 4 and polysilicon wire 10, which are used as interconnections, and has an impurity concentration adjusted to be 1×10^{20} atoms/cm³ or lower by ion implantation or the like.

In the step shown in FIG. 6(f), the silicon oxide film 52 and the high resistor film 53 made of polysilicon are formed over the isolation region 7. The high resistor film 53 has a sheet resistance higher than those of the gate electrode 4 and polysilicon wires 10 and has an impurity concentration adjusted to be 1×10^{20} atoms/cm³ or lower by ion implantation or the like. The silicon oxide film 52 and the high resistor film 53 are formed to provide a MIM capacitor and a resistor.

In the step shown in FIG. 6(g), a resist mask 55 covering at least the isolation region 7 is formed and arsenic ions 25 are implanted into the active region 6 to form the NMOS having the source/drain regions 5. During the process, arsenic ions are not implanted in the isolation region 7.

In the step shown in FIG. 6(h), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

In the semiconductor device according to the present embodiment, it is sufficient to consider the capacitance between the wiring and high resistor film instead of the capacitance between the wiring and substrate. In this case, since the resistance of the polysilicon film composing the high resistor film 53 is high, a voltage drop occurs between the top face of the high resistor film 53 and the surface of the semiconductor substrate 1. Accordingly, the voltage applied to the top and bottom faces of the interlayer insulating film is reduced, though the capacitance of the interlayer insulating film 12 remains unchanged. Since the amount of charge accumulated in the top and bottom faces of the interlayer insulating film 12 decreases in direct proportion to the voltage applied thereto, the time required for charging or discharging between the wiring and high resistor is reduced, resulting in the semiconductor device operating at a higher speed.

The high-resistance film 53 according to the present embodiment can be formed easily at low cost by patterning the same film as composing, e.g., the high resistor film of the resistor element and local wiring. Instead of forming the dummy gate 51, it is possible to form films corresponding to the high resistor film 53, the silicon oxide film 52, and the dummy gate 51 from three films composing the upper-layer film, capacitor insulating film, and lower-layer film composing the MIM capacitor formed anywhere on the semiconductor substrate.

It is also possible to increase the operating speed of the semiconductor device by reducing the time required for charging or discharging without forming either of the dummy gate 51 and the high resistor film 53 as well as the silicon oxide film 52.

Although the description has been given to the case where the high resistor film 53 composed of the polysilicon film and the silicon oxide film 52 are stacked in layers on the isolation region 7, similar effects can also be achieved in the case of using an amorphous silicon film or a silicon nitride film instead of the polysilicon film. In particular, the use of an insulating film composed of a silicon oxide film allows a reduction in total capacitance and a further increase in the operating speed of the semiconductor device.

(Fifth Embodiment)

FIG. 7 is a cross-sectional view of a semiconductor device according to a fifth embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate electrode 4.

In the present embodiment, the gate electrode 4 consists of a lower-layer portion 4a made of a first conductor film composed of a polysilicon film or the like and an upper-layer portion 4b made of a second conductor film composed of a tungsten film or the like. In the isolation region 7, there is provided a dummy gate 51 consisting of a lower-layer portion 51a composed of the same first conductor film as composing the lower-layer portion 4a of the gate electrode 4 and an upper-layer portion 51b composed of the same second conductor film composing the upper-layer portion 4b of the gate electrode 4. The lower-layer portion 51a of the dummy gate 51 has a top surface at the same level as the top face of each of the trench portions 8, so that planarization is achieved between the lower-layer portion 51a and the trench portions 8. The polysilicon wire 10 is composed only of the second conductor film composing the upper-layer portion 4b of the gate electrode 4. The dummy gate 51 has been formed at a given distance from each of the gate electrode 4 and polysilicon wire 10 so as to improve pattern accuracy in a photolithographic process in accordance with a line-and-space relationship. There are also provided an interlayer insulating film 12 composed of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

In accordance with a process of manufacturing the semiconductor device according to the present embodiment, the structure of the semiconductor device as shown in FIG. 7 can be implemented by the following procedure, though the drawing thereof is omitted here.

First, the gate insulating film and the first conductor film composed of a polysilicon film or the like are deposited on the semiconductor substrate, which are partially opened to form trenches. Thereafter, an insulating film is deposited on the substrate to fill in the trenches for planarization, thereby forming trench portions. Subsequently, the second conductor film of tungsten or the like is deposited on the planarized substrate and patterned to form the gate electrode 4, the dummy gate 51, and the polysilicon wires 10. After that, the interlayer insulating film 12 and the metal wire 13 can be formed by a well-known method.

In the present embodiment also, the operating speed can be increased by reducing the amount of charge accumulated in the top and bottom faces of the interlayer insulating film, similarly to the fourth embodiment. In the semiconductor device having such a structure as used in the present embodiment, the upper-layer portion 4b of the gate electrode 4 is typically composed of a low resistor film composed of silicide or the like. However, since the wiring-to-substrate voltage is also applied in series to the upper-layer and lower-layer portions 4b and 4a, the amount of charge is effectively reduced by a voltage drop and the operating speed of the semiconductor device is increased remarkably.

Although the present embodiment has not used such a high resistor film as used in the fourth embodiment, it will be appreciated that a high resistor film may be provided over the dummy gate with an insulating film interposed therebetween.

(Sixth Embodiment)

FIG. 8 is a cross-sectional view of a semiconductor device according to a sixth embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

In the isolation region 7, inter-trench insulating films 61 each composed of a silicon oxide film and surrounded by the trench portions 8 are formed to overlie the dummy semiconductor portions 9 and underlie the interlayer insulating film 12. The top faces of the inter-trench insulating films 61 are at the same level as the top faces of the buried trench portions 8, while the bottom faces thereof are at a level between the top and bottom faces of the buried trench portions 8.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 9(a) to 9(i) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 9(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 9(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 9(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 9(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface.

The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wires and the silicon substrate.

In the step shown in FIG. 9(e), the semiconductor portions of the isolation region 7 are subjected to dry etching for forming trenches 62.

In the step shown in FIG. 9(f), as silicon oxide film is filled in each of the trenches 62 to form the inter-trench insulating film 61.

In the step shown in FIG. 9(g), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 and the polysilicon wire 10 can be formed simultaneously by using a common semiconductor mask.

In the step shown in FIG. 9(h), arsenic ions 25 are implanted from above to form the NMOSFET having the source/drain regions in the active region 6. Although the arsenic ions 25 are also implanted into the isolation region 25 during the process, no trouble occurs. In the case of using a resist mask covering a region to be formed with a PMOSFET, however, the isolation region 7 may be covered with the resist mask.

In the step shown in FIG. 9(i), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

In the semiconductor device according to the present embodiment, the inter-trench insulating films 61 each composed of the silicon oxide film are formed over the dummy semiconductor portions 9 of the isolation region 7 and under the interlayer insulating film 12 to be surrounded by the buried trench portions 8. The top faces of the inter-trench insulating films 61 are at the same level as the top faces of the buried trench portions 8, while the bottom faces thereof are at a level between the top and bottom faces of the buried trench portions 8.

Thus, in the semiconductor device according to the present embodiment, the inter-trench insulating films 61 are formed by filling the silicon oxide films in the respective dummy semiconductor portions 9 that have been lowered in level, so that the distance between the wiring and the substrate is longer than in the conventional semiconductor device shown in FIG. 19. Since the wiring-to-substrate capacitance decreases in inverse proportion to the distance, the wiring-to-substrate capacitance is smaller in the semiconductor device according to the present embodiment than in the conventional semiconductor device, resulting in a higher operating speed.

Although the present embodiment has described the case where the silicon oxide film is buried in each of the semiconductor portions, similar effects can also be achieved if an insulating film composed of a silicon nitride film is used.

Although the semiconductor portions 9 have been lowered in level and filled with the silicon oxide films prior to the formation of the gate electrode, the method of manufacturing a semiconductor device according to the present invention is not limited to such an embodiment. The same effects as achieved in the present embodiment can also be achieved if the steps of lowering the semiconductor portions 9 in level and filling the silicon oxide films therein are performed after the formation of the gate electrode or prior to the formation of trench isolation.

(Seventh Embodiment)

FIG. 10 is a cross-sectional view of a semiconductor device according to a seventh embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

In upper portions of the dummy semiconductor portions 9 of the isolation region 7, oxygen atoms have been introduced by ion implantation or the like to form high resistor portions 71 each composed of a high-resistance silicon layer. Although the bottom faces of the high resistor portions 71 are at a level between the top and bottom faces of the trench portions 8, they may be positioned at a level lower than the bottom faces of the trench portions 8.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 11(a) to 11(h) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 11(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 11(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 11(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 11(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 11(e), a resist mask 73 covering the active region 6 is formed and oxygen ions 72 are implanted only into the isolation region 7 to form the high resistor portions 71 in the outermost surface of the silicon

substrate, in which the oxygen ions have been introduced as an impurity in the semiconductor portions 9 of the isolation region 7.

In the step shown in FIG. 11(f), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 and the polysilicon wire 10 can be formed simultaneously by using a common semiconductor mask.

In the step shown in FIG. 11(g), arsenic ions are implanted from above the substrate to form the NMOSFET having the source/drain regions 5 in the active region 6. Although the arsenic ions 25 are also implanted into the isolation region 7 during the process, no trouble occurs. In the case of using a resist mask covering a region to be formed with a PMOSFET, however, the isolation region 7 may be covered with the resist mask.

In the step shown in FIG. 11(h), a silicon oxide film is formed as the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

The semiconductor device according to the present embodiment is characterized in that the oxygen atoms have been introduced into the upper portions of the semiconductor portions 9 of the isolation region 7 by ion implantation or the like to form the high resistor portions 71 each composed of a high-resistance silicon layer. Although the bottom faces of the high resistor portions 71 are at a level between the top and bottom faces of the buried trench portions 8, they may be positioned at a level lower than the bottom faces of the buried trench portions 8.

Since the high resistor portions 71 each composed of a high-resistance silicon layer have been formed in the dummy semiconductor portions 9 of the silicon substrate, a voltage drop occurs in the high resistor portions 71 of the silicon substrate when a voltage is placed between the wiring and the substrate. Consequently, a potential difference between the wiring and semiconductor portions 9 is reduced so that the amount of charge is reduced in direct proportion to the placed voltage, though the capacitance of the interlayer insulating film 12 between the wiring and the semiconductor portions 9 is equal to that of the interlayer insulating film 12 in the conventional semiconductor device shown in FIG. 19. Accordingly, the time required for charging or discharging is reduced and the operating speed of the semiconductor device is increased.

Although the present embodiment has described the case where oxygen atoms are introduced as an impurity into the dummy semiconductor portions 9, similar effects can be achieved if nitrogen atoms are introduced.

Although the high resistor portions are formed prior to the formation of the gate electrode in the present embodiment, they may be formed at any stage of the process of manufacturing the semiconductor device provided that oxygen atoms can be introduced into the semiconductor portions.

(Eighth Embodiment)

FIG. 12 is a cross-sectional view of a semiconductor device according to an eighth embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; sidewalls 3 formed on the side faces of the gate electrode 4 and composed of silicon oxide films; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the

individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Over the dummy semiconductor portions 9 and trench portions 8 of the isolation region 7, an underlying insulating film 81 made of a silicon oxide film has been formed simultaneously with the sidewalls on the side faces of the gate electrode 4. The underlying insulating film 81 has been formed to cover the entire polysilicon wire 10.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 13(a) to 13(i) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 13(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 13(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 13(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 13(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 13(e), there are formed the gate oxide film 2, the gate electrode 4 made of polysilicon, and the polysilicon wire 10 by using a known technique. The gate electrode 4 can be formed simultaneously with the polysilicon wire by using a common semiconductor mask.

In the step shown in FIG. 13(f), a silicon oxide film 82 is deposited over the entire surface of the substrate, followed by a resist mask 84 formed thereon to cover the isolation region 7.

In the step shown in FIG. 13(g), a silicon oxide film 82 is removed selectively by anisotropic dry etching using the resist mask 84 to form an underlying insulating film 81 over the isolation region 7, while the sidewalls are formed on the side faces of the gate electrode 4. The polysilicon wire 10 is completely covered with the underlying insulating film 81.

In the step shown in FIG. 13(h), arsenic ions 25 are implanted from above to form the NMOSFET having the source/drain regions 5 in the active region 6. Although the arsenic ions are also implanted into the isolation region 7 during the process, no trouble occurs. However, in the case of using a resist mask covering a region to be formed with a PMOSFET, the isolation region 7 may be covered with the resist mask.

In the step shown in FIG. 13(i), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

The semiconductor device according to the present embodiment is characterized in that the underlying insulating film 81 composed of the silicon oxide film is formed simultaneously with the sidewalls on the side faces of the gate electrode 4 to extend over the dummy semiconductor portions 9 and buried trench portions 8 of the isolation region 7. The resulting underlying insulating film 81 covers the entire polysilicon wire 10.

Thus, in the semiconductor device according to the present embodiment, the underlying insulating film 81 composed of the silicon oxide film is present over the isolation region 7, so that the distance between the wiring and the substrate is longer than in the conventional semiconductor device shown in FIG. 19. Since the wiring-to-substrate capacitance decreases in inverse proportion to the distance, the wiring-to-substrate capacitance is reduced in the semiconductor device according to the present embodiment, resulting in a higher operating speed.

Although the present embodiment has described the case where the underlying insulating film 81 is composed of the silicon oxide film, similar effects can also be achieved if an insulating film composed of a silicon nitride film is used.

Although the present embodiment has described the case where the underlying insulating film is composed of a single-layer film, the underlying insulating film may be composed of a multi-layer film. For example, in the case where the sidewalls consist of L-shaped portions extending over the side faces of the gate electrode and the substrate and of upper wedge-shaped portions or, alternatively, the sidewalls are provided along with an on-gate protective film, the underlying insulating film should be composed of a multi-layer film. It will be appreciated that, in that case also, the same effects as achieved in the present embodiment are achieved.

(Ninth Embodiment)

FIG. 14(a) is a cross-sectional view of a semiconductor device according to a ninth embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Under the dummy semiconductor portions 9 and the trench portions 8, a buried insulating film 91 composed of a

silicon oxide film is formed in contact with the bottom faces of the trench portions 8. As a result, the side faces of the semiconductor portions 9 are in contact with the trench portions 8, while the bottom faces thereof are in contact with the buried insulating film 91.

FIG. 14(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment. In the semiconductor device according to the present embodiment, since the buried insulating film 91 composed of the silicon oxide film is formed in the silicon substrate, the capacitance C_{ij} becomes a half of the capacitance C_{j1} shown in FIG. 1(b) or less (T. Nishimura and Y. Inoue: Proceedings of VLSI TECHNOLOGY WORKSHOP ON "WHAT IS THE FUTURE OF SOI?" (1995) p.123).

Therefore, the total wiring-to-substrate capacitance C_{ijt} of the semiconductor device is represented by the following equation (11):

$$C_{ijt} = \{(Ca1 \times C_{ij}) / (Ca1 + C_{ij})\} + \Sigma Ca2 \quad (11)$$

which is smaller than the total capacitance C_{it} represented by the equation (3). Accordingly, the following inequality (12) is satisfied:

$$C_{ijt} < C_{it} \quad (12)$$

Hence,

$$C_{ijt} < Ca1$$

is derived from the relationship represented by the equation (4), so that the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment is reduced, resulting in the semiconductor device operating at a higher speed.

FIGS. 15(a) to 15(h) are cross-sectional views of the structure of the semiconductor device having the NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 15(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 15(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 15(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 15(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench

portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 15(e), a resist mask 92 covering the active region 6 is formed and oxygen ions 93 are implanted only into the isolation region 7 so that the buried insulating film 91 into which the oxygen atoms have been introduced as an impurity is formed. The buried insulating film 91 provides insulation between the silicon substrate 1 and the semiconductor portions 9 in the isolation region 7. In this case, the buried insulating film 91 is connected to the respective side faces of each of the individual trench portions 8a to 8c and energy for implanting the oxygen ions is set such that the semiconductor portions 9 are in the floating state.

In the step shown in FIG. 15(f), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 may be formed simultaneously with the polysilicon wire 10 by using a common semiconductor mask.

In the step shown in FIG. 15(g), a resist mask 95 is formed to cover the isolation region 7 and arsenic ions 25 are implanted into the active region 6 to form the NMOSFET having the source/drain regions 5. In this case, no implantation is performed with respect to the isolation region 7.

In the step shown in FIG. 15(h), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

In the semiconductor device formed by the manufacturing method according to the present embodiment, the buried insulating film 91 composed of the silicon oxide film is formed under the dummy semiconductor portions 9 and the buried trench portions 8 to be in contact with the bottom faces of the buried trench portions 8. As a result, the side faces of the semiconductor portions 9 are in contact with the buried trench portions 8, while the bottom faces thereof are in contact with the insulating film 91. Although the present embodiment has formed the buried insulating film by implanting oxygen ions prior to the formation of the gate electrode, the buried insulating film may be formed at any stage of the method of manufacturing the semiconductor device provided that oxygen atoms can be introduced into the semiconductor portions.

(Tenth Embodiment)

The present embodiment will basically describe another example of the manufacturing process shown in FIG. 14(b), which is for achieving the effect of capacitance reduction.

FIGS. 16(a) to 16(i) are cross-sectional views of the structure of a semiconductor device having an NMOSFET according to a tenth embodiment in the manufacturing process therefor.

In the step shown in FIG. 16(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on a P-type silicon substrate 1.

In the step shown in FIG. 16(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround an active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The trenches include one formed in a position immediately under

the polysilicon wire 10, which is to be formed in the subsequent step. In the step shown in FIG. 15(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 16(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 16(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively except for the portions overlying the active region 6 to form a plurality of buried trench portions 8 each filled with a silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 16(e), the semiconductor portions 9 of the isolation region 7 are subjected to dry etching for forming trenches 96.

In the step shown in FIG. 16(f), a silicon oxide film is deposited in each of the trenches 96 to form a buried insulating film 91, followed by a silicon film deposited thereon to form semiconductor portions 97 serving as dummy active regions. The buried insulating films 91 are in contact with the buried trench portions 8a to 8c.

In the step shown in FIG. 16(g), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 may be formed simultaneously with the polysilicon wire 10 by using a common semiconductor mask.

In the step shown in FIG. 16(h), a resist mask 98 is formed to cover the isolation region 7 and arsenic ions 25 are implanted into the active region 6 to form the NMOSFET having source/drain regions 5. In this case, implantation may be performed with respect to the isolation region 7, though it is not performed in the example.

In the step shown in FIG. 16(i), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

The manufacturing method according to the present embodiment also enables the formation of a semiconductor device having the same structure as the semiconductor device according to the ninth embodiment, resulting in smaller wiring-to-substrate capacitance and a higher operating speed.

Although the present embodiment has grown the silicon oxide films and the silicon films in the trenches 96 prior to forming the gate electrode, the silicon oxide films and the silicon films may be grown at any stage of the process of manufacturing the semiconductor device provided that they can be grown and buried in the trenches 96.

(Eleventh Embodiment)

The present embodiment will also basically describe still another example of the manufacturing process shown in FIG. 14(b), which is for achieving the effect of capacitance reduction.

FIGS. 17(a) to 17(f) and FIGS. 18(a) to 18(d) are cross-sectional views showing the structure of a semiconductor device having an NMOSFET according to an eleventh embodiment in the manufacturing process therefor.

In the step shown in FIG. 17(a), a trench 102 is formed in a region of a P-type silicon substrate 1 in which an isolation region is to be formed.

In the step shown in FIG. 17(b), a silicon oxide film is filled in the trench 102 to form an insulating film 101 so that the entire surface of the substrate is planarized.

In the step shown in FIG. 17(c), a silicon film 103 is epitaxially grown over the entire surface of the substrate. During the step, since single-crystal silicon is grown on single-crystal silicon in an active region 6, a semiconductor region having an excellent crystallographic property is formed therein, while a silicon film having an inferior crystallographic property is formed on the silicon oxide film in the isolation region 7. However, since the silicon film in the isolation region 7 does not function as an active region, the inferior crystallographic property thereof will not adversely affect the properties of the semiconductor device.

In the step shown in FIG. 17(d), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the silicon film 103.

In the step shown in FIG. 17(e), a plurality of trenches 14 each having a given width are formed in the substrate. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step. In forming the trenches 14, etching is performed till the surface of the buried insulating film 101 is exposed in the trenches 14.

In the step shown in FIG. 17(f), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 18(a), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form a plurality of buried trench portions 8 each filled with a silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 18(b), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 is formed simultaneously with the polysilicon wire 10.

In the step shown in FIG. 18(c), arsenic ions 25 are implanted into the active region 6 to form source/drain regions by using a resist mask 95 formed to cover the isolation region 7. The NMOSFET is formed by the foregoing process. Although arsenic ions 25 are not implanted in the isolation region 7 in the example, they may be implanted alternatively.

In the step shown in FIG. 18(d), a silicon oxide film is deposited to form an interlayer insulating film 12, followed by a metal wire 13 formed thereon.

The manufacturing method according to the present embodiment also enables the formation of a semiconductor device having the same structure as the semiconductor device according to the ninth embodiment, resulting in smaller wiring-to-substrate capacitance and a higher operating speed.

Although the present embodiment has formed the trench 102 in the silicon substrate 1 and buried the silicon oxide

film therein to form a miniaturized gate electrode 4, the silicon oxide film may be formed directly on the isolation region without forming the trench if the semiconductor substrate inferior in planarity does not adversely affect the patterning of the gate during the formation of the gate electrode.

(Variations of Individual Embodiments)

Although the eighth embodiments of the present invention have been described, there are variations obtained by combining the individual embodiments with each other.

By way of example, the first embodiment used in combination with the second to eighth embodiments achieves a further reduction in wiring-to-substrate capacitance and a reduction in time required for charging or discharging, so that the resulting semiconductor device operates at a higher speed than in the case where each of the embodiments is used singly.

Thus, according to the present invention, the individual embodiments used in combination can achieve more remarkable effects than in the case where each of the embodiments is used singly.

Although each of the embodiments has used the NMOS-FET as the element to be disposed in the active region 6, the present invention is not limited to such embodiments. The element includes an active element other than the MOSFET such as a bipolar transistor or diode or a passive element such as a capacitor.

We claim:

1. A method of manufacturing a semiconductor device, comprising:

a first step of forming, in a semiconductor substrate having a substrate region of a first conductivity type, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

a third step of forming an element on said active region; a fourth step of introducing an impurity containing at least an impurity of a second conductivity type into said dummy semiconductor portions of said isolation region to form at least one PN junction in said dummy semiconductor portions;

a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating film.

2. A method of manufacturing a semiconductor device according to claim 1, wherein said third and fourth steps include forming a gate electrode of a FET as said element on said active region, introducing the impurity of the second conductivity type into said active region and said dummy semiconductor portions, and thereby forming source/drain regions of said FET, while forming said at least one PN junction in said dummy semiconductor portions.

3. A method of manufacturing a semiconductor device according to claim 1, wherein

said third step includes forming a gate electrode of a FET as said element on said active region by using a first mask covering said isolation region and introducing the impurity of the second conductivity type into said active region to form source/drain regions of said FET and

said fourth step includes introducing the impurity containing at least the impurity of the second conductivity

type into said dummy semiconductor portions by using a second mask covering said active region to form said at least one PN junction in said dummy semiconductor portions.

4. A method of manufacturing a semiconductor device, comprising:

a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

a third step of forming an element on said active region;

a fourth step of forming a resistor film on each of said dummy semiconductor portions of said isolation region;

a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating film.

5. A method of manufacturing a semiconductor device according to claim 4, wherein said fourth step includes composing said resistor film of a film containing at least one of polysilicon and amorphous silicon.

6. A method of manufacturing a semiconductor device according to claim 4, wherein said fourth step includes composing said resistor film of a multilayer film constituted by two or more conductor films with at least an insulating film interposed therebetween.

7. A method of manufacturing a semiconductor device according to claim 4, wherein said fourth step includes introducing an impurity at a concentration of 1×10^{20} atoms/cm³ or lower into said resistor film.

8. A method of manufacturing a semiconductor device, comprising:

a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

a third step of forming an element on said active region;

a fourth step of implanting ions into an upper portion of each of said dummy semiconductor portions to form a high resistor portion therein;

a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating film.

9. A method of manufacturing a semiconductor device according to claim 8, wherein said fourth step includes implanting ions containing at least an atom having an oxidizing function to form said high resistor portion.

10. A method of manufacturing a semiconductor device according to claim 8, wherein said fourth step includes implanting ions containing at least an atom having a nitriding function to form said high resistor portion.

11. A method of manufacturing a semiconductor device, comprising:

- a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;
- a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;
- a third step of forming an element on said active region;
- a fourth step of forming an underlying insulating film over said dummy semiconductor portions of said isolation region;
- a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and
- a sixth step of forming a wire on said interlayer insulating film.

12. A method of manufacturing a semiconductor device according to claim 11, wherein said third step and said fourth step include forming a gate electrode of a FET forming said element on said active region, depositing a dielectric film on the substrate, performing anisotropic etching with respect to the dielectric film by using a mask covering said isolation region, and thereby leaving sidewalls on both side faces of said gate electrode, while leaving said underlying insulating film over said dummy semiconductor portions.

13. A method of manufacturing a semiconductor device according to claim 11, wherein said fourth step includes forming said underlying insulating film of a dielectric film containing at least silicon oxide.

14. A method of manufacturing a semiconductor device according to claim 11, wherein said fourth step includes forming said underlying insulating film of a dielectric film containing at least silicon nitride.

15. A method of manufacturing a semiconductor device, comprising:

- a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;
- a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;
- a third step of forming depressed portions by etching said dummy semiconductor portions and filling an insulating material in said depressed portions to form inter-trench insulating films each having a top face at the same level as respective top faces of said first and second buried trench portions;
- a fourth step of forming an element on said active region;
- a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and
- a sixth step of forming a wire on said interlayer insulating film.

16. A method of manufacturing a semiconductor device according to claim 15, wherein said fourth step includes forming each of said inter-trench insulating films of a dielectric film containing at least silicon oxide.

17. A method of manufacturing a semiconductor device according to claim 15, wherein said fourth step includes forming each of said inter-trench insulating films of a dielectric film containing at least silicon nitride.

18. A method of manufacturing a semiconductor device, comprising:

- a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;
- a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;
- a third step of implanting oxygen ions into each of said dummy semiconductor portions with said active region being covered by a mask to form a buried insulating film in an inner portion thereof;
- a fourth step of forming an element on said active region;
- a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and
- a sixth step of forming a wire on said interlayer insulating film.

19. A method of manufacturing a semiconductor device, comprising:

- a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;
- a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;
- a third step of forming third trenches by etching said semiconductor portions and filling an insulating material in said third trenches to form buried, insulating films each having a top face at a level lower than respective top faces of said first and second buried trench portions;
- a fourth step of growing semiconductor films on said buried insulating films, with said active region covered with a mask member, to form dummy semiconductor portions;
- a fifth step of forming an element on said active region;
- a sixth step of forming an interlayer insulating film over an entire surface of the substrate; and
- a seventh step of forming a wire on said interlayer insulating film.

20. A method of manufacturing a semiconductor device, comprising:

- a first step of forming, in a semiconductor substrate having a substrate region, a first trench extending over an entire isolation region of said substrate region, while leaving an active region of said substrate region;
- a second step of filling an insulating material in said first trench to form a buried insulating film having a top face at the same level as a top face of said isolation region;
- a third step of growing a semiconductor film over said active region and said buried insulating film;
- a fourth step of forming, in the semiconductor substrate, a second trench for partitioning said semiconductor film and said substrate region into the active region and the isolation region and a third trench for partitioning the portion of the semiconductor film overlying said isolation region into a plurality of dummy semiconductor portions;
- a fifth step of filling an insulating material in each of said second and third trenches to form a first buried trench portion and a second buried trench portion;

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a sixth step of forming an element on the portion of said semiconductor film overlying said active region;
a seventh step of forming an interlayer insulating film over an entire surface of the substrate; and

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an eighth step of forming a wire on said interlayer insulating film.

* * * * *

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PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

01/21/1998	DKING1	00000053	DAN:130203	08978137
01	FC:101	790.00	CH	
02	FC:102	738.00	CH	
03	FC:103	396.00	CH	

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103-39600

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Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney Docket No. 43889-677



PTO-FORM 1082 NEW APPLICATION TRANSMITTAL

Sir:

Transmitted herewith for filing is the X utility patent application of Inventors:

- (1) Takaaki UKEDA
- (2) Chiaki KUDO
- (3) Toshiki YABU

Entitled: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

Enclosed are:

1. The Papers Required For Filing Date Under 37 C.F.R. § 1.53(b):

- 72 Page(s) of Specification
- 14 Pages of Claims
- 1 Page of Abstract
- 21 Sheets of Drawings

2. X Executed Combined Declaration/Power of Attorney

3. Assignment

- X An Assignment (with Recordation Form Cover Sheet) of the invention to:

Matsushita Electric Industrial Co., Ltd.

4. Claim for Priority Under 35 U.S.C. § 120

- The benefit under 35 U.S.C. § 120 is hereby claimed from the following United States application(s):

5. Claim for Priority Under 35 U.S.C. § 119

- X The benefit of priority under 35 U.S.C. § 119 is hereby claimed from the following foreign application(s):

- (1) Japanese Patent Application No. 8-314762
Filed: 26 November 1996
- (2) Japanese Patent Application No. 9-023844
Filed: 06 February 1997

- A Letter submitting a certified copy of each above-identified foreign application(s) is enclosed.

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6. Fee Calculation

CLAIMS AS FILED

<u>Number Filed</u>	<u>Number Extra</u>	<u>Rate</u>	<u>Basic Fee</u> <u>\$ 790.00</u>
Total Claims	38-20	18 X \$ 22.00	396.00
Independent Claims	12- 3	9 X \$ 82.00	738.00
Multiple dependent claim(s), if any . _ \$270.00			0.00

Filing Fee Calculation

\$1924.00

- ☐ Amendment cancelling extra claims enclosed
- ☐ Amendment deleting multiple dependencies enclosed

7. Small Entity Statement

- ☐ A verified statement that this is a filing by a "small entity" under 37 C.F.R. §§ 1.9 and 1.27 is attached.
Filing Fee Calculation (50% of above) \$

8. Fee Payment

- ☒ Enclosed
 - ☒ Filing fee calculation above \$ 1924.00
 - ☒ Recording assignment (\$40.00; 37 C.F.R. § 1.21(h)(1)) \$ 40.00
- Total fees enclosed \$ 1964.00

9. Method of Payment of Fees

- ☒ Charge Deposit Account No. 13-0203 in the amount of \$1964.00

10. Other Enclosures: None

11. Authorization to Credit Overpayment or Charge Additional Fees

X The Commissioner is hereby authorized to credit any overpayment, or charge fees under 37 C.F.R. § 1.16 (filing fees) or 37 C.F.R. § 1.17 (application processing fees) which may be required, to Deposit Account No. 13-0203. A duplicate copy of this Transmittal Letter is attached for accounting purposes.

12. Conditional Petition For Extensions of Time

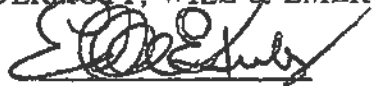
X Petition is hereby made under 37 C.F.R. § 1.136(a) for any extension of time required to ensure that any papers due in the U.S. Patent and Trademark Office during the pendency of this application are timely filed. Please charge any fees due for any extensions of time to Deposit Account No. 13-0203. A duplicate copy of this Transmittal Letter is attached for accounting purposes.

13. Correspondence Address:

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Respectfully submitted,

McDERMOTT, WILL & EMERY

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SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME



The present invention relates to a semiconductor device
providing a trench-isolated structure and, more particularly, to a
5 method of reducing the capacitance between the wiring and
substrate of the semiconductor device.

As higher-density and increasingly miniaturized
semiconductor devices have been implemented in recent years,
repeated attempts have been made to substitute a trench isolation
10 technique for a LOCOS technique which is most prevalently used
to form isolation for providing insulation between individual
elements of the semiconductor devices. In accordance with the
trench isolation technique, an insulating material is filled in
a trench formed in a semiconductor substrate to form isolation.

15 Since planarization of a surface of a semiconductor
substrate including the insulating material filled in the trench
is important to the trench isolation technique, chemical
mechanical polishing (CMP) has been used as a planarizing
technique which achieves excellent in-plane uniformity free from
20 pattern dependence. In the case where the trench occupies a large
area in a CMP process for planarization, the provision of dummy
island semiconductor portions has been proposed to avoid trouble
resulting from so-called pattern dependence, which causes
polishing properties to vary depending on the area of a region
25 to be planarized. In other words, the trench is divided into a

plurality of narrow trenches so that the surface of the semiconductor substrate is exposed between the individual trenches to form the dummy semiconductor portions which do not serve as active regions.

5 FIG. 19 shows an example of the conventional trench-isolated semiconductor device having the dummy island semiconductor portions.

As shown in FIG. 19, an active region 6 of a P-type silicon substrate 1 is formed with: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5 into which an impurity has been introduced. An isolation region 7 surrounding the active region 6 is formed with a plurality of trench portions 8 each filled with a silicon oxide film. Between the individual trench portions 8, there are provided semiconductor portions 9 having top surfaces at the same level as the top surfaces of the trench portions 8. On the trench portions 8 also, there is provided a polysilicon wire 10 formed simultaneously with the gate oxide film 2 and the gate electrode 4 of an element. An interlayer insulating film 12 is deposited over the entire surface of the substrate, followed by a metal wire 13 provided thereon.

In this case, if the trench portions have such large widths as shown in FIG. 21(b), a silicon oxide film filled in each of the trench portions is polished during the CMP process for planarizing the whole substrate so that the surface thereof is

depressed due to pattern dependence, which leads to the trouble of degraded planarity or the like. The isolation structure as shown in FIG. 19 has been proposed to prevent such trouble resulting from pattern dependence.

5 FIGS. 20(a) to 20(g) are cross-sectional views illustrating a process of manufacturing the conventional trench-isolated semiconductor device having an NMOS transistor.

10 In the step shown in FIG. 20(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

15 In the step shown in FIG. 20(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. However, the trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions.

20 In the step shown in FIG. 20(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in

the trenches 14.

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5 In the step shown in FIG. 20(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wires and the silicon substrate.

15 In the step shown in FIG. 20(e), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 and the polysilicon wire 10 are formed simultaneously.

20 In the step shown in FIG. 20(f), arsenic ions 25 are implanted into the active region 6 of the NMOSFET region by using a resist mask Rem covering the PMOSFET region and the isolation region to form the source/drain regions 5. The NMOSFET is formed by the foregoing process steps.

In the step shown in FIG. 20(g), the silicon oxide film is deposited to form the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

25 In the foregoing step shown in FIG. 20(f), ions of such an

impurity as phosphorus or arsenic have been implanted into the gate electrode 4 and source/drain regions 5 of the active region 6 in the step shown in FIG. 20(f). However, impurity ions are not implanted in principle in the region other than the active region 6, though they may be introduced slightly extensively into the periphery of the isolation region in considerations of mask displacement. Hence, impurity ions are not implanted in the dummy semiconductor portions 9 between the individual trench portions 8.

10 A description will be given to the wiring-to-substrate capacitance of the trench-isolated semiconductor device having the small trench portions 8 which are discretely located and the dummy semiconductor portions 9 as shown in FIG. 19 and in a semiconductor device having a wide isolating/insulating film such as a LOCOS film. FIG. 21(a) is a cross-sectional view for illustrating, by way of example, the wiring-to-substrate capacitance in the isolation region 7 having the dummy semiconductor portions 9. FIG. 21(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance of the semiconductor device having a LOCOS isolation film 100 and no dummy semiconductor portion. It is assumed here that impurity ions have not been implanted in the isolation region 7 during the implantation of ions into the source/drain regions and that the area occupied by the whole isolation region 7 is equal in each of the two semiconductor devices.

In the semiconductor device shown in FIG. 21(a), a total wiring-to-substrate capacitance C_{at} corresponds to the sum of capacitances C_{a1} and C_{a2} , which is represented by the following equation (1):

5 $C_{at} = \Sigma C_{a1} + \Sigma C_{a2} \quad \dots (1).$

In the case where a member interposed between the wiring and substrate is composed of a homogeneous material, the wiring-to-substrate capacitance per unit area is inversely proportional to the distance between the wiring and substrate, so that the
10 capacitance is larger as the distance is shorter. If the total wiring-to-substrate of the semiconductor device shown in FIG. 21(b) is represented by C_{bt} when the dimension D_{a2} shown in FIG. 21(a) is equal to the dimension D_{bt} shown in FIG. 21(b), the following inequality (2) is satisfied:

15 $C_{at} > C_{bt} \quad \dots (2),$

which indicates that the wiring-to-substrate capacitance C_{at} in the structure shown in FIG. 21(a) is larger than the wiring-to-substrate capacitance C_{bt} in the structure shown in FIG. 21(b).

Although the formation of the island pattern composed of
20 the dummy semiconductor portions in the isolation region has the advantage of achieving planarization with excellent in-plane uniformity, it also has the possibility of increasing the wiring-to-substrate capacitance and resultantly reducing the operating speed of the semiconductor device.

SUMMARY OF THE INVENTION

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In view of the foregoing, the present invention has been achieved based on the principle that, if each electrode of a parallel-plate capacitor occupies an equal area, the capacitance
5 of the capacitor is generally smaller as the distance between the electrodes is larger or on the physical phenomenon that, even when the capacitor has equal capacitance, the amount of charge accumulated therein is smaller as the voltage between the electrodes is lower.

10 It is therefore an object of the present invention to increase the operating speed of a trench-isolated semiconductor device comprising an isolation region consisting of trench portions and dummy semiconductor portions by providing therein means for reducing the wiring-to-substrate capacitance in the
15 isolation region or means for reducing the amount of charge accumulated in the capacitance present between the wiring and substrate in the isolation region.

A first semiconductor device according to the present invention comprises: a semiconductor substrate having an active
20 region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend
25 continuously over the active region and the isolation region; a

wire formed on the interlayer insulating film; and at least one PN junction formed in the semiconductor portions underlying the wire.

In the arrangement, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the upper portion of the PN junction of each of the semiconductor portions to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. Accordingly, the wiring-to-substrate capacitance of the whole semiconductor device is reduced, resulting in the semiconductor device operating at a higher speed.

The PN junction may include a plurality of PN junctions formed in the semiconductor portions.

The arrangement achieves a further reduction in wiring-to-substrate capacitance, resulting in a higher operating speed.

The active region may be formed with an impurity diffusion region and a PN junction may be formed at a bottom face of the impurity diffusion region, the PN junction of the isolation region being positioned at a level lower than the PN junction of the active region.

The arrangement further reduces the wiring-to-substrate capacitance.

A second semiconductor device according to the present

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invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; and a dielectric film interposed between at least the semiconductor portions of the isolation region and the interlayer insulating film.

In the arrangement, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the dielectric film to the capacitance in the interlayer insulating film, so that the total wiring-to-substrate capacitance is lowered. Consequently, the operating speed of the semiconductor device is increased.

As the dielectric film, an underlying insulating film may be provided between the interlayer insulating film and the semiconductor portions and trench portions.

There can be further provided a gate electrode formed on the semiconductor substrate within the active region and sidewalls made of an insulating material and formed on both side faces of the gate electrode such that the underlying insulating film is formed of the same film as forming the sidewalls.

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The underlying insulating film may be composed of a multilayer film.

The arrangement enables the underlying insulating film for reducing the wiring-to-substrate capacitance to be composed by
5 using the sidewalls required to form a MOSFET of so-called LDD structure. Consequently, the wiring-to-substrate capacitance can be reduced, while avoiding an increase in manufacturing cost.

The dielectric film may be formed in an upper portion of each of the semiconductor portions of the semiconductor substrate
10 to have a top face at approximately the same level as a top face of each of the trench portions.

Preferably, the dielectric film is composed of at least one of a silicon oxide film and a silicon nitride film.

A third semiconductor device according to the present
15 invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the
20 isolation region; an interlayer insulating film formed to extend continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; and a buried insulating film formed in an inner portion of each of the semiconductor portions in the isolation region.

25 The arrangement allows a reduction in the wiring-to-

substrate capacitance of the entire isolation region, resulting in a significant reduction in operating speed.

5 A fourth semiconductor device according to the present invention comprises: a semiconductor substrate having an active region and an isolation region surrounding the active region; a plurality of trench portions each formed in the isolation region and filled with an insulating material; semiconductor portions interposed between the individual trench portions in the isolation region; an interlayer insulating film formed to extend
10 continuously over the active region and the isolation region; a wire formed on the interlayer insulating film; an a resistor film formed between the interlayer insulating film and at least the semiconductor portions of the isolation region.

15 In the arrangement, a voltage drop in the resistor film reduces the amount of charge accumulated in the wiring-to-substrate capacitance in the region of the semiconductor device containing the resistor film, though the wiring-to-substrate capacitance is not reduced in the region. Consequently, the time required for charging or discharging is reduced, resulting in the
20 semiconductor device operating at a higher speed.

As the resistor film, an underlying resistor film may be formed to extend continuously over the semiconductor portions and trench portions.

25 The arrangement allows the wiring-to-substrate capacitance to be reduced by using various films having electric resistivity

which are formed on the semiconductor substrate.

There can further be provided a resistor element formed on the semiconductor substrate and having a high resistor film such that the underlying resistor film is formed of the same film as
5 composing the high resistor film of the resistor element.

In the arrangement, the underlying resistor film having the same resistance as the high resistor film used as a resistor element achieves a remarkable voltage dropping effect.

There can further be provided an element having an electrode
10 member composed of a conductor film formed on the semiconductor substrate within the active region such that the resistor film is composed of the same material as composing the electrode member.

There can further be provided a FET having a gate electrode
15 composed of a first conductor film formed on the semiconductor portion within the active region and a second conductor film deposited on the first conductor film such that a top surface of the first conductor film of the gate electrode is at approximately the same level as a top surface of each of the trench portions,
20 while a region of the resistor film overlying each of the semiconductor portions is formed of the same two films as composing the first and second conductor films of the gate electrode and a region of the resistor film overlying each of the trench portions is composed of the same material as composing the
25 first conductor film of the gate electrode.

Each of the arrangements eliminates the necessity for an additional step of forming the resistor film, so that the wiring-to-substrate capacitance is reduced, while an increase in manufacturing cost is prevented.

5 The resistor film may be formed in an upper portion of each of the semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top surface of each of the trench portions.

10 The resistor film may be composed of a silicon film containing at least one of an oxygen atom and a nitrogen atom.

 The resistor film may be composed of at least one of a polysilicon film and an amorphous silicon film.

15 The arrangement allows the formation of the resistor film by using the polysilicon film or amorphous silicon film to compose the gate electrode and the resistor element and thereby prevents an increase in manufacturing cost.

20 A first method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region of a first conductivity type, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second
25 trenches to form a first buried trench portion and a second buried

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trench portion; a third step of forming an element on the active region; a fourth step of introducing an impurity containing at least an impurity of a second conductivity type into the dummy semiconductor portions of the isolation region to form at least one PN junction in the dummy semiconductor portions; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

The method enables the formation of the semiconductor device including the dummy semiconductor portions each having the PN junction. The capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by adding in series the capacitance in the upper portion of the PN junction of each of the semiconductor portions to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. Accordingly, the wiring-to-substrate capacitance of the whole semiconductor device is reduced, resulting in the semiconductor device operating at a higher speed.

The third and fourth steps may include forming a gate electrode of a FET as the element on the active region, introducing the impurity of the second conductivity type into the active region and the dummy semiconductor portions, and thereby forming source/drain regions of the FET, while forming the at least one

PN junction in the dummy semiconductor portions.

The method enables the formation of the semiconductor device operating at a high speed by using a typical manufacturing process for forming a FET without an additional step of forming
5 the PN junction in each of the dummy semiconductor portions.

The third step may include forming a gate electrode of a FET as the element on the active region by using a first mask covering the isolation region and introducing the impurity of the second conductivity type into the active region to form
10 source/drain regions of the FET and the fourth step may include introducing the impurity containing at least the impurity of the second conductivity type into the dummy semiconductor portions by using a second mask covering the active region to form the at least one PN junction in the dummy semiconductor portions.

The method enables the formation of the semiconductor device having an arbitrary number of PN junctions without placing restraints on the depth and impurity concentration of the PN junction in the active region, resulting in a semiconductor device having minimum wiring-to-substrate capacitance.
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A second method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for
20 partitioning the isolation region into a plurality of dummy
25

semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming a resistor film on each of the dummy semiconductor portions of the isolation region; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

10 The method enables the formation of the semiconductor device comprising the resistor film between the interlayer insulating film and dummy semiconductor portions of the isolation region. A voltage drop in the resistor film reduces the amount of charge accumulated in the wiring-to-substrate capacitance, 15 though the wiring-to-substrate capacitance is not reduced in the region containing the resistor film of the semiconductor device. Consequently, the time required for charging or discharging is reduced, resulting in the semiconductor device operating at a higher speed.

20 The fourth step may include composing the resistor film of a film containing at least one of polysilicon and amorphous silicon.

The fourth step may include composing the resistor film of a multilayer film constituted by two or more conductor films with 25 at least an insulating film interposed therebetween.

The fourth step may include introducing an impurity at a concentration of 1×10^{20} atoms \cdot cm^{-3} or lower into the resistor film.

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A third method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of implanting ions into an upper portion of each of the dummy semiconductor portions to form a high resistor portion therein; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

The method allows the formation of the semiconductor device comprising the high resistor portion between the interlayer insulating film and dummy semiconductor portions of the isolation region. As described above, a voltage drop in the region containing the high resistor portion of the semiconductor device reduces the amount of charge accumulated in the wiring-to-substrate capacitance. What results is the semiconductor device

which requires a shorter time for charging or discharging and therefore operates insulating film at a higher speed.

The fourth step may include implanting ions containing at least an atom having an oxidizing function to form the high
5 resistor portion.

The fourth step may include implanting ions containing at least an atom having a nitriding function to form the high resistor portion.

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A fourth method of manufacturing a semiconductor device
10 according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy
15 semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming an underlying insulating film over the dummy
20 semiconductor portions of the isolation region; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

In accordance with the method, there is formed the
25 semiconductor device including the underlying insulating film

beneath the interlayer insulating film in the isolation region thereof. Consequently, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions of the isolation region is obtained by
5 adding in series the capacitance in the underlying insulating film to the capacitance in the interlayer insulating film, so that the total wiring-to-substrate capacitance is reduced. What results is the semiconductor device operating at a high speed.

10 The third step and the fourth step may include forming a gate electrode of a FET forming the element on the active region, depositing a dielectric film on the substrate, performing anisotropic etching with respect to the dielectric film by using a mask covering the isolation region, and thereby leaving sidewalls on both side faces of the gate electrode, while leaving
15 the underlying insulating film over the dummy semiconductor portions.

The method enables the formation of a semiconductor device operating at a high speed by using a typical manufacturing process for forming a FET without an additional step of forming the
20 underlying insulating film.

The fourth step may include forming the underlying insulating film of a dielectric film containing at least silicon oxide.

The fourth step may include forming the underlying
25 insulating film of a dielectric film containing at least silicon

nitride.

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A fifth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; a third step of forming an element on the active region; a fourth step of forming depressed portions by etching the dummy semiconductor portions and filling an insulating material in the depressed portions to form inter-trench insulating films each having a top face at the same level as respective top faces of the first and second buried trench portions; a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and a sixth step of forming a wire on the interlayer insulating film.

20 In accordance with the method, there is formed the semiconductor device comprising the inter-trench insulating films between the interlayer insulating films and dummy semiconductor portions of the isolation region thereof. Consequently, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor

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a wire on the interlayer insulating film.

A seventh method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region,
5 a first trench for partitioning the substrate region into an active region and an isolation region and a second trench for partitioning the isolation region into a plurality of dummy semiconductor portions; a second step of filling an insulating material in each of the first and second trenches to form a first
10 buried trench portion and a second buried trench portion; a third step of forming third trenches by etching the semiconductor portions and filling an insulating material in the third trenches to form buried insulating films each having a top face at a level lower than respective top faces of the first and second buried
15 trench portions; a fourth step of growing semiconductor films on the buried insulating films, with the active region covered with a mask member, to form dummy semiconductor portions; a sixth step of forming an interlayer insulating film over an entire surface of the substrate; a fifth step of forming an element on the active
20 region; a seventh step of forming a wire on the interlayer insulating film.

An eighth method of manufacturing a semiconductor device according to the present invention comprises: a first step of forming, in a semiconductor substrate having a substrate region,
25 a first trench extending over an entire isolation region of the

substrate region, while leaving an active region of the substrate region; a second step of filling an insulating material in the first trench to form a buried insulating film having a top face at the same level as a top face of the isolation region; a third
5 step of growing a semiconductor film over the active region and the buried insulating film; a fourth step of forming, in the semiconductor substrate, a second trench for partitioning the semiconductor film and the substrate region into the active region and the isolation region and a third trench for partitioning the
10 portion of the semiconductor film overlying the isolation region into a plurality of dummy semiconductor portions; a fifth step of filling an insulating material in each of the second and third trenches to form a first buried trench portion and a second buried trench portion; a sixth step of forming an element on the portion
15 of the semiconductor film overlying the active region; a seventh step of forming an interlayer insulating film over an entire surface of the substrate; and an eighth step of forming a wire on the interlayer insulating film.

In accordance with the methods, there are obtained
20 semiconductor devices each comprising a buried insulating film at a depth of each of the dummy semiconductor portions of the isolation region. What results is the semiconductor device having smaller wiring-to-substrate capacitance and operating at a higher speed.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(a) is a cross-sectional view of a semiconductor device according to a first embodiment, having shallow PN junctions formed in the semiconductor portions thereof and FIG.

5 1(b) is an enlarged cross-sectional view of an isolation region for illustrating the wiring-to-substrate capacitance in the semiconductor device;

FIGS. 2(a) to 2(g) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to
10 the first embodiment;

FIG. 3 is a cross-sectional view of a semiconductor device according to a second embodiment, having shallow PN junctions formed in the semiconductor portions thereof;

FIG. 4 is a cross-sectional view of a semiconductor device
15 according to a third embodiment, having two PN junctions in the semiconductor portions thereof;

FIG. 5 is a cross-sectional view of a semiconductor device according to a fourth embodiment, having a high resistor film formed on the semiconductor portions thereof;

20 FIGS. 6(a) to 6(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a fourth embodiment;

FIG. 7 is a cross-sectional view of a semiconductor device according to a fifth embodiment, having a multilayer gate provided
25 therein;

FIG. 8 is a cross-sectional view of a semiconductor device according to an eighth embodiment, having an inter-trench film formed on each of the semiconductor portions thereof;

FIGS. 9(a) to 9(i) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to the sixth embodiment;

FIG. 10 is a cross-sectional view of a semiconductor device according to a seventh embodiment, having a high resistor portion in the upper portion of each of the semiconductor portions;

FIGS. 11(a) to 11(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a seventh embodiment;

FIG. 12 is a cross-sectional view of a semiconductor device according to an eighth embodiment, having an underlying, having an underlying insulating film formed beneath an interlayer insulating film;

FIGS. 13(a) to 13(d) are cross-sectional views illustrating a process of manufacturing the semiconductor device according to the eighth embodiment;

FIG. 14(a) is a cross-sectional view of a semiconductor device according to a ninth embodiment, having a buried insulating film formed over the entire isolation region and FIG. 14(b) is an enlarged cross-sectional view of the isolation region for illustrating the wiring-to-substrate capacitance in the semiconductor device;

FIGS. 15(a) to 15(h) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to the ninth embodiment;

FIGS. 16(a) to 16(i) are cross-sectional views illustrating a process of manufacturing a semiconductor device according to a tenth embodiment;

FIGS. 17(a) to 17(f) are cross-sectional views illustrating the first half of a process of manufacturing a semiconductor device according to an eleventh embodiment;

FIGS. 18(a) to 18(d) are cross-sectional views illustrating the second half of the process of manufacturing the semiconductor device according to the eleventh embodiment;

FIG. 19 is a cross-sectional view of a conventional semiconductor device;

FIGS. 20(a) to 20(g) are cross-sectional views illustrating a process of manufacturing the conventional semiconductor device; and

FIG. 21 is a cross-sectional view for illustrating the wiring-to-substrate capacitance in each of a conventional trench-isolated semiconductor device and a conventional LOCOS-isolated semiconductor device.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to the drawings, the embodiments of the present invention will be described.

(First Embodiment)

FIG. 1(a) is a cross-sectional view of a semiconductor device having a MOSFET according to a first embodiment. As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as the MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Each of the semiconductor portions 9 formed in the isolation region 7 is provided with an impurity diffusion layer 21 into which an N-type impurity of the conductivity type opposite to that of the silicon substrate 1 has been introduced, so that a PN junction 22 is formed between the impurity diffusion layer 21 and the silicon substrate 1. The PN junction 22 is positioned at a level between those of the top and bottom faces of the trench portions

8.

FIG. 1(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance in the isolation region 7 of the semiconductor device according to the present embodiment. As shown in the drawing, the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment includes the components of capacitances $Ca1$ and $Ca2$, similarly to the wiring-to-substrate capacitance of the conventional semiconductor device shown in FIG. 21(a). Moreover, since the PN junction 22 is formed in each of the semiconductor portions 9, another capacitance $Cj1$ is added in series to the capacitance $Ca1$. Hence, the total wiring-to-substrate capacitance Cjt is represented by the following equation (3):

$$Cjt = \Sigma \{ (Ca1 \times Cj1) / (Ca1 + Cj1) \} + \Sigma Ca2 \quad \dots (3),$$

which is smaller than the total capacitance Cat represented by the equation(1). Accordingly, the following inequality (4) is satisfied(4):

$$Cjt < Cat \quad \dots (4).$$

Thus, the wiring-to-substrate capacitance can be reduced in the semiconductor device according to the present embodiment owing to the PN junction 22 present in each of the dummy semiconductor portions 9 of the isolation region 7, which increases the operating speed of the semiconductor device.

A description will be given next to a method of manufacturing a semiconductor device according to the present

embodiment. FIGS. 2(a) to 2(g) are cross-sectional views showing the structure of the semiconductor device having the NMOSFET according to the present embodiment in the manufacturing process therefor.

5 In the step shown in FIG. 2(a), the thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

10 In the step shown in FIG. 2(b), the plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active 6 region by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and
15 trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The
20 trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 2(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

25 In the step shown in FIG. 2(d), the silicon oxide film 23

is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The
5 buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wires and the silicon substrate.

10 In the step shown in FIG. 2(e), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wires 10 by using a known technique. The gate electrode 4 and the polysilicon wires 10 can be formed simultaneously by using a common mask.

15 In the step shown in FIG. 2(f), arsenic ions 25 are implanted not only into the active region 6 but also into the entire isolation region 7. As a result, the NMOSFET having the source/drain regions 5 is formed in the active region 6. On the other hand, an N-type impurity diffusion layer 31 is formed in each of the
20 dummy semiconductor portions 6 of the isolation region 7, resulting in a PN junction 32 formed between the N-type impurity diffusion layer 31 and the P-type silicon substrate 1. The present embodiment is characterized in that the PN junction 32 is positioned between the top and bottom faces of the buried trench
25 portions 8.

In the step shown in FIG. 2(g), the silicon oxide film is deposited to form the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

In the case of providing the MOSFET in the active region
5 as provided in accordance with the manufacturing method of the present embodiment, the PN junction 22 in each of the semiconductor portions 9 can be formed easily through the implantation of ions for forming the source/drain regions 5, so that manufacturing cost is not increased.

10 Although the present embodiment has described the case of using the P-type silicon substrate, it will be appreciated that the same effects as achieved in the present embodiment are also achieved in the case of using an N-type silicon substrate by introducing a P-type impurity into the upper portions of the
15 semiconductor portions located between the individual trench portions and thereby forming the PN junctions between the resulting P-type impurity diffusion layers and the N-type silicon substrate.

Although the formation of the PN junctions 32 in the dummy
20 semiconductor portions 9 of the isolation region 7 has been performed simultaneously with the formation of the source/drain regions 5 in the manufacturing method of the present embodiment, the formation of the dummy semiconductor portions 9 may be preformed at any stage of the process of manufacturing the
25 semiconductor device, provided that the PN junctions can be formed

in the dummy semiconductor portions.

(Second Embodiment)

FIG. 3 is a cross-sectional view of a semiconductor device according to a second embodiment.

5 As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is
10 formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided
15 a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

20 Each of the semiconductor portions 9 formed in the isolation region 7 is provided with an impurity diffusion layer 31 into which an N-type impurity of the conductivity type opposite to that of the impurity introduced into the silicon substrate 1 has been introduced, so that a PN junction 32 is formed between the impurity
25 diffusion layer 31 and the silicon substrate 1. The PN junction

32 is positioned at a level lower than the bottom faces of the trench portions 8.

The wiring-to-substrate capacitance in the isolation region 7 of the present embodiment is represented by the following equation (5):

$$C_{jt} = \sum \{ (C_{a1} \times C_{j1}) / (C_{a1} + C_{j1}) \} + \sum \{ (C_{a2} \times C_{k1}) / (C_{a2} + C_{k1}) \} \quad \dots (5),$$

which is smaller than the total capacitance C_{at} represented by the equation (1). In the foregoing equation (5), C_{k1} represents the capacitance between the bottom face of the trench portion 8 and the PN junction 32. Hence, the following inequality (6) is satisfied, similarly to the first embodiment:

$$C_{jt} < C_{at} \quad \dots (6).$$

Thus, the wiring-to-substrate capacitance can also be reduced in the semiconductor device according to the present embodiment since the PN junction 32 is present in each of the dummy semiconductor portions 9 of the isolation region 7, similarly to the first embodiment, so that the operating speed of the semiconductor device is increased. In particular, the present embodiment can reduce the wiring-to-substrate capacitance in the entire isolation region containing not only the semiconductor portions 9 but also the trench portions, so that the effect of increasing the operating speed is remarkable.

Although it is difficult to form the PN junction 32 as formed in the present embodiment through the implantation of impurity

ions for forming the source/drain regions of the MOSFET, the impurity concentration and the depth of ionic penetration into the substrate can be controlled arbitrarily, so that a higher effect of reducing the capacitance is achieved. In particular, 5 since the PN junction 32 is positioned at a level lower than the bottom faces of the trench portions 8, a higher effect of reducing the capacitance is achieved.

Although the present embodiment has described the case of using the P-type silicon substrate, an N-type silicon substrate 10 may also be used instead. In this case, a PN junction can be formed by introducing a P-type impurity into the semiconductor portions and thereby forming an impurity diffusion layer, so that the same effects as achieved in the present embodiment are achieved.

(Third Embodiment)

15 FIG. 4 is a cross-sectional view of a semiconductor device according to a third embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made 20 of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and 25 not serving as active regions. On one of the trench portions 8

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formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Each of the dummy semiconductor portions 9 formed in the isolation region 7 is provided with a P-type impurity diffusion layer 41 and an N-type impurity diffusion layer 42, which are arranged in this order from the surface of the silicon substrate. As a result, a first PN junction 43 is formed between the P-type impurity diffusion layer 41 and the N-type impurity diffusion layer 42, while a second PN junction 44 is formed between the N-type impurity diffusion layer 42 and the P-type silicon substrate 1. The first and second PN junctions 43 and 44 are positioned at levels between the top and bottom faces of the trench portions 8.

If respective junction capacitances in the P-type and N-type impurity diffusion layers 41 and 42 are designated at C_{j1} and C_{j2} , a total wiring-to-substrate capacitance C_{jt} in the semiconductor device according to the present embodiment is represented by the following equation (7):

$$C_{jt} = \Sigma \{1/[(1/C_{a1}) + (1/C_{j1}) + (1/C_{j2})]\} + \Sigma C_{a2} \quad \dots (7),$$

which is smaller than the total capacitance C_{at} of the semiconductor device according to the first embodiment represented by the equation (1). Hence, the following equation

(8) is satisfied:

$$C_{jt} < C_{at} \quad \dots (8).$$

Since the present embodiment has provided the plurality of PN junctions 43 and 44 in the respective dummy semiconductor portions of the isolation region 7, the capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions 9 of the semiconductor device can be represented by the capacitance obtained by connecting in series the respective capacitances in the P-type and N-type impurity diffusion layers 41 and 42 to the capacitance in the interlayer insulating film. Consequently, the wiring-to-substrate capacitance of the semiconductor device can further be reduced than in the first embodiment, resulting in the semiconductor device operating at a higher speed.

Although the present embodiment has described the case where the two PN junctions 43 and 44 are formed of the two impurity diffusion layers, if three or more PN junctions are formed of three or more impurity diffusion layers, the total wiring-to-substrate capacitance can be represented in the same fashion as represented by the equation (7). For example, if m PN junctions (m is an integer equal to or more than 3) are formed in each of the dummy active regions 9 and n PN junctions (n is an integer equal to or more than 3) are formed immediately under the trench portion 8, the total wiring-to-substrate capacitance C_{jt} is represented by the following equation (9):

$$C_{jt} = \Sigma \{1/[(1/C_{a1}) + \Sigma (1/C_{jm})]\} \\ + \Sigma \{1/[(1/C_{a2}) + \Sigma (1/C_{jn})]\} \quad \dots (9),$$

which is smaller than the total capacitance C_{at} represented by the equation (1). Hence, the following inequality (10) is satisfied:

$$C_{jt} < C_{at} \quad \dots (10).$$

In the case of using the structure, the wiring-to-substrate capacitance can be reduced significantly since not only the capacitance component in the region containing the semiconductor portions of the isolation region 7 but also the capacitance component in the region containing the trench portions thereof is also reduced.

(Fourth embodiment)

FIG. 5 is a cross-sectional view of a semiconductor device according to a fourth embodiment.

As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided

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a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. In addition, a dummy gate 51 composed of a polysilicon film formed simultaneously with the gate electrode 4 extends continuously over the semiconductor portions 9 and trench portions 8. Over the dummy gate 51, the polysilicon wire 10, and a surface of the silicon substrate (except for the active region), a silicon oxide film 52 and a high resistor film 53 composed of a polysilicon film are further formed in layers. The dummy gate 51 has been formed by patterning a first-layer polysilicon film used commonly to form the gate electrode 4 and the polysilicon wire 10 so that it is at a given distance from each of the gate electrode 4 and the polysilicon wire 10. The polysilicon film composing the high resistor film 53 has a sheet resistance film higher than that of the first-layer polysilicon film composing the gate electrode 4 and the like and an impurity concentration of $1 \times 10^{20} \text{ cm}^{-3}$ or less. The sheet resistance of the dummy gate 51 can also be held high by covering the isolation region with a resist film or the like during the implantation of an impurity into the active region.

20 In the semiconductor device according to the present embodiment, it is sufficient to consider the capacitance between the wiring and high resistor film instead of the capacitance between the wiring and substrate. In this case, since the resistance of the polysilicon film composing the high resistor
25 film 53 is high, a voltage drop occurs between the top face of

the high resistor film 53 and the surface of the semiconductor substrate 1. Accordingly, the voltage applied to the top and bottom faces of the interlayer insulating film is reduced, though the capacitance of the interlayer insulating film 12 remains unchanged. Since the amount of charge accumulated in the top and bottom faces of the interlayer insulating film 12 decreases in direct proportion to the voltage applied thereto, the time required for charging or discharging between the wiring and high resistor is reduced, resulting in the semiconductor device operating at a higher speed.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 6(a) to 6(h) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 6(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 6(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity

obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 6(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 6(d), the silicon oxide film 23 is polished by a CMP process. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form a plurality of buried trench portions 8 each filled with a silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wires and the silicon substrate.

In the step shown in FIG. 6(e), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wires 10 by using a known technique. During the process, the dummy gate 51 is formed

simultaneously with the gate electrode 4 and the polysilicon wire 10 and at a given distance from each of the gate electrode 4 and the polysilicon wire 10, so that the dummy gate 51 neither cross nor contact the gate electrode 4 and the polysilicon wire 10. The gate electrode 4, the polysilicon wire 10, and the dummy gate 51 can be formed simultaneously by using a common semiconductor mask. The dummy gate 51 has a sheet resistance higher than those of the gate electrode 4 and polysilicon wire 10, which are used as interconnections, and has an impurity concentration adjusted to be 1×10^{20} atoms \cdot cm^{-3} or lower by ion implantation or the like.

In the step shown in FIG. 6(f), the silicon oxide film 52 and the high resistor film 53 made of polysilicon are formed over the isolation region 7. The high resistor film 53 has a sheet resistance higher than those of the gate electrode 4 and polysilicon wires 10 and has an impurity concentration adjusted to be 1×10^{20} atoms \cdot cm^{-3} or lower by ion implantation or the like. The silicon oxide film 52 and the high resistor film 53 are formed to provide a MIM capacitor and a resistor.

In the step shown in FIG. 6(g), a resist mask 55 covering at least the isolation region 7 is formed and arsenic ions 25 are implanted into the active region 6 to form the NMOS having the source/drain regions 5. During the process, arsenic ions are not implanted in the isolation region 7.

In the step shown in FIG. 6(h), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by

a metal wire 13 formed thereon.

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5 In the semiconductor device according to the present embodiment, it is sufficient to consider the capacitance between the wiring and high resistor film instead of the capacitance between the wiring and substrate. In this case, since the resistance of the polysilicon film composing the high resistor film 53 is high, a voltage drop occurs between the top face of the high resistor film 53 and the surface of the semiconductor substrate 1. Accordingly, the voltage applied to the top and bottom faces of the interlayer insulating film is reduced, though the capacitance of the interlayer insulating film 12 remains unchanged. Since the amount of charge accumulated in the top and bottom faces of the interlayer insulating film 12 decreases in direct proportion to the voltage applied thereto, the time required for charging or discharging between the wiring and high resistor is reduced, resulting in the semiconductor device operating at a higher speed.

20 The high-resistance film 53 according to the present embodiment can be formed easily at low cost by patterning the same film as composing, e.g., the high resistor film of the resistor element and local wiring. Instead of forming the dummy gate 51, it is possible to form films corresponding to the high resistor film 53, the silicon oxide film 52, and the dummy gate 51 from three films composing the upper-layer film, capacitor insulating film, and lower-layer film composing the MIM capacitor formed

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anywhere on the semiconductor substrate.

It is also possible to increase the operating speed of the semiconductor device by reducing the time required for charging or discharging without forming either of the dummy gate 51 and
5 the high resistor film 53 as well as the silicon oxide film 52.

Although the description has been given to the case where the high resistor film 53 composed of the polysilicon film and the silicon oxide film 52 are stacked in layers on the isolation region 7, similar effects can also be achieved in the case of using
10 an amorphous silicon film or a silicon nitride film instead of the polysilicon film. In particular, the use of an insulating film composed of a silicon oxide film allows a reduction in total capacitance and a further increase in the operating speed of the semiconductor device.

15 (Fifth Embodiment)

FIG. 7 is a cross-sectional view of a semiconductor device according to a fifth embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as
20 a MOSFET composed of: a gate oxide film 2; a gate electrode 4; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor
25 portions 9 provided between the individual trench portions 8 and

not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate electrode 4.

In the present embodiment, the gate electrode 4 consists of a lower-layer portion 4a made of a first conductor film composed of a polysilicon film or the like and an upper-layer portion 4b made of a second conductor film composed of a tungsten film or the like. In the isolation region 7, there is provided a dummy gate 51 consisting of a lower-layer portion 51a composed of the same first conductor film as composing the lower-layer portion 4a of the gate electrode 4 and an upper-layer portion 51b composed of the same second conductor film composing the upper-layer portion 4b of the gate electrode 4. The lower-layer portion 51a of the dummy gate 51 has a top surface at the same level as the top face of each of the trench portions 8, so that planarization is achieved between the lower-layer portion 51a and the trench portions 8. The polysilicon wire 10 is composed only of the second conductor film composing the upper-layer portion 4b of the gate electrode 4. The dummy gate 51 has been formed at a given distance from each of the gate electrode 4 and polysilicon wire 10 so as to improve pattern accuracy in a photolithographic process in accordance with a line-and-space relationship. There are also provided an interlayer insulating film 12 composed of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

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In accordance with a process of manufacturing the semiconductor device according to the present embodiment, the structure of the semiconductor device as shown in FIG. 7 can be implemented by the following procedure, though the drawing thereof is omitted here.

First, the gate insulating film and the first conductor film composed of a polysilicon film or the like are deposited on the semiconductor substrate, which are partially opened to form trenches. Thereafter, an insulating film is deposited on the substrate to fill in the trenches for planarization, thereby forming trench portions. Subsequently, the second conductor film of tungsten or the like is deposited on the planarized substrate and patterned to form the gate electrode 4, the dummy gate 51, and the polysilicon wires 10. After that, the interlayer insulating film 12 and the metal wire 13 can be formed by a well-known method.

In the present embodiment also, the operating speed can be increased by reducing the amount of charge accumulated in the top and bottom faces of the interlayer insulating film, similarly to the fourth embodiment. In the semiconductor device having such a structure as used in the present embodiment, the upper-layer portion 4b of the gate electrode 4 is typically composed of a low resistor film composed of silicide or the like. However, since the wiring-to-substrate voltage is also applied in series to the upper-layer and lower-layer portions 4b and 4a, the amount of

charge is effectively reduced by a voltage drop and the operating speed of the semiconductor device is increased remarkably.

Although the present embodiment has not used such a high resistor film as used in the fourth embodiment, it will be appreciated that a high resistor film may be provided over the dummy gate with an insulating film interposed therebetween.
(Sixth Embodiment)

FIG. 8 is a cross-sectional view of a semiconductor device according to a sixth embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

In the isolation region 7, inter-trench insulating films

61 each composed of a silicon oxide film and surrounded by the trench portions 8 are formed to overlies the dummy semiconductor portions 9 and underlie the interlayer insulating film 12. The top faces of the inter-trench insulating films 61 are at the same level as the top faces of the buried trench portions 8, while the bottom faces thereof are at a level between the top and bottom faces of the buried trench portions 8.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 9(a) to 9(i) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 9(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 9(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided

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to form at least one projecting portion surrounded by the trenches
14. The semiconductor portions 9 may be considered as dummy
active regions which do not function as active regions. The
trenches include one formed in a position immediately under the
5 polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 9(c), a silicon oxide film 23 is
deposited over the entire surface of the substrate to fill in the
trenches 14.

10 In the step shown in FIG. 9(d), the silicon oxide film 23
is polished by a CMP method. Subsequently, the silicon nitride
film 22 and the silicon oxide film 21 are removed selectively to
form the plurality of buried trench portions 8 each filled with
the silicon oxide film and having a planarized surface. The
buried trench portions 8 include: buried trench portions 8a
15 functioning as isolation; buried trench portions 8b forming the
dummy semiconductor portions 9; and buried trench portions 8c for
providing insulation between the polysilicon wires and the
silicon substrate.

In the step shown in FIG. 9(e), the semiconductor portions
20 of the isolation region 7 are subjected to dry etching for forming
trenches 62.

In the step shown in FIG. 9(f), a silicon oxide film is filled
in each of the trenches 62 to form the inter-trench insulating
film 61.

25 In the step shown in FIG. 9(g), there are formed the gate

oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 and the polysilicon wire 10 can be formed simultaneously by using a common semiconductor mask.

5 In the step shown in FIG. 9(h), arsenic ions 25 are implanted from above to form the NMOSFET having the source/drain regions 5 in the active region 6. Although the arsenic ions 25 are also implanted into the isolation region 25 during the process, no trouble occurs. In the case of using a resist mask covering a
10 region to be formed with a PMOSFET, however, the isolation region 7 may be covered with the resist mask.

In the step shown in FIG. 9(i), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

15 In the semiconductor device according to the present embodiment, the inter-trench insulating films 61 each composed of the silicon oxide film are formed over the dummy semiconductor portions 9 of the isolation region 7 and under the interlayer insulating film 12 to be surrounded by the buried trench portions
20 8. The top faces of the inter-trench insulating films 61 are at the same level as the top faces of the buried trench portions 8, while the bottom faces thereof are at a level between the top and bottom faces of the buried trench portions 8.

Thus, in the semiconductor device according to the present
25 embodiment, the inter-trench insulating films 61 are formed by

filling the silicon oxide films in the respective dummy semiconductor portions 9 that have been lowered in level, so that the distance between the wiring and the substrate is longer than in the conventional semiconductor device shown in FIG. 19. Since the wiring-to-substrate capacitance decreases in inverse proportion to the distance, the wiring-to-substrate capacitance is smaller in the semiconductor device according to the present embodiment than in the conventional semiconductor device, resulting in a higher operating speed.

Although the present embodiment has described the case where the silicon oxide film is buried in each of the semiconductor portions, similar effects can also be achieved if an insulating film composed of a silicon nitride film is used.

Although the semiconductor portions 9 have been lowered in level and filled with the silicon oxide films prior to the formation of the gate electrode, the method of manufacturing a semiconductor device according to the present invention is not limited to such an embodiment. The same effects as achieved in the present embodiment can also be achieved if the steps of lowering the semiconductor portions 9 in level and filling the silicon oxide films therein are performed after the formation of the gate electrode or prior to the formation of trench isolation. (Seventh Embodiment)

FIG. 10 is a cross-sectional view of a semiconductor device according to a seventh embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

In upper portions of the dummy semiconductor portions 9 of the isolation region 7, oxygen atoms have been introduced by ion implantation or the like to form high resistor portions 71 each composed of a high-resistance silicon layer. Although the bottom faces of the high resistor portions 71 are at a level between the top and bottom faces of the trench portions 8, they may be positioned at a level lower than the bottom faces of the trench portions 8.

A description will be given next to a method of manufacturing a semiconductor device according to the present

embodiment. FIGS. 11(a) to 11(h) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

5 In the step shown in FIG. 11(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

10 In the step shown in FIG. 11(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and
15 trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The
20 trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 11(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

25 In the step shown in FIG. 11(d), the silicon oxide film 23

is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming the dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

10 In the step shown in FIG. 11(e), a resist mask 73 covering the active region 6 is formed and oxygen ions 72 are implanted only into the isolation region 7 to form the high resistor portions 71 in the outermost surface of the silicon substrate, in which the oxygen ions have been introduced as an impurity in the semiconductor portions 9 of the isolation region 7.

15 In the step shown in FIG. 11(f), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 and the polysilicon wire 10 can be formed simultaneously by using a common semiconductor mask.

20 In the step shown in FIG. 11(g), arsenic ions are implanted from above the substrate to form the NMOSFET having the source/drain regions 5 in the active region 6. Although the arsenic ions 25 are also implanted into the isolation region 7 during the process, no trouble occurs. In the case of using a

resist mask covering a region to be formed with a PMOSFET, however, the isolation region 7 may be covered with the resist mask.

In the step shown in FIG. 11(h), a silicon oxide film is formed as the interlayer insulating film 12, followed by the metal wire 13 formed thereon.

The semiconductor device according to the present embodiment is characterized in that the oxygen atoms have been introduced into the upper portions of the semiconductor portions 9 of the isolation region 7 by ion implantation or the like to form the high resistor portions 71 each composed of a high-resistance silicon layer. Although the bottom faces of the high resistor portions 71 are at a level between the top and bottom faces of the buried trench portions 8, they may be positioned at a level lower than the bottom faces of the buried trench portions 8.

Since the high resistor portions 71 each composed of a high-resistance silicon layer have been formed in the dummy semiconductor portions 9 of the silicon substrate, a voltage drop occurs in the high resistor portions 71 of the silicon substrate when a voltage is placed between the wiring and the substrate. Consequently, a potential difference between the wiring and semiconductor portions 9 is reduced so that the amount of charge is reduced in direct proportion to the placed voltage, though the capacitance of the interlayer insulating film 12 between the wiring and the semiconductor portions 9 is equal to that of the

interlayer insulating film 12 in the conventional semiconductor device shown in FIG. 19. Accordingly, the time required for charging or discharging is reduced and the operating speed of the semiconductor device is increased.

5 Although the present embodiment has described the case where oxygen atoms are introduced as an impurity into the dummy semiconductor portions 9, similar effects can be achieved if nitrogen atoms are introduced.

10 Although the high resistor portions are formed prior to the formation of the gate electrode in the present embodiment, they may be formed at any stage of the process of manufacturing the semiconductor device provided that oxygen atoms can be introduced into the semiconductor portions.

(Eighth Embodiment)

15 FIG. 12 is a cross-sectional view of a semiconductor device according to an eighth embodiment.

20 As shown in the drawing, a first active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; sidewalls 3 formed on the side faces of the gate electrode 4 and composed of silicon oxide films; and source/drain regions 5. An isolation region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an
25 insulating material and with dummy semiconductor portions 9

provided between the individual trench portions 8 and not serving as active regions. On one of the trench portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal wire 13 formed on the interlayer insulating film 12.

Over the dummy semiconductor portions 9 and trench portions 8 of the isolation region 7, an underlying insulating film 81 made of a silicon oxide film has been formed simultaneously with the sidewalls on the side faces of the gate electrode 4. The underlying insulating film 81 has been formed to cover the entire polysilicon wire 10.

A description will be given next to a method of manufacturing a semiconductor device according to the present embodiment. FIGS. 13(a) to 13(i) are cross-sectional views showing the structure of the semiconductor device having an NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 13(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 13(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate

1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity
5 obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy
10 active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 13(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in
15 the trenches 14.

In the step shown in FIG. 13(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with
20 the silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon
25 substrate.

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5 In the step shown in FIG. 13(e), there are formed the gate oxide film 2, the gate electrode 4 made of polysilicon, and the polysilicon wire 10 by using a known technique. The gate electrode 4 can be formed simultaneously with the polysilicon wire 10 by using a common semiconductor mask.

In the step shown in FIG. 13(f), a silicon oxide film 82 is deposited over the entire surface of the substrate, followed by a resist mask 84 formed thereon to cover the isolation region 7.

10 In the step shown in FIG. 13(g), a silicon oxide film 82 is removed selectively by anisotropic dry etching using the resist mask 84 to form an underlying insulating film 81 over the isolation region 7, while the sidewalls are formed on the side faces of the gate electrode 4. The polysilicon wire 10 is completely covered
15 with the underlying insulating film 81.

In the step shown in FIG. 13(h), arsenic ions 25 are implanted from above to form the NMOSFET having the source/drain regions 5 in the active region 6. Although the arsenic ions are also implanted into the isolation region 7 during the process,
20 no trouble occurs. However, in the case of using a resist mask covering a region to be formed with a PMOSFET, the isolation region 7 may be covered with the resist mask.

In the step shown in FIG. 13(i), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by
25 a metal wire 13 formed thereon.

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The semiconductor device according to the present embodiment is characterized in that the underlying insulating film 81 composed of the silicon oxide film is formed simultaneously with the sidewalls on the side faces of the gate electrode 4 to extend over the dummy semiconductor portions 9 and buried trench portions 8 of the isolation region 7. The resulting underlying insulating film 81 covers the entire polysilicon wire 10.

Thus, in the semiconductor device according to the present embodiment, the underlying insulating film 81 composed of the silicon oxide film is present over the isolation region 7, so that the distance between the wiring and the substrate is longer than in the conventional semiconductor device shown in FIG. 19. Since the wiring-to-substrate capacitance decreases in inverse proportion to the distance, the wiring-to-substrate capacitance is reduced in the semiconductor device according to the present embodiment, resulting in a higher operating speed.

Although the present embodiment has described the case where the underlying insulating film 81 is composed of the silicon oxide film, similar effects can also be achieved if an insulating film composed of a silicon nitride film is used.

Although the present embodiment has described the case where the underlying insulating film is composed of a single-layer film, the underlying insulating film may be composed of a multi-layer film. For example, in the case where the sidewalls

consist of L-shaped portions extending over the side faces of the gate electrode and the substrate and of upper wedge-shaped portions or, alternatively, the sidewalls are provided along with an on-gate protective film, the underlying insulating film should
5 be composed of a multi-layer film. It will be appreciated that, in that case also, the same effects as achieved in the present embodiment are achieved.

(Ninth Embodiment)

FIG. 14(a) is a cross-sectional view of a semiconductor
10 device according to a ninth embodiment.

As shown in the drawing, an active region 6 of a P-type silicon substrate 1 is provided with an element functioning as a MOSFET composed of: a gate oxide film 2; a gate electrode 4 made of a polysilicon film; and source/drain regions 5. An isolation
15 region 7 for electrically isolating the individual elements is formed with a plurality of trench portions 8 each filled with a silicon oxide film as an insulating material and with dummy semiconductor portions 9 provided between the individual trench portions 8 and not serving as active regions. On one of the trench
20 portions 8 formed in the isolation region 7, there is provided a polysilicon wire 10 formed simultaneously with the gate insulating film 2 and the gate electrode 4. There are further provided an interlayer insulating film 12 made of a silicon oxide film deposited over the entire surface of the substrate and a metal
25 wire 13 formed on the interlayer insulating film 12.

Under the dummy semiconductor portions 9 and the trench portions 8, a buried insulating film 91 composed of a silicon oxide film is formed in contact with the bottom faces of the trench portions 8. As a result, the side faces of the semiconductor portions 9 are in contact with the trench portions 8, while the bottom faces thereof are in contact with the buried insulating film 91.

FIG. 14(b) is a cross-sectional view for illustrating the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment. In the semiconductor device according to the present embodiment, since the buried insulating film 91 composed of the silicon oxide film is formed in the silicon substrate, the capacitance C_{ij} becomes a half of the capacitance C_{j1} shown in FIG. 1(b) or less (T. Nishimura and Y. Inoue: Proceedings of VLSI TECHNOLOGY WORKSHOP ON "WHAT IS THE FUTURE OF SOI?" (1995) p.123).

Therefore, the total wiring-to-substrate capacitance C_{ijt} of the semiconductor device is represented by the following equation (11):

$$C_{ijt} = \{(C_{a1} \times C_{ij}) / (C_{a1} + C_{ij})\} + \sum C_{a2} \quad \dots (11),$$

which is smaller than the total capacitance C_{jt} represented by the equation (3). Accordingly, the following inequality (12) is satisfied:

$$C_{ijt} < C_{jt} \quad \dots (12).$$

Hence,

$$C_{ijt} < C_{at}$$

is derived from the relationship represented by the equation (4), so that the wiring-to-substrate capacitance of the semiconductor device according to the present embodiment is reduced, resulting in the semiconductor device operating at a higher speed.

FIGS. 15(a) to 15(h) are cross-sectional views of the structure of the semiconductor device having the NMOSFET according to the present embodiment in the manufacturing process therefor.

In the step shown in FIG. 15(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the P-type silicon substrate 1.

In the step shown in FIG. 15(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, the semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the

polysilicon wire 10, which is to be formed in the subsequent step.

In the step shown in FIG. 15(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

5 In the step shown in FIG. 15(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form the plurality of buried trench portions 8 each filled with the silicon oxide film and having a planarized surface. The
10 buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

15 In the step shown in FIG. 15(e), a resist mask 92 covering the active region 6 is formed and oxygen ions 93 are implanted only into the isolation region 7 so that the buried insulating film 91 into which the oxygen atoms have been introduced as an impurity is formed. The buried insulating film 91 provides
20 insulation between the silicon substrate 1 and the semiconductor portions 9 in the isolation region 7. In this case, the buried insulating film 91 is connected to the respective side faces of each of the individual trench portions 8a to 8c and energy for implanting the oxygen ions is set such that the semiconductor
25 portions 9 are in the floating state.

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In the step shown in FIG. 15(f), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 may be formed simultaneously with
5 the polysilicon wire 10 by using a common semiconductor mask.

In the step shown in FIG. 15(g), a resist mask 95 is formed to cover the isolation region 7 and arsenic ions 25 are implanted into the active region 6 to form the NMOSFET having the source/drain regions 5. In this case, no implantation is
10 performed with respect to the isolation region 7.

In the step shown in FIG. 15(h), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

In the semiconductor device formed by the manufacturing
15 method according to the present embodiment, the buried insulating film 91 composed of the silicon oxide film is formed under the dummy semiconductor portions 9 and the buried trench portions 8 to be in contact with the bottom faces of the buried trench portions 8. As a result, the side faces of the semiconductor portions 9
20 are in contact with the buried trench portions 8, while the bottom faces thereof are in contact with the insulating film 91. Although the present embodiment has formed the buried insulating film by implanting oxygen ions prior to the formation of the gate electrode, the buried insulating film may be formed at any stage
25 of the method of manufacturing the semiconductor device provided

that oxygen atoms can be introduced into the semiconductor portions.

(Tenth Embodiment)

The present embodiment will basically describe another example of the manufacturing process shown in FIG. 14(b), which is for achieving the effect of capacitance reduction.

FIGS. 16(a) to 16(i) are cross-sectional views of the structure of a semiconductor device having an NMOSFET according to a tenth embodiment in the manufacturing process therefor.

10 In the step shown in FIG. 16(a), a thin silicon oxide film 21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on a P-type silicon substrate 1.

In the step shown in FIG. 16(b), a plurality of trenches 14 each having a given width are formed in the silicon substrate 1. The trenches 14 include: trenches 14a formed to surround an active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region 6 by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step. In the step shown in FIG. 15(c), a silicon oxide film 23

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is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 16(c), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 16(d), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively except for the portions overlying the active region 6 to form a plurality of buried trench portions 8 each filled with a silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 16(e), the semiconductor portions 9 of the isolation region 7 are subjected to dry etching for forming trenches 96.

In the step shown in FIG. 16(f), a silicon oxide film is deposited in each of the trenches 96 to form a buried insulating film 91, followed by a silicon film deposited thereon to form semiconductor portions 97 serving as dummy active regions. The buried insulating films 91 are in contact with the buried trench portions 8a to 8c.

In the step shown in FIG. 16(g), there are formed the gate

oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 may be formed simultaneously with the polysilicon wire 10 by using a common semiconductor mask.

5 In the step shown in FIG. 16(h), a resist mask 98 is formed to cover the isolation region 7 and arsenic ions 25 are implanted into the active region 6 to form the NMOSFET having source/drain regions 5. In this case, implantation may be performed with respect to the isolation region 7, though it is not performed
10 in the example.

In the step shown in FIG. 16(i), a silicon oxide film is deposited to form the interlayer insulating film 12, followed by a metal wire 13 formed thereon.

The manufacturing method according to the present
15 embodiment also enables the formation of a semiconductor device having the same structure as the semiconductor device according to the ninth embodiment, resulting in smaller wiring-to-substrate capacitance and a higher operating speed.

Although the present embodiment has grown the silicon oxide
20 films and the silicon films in the trenches 96 prior to forming the gate electrode, the silicon oxide films and the silicon films may be grown at any stage of the process of manufacturing the semiconductor device provided that they can be grown and buried in the trenches 96.

25 (Eleventh Embodiment)

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The present embodiment will also basically describe still another example of the manufacturing process shown in FIG. 14(b), which is for achieving the effect of capacitance reduction.

FIGS. 17(a) to 17(f) and FIGS. 18(a) to 18(d) are
5 cross-sectional views showing the structure of a semiconductor device having an NMOSFET according to an eleventh embodiment in the manufacturing process therefor.

10 In the step shown in FIG. 17(a), a trench 102 is formed in a region of a P-type silicon substrate 1 in which an isolation region is to be formed.

In the step shown in FIG. 17(b), a silicon oxide film is filled in the trench 102 to form an insulating film 101 so that the entire surface of the substrate is planarized.

15 In the step shown in FIG. 17(c), a silicon film 103 is epitaxially grown over the entire surface of the substrate. During the step, since single-crystal silicon is grown on single-crystal silicon in an active region 6, a semiconductor region having an excellent crystallographic property is formed therein, while a silicon film having an inferior crystallographic
20 property is formed on the silicon oxide film in the isolation region 7. However, since the silicon film in the isolation region 7 does not function as an active region, the inferior crystallographic property thereof will not adversely affect the properties of the semiconductor device.

25 In the step shown in FIG. 17(d), a thin silicon oxide film

21 having a thickness of 10 nm and a silicon nitride film 22 are formed sequentially on the silicon film 103.

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In the step shown in FIG. 17(e), a plurality of trenches 14 each having a given width are formed in the substrate. The trenches 14 include: trenches 14a formed to surround the active region 6 to be formed with the element; trenches 14b formed in the isolation region 7 separated from the active region by the trenches 14a to eliminate pattern dependence from planarity obtained at the completion of the manufacturing process; and trenches 14c for forming the polysilicon wires. In the isolation region 7 also, semiconductor portions 9 have been provided to form at least one projecting portion surrounded by the trenches 14. The semiconductor portions 9 may be considered as dummy active regions which do not function as active regions. The trenches include one formed in a position immediately under the polysilicon wire 10, which is to be formed in the subsequent step. In forming the trenches 14, etching is performed till the surface of the buried insulating film 101 is exposed in the trenches 14.

In the step shown in FIG. 17(f), a silicon oxide film 23 is deposited over the entire surface of the substrate to fill in the trenches 14.

In the step shown in FIG. 18(a), the silicon oxide film 23 is polished by a CMP method. Subsequently, the silicon nitride film 22 and the silicon oxide film 21 are removed selectively to form a plurality of buried trench portions 8 each filled with a

silicon oxide film and having a planarized surface. The buried trench portions 8 include: buried trench portions 8a functioning as isolation; buried trench portions 8b forming dummy semiconductor portions 9; and buried trench portions 8c for providing insulation between the polysilicon wire and the silicon substrate.

In the step shown in FIG. 18(b), there are formed the gate oxide film 2, the gate electrode 4 having sidewalls 24 on the side faces thereof, and the polysilicon wire 10 by using a known technique. The gate electrode 4 is formed simultaneously with the polysilicon wire 10.

In the step shown in FIG. 18(c), arsenic ions 25 are implanted into the active region 6 to form source/drain regions 5 by using a resist mask 95 formed to cover the isolation region 7. The NMOSFET is formed by the foregoing process. Although arsenic ions 25 are not implanted in the isolation region 7 in the example, they may be implanted alternatively.

In the step shown in FIG. 18(d), a silicon oxide film is deposited to form an interlayer insulating film 12, followed by a metal wire 13 formed thereon.

The manufacturing method according to the present embodiment also enables the formation of a semiconductor device having the same structure as the semiconductor device according to the ninth embodiment, resulting in smaller wiring-to-substrate capacitance and a higher operating speed.

Although the present embodiment has formed the trench 102 in the silicon substrate 1 and buried the silicon oxide film therein to form a miniaturized gate electrode 4, the silicon oxide film may be formed directly on the isolation region without forming the trench if the semiconductor substrate inferior in planarity does not adversely affect the patterning of the gate during the formation of the gate electrode.

(Variations of Individual Embodiments)

Although the eighth embodiments of the present invention have been described, there are variations obtained by combining the individual embodiments with each other.

By way of example, the first embodiment used in combination with the second to eighth embodiments achieves a further reduction in wiring-to-substrate capacitance and a reduction in time required for charging or discharging, so that the resulting semiconductor device operates at a higher speed than in the case where each of the embodiments is used singly.

Thus, according to the present invention, the individual embodiments used in combination can achieve more remarkable effects than in the case where each of the embodiments is used singly.

Although each of the embodiments has used the NMOSFET as the element to be disposed in the active region 6, the present invention is not limited to such embodiments. The element includes an active element other than the MOSFET such as a bipolar

transistor or diode or a passive element such as a capacitor.

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We claim:

1. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

5 a plurality of trench portions each formed in said isolation region and filled with an insulating material;

semiconductor portions interposed between said individual trench portions in said isolation region;

10 an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film; and

at least one PN junction formed in said semiconductor portions underlying said wire.

2. A semiconductor device according to claim 1, wherein said
15 PN junction includes a plurality of PN junctions formed in said semiconductor portions.

3. A semiconductor device according to claim 1, wherein said active region is formed with an impurity diffusion region and a PN junction is formed at a bottom face of said impurity diffusion
20 region, the PN junction of said isolation region being positioned at a level lower than the PN junction of said active region.

4. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

25 a plurality of trench portions each formed in said isolation

region and filled with an insulating material;

semiconductor portions interposed between said individual trench portions in said isolation region;

an interlayer insulating film formed to extend continuously
5 over said active region and said isolation region;

a wire formed on said interlayer insulating film; and

a dielectric film interposed between at least said semiconductor portions of said isolation region and said interlayer insulating film.

10 5. A semiconductor device according to claim 4, wherein said dielectric film is an underlying insulating film interposed between said interlayer insulating film and said semiconductor portions and trench portions.

15 6. A semiconductor device according to claim 5, further comprising a gate electrode formed on the semiconductor substrate within said active region and sidewalls made of an insulating material and formed on both side faces of said gate electrode, wherein said underlying insulating film is formed of the same film as forming said sidewalls.

20 7. A semiconductor device according to claim 6, wherein said underlying insulating film is composed of a multilayer film.

8. A semiconductor device according to claim 4, wherein said dielectric film is formed in an upper portion of each of said semiconductor portions of the semiconductor substrate to have a
25 top face at approximately the same level as a top face of each

of said trench portions.

9. A semiconductor device according to claim 4, wherein said dielectric film is composed of at least one of a silicon oxide film and a silicon nitride film.

5 10. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

a plurality of trench portions each formed in said isolation region and filled with an insulating material;

10 semiconductor portions interposed between said individual trench portions in said isolation region;

an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film; and

15 a buried insulating film formed in an inner portion of each of said semiconductor portions in said isolation region.

11. A semiconductor device comprising:

a semiconductor substrate having an active region and an isolation region surrounding said active region;

20 a plurality of trench portions each formed in said isolation region and filled with an insulating material;

semiconductor portions interposed between said individual trench portions in said isolation region;

25 an interlayer insulating film formed to extend continuously over said active region and said isolation region;

a wire formed on said interlayer insulating film; an
a resistor film formed between said interlayer insulating
film and at least said semiconductor portions of said isolation
region.

5 12. A semiconductor device according to claim 11, wherein
said resistor film is an underlying resistor film formed to extend
continuously over said semiconductor portions and trench
portions.

10 13. A semiconductor device according to claim 12, further
comprising a resistor element formed on said semiconductor
substrate and having a high resistor film, wherein said underlying
resistor film is formed of the same film as composing the high
resistor film of said resistor element.

15 14. A semiconductor device according to claim 12, further
comprising an element having an electrode member composed of a
conductor film formed on the semiconductor substrate within said
active region, wherein said resistor film is composed of the same
material as composing said electrode member.

20 15. A semiconductor device according to claim 12, further
comprising a FET having a gate electrode composed of a first
conductor film formed on the semiconductor portion within said
active region and a second conductor film deposited on said first
conductor film, wherein

25 a top surface of the first conductor film of said gate
electrode is at approximately the same level as a top surface of

each of said trench portions,

a region of said resistor film overlying each of said semiconductor portions is formed of the same two films as composing said first and second conductor films of said gate electrode, and

a region of said resistor film overlying each of said trench portions is composed of the same material as composing said first conductor film of said gate electrode.

16. A semiconductor device according to claim 11, wherein said resistor film is formed in an upper portion of each of said semiconductor portions of the semiconductor substrate to have a top face at approximately the same level as a top surface of each of said trench portions.

17. A semiconductor device according to claim 16, wherein said resistor film is composed of a silicon film containing at least one of an oxygen atom and a nitrogen atom.

18. A semiconductor device according to claim 11, wherein said resistor film is composed of at least one of a polysilicon film and an amorphous silicon film.

19. A method of manufacturing a semiconductor device, comprising:

a first step of forming, in a semiconductor substrate having a substrate region of a first conductivity type, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said

isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

a third step of forming an element on said active region;

a fourth step of introducing an impurity containing at least an impurity of a second conductivity type into said dummy semiconductor portions of said isolation region to form at least one PN junction in said dummy semiconductor portions;

a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating film.

20. A method of manufacturing a semiconductor device according to claim 19, wherein said third and fourth steps include forming a gate electrode of a FET as said element on said active region, introducing the impurity of the second conductivity type into said active region and said dummy semiconductor portions, and thereby forming source/drain regions of said FET, while forming said at least one PN junction in said dummy semiconductor portions.

3 31. A method of manufacturing a semiconductor device according to claim 19, wherein

said third step includes forming a gate electrode of a FET

as said element on said active region by using a first mask covering said isolation region and introducing the impurity of the second conductivity type into said active region to form source/drain regions of said FET and

5 said fourth step includes introducing the impurity containing at least the impurity of the second conductivity type into said dummy semiconductor portions by using a second mask covering said active region to form said at least one PN junction in said dummy semiconductor portions.

10 42p. A method of manufacturing a semiconductor device, comprising:

 a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and second
15 trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

 a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

20 a third step of forming an element on said active region;
 a fourth step of forming a resistor film on each of said dummy semiconductor portions of said isolation region;
 a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

25 a sixth step of forming a wire on said interlayer insulating

film.

5 5 23. A method of manufacturing a semiconductor device according to claim 22, wherein said fourth step includes composing said resistor film of a film containing at least one of polysilicon and amorphous silicon.

6 24. A method of manufacturing a semiconductor device according to claim 22, wherein said fourth step includes composing said resistor film of a multilayer film constituted by two or more conductor films with at least an insulating film interposed therebetween.

7 25. A method of manufacturing a semiconductor device according to claim 24, wherein said fourth step includes introducing an impurity at a concentration of 1×10^{20} atoms \cdot cm^{-3} or lower into said resistor film.

8 26. A method of manufacturing a semiconductor device, comprising:

a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

25 a third step of forming an element on said active region;

a fourth step of implanting ions into an upper portion of each of said dummy semiconductor portions to form a high resistor portion therein;

a fifth step of forming an interlayer insulating film over
5 an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating film.

9
27. A method of manufacturing a semiconductor device according to claim 26, wherein said fourth step includes
10 implanting ions containing at least an atom having an oxidizing function to form said high resistor portion.

10
28. A method of manufacturing a semiconductor device according to claim 26, wherein said fourth step includes
15 implanting ions containing at least an atom having a nitriding function to form said high resistor portion.

11
29. A method of manufacturing a semiconductor device, comprising:

a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate
20 region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench
25 portion and a second buried trench portion;

a third step of forming an element on said active region;
a fourth step of forming an underlying insulating film over
said dummy semiconductor portions of said isolation region;

a fifth step of forming an interlayer insulating film over
5 an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating
film.

12
30. A method of manufacturing a semiconductor device
according to claim 29¹¹, wherein said third step and said fourth
10 step include forming a gate electrode of a FET forming said element
on said active region, depositing a dielectric film on the
substrate, performing anisotropic etching with respect to the
dielectric film by using a mask covering said isolation region,
and thereby leaving sidewalls on both side faces of said gate
15 electrode, while leaving said underlying insulating film over
said dummy semiconductor portions.

13
31. A method of manufacturing a semiconductor device
according to claim 29¹¹, wherein said fourth step includes forming
said underlying insulating film of a dielectric film containing
20 at least silicon oxide.

14
32. A method of manufacturing a semiconductor device
according to claim 29¹¹, wherein said fourth step includes forming
said underlying insulating film of a dielectric film containing
at least silicon nitride.

25 33. A method of manufacturing a semiconductor device.

comprising:

5 a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

10 a third step of forming an element on said active region;

15 a fourth step of forming depressed portions by etching said dummy semiconductor portions and filling an insulating material in said depressed portions to form inter-trench insulating films each having a top face at the same level as respective top faces of said first and second buried trench portions;

a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating film.

20 34. A method of manufacturing a semiconductor device according to claim 15, wherein said fourth step includes forming each of said inter-trench insulating films of a dielectric film containing at least silicon oxide.

25 35. A method of manufacturing a semiconductor device according to claim 15, wherein said fourth step includes forming

each of said inter-trench insulating films of a dielectric film containing at least silicon nitride.

36. A method of manufacturing a semiconductor device, comprising:

5 a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

10 a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

a third step of forming an element on said active region;

15 a fourth step of implanting oxygen ions into each of said dummy semiconductor portions to form a buried insulating film in an inner portion thereof;

a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

20 a sixth step of forming a wire on said interlayer insulating film.

37. A method of manufacturing a semiconductor device, comprising:

25 a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region

and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench
5 portion and a second buried trench portion;

a third step of forming third trenches by etching said semiconductor portions and filling an insulating material in said third trenches to form buried insulating films each having a top
10 face at a level lower than respective top faces of said first and second buried trench portions;

a fourth step of growing semiconductor films on said buried insulating films, with said active region covered with a mask member, to form dummy semiconductor portions;

a fifth step of forming an element on said active region;
15 a sixth step of forming an interlayer insulating film over an entire surface of the substrate; and

a seventh step of forming a wire on said interlayer insulating film.

38. A method of manufacturing a semiconductor device,
20 comprising:

a first step of forming, in a semiconductor substrate having a substrate region, a first trench extending over an entire isolation region of said substrate region, while leaving an active region of said substrate region;

25 a second step of filling an insulating material in said

first trench to form a buried insulating film having a top face at the same level as a top face of said isolation region;

a third step of growing a semiconductor film over said active region and said buried insulating film;

5 a fourth step of forming, in the semiconductor substrate, a second trench for partitioning said semiconductor film and said substrate region into the active region and the isolation region and a third trench for partitioning the portion of the semiconductor film overlying said isolation region into a
10 plurality of dummy semiconductor portions;

a fifth step of filling an insulating material in each of said second and third trenches to form a first buried trench portion and a second buried trench portion;

a sixth step of forming an element on the portion of said
15 semiconductor film overlying said active region;

a seventh step of forming an interlayer insulating film over an entire surface of the substrate; and

an eighth step of forming a wire on said interlayer insulating film.

ABSTRACT OF THE DISCLOSURE

5 The top surface of a P-type semiconductor substrate is partitioned into an active region to be formed with an element and an isolation region surrounding the active region. The isolation region is composed of trench portions and dummy semiconductor portions. An interlayer insulating film is deposited on the substrate, followed by a wire formed thereon. In each of the semiconductor portions, an impurity diffusion layer is formed simultaneously with the implantation of ions into the element so that a PN junction is formed between the impurity diffusion layer and the silicon substrate. A capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions is obtained by adding in series the capacitance in the impurity diffusion layer to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. What results is a semiconductor device having lower total wiring-to-substrate capacitance and a higher operating speed.

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Fig. 1(a)

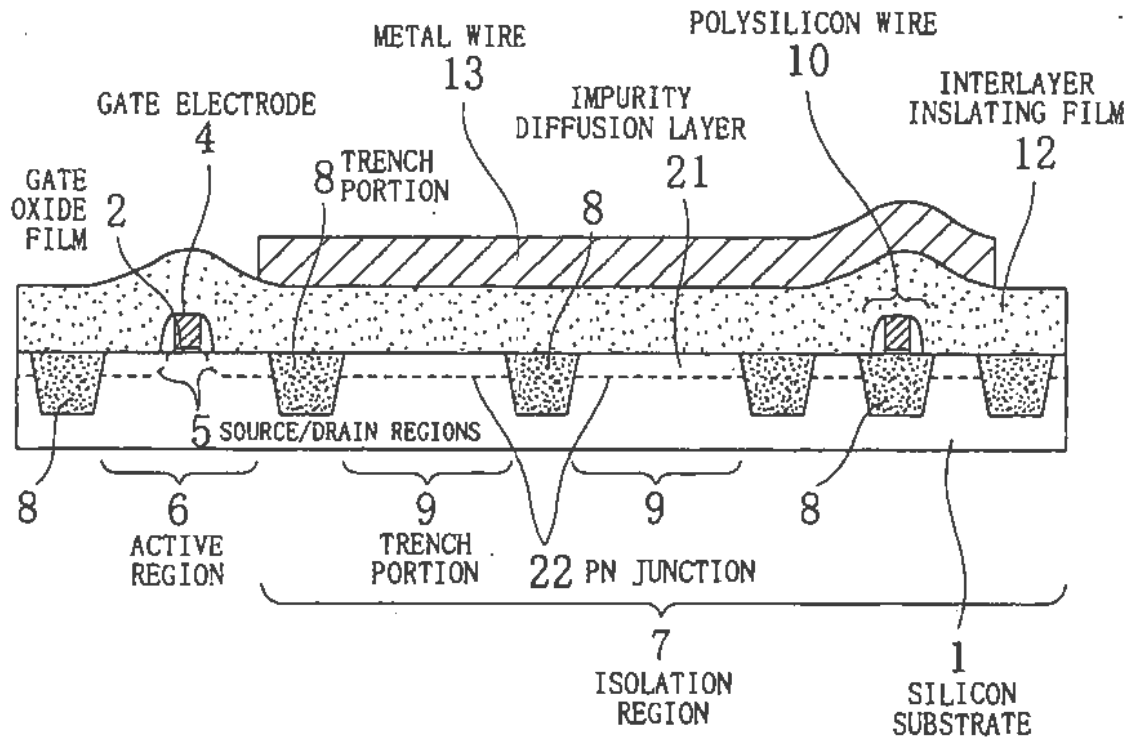
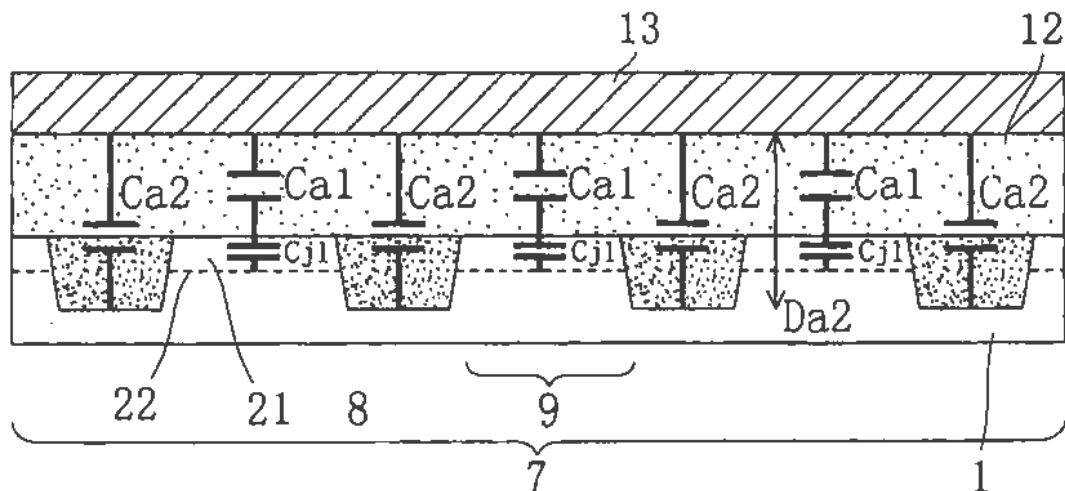


Fig. 1(b)



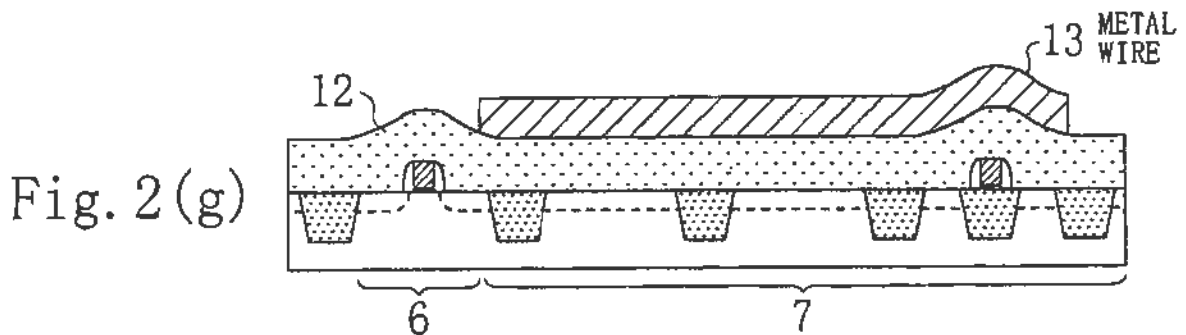
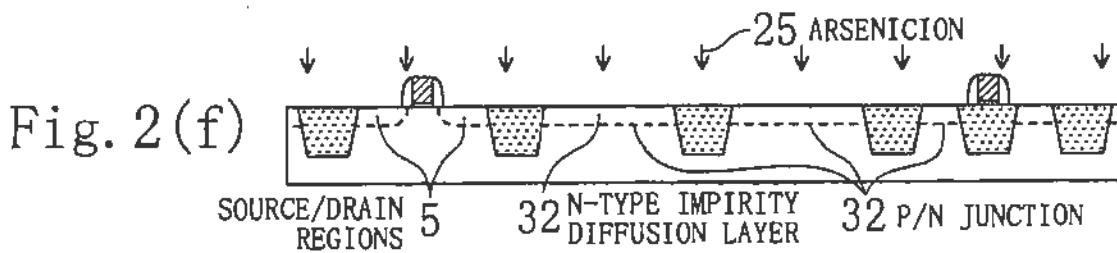
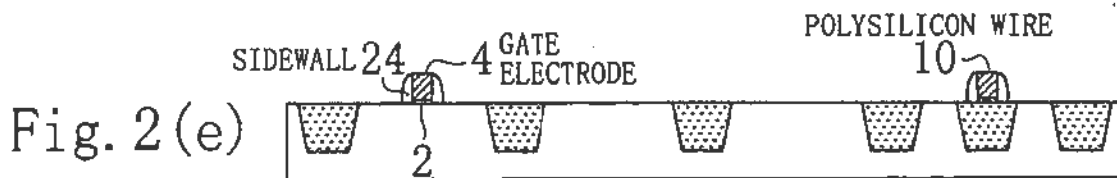
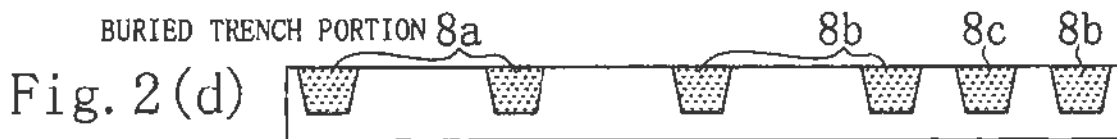
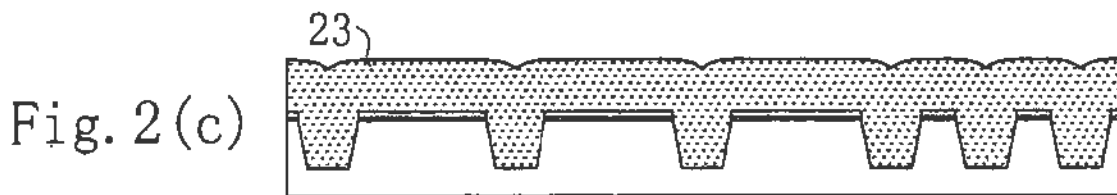
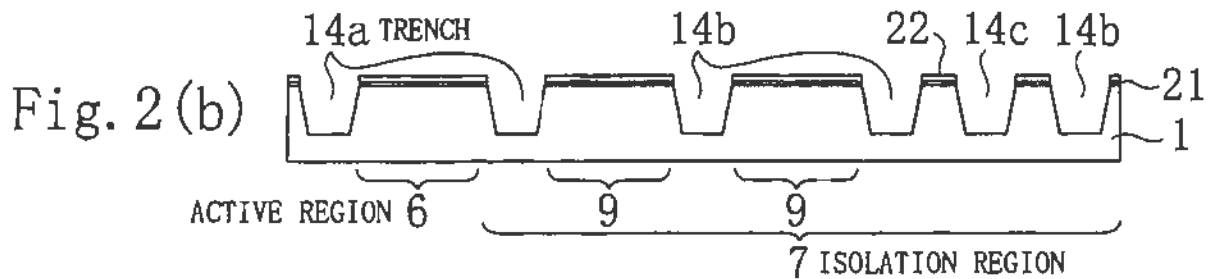


Fig. 3

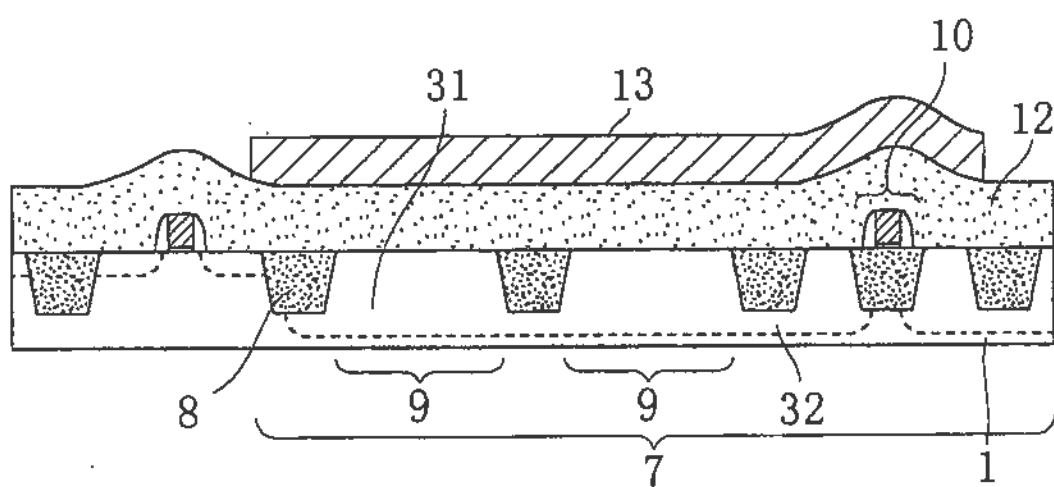
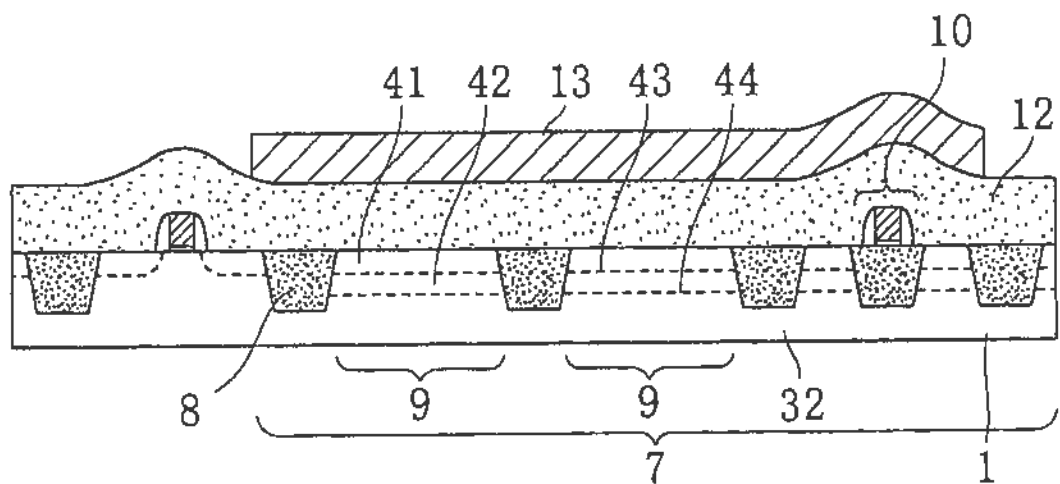
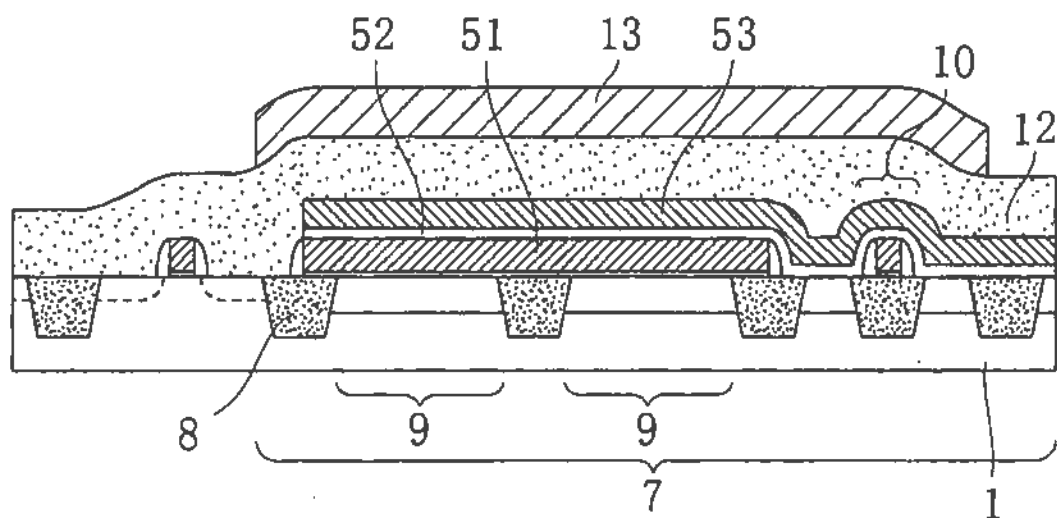


Fig. 4



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Fig. 5



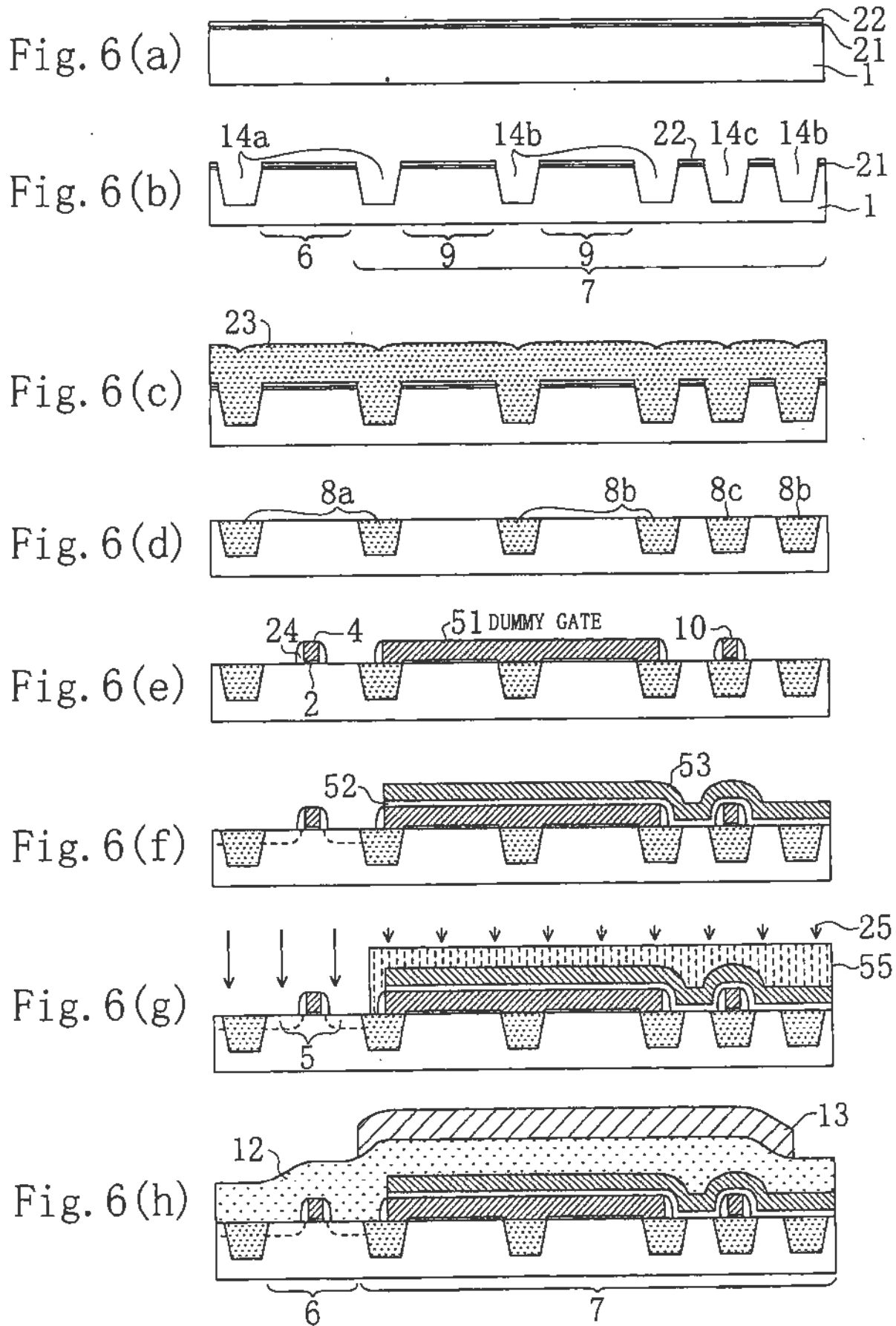


Fig. 7

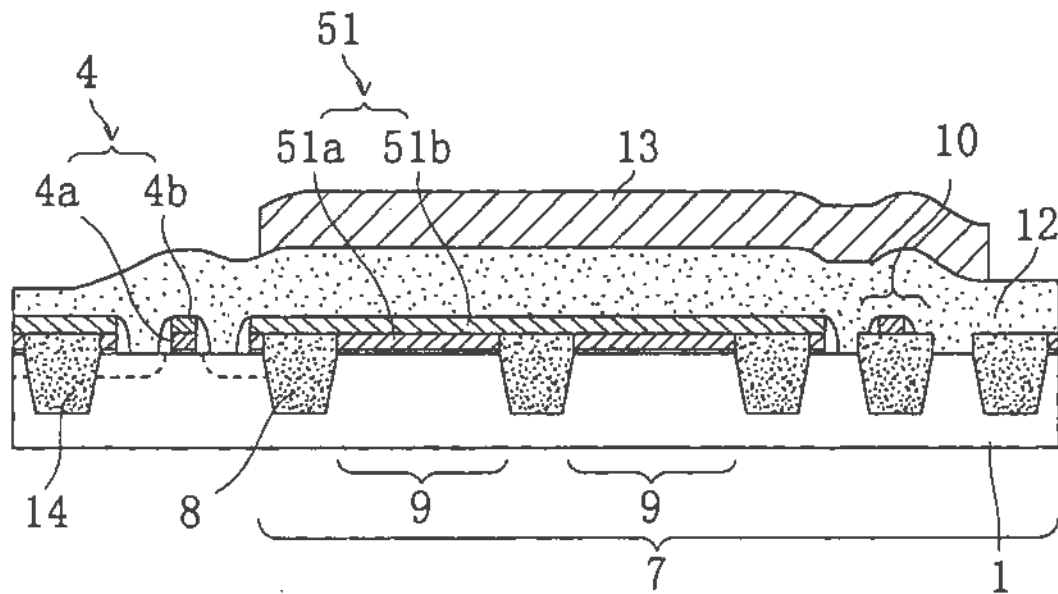
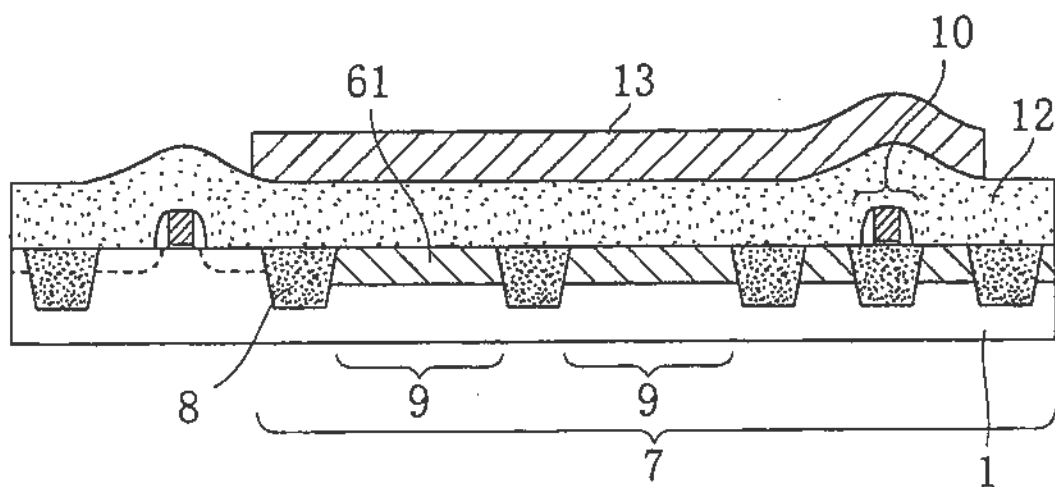
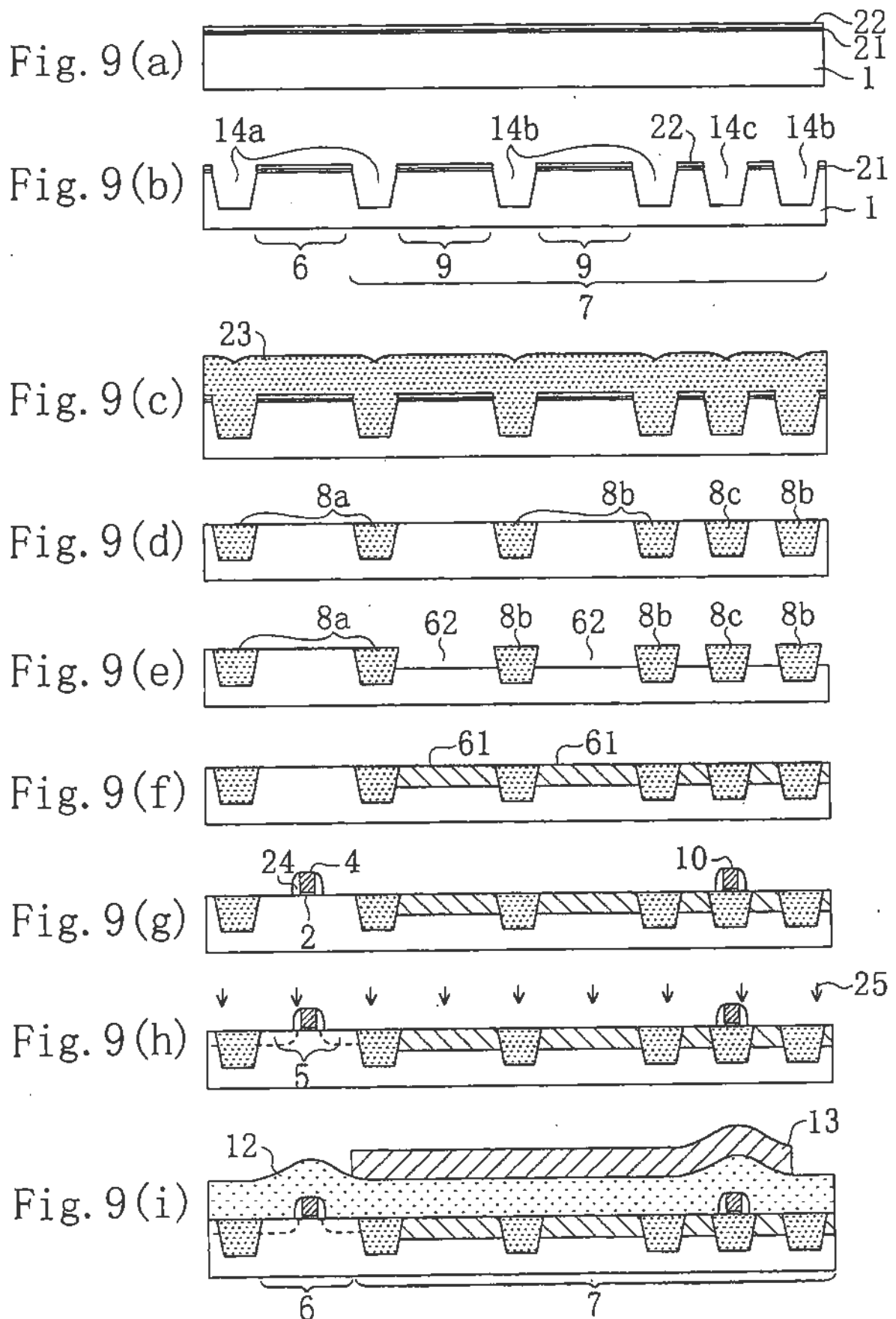


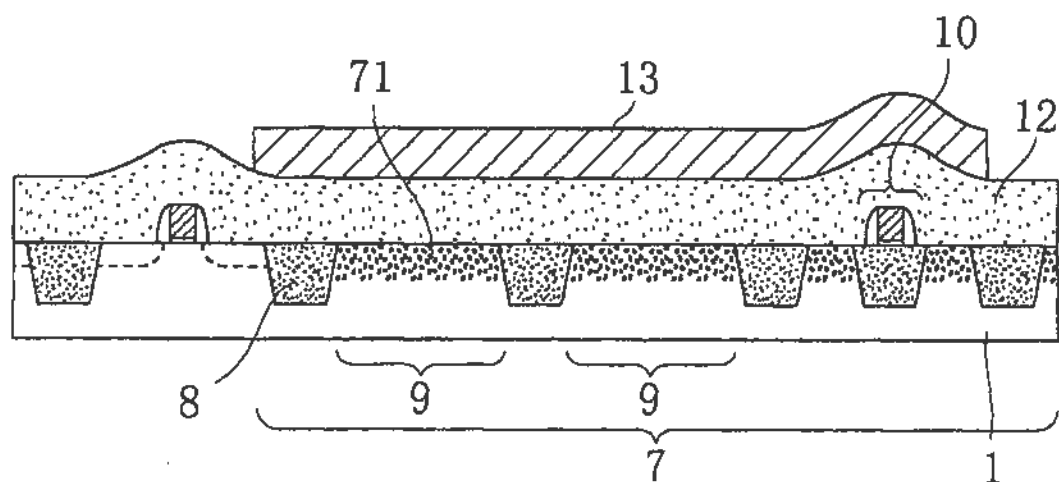
Fig. 8

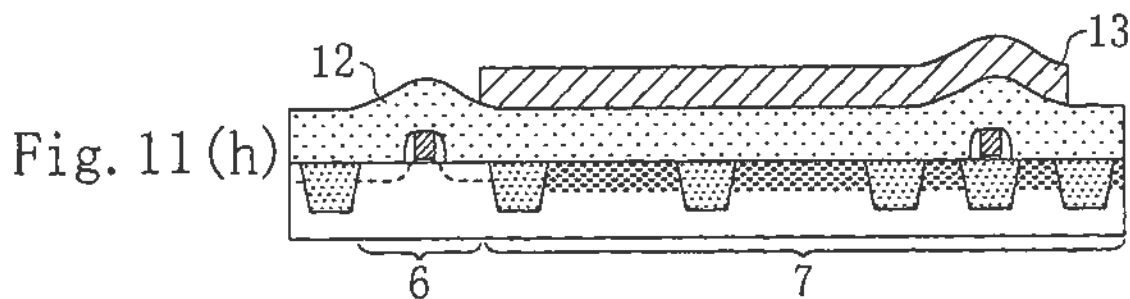
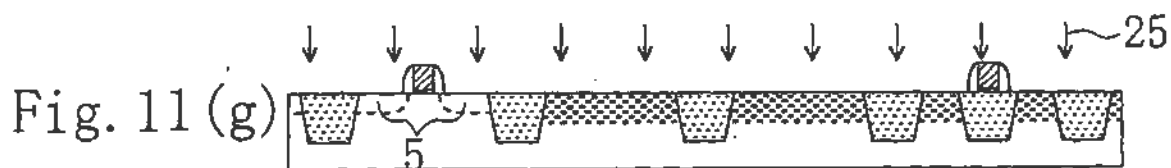
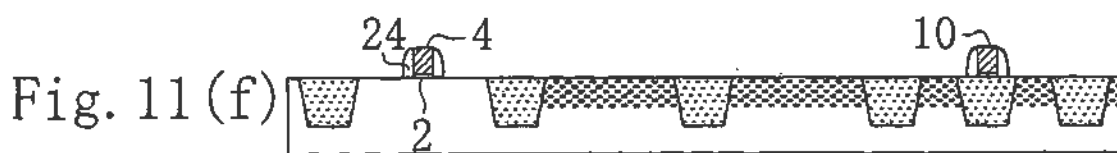
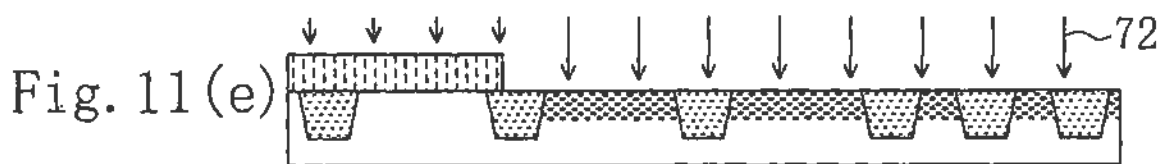
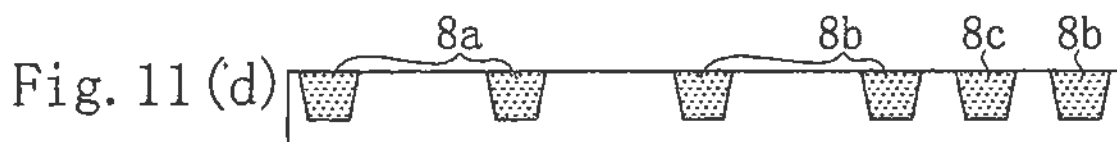
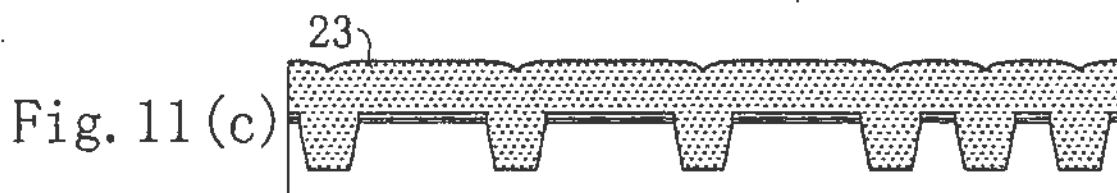
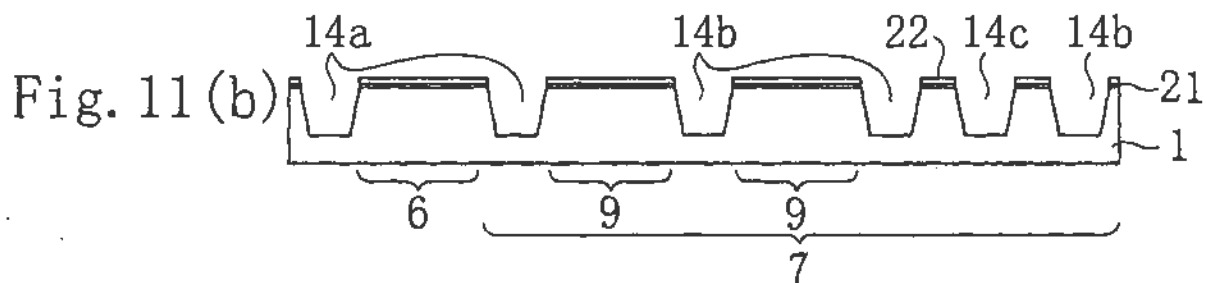




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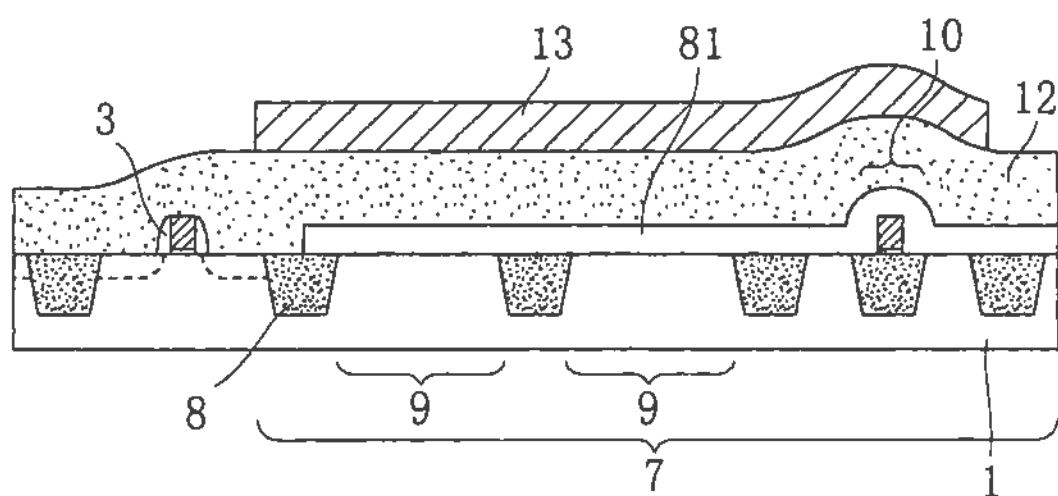
Fig. 10

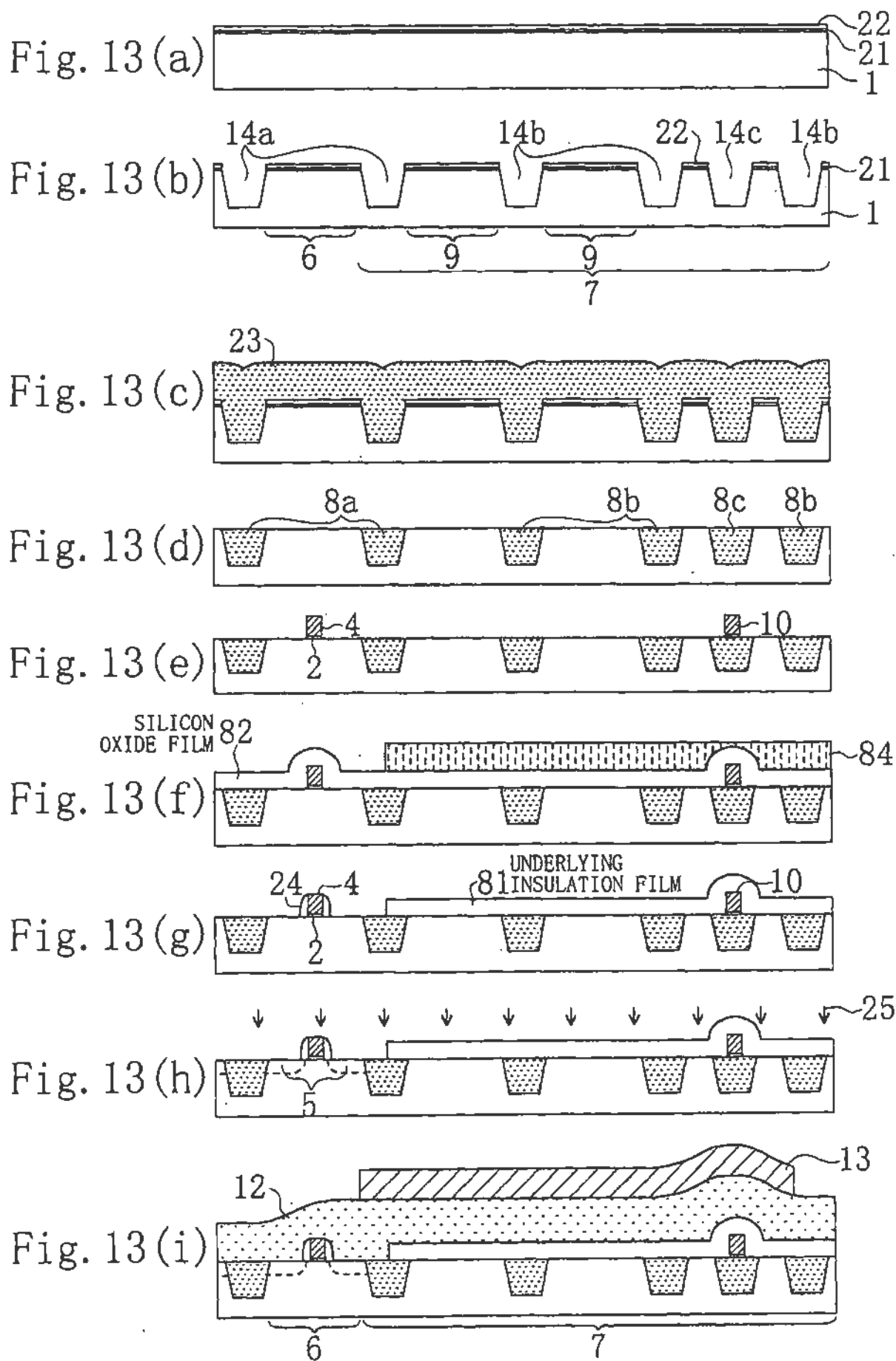




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Fig. 12





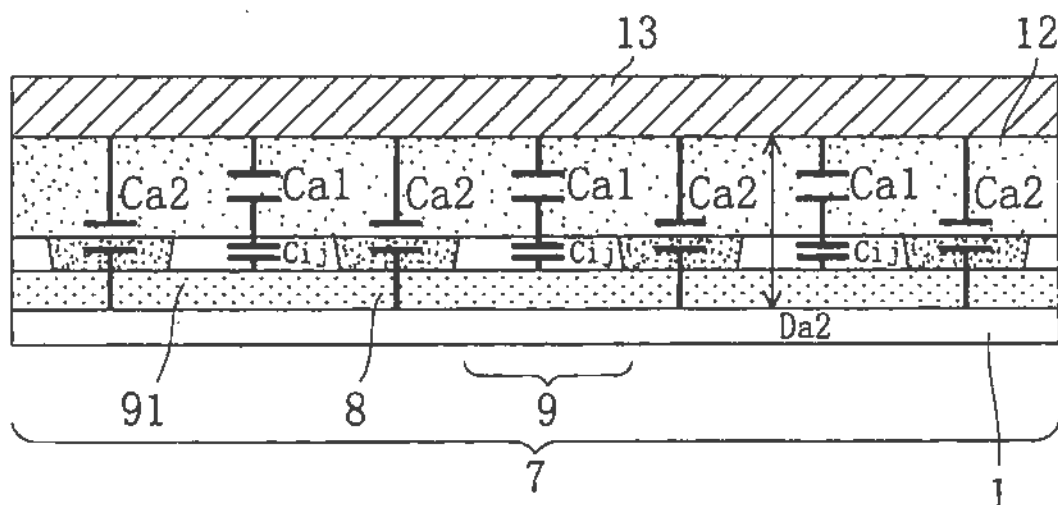
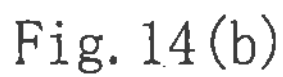


Fig. 15(a)



Fig. 15(b)

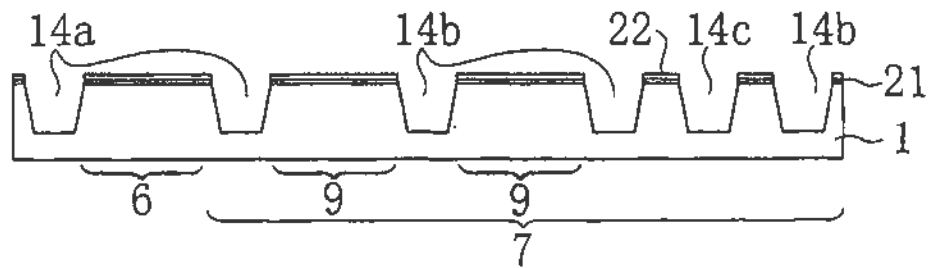


Fig. 15(c)

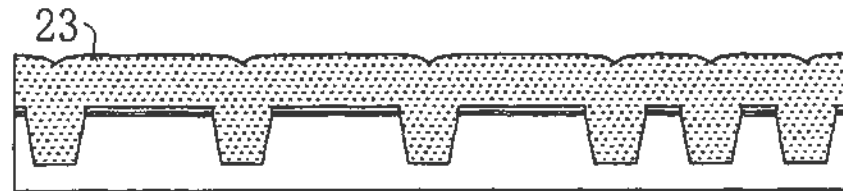


Fig. 15 (d)

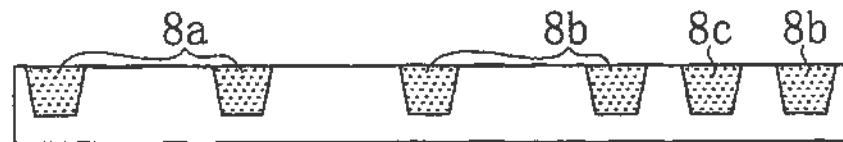


Fig. 15(e)

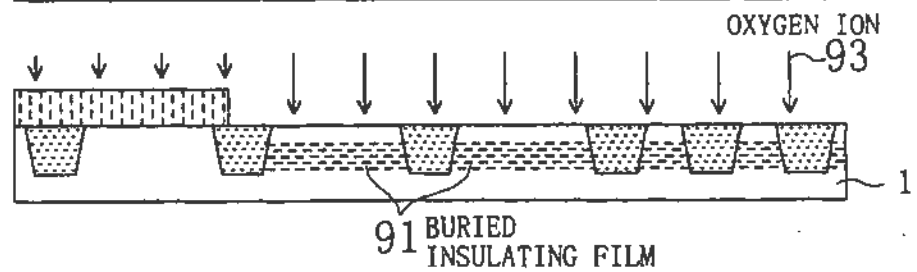


Fig. 15 (f)

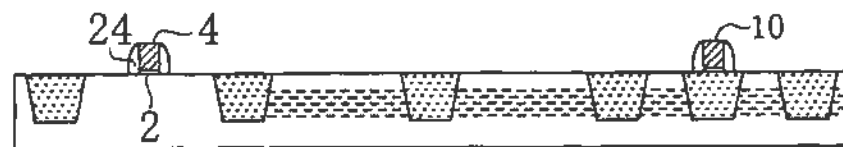


Fig. 15 (g)

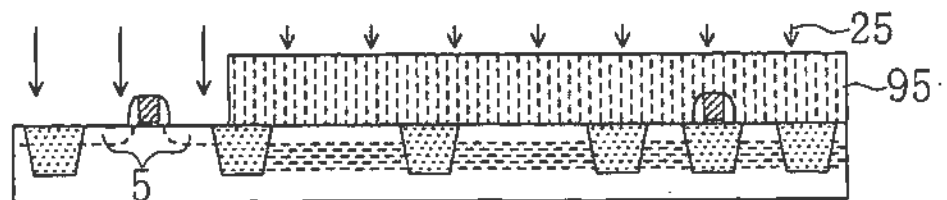
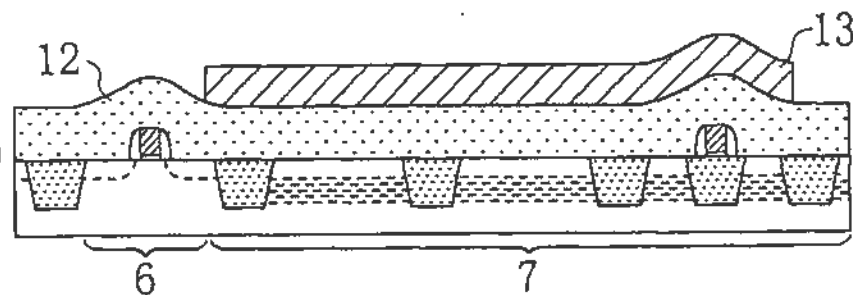
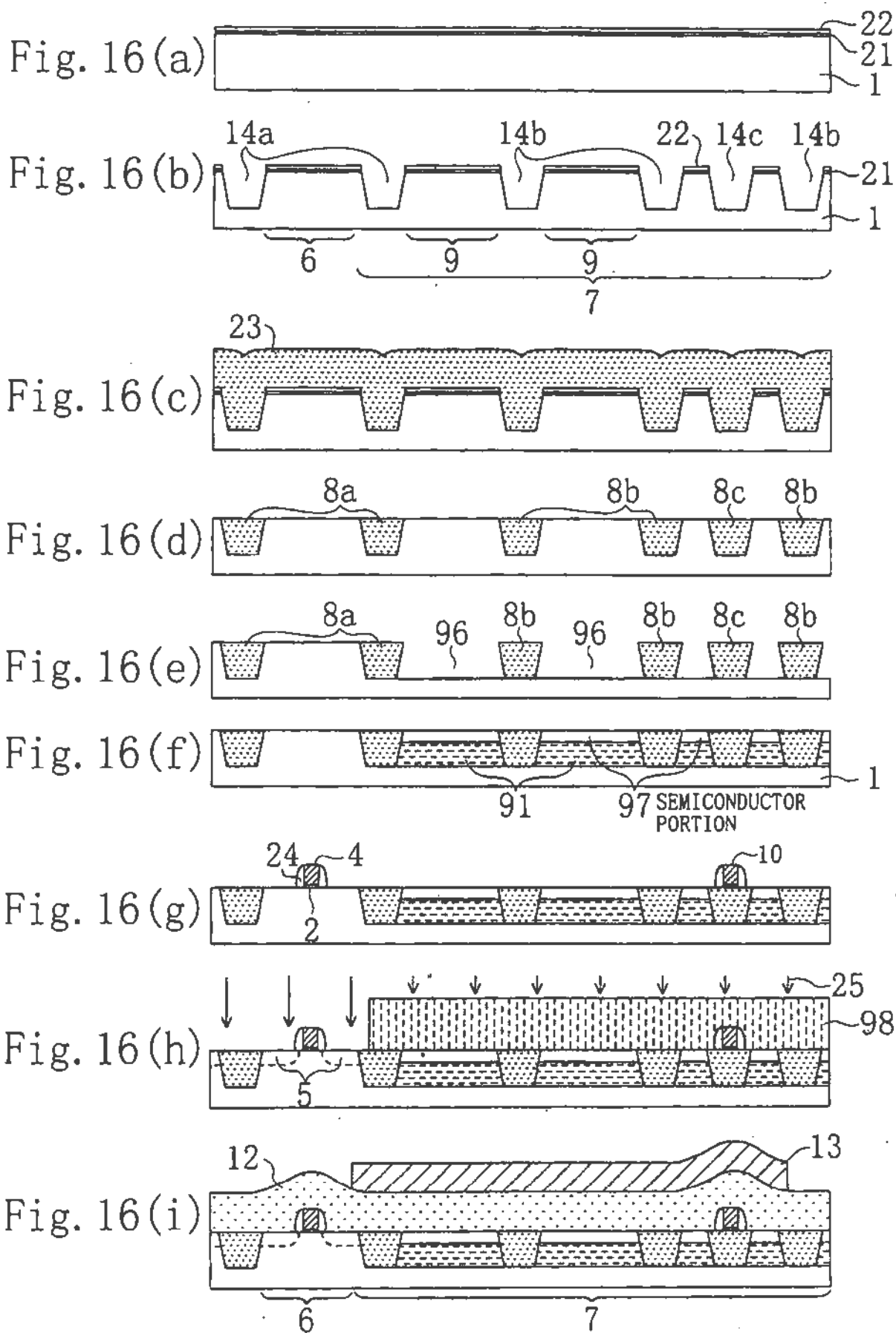
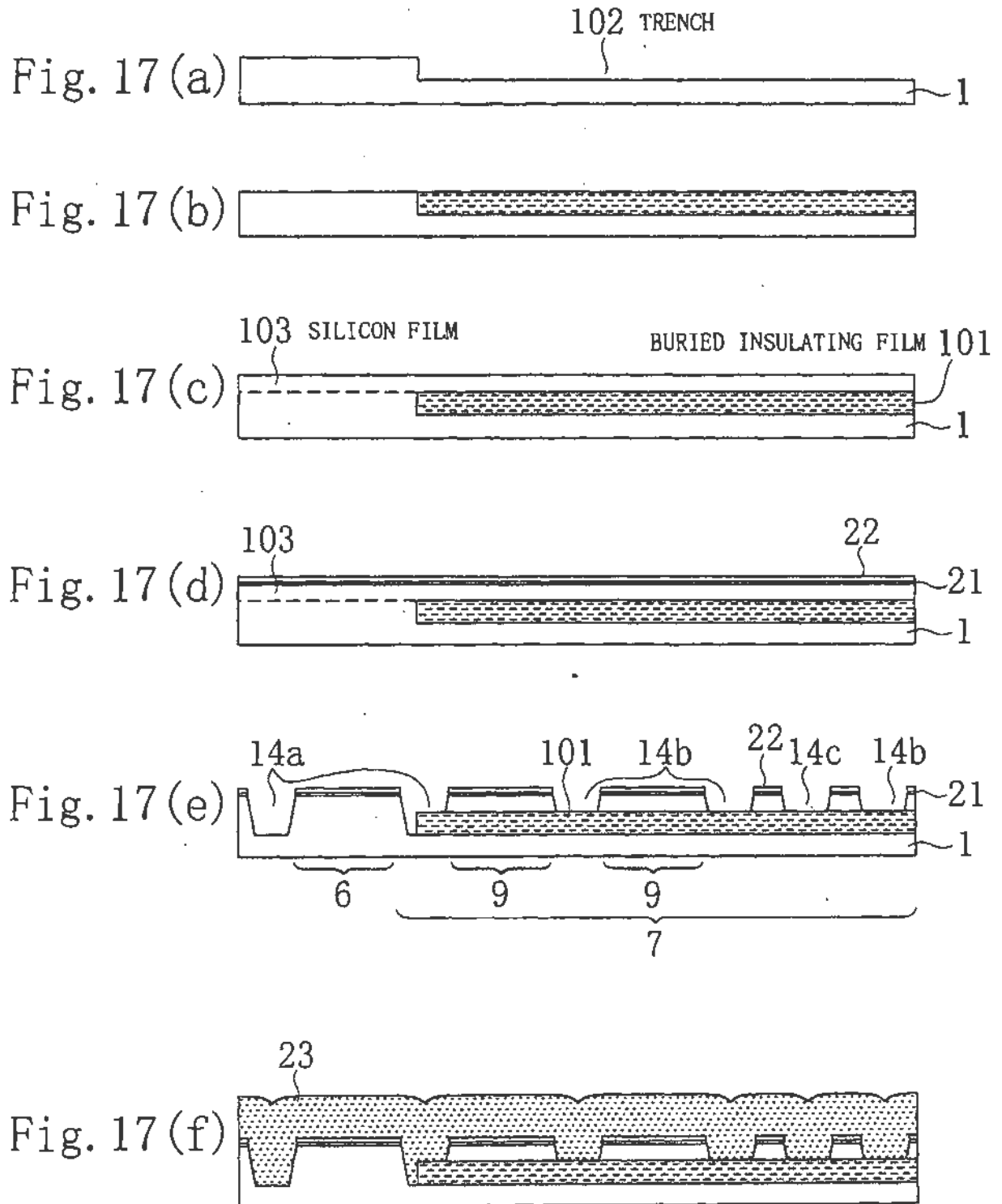


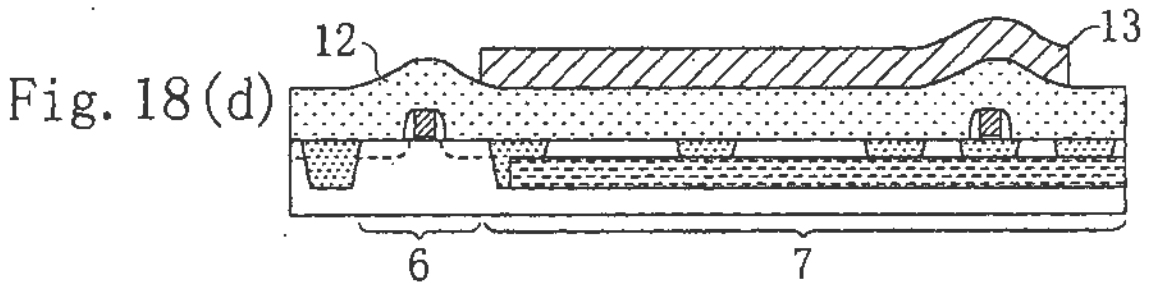
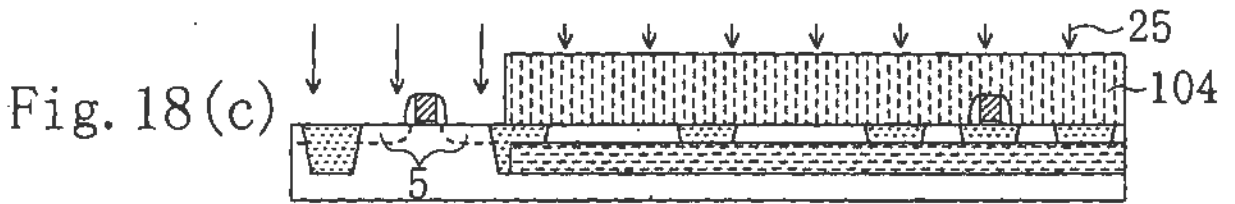
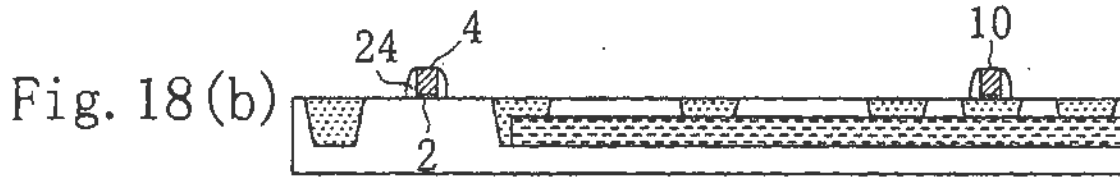
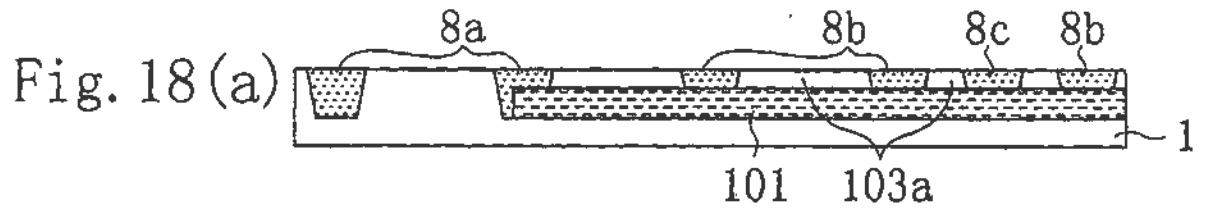
Fig. 15 (h)





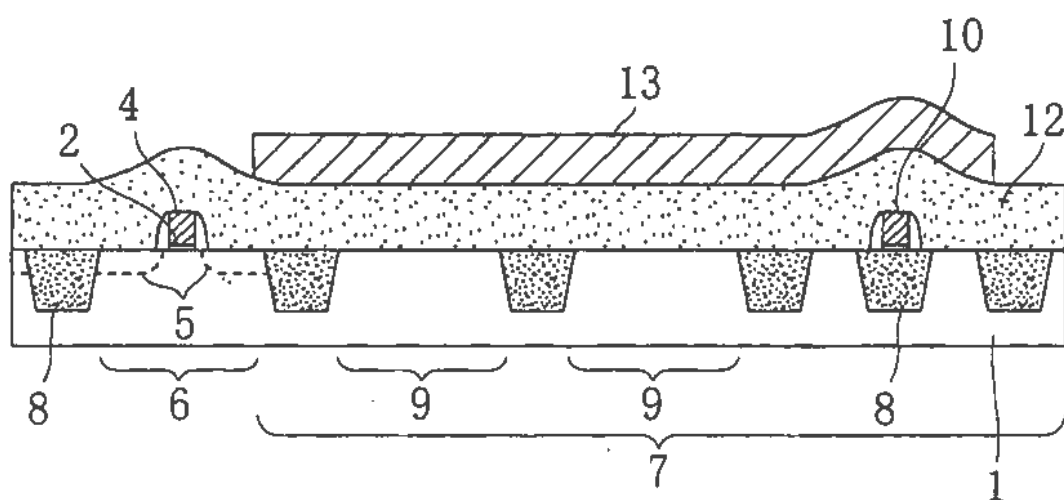
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Fig. 19
PRIOR ART



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Fig. 20(a)

PRIOR ART

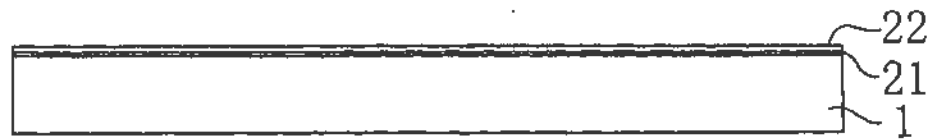


Fig. 20(b)

PRIOR ART

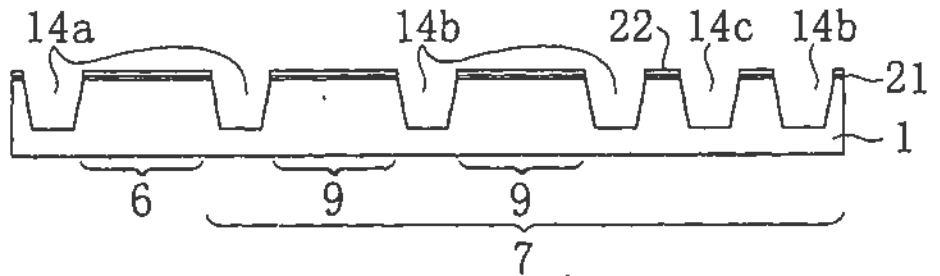


Fig. 20(c)

PRIOR ART

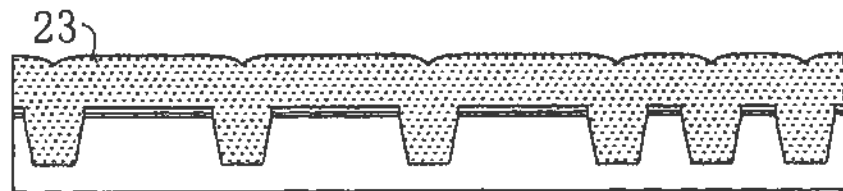


Fig. 20(d)

PRIOR ART

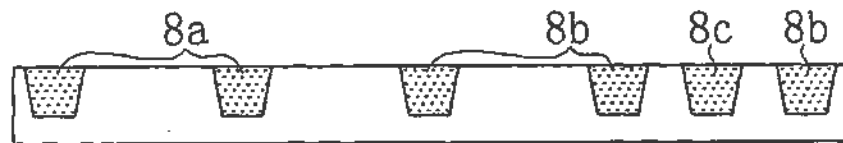


Fig. 20(e)

PRIOR ART

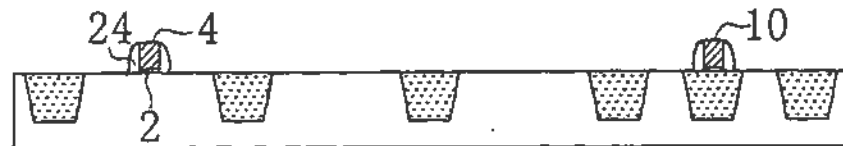


Fig. 20(f)

PRIOR ART

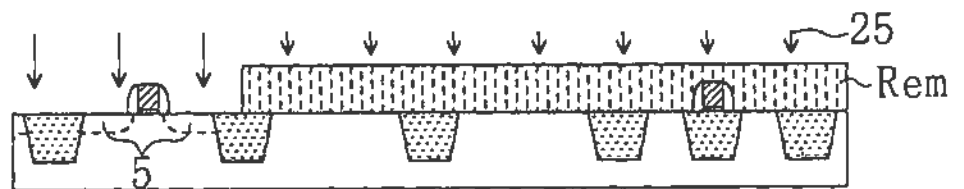


Fig. 20(g)

PRIOR ART

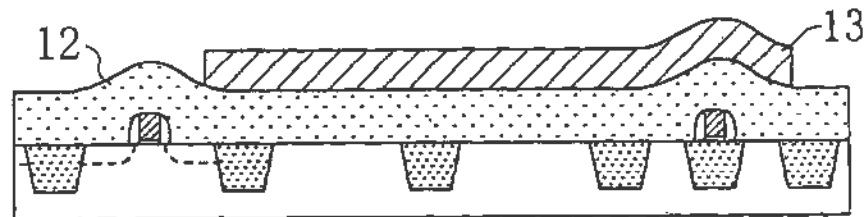


Fig. 21(a)

PRIOR ART

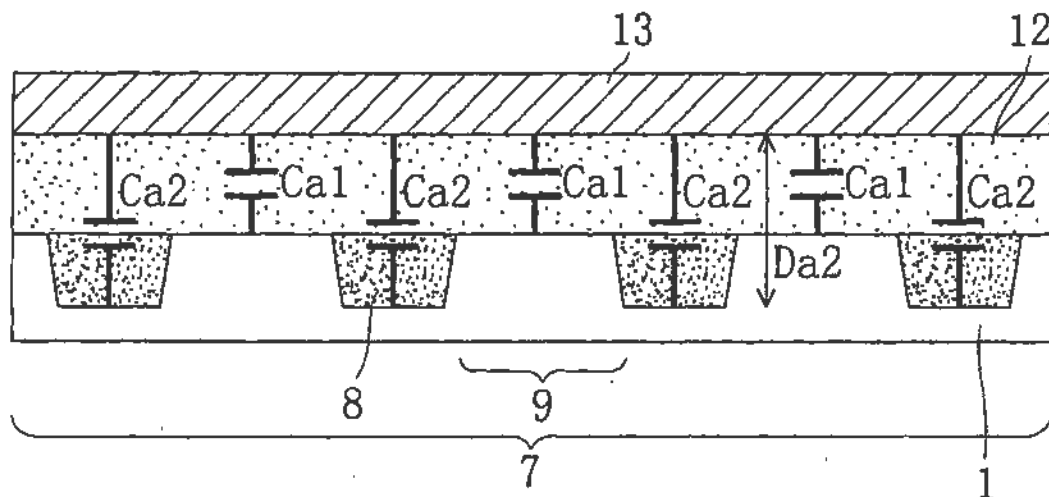


Fig. 21(b)

PRIOR ART

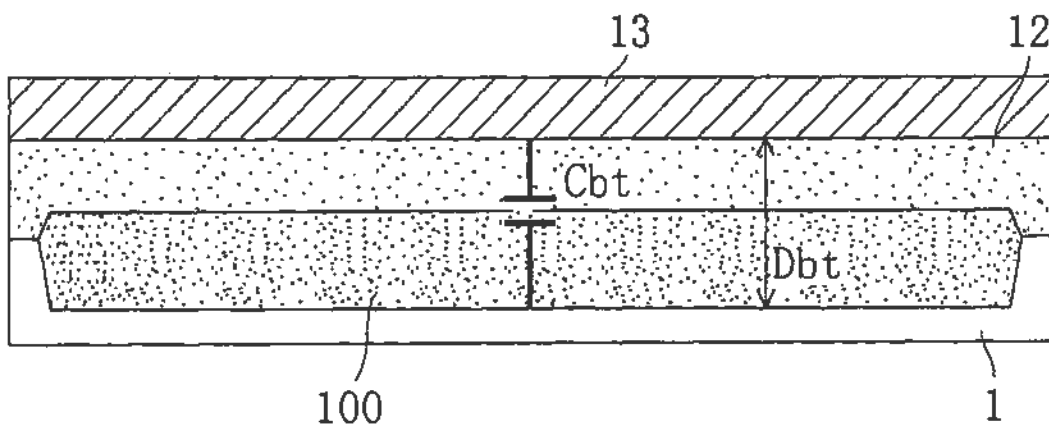


Fig. 1(a)

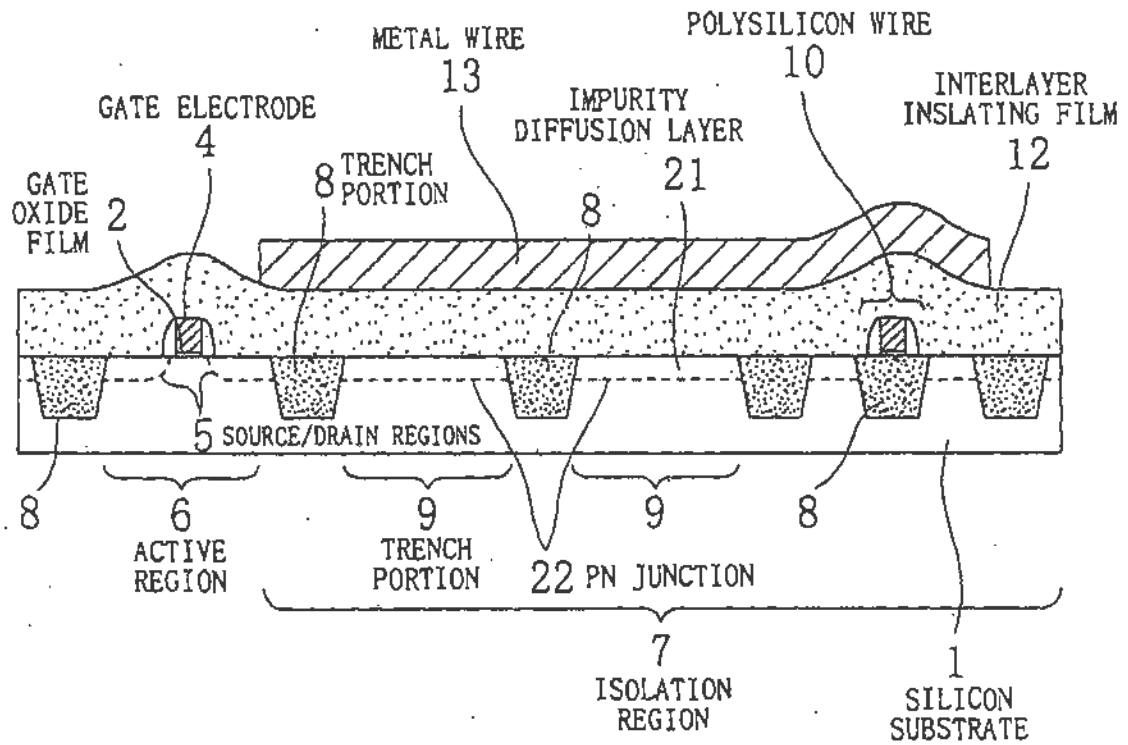
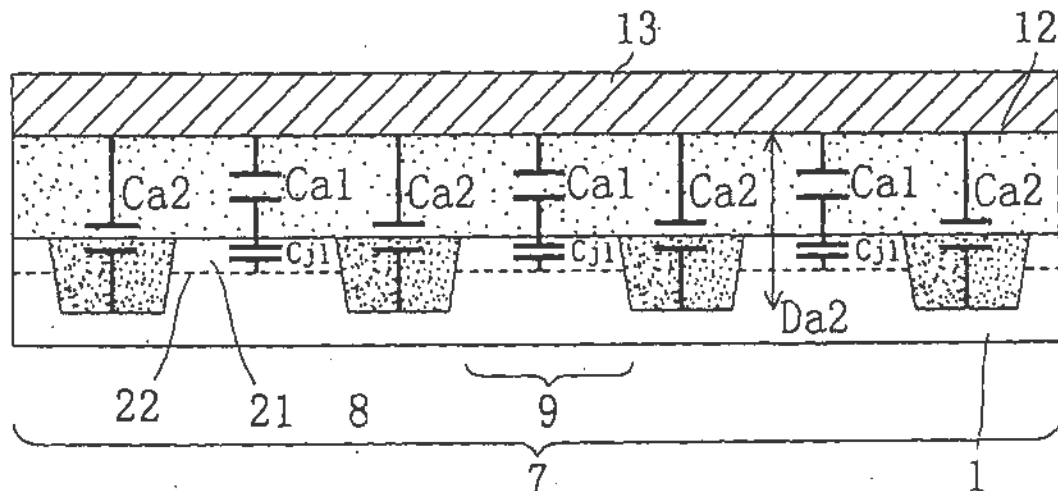
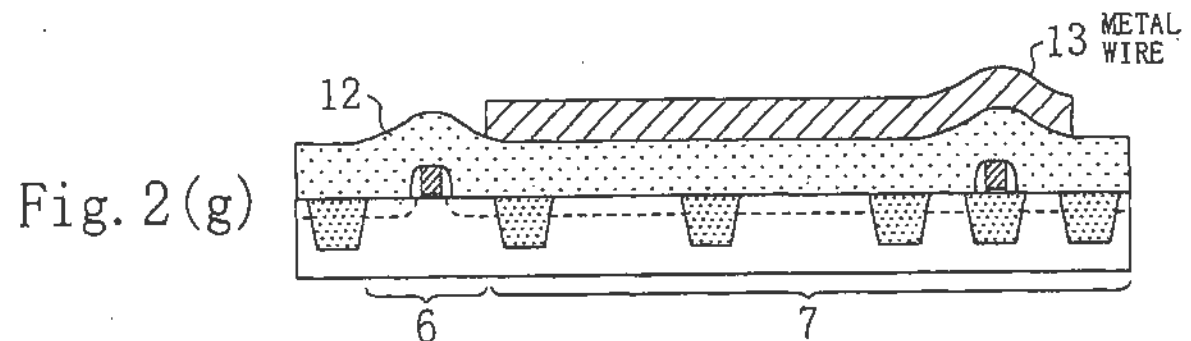
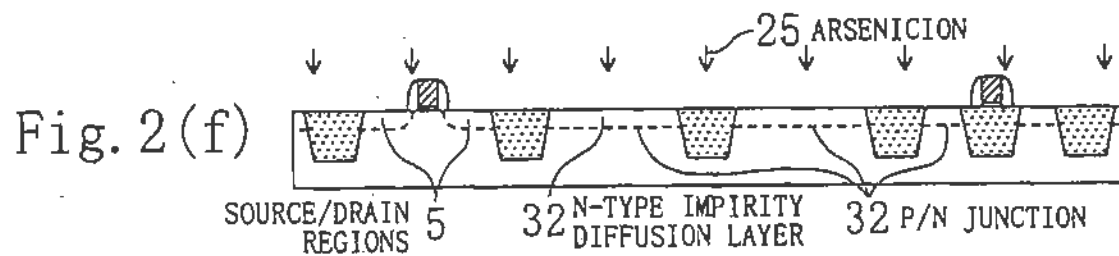
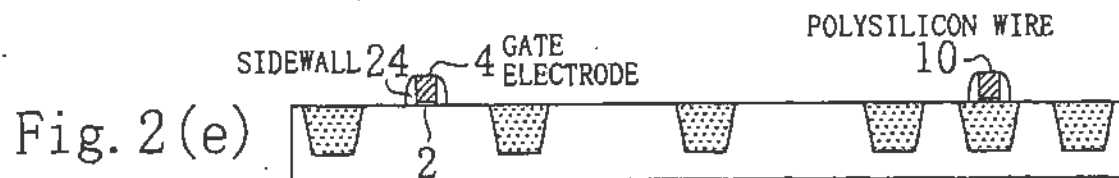
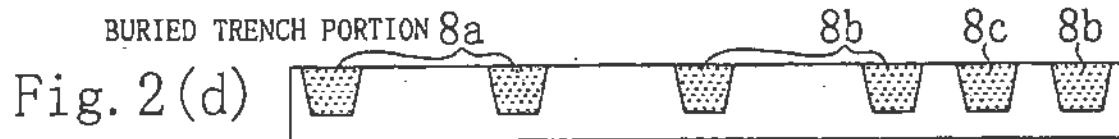
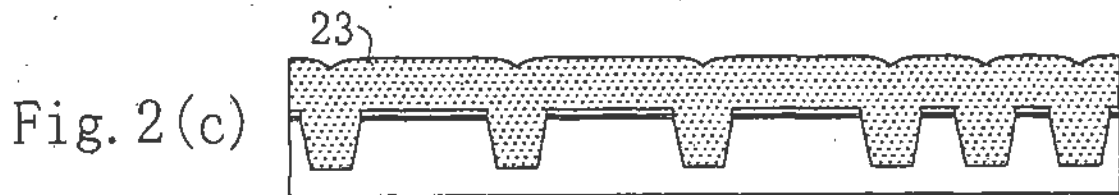
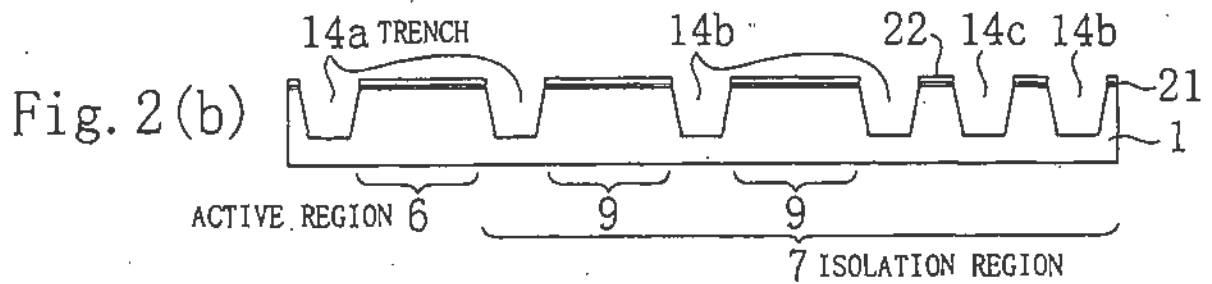
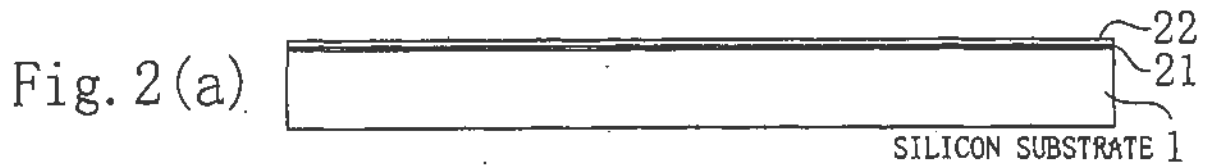


Fig. 1(b)

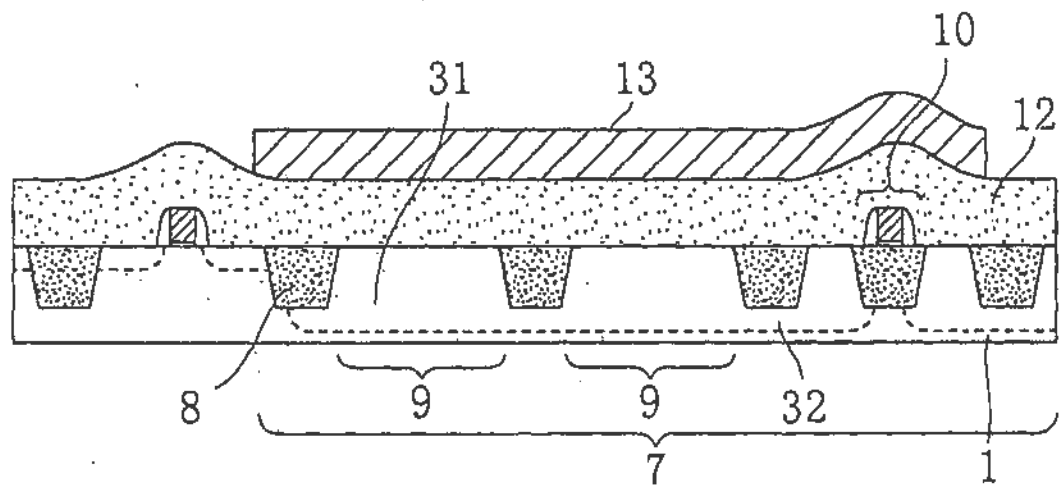


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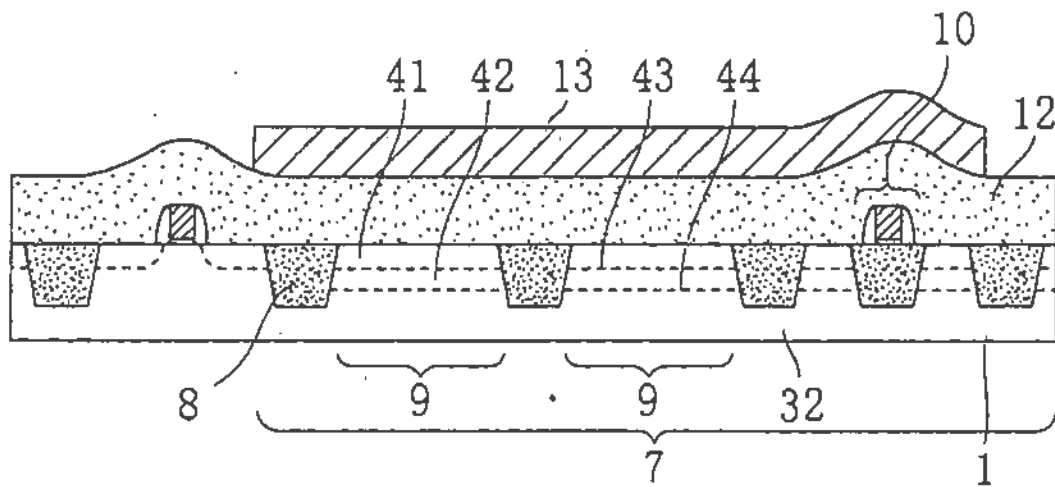
405077-1/18/2018

Fig. 3



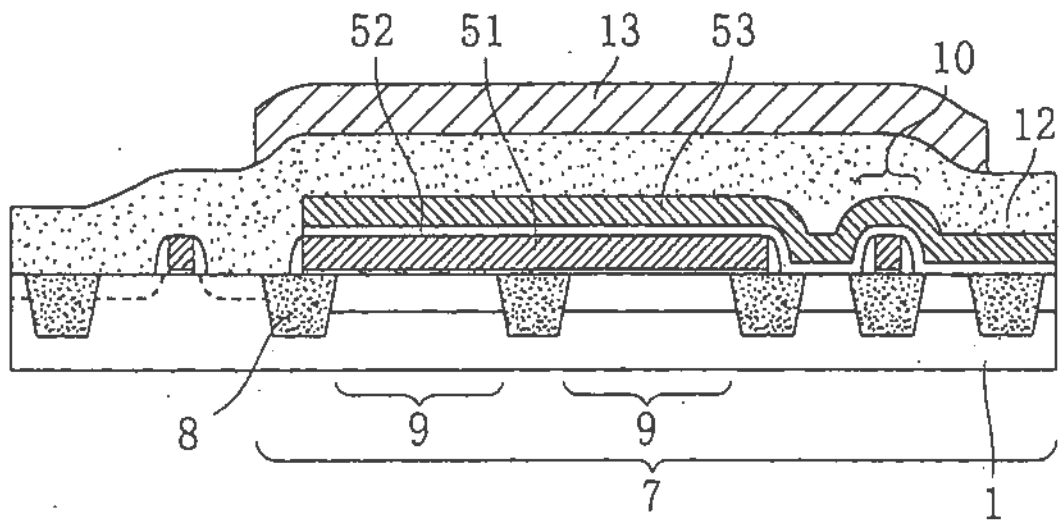
0891137-1138/680

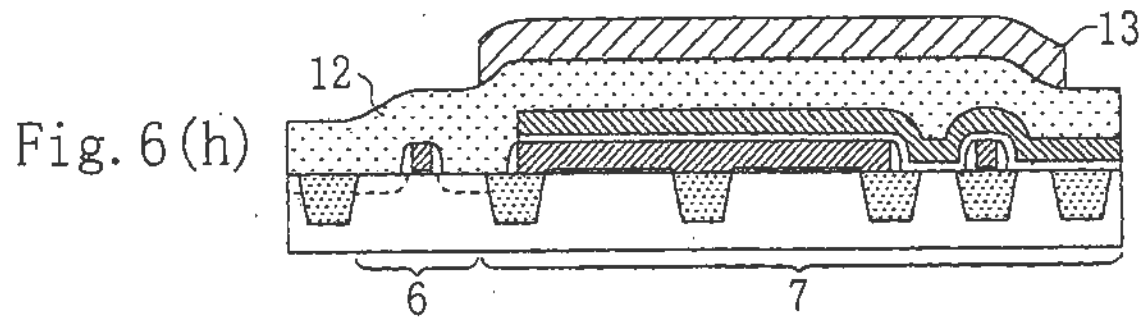
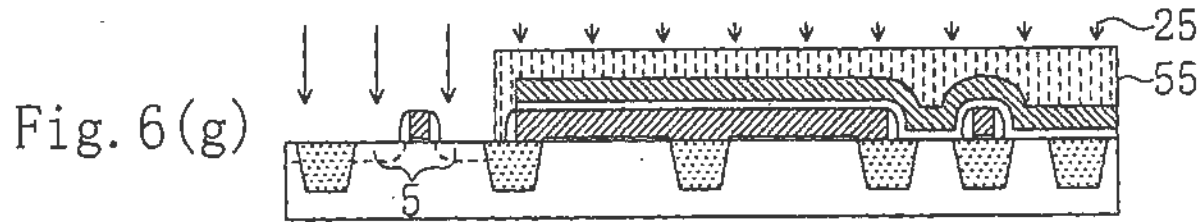
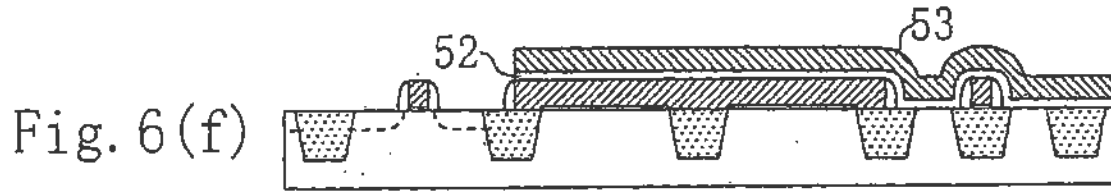
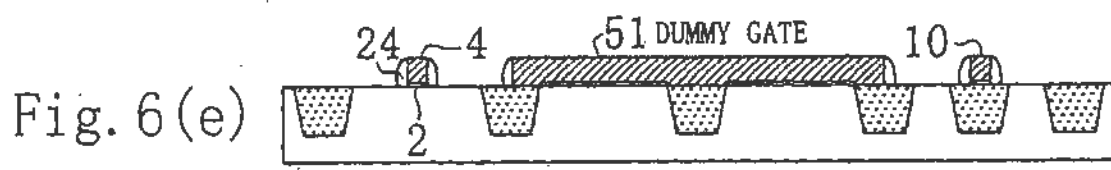
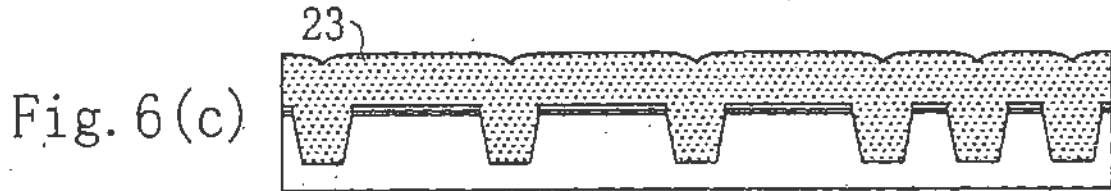
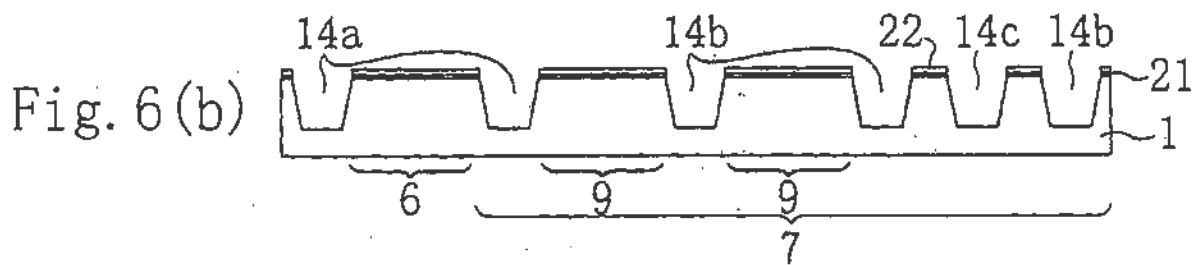
Fig. 4



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Fig. 5

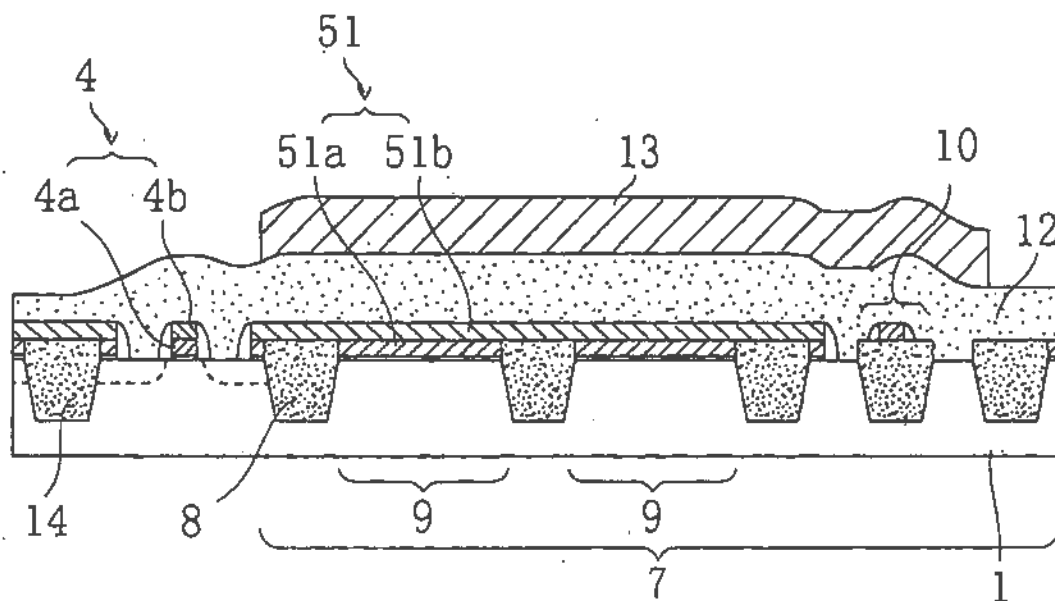




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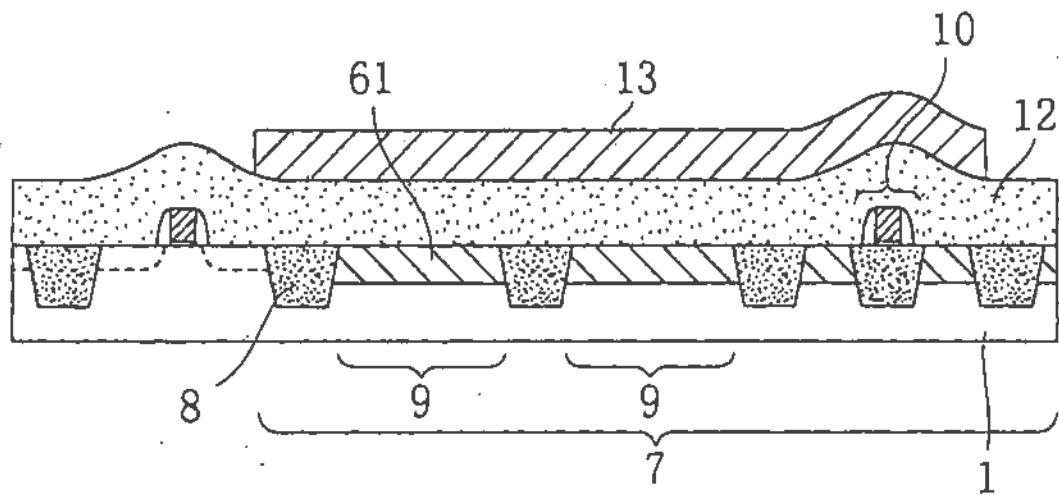
202511 26782680

Fig. 7



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Fig. 8



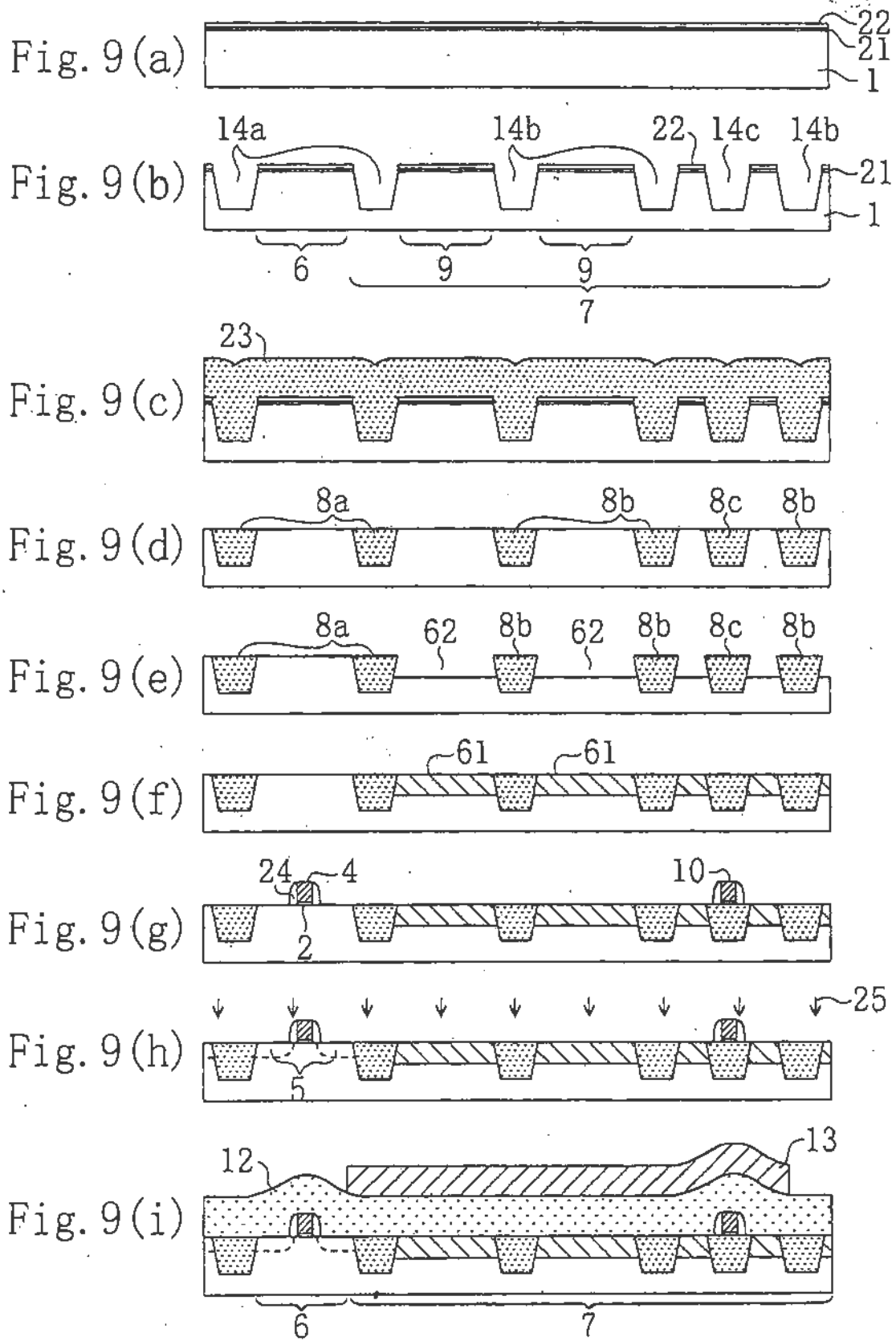
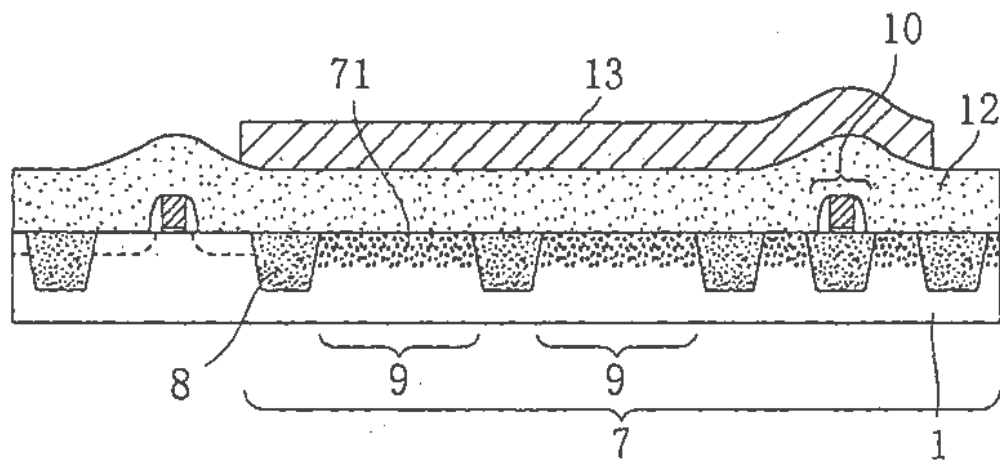
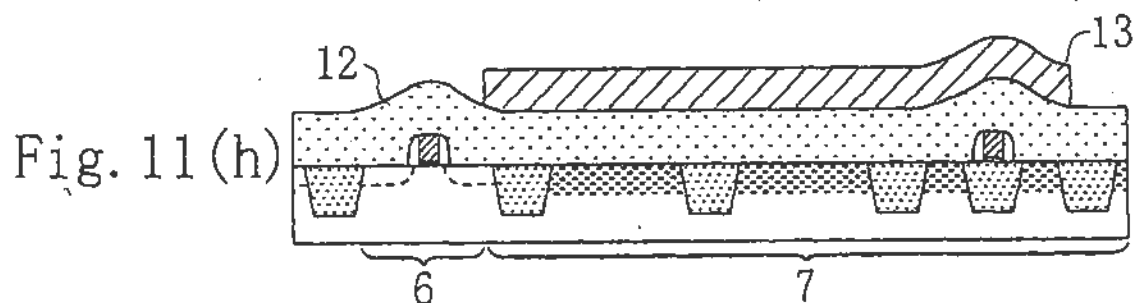
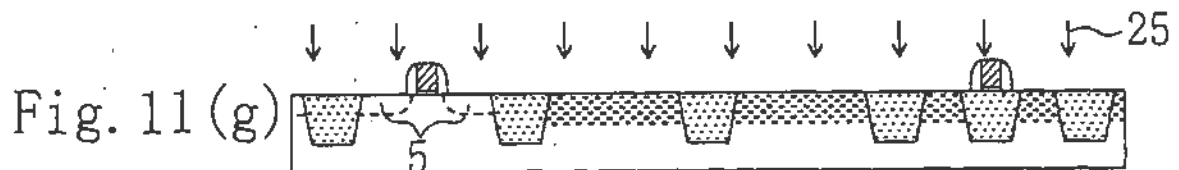
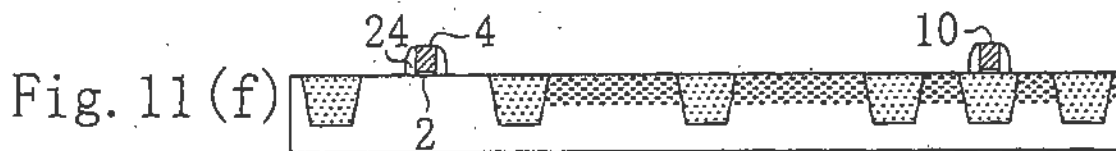
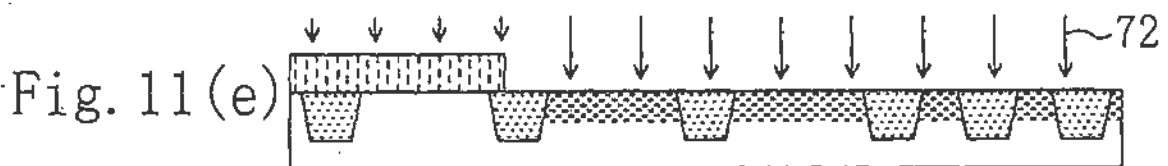
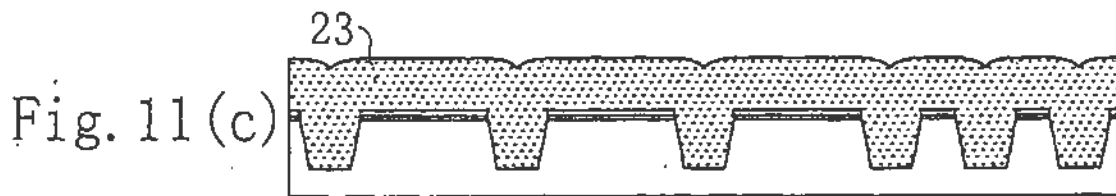
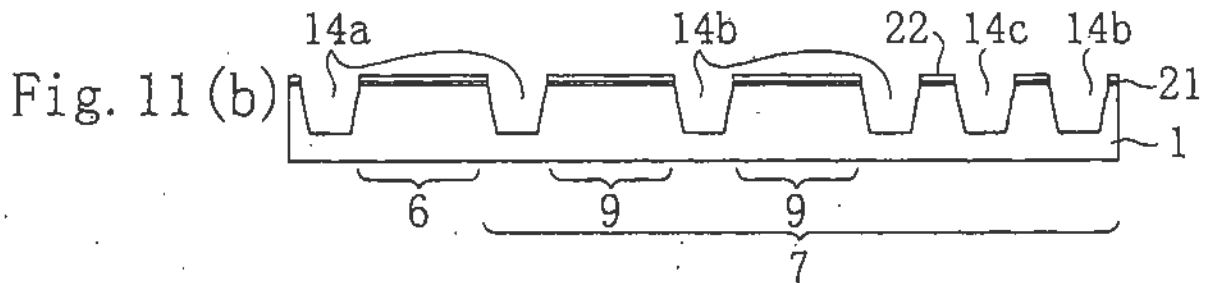


FIG. 10

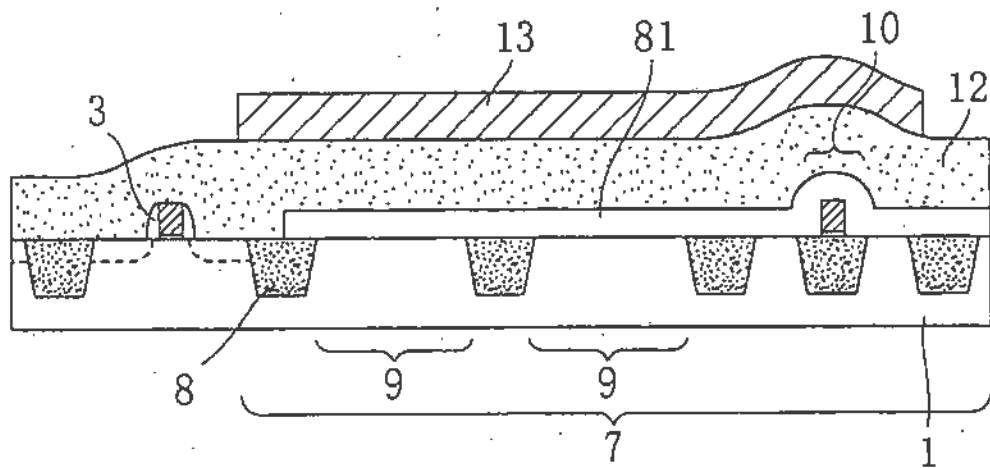
Fig. 10

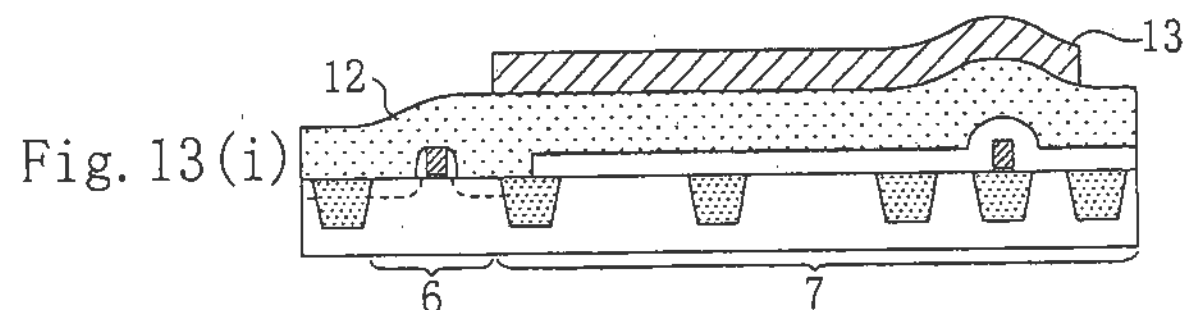
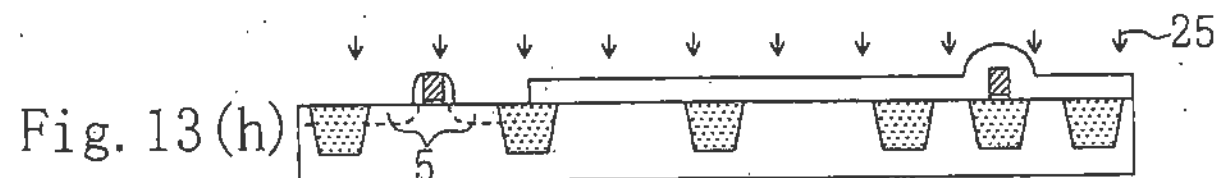
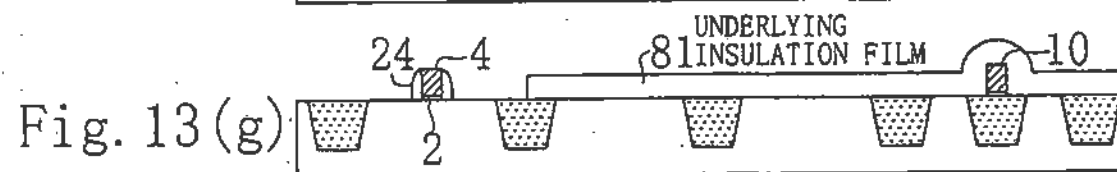
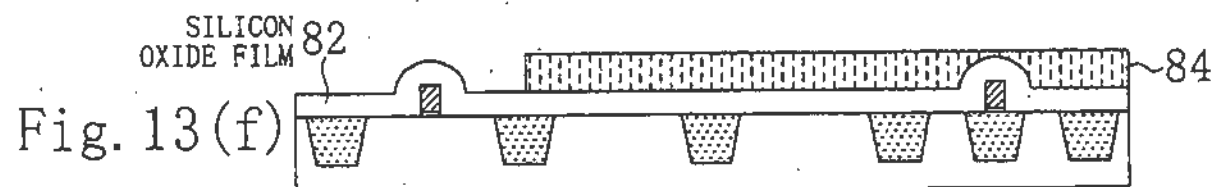
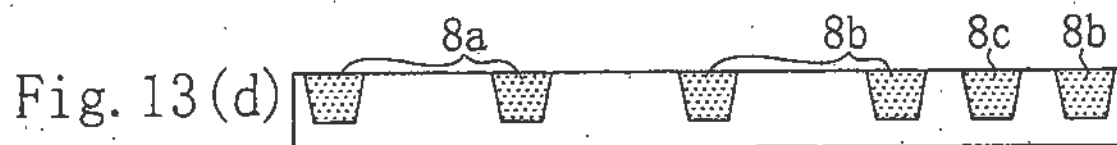
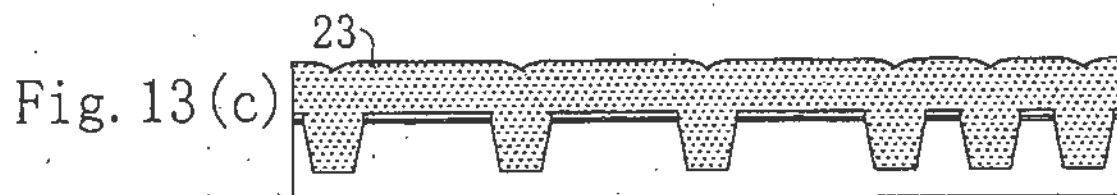
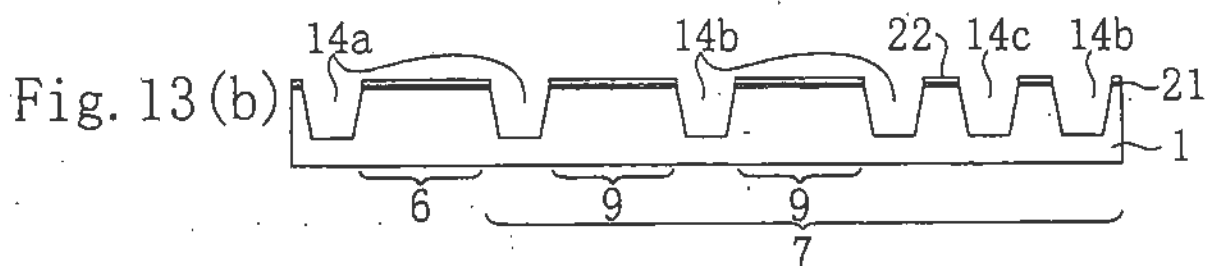




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Fig. 12





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Fig. 14(a)

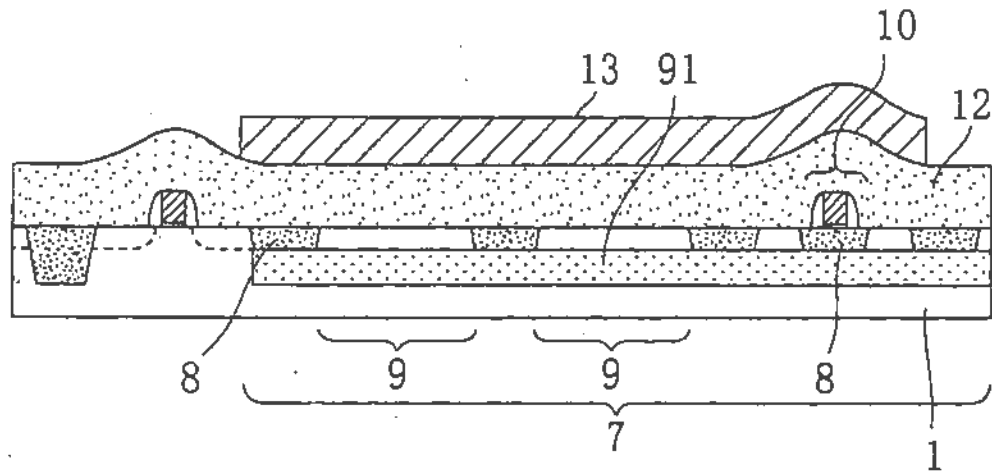
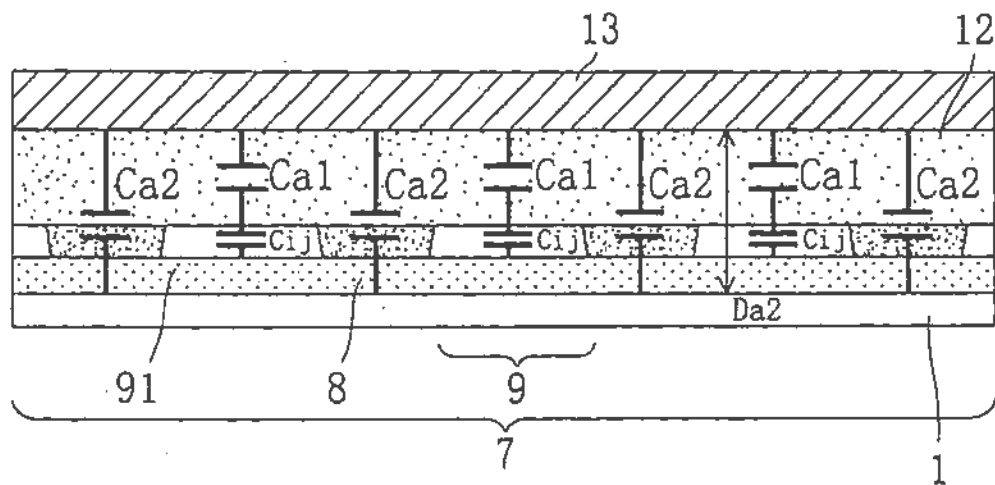
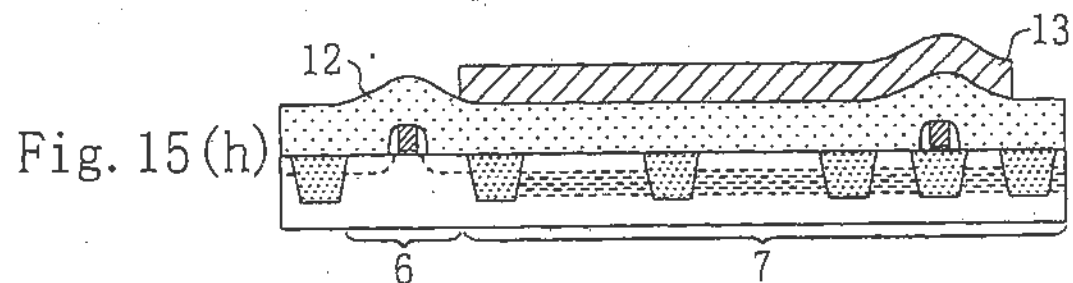
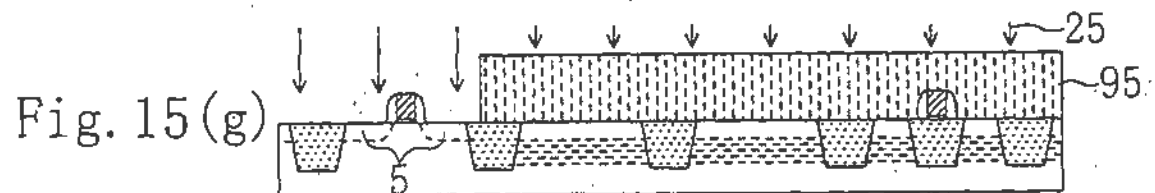
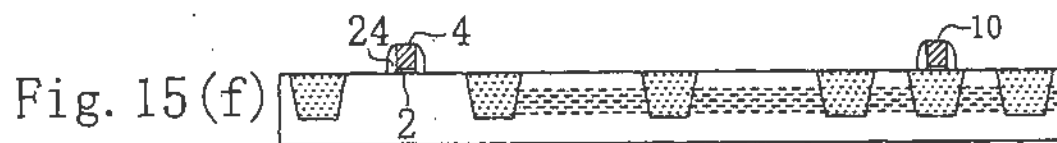
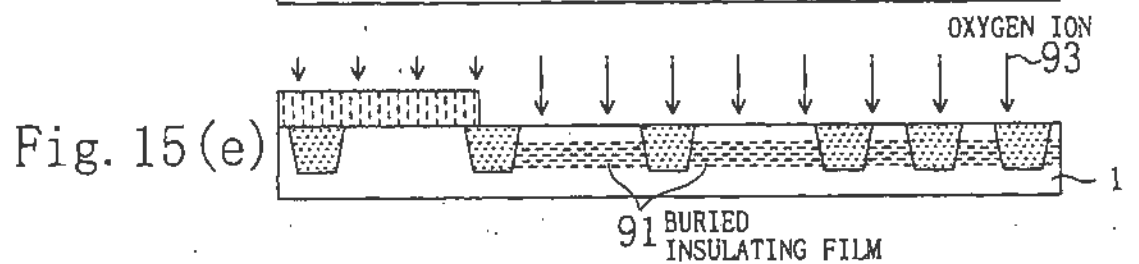
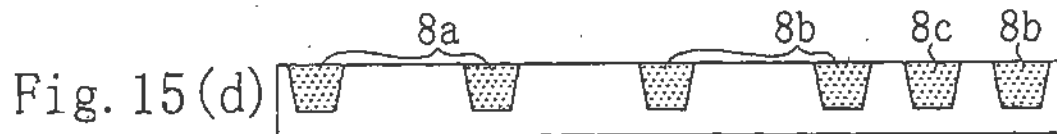
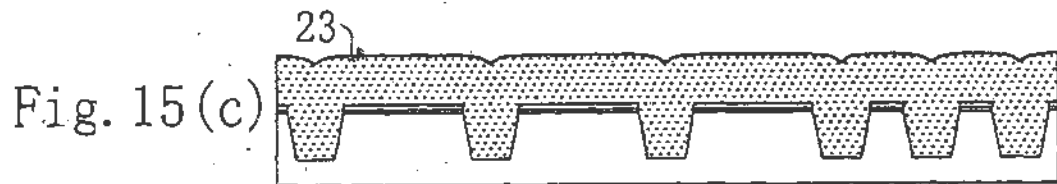
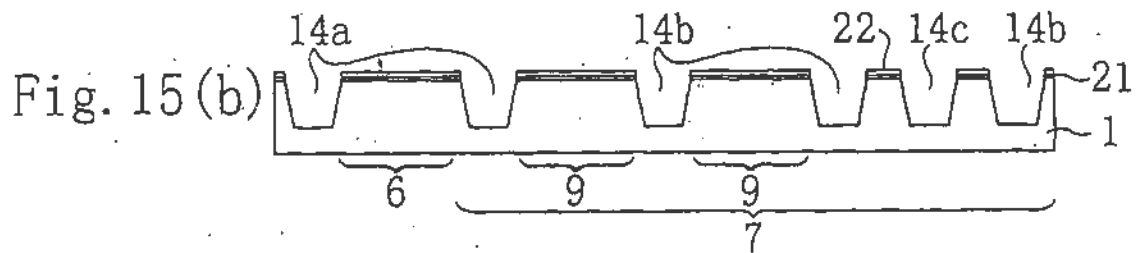
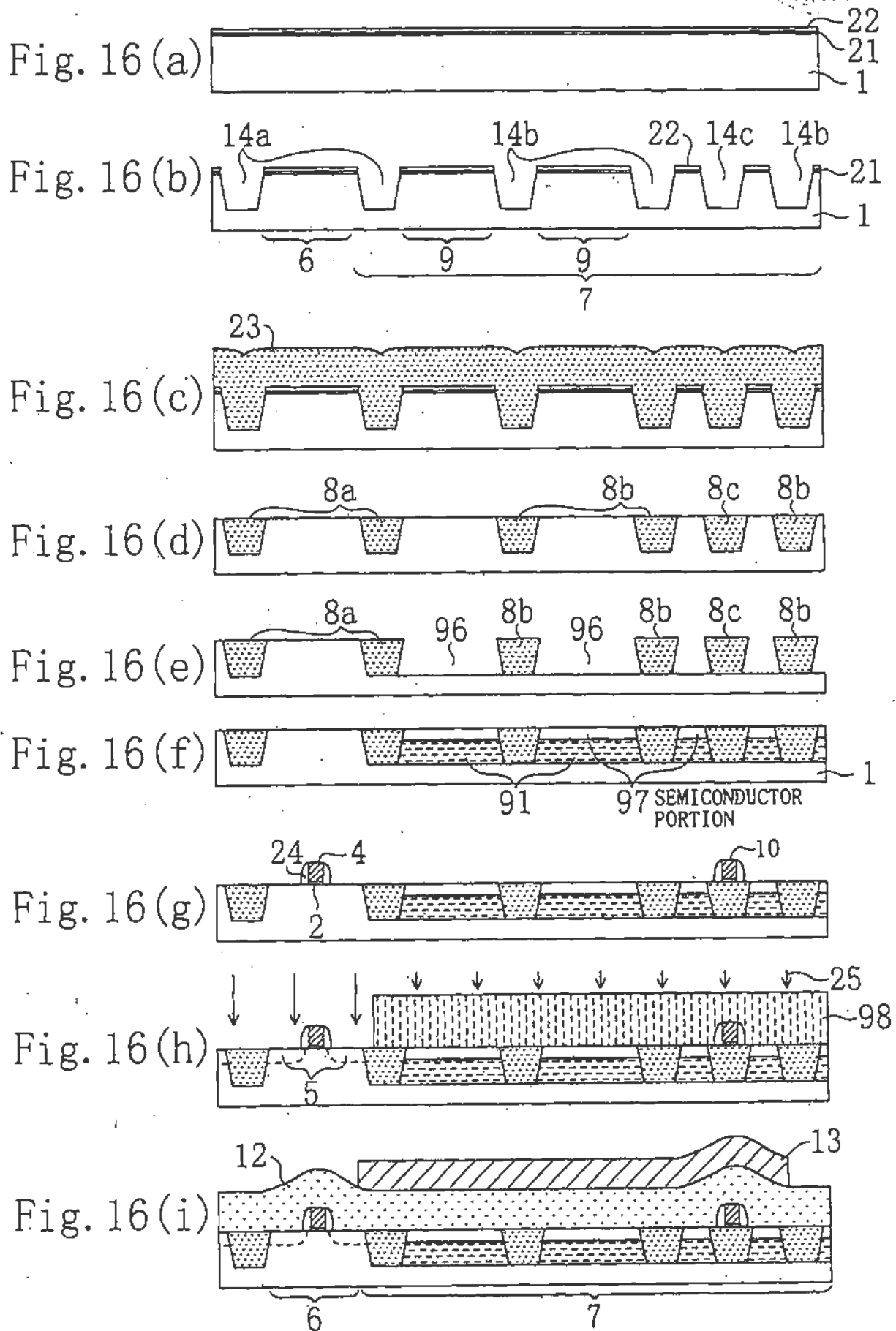


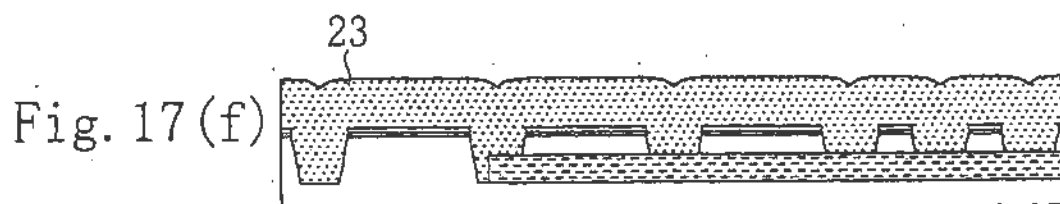
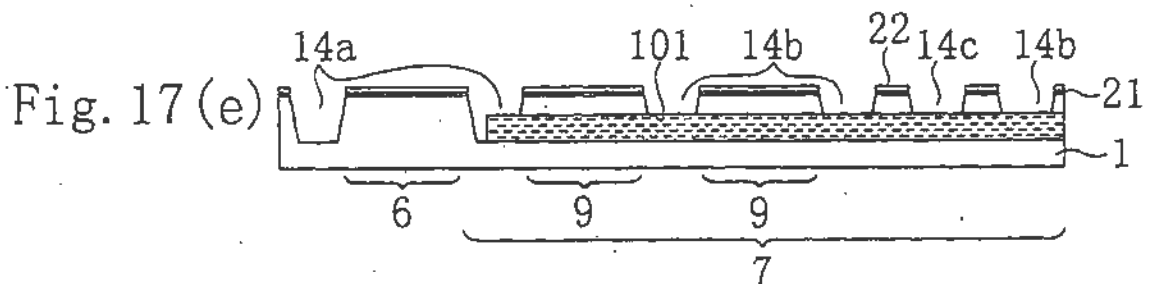
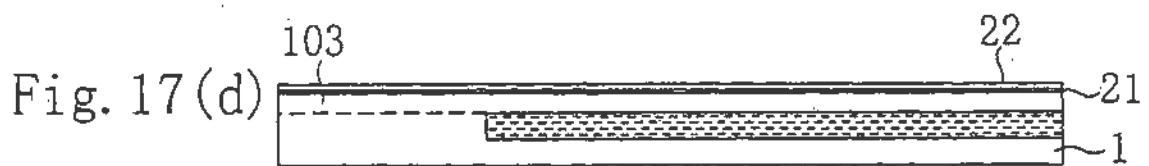
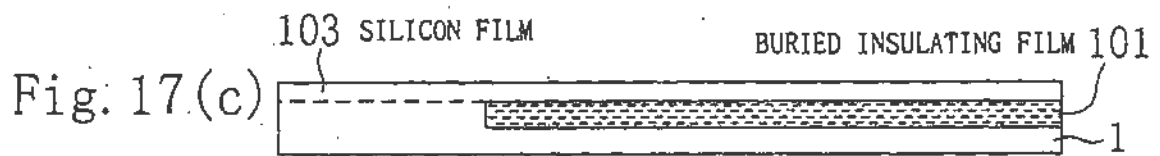
Fig. 14(b)

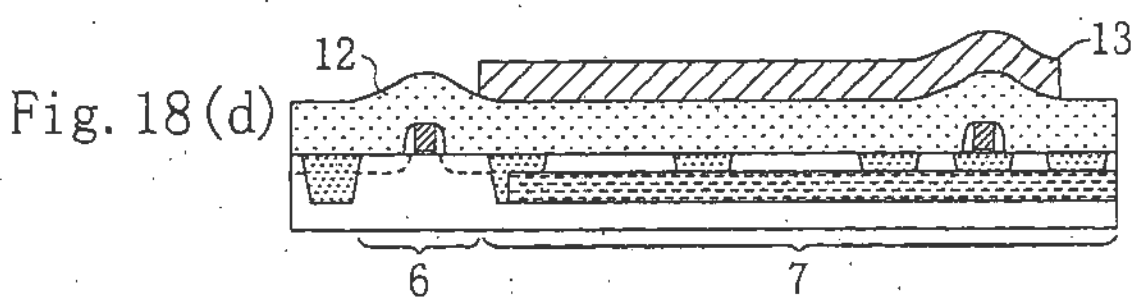
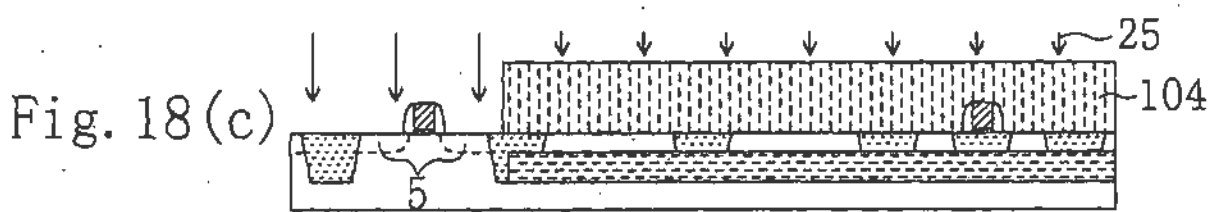
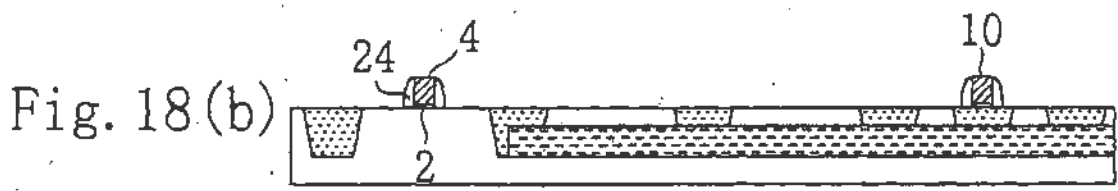
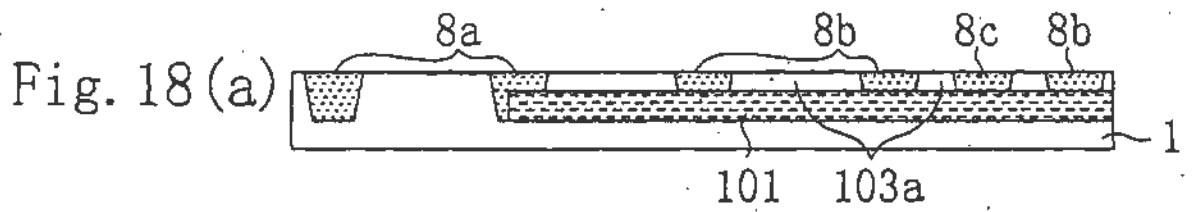






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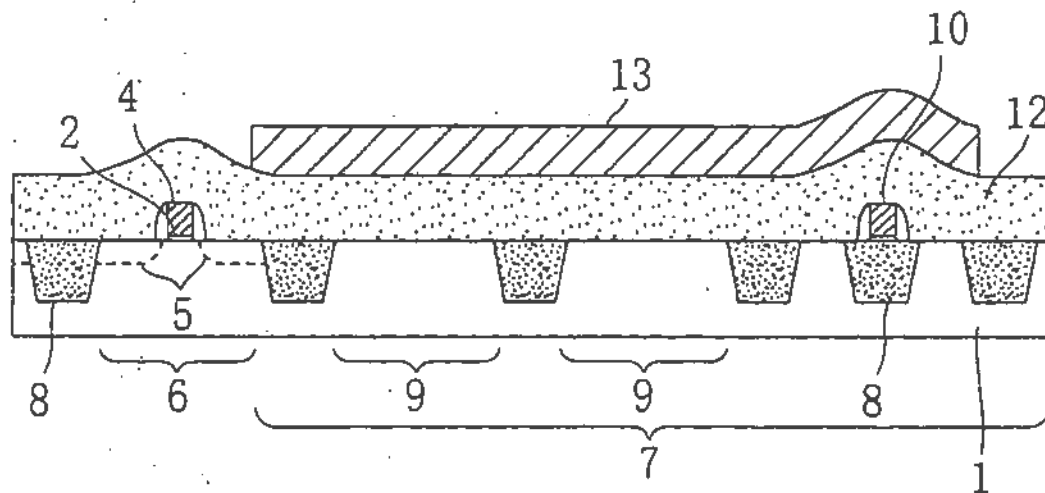




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100-100
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Fig. 19
PRIOR ART



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Fig. 20(a)
PRIOR ART



Fig. 20(b)
PRIOR ART

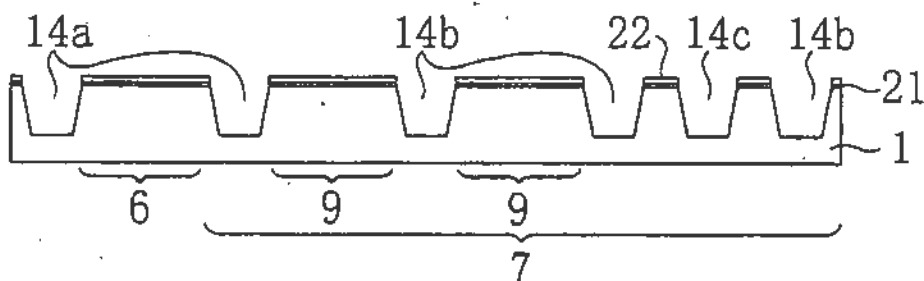


Fig. 20(c)
PRIOR ART

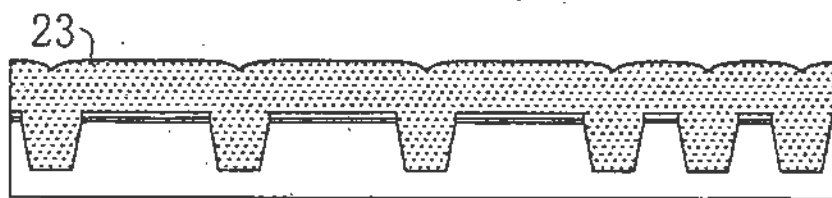


Fig. 20(d)
PRIOR ART

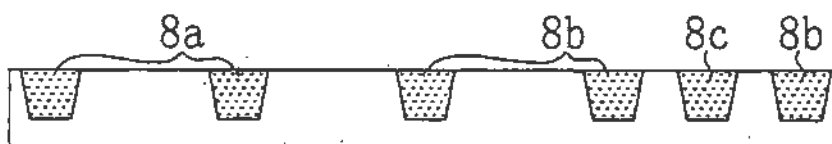


Fig. 20(e)
PRIOR ART

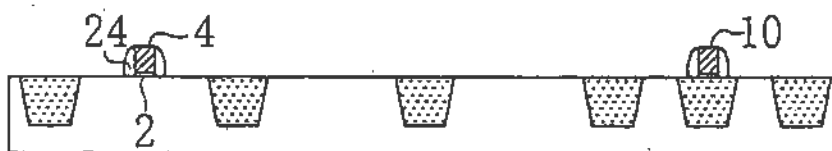


Fig. 20(f)
PRIOR ART

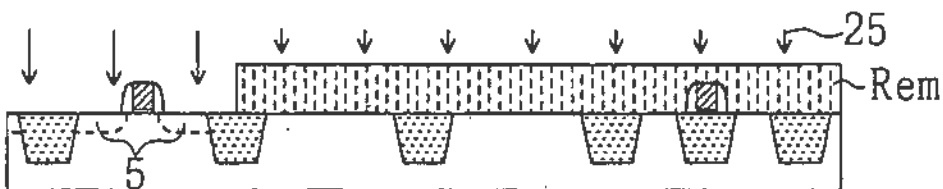
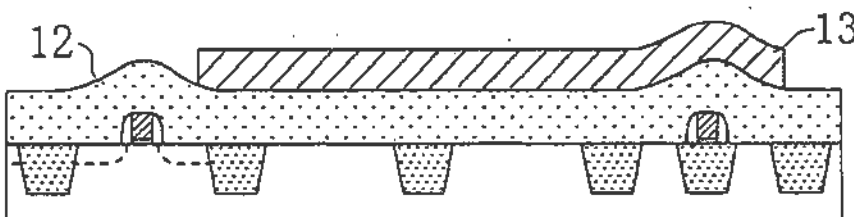


Fig. 20(g)
PRIOR ART



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Fig. 21(a)

PRIOR ART

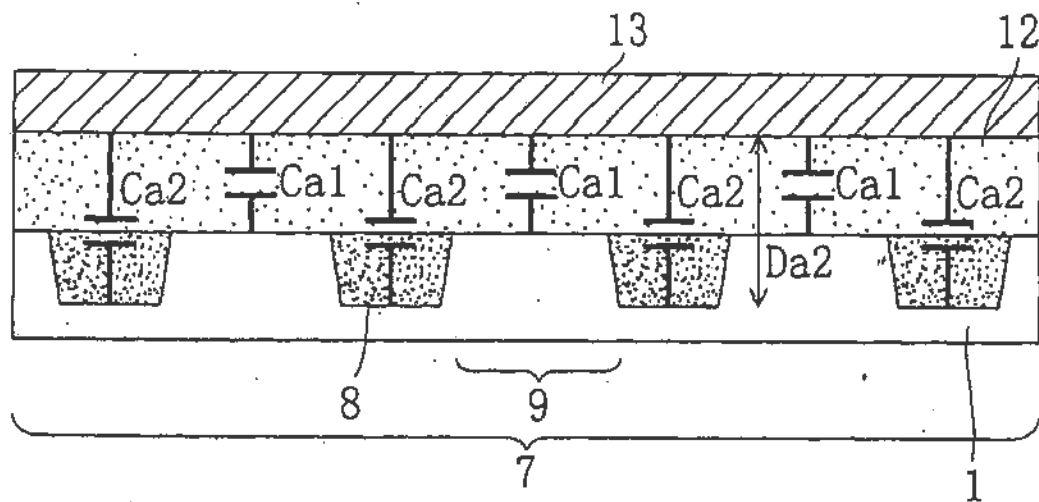


Fig. 21(b)

PRIOR ART

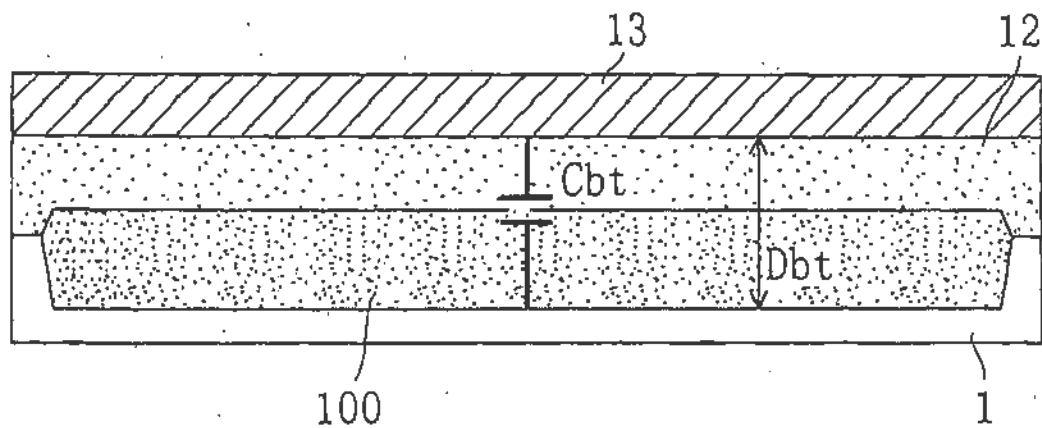


Fig. 1(a)

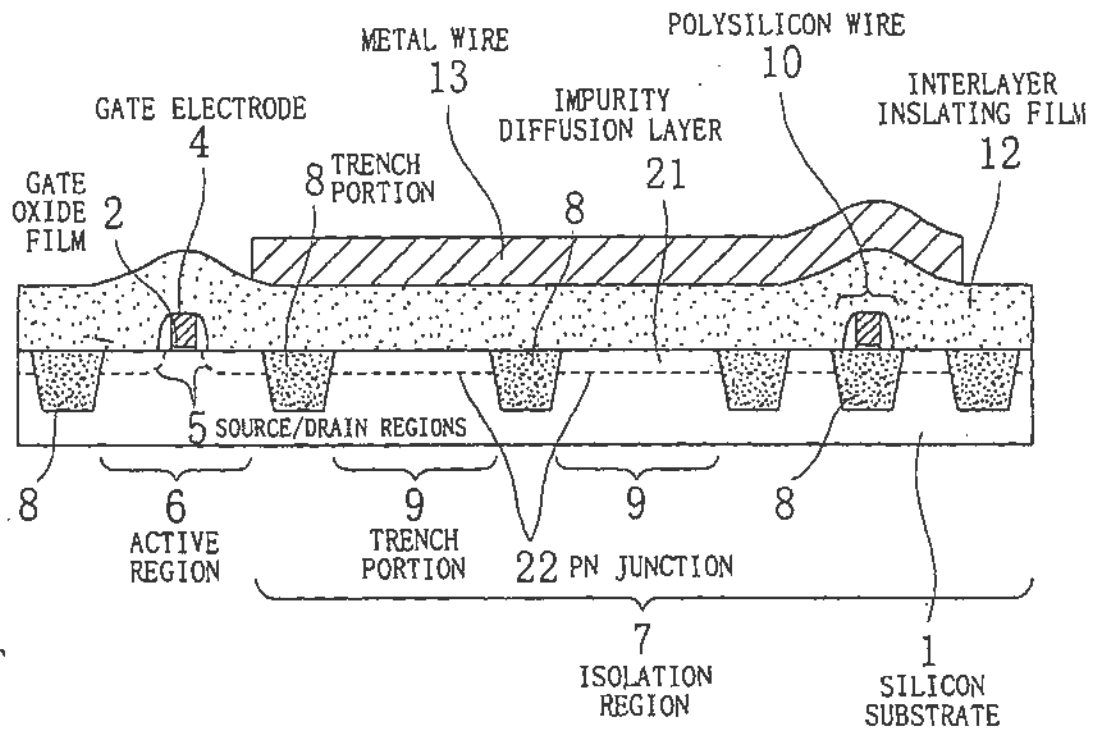
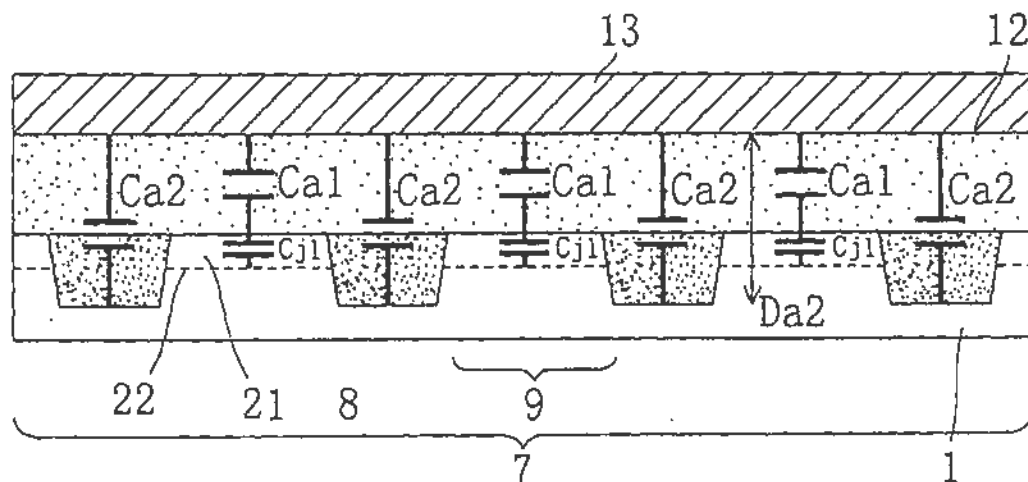
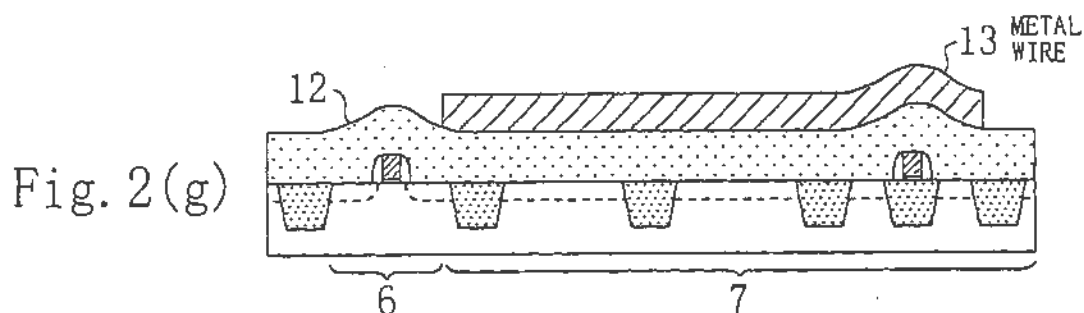
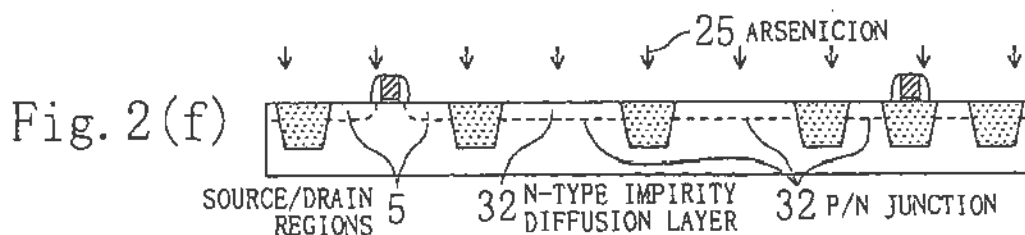
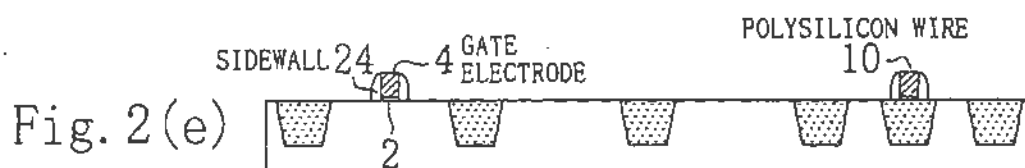
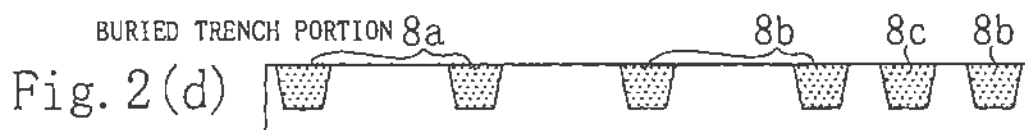
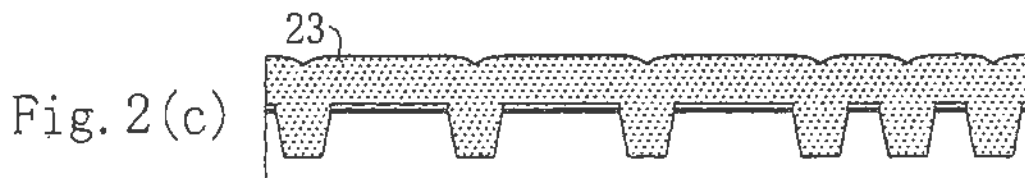
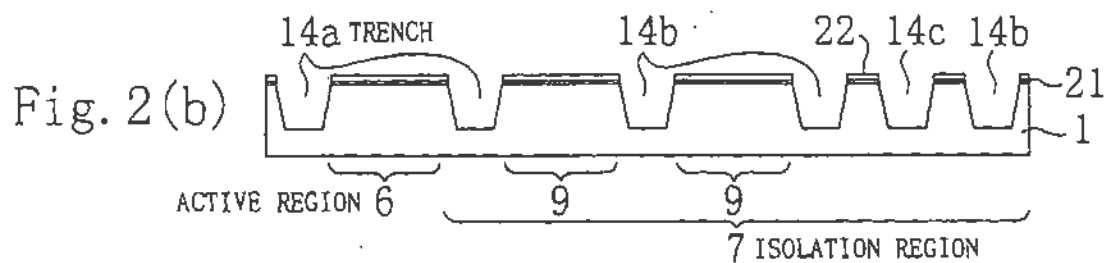


Fig. 1(b)

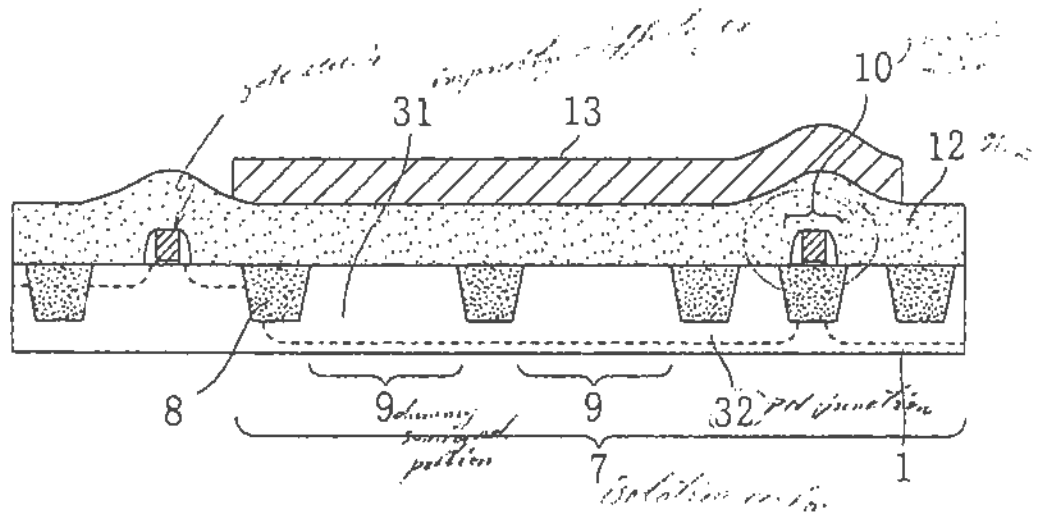


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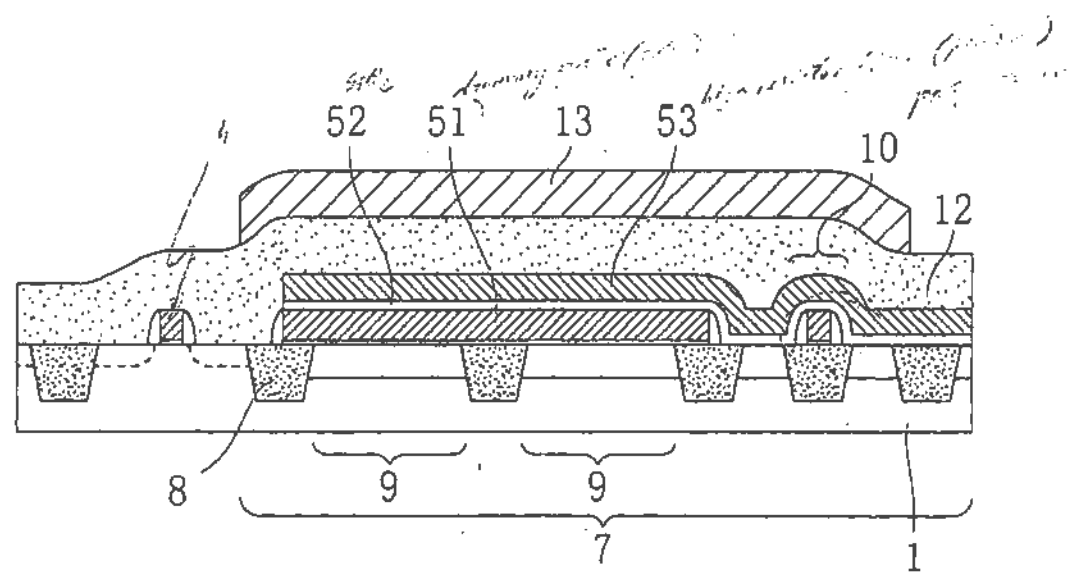
Fig. 3



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4th Embodiment

Fig. 5



4, 51, 10 form structure

Fig. 6(b)

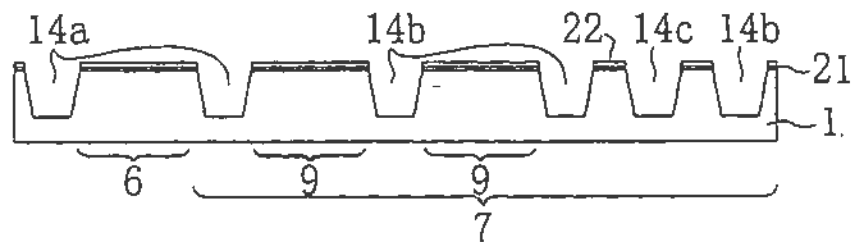


Fig. 6(c)

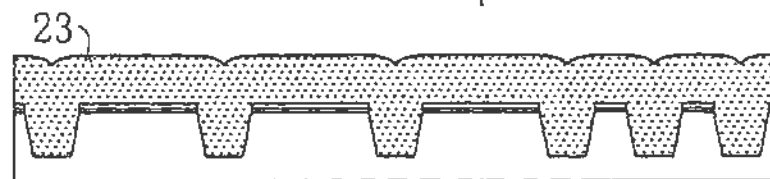


Fig. 6(d)



Fig. 6(e)



Fig. 6(f)

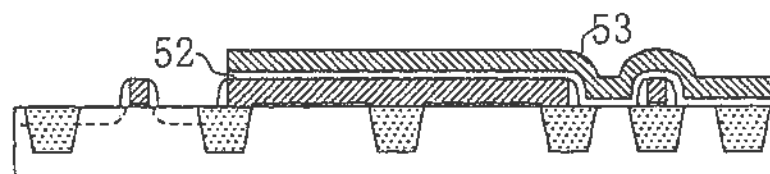


Fig. 6(g)

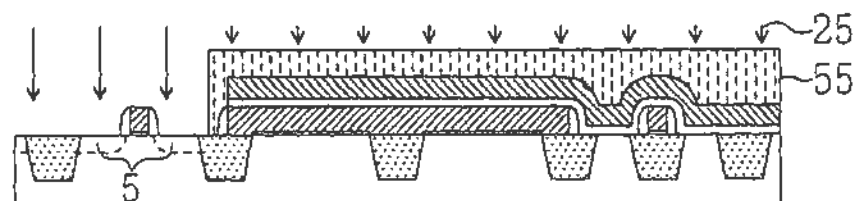
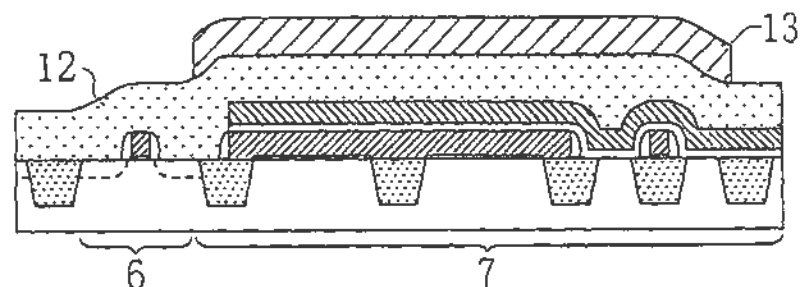
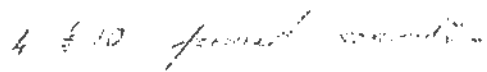


Fig. 6(h)



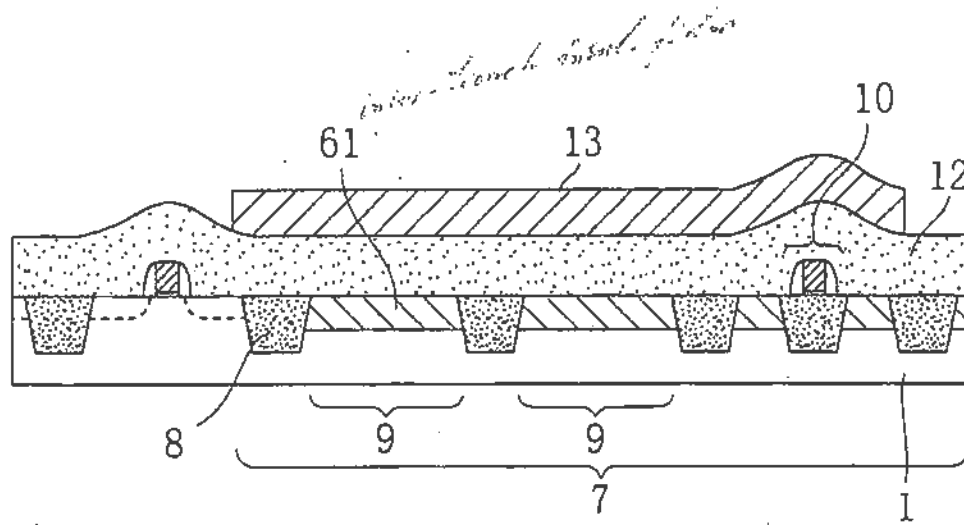
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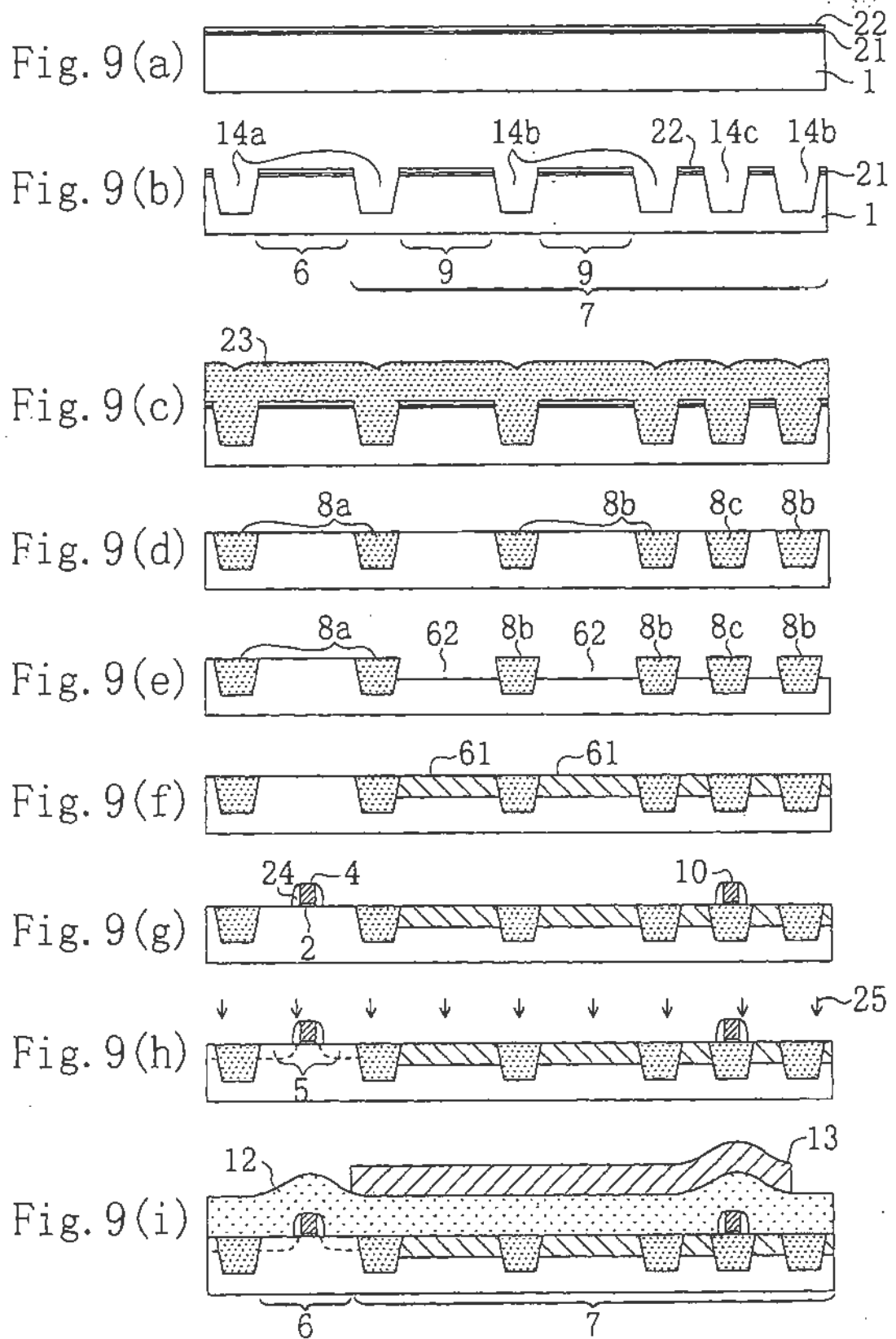
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the tool.

Fig. 8

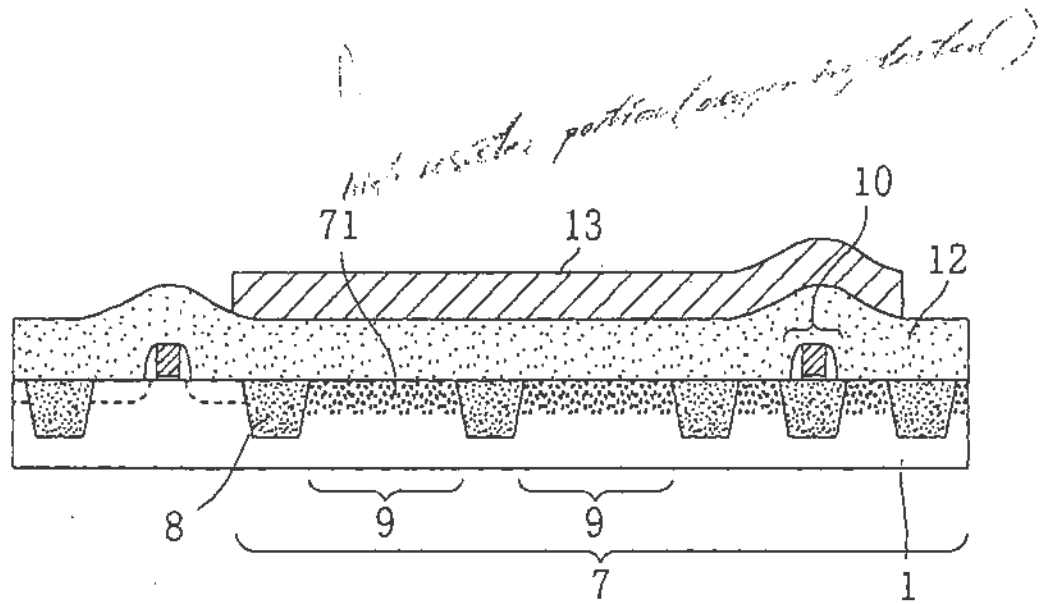




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7th Embodiment

Fig. 10



9

1, 8, 13, 14, 20

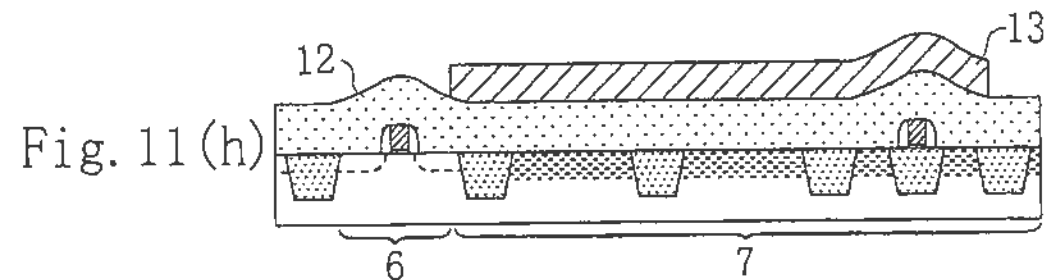
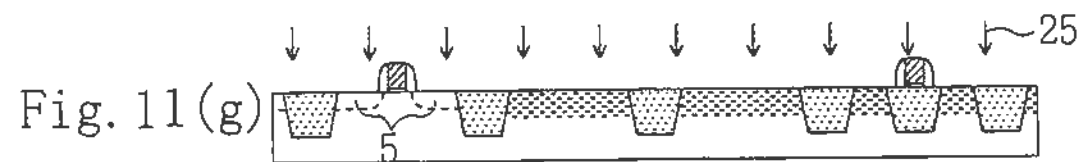
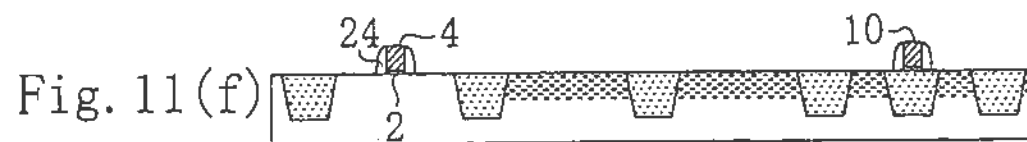
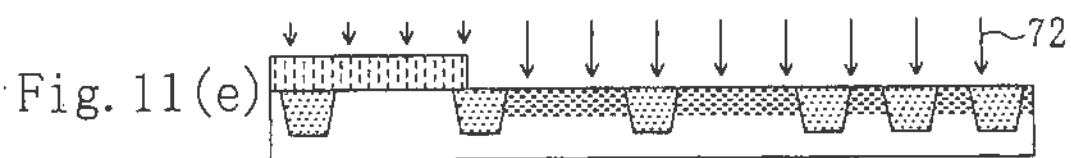
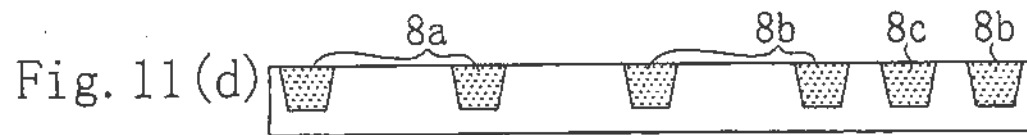
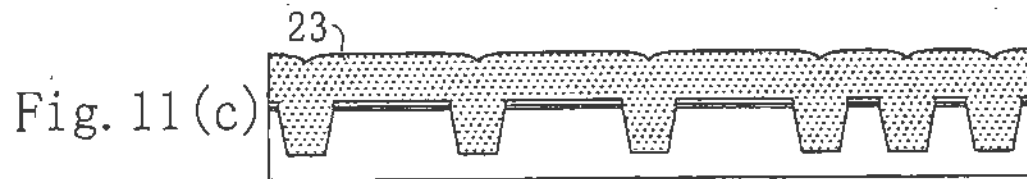
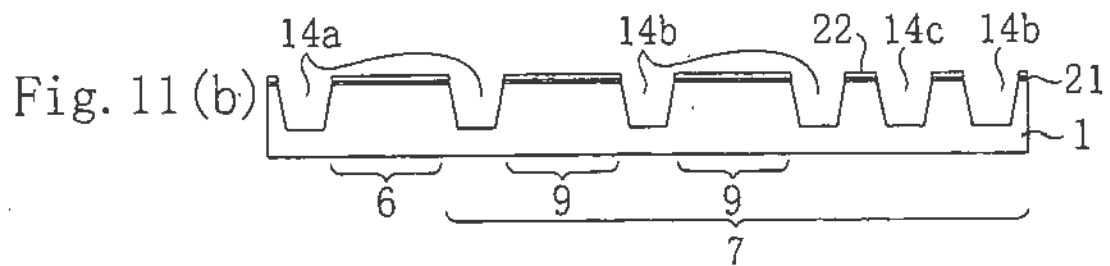
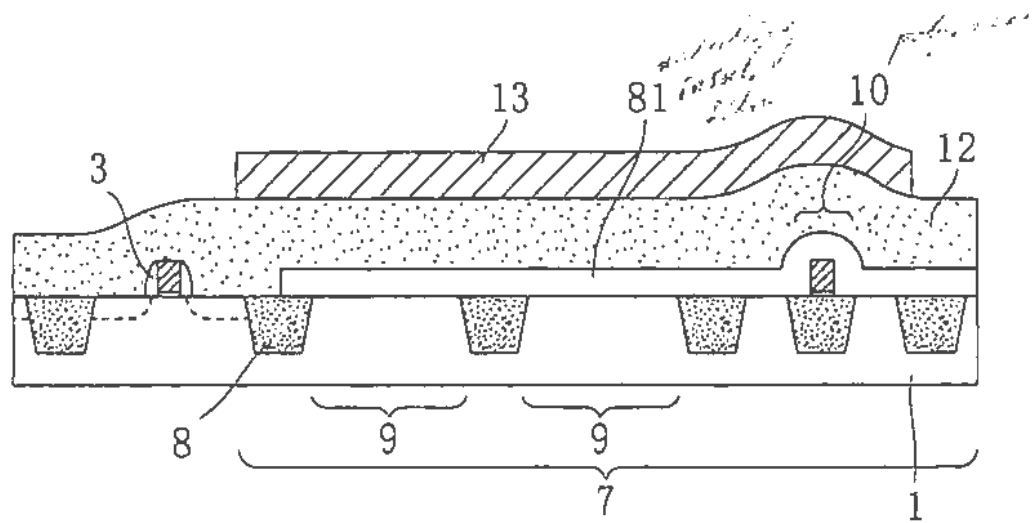
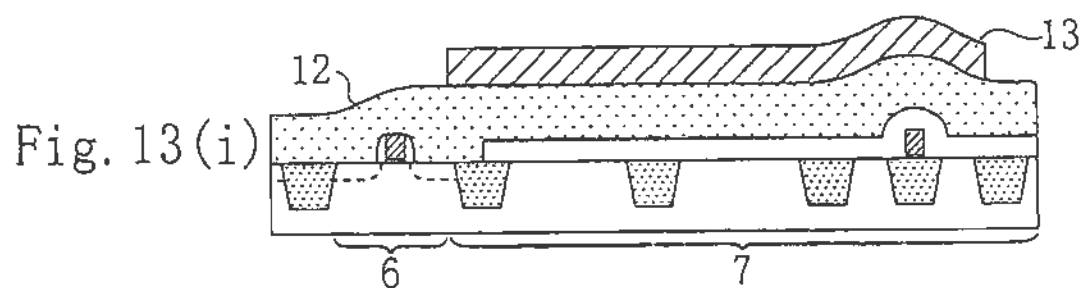
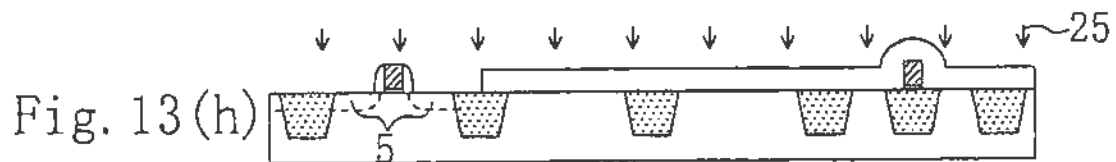
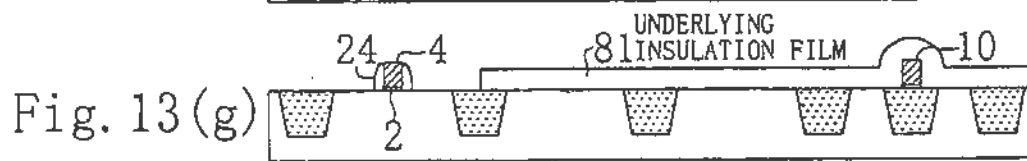
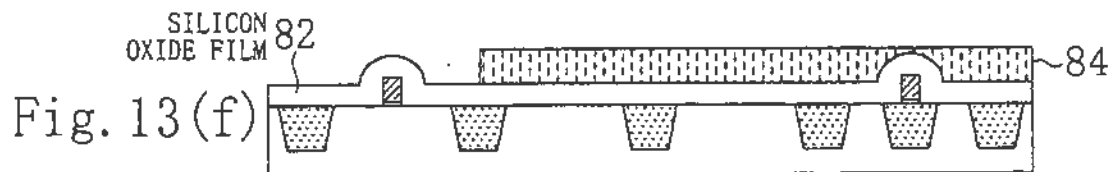
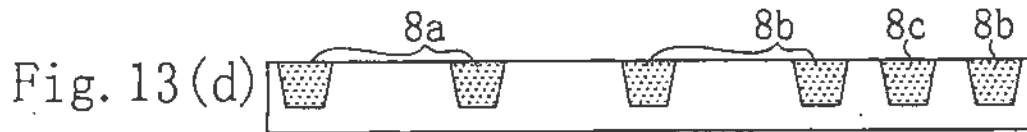
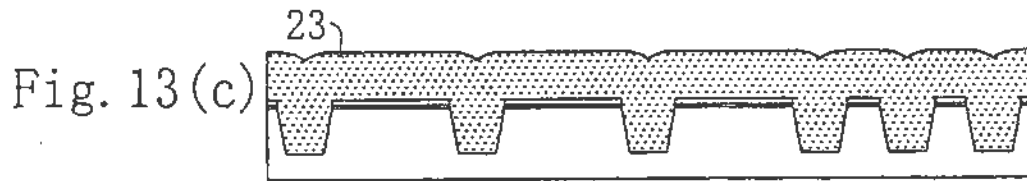
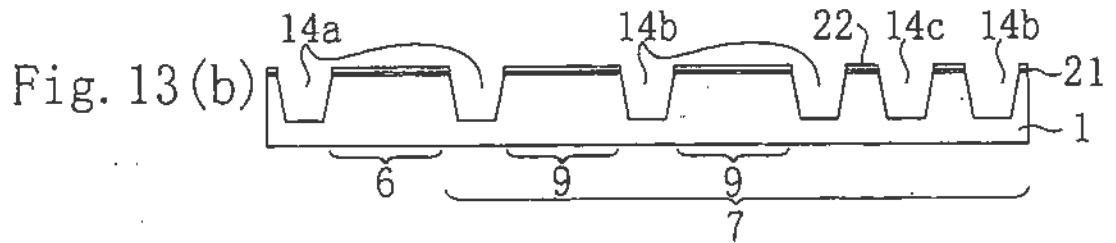


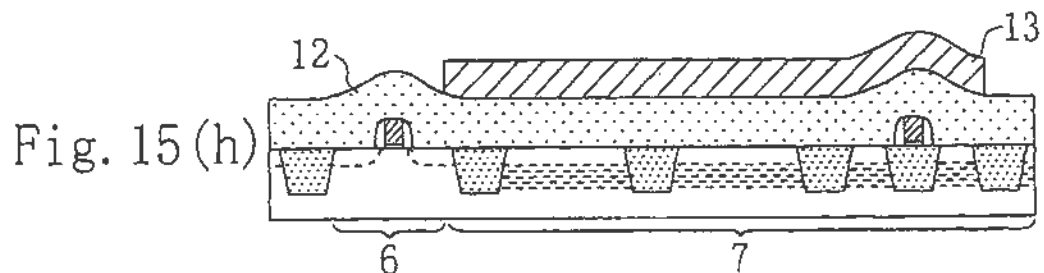
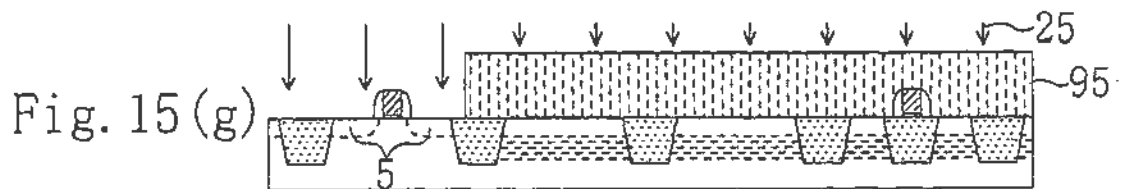
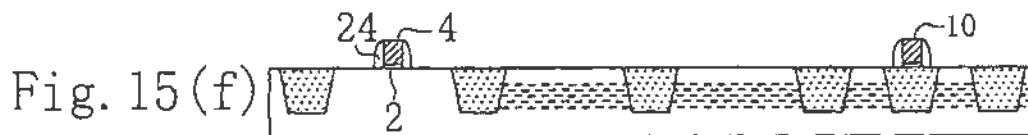
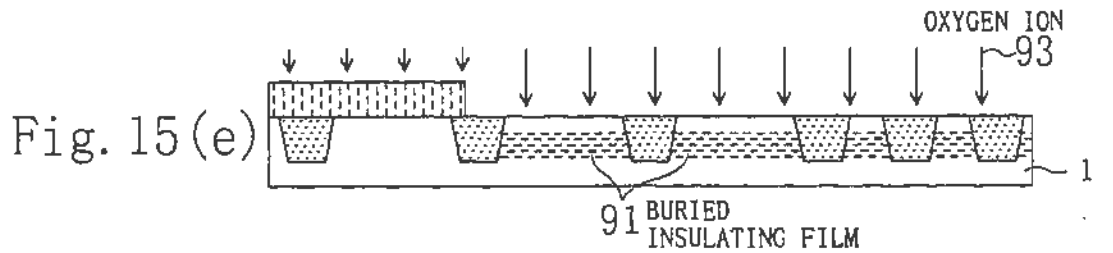
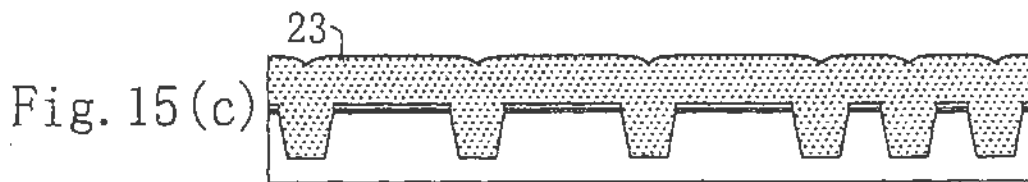
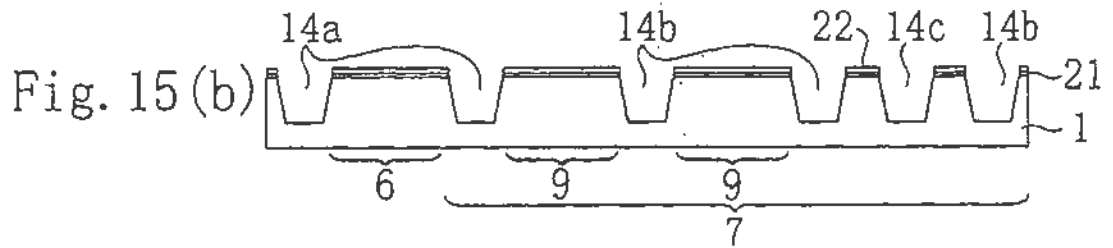
Fig. 12



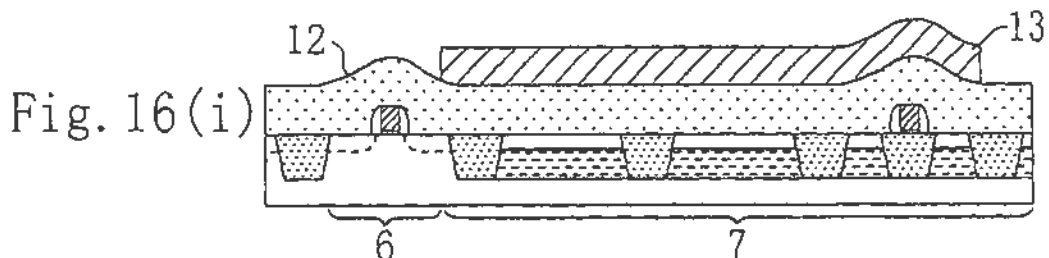
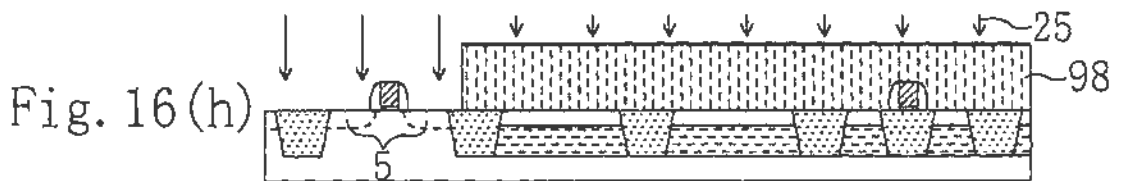
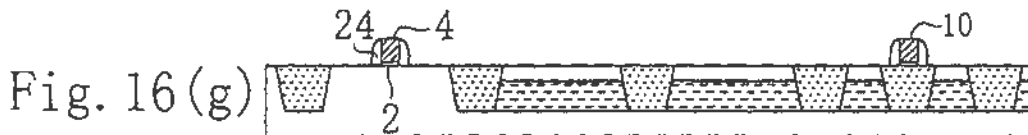
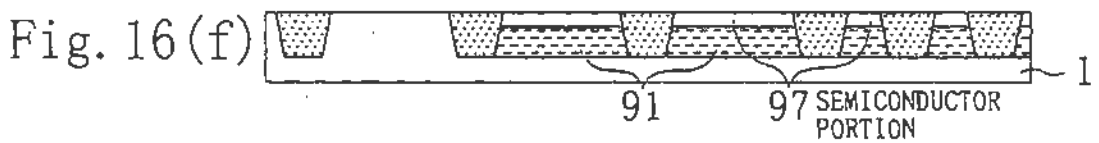
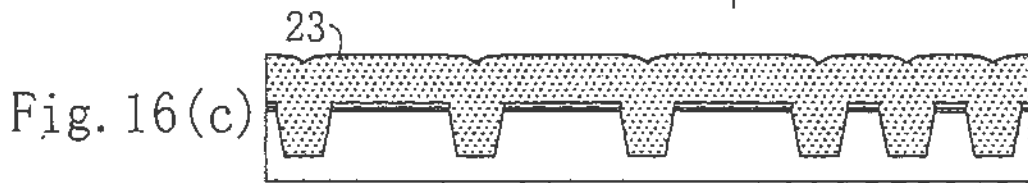
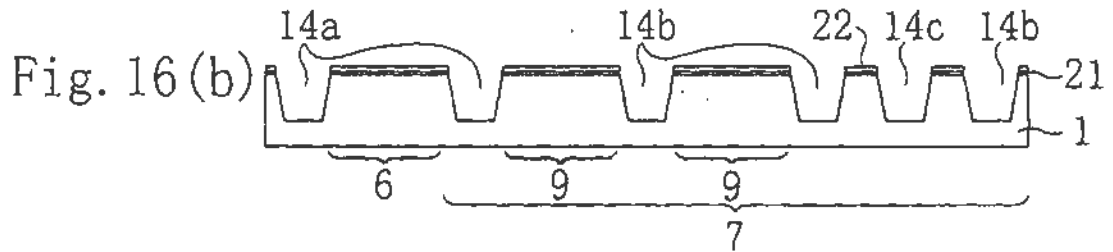
2/8/81 from Mrs. G. J. J. J.



9th Embod.



10th Embodiment



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3. *Conclusions*

102 TRENCH

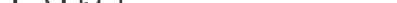
Fig. 17(a)  1

Fig. 17(b)

Fig. 17(c)

103 SILICON FILM

BURIED INSULATING FILM 101

1

Detailed description: This diagram shows a cross-section of a semiconductor device. A thick layer of silicon film, labeled 103, is positioned on top of a buried insulating film, labeled 101. The buried insulating film is shown with a hatched pattern. Below the buried insulating film is a substrate, labeled 1. A dashed line indicates the interface between the silicon film and the buried insulating film.

Fig. 17(d)


103 22 21 1

Fig. 17(e)

14a 101 14b 22 14c 14b 21 1

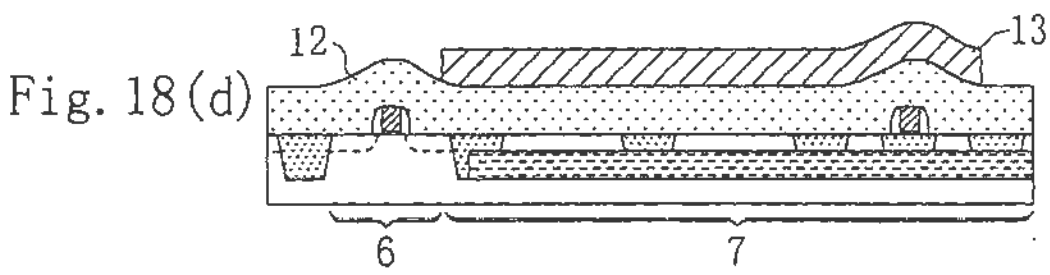
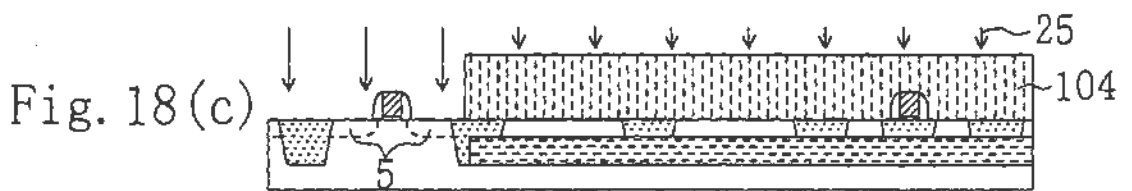
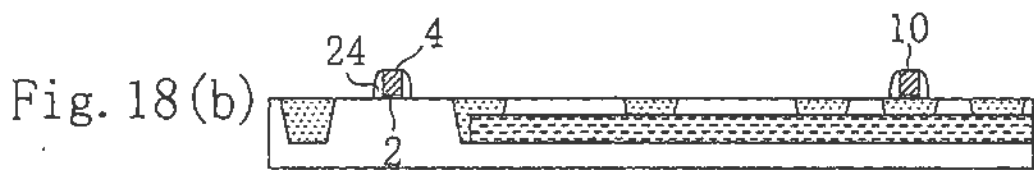
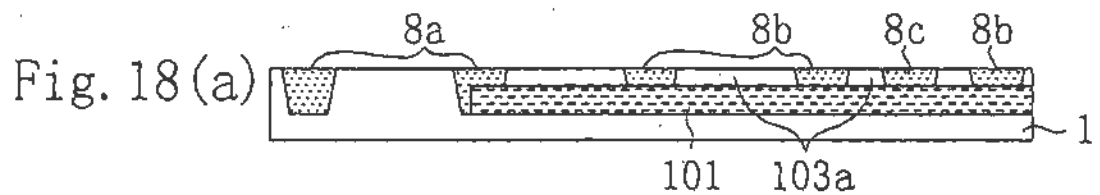
6 9 9 7

Fig. 17(f)



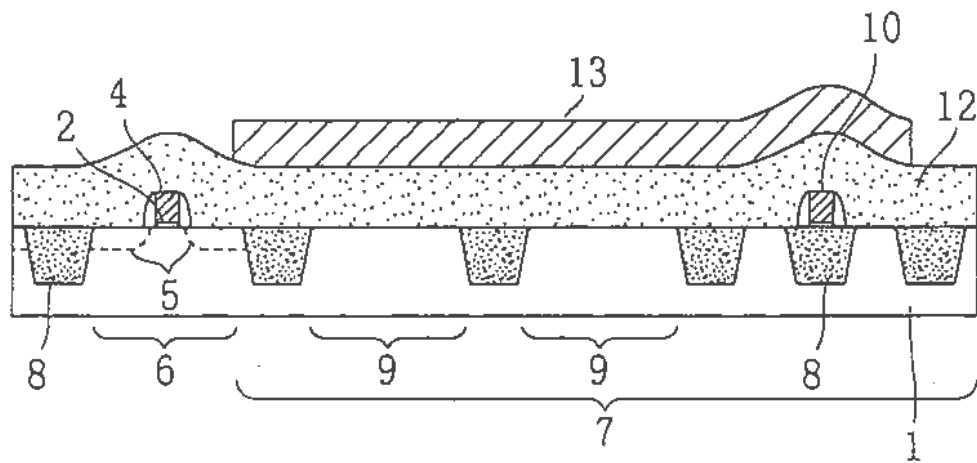
A cross-sectional view of a semiconductor device. A top layer, labeled 23, is shown with a wavy, irregular surface. Below this layer is a substrate with several rectangular openings. The openings are filled with a material, and the top layer 23 is positioned above these openings.

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Fig. 19
PRIOR ART



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Fig. 20(a)
PRIOR ART



Fig. 20(b)
PRIOR ART

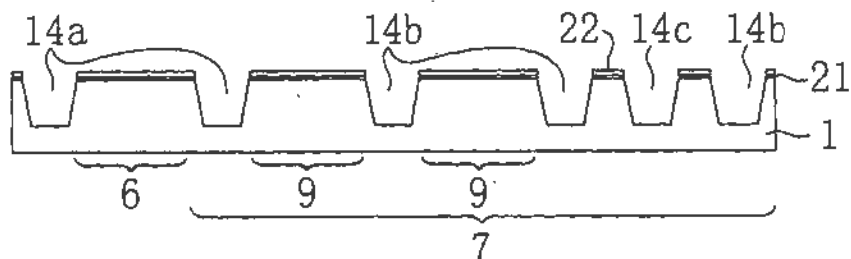


Fig. 20(c)
PRIOR ART

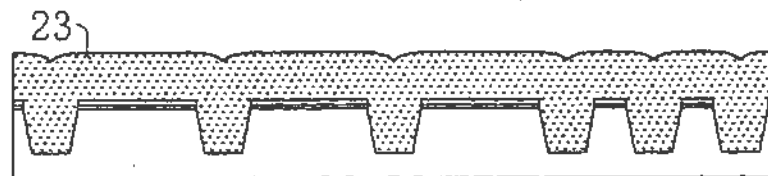


Fig. 20(d)
PRIOR ART

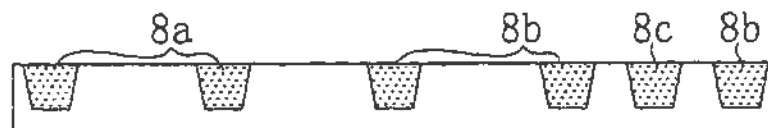


Fig. 20(e)
PRIOR ART



Fig. 20(f)
PRIOR ART

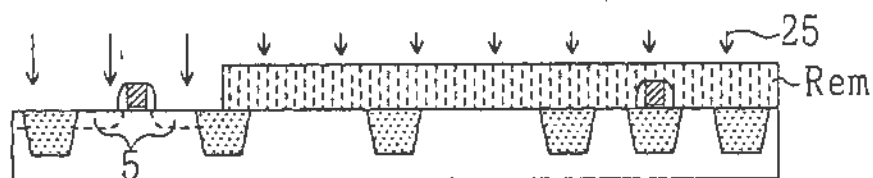
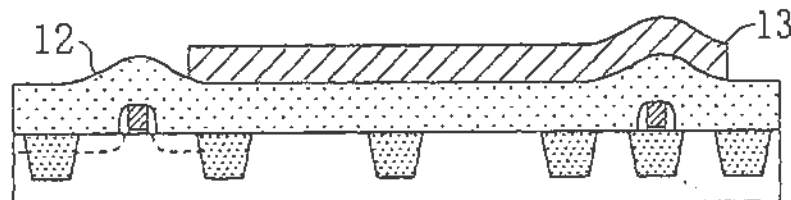


Fig. 20(g)
PRIOR ART



405217-2 FEB 2000

Fig. 21(a)
PRIOR ART

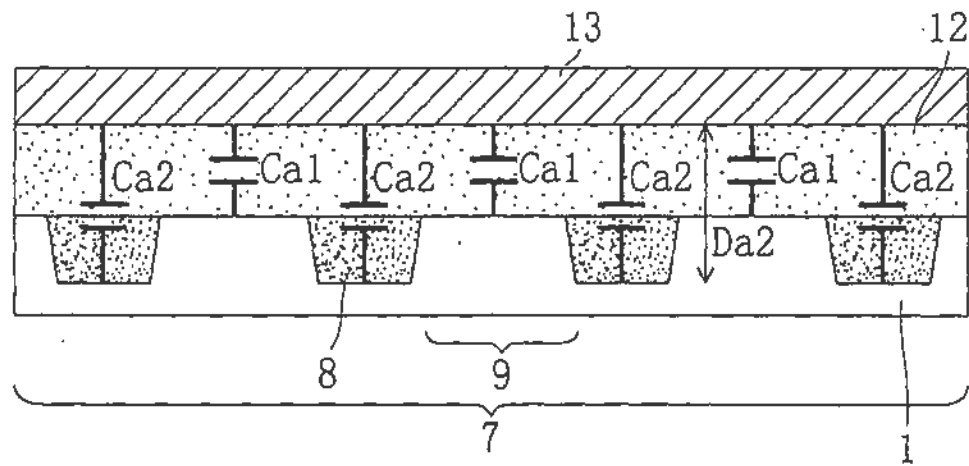
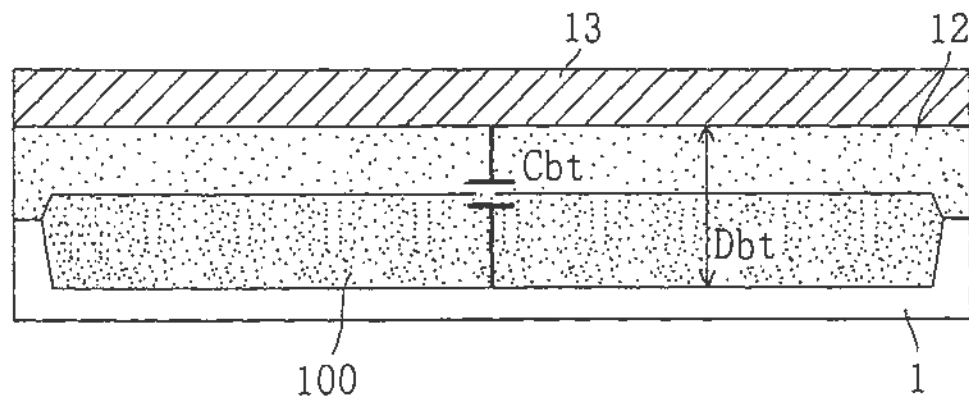


Fig. 21(b)
PRIOR ART



COMBINED DECLARATION/POWER OF ATTORNEY
FOR PATENT APPLICATION

As a below named inventor, I hereby declare that: ✓

My residence, post office address and citizenship are as stated below next to my name. ✓

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

_____, the specification of which

(check one) ☒ is attached hereto.

_____ was filed on _____ as
Application Serial No. _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. ✓

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a). ✓

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed: ✓

Prior Foreign Application(s)			Priority Claimed
<u>8-314762</u> (Number)	<u>JAPAN</u> (Country)	<u>26/11/1996</u> (Day/Month/Year Filed)	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
<u>9-023844</u> (Number)	<u>JAPAN</u> (Country)	<u>06/02/1997</u> (Day/Month/Year Filed)	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/> Yes <input type="checkbox"/> No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application: ✓

08978127-112597

(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)
(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)

I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Raphael V. Lupo (Reg. No. 28,363); Jack Q. Lever, Jr. (Reg. No. 28,149); Kenneth L. Cage (Reg. No. 26,151); Stanislaus Aksman (Reg. No. 28,562); Paul Devinsky (Reg. No. 28,553); Edward E. Kubasiewicz (Reg. No. 30,020), Michael E. Fogarty (Reg. No. 36,139); Brian E. Ferguson (Reg. No. 36,801); Robert W. Zelnick (Reg. No. 36,976); and Wilhlem F. Gadiano (Reg. No. 37,136).

Please address all correspondence and telephone calls to:

Kenneth L. Cage, Esquire
McDERMOTT, WILL & EMERY
1850 K STREET, N.W., SUITE 500
WASHINGTON, D.C. 20006
(202) 778-8300

PAYOR NO.
020277

The undersigned hereby authorizes the U.S. attorneys named herein to accept and follow instructions from Maeda Patent Office as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by the undersigned.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Takaaki UKEDA

Inventor's signature Takaaki Ukeda Date Nov. 18, 1997

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Post Office Address 6-2-205, Myokenzaka, Katano-shi, Osaka 576, Japan

Full name of second inventor Chiaki KUDO

Inventor's signature Chiaki Kudo Date Nov. 18, 1997

Residence* Kyoto, Japan Citizenship Japan

Post Office Address 108-D-504, Uji-hanpaku, Uji-shi, Kyoto 614, Japan

Full name of third inventor Toshiki YABU

Inventor's signature Toshiki Yabu Date Nov. 18, 1997

Residence* Osaka, Japan Citizenship Japan

Post Office Address 4-14-1, Nagaodai, Hirakata-shi, Osaka 573-01, Japan

* City and State, or City and Country for foreign inventors

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46500000 22184000

Application Assignment Record

According to the application transmittal letter, an assignment recording ownership was filed with this application; however, a copy of this record was not located in the original file history record obtained from the United States Patent and Trademark Office. Upon your request, we will attempt to obtain the assignment documents from the Assignment Recordation Branch of the United States Patent and Trademark Office or from a related application case (if applicable). Please note that additional charges will apply for this service.

ATTORNEY DOCKET NO. 43889-677

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE:

Takaaki UKEDA, et al.

SERIAL NO.

08/978,137

08/978,137

FILING DATE

25 November 1997

FOR: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE
SAME

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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

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In accordance with the provisions of 37 C.F.R. § 1.55, Applicants submit
herewith a certified copy of each of the following foreign application(s)

Japanese Patent Application No. 8-314762

Filed: 26 November 1996

Japanese Patent Application No. 9-023844

Filed: 06 February 1997

It is respectfully requested that Applicants be given benefit of the foreign filing
date, as evidenced by the certified papers attached hereto, in accordance with the
requirements of 35 U.S.C. § 119.

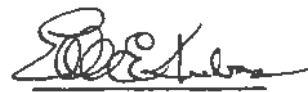
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duplicate copy of this communication is enclosed for accounting purposes.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 06 January 1998

By:



Edward E. Kubasiewicz
Registration No. 30,020

600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE: Takaaki UKEDA, et al.

SERIAL NO.: 08/978,137

FILING DATE: 25 November 1997

FOR: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE
SAME

**SUBMISSION OF CERTIFIED COPY(IES) OF PRIOR FOREIGN
APPLICATION(S) UNDER 37 C.F.R. § 1.55**

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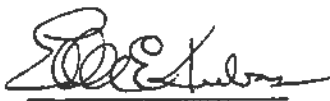
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with this communication or credit any overpayment to Deposit Account No. 13-0203. A
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Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 06 January 1998

By: 
Edward E. Kubasiewicz
Registration No. 30,020

600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

日本国特許庁

PATENT OFFICE
JAPANESE GOVERNMENT

別紙添付の書類に記載されている事項は下記の出願書類に記載されて
る事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed
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願年月日
Date of Application:

1996年11月26日

願番号
Application Number:

平成 8 年特許願第 3 1 4 7 6 2 号 GROUP 2500

願人
Applicant(s):

松下電器産業株式会社

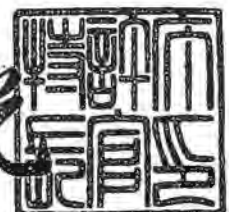
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特許庁長官
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Patent Office

荒井寿光



出証番号 出証特平09-3093004

【書類名】 特許願

【整理番号】 2020280487

【提出日】 平成 8年11月26日

【あて先】 特許庁長官 殿

【国際特許分類】 H01L 21/76

【発明の名称】 半導体装置

【請求項の数】 17

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 【弁理士】

 【氏名又は名称】 前田 弘

【選任した代理人】

 【識別番号】 100094134

【弁理士】

【氏名又は名称】 小山 廣毅

【選任した代理人】

【識別番号】 100107445

【弁理士】

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【予納台帳番号】 014409

【納付金額】 21,000円

【提出物件の目録】

【物件名】 明細書 1

【物件名】 図面 1

【物件名】 要約書 1

【包括委任状番号】 9601026

【プルーフの要否】 要

【書類名】 明細書

【発明の名称】 半導体装置

【特許請求の範囲】

【請求項1】 半導体基板上に形成され素子が配置される活性領域と、
上記活性領域を取り囲む素子分離領域と、
上記素子分離領域に形成され絶縁性材料が埋め込まれた複数の溝部と、
上記素子分離領域の上記各溝部の間に介在する半導体部と、
上記活性領域及び素子分離領域に亘る領域上に形成された層間絶縁膜と、
上記層間絶縁膜の上に形成された配線とを備えているとともに、
上記配線下方の上記半導体部に形成された少なくとも1つのPN接合部を備えていることを特徴とする半導体装置。

【請求項2】 請求項1記載の半導体装置において、
上記PN接合部は、上記半導体部に複数個形成されていることを特徴とする半導体装置。

【請求項3】 半導体基板上に形成され素子が配置される活性領域と、
上記活性領域を取り囲む素子分離領域と、
上記素子分離領域に形成され絶縁性材料が埋め込まれた複数の溝部と、
上記素子分離領域の上記各溝部の間に介在する半導体部と、
上記活性領域及び素子分離領域に亘る領域上に形成された層間絶縁膜と、
上記層間絶縁膜の上に形成された配線とを備えているとともに、
上記素子分離領域のうち少なくとも上記半導体部と上記層間絶縁膜との間に介設された誘電体膜を備えていることを特徴とする半導体装置。

【請求項4】 請求項3記載の半導体装置において、
上記誘電体膜は、上記半導体部及び溝部と上記層間絶縁膜の間に介在する下敷き絶縁膜であることを特徴とする半導体装置。

【請求項5】 請求項4記載の半導体装置において、
上記素子は、半導体基板上に形成されたゲート電極と、上記ゲート電極の両側面上に形成された絶縁性材料からなるサイドウォールとを有しており、
上記下敷き絶縁膜は、上記素子のサイドウォールと共通の膜から形成されてい

ることを特徴とする半導体装置。

【請求項6】 請求項5記載の半導体装置において、

上記下敷き絶縁膜は、積層膜により構成されていることを特徴とする半導体装置。

【請求項7】 請求項3記載の半導体装置において、

上記誘電体膜は、上記半導体部の上に形成され上記溝部と同じ上面位置を有する埋め込み絶縁膜であることを特徴とする半導体装置。

【請求項8】 請求項3, 4, 5, 6又は7記載の半導体装置において、

上記誘電体膜は、酸化珪素膜及び窒化珪素膜のうち少なくともいずれか一方により構成されていることを特徴とする半導体装置。

【請求項9】 半導体基板上に形成され素子が配置される活性領域と、

上記活性領域を取り囲む素子分離領域と、

上記素子分離領域に形成され絶縁性材料が埋め込まれた複数の溝部と、

上記素子分離領域の上記各溝部の間に介在する半導体部と、

上記活性領域及び素子分離領域に亘る領域上に形成された層間絶縁膜と、

上記層間絶縁膜の上に形成された配線とを備えているとともに、

上記素子分離領域のうち少なくとも1つの上記半導体部の奥方に形成された埋め込み絶縁膜を備えていることを特徴とする半導体装置。

【請求項10】 半導体基板上に形成され素子が配置される活性領域と、

上記活性領域を取り囲む素子分離領域と、

上記素子分離領域に形成され絶縁性材料が埋め込まれた複数の溝部と、

上記素子分離領域の上記各溝部の間に介在する半導体部と、

上記活性領域及び素子分離領域に亘る領域上に形成された層間絶縁膜と、

上記層間絶縁膜の上に形成された配線とを備えているとともに、

上記素子分離領域のうち少なくとも上記半導体部と上記層間絶縁膜との間に形成された抵抗体膜を備えていることを特徴とする半導体装置。

【請求項11】 請求項10記載の半導体装置において、

上記抵抗体膜は、上記半導体部と溝部とに亘る領域の上に形成された下敷き抵抗体膜であることを特徴とする半導体装置。

【請求項12】 請求項11記載の半導体装置において、
上記半導体基板上に形成され高抵抗膜を有する抵抗素子をさらに備え、
上記下敷き抵抗膜は、上記抵抗素子の高抵抗膜と同じ膜から形成されている
ことを特徴とする半導体装置。

【請求項13】 請求項11記載の半導体装置において、
上記素子は、半導体基板上に形成された導電膜からなるゲート電極を有してお
り、
上記抵抗膜は、上記ゲート電極と共通の膜から形成されていることを特徴と
する半導体装置。

【請求項14】 請求項11記載の半導体装置において、
上記素子は、半導体基板上に形成された第1の導電膜と該第1の導電膜の上に
堆積された第2の導電膜により構成されるゲート電極を有しており、
上記ゲート電極の第1の導電膜の上面と上記溝部の上面とがほぼ同じ高さ位置
にあり、

上記抵抗膜のうち上記半導体部の上方にある領域は、上記ゲート電極の上記
第1及び第2の導電膜と共通の2つの膜から形成されており、

上記抵抗膜のうち上記溝部の上方にある領域は、上記ゲート電極の上記第1
の導電膜と共通の膜から形成されていることを特徴とする半導体装置。

【請求項15】 請求項10記載の半導体装置において、
上記抵抗膜は、上記半導体部の上に形成され上記溝部とほぼ同じ上面位置を
有する埋め込み抵抗膜であることを特徴とする半導体装置。

【請求項16】 請求項15記載の半導体装置において、
上記埋め込み抵抗膜は、酸素原子及び窒素原子のうちいずれか一方を含んだ
シリコン膜により構成されていることを特徴とする半導体装置。

【請求項17】 請求項10、11、12、13、14又は15記載の半導
体装置において、

上記抵抗膜は、多結晶シリコン膜及び非晶質シリコン膜のうち少なくともい
ずれか一方により構成されていることを特徴とする半導体装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】

本発明は、トレンチ分離構造を有する半導体装置に係り、特に配線-基板間容量の低減対策に関する。

【0002】

【従来の技術】

近年、半導体装置の高密度化・微細化に伴い、半導体装置内の各素子間を分離絶縁するための素子分離を形成する技術として、現在最も一般的に用いられているLOCOSの代わりに、半導体基板に溝を形成し、この溝に絶縁性材料を埋め込んで素子分離とするトレンチ分離技術の導入が試みられている。

【0003】

このトレンチ分離技術においては、半導体基板及び絶縁材料が埋め込まれた溝部の表面を均一に平坦化することが重要であるので、近年、面内均一性に優れたパターン依存性の無い平坦化技術として化学機械研磨法（CMP法）の導入が試みられている。さらに、CMP法による平坦化を行う工程では、平坦化される領域の面積などに依存して研磨特性が変化するいわゆるパターン依存性による不具合を回避するために、溝部の面積が広くなるような場合には、素子分離領域に予めダミーの島状の半導体部を設けることが提案されている。つまり、溝部を複数の細い溝に分割して各溝間に半導体基板表面を露出させて活性領域としては機能しないダミーの半導体部を設けるのである。

【0004】

図10は、従来提案されている島状のダミーの半導体部を有するトレンチ分離型半導体装置の一例を示す。

【0005】

図10に示すように、P型シリコン基板1の活性領域6には、ゲート酸化膜2と、多結晶シリコン膜からなるゲート電極4と、不純物が導入されたソース・ドレイン5とが形成されている。また、活性領域6を取り囲む素子分離領域7には、酸化珪素膜が埋め込まれた複数の溝部8が形成されており、各溝部8の間には

、溝部3の上面と同じ上面位置を有する半導体部9が設けられている。なお、素子分離領域7内の溝部8にも素子のゲート酸化膜2及びゲート電極4と同時に形成された多結晶シリコン配線10が設けられている。また、基板の全面上には層間絶縁膜12が堆積されていて、この層間絶縁膜12の上にメタル配線13が設けられている。

【0006】

すなわち、例えば図11(b)に示すような広い溝部を形成すると、溝部に酸化珪素膜を埋め込んだ後、CMP法により基板全体を平坦化する際に、パターン依存性のため溝部に埋め込まれた酸化珪素膜が凹状に研磨されて平坦度が悪化する等の不具合が生じる。図10に示すような素子分離構造は、斯かるパターン依存性に起因する不具合を防止するべく提案されているものである。

【0007】

【発明が解決しようとする課題】

ところで、図10に示す半導体装置を形成する際に、活性領域6内のゲート電極4やソース・ドレイン5等には燐、硼素などの不純物イオンが注入される。しかし、活性領域6以外の領域では、マスクの合わせズレを考慮して素子分離領域まで若干拡大して導入されることはあっても、原則として不純物イオンの注入は行われない。したがって、各溝部8間のダミーの半導体部9には不純物イオンは注入されない。

【0008】

ここで、図10に示すような細分割された溝部8及びダミーの半導体部9とを有するトレンチ分離型半導体装置と、広い分離絶縁膜例えばLOCOS膜を有する半導体装置とにおける配線-基板間容量について説明する。図11(a)は、一例としてダミーの半導体部9を有する素子分離領域7の配線-基板間容量を説明するための断面図である。また、図11(b)は、ダミーの半導体部を設けていないLOCOS分離膜100を有する半導体装置の配線-基板間容量を説明するための断面図である。ただし、図11(a)、(b)とも、ソース・ドレイン注入時に素子分離領域7には不純物イオンが注入されておらず、かつ素子分離領域7全体の面積は等しいと仮定する。

【0009】

図11(a)に示す半導体装置においては、全配線-基板間容量 C_{at} は容量 C_{a1} と C_{a2} の総和として表される。つまり、下記式(1)

$$C_{at} = \Sigma C_{a1} + \Sigma C_{a2} \quad (1)$$

により表される。ところで、配線-基板間の単位面積当たりの容量は、両者間に存在する部材が均質な材料により構成されている場合には、配線-基板間の距離に反比例し、距離が短いほど容量は大きくなる。そのため、図11(a)に示す寸法 D_{a2} と図11(b)に示す寸法 D_{bt} が等しい場合、図11(b)に示す半導体装置における配線-基板間の全容量を C_{bt} とすると、

$$C_{at} > C_{bt} \quad (2)$$

なる関係が成立する。つまり、図11(a)に示す構造における配線-基板間の容量 C_{at} は、図11(b)に示す構造における配線-基板間の容量 C_{bt} よりも大きくなってしまふ。

【0010】

このように、素子分離領域にダミーの半導体部からなる島状パターンを形成すると、面内均一性のよい平坦化を行うことができるという利点はあるものの、反面、配線-基板間容量が増大し、その結果、半導体装置の動作速度が低下するおそれがあった。

【0011】

本発明は係る点に着目してなされたものであり、一般的に、平行平板キャパシターにおいて、電極面積が等しければ電極間距離が長いほどキャパシターの容量は小さくなるという原理、或いは同じキャパシター容量でも電極間電圧が低ければ蓄積電荷量は少ないという物理現象に着目して創案したものである。

【0012】

すなわち、本発明の第1の目的は、溝部とダミーの半導体部とからなる素子分離領域を備えたトレンチ分離型半導体装置において、素子分離領域内における配線-基板間容量を低減しうる手段を講ずることにより、動作速度の向上を図ることにある。

【0013】

本発明の第2の目的は、溝部とダミーの半導体部とからなる素子分離領域を備えたトレンチ分離型半導体装置において、素子分離領域内における配線-基板間に存在する容量に蓄積される電荷量を低減しうる手段を講ずることにより、動作速度の向上を図ることにある。

【0014】

【課題を解決するための手段】

上記第1の目的を達成するために、本発明では、請求項1～2に記載されている第1の半導体装置に関する手段と、請求項3～8に記載されている第2の半導体装置に関する手段と、請求項9に記載されている第3の半導体装置に関する手段とを講じている。

【0015】

本発明の第1の半導体装置は、請求項1に記載されているように、半導体基板上に形成され素子が配置される活性領域と、上記活性領域を取り囲む素子分離領域と、上記素子分離領域に形成され絶縁性材料が埋め込まれた複数の溝部と、上記素子分離領域の上記各溝部の間に介在する半導体部と、上記活性領域及び素子分離領域に亘る領域上に形成された層間絶縁膜と、上記層間絶縁膜の上に形成された配線とを備えているとともに、上記配線下方の上記半導体部に形成された少なくとも1つのPN接合部を備えている。

【0016】

これにより、配線-基板間容量のうち素子分離領域の半導体部を通る領域における容量成分は、層間絶縁膜による容量に対して、半導体部のうちPN接合部の上方の部分の容量を直列で付加したものになり、層間絶縁膜のみによる容量よりも小さくなる。したがって、半導体装置全体の配線-基板間容量も低減し、半導体装置の動作速度が向上することになる。

【0017】

請求項2に記載されているように、請求項1において、上記PN接合部を上記半導体部に複数個設けることができる。

【0018】

これにより、さらに配線-基板間容量のいっそうの低減が可能になるので、動作速度もさらに速くなる。

【0019】

本発明の第2の半導体装置は、請求項3に記載されているように、半導体基板上に形成され素子が配置される活性領域と、上記活性領域を取り囲む素子分離領域と、上記素子分離領域に形成され絶縁性材料が埋め込まれた複数の溝部と、上記素子分離領域の上記各溝部の間に介在する半導体部と、上記活性領域及び素子分離領域に亘る領域上に形成された層間絶縁膜と、上記層間絶縁膜の上に形成された配線とを備えているとともに、上記素子分離領域のうち少なくとも上記半導体部と上記層間絶縁膜の間に介設された誘電体膜を備えている。

【0020】

これにより、配線-基板間容量のうち素子分離領域の半導体部を通る領域における容量成分は、層間絶縁膜の容量に対して誘電体膜の容量が直列に付加された容量となるので、全体としての配線-基板間容量を低減することができる。したがって、半導体装置の動作速度が向上する。

【0021】

請求項4に記載されているように、請求項3において、上記誘電体膜として、上記半導体部及び溝部と上記層間絶縁膜との間に介在する下敷き絶縁膜を設けることができる。

【0022】

これにより、請求項3の作用効果を有効に得ることができる。

【0023】

請求項5に記載されているように、請求項4において、上記素子に、半導体基板上に形成されたゲート電極と、上記ゲート電極の両側面上に形成された絶縁性材料からなるサイドウォールとを設け、上記下敷き絶縁膜を上記素子のサイドウォールと共通の膜から形成することができる。

【0024】

この下敷き絶縁膜は、請求項6に記載されているように、積層膜により構成す

ることができる。

【0025】

請求項5又は6により、いわゆるLDD構造のMOSFETを形成するために必要となるサイドウォールを利用して、配線-基板間容量を低減するための下敷き絶縁膜を形成することができるので、製造コストの増大を回避しながら、請求項3の作用効果を得ることができる。

【0026】

請求項7に記載されているように、請求項3において、上記誘電体膜として、上記半導体部の上に形成され上記溝部と同じ上面位置を有する埋め込み絶縁膜を設けることができる。

【0027】

これによっても、請求項3の作用効果を有効に得ることができる。

【0028】

請求項8に記載されているように、請求項3、4、5、6又は7において、上記誘電体膜を、酸化珪素膜及び窒化珪素膜のうち少なくともいずれか一方により構成することが好ましい。

【0029】

本発明の第3の半導体装置は、請求項9に記載されているように、半導体基板上に形成され素子が配置される活性領域と、上記活性領域を取り囲む素子分離領域と、上記素子分離領域に形成され絶縁性材料が埋め込まれた複数の溝部と、上記素子分離領域の上記各溝部の間に介在する半導体部と、上記活性領域及び素子分離領域に亘る領域上に形成された層間絶縁膜と、上記層間絶縁膜の上に形成された配線とを備えているとともに、上記素子分離領域のうち少なくとも1つの上記半導体部の奥方に形成された埋め込み絶縁膜を備えている。

【0030】

これにより、素子分離領域全体の配線-基板間容量を低減することが可能となり、動作速度を大幅に低減することが可能となる。

【0031】

上記第2の目的を達成するために、本発明では、請求項10～17に記載され

ている第4の半導体装置に関する手段を講じている。

【0032】

本発明の第4の半導体装置は、請求項10に記載されているように、半導体基板上に形成され素子が配置される活性領域と、上記活性領域を取り囲む素子分離領域と、上記素子分離領域に形成され絶縁性材料が埋め込まれた複数の溝部と、上記素子分離領域の上記各溝部の間に介在する半導体部と、上記活性領域及び素子分離領域に亘る領域上に形成された層間絶縁膜と、上記層間絶縁膜の上に形成された配線とを備えているとともに、少なくとも上記半導体部と上記層間絶縁膜の間に介在する抵抗体膜を備えている。

【0033】

これにより、半導体装置の抵抗体膜を通る部分において、配線-基板間容量は小さくならなくても、抵抗体膜における電圧降下により、配線-基板間容量に蓄積される電荷量が低減する。したがって、電荷の充放電に要する時間が短くなり、半導体装置の動作速度が速くなる。

【0034】

請求項11に記載されているように、請求項10において、上記抵抗体膜として、上記半導体部と溝部とに亘る領域の上に形成された下敷き抵抗体膜を設けることができる。

【0035】

これにより、半導体基板上に形成される抵抗性を有する各種の膜を利用して、請求項10の作用効果を得ることが可能になる。

【0036】

請求項12に記載されているように、請求項11において、上記半導体基板上に形成され高抵抗膜を有する抵抗素子をさらに備え、上記下敷き抵抗体膜を、上記抵抗素子の高抵抗膜と同じ膜から形成することができる。

【0037】

これにより、抵抗素子に用いられる高抵抗膜と同じ抵抗を有する下敷き抵抗体膜によって、請求項10の電圧降下作用が顕著に得られる。

【0038】

請求項13に記載されているように、請求項11において、上記素子に半導体基板上に形成された導電膜からなるゲート電極を設け、上記抵抗体膜を上記ゲート電極と共通の膜から形成することができる。

【0039】

請求項14に記載されているように、請求項11において、上記素子に半導体基板上に形成された第1の導電膜と該第1の導電膜の上に堆積された第2の導電膜により構成されるゲート電極を設け、上記ゲート電極の第1の導電膜の上面と上記溝部の上面とをほぼ同じ高さ位置になるようにしておき、上記抵抗体膜のうち上記半導体部の上方にある領域を上記ゲート電極の上記第1及び第2の導電膜と共通の2つの膜から形成し、上記抵抗体膜のうち上記溝部の上方にある領域を上記ゲート電極の上記第1の導電膜と共通の膜から形成することができる。

【0040】

請求項13又は14により、別途抵抗体膜を形成するための工程が不要となるので、製造コストの増大を回避しつつ、請求項10の作用効果を得ることができる。

【0041】

請求項15に記載されているように、請求項10において、上記抵抗体膜として、上記半導体部の上に形成され上記溝部とほぼ同じ上面位置を有する埋め込み抵抗体部を設けることができる。

【0042】

請求項16に記載されているように、請求項15において、上記埋め込み抵抗体部を、酸素原子及び窒素原子のうちいずれか一方を含んだシリコン膜により構成することができる。

【0043】

請求項15又は16によっても、請求項10の作用効果を有効に得ることができる。

【0044】

請求項17に記載されているように、請求項10、11、12、13、14又

は15において、上記抵抗膜を、多結晶シリコン膜及び非晶質シリコン膜のうち少なくともいずれか一方により構成することができる。

【0045】

これにより、ゲート電極や抵抗素子を構成するために使用される多結晶シリコン膜や非晶質シリコン膜を利用して抵抗膜を形成できるので、製造コストの増大を回避しながら、請求項10の作用効果を得ることができる。

【0046】

【発明の実施の形態】

以下、本発明の実施の形態を図面を参照しながら説明する。

【0047】

(第1の実施形態)

図1(a)は、第1の実施形態にかかる半導体装置の断面図である。

【0048】

同図に示すように、P型シリコン基板1の活性領域6には、ゲート酸化膜2と、多結晶シリコン膜からなるゲート電極4と、ソース・ドレイン5とにより構成されるMOSFETとして機能する素子が設けられている。また、各素子を電氣的に分離するための素子分離領域7には、絶縁性材料である酸化珪素膜が埋め込まれた複数の溝部8と、各溝部8の間に設けられ活性領域としては機能しないダミーの半導体部9が存在する。また、素子分離領域7の1つの溝部8の上には、ゲート絶縁膜2及びゲート電極4と同時に形成された多結晶シリコン配線10が存在している。さらに基板の全面上に堆積された酸化珪素膜からなる層間絶縁膜12と、層間絶縁膜12の上に形成されたメタル配線13とを備えている。

【0049】

ここで、素子分離領域7中の半導体部9には、シリコン基板1と逆導電型の不純物であるN型不純物が導入された不純物拡散層21が設けられており、この不純物拡散層21とシリコン基板1との間にPN接合部22が形成されている。このPN接合部22は溝部14の上面と底面との間にある。

【0050】

図1(b)は、本実施形態に係る半導体装置の素子分離領域7における配線一

基板間容量を説明するための断面図である。同図に示すように、本実施形態に係る半導体装置の配線-基板間容量には、図11(a)に示す従来の半導体装置における配線-基板間容量と同様に、容量 C_{a1} と容量 C_{a2} の成分が存在する。さらに、本実施形態では、半導体部9内にPN接合部22が形成されるため、新たな容量 C_{j1} が容量 C_{a1} に対して直列に付加される。よって、全配線-基板間容量 C_{jt} は、下記式(3)

$$C_{jt} = \Sigma \{ (C_{a1} \times C_{j1}) / (C_{a1} + C_{j1}) \} + \Sigma C_{a2} \quad (3)$$

により表され、式(1)で表わされる全容量 C_{at} より小さくなる。すなわち、下記式(4)

$$C_{jt} < C_{at} \quad (4)$$

が成り立つ。

【0051】

したがって、本実施形態の半導体装置によると、素子分離領域7内のダミーの半導体部9内にPN接合部22が存在するために、配線-基板間容量を低減することが可能になり、半導体装置の動作速度の向上を図ることができる。

【0052】

また、本実施形態のごとく、活性領域にMOSFETを設ける場合、半導体部9のPN接合部22は、ソース・ドレイン5を形成する際の不純物イオンの注入によって容易に形成できるので、製造コストの増大を招くこともない。

【0053】

なお、本実施形態ではP型シリコン基板を用いた場合を述べたが、N型シリコン基板を用いる場合は、溝部間の半導体部の上部にP型の不純物を導入することで、N型シリコン基板との間にPN接合部が形成されるので、本実施形態と同様の効果が得られることはいうまでもない。

【0054】

(第2の実施形態)

図2は、第2の実施形態にかかる半導体装置の断面図である。

【0055】

同図に示すように、P型シリコン基板1の活性領域6には、ゲート酸化膜2と

、多結晶シリコン膜からなるゲート電極4と、ソース・ドレイン5とにより構成されるMOSFETとして機能する素子が設けられている。また、各素子を電気的に分離するための素子分離領域7には、絶縁性材料である酸化珪素膜が埋め込まれた複数の溝部8と、各溝部8の間に設けられ活性領域としては機能しないダミーの半導体部9が存在する。また、素子分離領域7の1つの溝部8の上には、ゲート絶縁膜2及びゲート電極4と同時に形成された多結晶シリコン配線10が存在している。さらに基板の全面上に堆積された酸化珪素膜からなる層間絶縁膜12と、層間絶縁膜12の上に形成されたメタル配線13とを備えている。

【0056】

ここで、素子分離領域7中のダミーの半導体部9にはシリコン基板1内の不純物と逆導電型の不純物であるN型不純物が導入された不純物拡散層31が形成されており、この不純物拡散層31とシリコン基板1との間に、PN接合部32が形成されている。このPN接合部32は、溝部8の底面より下方にある。

【0057】

上記実施形態の素子分離領域7における配線-基板間容量は、下記式(5)

$$C_{jt} = \Sigma \{ (C_{a1} \times C_{j1}) / (C_{a1} + C_{j1}) \} + \Sigma \{ (C_{a2} \times C_{k1}) / (C_{a2} + C_{k1}) \} \quad (5)$$

により表され、式(1)で表わされる全容量 C_{at} より小さくなる。ただし、 C_{k1} は溝部8の底面とPN接合部32との間の容量である。すなわち、上記第1の実施形態と同様に、下記式(6)

$$C_{jt} < C_{at} \quad (6)$$

が成立する。

【0058】

したがって、本実施形態の半導体装置においても、上記第1の実施形態と同様に、素子分離領域7内のダミーの半導体部9にPN接合部32が存在するため配線-基板間容量を低減することが可能になり、半導体装置の動作速度の向上を図ることができる。特に、本実施形態では、半導体部9を通る領域だけでなく溝部を通る領域をも含めた素子分離領域全体を通る領域における配線-基板間容量を低減することができるので、動作速度の向上効果は大きい。

【0059】

本実施形態のようなPN接合部32は、MOSFETのソース・ドレインの形成の際における不純物イオンの注入によっては形成が困難であるが、そのかわりに、不純物濃度や注入深さを任意に調整できるので、容量の低減効果を高めることができる。

【0060】

なお、本実施形態ではP型シリコン基板を用いた場合を述べたが、N型シリコン基板を用いてもよく、その場合には、半導体部内にはP型の不純物を導入して不純物拡散層を形成することによって、PN接合部を設けることができ、本実施形態と同様の効果が得られる。

【0061】

(第3の実施形態)

図3は、第3の実施形態にかかる半導体装置の断面図である。

【0062】

同図に示すように、P型シリコン基板1の活性領域6には、ゲート酸化膜2と、多結晶シリコン膜からなるゲート電極4と、ソース・ドレイン5とにより構成されるMOSFETとして機能する素子が設けられている。また、各素子を電気的に分離するための素子分離領域7には、絶縁性材料である酸化珪素膜が埋め込まれた複数の溝部8と、各溝部8の間に設けられ活性領域としては機能しないダミーの半導体部9が存在する。また、素子分離領域7の1つの溝部8の上には、ゲート絶縁膜2及びゲート電極4と同時に形成された多結晶シリコン配線10が存在している。さらに基板の全面上に堆積された酸化珪素膜からなる層間絶縁膜12と、層間絶縁膜12の上に形成されたメタル配線13とを備えている。

【0063】

ここで、素子分離領域7中のダミーの半導体部9内には、シリコン基板表面から順に、P型不純物拡散層41と、N型不純物拡散層42とが存在している。すなわち、P型不純物拡散層41とN型不純物拡散層42との間に第1PN接合部43が形成され、N型不純物拡散層42とP型シリコン基板1の間に第2PN接合部44が形成されている。なお、第1、第2PN接合部43、44は、いず

れも溝部 8 の上面と底面の間にある。

【0064】

ここで、本実施形態に係る半導体装置の全配線-基板間容量 C_{jt} は、P 型不純物層 4 1 の接合容量を C_{j1} 、N 型不純物層 4 2 の接合容量を C_{j2} とすると、下記式 (7)

$$C_{jt} = \Sigma \{ 1 / [(1 / C_{a1}) + (1 / C_{j1}) + (1 / C_{j2})] \} + \Sigma C_{a2} \quad (7)$$

により表され、上述の第 1 の実施形態の半導体装置における式 (1) で表わされる全容量 C_{at} より小さくなる。すなわち、下記式 (8)

$$C_{jt} < C_{at} \quad (8)$$

が成立する。

【0065】

本実施形態では、素子分離領域 7 内のダミーの半導体部 9 に複数の PN 接合部 4 3, 4 4 を設けたので、半導体装置の配線-基板間容量のうち半導体部 9 を通る領域における容量成分が、層間絶縁膜の容量に対して P 型不純物拡散層 4 1 及び N 型不純物拡散層 4 2 の容量を直列に接続してなる容量で表される。したがって、半導体装置の配線-基板間容量を上記第 1 の実施形態よりもさらに低減することが可能となり、半導体装置の動作速度の向上を図ることができる。

【0066】

なお、本実施形態では 2 層の不純物拡散層により 2 つの PN 接合部 4 3, 4 4 を形成した例を述べたが、3 層以上の不純物拡散層により 3 つ以上の PN 接合部を形成した場合も同様に表わせる。例えば、ダミー活性領域 9 に m 個の PN 接合部が形成され、さらに溝部 8 の直下に n 個の PN 接合部が形成されているとすると、全配線-基板間容量 C_{jt} は、下記式 (9)

$$C_{jt} = \Sigma \{ 1 / [(1 / C_{a1}) + \Sigma (1 / C_{jm})] \} + \Sigma \{ 1 / [(1 / C_{a2}) + \Sigma (1 / C_{jn})] \} \quad (9)$$

で表され、式 (1) で表わされる全容量 C_{at} より小さくなる。すなわち、下記式 (10)

$$C_{jt} < C_{at} \quad (10)$$

が成立する。

【0067】

このような構造の場合には、素子分離領域7の半導体部だけでなく溝部を通る領域の容量成分が小さくなるので、配線-基板間容量を大幅に低減することが可能になる。

【0068】

(第4の実施形態)

図4は、第4の実施形態にかかる半導体装置の断面図である。

【0069】

同図に示すように、P型シリコン基板1の活性領域6には、ゲート酸化膜2と、多結晶シリコン膜からなるゲート電極4と、ソース・ドレイン5とにより構成されるMOSFETとして機能する素子が設けられている。また、各素子を電気的に分離するための素子分離領域7には、絶縁性材料である酸化珪素膜が埋め込まれた複数の溝部8と、各溝部8の間に設けられ活性領域としては機能しないダミーの半導体部9が存在する。また、素子分離領域7の1つの溝部8の上には、ゲート絶縁膜2及びゲート絶縁膜2及びゲート電極4と同時に形成された多結晶シリコン配線10が存在している。また、上記素子分離領域7内の半導体部9及び溝部8に跨って、ゲート電極4と同時に形成された多結晶シリコン膜からなるダミーゲート51が存在している。さらに、ダミーゲート51、多結晶シリコン配線10及びシリコン基板表面(活性領域を除く)に亘る領域の上には、酸化珪素膜52と、多結晶シリコン膜からなる高抵抗膜53とが積層して形成されている。ダミーゲート51は、ゲート電極4及び多結晶シリコン配線10と共通の第1層目の多結晶シリコン膜をバタニングして形成されており、ゲート電極4及び多結晶シリコン配線10とは一定の間隔を隔てて形成されている。ここで、高抵抗膜53を構成する多結晶シリコン膜は、ゲート電極4等を構成する第1層目の多結晶シリコン膜よりも高いシート抵抗を有しており、不純物濃度は $1 \times 10^{20} \text{ cm}^{-3}$ 以下である。なお、ダミーゲート51のシート抵抗も、活性領域への不純物注入時に素子分離領域をレジスト膜等で覆っておくことにより、高抵抗に保つことができる。

【0070】

本実施形態の半導体装置においては、配線-基板間の容量ではなく配線-高抵抗膜間の容量を考慮すればよい。その場合、高抵抗膜53を構成する多結晶シリコン膜の抵抗が高いために、高抵抗膜53の上端とシリコン基板1の表面との間で電圧降下が起こる。したがって、層間絶縁膜12自体の容量は変わらないが、層間絶縁膜の両端に印加される電圧が低い。層間絶縁膜12の両側に蓄えられる電荷量は電圧に比例して減少するので、配線-高抵抗膜間における電荷の充放電に要する時間が短くなり、半導体装置の動作速度が向上する。

【0071】

本実施形態における高抵抗膜53は、例えば抵抗素子の高抵抗膜やローカル配線と共通の膜からパターニングすることにより容易かつ安価に形成することができる。また、ダミーゲート51の代わりに、半導体基板上のいずれかにMIMキャパシタを形成する際に使用する上層膜、容量絶縁膜及び下層膜を構成する3つの膜から上記高抵抗膜53、酸化珪素膜52及びダミーゲート51に相当する膜を形成することも可能である。

【0072】

さらに、上記ダミーゲート51及び高抵抗膜53のうちいずれか一方と酸化珪素膜52とがなくても、電荷の充放電に要する時間の低減による半導体装置の動作速度の向上を図ることは可能である。

【0073】

なお、ここでは素子分離領域7上に高抵抗膜53を構成する多結晶シリコン膜と酸化珪素膜52との積層膜が存在する場合を述べたが、多結晶シリコン膜の代わりに非晶質シリコン膜や窒化珪素膜を用いた場合でも同様の効果がある。特に、酸化珪素膜などの絶縁膜を用いれば、全容量も低減でき、半導体装置の動作速度をいっそう向上できる。

【0074】

(第5の実施形態)

図5は、第5の実施形態にかかる半導体装置の断面図である。

【0075】

同図に示すように、P型シリコン基板1の活性領域6には、ゲート酸化膜2と、多結晶シリコン膜からなるゲート電極4と、ソース・ドレイン5とにより構成されるMOSFETとして機能する素子が設けられている。また、各素子を電気的に分離するための素子分離領域7には、絶縁性材料である酸化珪素膜が埋め込まれた複数の溝部8と、各溝部8の間に設けられ活性領域としては機能しないダミーの半導体部9が存在する。また、素子分離領域7の1つの溝部8の上には、ゲート電極4と同時に形成された多結晶シリコン配線10が存在している。

【0076】

ここで、本実施形態では、ゲート電極4が第1の導電膜からなる下層部4aと、第2の導電膜からなる上層部4bとにより構成されている。そして、素子分離領域7には、ゲート電極4の下層部4aと同じ第1の導電膜により構成される下層部51aと、ゲート電極4の上層部4bと同じ第2の導電膜により構成される上層部51bとからなるダミーゲート51が設けられている。このダミーゲート51の下層部51aの上面は溝部8の上面と同じ高さ位置を有し、この下層部51aと溝部8とが平坦化されている。また、多結晶シリコン配線10は、ゲート電極4の上層部4bを構成する第2の導電膜のみにより構成されている。ダミーゲート51は、ゲート電極4及び多結晶シリコン配線10とは一定の間隔を隔てて形成されており、ラインアンドスペースの関係によってフォトリソグラフィ工程におけるパターニング精度を高くするようになされている。そして、基板の全面上に堆積された酸化珪素膜からなる層間絶縁膜12と、層間絶縁膜12の上に形成されたメタル配線13とを備えている。

【0077】

そして、基板の全面上に堆積された酸化珪素膜からなる層間絶縁膜12と、層間絶縁膜12の上に形成されたメタル配線13とを備えている。

【0078】

本実施形態においても、上記第4の実施形態と同様に、層間絶縁膜の両端に蓄積される電荷量の低減による動作速度の向上を図ることができる。なお、本実施形態のような構造を有する半導体装置においては、ゲート電極4のうち上層部4

bはシリサイドなど低抵抗の膜で構成されることが多いが、その場合にも、配線-基板間の電圧は上層部4bと下層部4aとに直列に印加されるので電圧降下による電荷量の低減作用、ひいては半導体装置の動作速度の向上効果を有効に発揮することができる。

【0079】

本実施形態では、上記第4の実施形態のような高抵抗膜を設けていないが、ダミーゲートの上に絶縁膜を挟んで高抵抗膜を設けてもよいことはいうまでもない。

【0080】

(第6の実施形態)

図6は、第6の実施形態にかかる半導体装置の断面図である。

【0081】

同図に示すように、P型シリコン基板1の活性領域6には、ゲート酸化膜2と、多結晶シリコン膜からなるゲート電極4と、ソース・ドレイン5とにより構成されるMOSFETとして機能する素子が設けられている。また、各素子を電気的に分離するための素子分離領域7には、絶縁性材料である酸化珪素膜が埋め込まれた複数の溝部8と、各溝部8の間に設けられ活性領域としては機能しないダミーの半導体部9が存在する。また、素子分離領域7の1つの溝部8の上には、ゲート絶縁膜2及びゲート電極4と同時に形成された多結晶シリコン配線10が存在している。さらに基板の全面上に堆積された酸化珪素膜からなる層間絶縁膜12と、層間絶縁膜12の上に形成されたメタル配線13とを備えている。

【0082】

ここで、素子分離領域7内のダミーの半導体部9の上方かつ層間絶縁膜12の下方には、酸化珪素膜からなる埋め込み絶縁膜61が溝部8に囲まれるように形成されている。この埋め込み絶縁膜61の上面は溝部8の上面と同じ高さ位置にあり、埋め込み絶縁膜61の下端は溝部8の上面と底面との間の高さ位置にある。

【0083】

本実施形態の半導体装置においては、ダミーの半導体部9が掘り下げられ、酸

化珪素膜で埋め込まれた埋め込み絶縁膜 61 が形成されているので、図 10 に示す従来の半導体装置に比べ、配線-基板間距離が長い。配線-基板間容量は距離に反比例して小さくなるので、本実施形態の半導体装置の配線-基板間容量は従来の半導体装置における配線-基板間容量よりも低減され、半導体装置の動作速度の向上を図ることができる。

【0084】

なお、本実施形態においては、ダミー活性領域に酸化珪素膜が埋め込まれた例について説明したが、酸化珪素膜の代わりに窒化珪素膜などの絶縁膜を用いても同様の効果が得られる。

【0085】

(第7の実施形態)

図7は第7の実施形態にかかる半導体装置の断面図である。

【0086】

同図に示すように、P型シリコン基板1の活性領域6には、ゲート酸化膜2と、多結晶シリコン膜からなるゲート電極4と、ソース・ドレイン5とにより構成されるMOSFETとして機能する素子が設けられている。また、各素子を電気的に分離するための素子分離領域7には、絶縁性材料である酸化珪素膜が埋め込まれた複数の溝部8と、各溝部8の間に設けられ活性領域としては機能しないダミーの半導体部9が存在する。また、素子分離領域7の1つの溝部8の上には、ゲート絶縁膜2及びゲート電極4と同時に形成された多結晶シリコン配線10が存在している。さらに基板の全面上に堆積された酸化珪素膜からなる層間絶縁膜12と、層間絶縁膜12の上に形成されたメタル配線13とを備えている。

【0087】

ここで、素子分離領域7内のダミーの半導体部9の上部には酸素原子がイオン注入などによって導入され、高抵抗のシリコン層からなる高抵抗体部71が形成されている。この高抵抗体部71の下端の高さ位置は、溝部8の上面と底面との間にあるが、溝部8の底面よりも下方に位置していてもよい。

【0088】

本実施形態に係る半導体装置においては、ダミーの半導体部9のシリコン基板

にイオン注入などにより酸素原子が導入され高抵抗のシリコン層からなる高抵抗体部71が形成されているために、配線-基板間に電圧が印加された場合に高抵抗体部71において電圧降下が生じる。したがって、配線-半導体部9間の電位差が小さくなり、配線-半導体部9間の層間絶縁膜12自体の容量は、図10に示す従来の半導体装置における層間絶縁膜12の容量と変わらないが、蓄積電荷量は電圧に比例して減少する。したがって、容量に対する電荷の充放電に要する時間が短くなり、半導体装置の動作速度が向上する。

【0089】

なお、本実施形態においては、ダミーの半導体部9に導入された不純物が酸素原子の例について説明したが、窒素原子を導入しても同様の効果が得られる。

【0090】

(第8の実施形態)

図8は、第8の実施形態にかかる半導体装置の断面図である。

【0091】

同図に示すように、P型シリコン基板1の活性領域6には、ゲート酸化膜2と、多結晶シリコン膜からなるゲート電極4と、ゲート電極4の側面上に形成された酸化珪素膜からなるサイドウォール3と、ソース・ドレイン5とにより構成されるMOSFETとして機能する素子が設けられている。また、各素子を電気的に分離するための素子分離領域7には、絶縁性材料である酸化珪素膜が埋め込まれた複数の溝部8と、各溝部8の間に設けられ活性領域としては機能しないダミーの半導体部9が存在する。また、素子分離領域7の1つの溝部8の上には、ゲート絶縁膜2及びゲート電極4と同時に形成された多結晶シリコン配線10が存在している。さらに基板の全面上に堆積された酸化珪素膜からなる層間絶縁膜12と、層間絶縁膜12の上に形成されたメタル配線13とを備えている。

【0092】

ここで、素子分離領域7内のダミーの半導体部9及び溝部8に跨って、ゲート電極4の側面上のサイドウォールと同時に形成された酸化珪素膜からなる下敷き絶縁膜81が形成されている。なお、この下敷き絶縁膜81は、多結晶シリコン配線10全体を覆うように形成されている。

【0093】

本実施形態の半導体装置によると、素子分離領域7の上には酸化珪素膜からなる下敷き絶縁膜81が存在しているので、図10に示す従来の半導体装置に比べ、配線-基板間距離が長い。配線-基板間容量は距離に反比例して小さくなるために、本実施形態の半導体装置では配線-基板間容量が低減され、よって、動作速度の向上を図ることができる。

【0094】

なお、本実施形態においては、下敷き絶縁膜81を酸化珪素膜により構成した例について説明したが、窒化珪素膜などの絶縁膜を用いても同様の効果が得られる。

【0095】

また、本実施形態においては下敷き膜が単層膜である場合について説明したが、下敷き絶縁膜は単層膜である必要はなく、積層膜であってもよい。例えば、サイドウォールがゲート電極の側面から基板上に跨るL字状の部分とその上のくさび状の部分とからなるものであったり、ゲート上保護膜とサイドウォールとを設けた場合などには、下敷き絶縁膜も積層膜となる。かかる場合にも本実施形態と同様の効果を発揮しうることはいうまでもない。

【0096】

(第9の実施形態)

図9(a)は、第9の実施形態にかかる半導体装置の断面図である。

【0097】

同図に示すように、P型シリコン基板1の活性領域6には、ゲート酸化膜2と、多結晶シリコン膜からなるゲート電極4と、ソース・ドレイン5とにより構成されるMOSFETとして機能する素子が設けられている。また、各素子を電気的に分離するための素子分離領域7には、絶縁性材料である酸化珪素膜が埋め込まれた複数の溝部8と、各溝部8の間に設けられ活性領域としては機能しないダミーの半導体部9が存在する。また、素子分離領域7の1つの溝部8の上には、ゲート絶縁膜2及びゲート電極4と同時に形成された多結晶シリコン配線10が存在している。さらに、基板の全面上に堆積された酸化珪素膜からなる層間絶縁

膜12と、層間絶縁膜12の上に形成されたメタル配線13とを備えている。

【0098】

ここで、上記ダミーの半導体部9及び溝部8の下方には、酸化珪素膜からなる埋め込み絶縁膜91が溝部8の下端に接して形成されている。その結果、半導体部9の側面は溝部8に、半導体部9の底面は埋め込み絶縁膜91に接している。

【0099】

図9(b)は、本実施形態に係る半導体装置の配線-基板間容量を説明するための断面図である。本実施形態に係る半導体装置によると、シリコン基板下に酸化珪素膜からなる埋め込み絶縁膜91を形成しているので、容量 C_{ij} は、図1(b)に示す容量 C_{j1} の2分の1以下になる(T. Nishimura and Y. Inoue: Proceedings of VLSI TECHNOLOGY WORKSHOP ON "WHAT IS THE FUTURE OF SOI?" (1995) p.123)。

【0100】

したがって、半導体装置の全配線-基板間容量 C_{ijt} は、下記式(11)

$$C_{ijt} = \Sigma \{ (C_{a1} \times C_{ij}) / (C_{a1} + C_{ij}) \} + \Sigma C_{a2} \quad (11)$$

で表され、式(3)で表わされる全容量 C_{jt} より小さくなる。すなわち、下記式(12)

$$C_{ijt} < C_{jt} \quad (12)$$

が成立する。よって、上述の式(4)の関係より

$$C_{ijt} < C_{at}$$

となり、本実施形態に係る半導体装置の配線-基板間容量が小さくなるので、半導体装置の動作速度が向上する。

【0101】

なお、上記各実施形態では、活性領域6内に配置される素子としてMOSFETを設けたが、本発明はかかる実施形態に限定されるものではなく、素子にはバイポーラトランジスタ、ダイオード等のMOSFET以外の能動素子や、キャパシタ等の受動素子も含まれるものとする。

【0102】

【発明の効果】

請求項1～2によると、絶縁性材料が埋め込まれた溝部と、それ自身としては活性領域として機能しないダミーの半導体部とからなる素子分離領域を有し、基板全体上に層間絶縁膜を介して配線を設けてなる半導体装置において、ダミーの半導体部にPN接合を設けたので、配線－基板間容量のうち半導体部を通る領域の容量成分を低減することができ、よって、半導体装置全体の配線－基板間容量の低減により半導体装置の動作速度の向上を図ることができる。

【0103】

請求項3～8によると、絶縁性材料が埋め込まれた溝部と、それ自身としては活性領域として機能しないダミーの半導体部とからなる素子分離領域を有し、基板全体上に層間絶縁膜を介して配線を設けてなる半導体装置において、素子分離領域のうち少なくともダミーの半導体部と層間絶縁膜との間に誘電体膜を設けたので、配線－基板間容量のうち少なくとも半導体部を通る領域の容量成分を低減することができ、よって、半導体装置全体の配線－基板間容量の低減により半導体装置の動作速度の向上を図ることができる。

【0104】

請求項9によると、絶縁性材料が埋め込まれた溝部と、それ自身としては活性領域として機能しないダミーの半導体部とからなる素子分離領域を有し、基板全体上に層間絶縁膜を介して配線を設けてなる半導体装置において、ダミーの半導体部の側面と底面を絶縁膜で囲むようにしたので、配線－基板間容量のうち素子分離領域を通る領域における容量成分を低減することができ、よって、半導体装置の動作速度の向上を図ることができる。

【0105】

請求項10～17によると、絶縁性材料が埋め込まれた溝部と、それ自身としては活性領域として機能しないダミーの半導体部とからなる素子分離領域を有し、基板全体上に層間絶縁膜を介して配線を設けてなる半導体装置において、素子分離領域のうち少なくともダミーの半導体部と層間絶縁膜との間に抵抗体膜を設けたので、配線－基板間における電圧の印加に対する層間絶縁膜にかかる電位差

の低下を利用して、蓄積電荷量を少なくすることができ、よって、電荷の充放電に要する時間の短縮により半導体装置の動作速度の向上を図ることができる。

【図面の簡単な説明】

【図1】

半導体部に浅いPN接合部を形成した第1の実施形態に係る半導体装置の断面図である。

【図2】

半導体部に深いPN接合部を形成した第2の実施形態に係る半導体装置の断面図である。

【図3】

半導体部に2つのPN接合部を形成した第3の実施形態に係る半導体装置の断面図である。

【図4】

半導体部の上に高抵抗体膜を設けた第4の実施形態に係る半導体装置の断面図である。

【図5】

積層ゲートを設けた第5の実施形態に係る半導体装置の断面図である。

【図6】

半導体部の上に埋め込み絶縁膜を設けた第6の実施形態に係る半導体装置の断面図である。

【図7】

半導体部の上部を高抵抗体部とした第7の実施形態に係る半導体装置の断面図である。

【図8】

層間絶縁膜の下方に下敷き絶縁膜を設けた第8の実施形態に係る半導体装置の断面図である。

【図9】

素子分離領域の全体に亘る埋め込み絶縁膜を設けた第9の実施形態に係る半導体装置の断面図である。

【図10】

従来の半導体装置の断面図である。

【図11】

従来のトレンチ分離型半導体装置とLOCOS分離型半導体装置とにおける配線-基板間容量を説明するための断面図である。

【符号の説明】

- 1 シリコン基板
- 2 ゲート酸化膜
- 3 サイドウォール
- 4 ゲート電極
- 5 ソース・ドレイン
- 6 活性領域
- 7 素子分離領域
- 8 溝部
- 9 半導体部
- 13 メタル配線
- 14 溝
- 21, 31 不純物拡散層
- 22, 32 PN接合部
- 41 P型不純物拡散層
- 42 N型不純物拡散層
- 43 第1PN接合部
- 44 第2PN接合部
- 51 ダミーゲート
- 52 酸化珪素膜
- 53 高抵抗膜
- 61 埋め込み絶縁膜
- 71 高抵抗体部
- 81 下敷き絶縁膜

特平 8-314762

91 埋め込み絶縁膜

【書類名】 要約書

【要約】

【課題】 素子分離領域内の配線-基板間容量の低減し、又は容量内の蓄積電荷量を低減することにより、動作速度の高い半導体装置を提供する。

【解決手段】 P型シリコン基板1の上に、素子が配置される活性領域6と、これを囲む素子分離領域7とが設けられ、素子分離領域7は、溝部8とダミーの半導体部9とにより構成されている。基板上には層間絶縁膜12が堆積され、その上には配線13が設けられている。半導体部9内には、素子へのイオン注入と同時に形成された不純物拡散層21が形成され、不純物拡散層21とシリコン基板1との間にPN接合部22が形成されている。配線-基板間容量のうち半導体部9を通る領域の容量成分は、層間絶縁膜12の容量に不純物拡散層21の容量が直列に付加されたものとなり、層間絶縁膜のみによる容量よりも小さくなるので、全配線-基板間容量が低減し、半導体装置の動作速度が速くなる。

【選択図】 図1

【書類名】 職権訂正データ
【訂正書類】 特許願

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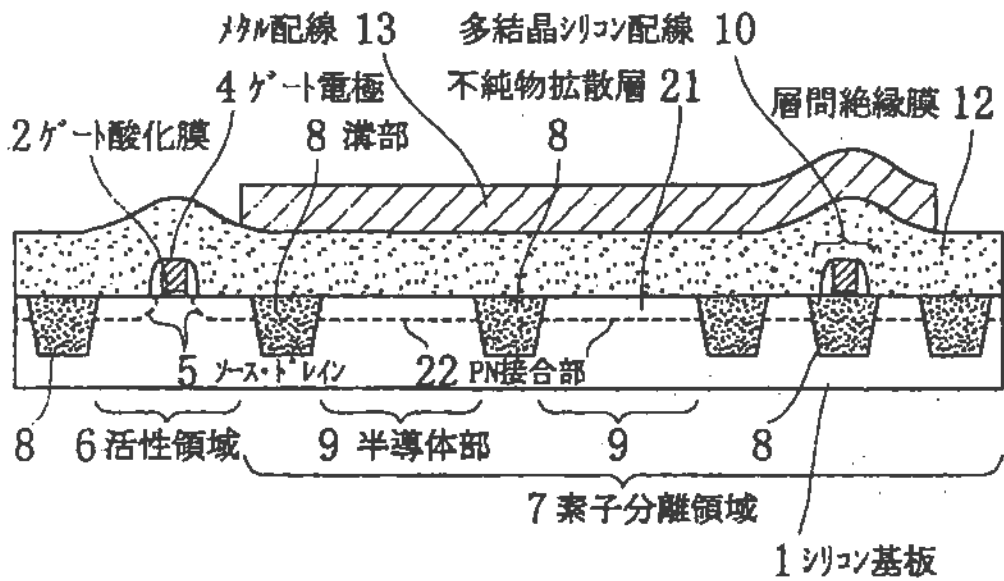
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氏 名 松下電器産業株式会社

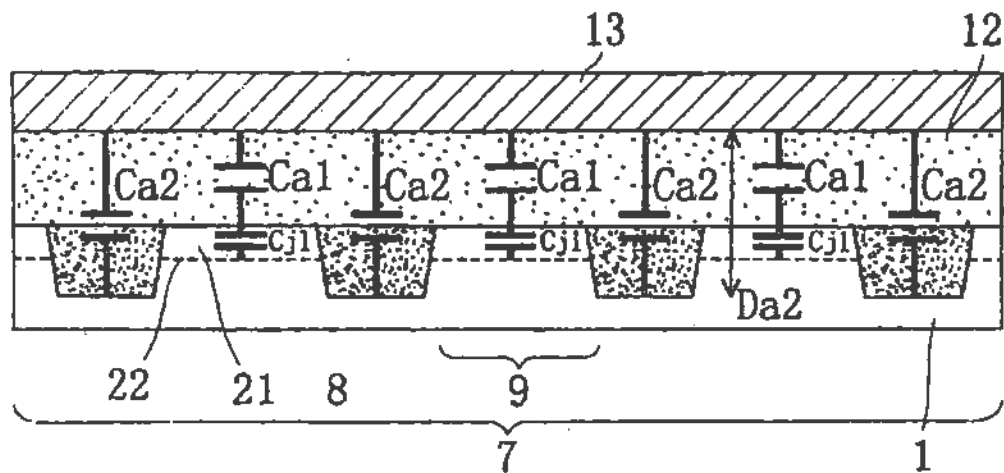
【書類名】 図面

【図1】

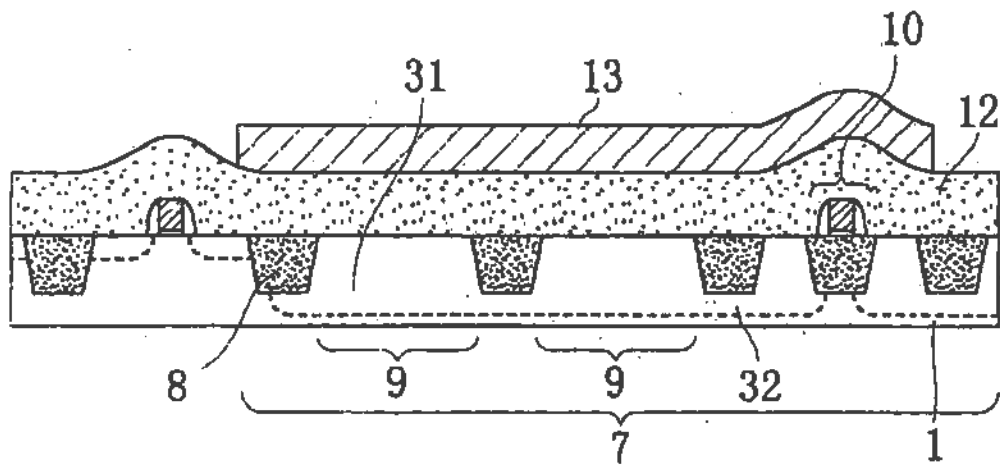
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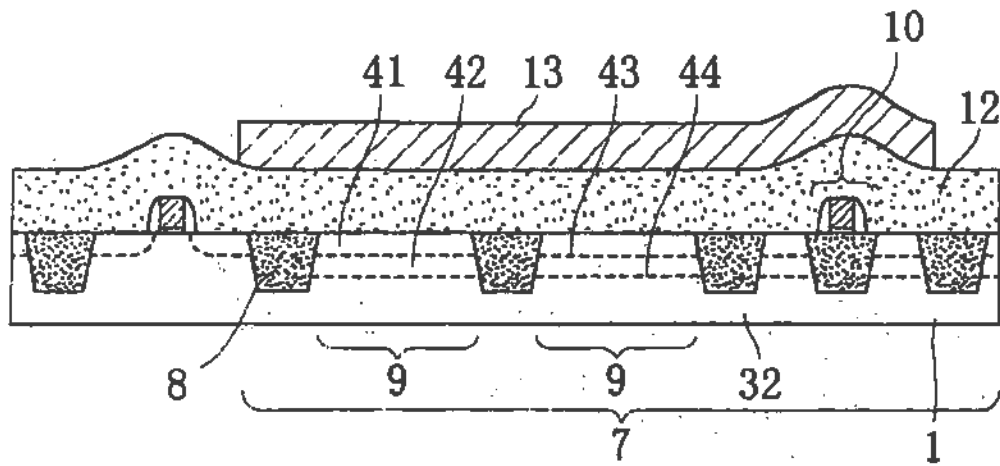
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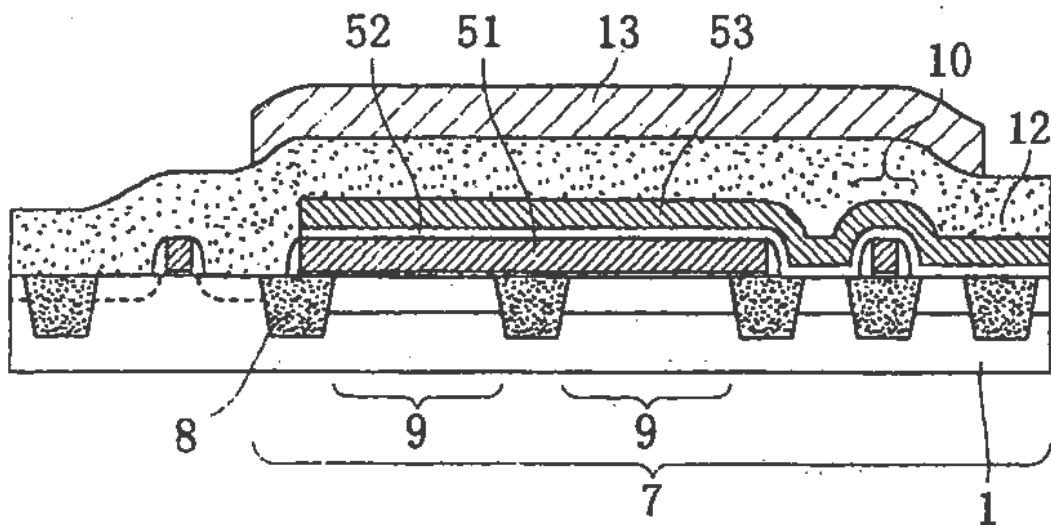
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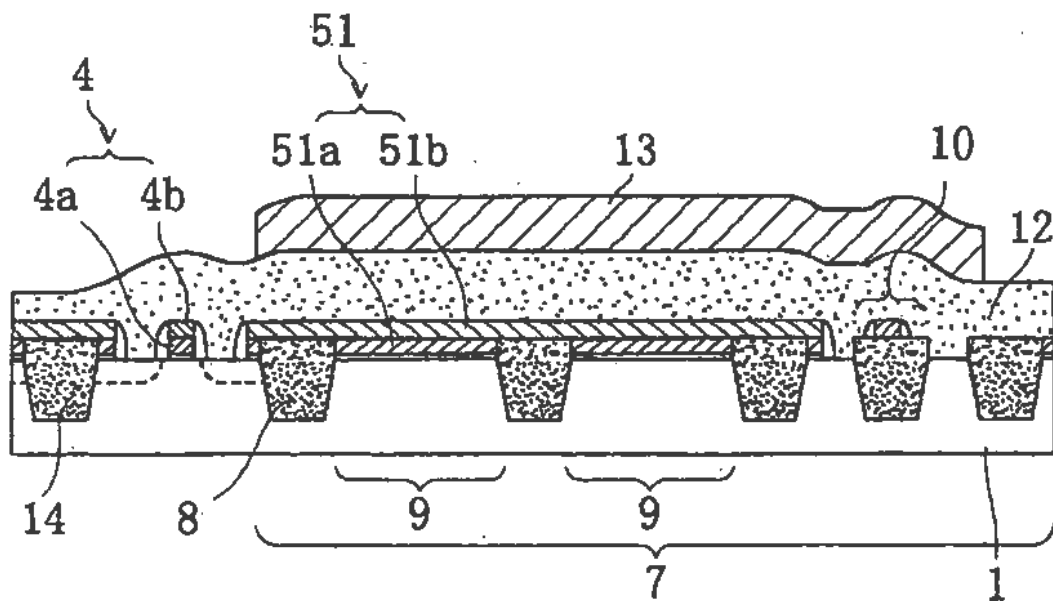
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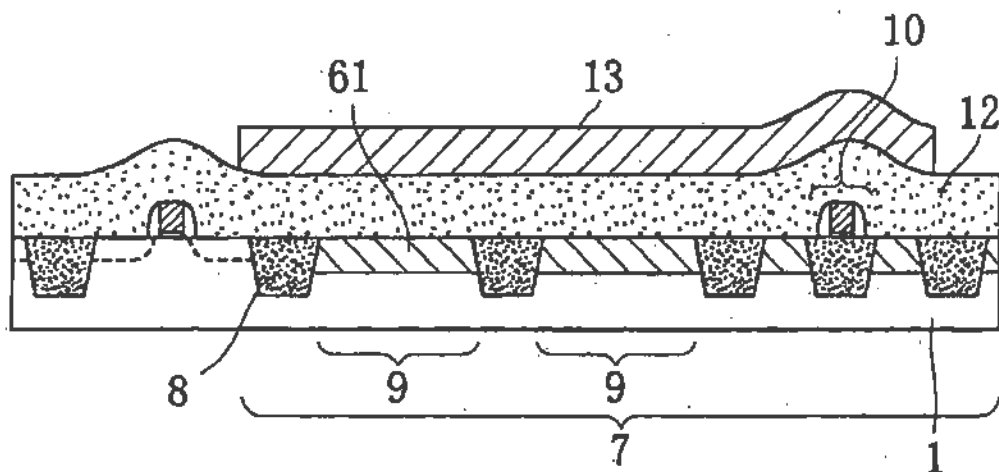
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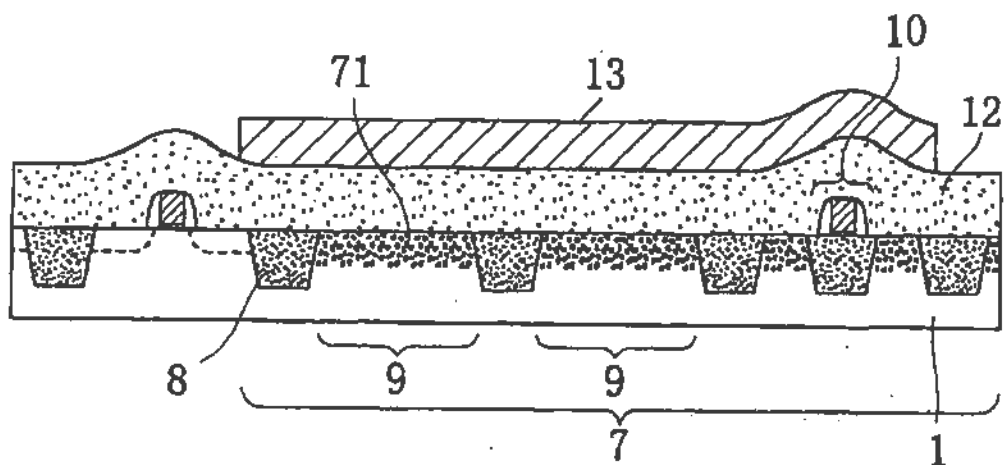
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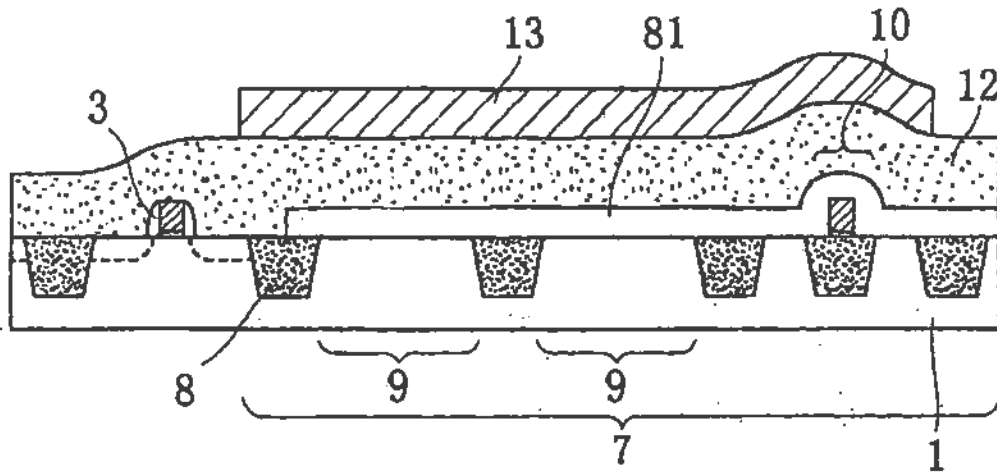
【图 6】



【圖 7】

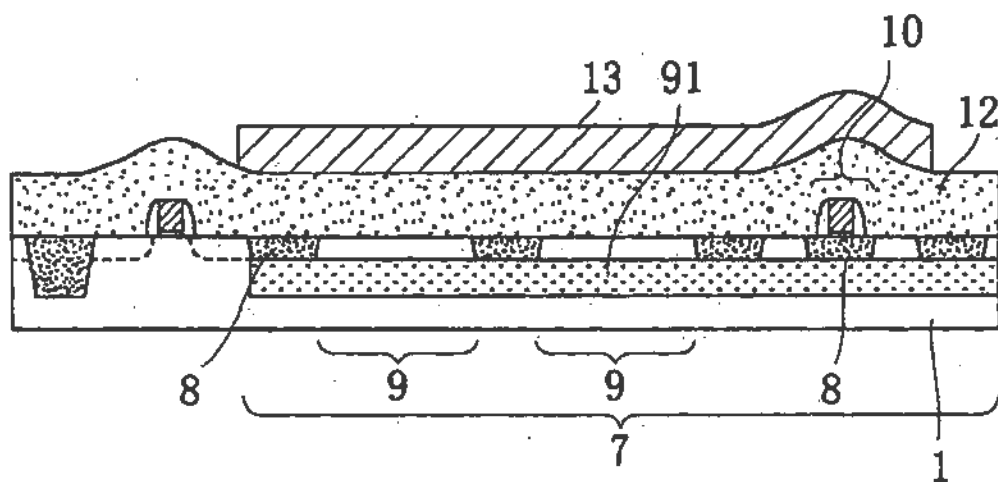


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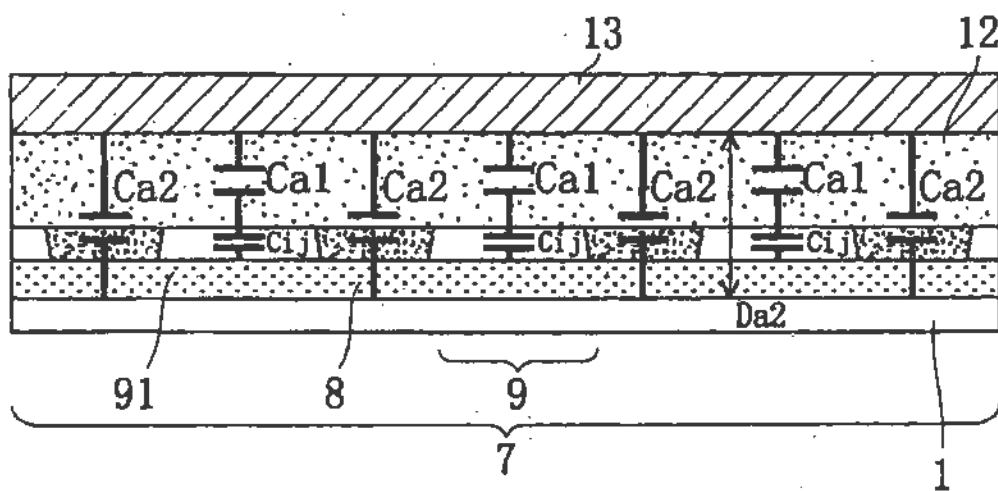


【図9】

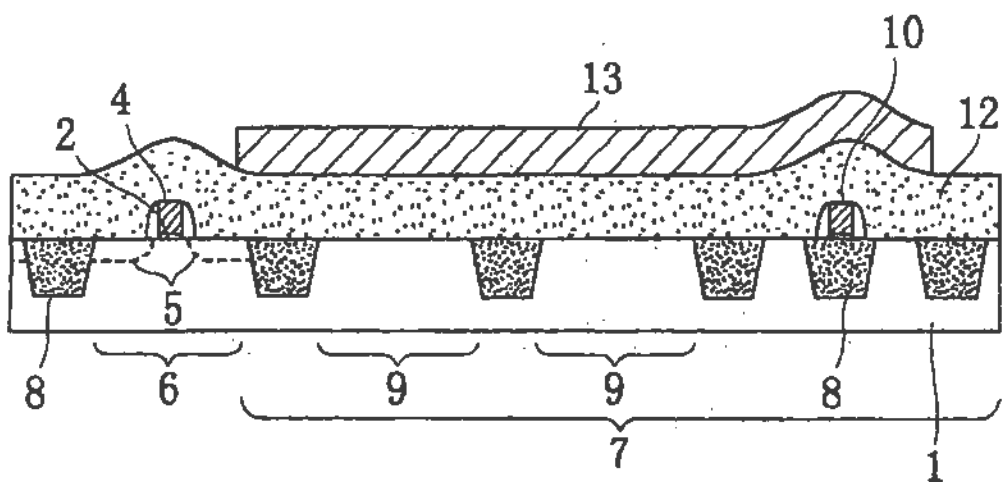
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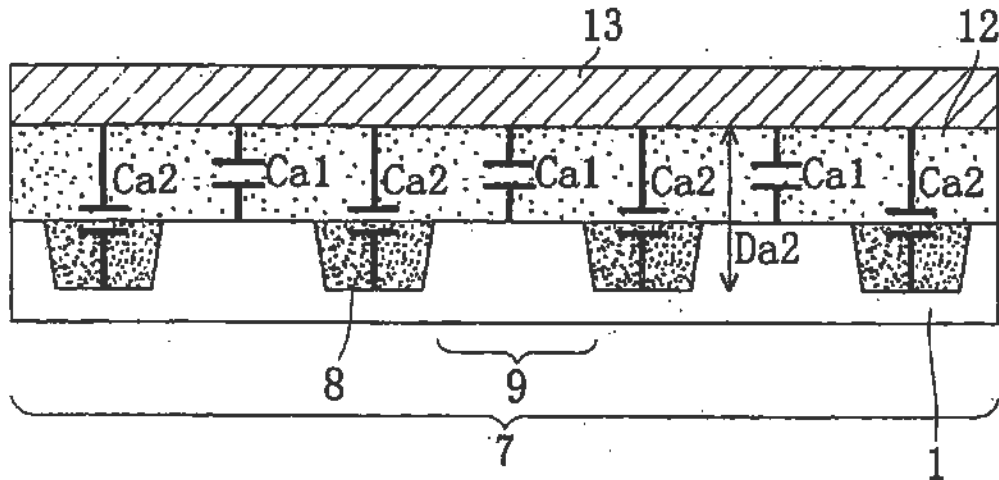


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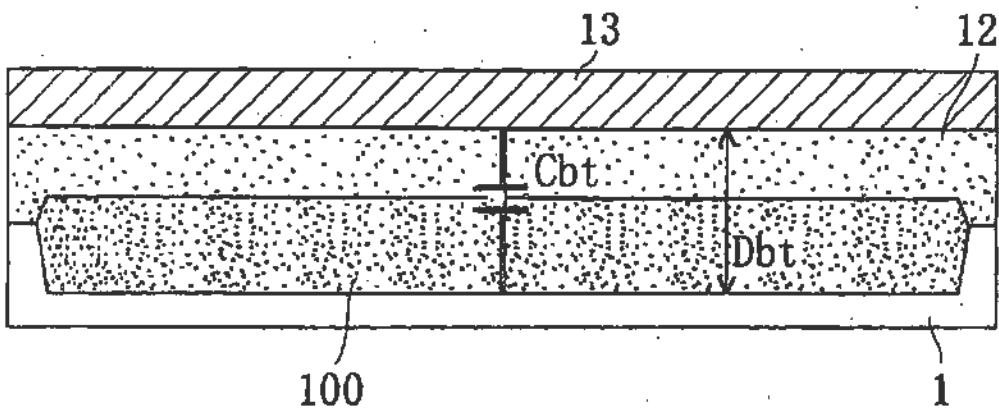


【図11】

(a)



(b)



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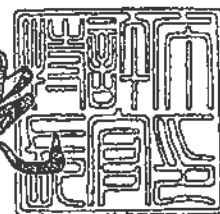


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【請求項の数】 19

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【書類名】 明細書

【発明の名称】 半導体装置の製造方法

【特許請求の範囲】

【請求項1】 第1導電型の基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、

上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、

上記活性領域上に素子を形成する第3の工程と、

上記素子分離領域の上記ダミーの半導体部に第2導電型不純物を導入して、上記ダミーの半導体部に少なくとも1つのPN接合部を形成する第4の工程と、

基板の全面上に層間絶縁膜を形成する第5の工程と、

上記層間絶縁膜の上に配線を形成する第6の工程とを備えていることを特徴とする半導体装置の製造方法。

【請求項2】 請求項1記載の半導体装置の製造方法において、

上記第3の工程及び上記第4の工程では、上記活性領域上に上記素子としてのFETのゲート電極を形成した後、上記活性領域及び上記ダミーの半導体部に第2導電型不純物を導入することにより、上記活性領域には上記FETのソース・ドレインを形成する一方、上記ダミーの半導体部には1つの上記PN接合部を形成することを特徴とする半導体装置の製造方法。

【請求項3】 基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、

上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、

上記活性領域に素子を形成する第3の工程と、

上記素子分離領域の上記ダミーの半導体部の上に抵抗体膜を形成する第4の工程と、

基板の全面上に層間絶縁膜を形成する第5の工程と、

上記層間絶縁膜の上に配線を形成する第6の工程と
を備えていることを特徴とする半導体装置の製造方法。

【請求項4】 請求項3記載の半導体装置の製造方法において、

上記第4の工程では、上記抵抗膜を多結晶シリコン及び非晶質シリコンのうち少なくともいずれか一方を含む膜により構成することを特徴とする半導体装置の製造方法。

【請求項5】 請求項3記載の半導体装置の製造方法において、

上記第4の工程では、上記抵抗膜を少なくとも絶縁膜を挟んだ2つ以上の導体膜からなる積層膜により構成することを特徴とする半導体装置の製造方法。

【請求項6】 請求項3又は4記載の半導体装置の製造方法において、

上記第4の工程では、上記抵抗膜に $1 \times 10^{20} \text{ atoms} \cdot \text{cm}^{-3}$ 以下の濃度の不純物を導入することを特徴とする半導体装置の製造方法。

【請求項7】 基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、

上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、

上記活性領域に素子を形成する第3の工程と、

上記ダミーの半導体部の上部にイオン注入を行って上記半導体部の上部に高抵抗層を形成する第4の工程と、

基板の全面上に層間絶縁膜を形成する第5の工程と、

上記層間絶縁膜の上に配線を形成する第6の工程と
を備えていることを特徴とする半導体装置の製造方法。

【請求項8】 請求項7記載の半導体装置の製造方法において、

上記第4の工程では、少なくとも酸化原子を含むイオンを注入して上記高抵抗層を形成することを特徴とする半導体装置の製造方法。

【請求項9】 請求項7記載の半導体装置の製造方法において、

上記第4の工程では、少なくとも窒化原子を含むイオンを注入して上記高抵抗層を形成することを特徴とする半導体装置の製造方法。

【請求項10】 基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、

上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、

上記活性領域に素子を形成する第3の工程と、

上記素子分離領域の上記ダミーの半導体部の上に下敷き絶縁膜を形成する第4の工程と、

基板の全面上に層間絶縁膜を形成する第5の工程と、

上記層間絶縁膜の上に配線を形成する第6の工程とを備えていることを特徴とする半導体装置の製造方法。

【請求項11】 請求項10記載の半導体装置の製造方法において、

上記第3の工程及び上記第4の工程では、上記活性領域上に上記素子となるFETのゲート電極を形成した後、基板上に誘電体膜を堆積して、上記素子分離領域上を覆うマスクを用いてこの誘電体膜の異方性エッチングを行うことにより、上記ゲート電極の側面上にはサイドウォールを、上記ダミーの半導体部の上には上記下敷き絶縁膜をそれぞれ残すことを特徴とする半導体装置の製造方法。

【請求項12】 請求項10又は11記載の半導体装置の製造方法において、

上記第4の工程では、少なくとも酸化珪素を含む誘電体膜により上記下敷き絶縁膜を形成することを特徴とする半導体装置の製造方法。

【請求項13】 請求項10又は11記載の半導体装置の製造方法において、

上記第4の工程では、少なくとも窒化珪素を含む誘電体膜により上記下敷き絶縁膜を形成することを特徴とする半導体装置の製造方法。

【請求項14】 基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、

上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の

埋め込み溝部とをそれぞれ形成する第2の工程と、

上記活性領域に素子を形成する第3の工程と、

上記ダミーの半導体部をエッチングにより除去して第3の溝を形成し、上記第3の溝内に絶縁性材料を埋め込んで上記第1及び第2の埋め込み溝部と共通の上面位置を有する埋め込み絶縁膜を形成する第4の工程と、

基板の全面上に層間絶縁膜を形成する第5の工程と、

上記層間絶縁膜の上に配線を形成する第6の工程と
を備えていることを特徴とする半導体装置の製造方法。

【請求項15】 請求項14記載の半導体装置の製造方法において、

上記第4の工程では、少なくとも酸化珪素を含む誘電体膜により上記埋め込み絶縁膜を形成することを特徴とする半導体装置の製造方法。

【請求項16】 請求項14記載の半導体装置の製造方法において、

上記第4の工程では、少なくとも窒化珪素を含む誘電体膜により上記埋め込み絶縁膜を形成することを特徴とする半導体装置の製造方法。

【請求項17】 基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、

上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、

上記活性領域に素子を形成する第3の工程と、

上記ダミーの半導体部の内部に酸素イオンの注入を行って上記半導体部の奥方に埋め込み絶縁膜を形成する第4の工程と、

基板の全面上に層間絶縁膜を形成する第5の工程と、

上記層間絶縁膜の上に配線を形成する第6の工程と
を備えていることを特徴とする半導体装置の製造方法。

【請求項18】 基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数の半導体部に分割する第2の溝とを形成する第1の工程と、

上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の

埋め込み溝部とをそれぞれ形成する第2の工程と、

上記半導体部をエッチングにより除去して第3の溝を形成し、上記第3の溝内に絶縁性材料を埋め込んで上記第1及び第2の埋め込み溝部よりも低い上面位置を有する埋め込み絶縁膜を形成する第3の工程と、

上記活性領域をマスク部材で覆った状態で上記埋め込み絶縁膜の上に半導体膜を成長させてダミーの半導体部を形成する第4の工程と、

上記活性領域の上に素子を形成する第5の工程と、

基板の全面上に層間絶縁膜を形成する第6の工程と、

上記層間絶縁膜の上に配線を形成する第7の工程とを備えていることを特徴とする半導体装置の製造方法。

【請求項19】 基板領域を有する半導体基板に、上記基板領域のうち素子分離領域全体に亘る第1の溝を形成し、上記基板領域のうち活性領域を残す第1の工程と、

上記第1の溝に絶縁性材料を埋め込んで上記素子形成領域と共通の上面位置を有する埋め込み絶縁膜を形成する第2の工程と、

上記活性領域及び上記埋め込み絶縁膜の上に半導体膜を成長させる第3の工程と、

半導体基板基板に、上記半導体膜及び上記基板領域を活性領域と素子分離領域とに区画する第2の溝と、上記素子分離領域の半導体膜を複数のダミーの半導体部に分割する第3の溝とを形成する第4の工程と、

上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第5の工程と、

上記活性領域上の上記半導体膜の上に素子を形成する第6の工程と、

基板の全面上に層間絶縁膜を形成する第7の工程と、

上記層間絶縁膜の上に配線を形成する第8の工程とを備えていることを特徴とする半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】

本発明は、トレンチ分離構造を有する半導体装置に係り、特に配線－基板間容量の低減対策に関する。

【0002】

【従来の技術】

近年、半導体装置の高密度化・微細化に伴い、半導体装置内の各素子間を分離絶縁するための素子分離を形成する技術として、現在最も一般的に用いられているLOCOSの代わりに、半導体基板に溝を形成し、この溝に絶縁性材料を埋め込んで素子分離とするトレンチ分離技術の導入が試みられている。

【0003】

このトレンチ分離技術においては、半導体基板及び絶縁材料が埋め込まれた埋め込み溝部の表面を均一に平坦化することが重要であるので、近年、面内均一性に優れパターン依存性の無い平坦化技術として化学機械研磨法（CMP法）の導入が試みられている。さらに、CMP法による平坦化を行う工程では、平坦化される領域の面積などに依存して研磨特性が変化するいわゆるパターン依存性による不具合を回避するために、埋め込み溝部の面積が広くなるような場合には、素子分離領域に予めダミーの島状の半導体部を設けることが提案されている。つまり、埋め込み溝部を複数の細い溝に分割して各溝間に半導体基板表面を露出させて活性領域としては機能しないダミーの半導体部を設けるのである。

【0004】

図12（a）～（g）に従来のトレンチ分離を用いたNMOSトランジスタを有する半導体装置の製造方法の一例を示す。

【0005】

図12（a）に示す工程では、P型シリコン基板1に、厚さ10nmの薄い酸化珪素膜21と窒化珪素膜22を順次形成する。

【0006】

図12（b）に示す工程では、シリコン基板1に所定幅の複数の溝14を形成

する。ただし、これらの溝14には、素子が形成される活性領域6を取り囲むように形成された溝14aと、この溝によって活性領域と区画される素子分離領域7に形成される仕上りの平坦性のパターン依存性を解消するための溝14bと、多結晶シリコン配線を形成するための溝14cとがある。そして、素子分離領域7内にも、上記溝14によって囲まれる1つ以上の凸部となる半導体部9が形成されている。この半導体部9は、活性領域としては機能しないダミーの活性領域ともいうべきものである。

【0007】

図12(c)に示す工程では、基板の全面上に酸化珪素膜23を堆積し、溝14を酸化珪素膜で埋め込む。

【0008】

図12(d)に示す工程では、CMP法を用いて酸化珪素膜23を研磨する。続いて、窒化珪素膜22と酸化珪素膜21を除去し、表面が平坦で酸化珪素膜で埋め込まれた複数の埋め込み溝部8を形成する。この埋め込み溝部8のうち埋め込み溝部8aが素子分離として機能するものであり、埋め込み溝部8bはダミーの半導体部9を形成するものであり、埋め込み溝部8cが多結晶シリコン配線とシリコン基板とを絶縁する機能を有するものである。

【0009】

図12(e)に示す工程では、周知の技術を用いてゲート酸化膜2と、側面上にサイドウォール24を有するゲート電極4と、多結晶シリコン配線10とを形成する。ゲート電極4と多結晶シリコン配線10は同時に形成される。

【0010】

図12(f)に示す工程では、PMOSFET領域及び素子分離領域を覆うレジストマスクRemを用いて、NMOSFET領域の活性領域6に砒素イオン25を注入し、ソース・ドレイン5を形成する。これまでの工程によって、NMOSFETが形成される。

【0011】

その後、図12(g)に示す工程では、酸化珪素膜を堆積して層間絶縁膜12を形成し、さらにその上にメタル配線13を形成する。

【0012】

図13(a)は、上述の工程で得られた半導体装置の素子分離領域7を拡大して示す断面図である。

【0013】

すなわち、例えば図13(b)に示すような広い埋め込み溝部を形成すると、埋め込み溝部に酸化珪素膜を埋め込んだ後、CMP法により基板全体を平坦化する際に、パターン依存性のため埋め込み溝部に埋め込まれた酸化珪素膜が凹状に研磨されて平坦度が悪化する等の不具合が生じる。図12(a)～(g)に示すような半導体装置の製造方法は、斯かるパターン依存性に起因する不具合を防止するべく提案されているものである。

【0014】

【発明が解決しようとする課題】

ところで、図12(f)に示す工程において、活性領域6内のゲート電極4やソース・ドレイン5等には砒素イオン、燐、硼素などの不純物イオンが注入される。しかし、活性領域6以外の領域では、マスクの合わせズレを考慮して素子分離領域まで若干拡大して導入されることはあっても、原則として不純物イオンの注入は行われない。したがって、各埋め込み溝部8間のダミーの半導体部9には不純物イオンは注入されない。

【0015】

ここで、図13(a)に示すような細分割された埋め込み溝部8及びダミーの半導体部9とを有するトレンチ分離型半導体装置と、図13(b)に示すようなダミーの半導体部のない広い分離絶縁膜例えばLOCOS膜100を有する半導体装置とにおける配線-基板間容量について説明する。ただし、図13(a)、(b)に示すいずれの構造においても、ソース・ドレイン注入時に素子分離領域7には不純物イオンが注入されておらず、かつ素子分離領域7全体の面積は等しいと仮定する。

【0016】

図13(a)に示す半導体装置においては、全配線-基板間容量 C_{at} は容量 C_{a1} と C_{a2} の総和として表される。つまり、下記式(1)

$$C_{at} = \Sigma C_{a1} + \Sigma C_{a2} \quad (1)$$

により表される。ところで、配線－基板間の単位面積当たりの容量は、両者間に存在する部材が均質な材料により構成されている場合には、配線－基板間の距離に反比例し、距離が短いほど容量は大きくなる。そのため、図13(a)に示す寸法 D_{a2} と図13(b)に示す寸法 D_{bt} が等しい場合、図13(b)に示す半導体装置における配線－基板間の全容量を C_{bt} とすると、

$$C_{at} > C_{bt} \quad (2)$$

なる関係が成立する。つまり、図13(a)に示す構造における配線－基板間の容量 C_{at} は、図13(b)に示す構造における配線基板間の容量 C_{bt} よりも大きくなってしまう。

【0017】

このように、素子分離領域にダミーの半導体部からなる凸状パターンを形成すると、面内均一性のよい平坦化を行うことができるという利点はあるものの、反面、配線－基板間容量が増大し、その結果、半導体装置の動作速度が低下するおそれがあった。

【0018】

本発明に係る点に着目してなされたものであり、一般的に、平行平板キャパシターにおいて、電極面積が等しければ電極間距離が長いほどキャパシターの容量は小さくなるという原理、或いは同じキャパシター容量でも電極間電圧が低ければ蓄積電荷量は少ないという物理現象に着目して創案したものである。

【0019】

すなわち、本発明の第1の目的は、埋め込み溝部とダミーの半導体部とからなる素子分離領域を備えたトレンチ分離型半導体装置において、素子分離領域内における配線－基板間容量を低減しうる手段を講ずることにより、動作速度の向上を図ることにある。

【0020】

本発明の第2の目的は、埋め込み溝部とダミーの半導体部とからなる素子分離領域を備えたトレンチ分離型半導体装置において、素子分離領域内における配線－基板間に存在する容量に蓄積される電荷量を低減しうる手段を講ずることによ

り、動作速度の向上を図ることにある。

【0021】

【課題を解決するための手段】

上記第1の目的を達成するために、本発明では、請求項1、2に記載されている第1の半導体装置の製造方法に関する手段と、請求項10～13に記載されている第4の半導体装置の製造方法に関する手段と、請求項14～16に記載されている第5の半導体装置の製造方法に関する手段と、請求項17に記載されている第6の半導体装置の製造方法に関する手段と、請求項18に記載されている第7の半導体装置の製造方法に関する手段と、請求項19に記載されている第8の半導体装置の製造方法に関する手段とを講じている。

【0022】

また、上記第2の目的を達成するために、本発明では、請求項3～6に記載されている第2の半導体装置の製造方法に関する手段と、請求項7～9に記載されている第3の半導体装置の製造方法に関する手段とを講じている。

【0023】

本発明の第1の半導体装置の製造方法は、請求項1に記載されているように、第1導電型の基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、上記活性領域上に素子を形成する第3の工程と、上記素子分離領域の上記ダミーの半導体部に第2導電型不純物を導入して、上記ダミーの半導体部に少なくとも1つのPN接合部を形成する第4の工程と、基板の全面上に層間絶縁膜を形成する第5の工程と、上記層間絶縁膜の上に配線を形成する第6の工程とを備えている。

【0024】

この方法により、PN接合部を有するダミーの半導体部を備えた半導体装置が形成される。そして、配線－基板間容量のうち素子分離領域の半導体部を通る領域における容量成分は、層間絶縁膜による容量に対して、半導体部のうちPN接

合部の上方の部分の容量を直列で付加したものになり、層間絶縁膜のみによる容量よりも小さくなる。したがって、半導体装置全体の配線-基板間容量も小さくなり、動作速度の高い半導体装置が形成される。

【0025】

請求項2に記載されているように、請求項1において、上記第3の工程及び上記第4の工程では、上記活性領域上に上記素子としてのFETのゲート電極を形成した後、上記活性領域及び上記ダミーの半導体部に第2導電型不純物を導入することにより、上記活性領域には上記FETのソース・ドレインを形成する一方、上記ダミーの半導体部には1つの上記PN接合部を形成することができる。

【0026】

この方法により、一般的なFETの形成のための製造工程を利用して、ダミーの半導体部におけるPN接合部を形成するための工程を別途設けることなく、動作速度の高い半導体装置を形成することができる。

【0027】

本発明の第2の半導体装置の製造方法は、請求項3に記載されているように、基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、上記活性領域に素子を形成する第3の工程と、上記素子分離領域の上記ダミーの半導体部の上に抵抗膜を形成する第4の工程と、基板の全面上に層間絶縁膜を形成する第5の工程と、上記層間絶縁膜の上に配線を形成する第6の工程とを備えている。

【0028】

この方法により、素子分離領域において層間絶縁膜とダミーの半導体部との間に抵抗膜を備えた半導体装置が形成される。そして、半導体装置の抵抗膜を通る部分において、配線-基板間容量は小さくならなくても、抵抗膜における電圧降下により、配線-基板間容量に蓄積される電荷量が低減する。したがって、電荷の充放電に要する時間の短い、つまり動作速度の高い半導体装置が形成さ

れる。

【0029】

請求項4に記載されているように、請求項3において、上記第4の工程では、上記抵抗体膜を多結晶シリコン及び非晶質シリコンのうち少なくともいずれか一方を含む膜により構成することができる。

【0030】

請求項5に記載されているように、請求項3において、上記第4の工程では、上記抵抗体膜を少なくとも絶縁膜を挟んだ2つ以上の導体膜からなる積層膜により構成することができる。

【0031】

請求項6に記載されているように、請求項3又は4において、上記第4の工程では、上記抵抗体膜に $1 \times 10^{20} \text{ atoms} \cdot \text{cm}^{-3}$ 以下の濃度の不純物を導入することが好ましい。

【0032】

本発明の第3の半導体装置の製造方法は、請求項7に記載されているように、基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、上記活性領域に素子を形成する第3の工程と、上記ダミーの半導体部の上部にイオン注入を行って上記半導体部の上部に高抵抗層を形成する第4の工程と、基板の全面上に層間絶縁膜を形成する第5の工程と、上記層間絶縁膜の上に配線を形成する第6の工程とを備えている。

【0033】

これにより、素子分離領域において層間絶縁膜とダミーの半導体部との間に高抵抗層を備えた半導体装置が形成される。そして、請求項3と同じ作用により、配線-基板間に半導体装置の高抵抗層を通る部分において、高抵抗層における電圧降下により、配線-基板間容量に蓄積される電荷量が低減する。したがって、電荷の充放電に要する時間の短い、つまり動作速度の高い半導体装置を得ること

ができる。

【0034】

請求項8に記載されているように、請求項7において、上記第4の工程では、少なくとも酸化原子を含むイオンを注入して上記高抵抗層を形成することができる。

【0035】

請求項9に記載されているように、請求項7において、上記第4の工程では、少なくとも窒化原子を含むイオンを注入して上記高抵抗層を形成することができる。

【0036】

本発明の第4の半導体装置の製造方法は、請求項10に記載されているように、基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、上記活性領域に素子を形成する第3の工程と、上記素子分離領域の上記ダミーの半導体部の上に下敷き絶縁膜を形成する第4の工程と、基板の全面上に層間絶縁膜を形成する第5の工程と、上記層間絶縁膜の上に配線を形成する第6の工程とを備えている。

【0037】

この方法により、素子分離領域において層間絶縁膜の下方に下敷き絶縁膜を備えた半導体装置が形成される。したがって、配線-基板間容量のうち素子分離領域の半導体部を通る領域における容量成分は、層間絶縁膜の容量に対して下敷き絶縁膜の容量が直列に付加された容量となるので、全体としての配線-基板間容量が小さくなる。すなわち、動作速度の高い半導体装置を得ることができる。

【0038】

請求項11に記載されているように、請求項10において、上記第3の工程及び上記第4の工程では、上記活性領域上に上記素子となるFETのゲート電極を形成した後、基板上に誘電体膜を堆積して、上記素子分離領域上を覆うマスクを

用いてこの誘電体膜の異方性エッチングを行うことにより、上記ゲート電極の側面上にはサイドウォールを、上記ダミーの半導体部の上には上記下敷き絶縁膜をそれぞれ残すことができる。

【0039】

この方法により、ゲート電極の側面上にサイドウォールを備えたFETの一般的な製造工程を利用しながら、下敷き絶縁膜を形成するための工程を別途設けることなく、動作速度の高い半導体装置を形成することができる。

【0040】

請求項12に記載されているように、請求項10又は11において、上記第4の工程では、少なくとも酸化珪素を含む誘電体膜により上記下敷き絶縁膜を形成することができる。

【0041】

請求項13に記載されているように、請求項10又は11において、上記第4の工程では、少なくとも窒化珪素を含む誘電体膜により上記下敷き絶縁膜を形成することができる。

【0042】

本発明の第5の半導体装置の製造方法は、請求項14に記載されているように、基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、上記活性領域に素子を形成する第3の工程と、上記ダミーの半導体部をエッチングにより除去して第3の溝を形成し、上記第3の溝内に絶縁性材料を埋め込んで上記第1及び第2の埋め込み溝部と共通の上面位置を有する埋め込み絶縁膜を形成する第4の工程と、基板の全面上に層間絶縁膜を形成する第5の工程と、上記層間絶縁膜の上に配線を形成する第6の工程とを備えている。

【0043】

この方法により、素子分離領域において層間絶縁膜とダミーの半導体部との間に埋め込み絶縁膜を備えた半導体装置が形成される。したがって、配線-基板間

容量のうち素子分離領域の半導体部を通る領域における容量成分は、層間絶縁膜の容量に対して埋め込み絶縁膜の容量が直列に付加された容量となるので、全体としての配線-基板間容量が小さくなる。すなわち、動作速度の高い半導体装置を得ることができる。

【0044】

請求項15に記載されているように、請求項14において、上記第4の工程では、少なくとも酸化珪素を含む誘電体膜により上記埋め込み絶縁膜を形成することができる。

【0045】

請求項16に記載されているように、請求項14において、上記第4の工程では、少なくとも窒化珪素を含む誘電体膜により上記埋め込み絶縁膜を形成することができる。

【0046】

本発明の第6の半導体装置の製造方法は、請求項17に記載されているように、基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数のダミーの半導体部に分割する第2の溝とを形成する第1の工程と、上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、上記活性領域に素子を形成する第3の工程と、上記ダミーの半導体部の内部に酸素イオンの注入を行って上記半導体部の奥方に埋め込み絶縁膜を形成する第4の工程と、基板の全面上に層間絶縁膜を形成する第5の工程と、上記層間絶縁膜の上に配線を形成する第6の工程とを備えている。

【0047】

本発明の第7の半導体装置の製造方法は、請求項18に記載されているように、基板領域を有する半導体基板に、上記基板領域を活性領域と素子分離領域とに区画する第1の溝と、上記素子分離領域を複数の半導体部に分割する第2の溝とを形成する第1の工程と、上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第2の工程と、上記半導体部をエッチングにより除去して第3の溝を形成し、上記第3の溝内に絶縁

性材料を埋め込んで上記第1及び第2の埋め込み溝部よりも低い上面位置を有する埋め込み絶縁膜を形成する第3の工程と、上記活性領域をマスク部材で覆った状態で上記埋め込み絶縁膜の上に半導体膜を成長させてダミーの半導体部を形成する第4の工程と、上記活性領域の上に素子を形成する第5の工程と、基板の全面上に層間絶縁膜を形成する第6の工程と、上記層間絶縁膜の上に配線を形成する第7の工程とを備えている。

【0048】

本発明の第8の半導体装置の製造方法は、請求項19に記載されているように、基板領域を有する半導体基板に、上記基板領域のうち素子分離領域全体に亘る第1の溝を形成し、上記基板領域のうち活性領域を残す第1の工程と、上記第1の溝に絶縁性材料を埋め込んで上記素子形成領域と共通の上面位置を有する埋め込み絶縁膜を形成する第2の工程と、上記活性領域及び上記埋め込み絶縁膜の上に半導体膜を成長させる第3の工程と、半導体基板基板に、上記半導体膜及び上記基板領域を活性領域と素子分離領域とに区画する第2の溝と、上記素子分離領域の半導体膜を複数のダミーの半導体部に分割する第3の溝とを形成する第4の工程と、上記第1及び第2の溝に絶縁性材料を埋め込んで第1の埋め込み溝部と第2の埋め込み溝部とをそれぞれ形成する第5の工程と、上記活性領域上の上記半導体膜の上に素子を形成する第6の工程と、基板の全面上に層間絶縁膜を形成する第7の工程と、上記層間絶縁膜の上に配線を形成する第8の工程とを備えている。

【0049】

請求項17、18又は19により、素子分離領域においてダミーの半導体部の奥方に埋め込み絶縁膜を備えた半導体装置が得られる。したがって、請求項14と同様の作用が得られ、動作速度の高い半導体装置が得られる。

【0050】

【発明の実施の形態】

(第1の実施形態)

図1(a)～(g)は、第1の実施形態にかかるNMOSFETを有する半導体装置の製造工程における構造を示す断面図である。

【0051】

図1(a)に示す工程では、P型シリコン基板1の上に、厚さ10nmの薄い酸化珪素膜21と窒化珪素膜22とを順次形成する。

【0052】

図1(b)に示す工程では、シリコン基板1に所定幅の複数の溝14を形成する。ただし、これらの溝14には、素子が形成される活性領域6を取り囲むように形成された溝14aと、この溝によって活性領域と区画される素子分離領域7に形成される仕上りの平坦性のパターン依存性を解消するための溝14bと、多結晶シリコン配線を形成するための溝14cとがある。そして、素子分離領域7内にも、上記溝14によって囲まれる1つ以上の凸部となる半導体部9が形成されている。この半導体部9は、活性領域としては機能しないダミーの活性領域ともいふべきものである。さらに、後の工程で形成される多結晶シリコン配線10の直下にも溝を形成する。

【0053】

図1(c)に示す工程では、基板の全面上に酸化珪素膜23を堆積し、各溝14を酸化珪素膜で埋め込む。

【0054】

図1(d)に示す工程では、CMP法を用いて酸化珪素膜23を研磨する。続いて、窒化珪素膜22と酸化珪素膜21を除去し、表面が平坦で酸化珪素膜が埋め込まれた埋め込み溝部8を形成する。この埋め込み溝部8のうち埋め込み溝部8aが素子分離として機能するものであり、埋め込み溝部8bはダミーの半導体部9を形成するものであり、埋め込み溝部8cが多結晶シリコン配線とシリコン基板とを絶縁する機能を有するものである。

【0055】

図1(e)に示す工程では、周知の技術を用いてゲート酸化膜2と、側面上にサイドウォール24を有するゲート電極4と、多結晶シリコン配線10とを形成する。ゲート電極4と多結晶シリコン配線10とは同一の半導体マスクを用いて同時に形成することが可能である。

【0056】

図1(f)に示す工程では、活性領域6だけでなく素子分離領域7全体にも砒素イオン25を注入する。この工程により、活性領域6にはソース・ドレイン5を有するNMOSFETが形成される。一方、素子分離領域7のダミーの半導体部6内には、N型不純物拡散層31が形成され、このN型不純物拡散層31とP型シリコン基板1との間にPN接合部32が形成されている。このPN接合部32は埋め込み溝部8の上面と底面との間にある。この点为本実施形態の特徴部分である。

【0057】

図1(g)に示す工程では、酸化珪素膜を堆積して層間絶縁膜12を形成し、さらにその上にメタル配線13を形成する。

【0058】

図2は、本実施形態に係る半導体装置の素子分離領域7における配線-基板間容量を説明するための断面図である。同図に示すように、本実施形態に係る半導体装置の配線-基板間容量には、図13(a)に示す従来の半導体装置における配線-基板間容量と同様に、容量Ca1と容量Ca2の成分が存在する。さらに、本実施形態では、半導体部9内にPN接合部32が形成されるため、新たな容量Cj1が容量Ca1に対して直列に付加される。よって、全配線-基板間容量Cjtは、下記式(3)

$$C_{jt} = \Sigma \{ (Ca1 \times Cj1) / (Ca1 + Cj1) \} + \Sigma Ca2 \quad (3)$$

により表され、式(1)で表わされる全容量Catより小さくなる。すなわち、下記式(4)

$$C_{jt} < Cat \quad (4)$$

が成り立つ。

【0059】

したがって、本実施形態の半導体装置によると、素子分離領域7内のダミーの半導体部9内にPN接合部32が存在するために、配線-基板間容量を低減することが可能になり、半導体装置の動作速度の向上を図ることができる。

【0060】

また、本実施形態のごとく、活性領域にMOSFETを設ける場合、半導体部9のPN接合部32は、ソース・ドレイン5を形成する際の不純物イオンの注入によって容易に形成できるので、製造コストの増大を招くこともない。

【0061】

なお、本実施形態ではP型シリコン基板を用いた場合を述べたが、N型シリコン基板を用いる場合は、埋め込み溝部の間の半導体部の上部にP型の不純物を導入することで、N型シリコン基板との間にPN接合部が形成されるので、本実施形態と同様の効果が得られることはいうまでもない。

【0062】

本実施形態では、素子分離領域7内のダミーの半導体部9におけるPN接合部32の形成をソース・ドレイン5の形成と同時に行っているが、ダミーの半導体部内にPN接合部の形成が可能であれば、半導体装置の製造工程中のどの段階で行っても構わない。

【0063】

また、本実施形態ではPN接合部が1層構造で存在する場合を述べたが、2層以上の場合も同様に表わせ、半導体部9にPN接合部がm層構造を、さらに埋め込み溝部8a, 8b, 8c直下にn層構造をなしているとすると、全配線-基板間容量Cjtは、下記式(5)

$$C_{jt} = \Sigma \{ 1 / [(1 / C_{a1}) + \Sigma (1 / C_{jm})] \} \\ + \Sigma \{ 1 / [(1 / C_{a2}) + \Sigma (1 / C_{jn})] \} \quad (5)$$

により表され、式(1)で表わされる全容量Catより小さくなる。ただし、Ck1は埋め込み溝部の底面とPN接合部との間の容量である。すなわち、上記第1の実施形態と同様に、下記式(6)

$$C_{jt} < C_{at} \quad (6)$$

が成立する。

【0064】

すなわち、素子分離領域7内の半導体部9に少なくとも1つのPN接合部が存在することにより、各容量が直列に接続されるため配線-基板間容量を低減する

ことが可能になり、半導体装置の速度向上に寄与する。

【0065】

(第2の実施形態)

図3(a)～(h)は、第2の実施形態にかかるNMOSFETを有する半導体装置の製造工程における構造を示す断面図である。。

【0066】

図3(a)に示す工程では、P型シリコン基板1上に、厚さ10nmの薄い酸化珪素膜21と窒化珪素膜22とを順次形成する。

【0067】

図3(b)に示す工程では、シリコン基板1に所定幅の複数の溝14を形成する。ただし、これらの溝14には、素子が形成される活性領域6を取り囲むように形成された溝14aと、この溝によって活性領域と区画される素子分離領域7に形成される仕上りの平坦性のパターン依存性を解消するための溝14bと、多結晶シリコン配線を形成するための溝14cとがある。そして、素子分離領域7内にも、上記溝14によって囲まれる1つ以上の凸部となる半導体部9が形成されている。この半導体部9は、活性領域としては機能しないダミーの活性領域ともいふべきものである。さらに、後の工程で形成される多結晶シリコン配線10の直下にも溝を形成する。

【0068】

図3(c)に示す工程では、基板の全面上に酸化珪素膜23を堆積し、溝14を酸化珪素膜で埋め込む。

【0069】

図3(d)に示す工程では、CMP法を用いて酸化珪素膜23を研磨する。続いて、窒化珪素膜22と酸化珪素膜21を除去し、表面が平坦で酸化珪素膜で埋め込まれた複数の埋め込み溝部8を形成する。この埋め込み溝部8のうち埋め込み溝部8aが素子分離として機能するものであり、埋め込み溝部8bはダミーの半導体部9を形成するものであり、埋め込み溝部8cが多結晶シリコン配線とシリコン基板とを絶縁する機能を有するものである。

【0070】

図3(e)に示す工程では、周知の技術を用いて、ゲート酸化膜2と、側面上にサイドウォール24を有するゲート電極4と、多結晶シリコン配線10を形成する。そして、このゲート電極4及び多結晶シリコン配線10と共に、ゲート電極4および多結晶シリコン配線10とは一定の距離をおいて離れ、かつお互いに交差もしくは接することはないダミーゲート51を形成する。ゲート電極4、多結晶シリコン配線10及びダミーゲート51は同一の半導体マスクで同時に形成することが可能である。ここで、ダミーゲート51は、配線として使われるゲート電極や多結晶シリコン配線10よりシート抵抗が高く、不純物濃度は $1 \times 10^{20} \text{ atoms} \cdot \text{cm}^{-3}$ 以下になるようイオン注入法などで不純物濃度が調整されている。

【0071】

図3(f)に示す工程では、素子分離領域7の上方に、酸化珪素膜52と、多結晶シリコンからなる高抵抗膜53を形成する。ここで高抵抗膜53は、配線として使われるゲート電極4や多結晶シリコン配線10よりシート抵抗が高く、不純物濃度は $1 \times 10^{20} \text{ atoms} \cdot \text{cm}^{-3}$ 以下になるようイオン注入法などで不純物濃度が調整されている。なお、酸化珪素膜52、高抵抗膜53は、MIMキャパシタや抵抗体を設けるために形成される。

【0072】

図3(g)に示す工程では、少なくとも素子分離領域7を覆うレジストマスク55を形成し、活性領域6に砒素イオン25を注入して、ソース・ドレイン5を有するNMOSを形成する。このとき、素子分離領域7には砒素イオンの注入は行わない。

【0073】

図3(h)に示す工程では、酸化珪素膜を堆積して層間絶縁膜12を形成し、さらにその上にメタル配線13を形成する。

【0074】

本実施形態の製造方法によって形成される半導体装置においては、配線-基板間の容量ではなく配線-高抵抗膜間の容量を考慮すればよい。その場合、高抵抗

膜53を構成する多結晶シリコン膜の抵抗が高いために、高抵抗膜53の上端とシリコン基板1の表面との間で電圧降下が起こる。したがって、層間絶縁膜12自体の容量は変わらないが、層間絶縁膜の両端に印加される電圧が低い。層間絶縁膜12の両側に蓄えられる電荷量は電圧に比例して減少するので、配線-高抵抗膜間における電荷の充放電に要する時間が短くなり、半導体装置の動作速度が向上する。

【0075】

本実施形態における高抵抗膜53は、例えば抵抗素子の高抵抗膜やローカル配線と共通の膜からパターニングすることにより容易かつ安価に形成することができる。また、ダミーゲート51の代わりに、半導体基板上のいずれかにMIMキャパシタを形成する際に使用する上層膜、容量絶縁膜及び下層膜を構成する3つの膜から上記高抵抗膜53、酸化珪素膜52及びダミーゲート51に相当する膜を形成することも可能である。

【0076】

さらに、上記ダミーゲート51及び高抵抗膜53のうちいずれか一方と酸化珪素膜52とを形成しなくても、電荷の充放電に要する時間の低減による半導体装置の動作速度の向上を図ることは可能である。

【0077】

なお、ここでは素子分離領域7上に高抵抗膜53を構成する多結晶シリコン膜と酸化珪素膜52との積層膜が存在する場合を述べたが、多結晶シリコン膜の代わりに非晶質シリコン膜を用いた場合でも同様の効果がある。

【0078】

(第3の実施形態)

図4は第3の実施形態にかかるNMOSFETを有する半導体装置の製造工程における構造を示す断面図である。

【0079】

図4(a)に示す工程では、P型シリコン基板1の上に、厚さ10nmの薄い酸化珪素膜21と窒化珪素膜22とを順次形成する。

【0080】

図4 (b) に示す工程では、シリコン基板1に所定幅の複数の溝14を形成する。ただし、これらの溝14には、素子が形成される活性領域6を取り囲むように形成された溝14aと、この溝によって活性領域と区画される素子分離領域7に形成される仕上りの平坦性のパターン依存性を解消するための溝14bと、多結晶シリコン配線を形成するための溝14cとがある。そして、素子分離領域7内にも、上記溝14によって囲まれる1つ以上の凸部となる半導体部9が形成されている。この半導体部9は、活性領域としては機能しないダミーの活性領域ともいふべきものである。さらに、後の工程で形成される多結晶シリコン配線10の直下にも溝を形成する。

【0081】

図4 (c) に示す工程では、基板の全面上に酸化珪素膜23を堆積し、溝14を酸化珪素膜で埋め込む。

【0082】

図4 (d) に示す工程では、CMP法を用いて酸化珪素膜23を研磨する。続いて、窒化珪素膜22と酸化珪素膜21を除去し、表面が平坦で酸化珪素膜が埋め込まれた埋め込み溝部8を形成する。この埋め込み溝部8のうち埋め込み溝部8aが素子分離として機能するものであり、埋め込み溝部8bはダミーの半導体部9を形成するものであり、埋め込み溝部8cが多結晶シリコン配線とシリコン基板とを絶縁する機能を有するものである。

【0083】

図4 (e) に示す工程では、素子分離領域7中の半導体部9をドライエッチングにより除去し、溝62を形成する。

【0084】

図4 (f) に示す工程では、溝62に酸化珪素膜を埋め込んで埋め込み絶縁膜61を形成する。

【0085】

図4 (g) に示す工程では、周知の技術を用いてゲート酸化膜2と、側面上にサイドウォール24を有するゲート電極4と、多結晶シリコン配線10とを形成

する。ゲート電極4と多結晶シリコン配線10とは同一の半導体マスクを用いて同時に形成することが可能である。

【0086】

図4(h)に示す工程では、上方から砒素イオン25を注入し、活性領域6にソース・ドレイン5を有するNMOSFETを形成する。このとき素子分離領域7に、砒素イオン25が注入されるが、不具合は生じない。もっとも、PMOSFET形成領域を覆うレジストマスクを使用する場合には、このレジストマスクにより素子分離領域7を覆っておいてもよい。

【0087】

図4(i)に示す工程では、酸化珪素膜を堆積して層間絶縁膜12を形成し、さらにその上にメタル配線13を形成する。

【0088】

本実施形態の製造方法によって形成される半導体装置においては、素子分離領域7内のダミーの半導体部9の上方かつ層間絶縁膜12の下方には、酸化珪素膜からなる埋め込み絶縁膜61が埋め込み溝部8に囲まれるように形成されている。この埋め込み絶縁膜61の上面は埋め込み溝部8の上面と同じ高さ位置にあり、埋め込み絶縁膜61の下端は埋め込み溝部8の上面と底面との間の高さ位置にある。

【0089】

したがって、本実施形態の半導体装置においては、ダミーの半導体部9が掘り下げられ、酸化珪素膜で埋め込まれた埋め込み絶縁膜61が形成されているので、図13(a)に示す従来の半導体装置に比べ、配線-基板間距離が長い。配線-基板間容量は距離に反比例して小さくなるので、本実施形態の半導体装置の配線-基板間容量は従来の半導体装置における配線-基板間容量よりも低減され、半導体装置の動作速度の向上を図ることができる。

【0090】

なお、本実施形態においては、半導体部に酸化珪素膜が埋め込まれた例について説明したが、窒化珪素膜などの絶縁膜を用いても同様の効果が得られる。

【0091】

さらに、本実施形態においては、ゲート電極形成前に半導体部9の掘り下げと酸化珪素膜の埋め込みを行っているが、本発明の半導体装置の製造方法はかかる実施形態に限定されるものではない。すなわち、半導体部9の掘り下げ工程と酸化珪素膜の埋め込み工程とをゲート電極の形成後、あるいは、トレンチ分離の形成前に行っても、本実施形態と同様の効果がある。

【0092】

(第4の実施形態)

図5(a)～(h)は、第4の実施形態にかかるNMOSFETを有する半導体装置の製造工程における構造を示す断面図である。

【0093】

図5(a)に示す工程では、P型シリコン基板1の上に、厚さ10nmの薄い酸化珪素膜21と窒化珪素膜22とを順次形成する。

【0094】

図5(b)に示す工程では、シリコン基板1に所定幅の複数の溝14を形成する。ただし、これらの溝14には、素子が形成される活性領域6を取り囲むように形成された溝14aと、この溝によって活性領域と区画される素子分離領域7に形成される仕上りの平坦性のパターン依存性を解消するための溝14bと、多結晶シリコン配線を形成するための溝14cとがある。そして、素子分離領域7内にも、上記溝14によって囲まれる1つ以上の凸部となる半導体部9が形成されている。この半導体部9は、活性領域としては機能しないダミーの活性領域ともいふべきものである。さらに、後の工程で形成される多結晶シリコン配線10の直下にも溝を形成する。

【0095】

図5(c)に示す工程では、基板の全面上に酸化珪素膜23を堆積し、溝14を酸化珪素膜で埋め込む。

【0096】

図5(d)に示す工程では、CMP法を用いて酸化珪素膜23を研磨する。続いて、窒化珪素膜22と酸化珪素膜21を除去し、表面が平坦で酸化珪素膜が埋

め込まれた埋め込み溝部 8 を形成する。この埋め込み溝部 8 のうち埋め込み溝部 8 a が素子分離として機能するものであり、埋め込み溝部 8 b はダミーの半導体部 9 を形成するものであり、埋め込み溝部 8 c が多結晶シリコン配線とシリコン基板とを絶縁する機能を有するものである。

【0097】

図 5 (e) に示す工程では、活性領域 6 を覆うレジストマスク 7 3 を形成した後、素子分離領域 7 のみに酸素イオン 7 2 の注入を行い、素子分離領域 7 の半導体部 9 内に酸素原子が不純物として導入された高抵抗層 7 1 をシリコン基板の最表面に形成する。

【0098】

図 5 (f) に示す工程では、周知の技術を用いてゲート酸化膜 2 と、側面上にサイドウォール 2 4 を有するゲート電極 4 と、多結晶シリコン配線 1 0 とを形成する。ゲート電極 4 と多結晶シリコン配線 1 0 とは同一の半導体マスクを用いて同時に形成することが可能である。

【0099】

図 5 (g) に示す工程では、基板の上方から砒素イオンの注入を行い、活性領域 6 に、ソース・ドレイン 5 を有する NMOSFET を形成する。このとき、素子分離領域 7 にも砒素イオン 2 5 が注入されるが、不具合は生じない。もっとも、PMOSFET 形成領域を覆うレジストマスクを使用する場合には、このレジストマスクにより素子分離領域 7 を覆っておいてもよい。

【0100】

図 5 (h) に示す工程では、層間絶縁膜として酸化珪素膜 1 2 を形成し、メタル配線 1 3 を形成する。

【0101】

本実施形態の製造方法によって形成される半導体装置の特徴は、素子分離領域 7 内のダミーの半導体部 9 の上部に酸素原子がイオン注入などによって導入され、高抵抗のシリコン層からなる高抵抗層 7 1 が形成されている点である。この高抵抗層 7 1 の下端の高さ位置は、埋め込み溝部 8 の上面と底面との間にあるが、埋め込み溝部 8 の底面よりも下方に位置していてもよい。

【0102】

本実施形態に係る半導体装置においては、ダミーの半導体部9のシリコン基板にイオン注入などにより酸素原子が導入され高抵抗のシリコン層からなる高抵抗層71が形成されているために、配線-基板間に電圧が印加された場合に高抵抗層71において電圧降下が生じる。したがって、配線-半導体部9間の電位差が小さくなり、配線-半導体部9間の層間絶縁膜12自体の容量は、図13(a)に示す従来の半導体装置における層間絶縁膜12の容量と変わらないが、蓄積電荷量は電圧に比例して減少する。したがって、容量に対する電荷の充放電に要する時間が短くなり、半導体装置の動作速度が向上する。

【0103】

なお、本実施形態においては、ダミーの半導体部9に導入された不純物が酸素原子の例について説明したが、窒素原子を導入しても同様の効果が得られる。

【0104】

なお、本実施形態においては、半導体部9に導入された不純物が酸素原子の例について説明したが、窒素原子を導入しても同様の効果が得られる。

【0105】

さらに、本実施形態においては、ゲート電極の形成前に高抵抗層の形成を行っているが、半導体部への酸素原子の導入が可能であれば半導体装置の製造工程のどの段階で行っても構わない。

【0106】

(第5の実施形態)

図6(a)～(i)は、第5の実施形態にかかるNMOSFETを有する半導体装置の製造工程における構造を示す断面図である。

【0107】

図6(a)に示す工程では、P型シリコン基板1の上に、厚さ10nmの薄い酸化珪素膜21と窒化珪素膜22とを順次形成する。

【0108】

図6(b)に示す工程では、シリコン基板1に所定幅の複数の溝14を形成する。ただし、これらの溝14には、素子が形成される活性領域6を取り囲むよう

に形成された溝14aと、この溝によって活性領域と区画される素子分離領域7に形成される仕上がりの平坦性のパターン依存性を解消するための溝14bと、多結晶シリコン配線を形成するための溝14cとがある。そして、素子分離領域7内にも、上記溝14によって囲まれる1つ以上の凸部となる半導体部9が形成されている。この半導体部9は、活性領域としては機能しないダミーの活性領域ともいふべきものである。さらに、後の工程で形成される多結晶シリコン配線10の直下にも溝を形成する。

【0109】

図6(c)に示す工程では、基板の全面上に酸化珪素膜23を堆積し、溝14を酸化珪素膜で埋め込む。

【0110】

図6(d)に示す工程では、CMP法を用いて酸化珪素膜23を研磨する。続いて、窒化珪素膜22と酸化珪素膜21を除去し、表面が平坦で酸化珪素膜が埋め込まれた埋め込み溝部8を形成する。この埋め込み溝部8のうち埋め込み溝部8aが素子分離として機能するものであり、埋め込み溝部8bはダミーの半導体部9を形成するものであり、埋め込み溝部8cが多結晶シリコン配線とシリコン基板とを絶縁する機能を有するものである。

【0111】

図6(e)に示す工程では、周知の技術を用いてゲート酸化膜2と、多結晶シリコンからなるゲート電極4と、多結晶シリコン配線10とを形成する。ゲート電極4と多結晶シリコン配線10とは同一の半導体マスクを用いて同時に形成することが可能である。

【0112】

図6(f)に示す工程では、酸化珪素膜82を基板全面に堆積し、酸化珪素膜82の上に、素子分離領域7を覆うレジストマスク84を形成する。

【0113】

図6(g)に示す工程では、レジストマスク84を用いた異方性ドライエッチングにより酸化珪素膜82の一部を選択的に除去し、素子分離領域7の上方に下敷き絶縁膜81を形成するとともに、ゲート電極4の側面上にサイドウォール2

4を形成する。ただし、多結晶シリコン配線10は周囲を下敷き絶縁膜81で覆われている。

【0114】

図6(h)に示す工程では、上方から砒素イオン25の注入を行い、活性領域6に、ソース・ドレイン5を有するNMOSFETを形成する。このとき素子分離領域7にも砒素イオン25が注入されるが不具合は生じない。もっとも、PMOSFET形成領域を覆うレジストマスクを使用する場合には、このレジストマスクにより素子分離領域7を覆っておいてもよい。

【0115】

図6(i)に示す工程では、酸化珪素膜を堆積して層間絶縁膜12を形成し、さらにその上にメタル配線13を形成する。

【0116】

本実施形態の製造方法によって形成された半導体装置においては、素子分離領域7内のダミーの半導体部9及び埋め込み溝部8に跨って、ゲート電極4の側面上のサイドウォール24と同時に形成された酸化珪素膜からなる下敷き絶縁膜81が形成されている点が特徴である。この下敷き絶縁膜81は、多結晶シリコン配線10全体を覆うように形成されている。

【0117】

本実施形態の半導体装置によると、素子分離領域7の上には酸化珪素膜からなる下敷き絶縁膜81が存在しているので、図13(a)に示す従来の半導体装置に比べ、配線-基板間距離が長い。配線-基板間容量は距離に反比例して小さくなるために、本実施形態の半導体装置では配線-基板間容量が低減され、よって、動作速度の向上を図ることができる。

【0118】

なお、本実施形態においては、下敷き絶縁膜81を酸化珪素膜により構成した例について説明したが、窒化珪素膜などの絶縁膜を用いても同様の効果が得られる。

【0119】

また、本実施形態においては下敷き絶縁膜が単層膜である場合について説明し

たが、下敷き絶縁膜は単層膜である必要はなく、積層膜であってもよい。例えば、サイドウォールがゲート電極の側面から基板上に跨るL字状の部分とその上のくさび状の部分とからなるものであったり、ゲート上保護膜とサイドウォールとを設けた場合などには、下敷き絶縁膜も積層膜となる。かかる場合にも本実施形態と同様の効果を発揮しうることはいうまでもない。

【0120】

(第6の実施形態)

図7(a)～(h)は、第6の実施形態にかかるNMOSFETを有する半導体装置の製造工程における構造を示す断面図である。

【0121】

図7(a)に示す工程では、P型シリコン基板1の上に、厚さ10nmの薄い酸化珪素膜21と窒化珪素膜22とを順次形成する。

【0122】

図7(b)に示す工程では、シリコン基板1に所定幅の複数の溝14を形成する。ただし、これらの溝14には、素子が形成される活性領域6を取り囲むように形成された溝14aと、この溝によって活性領域と区画される素子分離領域7に形成される仕上りの平坦性のパターン依存性を解消するための溝14bと、多結晶シリコン配線を形成するための溝14cとがある。そして、素子分離領域7内にも、上記溝14によって囲まれる1つ以上の凸部となる半導体部9が形成されている。この半導体部9は、活性領域としては機能しないダミーの活性領域ともいふべきものである。さらに、後の工程で形成される多結晶シリコン配線10の直下にも溝を形成する。

【0123】

図7(c)に示す工程では、基板の全面上に酸化珪素膜23を堆積し、溝14を酸化珪素膜で埋め込む。

【0124】

図7(d)に示す工程では、CMP法を用いて酸化珪素膜23を研磨する。続いて、窒化珪素膜22と酸化珪素膜21を除去し、表面が平坦で酸化珪素膜が埋め込まれた埋め込み溝部8を形成する。この埋め込み溝部8のうち埋め込み溝部

8aが素子分離として機能するものであり、埋め込み溝部8bはダミーの半導体部9を形成するものであり、埋め込み溝部8cが多結晶シリコン配線とシリコン基板とを絶縁する機能を有するものである。

【0125】

図7(e)に示す工程では、活性領域6を覆うレジストマスク92を形成し、素子分離領域7のみに酸素イオン93の注入を行い、酸素原子が不純物として導入された埋め込み絶縁膜91を形成する。この埋め込み絶縁膜91によって、素子分離領域7において、シリコン基板1と半導体部9とが絶縁される。このとき、埋め込み絶縁膜91は、各埋め込み溝部8a～8cと側面で接続され、半導体部9はフローティング状態になるように酸素イオン注入時のエネルギーを設定する。

【0126】

図7(f)に示す工程では、周知の技術を用いてゲート酸化膜2と、側面上にサイドウォール24を有するゲート電極4と、多結晶シリコン配線10とを形成する。ゲート電極4と多結晶シリコン配線10とは同一の半導体マスクを用いて同時に形成することが可能である。

【0127】

図7(g)に示す工程では、素子分離領域7を覆うレジストマスク95を形成した後、活性領域6に砒素イオン25の注入を行い、ソース・ドレイン5を有するNMOSFETを形成する。このとき素子分離領域7には注入は行わない。

【0128】

図7(h)に示す工程では、酸化珪素膜を堆積して層間絶縁膜12を形成し、さらにその上にメタル配線13を形成する。

【0129】

本実施形態の製造方法によって形成される半導体装置において、上記ダミーの半導体部9及び埋め込み溝部8の下方には、酸化珪素膜からなる埋め込み絶縁膜91が埋め込み溝部8の下端に接して形成されている。その結果、半導体部9の側面は埋め込み溝部8に、半導体部9の底面は埋め込み絶縁膜91に接している。

【0130】

図8は、本実施形態に係る半導体装置の配線-基板間容量を説明するための断面図である。本実施形態に係る半導体装置によると、シリコン基板下に酸化珪素膜からなる埋め込み絶縁膜91を形成しているので、容量 C_{ij} は、図2に示す容量 C_{j1} の2分の1以下になる (T. Nishimura and Y. Inoue: Proceedings of VLSI TECHNOLOGY WORKSHOP ON "WHAT IS THE FUTURE OF SOI?" (1995) p.123)

【0131】

したがって、半導体装置の全配線-基板間容量 C_{ijt} は、下記式(7)

$$C_{ijt} = \sum \{ (C_{a1} \times C_{ij}) / (C_{a1} + C_{ij}) \} + \sum C_{a2} \quad (7)$$

で表され、式(3)で表わされる全容量 C_{jt} より小さくなる。すなわち、下記式(8)

$$C_{ijt} < C_{jt} \quad (8)$$

が成立する。よって、上述の式(4)の関係より

$$C_{ijt} < C_{at}$$

となり、本実施形態に係る半導体装置の配線-基板間容量が小さくなるので、半導体装置の動作速度が向上する。

【0132】

なお、本実施形態においては、ゲート電極の形成前に酸素イオンの注入を行って埋め込み絶縁膜を形成しているが、半導体部への酸素原子の導入が可能であれば半導体装置の製造工程中のどの段階で行っても構わない。

【0133】

(第7の実施形態)

図9(a)～(i)は、第7の実施形態にかかるNMOSFETを有する半導体装置の製造工程における構造を示す断面図である。

【0134】

図9(a)に示す工程では、P型シリコン基板1の上に、厚さ10nmの薄い酸化珪素膜21と窒化珪素膜22とを順次形成する。

【0135】

図9(b)に示す工程では、シリコン基板1に所定幅の複数の溝14を形成する。ただし、これらの溝14には、素子が形成される活性領域6を取り囲むように形成された溝14aと、この溝によって活性領域と区画される素子分離領域7に形成される仕上りの平坦性のパターン依存性を解消するための溝14bと、多結晶シリコン配線を形成するための溝14cとがある。そして、素子分離領域7内にも、上記溝14によって囲まれる1つ以上の凸部となる半導体部9が形成されている。さらに、後の工程で形成される多結晶シリコン配線10の直下にも溝を形成する。

【0136】

図9(c)に示す工程では、基板の全面上に酸化珪素膜23を堆積し、溝14を酸化珪素膜で埋め込む。

【0137】

図9(d)に示す工程では、CMP法を用いて酸化珪素膜23を研磨する。続いて、活性領域6上以外の酸化珪素膜22と酸化珪素膜21を除去し、表面が平坦で酸化珪素膜が埋め込まれた埋め込み溝部8を形成する。この埋め込み溝部8のうち埋め込み溝部8aが素子分離として機能するものであり、埋め込み溝部8bはダミーの半導体部9を形成するものであり、埋め込み溝部8cが多結晶シリコン配線とシリコン基板とを絶縁する機能を有するものである。

【0138】

図9(e)に示す工程では、素子分離領域7中の半導体部9をドライエッチングにより除去し、溝96を形成する。

【0139】

図9(f)に示す工程では、溝96内に酸化珪素膜を堆積して埋め込み絶縁膜91を形成し、さらにその上にシリコン膜を堆積してダミーの活性領域となる半導体部97を形成する。ここで、埋め込み絶縁膜91は、埋め込み溝部8a～8cと接している。

【0140】

図9(g)に示す工程では、周知の技術を用いてゲート酸化膜2と、側面上に

サイドウォール24を有するゲート電極4と、多結晶シリコン配線10とを形成する。ゲート電極4と多結晶シリコン配線10とは同一の半導体マスクを用いて同時に形成することが可能である。

【0141】

図9(h)に示す工程では、素子分離領域7を覆うレジストマスク98を形成し、活性領域6に砒素イオン25を注入して、ソース・ドレイン5を有するNMOSFETを形成する。このとき素子分離領域7には注入は行わないが、注入してもかまわない。

【0142】

図9(i)に示す工程では、酸化珪素膜を堆積して層間絶縁膜12を形成し、さらにその上にメタル配線13を形成する。

【0143】

本実施形態の製造方法によっても、第6の実施形態に係る半導体装置と同じ構造が得られ、第6の実施形態で説明したように、配線-基板間容量が小さく、動作速度の高い半導体装置を形成することができる。

【0144】

なお、本実施形態においては、ゲート電極の形成前に、溝96への酸化珪素膜とシリコン膜の成長とを行っているが、溝96への埋め込み、成長が可能であれば半導体装置の製造工程中のどの段階で行っても構わない。

【0145】

(第8の実施形態)

図10(a)～(f)及び図11(a)～(d)は、いずれも第8の実施形態にかかるNMOSFETを有する半導体装置の製造工程における構造を示す断面図である。

【0146】

図10(a)に示す工程では、P型シリコン基板1の素子分離領域形成領域に溝102を形成する。

【0147】

図10(b)に示す工程では、溝102に酸化珪素膜を埋め込んで埋め込み絶

縁膜101を形成し、基板の表面全体を平坦化する。

【0148】

図10(c)に示す工程では、基板の全面上にシリコン膜103をエピタキシャル成長させる。このとき、活性領域6には単結晶シリコンの上に単結晶シリコンが成長するので、結晶性のよい半導体領域が形成されるが、素子分離領域7には酸化珪素膜の上にあまり結晶性のよくないシリコン膜が形成される。しかし、素子分離領域7のシリコン膜は、活性領域としては機能しないので、半導体装置の特性に悪影響を与えることはない。

【0149】

図10(d)に示す工程では、シリコン膜103の上に、厚さ10nmの薄い酸化珪素膜21と窒化珪素膜22とを順次形成する。

【0150】

図10(e)に示す工程では、基板に所定幅の複数の溝14を形成する。ただし、これらの溝14には、素子が形成される活性領域6を取り囲むように形成された溝14aと、この溝によって活性領域と区画される素子分離領域7に形成される仕上がりの平坦性のパターン依存性を解消するための溝14bと、多結晶シリコン配線を形成するための溝14cとがある。そして、素子分離領域7内にも、上記溝14によって囲まれる1つ以上の凸部となる半導体部103aが形成されている。この半導体部103aは、活性領域としては機能しないダミーの活性領域ともいうべきものである。さらに、後の工程で形成される多結晶シリコン配線10の直下にも溝を形成する。ここで、溝14を形成する際、溝14内に埋め込み絶縁膜101の表面が露出するまでエッチングを行う。

【0151】

図10(f)に示す工程では、基板の全面上に酸化珪素膜23を堆積し、溝14を酸化珪素膜で埋め込む。

【0152】

図11(a)に示す工程では、CMP法を用いて酸化珪素膜23を研磨する。続いて、窒化珪素膜22と酸化珪素膜21を除去し、表面が平坦で酸化珪素膜で埋め込まれた複数の埋め込み溝部8を形成する。この埋め込み溝部8のうち埋め

込み溝部 8 a が素子分離として機能するものであり、埋め込み溝部 8 b はダミーの半導体部 9 を形成するものであり、埋め込み溝部 8 c が多結晶シリコン配線とシリコン基板とを絶縁する機能を有するものである。

【0153】

図 11 (b) に示す工程では、周知の技術を用いてゲート酸化膜 2 と、側面上にサイドウォール 24 を有するゲート電極 4 と、多結晶シリコン配線 10 とを形成する。ゲート電極 4 と多結晶シリコン配線 10 は同時に形成される。

【0154】

図 11 (c) に示す工程では、素子分離領域 7 を覆うレジストマスク 104 を用いて、活性領域 6 に砒素イオン 25 を注入し、ソース・ドレイン 5 を形成する。これまでの工程によって、NMOSFET が形成される。このとき素子分離領域 7 には砒素イオン 25 の注入は行わないが、砒素イオンの注入を行ってもかまわない。

【0155】

図 11 (d) に示す工程では、酸化珪素膜を堆積して層間絶縁膜 12 を形成し、さらにその上にメタル配線 13 を形成する。

【0156】

本実施形態の製造方法によっても、第 6 の実施形態に係る半導体装置と同じ構造が得られ、第 6 の実施形態で説明したように、配線-基板間容量が小さく、動作速度の高い半導体装置を形成することができる。

【0157】

なお、本実施形態においては、微細なゲート電極 4 を形成するために、シリコン基板 1 に溝 102 を形成し酸化珪素膜を埋め込んだ。しかし、ゲート電極の形成に際して半導体基板の平坦性の影響が小さい場合は、溝を形成せず、直接素子分離領域上に酸化珪素膜を形成しても構わない。

【0158】

(各実施形態の変形形態)

以上、本発明における 8 通りの実施形態を説明したが、各実施形態の組合せによる変形形態がある。

【0159】

一例として第1の実施形態を第2～第8の実施形態組み合わせて使えば、いっ
その配線－基板間容量の低減と、容量に対する電荷の充放電の時間短縮とを同
時に行うことが可能となり、各実施形態単独の場合よりさらに半導体装置の速度
が向上する。

【0160】

このように、本発明においては、各実施形態単独で効果があるだけでなく、そ
れぞれを組み合わせることでより大きな効果を実現できる。

【0161】

【発明の効果】

請求項1又は2によると、半導体装置の製造方法として、素子分離領域内に活
性領域としては機能しないダミーの半導体部にPN接合部を形成するようにした
ので、PN接合部の容量の直列付加により配線－基板間容量が低減し、よって、
動作速度の高い、高性能の半導体装置を製造することができる。

【0162】

請求項2, 3, 4, 5又は6によると、半導体装置の製造方法として、素子分
離領域のダミーの半導体部の上に抵抗膜を形成するようにしたので、層間絶縁
膜にかかる電位差が低下して容量への蓄積電荷量が少なくなり、よって、動作速
度の高い、高性能の半導体装置を製造することができる。

【0163】

請求項7, 8又は9によると、半導体装置の製造方法として、素子分離領域内
のダミーの半導体部の上部にイオンを注入してダミーの半導体部を高抵抗層に変
えるようにしたので、層間絶縁膜にかかる電位差が低下して容量への蓄積電荷量
が少なくなり、よって、動作速度の高い、高性能の半導体装置を製造することが
できる。

【0164】

請求項10, 11, 12又は13によると、半導体装置の製造方法として、素
子分離領域内のダミーの半導体部の上に下敷き絶縁膜を形成するようにしたので
、配線－基板間の距離が長くなることによって配線－基板間容量が低減し、よっ

て、動作速度の高い、高性能の半導体装置を製造することができる。

【0165】

請求項14、15又は16によると、半導体装置の製造方法として、素子分離領域内のダミーの半導体部の上に埋め込み絶縁膜を形成するようにしたので、配線-基板領域間の距離が長くなることによって配線-基板間容量が低減し、よって、動作速度の高い、高性能の半導体装置を製造することができる。

【0166】

請求項17によると、半導体装置の製造方法として、素子分離領域内のダミーの半導体部の内部に酸素イオンを注入して埋め込み絶縁膜を形成するようにしたので、埋め込み絶縁膜の容量の直列付加により配線-基板間容量が低減し、よって、動作速度の高い、高性能の半導体装置を製造することができる。

【0167】

請求項18によると、半導体装置の製造方法として、素子分離領域内の半導体部をいったん除去した後絶縁性材料を埋め込んで埋め込み絶縁膜を形成し、埋め込み絶縁膜の上に半導体膜を成長させて、ダミーの半導体部を形成するようにしたので、埋め込み絶縁膜の容量の直列付加により配線-基板間容量が低減し、よって、動作速度の高い、高性能の半導体装置を製造することができる。

【0168】

請求項19によると、半導体装置の製造方法として、素子分離領域全体に亘る溝を形成してから溝内に絶縁性材料を埋め込んで埋め込み絶縁膜を形成した後、埋め込み絶縁膜の上に半導体膜を成長させて、ダミーの半導体部を形成するようにしたので、埋め込み絶縁膜の容量の直列付加により配線-基板間容量が低減し、よって、動作速度の高い、高性能の半導体装置を製造することができる。

【図面の簡単な説明】

【図1】

第1の実施形態に係るNMOSFETを有する半導体装置の製造工程を示す断面図である。

【図2】

第1の実施形態に係る半導体装置の配線-基板間容量を説明するために素子分

離領域を拡大して示す断面図である。

【図3】

第2の実施形態に係るNMOSFETを有する半導体装置の製造工程を示す断面図である。

【図4】

第3の実施形態に係るNMOSFETを有する半導体装置の製造工程を示す断面図である。

【図5】

第4の実施形態に係るNMOSFETを有する半導体装置の製造工程を示す断面図である。

【図6】

第5の実施形態に係るNMOSFETを有する半導体装置の製造工程を示す断面図である。

【図7】

第6の実施形態に係るNMOSFETを有する半導体装置の製造工程を示す断面図である。

【図8】

第6の実施形態に係る半導体装置の配線-基板間容量を説明するために素子分離領域を拡大して示す断面図である。

【図9】

第7の実施形態に係るNMOSFETを有する半導体装置の製造工程を示す断面図である。

【図10】

第8の実施形態に係るNMOSFETを有する半導体装置の前半の製造工程を示す断面図である。

【図11】

第8の実施形態に係るNMOSFETを有する半導体装置の後半の製造工程を示す断面図である。

【図12】

従来の発明のNMOSFETを有する半導体装置の製造工程を示す断面図である。

【図13】

従来の半導体装置の配線-基板間容量を説明するために素子分離領域を拡大して示す断面図である。

【符号の説明】

- 1 シリコン基板
- 2 ゲート酸化膜
- 4 ゲート電極
- 5 ソース・ドレイン
- 6 活性領域
- 7 素子分離領域
- 8 埋め込み溝部
- 9 半導体部
- 10 多結晶シリコン配線
- 13 メタル配線
- 14 溝
- 21 酸化珪素膜
- 22 窒化珪素膜
- 23 酸化珪素膜
- 24 サイドウォール
- 25 砒素イオン
- 31 N型不純物拡散層
- 32 PN接合部
- 51 ダミーゲート
- 52 酸化珪素膜
- 53 高抵抗膜
- 61 埋め込み絶縁膜

- 6 2 溝
- 7 1 高抵抗層
- 7 2 酸素イオン
- 8 1 下敷き絶縁膜
- 8 2 酸化珪素膜
- 8 4 レジストマスク
- 9 1 埋め込み絶縁膜
- 9 2 レジストマスク
- 9 3 酸素イオン
- 9 5 レジストマスク
- 9 6 溝
- 9 7 半導体部
- 9 8 レジストマスク
- 1 0 1 埋め込み絶縁膜
- 1 0 2 溝
- 1 0 3 シリコン膜
- 1 0 3 a 半導体部
- 1 0 4 レジストマスク

【書類名】 要約書

【要約】

【課題】 素子分離領域内の配線-基板間容量が小さい、又は容量内の蓄積電荷量が小さくて動作速度の高い半導体装置の製造方法を提供する。

【解決手段】 P型シリコン基板1上に、酸化珪素膜が埋め込まれた埋め込み溝部8a~8cを形成して、素子分離領域7内に凸状のダミーの活性領域となる半導体部9を形成する工程と、ゲート電極4や多結晶シリコン配線10を形成する工程と、砒素イオン25の注入により活性領域6にはソース・ドレイン5を、半導体部9内には不純物拡散層31をそれぞれ形成する工程と、基板上に層間絶縁膜12及びメタル配線13を形成する工程とを備えている。半導体部9内において、不純物拡散層21とシリコン基板1との間にPN接合部32が形成されるので、層間絶縁膜12の容量にPN接合部32の容量が直列に付加され、全配線-基板間容量が低減し、半導体装置の動作速度が速くなる。

【選択図】 図1

【書類名】 職権訂正データ
【訂正書類】 特許願

<認定情報・付加情報>

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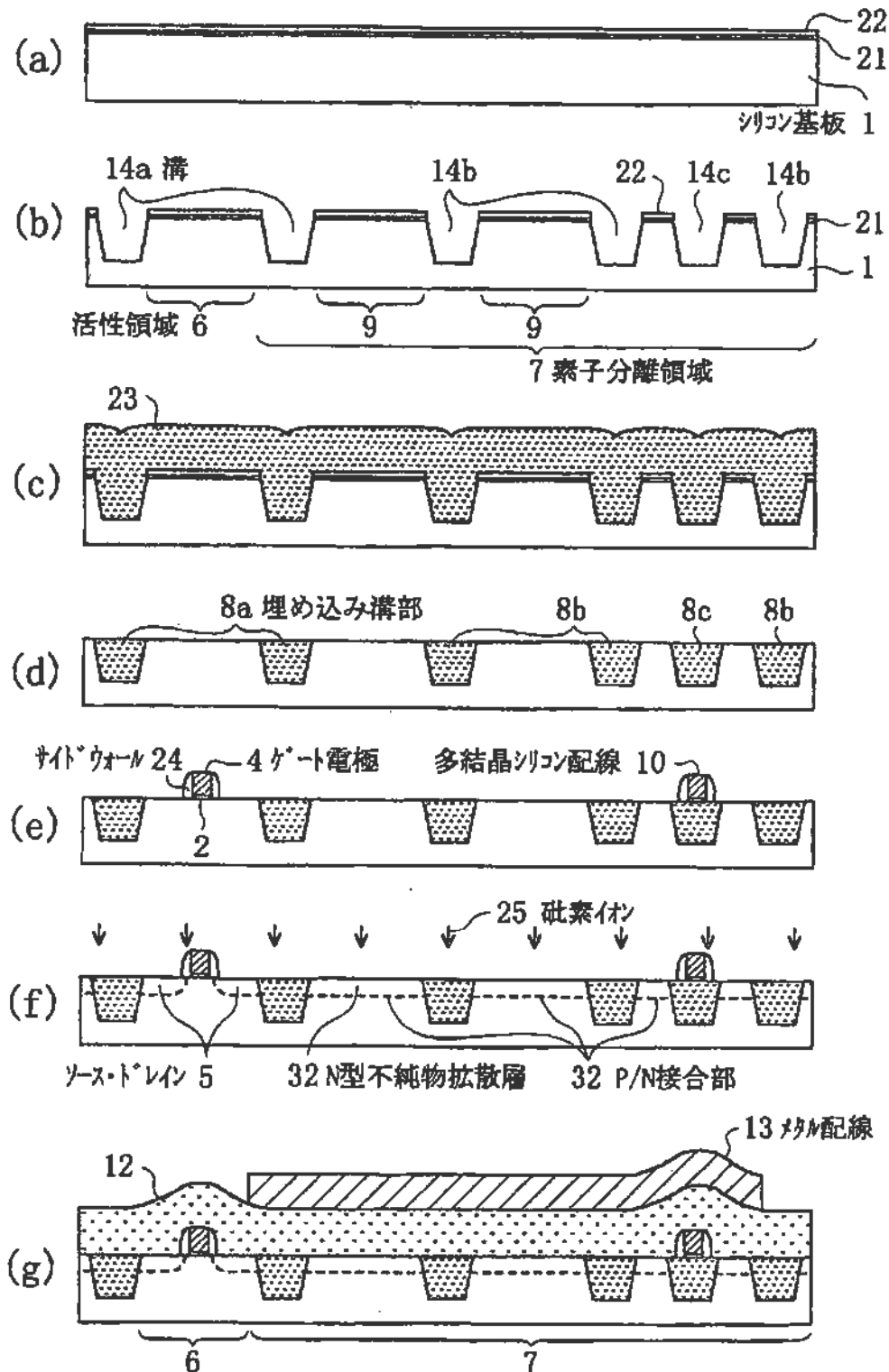
出 願 人 履 歴 情 報

識別番号 [000005821]

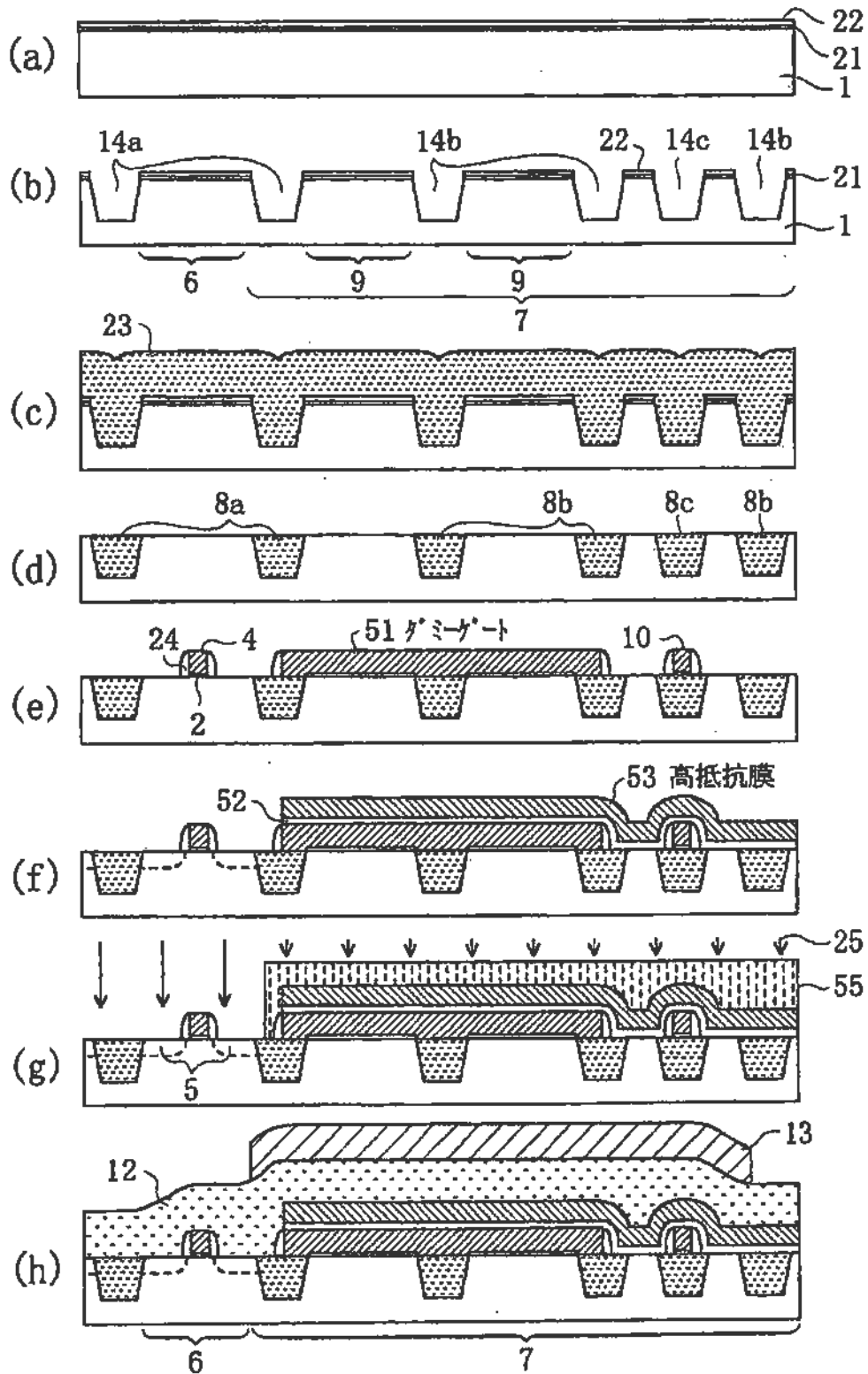
1. 変更年月日	1990年 8月28日
[変更理由]	新規登録
住 所	大阪府門真市大字門真1006番地
氏 名	松下電器産業株式会社

【書類名】 図面

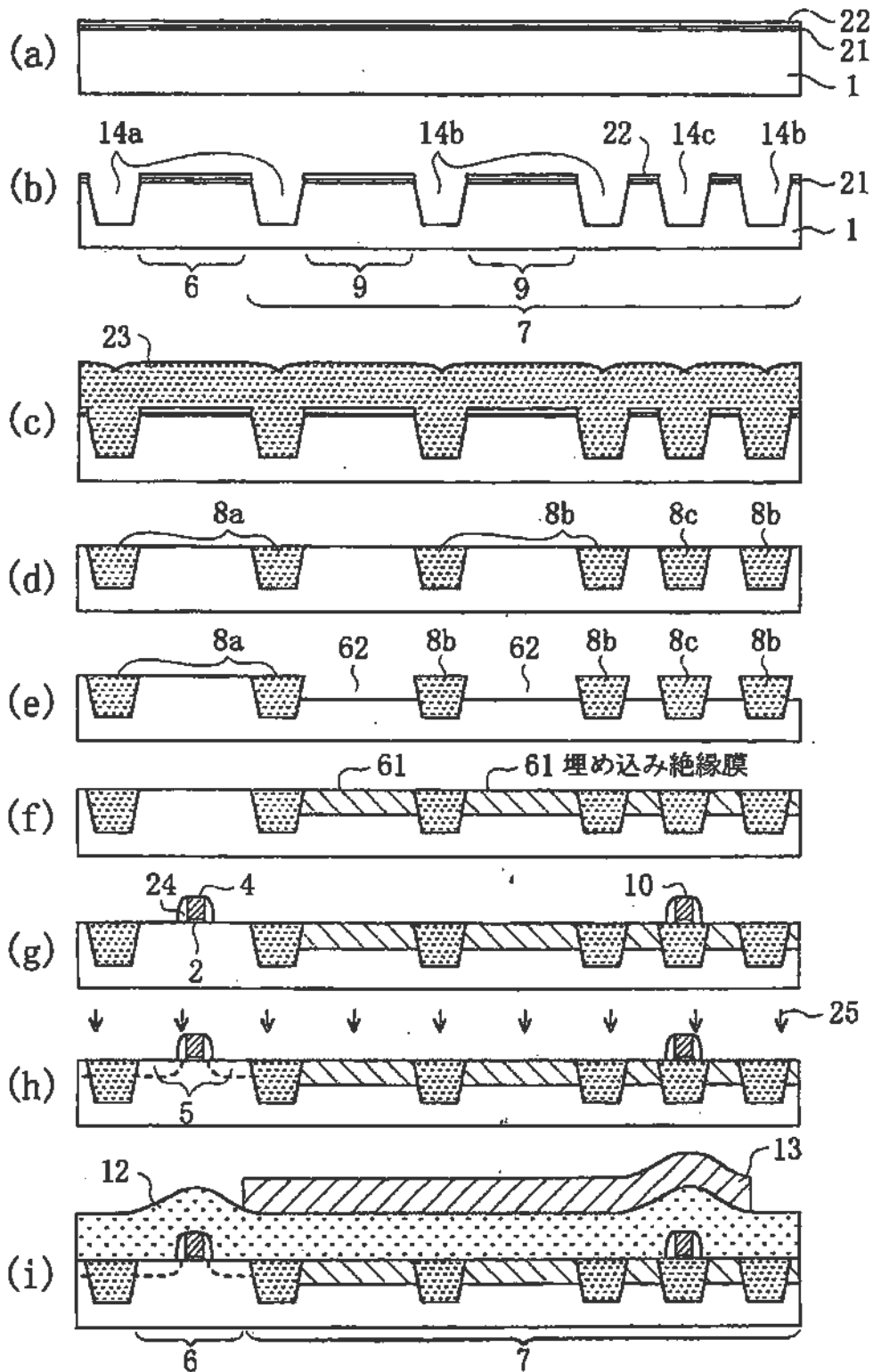
【図1】



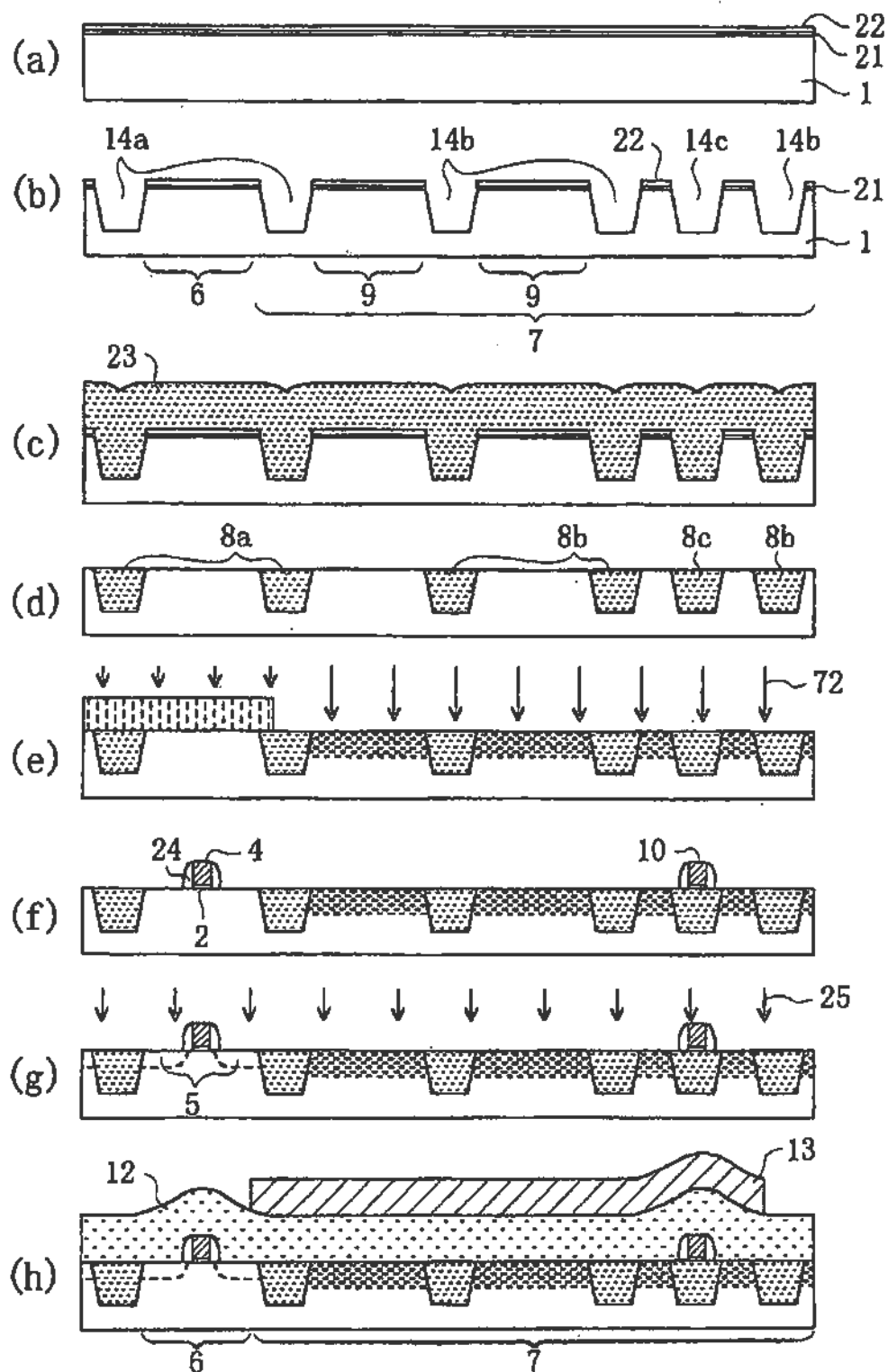
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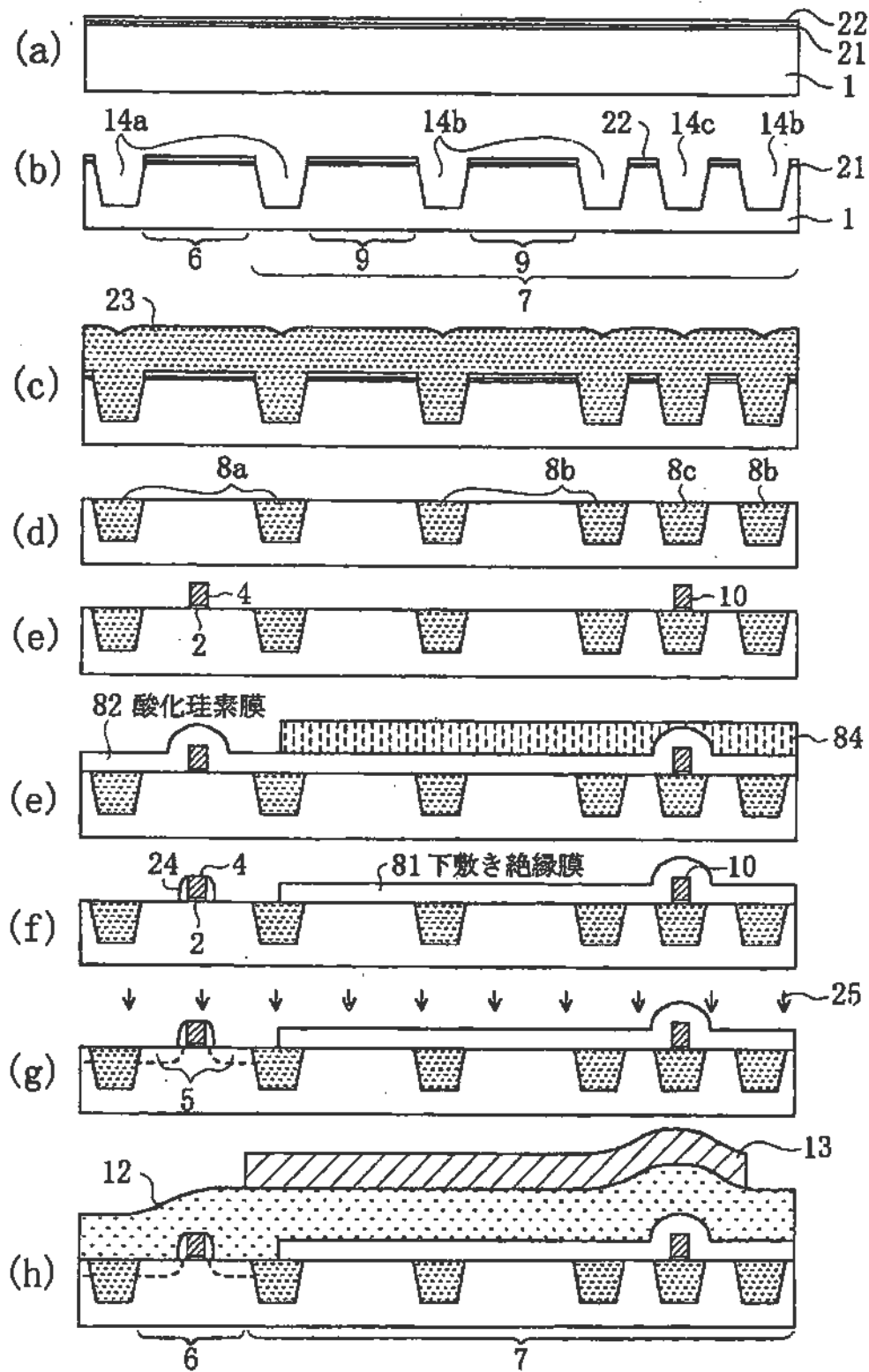
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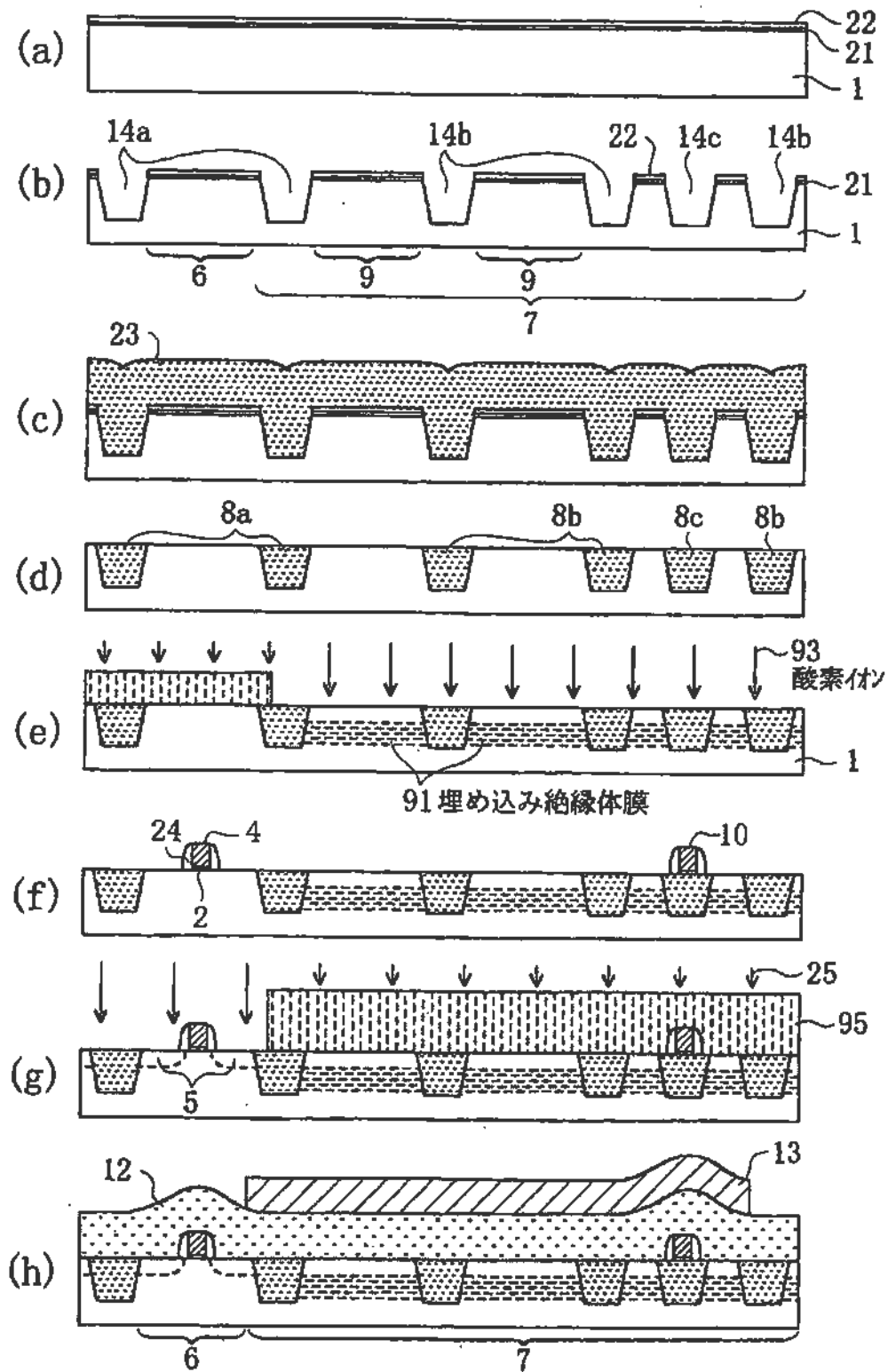
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【図6】

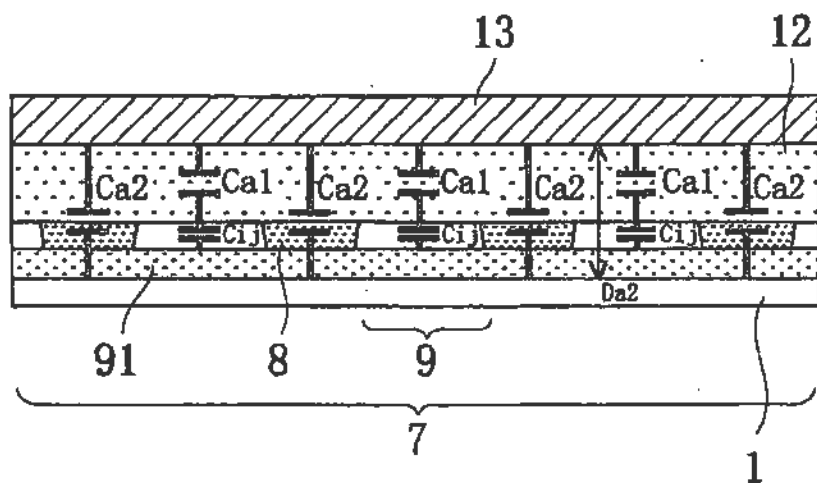


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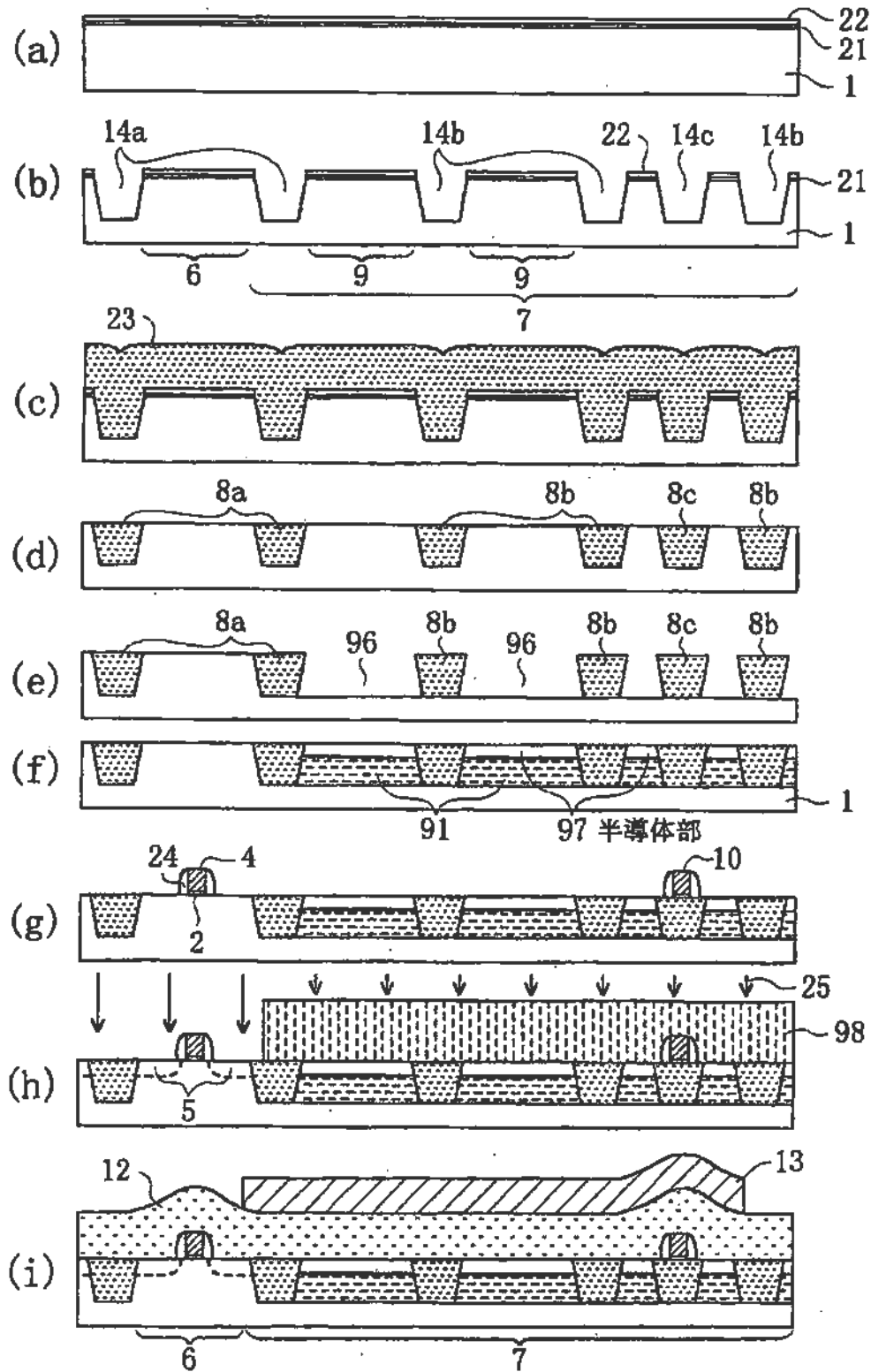




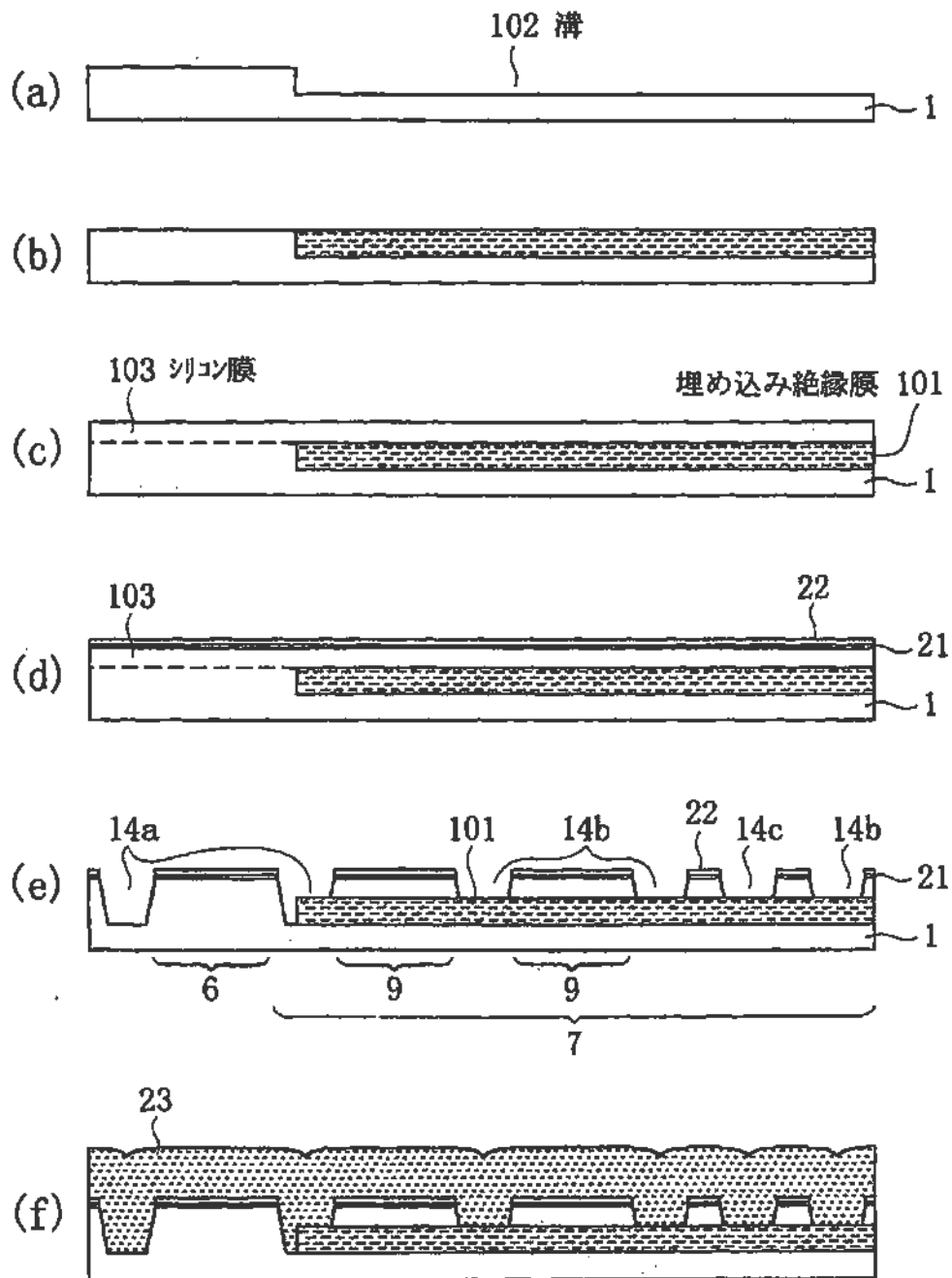
【図 8】



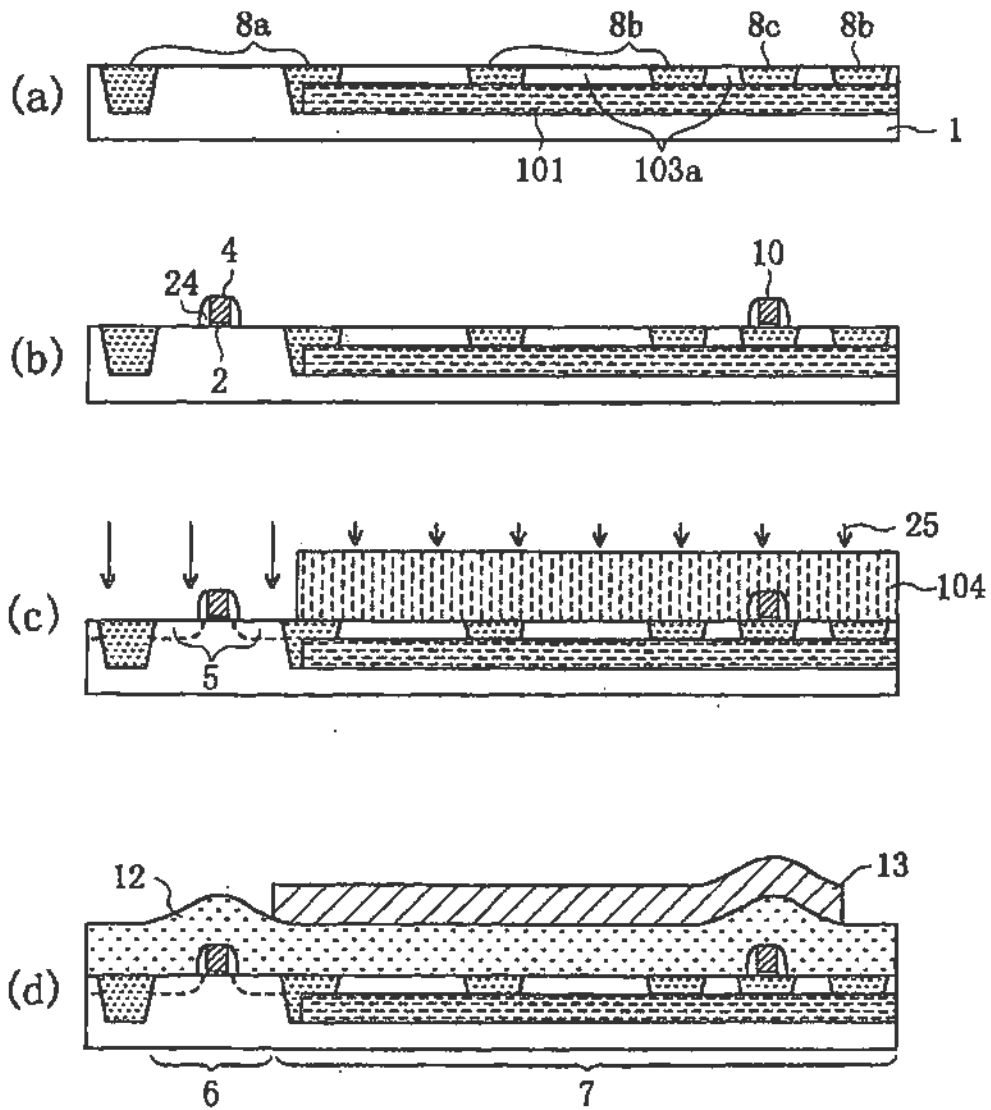
【図9】



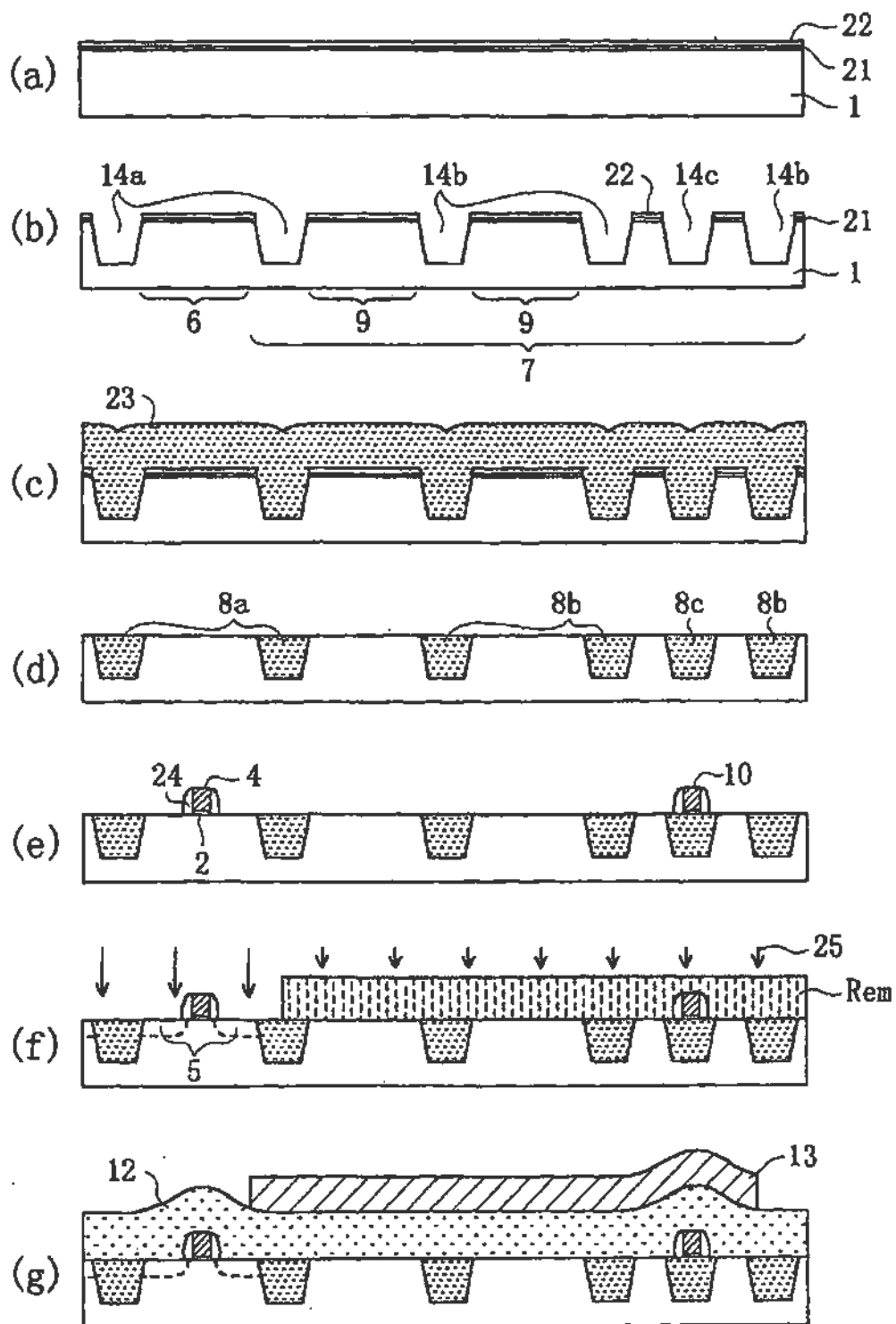
【図10】



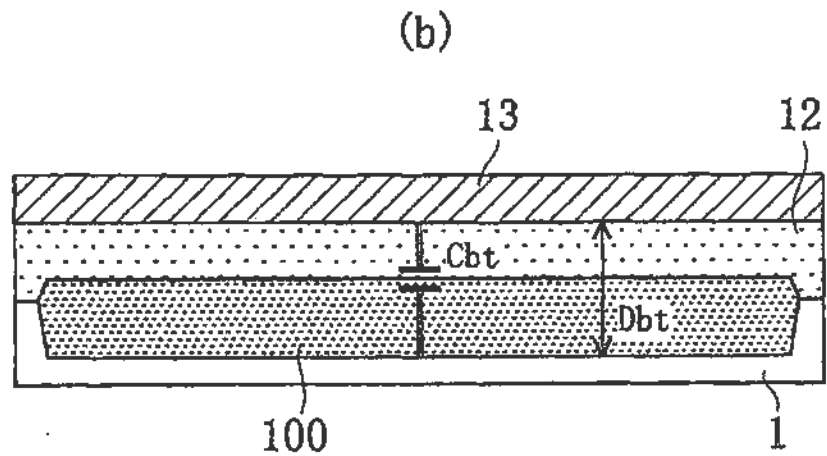
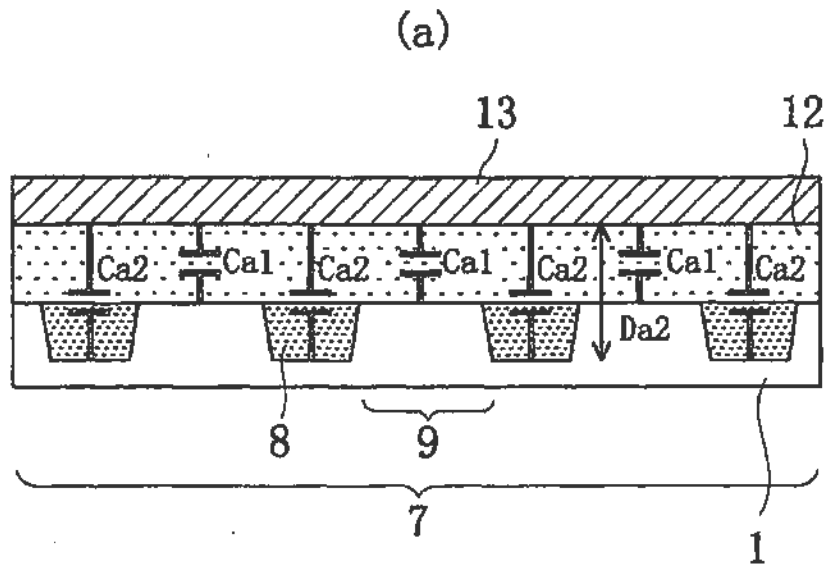
【図11】

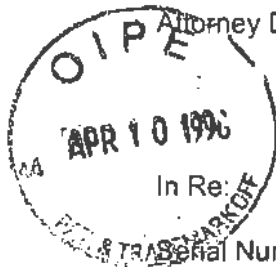


【図12】



【図13】





Attorney Docket No. 43889-677

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re: Takaaki UKEDA, et al.

Serial Number: 08/978,137 ✓

Filing Date: 25 November 1997

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE
SAME

REQUEST FOR CORRECTED OFFICIAL FILING RECEIPT

Assistant Commissioner for Patents
Washington, D. C. 20231

MAY 27 1998

GROUP 2100

Sir:

A corrected Official Filing Receipt is hereby requested in view of the errors which appear in the original. For the convenience of the Patent and Trademark Office, attached is a photocopy of the original receipt on which the errors have been highlighted.

Because the error was made by the Patent and Trademark Office, it is believed that no fee is required. Please grant any extension of time deemed necessary. Please charge any deficient fees, or credit any overpayment of fees, to Deposit Account No. 13-0203. A duplicate copy of this communication is enclosed.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date: 10 April 1998

By: 
Edward E. Kubasiewicz
Registration No. 30,020

600 13th Street, N.W.
Washington, D.C. 20005-3096
(202) 756-8000
(202) 756-8087

Attorney Docket No. 43889-677

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re: Takaaki UKEDA, et al.

Serial Number: 08/978,137

Filing Date: 25 November 1997

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE
SAME

REQUEST FOR CORRECTED OFFICIAL FILING RECEIPT

Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

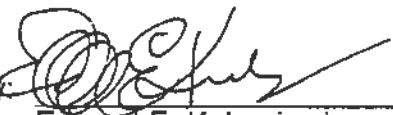
A corrected Official Filing Receipt is hereby requested in view of the errors which appear in the original. For the convenience of the Patent and Trademark Office, attached is a photocopy of the original receipt on which the errors have been highlighted.

Because the error was made by the Patent and Trademark Office, it is believed that no fee is required. Please grant any extension of time deemed necessary. Please charge any deficient fees, or credit any overpayment of fees, to Deposit Account No. 13-0203. A duplicate copy of this communication is enclosed.

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By: 
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600 13th Street, N.W.
Washington, D.C. 20005-3096
(202) 756-8000
(202) 756-8087

FILING RECEIPT



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTORNEY DOCKET NO.	DRWGS	TOT CL	IND CL
08/978,137	11/25/97	2503	\$1,924.00	43889-677	21	38	12

KENNETH L CAGE
MCDERMOTT WILL & EMERY
1850 K STREET NW
SUITE 500
WASHINGTON DC 20006

RECEIVED

MAR 23 1998

McDermott, Will & Emery

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Application Processing Division's Customer Correction Branch within 10 days of receipt. Please provide a copy of the Filing Receipt with the changes noted thereon.

Applicant(s)

TAKAAKI UKEDA, OSAKA, JAPAN; CHIAKI KUDO, KYOTO, JAPAN;
TOSHIKI ~~TAKA~~ OSAKA, JAPAN.
YABU

FOREIGN APPLICATIONS-

JAPAN
JAPAN

8-314762
9-023844

11/26/96
02/06/97

TITLE

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

PRELIMINARY CLASS: 257

ATTORNEY DOCKET NO. 3889-677

82815

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION:

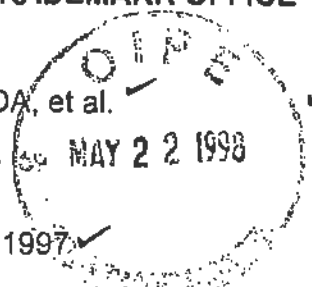
Takaaki UKEDA, et al.

SERIAL NO.:

08/978,137 ✓

FILING DATE:

25 November 1997 ✓



#4
27-98
R. Smith

RE: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME ✓

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

MAY 22 1998


Sir:

In accordance with the duty of disclosure under 37 C.F.R. §§ 1.56 and 1.98, Applicant(s) wish(es) to bring to the attention of the U.S. Patent and Trademark Office the reference(s) listed on the enclosed Form PTO-1449 (2). The references were cited in the corresponding European Search Report. Copies of the listed reference(s) and search report are attached.

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 13-0203. A duplicate copy of this communication is enclosed for accounting purposes.

Respectfully submitted,
McDERMOTT, WILL & EMERY

Date: 22 May 1998

By: 
Edward E. Kubasiewicz
Registration No. 30,020 ✓

600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

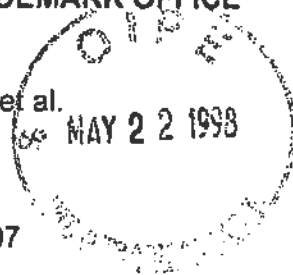
ATTORNEY DOCKET NO. 43889-677

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION: Takaaki UKEDA, et al.

SERIAL NO.: 08/978,137

FILING DATE: 25 November 1997



RE: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure under 37 C.F.R. §§ 1.56 and 1.98, Applicant(s) wish(es) to bring to the attention of the U.S. Patent and Trademark Office the reference(s) listed on the enclosed Form PTO-1449 (2). The references were cited in the corresponding European Search Report. Copies of the listed reference(s) and search report are attached.

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Respectfully submitted,
McDERMOTT, WILL & EMERY

Date: 22 May 1998

By: 
Edward E. Kubasiewicz
Registration No. 30,020

600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
43889-677

SERIAL NO.

LIST OF REFERENCES CITED BY APPLICANT
(Use Several Sheets if Necessary)

APPLICANT

Takaaki UKEDA, et al.

FILING DATE 25 November 1997

GROUP

2822

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	FILING DATE IF APPROPRIATE
	AA				
	AB				
	AC				
	AD				
	AE				
	AF				
	AG				
	AH				
	AI				
	AJ				
	AK				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO
<i>NBP</i>	AL	02272745	07/11/90	Japan	XX
<i>↓</i>	AM	0220500	25/09/86	Europe	XX
	AN				
	AO				
	AP				

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	
	AS	
	AT	

Examiner: KHANH DUNG

DATE CONSIDERED: 4/26/99
IPR2018-00756 Page 00318

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
43889-677SERIAL NO.
08/976,137

MAY 22 1998

LIST OF REFERENCES CITED BY APPLICANT
(Use Several Sheets if Necessary)

APPLICANT

Takaaki UKEDA, et al.

FILING DATE 25 November 1997

GROUP

2822

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB. CLASS	FILING DATE IF APPROPRIATE
KBP	AA	5,665,633 equivalent to Japanese No. 08288380	09/09/97	Meyer	438	427	
	AB	5,663,588 equivalent to Japanese No. 08032039	02/09/97	Suzuki, et al.	257	350	
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO
KBP	AL	63246842	13/10/88	Japan	XX
	AM	60015944	26/01/85	Japan	XX
	AN	05013565	22/01/93	Japan	XX
	AO	0538807	20/10/92	Europe	XX
	AP	5820054	22/11/83	Japan	XX

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	
	AS	
	AT	

Examiner: KHANH DUONG

Date: 4/26/99



P.O. 5818 - Patenlaan 2
2280 HV Rijswijk (ZH)
☎ (070) 3 40 20 40
TX 31651 epo nl
FAX (070) 3 40 30 16

Europäisches
Patentamt

Zweigstelle
in Den Haag
Recherchen-
abteilung

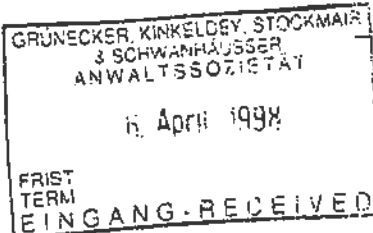
European
Patent Office

Branch at
The Hague
Search
division

Office européen
des brevets

Département à
La Haye
Division de la
recherche

Grünecker, Kinkeldey,
Stockmair & Schwanhäusser
Anwaltssozietät
Maximilianstrasse 58
80538 München
ALLEMAGNE



Datum/Date

26.03.98

Zeichen/Ref./Réf. EP14290-011/do ✓	Anmeldung Nr./Application No./Demande n°/Patent Nr./Patent No./Brevet n° 97120656.0-2203- ✓
Anmelder/Applicant/Demandeur/Patent/inhaber/Propriétaire/Titulaire MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. ✓	

COMMUNICATION

The European Patent Office herewith transmits as an enclosure the European search report for the above-mentioned European patent application.

If applicable, copies of the documents cited in the European search report are attached.

☒ Additional set(s) of copies of the documents cited in the European search report is (are) enclosed as well.

The following specifications given by the applicant have been approved by the Search Division:

☒ abstract

☒ title

☐ The abstract was modified by the Search Division and the definitive text is attached to this communication.

The following figure will be published together with the abstract:

3

REFUND OF THE SEARCH FEE

If applicable under Article 10 Rules relating to fees, a separate communication from the Receiving Section on the refund of the search fee will be sent later.





DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y ① A	JP 08 288 380 A (MOTOROLA INCORPORATED) 1 November 1996 - & US 5 665 633 A (MEYER GEORGE R) * abstract; claims; figures * * column 4, line 60 - column 5, line 45 *	1-12, 16, 19-21 29-35	H01L21/762 H01L29/06 H01L23/522 H01L21/3205
Y ②	PATENT ABSTRACTS OF JAPAN vol. 013, no. 053 (E-713), 7 February 1989 - & JP 63 246842 A (NEC CORP), 13 October 1988, * abstract *	1, 3, 19-21	
Y ③	PATENT ABSTRACTS OF JAPAN vol. 009, no. 126 (E-318), 31 May 1985 - & JP 60 015944 A (HITACHI SEISAKUSHO KK), 26 January 1985, * abstract *	1, 2	
Y ④ A	PATENT ABSTRACTS OF JAPAN vol. 017, no. 276 (E-1372), 27 May 1993 - & JP 05 013565 A (FUJITSU LTD), 22 January 1993, * figure 5 *	4-12, 16	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A ⑤	PATENT ABSTRACTS OF JAPAN vol. 096, no. 006, 28 June 1996 - & JP 08 032039 A (NIPPONDENSO CO LTD), 2 February 1996, * abstract * - & US 5 663 588 A (SUZUKI MEGUMI ET AL) * abstract; claims; figures * * column 5, line 18 - line 27 *	22, 23, 25 10, 37, 38	
A ⑥	EP 0 538 807 A (NIPPON ELECTRIC CO) * abstract; claims; figures *	11, 22, 23, 25	
-/-			
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 19 March 1998	Examiner Wirner, C
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

5

EPO FORM 1503 03.12 (P04C01)



DOCUMENTS CONSIDERED TO BE RELEVANT															
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)												
A (4)	PATENT ABSTRACTS OF JAPAN vol. 008, no. 044 (E-229), 25 February 1984 -& JP 58 200554 A (HITACHI SEISAKUSHO KK), 22 November 1983, * abstract *	26-28													
A (8)	PATENT ABSTRACTS OF JAPAN vol. 015, no. 029 (E-1026), 23 January 1991 -& JP 02 272745 A (NEC CORP), 7 November 1990, * abstract *	33-35													
A (9)	EP 0 220 500 A (TOKYO SHIBAURA ELECTRIC CO) * abstract; claims; figures * * column 2, line 6 - line 32 *	1,3													
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)												
The present search report has been drawn up for all claims															
Place of search THE HAGUE		Date of completion of the search 19 March 1998	Examiner Wirner, C												
<table border="0"><tr><td>CATEGORY OF CITED DOCUMENTS</td><td>T : theory or principle underlying the invention</td></tr><tr><td>X : particularly relevant if taken alone</td><td>E : earlier patent document, but published on, or after the filing date</td></tr><tr><td>Y : particularly relevant if combined with another document of the same category</td><td>D : document cited in the application</td></tr><tr><td>A : technological background</td><td>L : document cited for other reasons</td></tr><tr><td>O : non-written disclosure</td><td></td></tr><tr><td>P : intermediate document</td><td>& : member of the same patent family, corresponding document</td></tr></table>				CATEGORY OF CITED DOCUMENTS	T : theory or principle underlying the invention	X : particularly relevant if taken alone	E : earlier patent document, but published on, or after the filing date	Y : particularly relevant if combined with another document of the same category	D : document cited in the application	A : technological background	L : document cited for other reasons	O : non-written disclosure		P : intermediate document	& : member of the same patent family, corresponding document
CATEGORY OF CITED DOCUMENTS	T : theory or principle underlying the invention														
X : particularly relevant if taken alone	E : earlier patent document, but published on, or after the filing date														
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A : technological background	L : document cited for other reasons														
O : non-written disclosure															
P : intermediate document	& : member of the same patent family, corresponding document														

5
EPO FORM 1503 03.82 (Pst/C61)

ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.

EP 97 12 0656

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

19-03-1998

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 8288380 A	01-11-96	US 5665633 A	09-09-97
EP 0538807 A	28-04-93	JP 5121664 A	18-05-93
EP 0220500 A	06-05-87	JP 62072144 A	02-04-87
		US 4960725 A	02-10-90

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, DC 20231

APPLICATION NO.	FILING DATE	FIRST NAME OF INVENTOR	ATTORNEY DOCKET NO.
08/978,137	11/25/97	UKEDA T	43889-677

KENNETH L. CAGE
MODERMOTT WILL & EMERY
1850 K STREET NW
SUITE 500
WASHINGTON DC 20006

MM21/0121

EXAMINER
JACKSON JR, J

ART UNIT
2815

PAPER NUMBER

DATE MAILED: 01/21/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

978137

Applicant(s)

Yheda

Examiner

J

Group Art Unit

2875

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- ☐ Responsive to communication(s) filed on _____.
- ☐ This action is FINAL.
- ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- ☒ Claim(s) 1 - 38 is/are pending in the application.
- ☐ Of the above claim(s) _____ is/are withdrawn from consideration.
- ☐ Claim(s) _____ is/are allowed.
- ☐ Claim(s) _____ is/are rejected.
- ☐ Claim(s) _____ is/are objected to.
- ☒ Claim(s) 1 - 38 are subject to restriction or election requirement.

Application Papers

- ☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The proposed drawing correction, filed on _____, is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

- ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
 - ☐ All ☐ Some ☐ None of the CERTIFIED copies of the priority documents have been received.
 - ☐ received in Application No. (Series Code/Serial Number) _____.
 - ☐ received in this national stage application from the International Bureau (PCT Rule 1.7.2(a)).

*Certified copies not received: _____

Attachment(s)

- ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____
- ☐ Interview Summary, PTO-413
- ☐ Notice of Reference(s) Cited, PTO-892
- ☐ Notice of Informal Patent Application, PTO-152
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Other _____

Office Action Summary

Art Unit: 2815

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-18, drawn to a device, classified in class 257, subclass 355.

II. Claims 19-38, drawn to a process, classified in class 437, subclass 15+.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by a materially different process such as forming the element prior to filling the trench.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any


Art Unit: 2815

amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerome Jackson whose telephone number is (703) 308-4937.

jj

January 13, 1999



Jerome Jackson, Jr.
Primary Examiner



ATTORNEY DOCKET NO. 43889-677
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Takaaki UKEDA et al.) Group Art Unit: 2815
Serial No.: 08/978,137)
Filed: July 7, 1997) Examiner: J. Jackson, Jr.
For: SEMICONDUCTOR DEVICE AND)
METHOD OF MANUFACTURING THE SAME)

REQUEST FOR CHANGE OF ADDRESS

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

Applicants, by and through their attorney, hereby request
that, for the above-identified application, all future
correspondence, facsimiles and telephone calls be addressed to:

Edward E. Kubasiewicz, Esq.
600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087



020277

PATENT AND TRADEMARK OFFICE

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date: February 1, 1999

By: 

Kenneth L. Cage
Registration No. 26,151

600 13th Street, N.W.
Washington, D.C. 20005-3096
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Facsimile: 202-756-8087
\\43889\\677\\CHG-ADD.FIL

#11/CA
10/13/99
Purlee

RECEIVED

FEB 16 1999

GROUP 2100

CF

ATTORNEY DOCKET NO. 43889/677
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Takaai UKEDA et al.

Serial No.: 08/978,133

Filed: November 25, 1997

For: SEMICONDUCTOR DEVICE AND
METHOD OF MANUFACTURING THE
SAME



Group Art Unit: 2503

Examiner: O. NADAV

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FEB 17 1999

ELECTION UNDER 35 U.S.C. § 121 GROUP 2100

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed January 21, 1999, a shortened statutory period for response due to expire on February 21, 1999, requiring that Applicants elect one of the following groups for prosecution in the above-identified application:

Group I - Claims 1-18, drawn to a device; and

Group II - Claims 19-38, drawn to a process.

Applicants hereby provisionally elect Group II, Claims 19-38, drawn to a process for prosecution on the merits.

Applicants reserve the right to file a divisional application on the non-elected claims.

#6/elected
2/18/99
V. Varnado

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 13-0203. A duplicate copy of this communication is enclosed for accounting purposes.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date: February 16, 1999

By: 

Edward E. Kubasiewicz
Registration No. 30,020

600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087
\\43889\\677\\ELECTION.RES

ATTORNEY DOCKET NO. 43889/677
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Takaai UKEDA et al.)
Serial No.: 08/978,137) Group Art Unit: 2503
Filed: November 25, 1997) Examiner: O. NADAV
For: SEMICONDUCTOR DEVICE AND)
METHOD OF MANUFACTURING THE)
SAME)

ELECTION UNDER 35 U.S.C. § 121

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

RECEIVED
FEB 17 1999
GROUP 2100

Sir:

In response to the Office Action mailed January 21, 1999, a shortened statutory period for response due to expire on February 21, 1999, requiring that Applicants elect one of the following groups for prosecution in the above-identified application:

- Group I - Claims 1-18, drawn to a device; and
- Group II - Claims 19-38, drawn to a process.

Applicants hereby provisionally elect Group II, Claims 19-38, drawn to a process for prosecution on the merits.

Applicants reserve the right to file a divisional application on the non-elected claims.

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 13-0203. A duplicate copy of this communication is enclosed for accounting purposes.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: February 16, 1999

By: 

Edward S. Kubasiewicz
Registration No. 30,020

600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087
\\43889\\677\\ELECTION.RES



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/978,137	11/25/97	UKEDA T	43889-677

KENNETH L CAGE
MCDERMOTT WILL & EMERY
1850 K STREET NW
SUITE 500
WASHINGTON DC 20006

MM21/0510

EXAMINER

DUONG, K

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 05/10/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action SummaryApplication No.
08/978,137Applicant(s)
Ukeda et al.Examiner
Khanh DuongGroup Art Unit
2822☒ Responsive to communication(s) filed on Feb 16, 1999☐ This action is **FINAL**.☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims☒ Claim(s) 1-38 is/are pending in the application.Of the above, claim(s) 1-18 is/are withdrawn from consideration.☒ Claim(s) 22-35, 37, and 38 is/are allowed.☒ Claim(s) 19-21 and 36 is/are rejected.☐ Claim(s) _____ is/are objected to.☐ Claims _____ are subject to restriction or election requirement.**Application Papers**☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.☐ The drawing(s) filed on _____ is/are objected to by the Examiner.☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.☐ The specification is objected to by the Examiner.☐ The oath or declaration is objected to by the Examiner.**Priority under 35 U.S.C. § 119**☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been☒ received.☐ received in Application No. (Series Code/Serial Number) _____☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).**Attachment(s)**☒ Notice of References Cited, PTO-892☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4☐ Interview Summary, PTO-413☒ Notice of Draftsperson's Patent Drawing Review, PTO-948☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Art Unit: 2822

DETAILED ACTION

Election/Restriction

1. Applicant's election of claims 19-38 in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over *applicants' admitted prior art* in view of *Kinoshita et al. (US 5,856,218)*.

Applicants' admitted prior art discloses a method of fabricating a semiconductor device (see Figs 20a-20g) comprising at least the steps of: forming buried trench portions; forming a

Art Unit: 2822

transistor element on an active region; forming an interlayer insulating film over the entire surface of the substrate; and forming a wire on the interlayer insulating film.

However, *applicants' admitted prior art* fails to teach introducing an impurity of a second conductivity type into the semiconductor portions of an isolation region to form at least one PN junction. *Kinoshita et al.* teaches (see Figs 1E-2B; col 4, lines 18-37) to implant N-type impurity into a P-type substrate to simultaneously form N-type source/drain regions 17, an N⁺ layer 20, and an N⁺ layer 22. Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the process of *applicants' admitted prior art* by implanting an impurity of a second conductivity type into the substrate to form at least one PN junction as taught by *Kinoshita et al.* because of the desirability to minimize process steps and manufacturing cost. Re further claim 21, even though the preferred embodiment of *Kinoshita et al.* is simultaneously forming the source/drain and the PN junction, it would have been obvious to one having an ordinary skill in the art to form the source/drain regions and the PN junction in separate steps, since it has been held that the performance of two steps simultaneously or in sequence has been held to be obvious. See *In re Tatincloux*, 108 USPQ 125 (CCPA 1955).

5. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over *applicants' admitted prior art* in view of *Beitman* (US 4,929,566).

Applicants' admitted prior art discloses a method of fabricating a semiconductor device previously as described, which method is repeated herein.

Art Unit: 2822

However, *applicants' admitted prior art* fails to teach implanting oxygen ions into each of the dummy semiconductor portions to form a buried insulating film. *Beitman* teaches (see Fig 7; col 3, lines 16-22) to implant oxygen ions into the epitaxial layer 12 to form a buried insulating film 22. Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the process of *applicants' admitted prior art* by implanting oxygen ions into each of the dummy semiconductor portions because of the desirability to form "totally dielectrically isolated islands" as suggested by *Beitman* at column 3, lines 3-5.

Allowable Subject Matter

6. Claims 22-35, 37 and 38 are allowed over the art of record.
7. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not show or suggest a method of fabricating a semiconductor device comprising the steps in the independent claims as follow:

22. *A method of ... forming a resistor film on each of said dummy semiconductor portions of said isolation region...*

26. *A method of ... implanting ions into an upper portion of each of said dummy semiconductor portions to form a high resistor portion therein...*

29. *A method of ... forming an underlying insulating film over said dummy semiconductor portions of said isolation region...*

Art Unit: 2822

33. *A method of ... forming depressed portions by etching said dummy semiconductor portions and filling an insulating material in said depressed portions to form inter-trench insulating films each having a top face at the same level as respective top faces of said first and second buried trench portions...*

37. *A method of ... forming third trenches by etching said semiconductor portions and filling an insulating material in said third trenches to form buried insulating films each having a top face at a level lower than respective top faces of said first and second buried trench portions ... growing semiconductor films on said buried insulating films, with said active region covered with a mask member, to form dummy semiconductor portions...*

38. *A method of ... forming, in a semiconductor substrate having a substrate region, a first trench extending over an entire isolation region of said substrate region, while leaving an active region of said substrate region ... filling an insulating material in said first trench to form a buried insulating film having a top face at the same level as a top face of said isolation region ... growing a semiconductor film over said active region and said buried insulating film...*

Conclusion

This office action has been created under the Patent and Trademark Office Semiconductor Technology Quality Assurance Pilot Program. It incorporates the examination quality standards set as a result of customer focus sessions with the semiconductor industry. The listing of the field of search to follow is one of these standards.

Art Unit: 2822

Field of Search	Date
U.S. Class and subclass: 438/404,405,412-414,423-425,427,353-357,359,360,370	4/28/99
Electronic data base(s): USPAT	4/28/99

Contacts Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Duong whose telephone number is (703) 308-5840. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Toby Brown, can be reached at (703) 308-4083. The fax numbers for the Group is (703) 305-3431 and (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (703) 308-1778.



KBD

April 29, 1999



TERESA M. ARROYO
PRIMARY EXAMINER
GROUP 2810

ACTING
PE

Notice of References Cited

Application No.
08/978,137

Applicant(s)
Ukeda et al.

Examiner
Khanh Duong

Group Art Unit
2822

Page 1 of 1

U.S. PATENT DOCUMENTS

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A	3,622,382	11/23/71	Brack et al.	428	448
B	4,929,566	5/29/90	Beitman	438	423
C	4,946,742	8/14/90	Nishimura et al.	438	423
D	5,426,062	6/20/95	Hwang	438	423
E	5,270,285	12/14/93	Hemmenway et al.	438	404
F	5,760,444	8/2/98	Okumura	257	350
G	5,856,218	1/5/99	Kinoshita et al.	438	414
H	5,877,066	3/2/99	Stolmeijer et al.	438	424
I					
J					
K					
L					
M					

FOREIGN PATENT DOCUMENTS

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
N						
O						
P						
Q						
R						
S						
T						

NON-PATENT DOCUMENTS

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U		
V		
W		
X		

978/37

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

PTO Draftpersons review all originally filed drawings regardless of whether they are designated as formal or informal. Additionally, patent Examiners will review the drawings for compliance with the regulations. Direct telephone inquiries concerning this review to the Drawing Review Branch, 703-305-8404.

The drawings filed (insert date) 11/25/97 are
 A. ☒ not objected to by the Draftsperson under 37 CFR 1.84 or 1.152.
 B. ☐ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawings must be submitted according to the instructions on the back of this Notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:

Black ink. Color.

- ☐ Not black solid lines. Fig(s) _____
☐ Color drawings are not acceptable until petition is granted. Fig(s) _____

2. PHOTOGRAPHS. 37 CFR 1.84(b)

- ☐ Photographs are not acceptable until petition is granted. Fig(s) _____
☐ Photographs not properly mounted (must use bristol board or photographic double-weight paper). Fig(s) _____
☐ Poor quality (half-tone). Fig(s) _____

3. GRAPHIC FORMS. 37 CFR 1.84(d)

- ☐ Chemical or mathematical formula not labeled as separate figure. Fig(s) _____
☐ Group of waveforms not presented as a single figure, using common vertical axis with time extending along horizontal axis. Fig(s) _____
☐ Individual waveform not identified with a separate letter designation adjacent to the vertical axis. Fig(s) _____

4. TYPE OF PAPER. 37 CFR 1.84(c)

- ☐ Paper not flexible, strong, white, smooth, nonshiny, and durable. Sheet(s) _____
☐ Erasures, alterations, overwritings, interlineations, cracks, creases, and folds copy machine marks not accepted. Fig(s) _____
☐ Mylar, vellum paper is not acceptable (too thin). Fig(s) _____

5. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:

- 21.6 cm. by 35.6 cm. (8 1/2 by 14 inches)
 21.6 cm. by 33.1 cm. (8 1/2 by 13 inches)
 21.6 cm. by 27.9 cm. (8 1/2 by 11 inches)
 21.0 cm. by 29.7 cm. (DIN size A4)

- ☐ All drawing sheets not the same size. Sheet(s) _____
☐ Drawing sheet not an acceptable size. Sheet(s) _____

6. MARGINS. 37 CFR 1.84(g): Acceptable margins:

Paper size

21.6 cm. X 35.6 cm. (8 1/2 X 14 inches)	21.6 cm. X 33.1 cm. (8 1/2 X 13 inches)	21.6 cm. X 27.9 cm. (8 1/2 X 11 inches)	21.0 cm. X 29.7 cm. (DIN Size A4)
Top (T) 5.1 cm. (2")	2.5 cm. (1")	2.5 cm. (1")	2.5 cm.
Left (L) .64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	2.5 cm.
Right (R) .64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	1.5 cm.
Bottom (B) .64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	1.0 cm.

Margins do not conform to chart above.

Sheet(s) _____

Top (T) _____ Left (L) _____ Right (R) _____ Bottom (B) _____

7. VIEWS. 37 CFR 1.84(h)

- REMARKER: Specification may require revision to correspond to drawing changes.
☐ All views not grouped together. Fig(s) _____
☐ Views connected by projection lines or lead lines. Fig(s) _____
 Partial views. 37 CFR 1.84(h) 2

☐ View and enlarged view not labeled separately or properly.

Fig(s) _____

☐ Sectional views. 37 CFR 1.84 (h) 3☐ Hatching not indicated for sectional portions of an object.

Fig(s) _____

☐ Cross section not drawn same as view with parts in cross section with regularly spaced parallel oblique strokes. Fig(s) _____

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)

☐ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____

9. SCALE. 37 CFR 1.84(k)

☐ Scale not large enough to show mechanism with crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) _____
☐ Indication such as "actual size" or scale 1/2" not permitted. Fig(s) _____

10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(j)

☐ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (except for color drawings). Fig(s) _____

11. SHADING. 37 CFR 1.84(in)

☐ Solid black shading areas not permitted. Fig(s) _____
☐ Shade lines, pale, rough and blurred. Fig(s) _____

12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)

☐ Numbers and reference characters not plain and legible. 37 CFR 1.84(p)(1) Fig(s) _____
☐ Numbers and reference characters not oriented in same direction as the view. 37 CFR 1.84(p)(1) Fig(s) _____
☐ English alphabet not used. 37 CFR 1.84(p)(2) Fig(s) _____
☐ Numbers, letters, and reference characters do not measure at least .32 cm. (1/8 inch) in height. 37 CFR(p)(3) Fig(s) _____

13. LEAD LINES. 37 CFR 1.84(q)

☐ Lead lines cross each other. Fig(s) _____
☐ Lead lines missing. Fig(s) _____

14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(r)

☐ Sheets not numbered consecutively, and in Arabic numerals, beginning with number 1. Sheet(s) _____

15. NUMBER OF VIEWS. 37 CFR 1.84(u)

☐ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____
☐ View numbers not preceded by the abbreviation Fig. Fig(s) _____

16. CORRECTIONS. 37 CFR 1.84(w)

☐ Corrections not made from prior PTO-948. Fig(s) _____

17. DESIGN DRAWING. 37 CFR 1.152

☐ Surface shading shown not appropriate. Fig(s) _____
☐ Solid black shading not used for color contrast. Fig(s) _____

COMMENTS:



EP 2822#

PATENT APPLICATION
ATTORNEY DOCKET NO. 43889-677

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Takashi UKEDA et al.

Serial No.: 08/978,137

Group Art Unit: 2822

Filed: November 25, 1997

Examiner: K. Duong

For: SEMICONDUCTOR DEVICE AND
METHOD OF MANUFACTURING THE SAME

AMENDMENT TRANSMITTAL

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

1. ☒ Transmitted herewith is an amendment for the above-identified application.

STATUS

2. ☐ Applicant is ☐ is small entity - verified statement:
☐ attached ☐ already filed.
☒ other than a small entity.

EXTENSION OF TIME

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

- (a) ☒ Applicant petitions for an extension of time for the total number of months checked below:

EXTENSION (months)	FEE FOR SMALL ENTITY	FEE FOR OTHER THAN SMALL ENTITY
<input checked="" type="checkbox"/> one month	\$ 55.00	\$ 110.00
<input type="checkbox"/> two months	190.00	380.00
<input type="checkbox"/> three months	435.00	870.00
<input type="checkbox"/> four months	680.00	1,360.00

09/10/1999 ANDREW 00000058 130203

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110.00 CN

Fee \$ 110.00

If an additional extension of time is required, please consider this a petition therefor.

☐ An extension for ☐ months has already been secured and the fee paid therefor of ☐ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this Request \$ _____

- (b) ☐ Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time.

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4. X The fee for claims has been calculated as shown below:

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	Rate	Additional Fee
Total					
Claims	20	38	0	x \$ 18.00 =	0.00
Independent					
Claims	8	12	0	x \$ 78.00 =	0.00
Multiple Dependent Claims (first presentation)					\$260.00 = 0.00
Total					= 0.00
Reduction by 1/4 for small entity					- 0.00
TOTAL FEE					= 0.00

- (a) X No additional fee for claims is required.

-OR-

- (b) The total additional fee for claims required \$.

FEE PAYMENT

5. Attached is a check in the amount of \$.

- X Charge Deposit Account No. 13-0203 the amount of 110.00. A duplicate copy of this Transmittal is enclosed for accounting purposes.

FEE DEFICIENCY

- X If any additional extension and/or fee is required, this is the request therefor and to charge Deposit Account No. 13-0203.

AND/OR

- X If any additional fee for claims is required, charge Deposit Account No. 13-0203. A duplicate copy of this Transmittal is enclosed for accounting purposes.

Respectfully submitted,

McDERMOTT, WILL & EMERY.

Date: September 9, 1999

By: 
Michael E. Fogarty
Registration No. 36,139

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Washington, D.C. 20005-3096
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ATTORNEY DOCKET NO. 43889/677
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

9/A
9/15/99
JProct

In re Application of:)
Takaai UKEDA et al.)
Serial No.: 08/978,137) Group Art Unit: 2822
Filed: November 25, 1997) Examiner: K. DUONG
For: SEMICONDUCTOR DEVICE AND)
METHOD OF MANUFACTURING THE)
SAME)

AMENDMENT UNDER 37 C.F.R. § 1.111

Honorable Assistant Commissioner
for Patents and Trademarks
Washington, D.C. 20231

Sir:

In response to the Office Action dated May 10, 1999, having a (3) three-month period for response set to expire August 10, 1999, a one month petition for an extension of time up to and including September 10, 1999 being filed concurrently herewith, please amend the application as follows:

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A

IN THE DRAWINGS:

Please amend Fig. 1(a) as illustrated on the marked-up copy of the figure enclosed herewith. It is noted that the amendment to Fig. 1(a) corrects an inadvertent clerical error.

IN THE CLAIMS:

Please cancel claims 1-18, without prejudice, and amend claims 33 and 36 as follows:

15 33. (Amended) A method of manufacturing a semiconductor device, comprising:

a¹ a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

a third step of [forming an element on said active region;

a fourth step of] forming depressed portions by etching said dummy semiconductor portions and filling an insulating material in said depressed portions to form inter-trench insulating films each having a top face at the same level as respective top faces of said first and second buried trench portions;

a fourth step of forming an element on said active region;

cont 1
a1
a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating film.

18
36. (Amended) A method of manufacturing a semiconductor device, comprising:

a2
a first step of forming, in a semiconductor substrate having a substrate region, a first trench for partitioning said substrate region into an active region and an isolation region and a second trench for partitioning said isolation region into a plurality of dummy semiconductor portions;

a second step of filling an insulating material in each of said first and second trenches to form a first buried trench portion and a second buried trench portion;

a third step of [forming an element on said active region;

a fourth step of] implanting oxygen ions into each of said dummy semiconductor portions with said active region being covered by a mask to form a buried insulating film in an inner portion thereof;

a fourth step of forming an element on said active region;

a fifth step of forming an interlayer insulating film over an entire surface of the substrate; and

a sixth step of forming a wire on said interlayer insulating film.

R E M A R K S

I. Introduction

In response to the outstanding Office Action, Applicants have amended Fig. 1(a) to indicate that reference numeral 9 corresponds to the "dummy semiconductor portion", and not the trench portion as erroneously indicated in the figure as originally filed. Support for the amendment can be found on page 27, lines 10-11 of the specification. Applicants would like to thank the Examiner for the indication of allowance of claims 22-35, 37 and 38. Applicants respectfully traverse the rejection of claims 19-21 and 36 under 35 U.S.C. § 103 for the reasons set forth below.

Finally, claims 1-18 have been cancelled, without prejudice. Claims 1-18 were subject to a restriction requirement and were not elected for prosecution on the merits in the instant application. Claims 33 and 36 have been amended so as to more particularly recite the subject matter that the Applicants regard as the invention.

II. The Rejection Of Claims 19 And 36 Under 35 U.S.C. § 103

Claims 19-21 were rejected under 35 U.S.C. § 103 as being unpatentable over the Applicants' Admitted Prior Art (AAPA) in view of Kinoshita et al. (USP No. 5,856,218). Claim 36 was rejected under 35 U.S.C. § 103 as being unpatentable over the Applicants' Admitted Prior Art (AAPA) in view of Beitman (USP No. 4,929,566). Applicants respectfully traverse the pending rejections for the reasons set forth below.

A. Claims 19-21

Claim 19 recites a novel method of manufacturing a trench-isolated semiconductor device. One of the novel features of the claim resides in the fourth step, wherein an impurity containing at least an impurity of a second conductivity type is introduced into dummy semiconductor portions, which are formed by forming a second trench in an isolation region. The introduction of the impurity into the dummy semiconductor portions results in the formation of at least one PN junction in the dummy semiconductor portions, which produces significant advantages and solves problems associated with prior art devices.

More specifically, it is a known technique to form dummy semiconductor portions in an isolation region in order to obtain an isolation region having a planarized surface. Indeed, without such dummy semiconductor portions, it would be difficult to obtain a planarized surface of the isolation region. However, prior to the present invention there has been the problem that the formation of the dummy semiconductor portions increases the wiring-to-substrate capacitance in the isolation region, as described in the "BACKGROUND OF THE INVENTION" portion of the specification and Figs. 21(a)-21(c).

The Applicants' have discovered that in order to overcome this problem, according to the claimed method, a PN junction is formed within the dummy semiconductor portions in the isolation region. As shown in Fig. 1(b) while formation of the dummy semiconductor portions 9 produces an additional capacitance C_{j1} , because of formation of the PN junction 22 within the dummy semiconductor portions 9, the capacitance C_{j1} is added in series to a capacitance C_{a1} , which decreases the wiring-to-

substrate capacitance in the isolation region. As a result, the operation speed of the device is advantageously increased.

Turning to the cited art, it is asserted that because Kinoshita teaches implantation of N-type impurity into a P-type substrate to form N-type source/drain regions 17, an N+ layer 20 and an N layer 22, Kinoshita suggests formation of at least one PN junction. It is then concluded that because Kinoshita discloses the formation of a PN junction, the combination of Kinoshita and the AAPA renders the claimed invention obvious. Applicants respectfully disagree.

First and foremost, there is absolutely no motivation to combine Kinoshita with the AAPA as set forth in the Office Action. Kinoshita does not disclose a trench-isolated semiconductor device having dummy semiconductor portions (Kinoshita relates to the formation of a bi-polar transistor wherein the isolations 12 extend above the surface of the semiconductor substrate), and Kinoshita neither acknowledges nor addresses the problem solved by the present invention. Accordingly, there is no motivation, whatsoever, found in Kinoshita that would suggest forming a PN junction in the dummy semiconductor portion of the claimed trench-isolated semiconductor to decrease the wiring-to-substrate capacitance in the isolation region. As such, the rejection is clearly in error.

Furthermore, it is also noted that all of the N-type source/drain regions 17, the N+ layer 20 and the N layer 22 layer in Kinoshita are formed *in an active region* for forming a transistor, not in dummy semiconductor portions which are formed in the isolation region as claimed by the present invention. More specifically, in Kinoshita, the N-type source/drain region 17 forms collector electrode junction of the NPN bipolar

translator 25, the N+ layer 20 forms an emitter electrode junction of the NPN bipolar transistor 25, and the N+ layer 22 is a diffusion layer forming a transistor. Thus, it is clear that Kinoshita does not disclose forming PN junctions in dummy semiconductor portions.

It is well known that the fact that the prior art could be modified so as to result in the combination defined by the claims at bar would not have made the modification obvious unless the prior art suggests the desirability of the modification. *In re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986).

Moreover, recognizing after the fact that such a modification would provide an improvement or advantage, without suggestion thereof by the prior art, rather than dictating a conclusion of obviousness, is an indication of improper application of hindsight considerations. Simplicity and hindsight are not proper criteria for resolving obviousness. *In re Warner*, 379 F.2d 1011, 154, USPQ 173 (CCPA 1967).

It is only Applicants' disclosure that discloses the formation of a PN junction in the dummy semiconductor portion of the claimed trench-isolated semiconductor to decrease the wiring-to-substrate capacitance in the isolation region. Neither AAPA nor Kinoshita describe or suggest this claimed feature. Moreover, Kinoshita does not even acknowledge the problems solved by the present invention. Thus, the only motivation of record for the proposed modification of the device of AAPA to arrive at the claimed invention is found in Applicants' disclosure which, of course, may not properly be relied upon to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 227 1 USPQ2d 1593 (Fed. Cir. 1987).

For all of the foregoing reasons, the Applicants' admitted prior art and Kinoshita, even if combined, do not render the present invention, as recited by claims 19-21, obvious.

B. Claim 36

Claim 36 also recites a novel method of manufacturing a trench-isolated semiconductor device having dummy semiconductor portions. One of the novel features of the claim resides in the third step (as amended), wherein oxygen ions are implanted into each of dummy semiconductor portions, which are formed by forming a second trench in an isolation region so as to form a buried insulating film in an inner portion of each of the dummy semiconductor portions. The formation of the buried insulation film produces the same advantages that are produced by the method recited by claims 19-21.

Turning to the pending rejection, similar to the rejection of claims 19-21, it is asserted that the combination of a reference (Beitman) that merely discloses implanting oxygen ions to form a buried insulating film and the AAPA renders the claimed invention obvious. For the same reasons as set forth above, it is respectfully submitted that there is no motivation to combine Beitman with the AAPA, and therefore the pending rejection does not establish a *prima facie* case of obviousness and should be withdrawn.

More specifically, Beitman merely discloses that oxygen ions are implanted into the epitaxial layer 20 on a substrate 10, which includes an insulative layer 12. Beitman fails to disclose or suggest that implantation of oxygen ions is performed on an inner

portion of the dummy semiconductor portions with an active region covered with a mask so as to form a buried insulating film only in an inner portion of each of the dummy semiconductor portions, which are formed in an isolation region, as claimed. Further, as with Kinoshita, Beitman does not even appear to address the issue of reducing a wiring-to-substrate capacitance in an isolation region.

It is only Applicants' disclosure that discloses the formation of a buried insulating film in the dummy semiconductor portion of the claimed trench-isolated semiconductor to decrease the wiring-to-substrate capacitance in the isolation region. Neither AAPA nor Beitman describe or suggest this claimed feature. Moreover, Beitman does not even acknowledge the problems solved by the present invention. Thus, the only motivation of record for the proposed modification of the device of AAPA to arrive at the claimed invention is found in Applicants' disclosure which, of course, may not properly be relied upon to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103.

Panduit Corp. v. Dennison Mfg. Co., 810 F.2d 1561, 227 1 USPQ2d 1593 (Fed. Cir. 1987).

For all of the foregoing reasons, the Applicants' admitted prior art and Beitman, even if combined, do not render the present invention, as recited by claim 36, obvious.

III. REQUEST FOR NOTICE OF ALLOWANCE

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: September 9, 1999

By: _____


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087
89W388967751A1MDMAF.001

Approved!
KBD 9/30/99

Fig. 1(a)

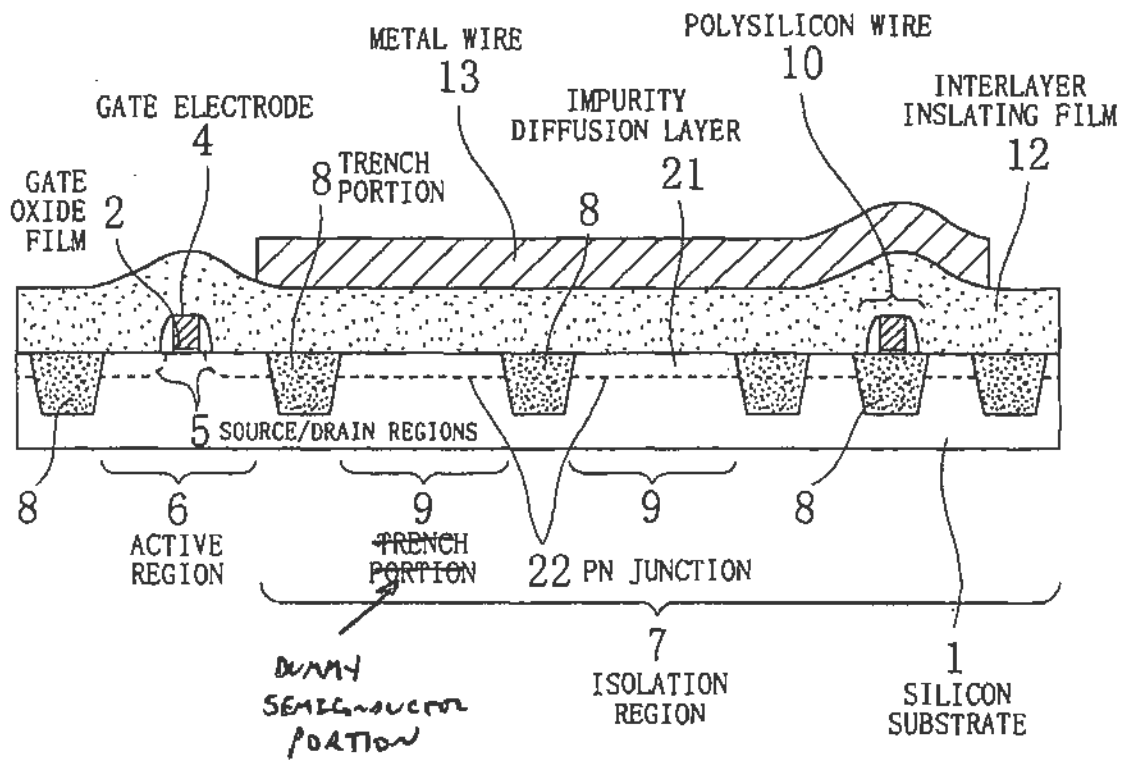
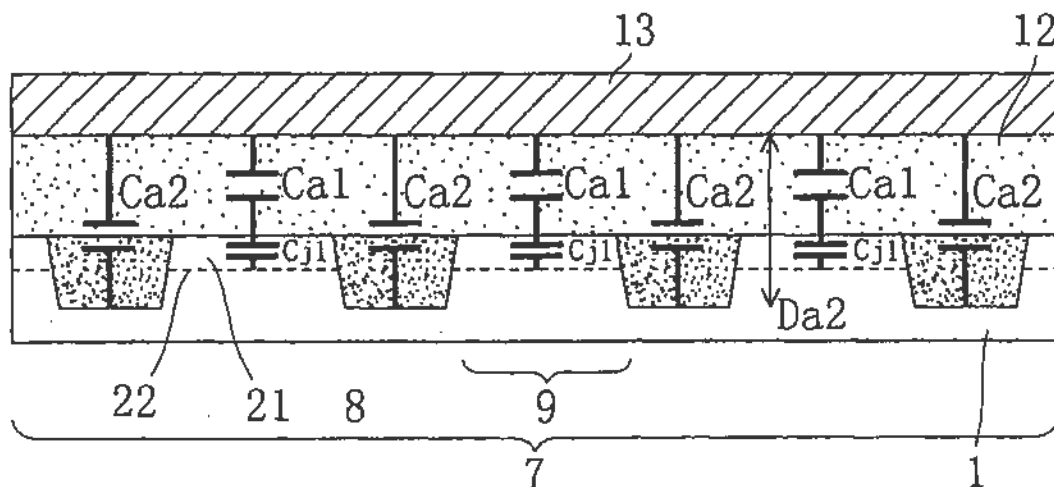


Fig. 1(b)





**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
087978,137	11/25/97	OKEDA	43889-677

KENNETH L. CAGE
MCDERMOTT WILL & EMERY
1850 K STREET, NW
SUITE 500
WASHINGTON DC 20006

MM21/1001

EXAMINER

DUONG, R.

ART UNIT

PAPER NUMBER

2822

DATE MAILED:

10/01/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Notice of Allowability

Application No.

08/978,137

Applicant(s)

Okeda et al.

Examiner

Khanh Duong

Group Art Unit

2822



All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to Sept 9, 1999

☒ The allowed claim(s) is/are 19-38

☐ The drawings filed on _____ are acceptable.

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftsperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____

☒ including changes required by the proposed drawing correction filed on Sept 9, 1999, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☒ Examiner's Statement of Reasons for Allowance

Carl Whitehead, Jr.
Carl Whitehead, Jr.
Supervisory Patent Examiner
Semiconductor Technology

Art Unit: 2822

DETAILED ACTION

1. In response to the Amendment dated September 9, 1999, claims 19-38 are active in this application and claims 1-18 are cancelled.

Drawings

2. The corrected or substitute drawings were received on September 9, 1999. These drawings are approved.

Examiner's Amendment

3. The application has been amended as follows: Please substitute the title with the following new title: --METHOD OF MANUFACTURING TRENCH-ISOLATED SEMICONDUCTOR DEVICE--.

Allowable Subject Matter

4. Claims 19-38 are allowed.
5. The following is an examiner's statement of reasons for allowance: the prior art of record does not show or suggest a method for fabricating a semiconductor device comprising the steps of: *filling an insulating material in each of the first and second trenches to form a first buried trench portion and a second buried trench portion; forming an element on the active region; introducing an impurity containing at least an impurity of a second conductivity type into the dummy semiconductor portions of the isolation region to form at least one PN junction in the dummy semiconductor portions; forming an interlayer insulating film over an entire surface of the substrate; forming a wire on the interlayer insulating film.*

Art Unit: 2822

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contacts Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Khanh Duong* whose telephone number is (703) 308-5840. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Carl Whitehead*, can be reached at (703) 308-4940. The fax numbers for the Group is (703) 305-3431 and (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (703) 308-0956.


KBD

October 1, 1999


Carl Whitehead, Jr.
Supervisory Patent Examiner
Semiconductor Technology



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

MM21/1001

KENNETH L. CAGE
MODERMOTT WILL & EMERY
1850 K STREET NW
SUITE 500
WASHINGTON DC 20006

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/978,137	11/25/97	020	DUONG, K	2822 10/01/98
First Named Applicant	UKEDA, 35 USC 154(b) term ext. = 0 Days.			

TITLE OF INVENTION METHOD OF MANUFACTURING TRENCH-ISOLATED SEMICONDUCTOR DEVICE
(AS AMENDED)

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2	43889-677	438-424.000	C61 UTILITY	NO	\$1210.00	01/03/99

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
- B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

- A. Pay FEE DUE shown above, or
- B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

- II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.
- III. All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

Docket No.: 43889-677



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Takaaki UKEDA, et al.

Serial No.: 08/978,137

Filed: November 25, 1997

BATCH NO.: C61
Group Art Unit: 2822
Allowed: October 01, 1999
Examiner: K. Duong

RECEIVED

NOV 04 1999

PUBLICATION DIVISION
62

For: METHOD OF MANUFACTURING TRENCH-ISOLATED SEMICONDUCTOR
DEVICE (AS AMENDED)

AMENDMENT UNDER 37 CFR 1.312

Box Issue Fee
Assistant Commissioner for Patents
Washington, DC 20231

Sir:

We are in receipt of the Notice of Allowance dated October 01, 1999, issued in connection with the above-identified application.

Please make the following changes in the specification:

IN THE SPECIFICATION

Page 25, line 17, change "(h)" to --(i)--; and

Page 26, line 18, change "FIG. 21 is a cross-sectional view" to --FIGS. 21(a) and 21(b) are cross-sectional views--.

08/978,137

REMARKS

The drawing corrections required in the Notice of Allowability and PTO 948 have now been made. The corrected formal drawings are being filed concurrently herewith. The above amendment was made to have the specification correspond to the required drawing changes and does not contain any new matter. Accordingly, it is respectfully requested that this amendment be entered.

Respectfully submitted,

MCDERMOTT, WILL & EMERY


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 MEF:th
Date: November 3, 1999
Facsimile: (202) 756-8087

Docket No.: 43889-677

#12
OIA 4/14/00
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Takaaki UKEDA, et al.

Serial No.: 08/978,137

Filed: November 25, 1997



BATCH NO.: C61

Group Art Unit: 2822

Allowed: October 01, 1999

Examiner: K. Duong

For: METHOD OF MANUFACTURING TRENCH-ISOLATED SEMICONDUCTOR
DEVICE (AS AMENDED)

LETTER SUBMITTING FORMAL DRAWINGS

Box Issue Fee

Assistant Commissioner for Patents

Washington, DC 20231

Sir:

In response to the Notice of Allowability dated October 01, 1999, submitted herewith are
twenty-one (21) sheets of Formal Drawings in connection with the above referenced application.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

A handwritten signature in cursive script, appearing to read "Michael E. Fogarty".

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 MEF:th
Date: November 3, 1999
Facsimile: (202) 756-8087

6130139

Fig. 1(a)

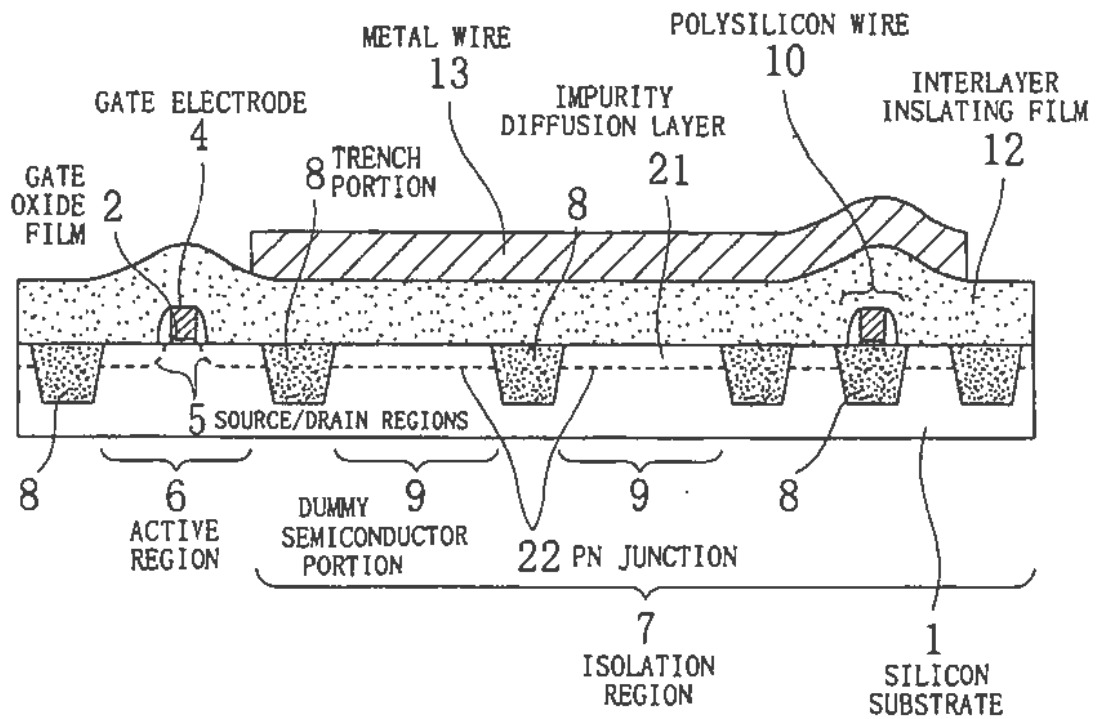
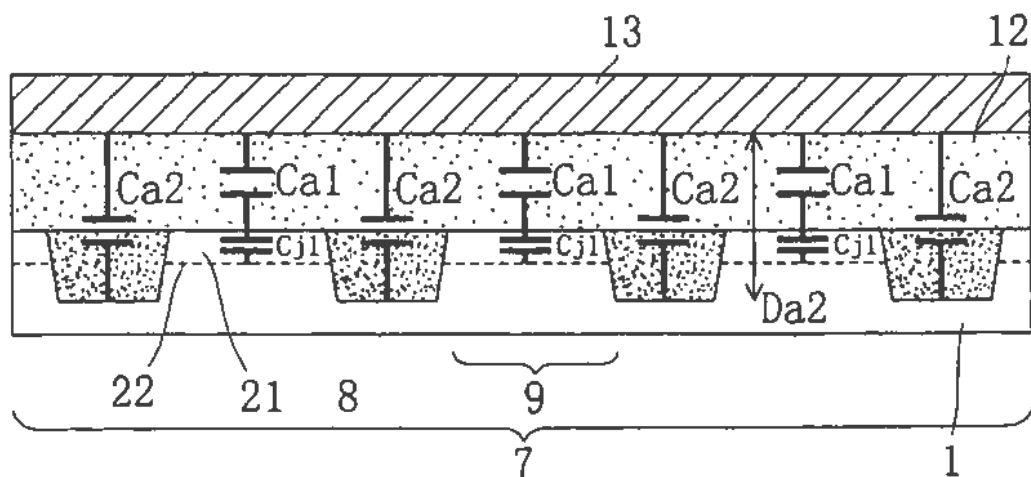


Fig. 1(b)



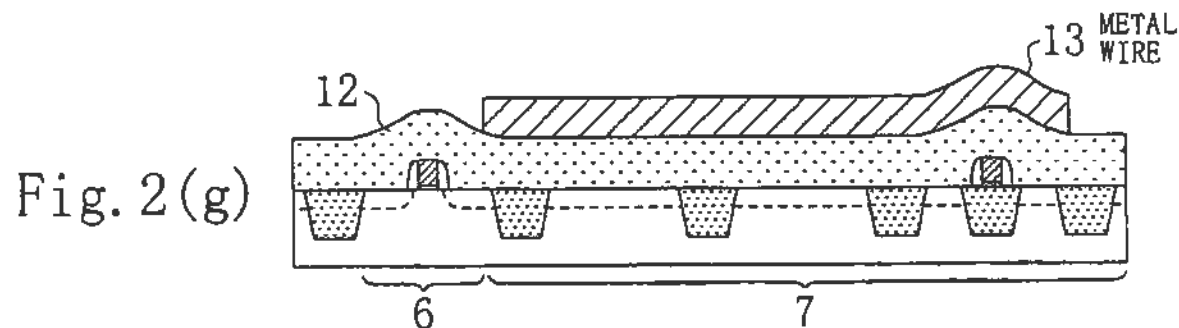
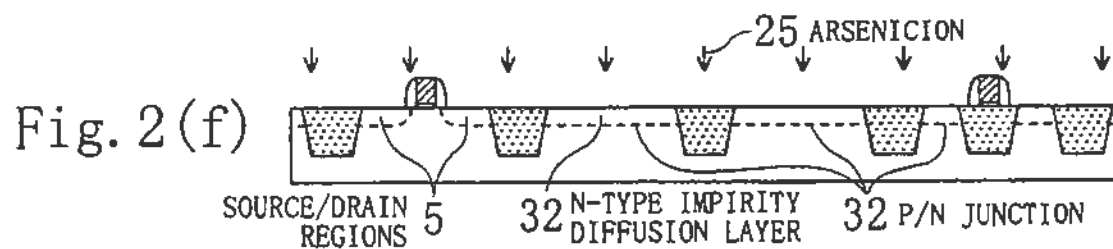
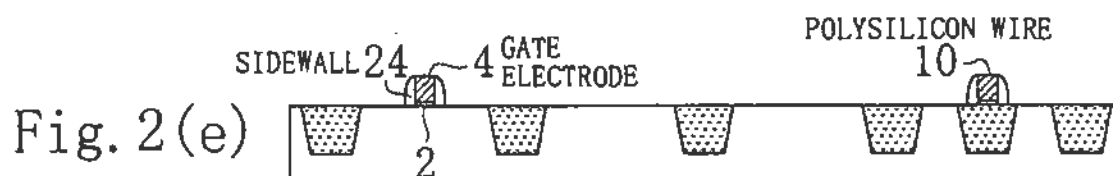
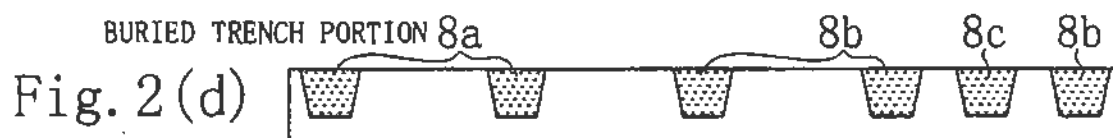
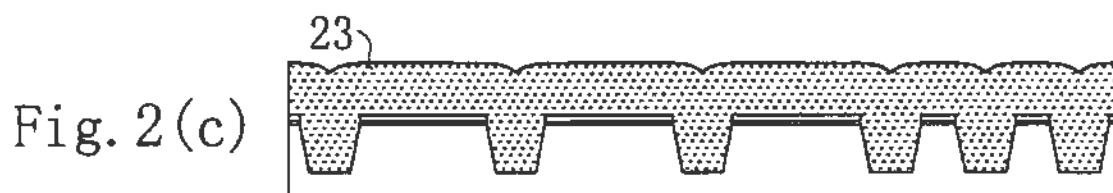
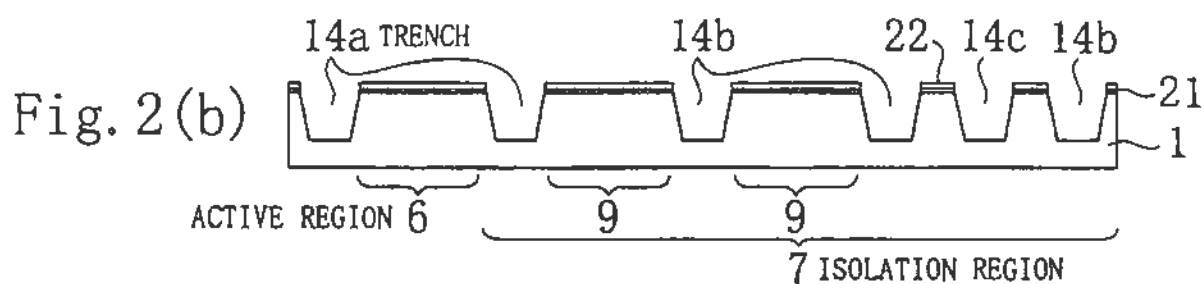


Fig. 3

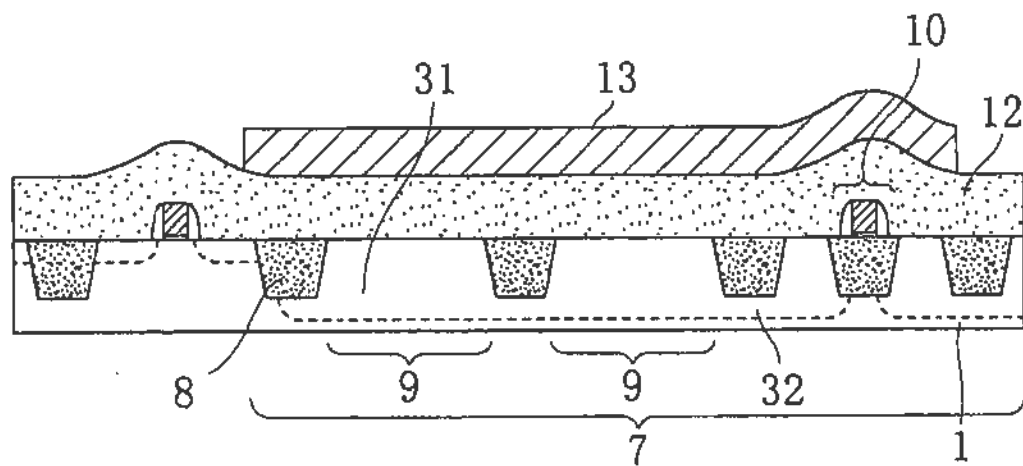


Fig. 4

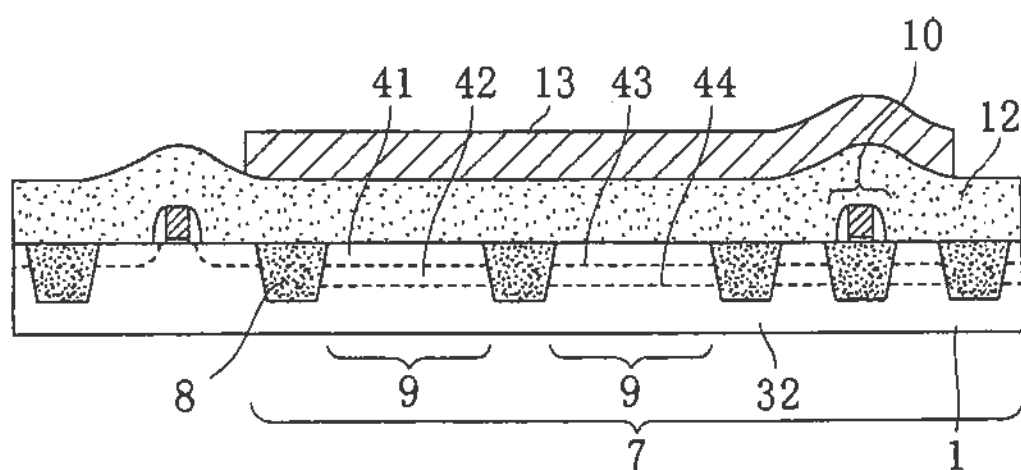


Fig. 5

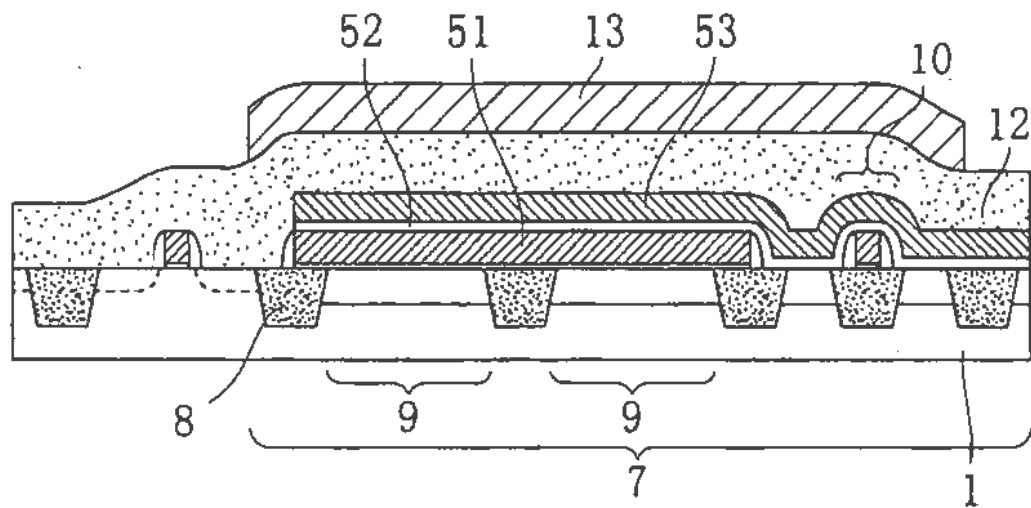


Fig. 7

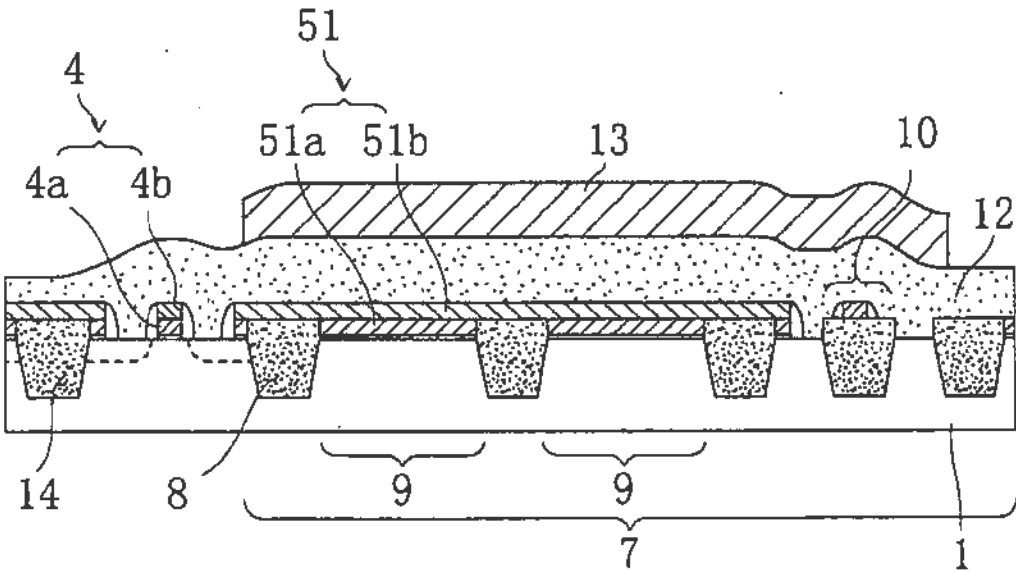
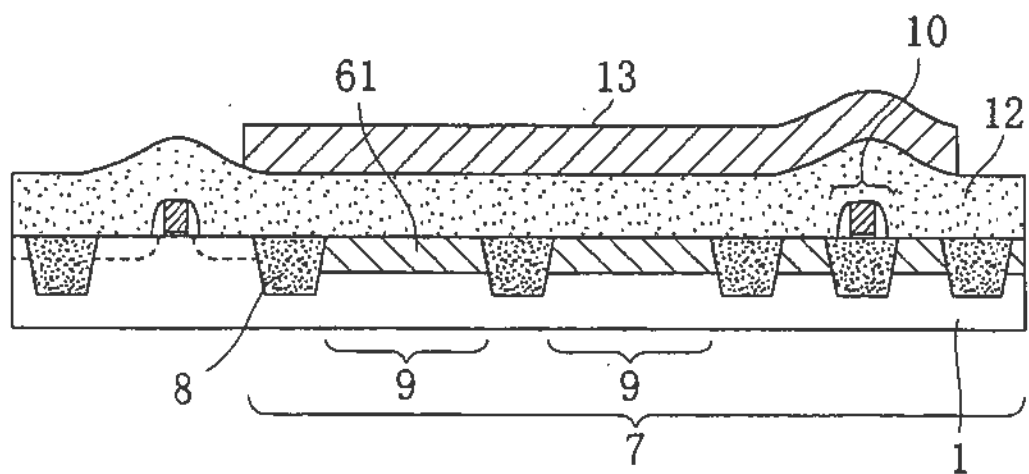


Fig. 8



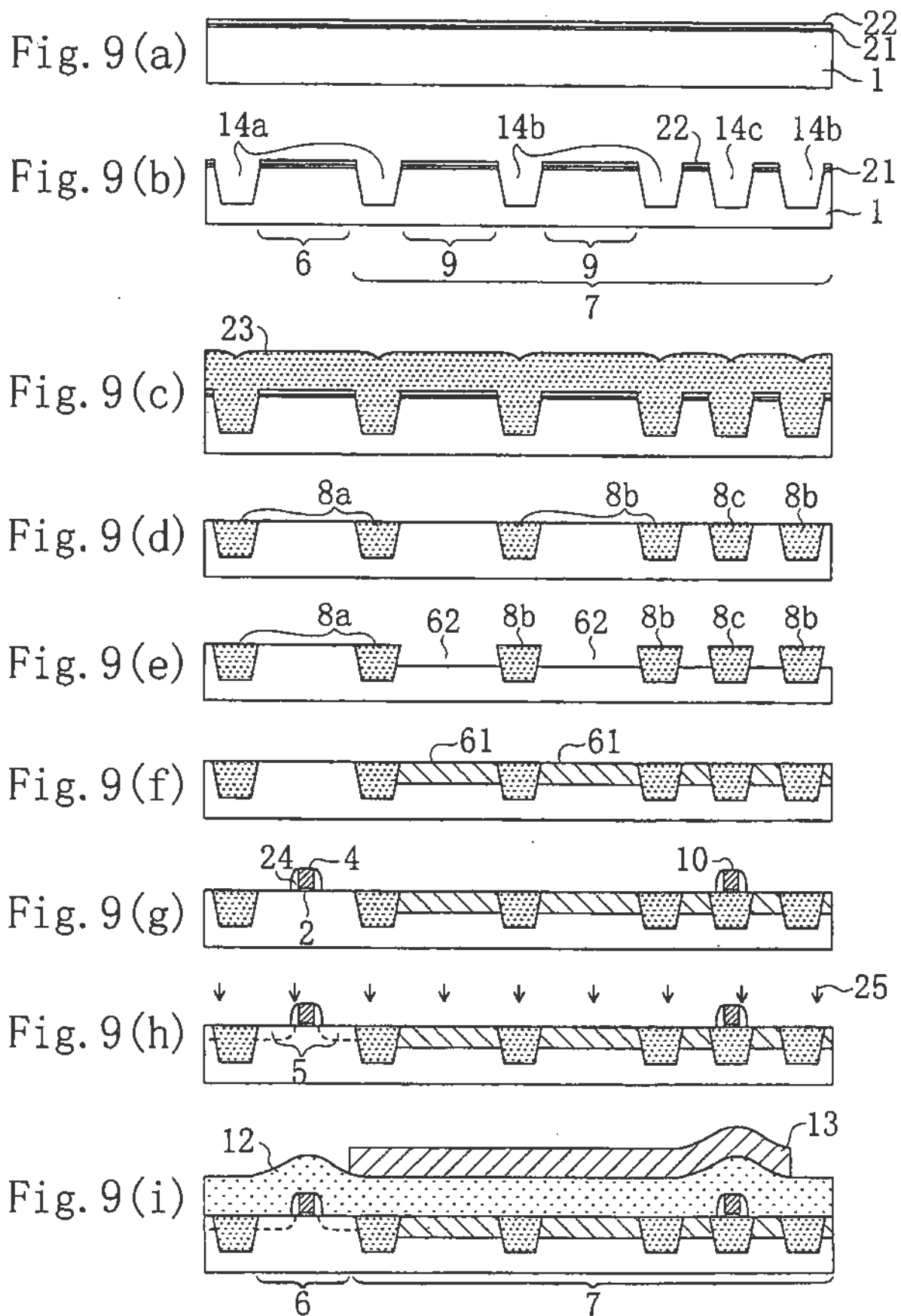
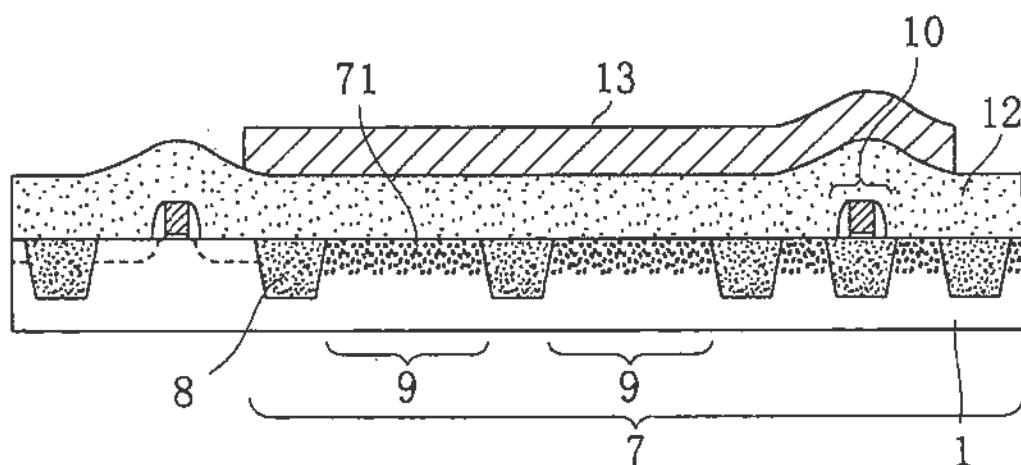


Fig. 10



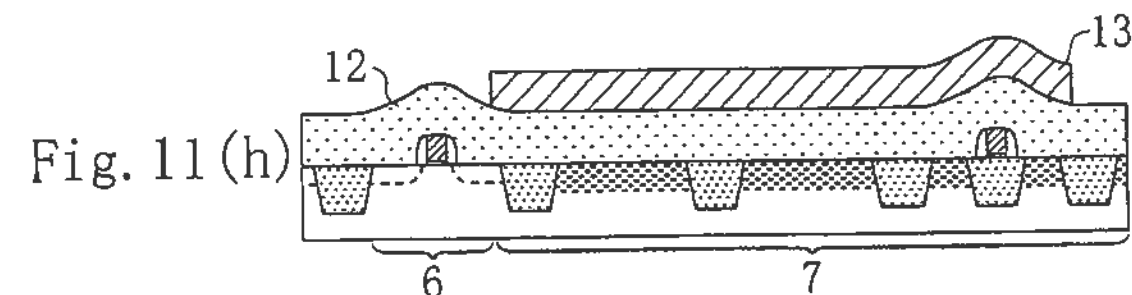
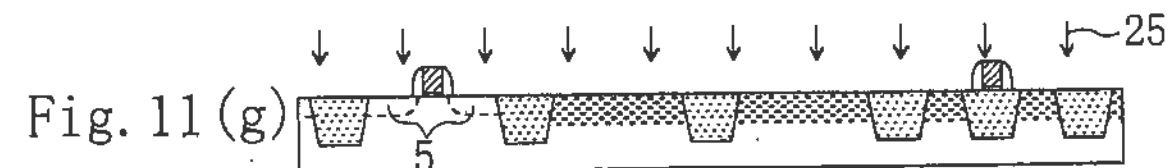
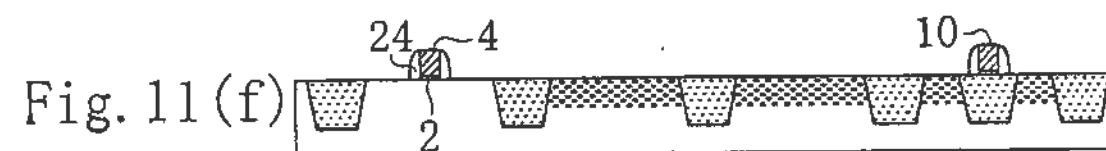
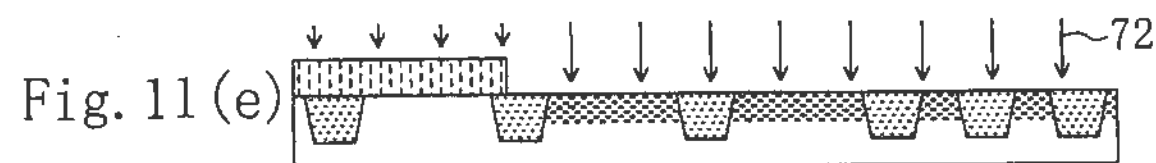
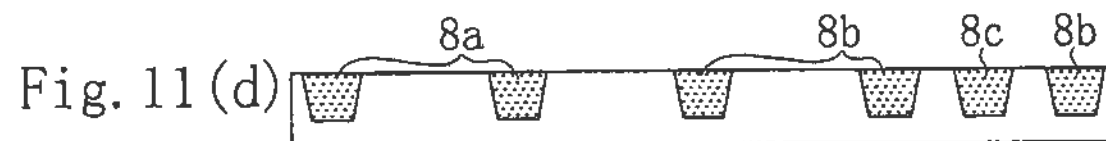
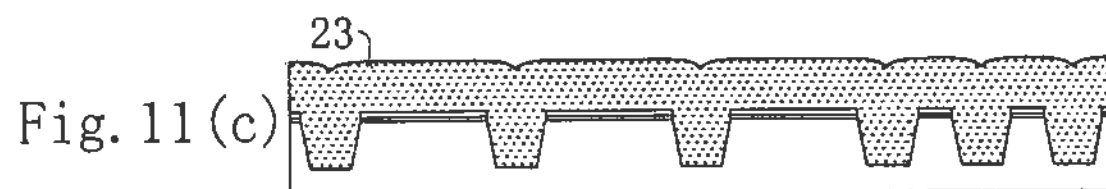
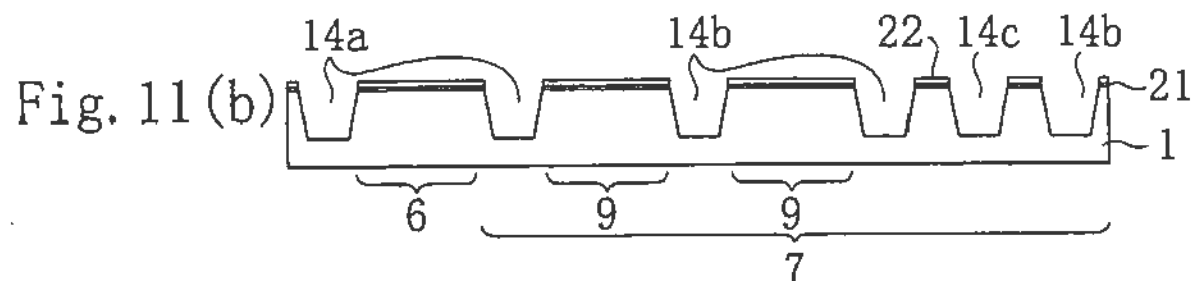
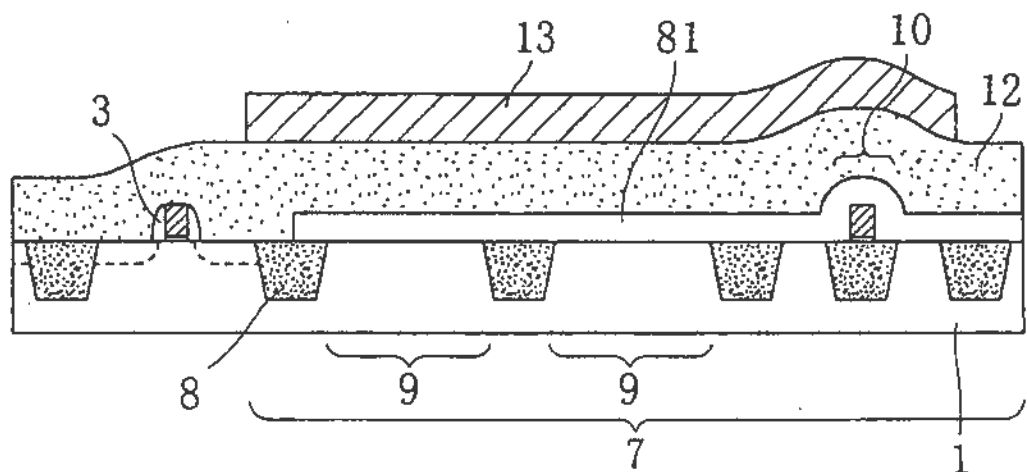


Fig. 12



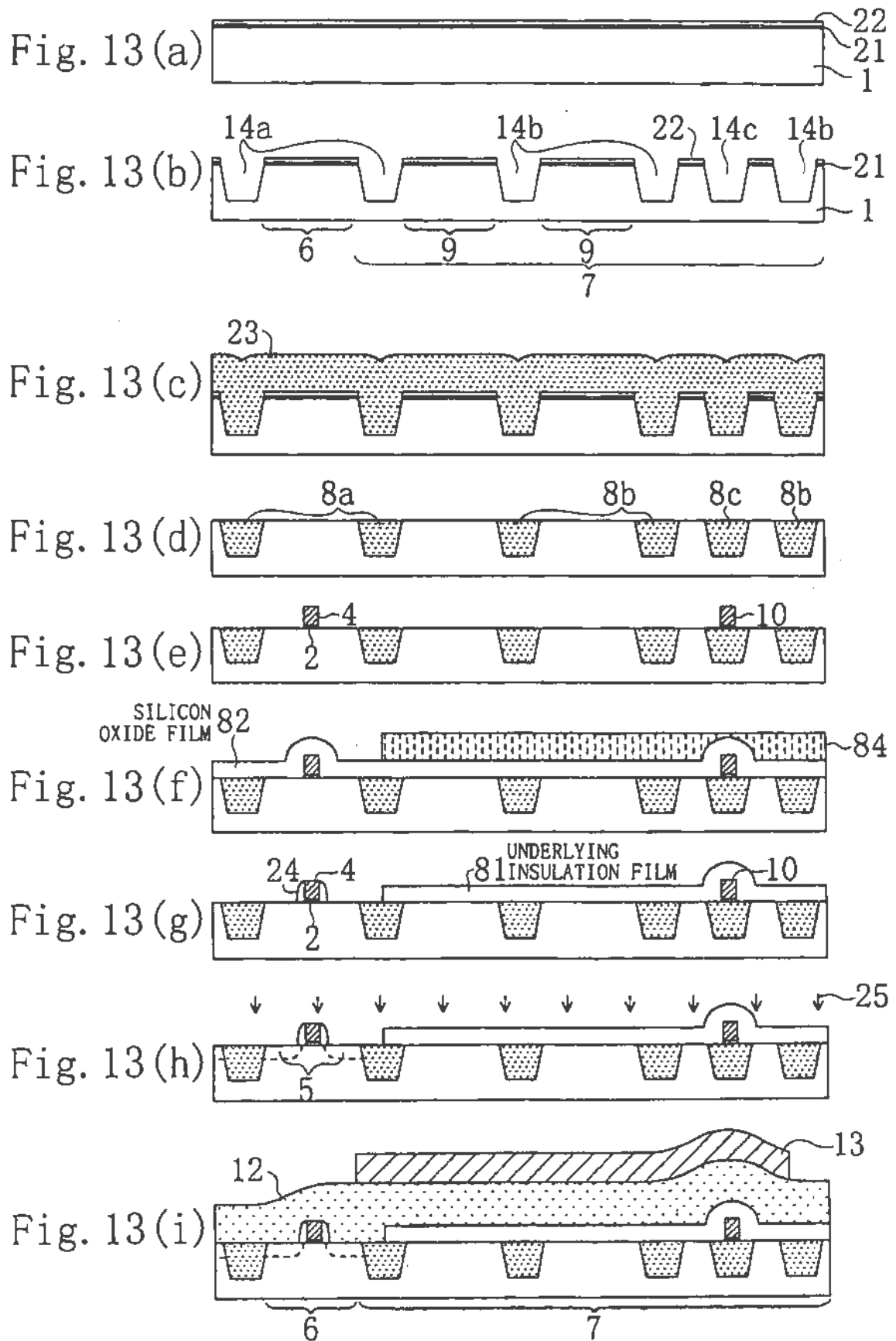


Fig. 14(a)

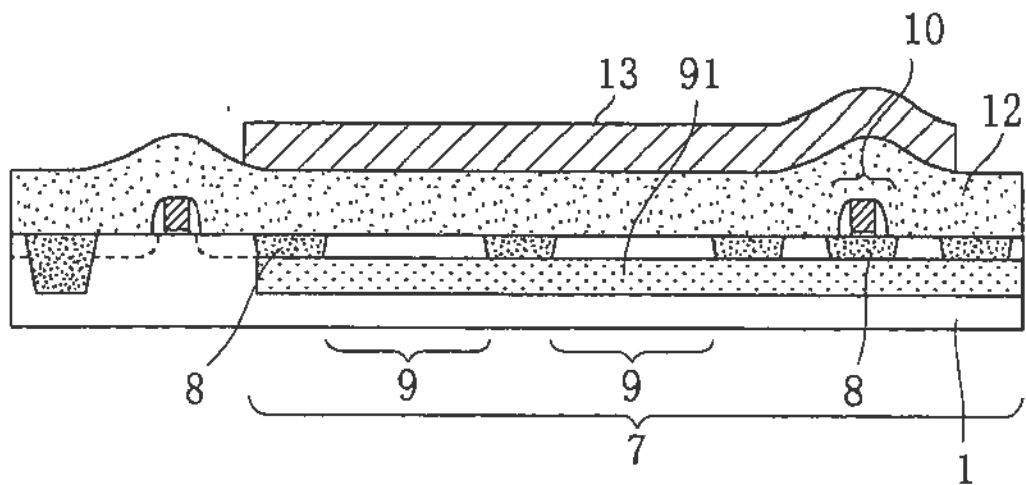
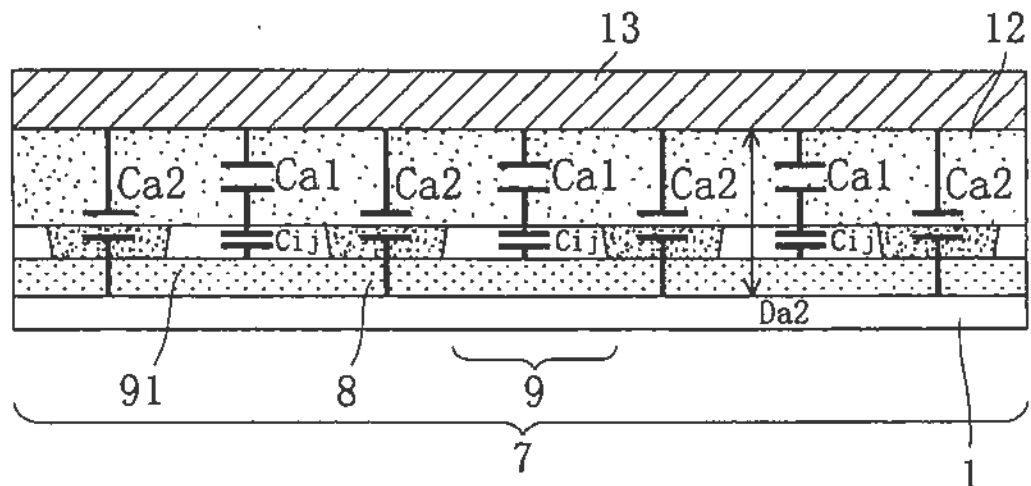


Fig. 14(b)



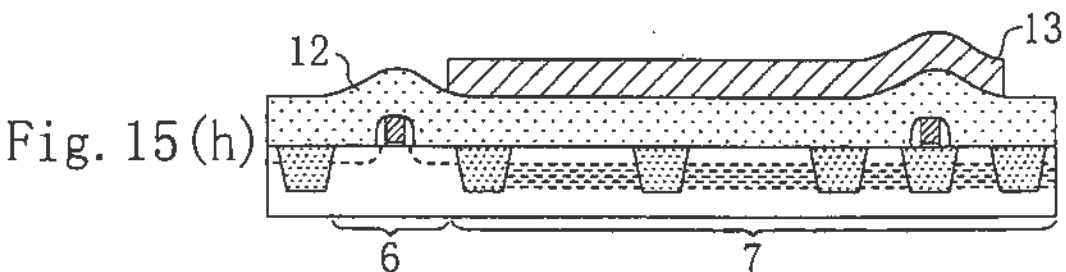
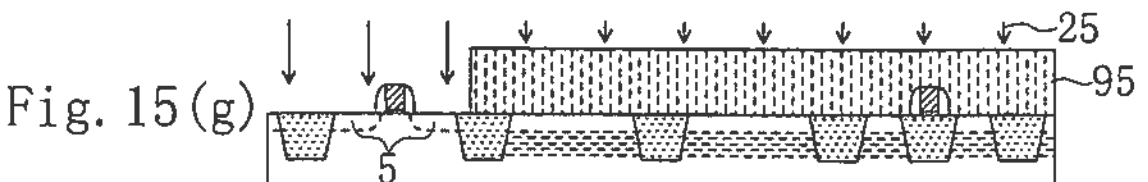
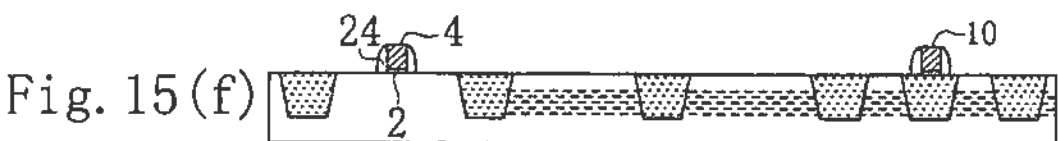
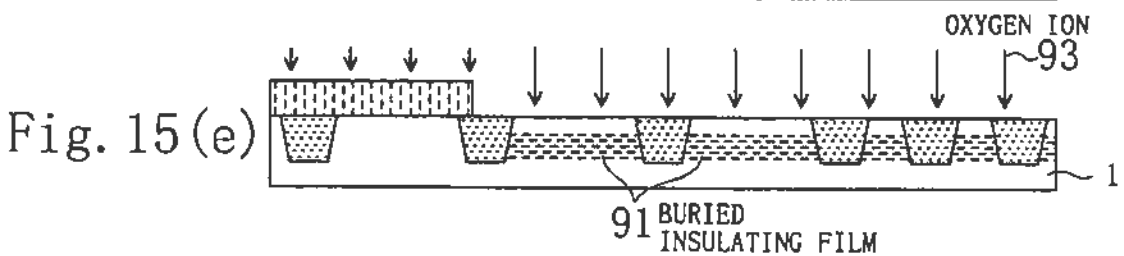
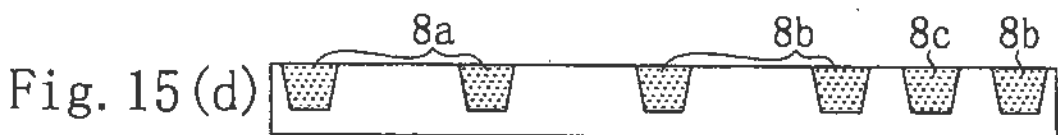
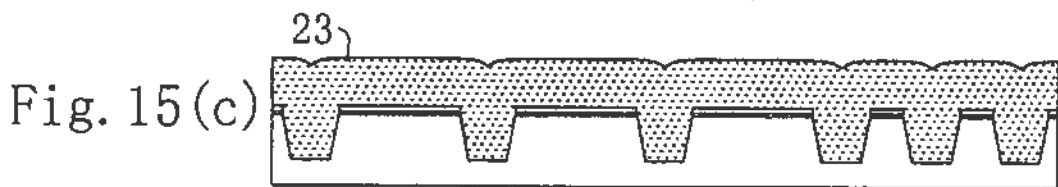
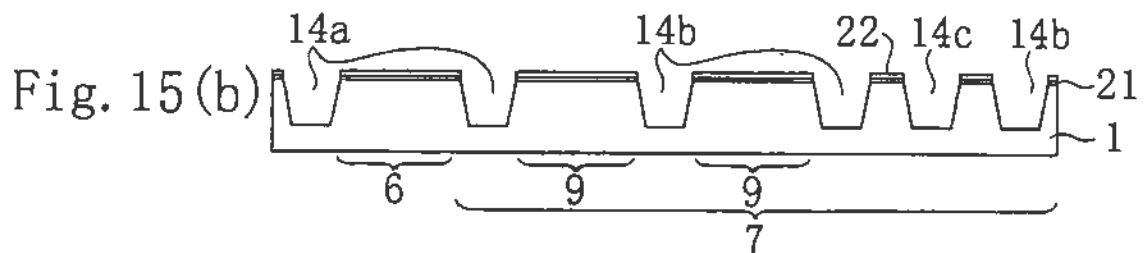
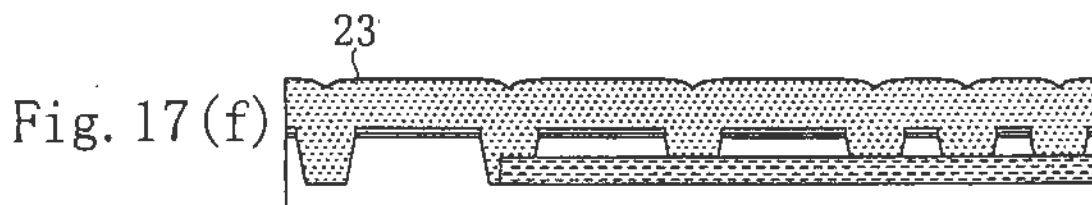
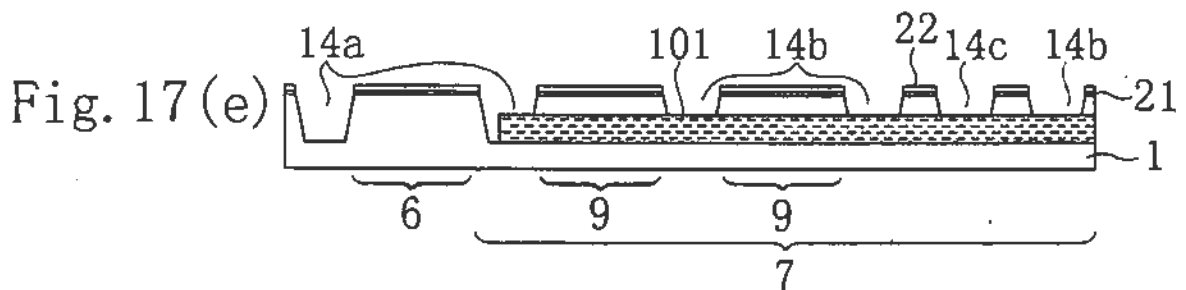
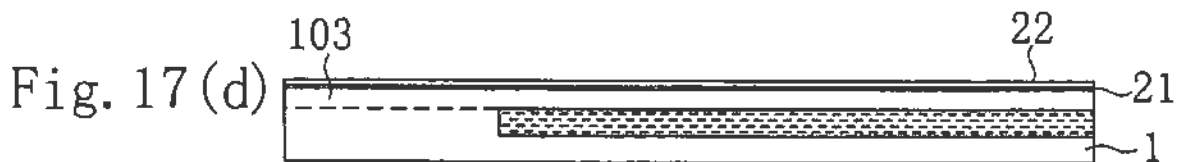
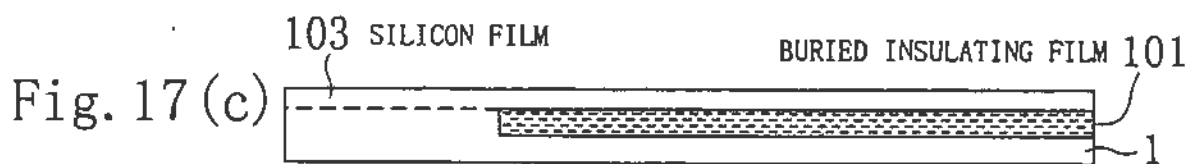


Fig. 1 is a perspective view of a rectangular plate 1. The plate has a top surface 21 and a bottom surface 22.

A cross-sectional view of a semiconductor device. A substrate 1 is shown with a series of rectangular structures 21 on its surface. Each structure 21 consists of a top layer 22 and a bottom layer 14. The bottom layer 14 is divided into three regions: 14a, 14b, and 14c. The width of region 14a is labeled 6, the width of region 14b is labeled 9, and the width of region 14c is labeled 7. The total width of the bottom layer 14 is labeled 9. The top layer 22 is shown as a thin layer on top of the bottom layer 14.

91 97 SEMICONDUCTOR PORTION 1



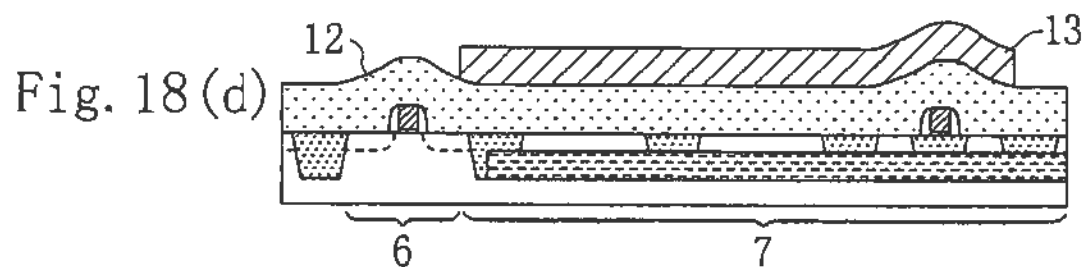
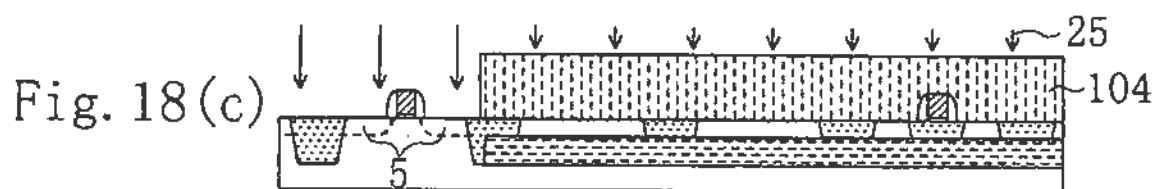
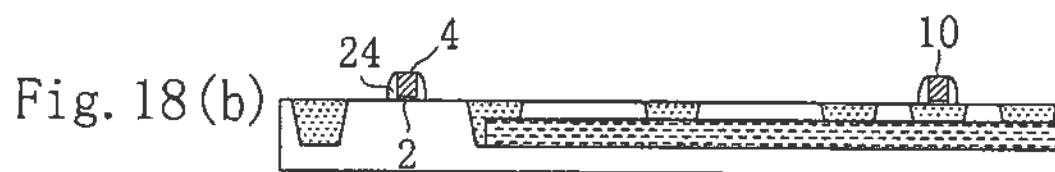
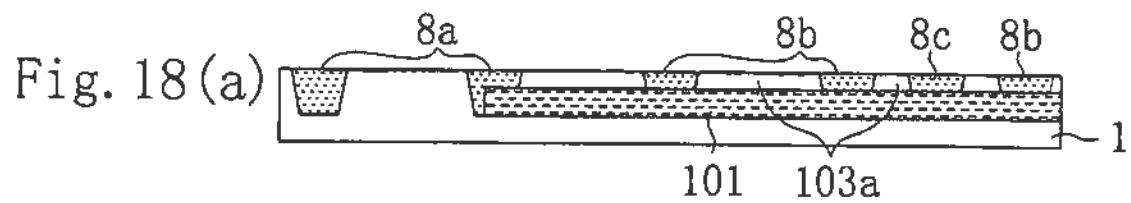


Fig. 19
PRIOR ART

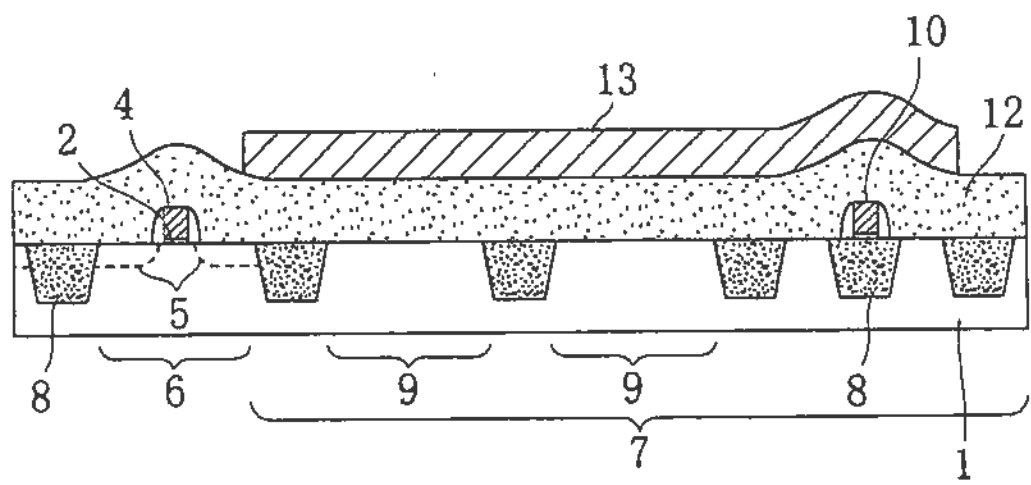


Fig. 20(a)
PRIOR ART



Fig. 20(b)
PRIOR ART

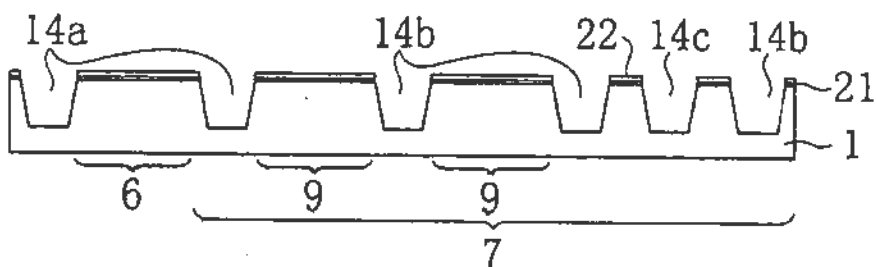


Fig. 20(c)
PRIOR ART

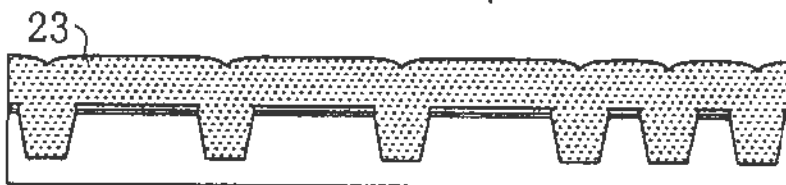


Fig. 20(d)
PRIOR ART

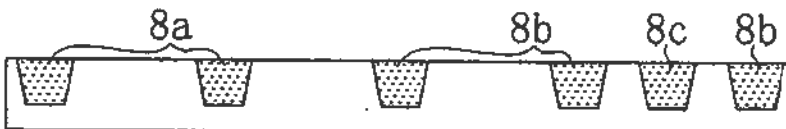


Fig. 20(e)
PRIOR ART

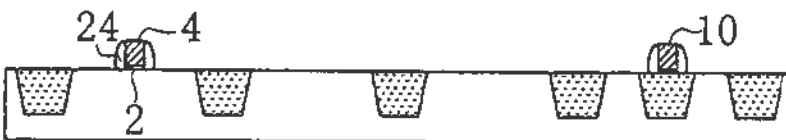


Fig. 20(f)
PRIOR ART

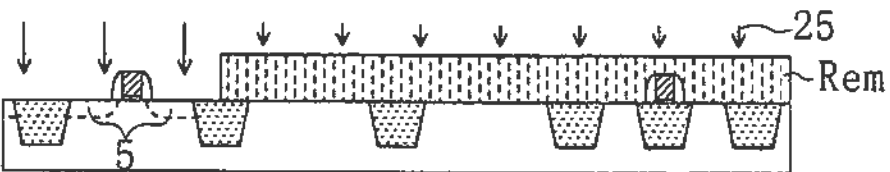


Fig. 20(g)
PRIOR ART

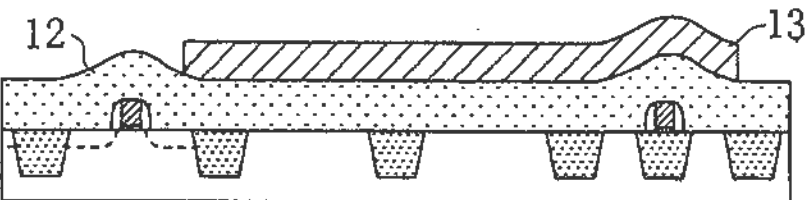


Fig. 21(a)

PRIOR ART

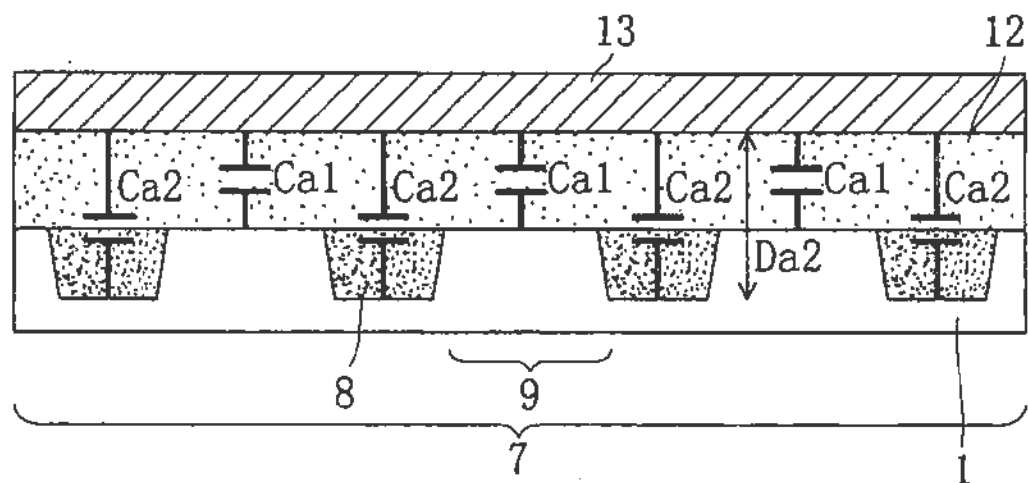
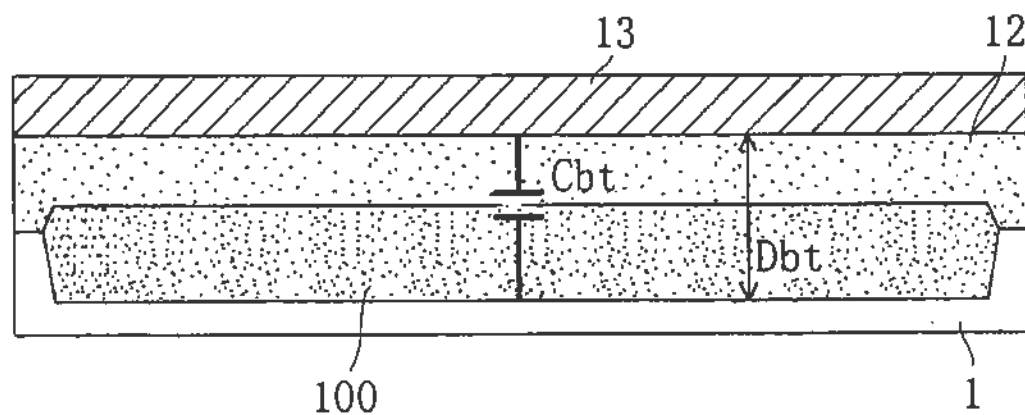


Fig. 21(b)

PRIOR ART



STATUS
093

PART B—ISSUE FEE TRANSMITTAL

WO

Complete and mail this form, together with applicable fees, to:

Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

KENNETH L. GAGE
MCDERMOTT WILL & EMERY
1000 K STREET NW
SUITE 500
WASHINGTON DC 20006

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I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FLING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/978,137	11/25/97	020	DUONG, K	2822 10/01/99
First Named Applicant	UKEDA,	35 USC 154(b) term ext. =	0 Days.	

TITLE OF INVENTION

METHOD OF MANUFACTURING TRENCH-ISOLATED SEMICONDUCTOR DEVICE
(AS AMENDED)

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPL. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2	43889-677	438-424.000	C61	UTILITY	NO	\$1210.00 01/03/00

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
Use of PTO form(s) and Customer Number are recommended, but not required.

☒ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. MCDERMOTT, WILL &2. EMERY

3. _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

(B) RESIDENCE: (CITY & STATE OR COUNTRY)

Osaka, JAPAN

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ Individual☒ corporation or other private group entity☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

☐ Issue Fee☐ Advance Order - # of Copies _____

4b. The following fees or deficiency in these fees should be charged to:
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☒ Issue Fee☐ Advance Order - # of Copies _____

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature)

Michael E. Fogarty, Reg. #36,139

(Date)

12/10/99

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

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TRANSMIT THIS FORM WITH FEE

Docket No.: 43889-677

#13 TW 427.00
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Takaaki UKEDA, et al.

Serial No.: 08/978,137

Filed: November 25, 1997



Batch No.: C61

Group Art Unit: 2822

Allowed: 10/1/99

Examiner: K. Duong

For: **METHOD OF MANUFACTURING TRENCH-ISOLATED SEMICONDUCTOR
DEVICE (AS AMENDED)**

Honorable Commissioner of
Patents and Trademarks
Washington, D. C. 20231

CORRESPONDENCE ADDRESS CHANGE

Sir:

Please change the records to indicate the current firm name and telephone number for the
above-identified application and forward all future correspondence as follows:

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

202-756-8000
Facsimile: 202-756-8087

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Michael E. Fogarty
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600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 MEF:th
Date: December 10, 1999
Facsimile: (202) 756-8087

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12
TECH 6

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Publishing Division

DEC 20 1999

11
TECH 6

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2000-10-10

Document Title - USPTO Grant

PATENT APPLICATION FEE DETERMINATION RECORD

Effective November 10, 1998

Application or Docket Number

CLAIMS AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	minus 20 = *	
INDEPENDENT CLAIMS	minus 3 = *	
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY
TYPE ☐

OR OTHER THAN
SMALL ENTITY

RATE	FEE	OR	RATE	FEE
	380.00			760.00
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1)	(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 20	Minus ** 38	=
Independent	* 8	Minus *** 12	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

SMALL ENTITY

OR OTHER THAN
SMALL ENTITY

RATE	ADDI- TIONAL FEE	OR	RATE	ADDI- TIONAL FEE
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1)	(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

RATE	ADDI- TIONAL FEE	OR	RATE	ADDI- TIONAL FEE
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1)	(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

RATE	ADDI- TIONAL FEE	OR	RATE	ADDI- TIONAL FEE
X\$ 9=		OR	X\$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

- * If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 - ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
 - *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
- The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1997

Application or Docket Number

8/978, 137

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	38 minus 20 =	18
INDEPENDENT CLAIMS	12 minus 3 =	9
MULTIPLE DEPENDENT CLAIM PRESENT		N

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐

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	395.00
x\$11=	
x41=	
+135=	
TOTAL	

OR OTHER THAN SMALL ENTITY

RATE	FEE
	790.00
x\$22=	396.00
x82=	738.00
+270=	
TOTAL	1924.00

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

SMALL ENTITY

RATE	ADDITIONAL FEE
x\$11=	
x41=	
+135=	
TOTAL ADDIT. FEE	

OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
x\$22=	
x82=	
+270=	
TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

RATE	ADDITIONAL FEE
x\$11=	
x41=	
+135=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
x\$22=	
x82=	
+270=	
TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

RATE	ADDITIONAL FEE
x\$11=	
x41=	
+135=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
x\$22=	
x82=	
+270=	
TOTAL ADDIT. FEE	

*** If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Table of Contents

1. US6130139A Method of manufacturing trench-isolated semiconductor device
-

Family 1/1

9 record(s) per family, collapsed by 7 record(s)

Record 1/7 JP10154751A SEMICONDUCTOR DEVICE

Publication Number: JP10154751A 19980609

Title: SEMICONDUCTOR DEVICE

Title - DWPI: Semiconductor device comprises semiconductor substrate with active region and isolation region, trench portions, semiconductor portions, interlayer insulating film, wire and PN junction

Priority Number: JP1996314762A

Priority Date: 1996-11-26

Application Number: JP1996314762A

Application Date: 1996-11-26

Publication Date: 1998-06-09

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L002176	H	H01	H01L	H01L0021	H01L002176
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L002978	H	H01	H01L	H01L0029	H01L002978

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L002102	H	H01	H01L	H01L0021	H01L002102
H01L002170	H	H01	H01L	H01L0021	H01L002170
H01L002352	H	H01	H01L	H01L0023	H01L002352
H01L002902	H	H01	H01L	H01L0029	H01L002902
H01L002966	H	H01	H01L	H01L0029	H01L002966
H01L00213205	H	H01	H01L	H01L0021	H01L00213205

H01L002176	H	H01	H01L	H01L0021	H01L002176
H01L0021762	H	H01	H01L	H01L0021	H01L0021762
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L002906	H	H01	H01L	H01L0029	H01L002906
H01L002978	H	H01	H01L	H01L0029	H01L002978

Assignee/Applicant: MATSUSHITA ELECTRIC IND CO LTD

JP F Terms: | 5F032AA34 | 5F032AA44 | 5F032BA01 | 5F032BA02 | 5F032BA03 | 5F032BB03 | 5F032BB04 | 5F032CA01 | 5F032CA03 | 5F032CA17 | 5F033BA02 | 5F033CA04 | 5F033DA07 | 5F033DA32 | 5F033EA25 | 5F033HH04 | 5F033HH05 | 5F033HH07 | 5F033HH26 | 5F033LL03 | 5F033MM05 | 5F033QQ58 | 5F033QQ63 | 5F033RR04 | 5F033RR06 | 5F033TT00 | 5F033TT02 | 5F033TT08 | 5F033VV01 | 5F033VV06 | 5F033VV09 | 5F033VV10 | 5F033XX24 | 5F040DA01 | 5F040DB01 | 5F040DC01 | 5F040EC07 | 5F040EK05 | 5F140AA00 | 5F140AA01 | 5F140AA15 | 5F140AB10 | 5F140BA01 | 5F140BF01 | 5F140BF04 | 5F140BF11 | 5F140BF18 | 5F140CA01 | 5F140CA03 | 5F140CA04 | 5F140CA06 | 5F140CB04 | 5F140CC01 | 5F140CC03 | 5F140CC08 | 5F140CE07 | 5F140CF00 | 5F140CF01

JP FI Codes: | H01L002176-N | H01L002190-V | H01L002978-301X

Assignee - Original: MATSUSHITA ELECTRIC IND CO LTD

Any CPC Table:

ECLA:

Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device of high operation speed, by reducing a wiring-substrate capacitance in an element isolation region, or reducing an accumulated electric charge amount in capacitance.

SOLUTION: On a P-type silicon substrate 1, an active region 6 where an element is provided, and an element isolation region 7 surrounding it are provided, and comprises a groove part 8 and a dummy semiconductor part 9. An inter-layer insulation film 12 is deposited on the substrate, with a wiring 13 over it. In the semiconductor part 9, an impurity diffusion layer 21 which is formed at the same time with ion-implantation into element is formed, while a PN joint part 22 formed between the impurity diffusion layer 21 and the silicon substrate 1. The capacitance component in the region passing the semiconductor part 9 among wiring-substrate capacitance is equal to addition, in series, of capacitance of impurity diffusion layer 21 to that of inter-layer insulation film 12, resulting in the amount less than the capacitance only with inter-layer insulation film, so that the

entire wiring-substrate capacitance is reduced and the semiconductor device & operate at higher speeds.

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PROBLEM TO BE SOLVED: To provide a semiconductor device of high operation speed, by reducing a wiring-substrate capacitance in an element isolation region, or reducing an accumulated electric charge amount in capacitance. **SOLUTION:** On a P-type silicon substrate 1, an active region 6 where an element is provided, and an element isolation region 7 surrounding it are provided, and comprises a groove part 8 and a dummy semiconductor part 9. An inter-layer insulation film 12 is deposited on the substrate, with a wiring 13 over it. In the semiconductor part 9, an impurity diffusion layer 21 which is formed at the same time with ion-implantation into element is formed, while a PN joint part 22 formed between the impurity diffusion layer 21 and the silicon substrate 1. The capacitance component in the region passing the semiconductor part 9 among wiring-substrate capacitance is equal to addition, in series, of capacitance of impurity diffusion layer 21 to that of inter-layer insulation film 12, resulting in the amount less than the capacitance only with inter-layer insulation film, so that the entire wiring-substrate capacitance is reduced and the semiconductor device & operate at higher speeds.

Language of Publication: JA

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2005-05-18	A02	-
Description: DECISION OF REFUSAL JAPANESE INTERMEDIATE CODE: A02 2005-05-17		

Post-Issuance (US):

Reassignment (US) Table:

Maintenance Status (US):

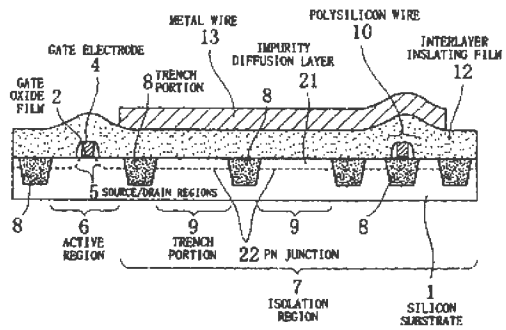
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



Publication Number: JP10223750A 19980821

Title: MANUFACTURE OF SEMICONDUCTOR DEVICE

Title - DWPI: Semiconductor device comprises semiconductor substrate with active region and isolation region, trench portions, semiconductor portions, interlayer insulating film, wire and PN junction

Priority Number: JP199723844A

Priority Date: 1997-02-06

Application Number: JP199723844A

Application Date: 1997-02-06

Publication Date: 1998-08-21

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L002176	H	H01	H01L	H01L0021	H01L002176
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L002978	H	H01	H01L	H01L0029	H01L002978

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L002102	H	H01	H01L	H01L0021	H01L002102
H01L002170	H	H01	H01L	H01L0021	H01L002170
H01L002352	H	H01	H01L	H01L0023	H01L002352
H01L002902	H	H01	H01L	H01L0029	H01L002902
H01L002966	H	H01	H01L	H01L0029	H01L002966
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L002176	H	H01	H01L	H01L0021	H01L002176
H01L0021762	H	H01	H01L	H01L0021	H01L0021762
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L002906	H	H01	H01L	H01L0029	H01L002906
H01L002978	H	H01	H01L	H01L0029	H01L002978

Assignee/Applicant: MATSUSHITA ELECTRIC IND CO LTD

JP F Terms: | 5F032AA34 | 5F032AA44 | 5F032AA48 | 5F032AA67 | 5F032AA70 | 5F032BA01 | 5F032BB03 | 5F032BB04 | 5F032CA17 | 5F032CA20 | 5F032DA14 | 5F032DA33 | 5F032DA43 | 5F032DA60 | 5F032DA78 | 5F033BA02 | 5F033EA25 | 5F033FA03 | 5F033HH07 | 5F033KK01 | 5F033LL04 | 5F033QQ48 | 5F033QQ58 | 5F033QQ63 | 5F033QQ65 | 5F033RR04 | 5F033VV01 | 5F033VV10 | 5F033VV15 | 5F033XX24 | 5F033XX27 | 5F040DA01 | 5F040DB01 | 5F040DB03 | 5F040DC01 | 5F040EC07 | 5F040EK05 | 5F040FA05 | 5F040FB04 | 5F140AA00 | 5F140AA01 | 5F140AA15 | 5F140AB09 | 5F140AB10 | 5F140BA01 | 5F140BF01 | 5F140BF04 | 5F140BG08 | 5F140BG09 | 5F140BG12 | 5F140BG14 | 5F140BK13 | 5F140CA03 | 5F140CB04 | 5F140CC01 | 5F140CC03 | 5F140CC08 | 5F140CE07

JP FI Codes: | H01L002176-N | H01L002190-V | H01L002978-301X

Assignee - Original: MATSUSHITA ELECTRIC IND CO LTD

Any CPC Table:

ECLA:

Abstract:

PROBLEM TO BE SOLVED: To obtain a semiconductor device in which a capacitance across an interconnection and a substrate inside an element isolation region is reduced by a method wherein a P-N junction part is formed in a dummy semiconductor part which does not function as an active region inside the element isolation region.

SOLUTION: A thin silicon oxide film 21 and a thin silicon nitride film 22 are formed sequentially on a P-type silicon substrate 1, and, in succession, a plurality of grooves 14a to 14c having a prescribed width are formed in the P-type silicon substrate 1. Then, dummy semiconductor parts 9 which are surrounded by the respective grooves 14a to 14c, which are used as one or more protruding parts and which do not function as an active region are formed inside element isolation regions 7. N-type impurity diffusion layers are formed inside the dummy semiconductor parts 9, and P-N junction parts 32 are formed between the N-type impurity diffused layers and the P-type silicon substrate 1. Thereby, it is possible to reduce a capacitance across an interaction and the substrate inside the element isolation regions 7, and the operating speed of a semiconductor device can be enhanced.

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Language of Publication: JA

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2004-03-03	A02	-
Description: DECISION OF REFUSAL JAPANESE INTERMEDIATE CODE: A02 2004-03-02		
2004-01-07	A521	-
Description: WRITTEN AMENDMENT JAPANESE INTERMEDIATE CODE: A523 2004-01-06		
2003-11-26	A131	-
Description: NOTIFICATION OF REASONS FOR REFUSAL JAPANESE INTERMEDIATE CODE: A131 2003-11-25		

Post-Issuance (US):

Reassignment (US) Table:

Maintenance Status (US):

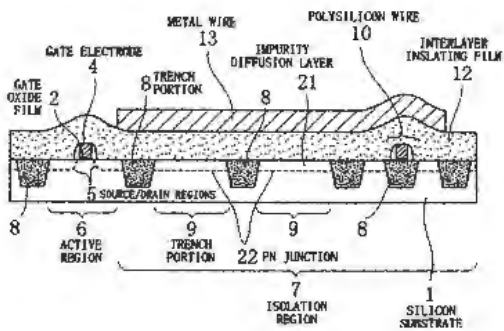
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



Record 3/7 US6130139A Method of manufacturing trench-isolated semiconductor device

Publication Number: US6130139A 20001010

Title: Method of manufacturing trench-isolated semiconductor device

Title - DWPI: Semiconductor device comprises semiconductor substrate with active region and isolation region, trench portions, semiconductor portions, interlayer insulating film, wire and PN junction

Priority Number: JP1996314762A | JP199723844A

Priority Date: 1996-11-26 | 1997-02-06

Application Number: US1997978137A

Application Date: 1997-11-25

Publication Date: 2000-10-10

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L0021762	H	H01	H01L	H01L0021	H01L0021762
H01L0023522	H	H01	H01L	H01L0023	H01L0023522

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L002102	H	H01	H01L	H01L0021	H01L002102
H01L002170	H	H01	H01L	H01L0021	H01L002170
H01L002352	H	H01	H01L	H01L0023	H01L002352
H01L002902	H	H01	H01L	H01L0029	H01L002902
H01L002966	H	H01	H01L	H01L0029	H01L002966
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L002176	H	H01	H01L	H01L0021	H01L002176
H01L0021762	H	H01	H01L	H01L0021	H01L0021762
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L002906	H	H01	H01L	H01L0029	H01L002906
H01L002978	H	H01	H01L	H01L0029	H01L002978

Assignee/Applicant: Matsushita Electric Industrial Co. Ltd.,Osaka,JP

JP F Terms:

JP FI Codes:**Assignee - Original:** Matsushita Electric Industrial Co. Ltd.**Any CPC Table:**

Type	Invention	Additional	Version	Office
Current	H01L 23/5222	-	20130101	EP
Current	H01L 21/76232		20130101	EP

ECLA: H01L0021762C6 | H01L0023522C**Abstract:**

The top surface of a P-type semiconductor substrate is partitioned into an active region to be formed with an element and an isolation region surrounding the active region. The isolation region is composed of trench portions and dummy semiconductor portions. An interlayer insulating film is deposited on the substrate, followed by a wire formed thereon. In each of the semiconductor portions, an impurity diffusion layer is formed simultaneously with the implantation of ions into the element so that a PN junction is formed between the impurity diffusion layer and the silicon substrate. A capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions is obtained by adding in series the capacitance in the impurity diffusion layer to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the inter layer insulating film. What results is a semiconductor device having lower total wiring to-substrate capacitance and a higher operating speed.

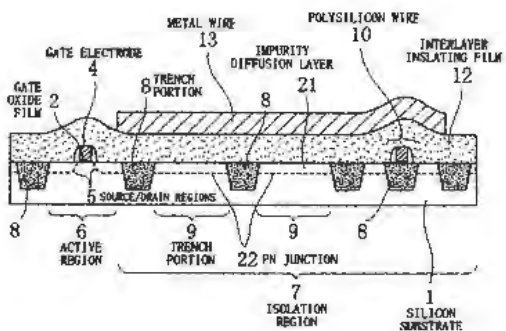
Language of Publication: EN**INPADOC Legal Status Table:**

Gazette Date	Code	INPADOC Legal Status Impact
2014-02-03	AS	-
Description: ASSIGNMENT GODO KAISHA IP BRIDGE 1, JAPAN ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR:PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.); REEL/FRAME:032152/0514 2014-01-17		
2012-03-20	FPAY	+
Description: FEE PAYMENT		
2008-03-13	FPAY	+
Description: FEE PAYMENT		
2004-03-10	FPAY	+
Description: FEE PAYMENT		
1997-11-25	AS	-
Description: ASSIGNMENT MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., JAPAN ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNORS:UKEDA, TAKAAKI; KUDO, CHIAKI; YABU, TOSHIKI; REEL/FRAME:008899/0411 1997-11-18		

Post-Issuance (US):
Reassignment (US) Table:

Assignee	Assignor	Date Signed	Reel/Frame	Date
GODO KAISHA IP BRIDGE 1,TOKYO,JP	PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.)	2014-01-17	032152/0514	2014-02-03
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVE. NW SUITE 800 WASHINGTON, DC 20037-3213				
MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD.,OSAKA 571,JP	UKEDA, TAKAAKI	1997-11-18	008899/0411	1997-11-25
	KUDO, CHIAKI	1997-11-18		
	YABU, TOSHIKI	1997-11-18		
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: MCDERMOTT, WILL & EMERY EDWARD E. KUBASIEWICZ, ESQ. 600 13TH STREET, N.W. WASHINGTON, D.C. 20005-3096				

Maintenance Status (US):
Litigation (US):
Opposition (EP):
License (EP):
EPO Procedural Status:
Front Page Drawing:



Record 4/7 US6346736B1 Trench isolated semiconductor device

Publication Number: US6346736B1 20020212

Title: Trench isolated semiconductor device

Title - DWPI: Semiconductor device comprises semiconductor substrate with active region and isolation region, trench portions, semiconductor portions, interlayer insulating film, wire and PN junction

Priority Number: JP1996314762A | JP199723844A | US1997978137A

Priority Date: 1996-11-26 | 1997-02-06 | 1997-11-25

Application Number: US1999469498A

Application Date: 1999-12-22

Publication Date: 2002-02-12

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L0021762	H	H01	H01L	H01L0021	H01L0021762
H01L0023522	H	H01	H01L	H01L0023	H01L0023522

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L002102	H	H01	H01L	H01L0021	H01L002102
H01L002170	H	H01	H01L	H01L0021	H01L002170
H01L002352	H	H01	H01L	H01L0023	H01L002352
H01L002902	H	H01	H01L	H01L0029	H01L002902
H01L002966	H	H01	H01L	H01L0029	H01L002966
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L002176	H	H01	H01L	H01L0021	H01L002176
H01L0021762	H	H01	H01L	H01L0021	H01L0021762
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L002906	H	H01	H01L	H01L0029	H01L002906
H01L002978	H	H01	H01L	H01L0029	H01L002978

Assignee/Applicant: Matsushita Electric Industrial Co. Ltd., Osaka, JP

JP F Terms:

JP FI Codes:**Assignee - Original:** Matsushita Electric Industrial Co. Ltd.**Any CPC Table:**

Type	Invention	Additional	Version	Office
Current	H01L 23/5222	-	20130101	EP
Current	H01L 21/76232		20130101	EP

ECLA: H01L0021762C6 | H01L0023522C**Abstract:**

The top surface of a P-type semiconductor substrate is partitioned into an active region to be formed with an element and an isolation region surrounding the active region. The isolation region is composed of trench portions and dummy semiconductor portions. An interlayer insulating film is deposited on the substrate, followed by a wire formed thereon. In each of the semiconductor portions, an impurity diffusion layer is formed simultaneously with the implantation of ions into the element so that a PN junction is formed between the impurity diffusion layer and the silicon substrate. A capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions is obtained by adding in series the capacitance in the impurity diffusion layer to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. What results is a semiconductor device having lower total wiring-to-substrate capacitance and a higher operating speed.

Language of Publication: EN**INPADOC Legal Status Table:**

Gazette Date	Code	INPADOC Legal Status Impact
2014-02-03	AS	-
Description: ASSIGNMENT GODO KAISHA IP BRIDGE 1, JAPAN ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR:PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.); REEL/FRAME:032152/0514 2014-01-17		
2013-03-13	FPAY	+
Description: FEE PAYMENT		
2009-07-15	FPAY	+
Description: FEE PAYMENT		
2005-07-20	FPAY	+
Description: FEE PAYMENT		

Post-Issuance (US):**Reassignment (US) Table:**

Assignee	Assignor	Date Signed	Reel/Frame	Date
GODO KAISHA IP BRIDGE 1,TOKYO,JP	PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.)	2014-01-17	032152/0514	2014-02-03
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVE. NW SUITE 800 WASHINGTON, DC 20037-3213				

Maintenance Status (US):

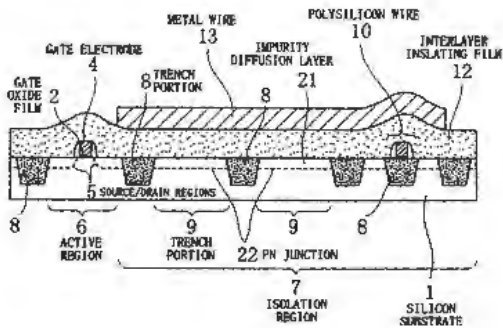
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



Publication Number: KR403012B1 20040205

Title:

Title - DWPI:

Priority Number: JP1996314762A | JP199723844A

Priority Date: 1996-11-26 | 1997-02-06

Application Number: KR199763007A

Application Date: 1997-11-26

Publication Date: 2004-02-05

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L002176	H	H01	H01L	H01L0021	H01L002176
H01L0021762	H	H01	H01L	H01L0021	H01L0021762
H01L0023522	H	H01	H01L	H01L0023	H01L0023522

IPC Class Table - DWPI:

Assignee/Applicant:

JP F Terms:

JP FI Codes:

Assignee - Original:

Any CPC Table:

Type	Invention	Additional	Version	Office
Current	H01L 23/5222	-	20130101	EP
Current	H01L 21/76232		20130101	EP

ECLA:

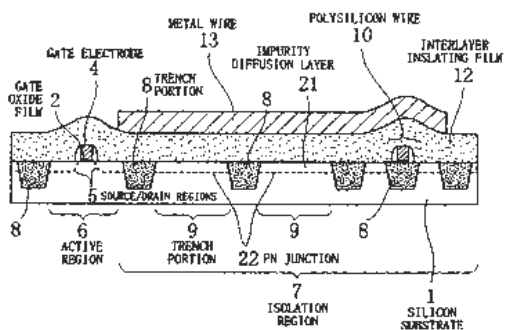
Abstract:

The top surface of a P-type semiconductor substrate is partitioned into an active region to be formed with an element and an isolation region surrounding the active region. The isolation region is composed of trench portions and dummy semiconductor portions. An interlayer insulating film is deposited on the substrate, followed by a wire formed thereon. In each of the semiconductor portions, an impurity diffusion layer is formed simultaneously with the implantation of ions into the element so that a PN junction is formed between the impurity diffusion layer and the silicon substrate. A capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions is obtained by adding in series the capacitance in the impurity diffusion layer to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. What results is a semiconductor device having lower total wiring-to-substrate capacitance and a higher operating speed. <IMAGE>

Language of Publication: KO

INPADOC Legal Status Table:

Front Page Drawing:



Record 6/7 EP844660B1 Semiconductor device and method of manufacturing the same | Halbleitervorrichtung und deren Herstellungsverfahren | Dispositif semi-conducteur et son procédé de fabrication

Publication Number: EP844660B1 20070815
EP844660A1 19980527

Title: Semiconductor device and method of manufacturing the same | Halbleitervorrichtung und deren Herstellungsverfahren | Dispositif semi-conducteur et son procédé de fabrication

Title - DWPI: Semiconductor device comprises semiconductor substrate with active region and isolation region, trench portions, semiconductor portions, interlayer insulating film, wire and PN junction

Priority Number: JP1996314762A | JP199723844A

Priority Date: 1996-11-26 | 1997-02-06

Application Number: EP1997120656A

Application Date: 1997-11-25

Publication Date: 2007-08-15

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L0021762	H	H01	H01L	H01L0021	H01L0021762
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L002906	H	H01	H01L	H01L0029	H01L002906

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L002102	H	H01	H01L	H01L0021	H01L002102
H01L002170	H	H01	H01L	H01L0021	H01L002170
H01L002352	H	H01	H01L	H01L0023	H01L002352
H01L002902	H	H01	H01L	H01L0029	H01L002902
H01L002966	H	H01	H01L	H01L0029	H01L002966
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L002176	H	H01	H01L	H01L0021	H01L002176
H01L0021762	H	H01	H01L	H01L0021	H01L0021762
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522

H01L002906	H	H01	H01L	H01L0029	H01L002906
H01L002978	H	H01	H01L	H01L0029	H01L002978

Assignee/Applicant: MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD.,Kadoma-shi, Osaka 571-0050,JP,00216885

JP F Terms:

JP FI Codes:

Assignee - Original: MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD.

Any CPC Table:

Type	Invention	Additional	Version	Office
Current	H01L 23/5222	-	20130101	EP
Current	H01L 21/76232		20130101	EP

ECLA: H01L0021762C6 | H01L0023522C

Abstract:

The top surface of a P-type semiconductor substrate is partitioned into an active region to be formed with an element and an isolation region surrounding the active region. The isolation region is composed of trench portions and dummy semiconductor portions. An interlayer insulating film is deposited on the substrate, followed by a wire formed thereon. In each of the semiconductor portions, an impurity diffusion layer is formed simultaneously with the implantation of ions into the element so that a PN junction is formed between the impurity diffusion layer and the silicon substrate. A capacitance component of the wiring-to-substrate capacitance in the region containing the semiconductor portions is obtained by adding in series the capacitance in the impurity diffusion layer to the capacitance in the interlayer insulating film, which is smaller than the capacitance only in the interlayer insulating film. What results is a semiconductor device having lower total wiring-to-substrate capacitance and a higher operating speed.

Language of Publication: EN

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2014-02-28	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2014-01-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		
2014-01-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE DE		
2014-01-31	PGFP	+

Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE FR		
2013-03-29	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2013-02-28	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		
2013-01-31	PGFP	+
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Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
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2008-01-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2007-12-28	ET	+

Description: FR: TRANSLATION FILED		
2007-09-27	REF	-
Description: CORRESPONDS TO: DE 69738012 P		
2007-08-15	REG	-
Description: REFERENCE TO A NATIONAL CODE GB FG4D EUROPEAN PATENT GRANTED		
2007-08-15	AK	+
Description: DESIGNATED CONTRACTING STATES: EP 0844660 B1 DE; FR; GB; NL		
2004-07-28	17Q	+
Description: FIRST EXAMINATION REPORT 2004-06-15		
1999-02-10	RBV	+
Description: DESIGNATED CONTRACTING STATES (CORRECTION): DE; FR; GB; NL		
1999-02-10	AKX	+
Description: PAYMENT OF DESIGNATION FEES DE FR GB NL		
1998-10-14	17P	+
Description: REQUEST FOR EXAMINATION FILED 1998-08-14		
1998-05-27	AX	+
Description: EXTENSION OR VALIDATION OF THE EUROPEAN PATENT TO AL; LT; LV; MK; RO; SI		
1998-05-27	AK	+
Description: DESIGNATED CONTRACTING STATES: EP 0844660 A1 DE; FR; GB; NL		

Post-Issuance (US):

Reassignment (US) Table:

Maintenance Status (US):

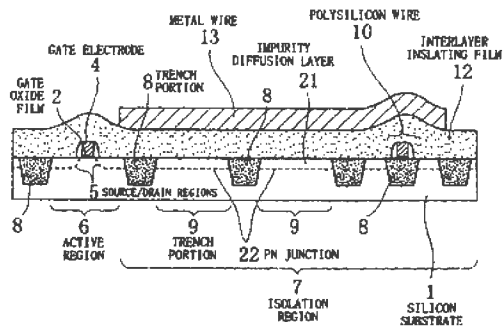
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status: EX-REPORT 2004-06-15 2004 Dispatch of 1st examination report | EX-RQ 1998-08-14 1998 Request for examination

Front Page Drawing:



Record 7/7 DE69738012T2 Halbleitervorrichtung und deren Herstellungsverfahren

Publication Number: DE69738012T2 20071213
DE69738012D1 20070927

Title: Halbleitervorrichtung und deren Herstellungsverfahren

Title - DWPI: Semiconductor device comprises semiconductor substrate with active region and isolation region, trench portions, semiconductor portions, interlayer insulating film, wire and PN junction

Priority Number: JP1996314762A | JP199723844A

Priority Date: 1996-11-26 | 1997-02-06

Application Number: DE69738012A

Application Date: 1997-11-25

Publication Date: 2007-12-13

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L0021762	H	H01	H01L	H01L0021	H01L0021762
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L002906	H	H01	H01L	H01L0029	H01L002906

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L002102	H	H01	H01L	H01L0021	H01L002102
H01L002170	H	H01	H01L	H01L0021	H01L002170
H01L002352	H	H01	H01L	H01L0023	H01L002352
H01L002902	H	H01	H01L	H01L0029	H01L002902
H01L002966	H	H01	H01L	H01L0029	H01L002966
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L002176	H	H01	H01L	H01L0021	H01L002176
H01L0021762	H	H01	H01L	H01L0021	H01L0021762
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L002906	H	H01	H01L	H01L0029	H01L002906

H01L002978	H	H01	H01L	H01L0029	H01L002978
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Assignee/Applicant: Matsushita Electric Industrial Co. Ltd.,JP

JP F Terms:

JP FI Codes:

Assignee - Original: Matsushita Electric Industrial Co. Ltd.

Any CPC Table:

Type	Invention	Additional	Version	Office
Current	H01L 23/5222	-	20130101	EP
Current	H01L 21/76232		20130101	EP

ECLA: H01L0021762C6 | H01L0023522C

Abstract:

Language of Publication: DE

INPADOC Legal Status Table:

Post-Issuance (US):

Reassignment (US) Table:

Maintenance Status (US):

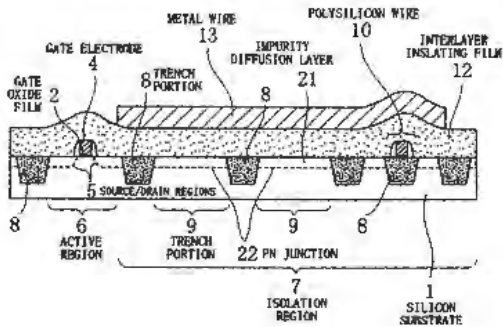
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



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USPTO Maintenance Report					
Patent Bibliographic Data				08/29/2014 02:49 AM	
Patent Number:	6130139		Application Number:	08978137	
Issue Date:	10/10/2000		Filing Date:	11/25/1997	
Title:	METHOD OF MANUFACTURING TRENCH-ISOLATED SEMICONDUCTOR DEVICE				
Status:	4th, 8th and 12th year fees paid			Entity:	LARGE
Window Opens:	N/A	Surcharge Date:	N/A	Expiration:	N/A
Fee Amt Due:	Window not open	Surchg Amt Due:	Window not open	Total Amt Due:	Window not open
Fee Code:					
Surcharge Fee Code:					
Most recent events (up to 7):	03/20/2012 02/07/2012 02/07/2012 03/13/2008 03/10/2004 09/12/2001	Payment of Maintenance Fee, 12th Year, Large Entity. Payor Number Assigned. Payer Number De-assigned. Payment of Maintenance Fee, 8th Year, Large Entity. Payment of Maintenance Fee, 4th Year, Large Entity. Payor Number Assigned. --- End of Maintenance History ---			
Address for fee purposes:	PANASONIC PATENT CENTER 20000 Mariner Avenue, Suite 200 Torrance CA 90503				