UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

GODO KAISHA IP BRIDGE 1,

Plaintiff,

-against-

Case No. 2:17-cv-00676-RWS-RSP

INTEL CORPORATION,

Defendant.

June 8, 2018
9:36 a.m.

Deposition of DR. JOHN BRAVMAN, taken by Plaintiff, pursuant to Notice, held at the offices of Kirkland & Ellis LLP, 601 Lexington Avenue, New York, New York, before Joseph R. Danyo, a Shorthand Reporter and Notary Public within and for the State of New York.

Job No. 143156

A P P E A R A N C E S :

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By: JON CARTER, ESQ.

Also Present:
LAURA ZHU

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Dr. J O H N B R A V M A N, having been first duly sworn by Joseph R. Danyo, a Notary Public, was examined and testified as follows:

EXAMINATION BY MR. MIDDLETON:

Q. Good morning, Dr. Bravman.

A. Good morning.

Q. I am handing you Exhibit 1. Exhibit 1 is a piece of paper with Intel's construction for the term "dielectric film" in this case?

A. That's correct.

(Bravman Exhibit 1, Piece of paper with Intel's construction for term "dielectric film", was so marked for identification, as of this date.)

Q. Okay, and Intel's proposed construction requires that the dielectric film reduce capacitance between the wire and the substrate. Is that right?

A. That is what the words say, yes.

Q. You agree with that construction?

A. Yes.

Q. Under this construction, what is the structure that it is being compared with in order to determine whether the capacitance between the

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wire and the substrate has been reduced?

A. The structure that would otherwise be there as laid out in the prior elements of the claim.

Q. So are you saying, for example, that the layers without the same thickness in the other structure?

A. Could I look at the patent? Can I have a copy of the patent?

Q. You want to look at the claim?

A. Can I just look at the patent?

Q. You cannot answer that without looking at the patent?

A. I prefer to just have the patent in front of me.

Q. Well, I will give you --

MR. MIDDLETON: Let's mark this as Exhibit 2.

(Bravman Exhibit 2, Text of claim 6, was so marked for identification, as of this date.)

MR. CARTER: I will note for the record that Exhibit 2 is, it just appears to be the text of claim 6, but it is not

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the complete patent or any other part of the patent.

MR. MIDDLETON: I think that is a fair characterization of Exhibit 2.

Q. So, Dr. Bravman, do you recognize Exhibit 2 to be claim 6 of the '736 patent?

A. Yes, it appears to be that.

Q. Okay. So when you determined whether a device has a dielectric film of claim 6, the structure that it is being compared, would all the layers have the same thicknesses in that structure and just exclude the dielectric film?

A. The thicknesses of the layers here along with many other characteristics of the layers and the structures are not specifically laid out here, and of course I read this claim and all the claims and all the claim elements in light of the teaching to a person of ordinary skill of the whole patent, and so that is why I asked for a copy of the patent, but these claims here by themselves are of course silent on a very large number of issues.

Q. Okay, so just looking at the claim, though, itself, if you were to determine whether

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the device has the dielectric film, are you saying that all these other layers that are in claim 6 besides the dielectric film, they would be the same in the device you are comparing it to?

MR. CARTER: Objection to form.

A. Again, as I said before, in this claim there are many things that are unspecified including thicknesses that you posit.

Q. So if you were to look at a device, how would you determine whether it has the dielectric film of claim 6 based on the claim language?

A. Well, I would look at things, assuming I could look at things, such as process flows and device -- teardown analyses, stuff I did for a long time, and then that would be, that would allow me to know what layers are present, presumably, if I had the right information presented to me, but again interpreting whether the claim elements or the claim as a whole were met would involve looking at the claim in the context of the entire patent and then making my best-faith determination about a given set of

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structures whether or not they were within the elements of the claim in light of the patent language.

Q. So you would need to look at the patent to determine whether a claim limitation is met, is that right?

A. Well, because the claim limitations are expressed in words and words have meanings, I understand that starting with the intrinsic record of the entire patent and even the patent's prosecution history is important for understanding what the claim and claim elements mean, and so I would have to have a fair -- I would have to convince myself I understood what a claim and its elements meant and then take that understanding and apply it to a situation, a structure, a device, assuming I had enough information to compare the two.

Q. All right. I want you to assume that all of the elements except for the dielectric film are given a plain and ordinary meaning and that the term "dielectric film" is given the construction provided by Intel.

With that as background, would you

need to look at the patent to determine whether a claim limitation is met in a product?

A. I'm not sure that I fully understand the implications of your question, but the patents I think there is commonality of understanding. The patent is aimed at improving the performance of a chip, for increasing the speed, increasing the rate of charge and discharge. Those are all expressions of the same thing. And in service of that overall purpose or teaching of the patent, the patent goes on to explain that there are certain ways of doing that within the scope of this patent, and it is within that context that this claim is written and therefore properly understood as teaching a reader what the patent actually teaches the reader as a whole.

Q. So is that a no? I'm sorry.

A. So please repeat your question. I will answer it if I can.

Q. I want you to assume that all of the elements in claim 6 except for the dielectric film are given their plain and ordinary meaning and the term "dielectric film" is given the

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construction provided by Intel.

With that as background, would you have to look at the patent in order to determine whether a claim limitation is met in a product?

A. Yes. I would never want to say what a claim element means without understanding the context with which it -- in which it is embedded, i.e., the patent as a whole.

Q. And claim 6 itself doesn't give sufficient context?

A. There is a lot of information in claim 6, and there is a lot more that is not included, and so one needs to understand what claim 6 actually is saying, and my understanding is that I am to do that as a person of ordinary skill would in the time frame of the patent in light of what the specification, the claims themselves and the file history suggests and at times also bringing in, if I thought I needed to, you know, other extrinsic evidence.

Q. So claim 6 itself doesn't give sufficient context? Yes or no?

MR. CARTER: Objection to form.

A. Again, I think I have answered the

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question. My understanding is I am supposed to read meaning and context in light of the patent so I understand what has actually been claimed.

Q. So that is a no?

MR. CARTER: Same objection.

A. Yeah. I don't think it is a yes or no question. I have given my answer. I have said -- you said, I believe you asked me is the context sufficient, and I am saying that I have to interpret any claim in light of the entire patent, and if I am understanding you correctly, I guess then the answer is you could characterize the answer as no, because reading this in the abstract devoid of all other information, that is not what I understand my job is in interpreting a patent claim.

Q. Well, I want you to assume that the claim has already been interpreted to use Intel's construction for dielectric film and that the court has instructed you to use plain and ordinary meaning for all other terms in this claim. Do you follow that?

A. Yes.

Q. Okay. Under those assumptions, what

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structure would you need to look at to determine whether -- I will withdraw that.

Under those assumptions, when looking at whether a structure has the claimed dielectric film, what would you compare that structure to?

A. I would want to know what the thing such as the reason why a dielectric film, and this is why I agree with the construction, was put in place as it was, assuming that it is there, and to see if that comports with the claim in light of the patent.

Dielectric films have many purposes. They are well known. I am sure we agree that the patentee is not claiming to have discovered their uses, and so, in the context of this patent, it is very clear about why this dielectric film is in place, and to understand what the patentee has a right to, I would want to understand the language, and I believe the asserted claim construction helps the reader to do that, but I'm not a lawyer, but I don't think that inserting a claim construction allows one then to take the claim and sort of forget about the rest of the patent. It just helps one and clarifies what some of the words mean.

Q. So in order to understand whether a product has a dielectric film that satisfies Intel's construction, you would need to know why that dielectric film was included in the structure?

A. Well, knowing whether or not something physically exists is a different question, and dielectric film, as I just said, exists and are used for a number of reasons, so there is ways to discern whether or not given materials or structures of course are present, but whether or not it is -- it comports with the teaching of a claim or its elements, again, my understanding is one does that looking carefully at the claims in light of what the patent says overall.

Q. So in order to understand whether a product has a dielectric film that satisfies Intel's constructions, would you need to know why that dielectric film was included in the structure?

A. Because dielectrics, that is what we are talking about, have many purposes in light of

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understanding this patent, yes. The answer would be yes.

Q. Now the construction for resistor film proposed by Intel is the same as the construction for dielectric film except that the word "dielectric film" is replaced with "resistor film." Is that right?

A. That is my recollection. Yes.

Q. And would your answers that you just gave for dielectric film as to how you would figure out whether a product has dielectric film, would those same answers apply to resistor film?

A. Well, my answers with regard to how I interpret a claim and a structure, et cetera, I would hope I would be consistent with that whenever I am reading a claim and looking at a structure, yes, so yes, if I understand your question correctly.

Q. So do you agree that the capacitance of a capacitor is constant, because the capacitance is a material property of the dielectric material?

MR. CARTER: Objection to form.

A. Capacitance of a material is a fairly

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imprecisely used phrase. We know materials have properties. They have relative dielectric constants, which is multiplied by the permittivity of free space to give you the dielectric constant of a material. The capacitance is usually that phrase, what is the capacitance is usually the capacitance of a structure with geometry such as distance between plates and things such as that.

A worker of skill may often be able to interpret what an author meant, but materials have inherent properties that go into, of course, helping to determine what the capacitance of a structure using those materials would possess.

Q. What is your understanding of the term "capacitance" as it is used in this context of the '736 patent?

A. Well, I think the word appears in many places, so it clearly is generally and generically referring to the ability to store energy or charge, a well-known feature of a structure.

Q. So with that understanding of capacitance from the '736 patent, do you agree

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that the capacitance of a capacitor with a given geometry is constant, because the capacitance is a material property of the dielectric material?

A. The capacitance of a capacitor, now you are talking about a specific device with specific materials and geometries, that is generally, yeah, a correct statement.

(Bravman Exhibit 3, '736 patent, was so marked for identification, as of this date.)

Q. You have been handed Bravman Exhibit 3, which is a copy of the '736 patent.

A. Yes.

Q. Can you go to the last set of figures.

A. Um-hum.

Q. Sheet 21 of 21.

A. I have it.

Q. Okay. Actually, I'm sorry. Figure 19. My apologies.

A. Okay.

MR. CARTER: Just to clarify, we are on sheet 19 of 21?

MR. MIDDLETON: And also figure 19.

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Yes.

MR. CARTER: Thank you.

Q. Do you agree that looking at figure 19, that adding a dielectric film to the structure in figure 19 of the '736 patent would have increased the costs and complexity of fabricating a semiconductor device in comparison to the prior art device, because it would involve multiple additional steps relating to deposition, patterning and/or etching?

A. It could, yes, depending on where the film was and what the other process flows were, yes.

Q. It could or it will?

A. The costs in terms of upfront costs would have to be considered, but there is also costs of reliability, of additional metrology, the whole lifecycle costs, so as a general principle, I would say, as you make a circuit more complicated, there is a good chance that costs of one type or another could be incurred.

The industry is famous for not doing anything unless there is a specific purpose for doing it, and there is a number of reasons for

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that, and one of them can be lifecycle costs.

Q. And would your answer be the same about if the question was relating to adding a resistor film to that structure?

A. Yes. Again, it would be the same based on the same general statements that the industry doesn't do things unless it has to, and one of the reasons it has that concern is lifecycle costs.

Q. At the time of the filing of the '736 patent, the semiconductor industry had a well-established culture of not adding or subtracting process steps without a known direct benefit. Is that right?

A. That is certainly a general principle that I believe the industry adhered to long before the patent was written.

Q. Now previously, not in this case, but in connection with Intel, you provided opinions in support of interparty's review petitions against the '736 patent, is that right?

A. Yes. They have been filed is my understanding.

Q. You provided two declarations in

connection with those IPR petitions, is that right?

A. I think that is correct. Yes.

Q. And one of the IPRs, sorry, let me withdraw that. One of your declarations in connection with those IPRs addressed claims 6 and 13 of the '736 patent, right?

A. Well, I would presume that it did, because I know those are at issue. I have not reviewed those in many months. I think I finished my work on those at the end of last year, but I know those claims are in dispute. So I would assume that I did.

Q. You have previously provided expert reports in other cases?

A. Yes.

Q. And you also provided testimony in other cases?

A. Yes.

Q. Has a judge ever rejected your opinions?

A. Not to my recollection, but that is just a recollection. If you are asking me do I recall on a stand or via writing, I suppose, that

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a judge said, no, you are wrong, I don't have a recollection of that.

Q. Do you have a recollection of a judge ever criticizing your opinions?

A. No. I have seen a live attorney argument during a cross-exam or a direct where the judge has often made a ruling about what I am to use as an understanding and whether or not in every instance that was consistent with or somewhat different from what, the basis on which I was arguing, again, I don't have a specific memory either way, but that is certainly possible.

Q. Do you recall a judge ever saying that your testimony was inconsistent with an understanding you were supposed to use?

A. Again, I don't have a recollection of that, but I don't think I would have specific recollection of anything a judge said to me in a case.

Q. Has a judge ever adopted an opposing expert's opinions over your opinions?

A. In humility, I would have to say probably. I mean, again, I don't recall that

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specifically, but I'm not going to claim I bat a thousand.

Q. But you are not aware of any specific instances?

A. As I sit here, no, I can't recall.

(Bravman Exhibit 4, Declaration, was so marked for identification, as of this date.)

Q. You have been handed Exhibit 4. Is this a copy of the declaration you submitted in this case?

A. Yes.

Q. Can you turn to paragraph 10 of your declaration.

A. Okay. I have it.

Q. So in forming your opinions on claim construction, among other things you considered the '736 patent?

A. Yes.

Q. You also considered the prosecution history of the '736 patent?

A. Yes.

Q. You also considered the parties' proposed claim constructions for certain terms in

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the patents?

A. Yes.

Q. Then you also mention any other materials cited or referred to in this declaration?

A. Yes.

Q. Did you consider the parties' infringement or invalidity contentions?

A. No.

Q. Have you seen the parties' infringement or invalidity contentions?

A. Maybe I did for the IPR, I can't recall, but not in preparation for today's proceedings. I have no recollection of that. I certainly didn't review anything for today, but maybe I did for the IPRs that you mentioned.

Q. When did you form the opinions that are included in your declaration?

A. Oh, I can't remember the date when this was submitted, but --

Q. Well, sorry to cut you off, but let's go to the last page. That is your signature on May 23rd?

A. Yes. So very recently I signed a

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final version of this document. I suppose I worked on it over the previous month or so.

Q. Prior to commencing work on this declaration, did you have an opinion as to what the proper claim constructions of the terms "dielectric film" and "resistor film" were?

A. In light of this patent, again, I obviously read it carefully in preparation for the IPR, so again, not having reviewed those documents recently, but if I did, it would be expressed most likely in that document. Documents.

Q. When you say in that document, are you referring to the IPR declaration?

A. Yes.

Q. And if there is no discussion of claim construction in your declaration -- well, I will withdraw that.

Now, generally speaking, outside the context of the '736 patent, would the term "dielectric film" be a term that could be understood without clarification?

A. Certainly as a general proposition a worker of skill would understand the phrase

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"dielectric film" to refer to a material in a film-like configuration that had certain electronic properties.

Q. What electronic properties?

A. Well, a dielectric film is an insulator, but when you say dielectric as opposed to insulator, you are referring to the property of the material that allows it to sustain a polarization, and that is what makes it useful in capacitor-type devices.

Q. Just to clarify, is a dielectric film an insulating film?

A. Yes, in that it is a very poor conductor and usually only conducts upon a breakdown phenomenon.

Q. Can you go to paragraph 32 of your declaration.

A. Okay.

Q. In paragraph 32 there is an equation in the middle of the paragraph. Do you see that?

A. Yes.

Q. Just to clarify, the epsilon naught is a permittivity of free space, correct?

A. Yes.

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Q. Is that a constant?

A. Yes, it is an assumed constant in physics in the natural world.

Q. And I don't see you defining A there, but is A the area of the plates of the capacitor?

A. Yes. I apologize for that oversight. D, as it says, is the distance between the plates.

Q. So the capacitance is a function of the distance between the plates, the dielectric constant of the dielectric between the plates and the area of the plates. Is that right?

A. Yes, for the configuration of a capacitor, a device, as described in paragraph 32, this is the standard textbook formula that engineers and physicists and others learn. It assumes things such as very large plates compared to the separation between them and what have you, because that essentially renders immaterial edge effects, but this is certainly the standard formula for a parallel plate capacitor.

Q. In the context of the '736 patent, is this the proper equation to consider for capacitance?

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A. Well, the question would be the capacitance of what, because there is, as we know, capacitance built in deliberately into structures such as capacitors in integrated circuits, and then there is a whole range of unwanted or parasitic capacitances, and the calculation of the actual capacitance between say a wire and a substrate is much more complicated than this formula allows. It is a three-dimensional phenomena.

A wire running over the surface of an integrated circuit has parasitic effects with many structures underneath it, and so there is no way you can just simply apply area and distance and those kinds of things, but this is the start of any such simulation or calculation. It depends on materials and geometries.

Q. Can you look at figure 19 of the '736 patent.

A. Yes.

Q. Consider the region. Do you see -- well, let me back up. There are two areas labeled 9.

A. Yes.

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Q. In figure 19. Consider the leftmost portion of the left figure 9 to the rightmost portion of the right -- let me withdraw that. Consider the leftmost portion of the element, leftmost area labeled 9 to the rightmost portion of the area labeled -- the rightmost area labeled 9.

A. We are not on video here, but if you want to just annotate just so I know, that I see what you are saying.

Q. Yeah. Maybe I'll annotate this.

A. I just want to understand your question. Okay.

Q. Okay. So on figure 9 of Exhibit 1, I have added two red marking points.

A. Yes.

Q. Okay. So consider the region between those two red marks.

A. I understand.

Q. Okay. Can you use the equation in paragraph 32 of your report or declaration to determine the capacitance of that region?

A. No, because this is a two-dimensional slice through a three-dimensional object, and

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there is no way to know what the area is. That would require knowledge of the geometry in and out of the page.

Q. Okay. Assume that the area where there is 13 and the leftmost section 9, assume that that is area A1 with overlap. Does that make sense? The wire 13 comes in and out of the page, correct?

A. Right. It has some finite width in and out of the page.

Q. And the left number 9 in figure 19, it has some area as well, correct?

A. Certainly.

Q. And if you go vertically from 9 to 13, there is some overlapping area between 9 and 13?

A. Yes.

Q. Okay. Assume that that is A1. The area is A1.

A. Sorry. I'm not understanding your question, because the area is still -- you asked me could I calculate the capacitance.

Q. No. I just want you to -- do you understand that assumption? Just focusing in on

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that region over 9.

A. Focusing on the region --

Q. On the left 9.

A. Within the two red marks?

Q. No. The region over the 9. The left 9.

A. This one right here?

Q. Yes.

A. Okay. The region straight up 9. We don't know the in and out of the page dimensions. We don't know if the structures 13, 12 and 9 are the same extent in and out of the page. I mean 9 is a piece of the whole substrate, so it is infinite in size effectively compared to micron scale structures. And then the dielectric 12 and the wire conductor 13, I don't know what their vertical extent in and out of the drawing of the page is.

Other than that, I do understand you are asking me to draw in my mind a vertical line like a football goalpost up over the leftmost region 9, and presumably in this drawing all structures shown in fact are in this plane.

Q. You say in this plane. You mean the

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plane left and right on the page?

A. That are up and down left and right of the page. Yes.

Q. Now, when you consider also coming in and out of the page, the left, the region on the left labeled 9 and the wire 13, there is going to be an overlapping area, correct?

A. Well, this diagram, since I have made the assumption that all these structures are at least in this page, a plane of the page, there is some area that overlaps, yes.

Q. Okay. I want you to assume that where there is overlap, the dielectric film 12 is in between that overlap region. Does that make sense?

A. Yes. Again, at least in this slice of the page it is clearly directly above this portion of region 9 and directly below that particular portion of element 13.

Q. Okay. For that region where there is overlap, can you determine what the capacitance is due to that effect based on the equation in paragraph 32 of your declaration?

A. I'm sorry, due to which effect?

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Q. The effect of the overlap -- well, let me back up for a second. Would you agree that there is a capacitor formed by the layers 13, 12 and 9 where 13 and 9 overlap vertically?

A. So in loose colloquial language amongst persons of skill, one would understand that phrase. In this case, however, when you say, I think you asked me is there a capacitor there, it is not a capacitor that is constructed deliberately for the purpose of storing charge. Those people in that colloquial sense would understand likely, given the question you are referring to the unwanted parasitic capacitance between conductor 13 and the substrate 9, and with those provisos, they would say sure there is a capacitance there. That is unfortunate, because it limits the performance of the device.

Q. So you would agree that there is a parasitic capacitor formed by the layers 13, 12 and 9 where the layers 13 and 9 overlap vertically?

A. Well, if I was speaking, I believe I would try to be more precise and say there is a parasitic capacitance and that this then can be

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modeled as the patent does making certain assumptions, some of them not even explicated, that we can model that as a capacitor just like we can model the structure to the left or right, which includes the trench as a capacitor, and we can think about these in parallel or series and come to understandings about the effect upon the parasitic capacitance with these kinds of simple models, but I would want to use the word "capacitance" rather than capacitor.

Q. Okay. So you would agree there is a parasitic capacitance formed by the layers 12, 13 and 9 where the layers 13 and 9 overlap vertically?

A. Yes, and not just where they overlap vertically, because that is the way parasitic capacitance works, but certainly where they overlap, yes.

Q. Can you determine that parasitic capacitance using the equation in paragraph 32 of your declaration?

A. So do you mean determine the capacitance with actual numerical value?

Q. Well, assume that somebody was able

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to tell you what the dielectric constant of layer 12 was. They were able to tell you what the thickness of layer 12 was between layers 9 and 13. And they were also able to tell you the area of overlap between layers 9 and 13.

If you were given that information, would you be able to determine the capacitance, the parasitic capacitance, using the equation in paragraph 32 of your declaration?

A. I would be able to estimate the parasitic capacitance that line 13 would experience in its totality as in this hypothetical as it would be experiencing contribution from that area.

If the hypothetical is I magically cut out all other componentry and just now had this little cube and I had all the right dimensions and all the materials parameters with nothing else outside of the area of overlap, the formula would be adequate for getting a reasonable estimate of what the parasitic capacitance would be in that hypothetical.

Q. Okay, and similarly, would you be able to use the equation in paragraph 32 of your

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declaration to determine the contribution of parasitic capacitance from the region between line 13 and below the trench isolation that is between the two sections labeled 9 in figure 19?

A. Again, as a starting proposition, that formula in paragraph 32 of my report is correct. You know, in this case, we have a little bit of added complexity immediately, because of the, at least as illustrated in figure 19, trapezoidal shape of the trench, and since we are talking about the capacitance between wire 13 and the substrate now directly underneath the trench, if I am understanding your question correctly, in my previous hypothetical, if you took the smallest dimension at the bottom of the trapezoid and in two dimensions, three dimensions, cut out everything that is outside those vertical lines, then it would be the same answer.

You would have two different, presumably at least the possibility of two different dielectric constants for two different structures, but yes, as a starting point, if you hypothetically cut everything away, yes, that is how I would estimate it.

Q. Okay, and similarly for the region, for the rightmost region labeled 9, you could use the equation in paragraph 32 of your declaration to calculate the contribution of parasitic capacitance from that region?

A. I would give the same answer as I did in totality for the leftmost region 9.

Q. And again, that capacitance would be a function of the distance between the two, sorry, the thickness of the insulating material between the two regions of interest, the overlapping area of the regions of interest and the dielectric constants of the insulating material?

A. In the hypothetical where you cut out and removed everything else, yes. Then you would have a simple parallel plate capacitor.

Q. Okay. If you go to paragraph 35 of your declaration, that is what is being done in figure 21A? Is that right?

A. Yes. The patentee in figure 21A and B is drawing schematics of how in a simple model you would compare the capacitance between element

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13 and substrate with these two different structures, and it is subject to all the provisos that we were just discussing.

It assumes, for instance, that you are only talking about the regions directly overlapping as you posited. It assumes from A to B that areas haven't changed and things like that, so a worker of skill understands it for what it is, and it is illustrative, and it makes the point of why different structures of these two types will have different capacitances, all things else being equal.

Q. And is it your understanding that in the '736 patent, to the extent there is discussion of reducing capacitance, this is what they are using as a comparison?

MR. CARTER: Objection to form.

A. I think in the '736, again, it is what the patentee is alleging is one solution to increasing the speed of chips, and this was of course well known as desirable, and parasitic capacitances were well known as deleterious to that effort, and with that understanding, he correctly posits that the parasitic capacitances

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in the region of these isolation structures can be reduced by two means and that the worker of skill understands that, independent of everything else that is going on everywhere else in this chip with millions perhaps of transistors and miles of wires, that the contribution made to the overall speed of the chip could be improved by addressing this issue in this particular region of a chip.

Q. Can you assume for me that the area of overlap where the capacitance CA1 is shown, that that area of overlap is A1?

A. And so there would be three A1's here?

Q. There would be three A1's, yes.

A. In figure 21A.

Q. Yes.

A. Okay. I understand your posit. I don't know what area is, but I'll just assume there is some area of overlap.

Q. Well, the area of overlap between 13 and -- between the wire 13 and the substrate.

A. Yes.

Q. As is relevant to the calculation,

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your formula.

A. Right.

Q. Okay. Can you also assume for me that the distance between the wire 13 and the substrate is D1 in that region?

A. The green insulator, yes.

Q. Yes. Okay, and assume that the dielectric constant of the green insulator is epsilon 1?

A. Okay.

(Bravman Exhibit 5, Blank piece of paper, was so marked for identification, as of this date.)

Q. This is a blank piece of paper. Exhibit 5 is a blank piece of paper, correct?

A. Yes.

Q. Can you, with the assumptions we just discussed about the capacitance in CA1, can you write out what CA1 is.

With the assumptions we just discussed about the area, distance and dielectric constant, can you write out the formula for what CA1 is using your equation in paragraph 32?

A. Well, I am only -- first of all, it

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is going to be such a calculation or an equation for such a calculation always is going to have certain assumptions built in, and if we build in the assumption that again I'm magically cutting everything out except the overlapping areas to the left and right above and below the page, then it is simply the formula that is in my report, and it would be that formula.

Q. Can you just write that on the page, please, for me.

A. Call it what? CA1?

Q. CA1.

A. So it is going to be CA1 equals epsilon zero, and then epsilon 1, and then it is over times A the area and the distance, and that assumes no other materials present outside of, I will put in quotes, projected area of overlap.

Q. And I think I said that the distance we'll assume is D1, and the area of overlap is A1. Okay.

What about CA2? Can you write the formula for that, assuming that the distance there is D2, and the area of overlap is A2. Well, let's assume that the dielectric constant of region 8 and the dielectric constant of region 12 is the same, just to make it simple.

A. Okay.

Q. That also is epsilon 1 for the dielectric.

A. Also epsilon 1. Yes. That is CA2. CA2 equals permittivity of free space times again epsilon 1 under our assumption and times the area of overlap A2 divided by D2 with the same assumptions as above and assuming the dielectric constant of 12 and 8 are the same.

Q. Thank you for that. You are a professor?

A. Yes.

Q. You teach classes right now?

A. I give guest lectures.

Q. When you say guest lectures, what do you mean?

A. I give a lecture or two in classes where I'm not the professor of record.

Q. So if the professor is unavailable, then you will step in, perhaps?

A. No, if he asks me to give a class or if she asks me to give a class on their behalf.

Bravman

Q. What subjects will professors ask you to step in to give a class?

A. Materials science and specifically related to the microelectronic industry.

Q. For a given capacitor, if you change the voltage applied to the plates of the capacitor, that won't change the actual capacitance of the capacitor, will it?

A. Assuming that you haven't damaged the capacitor by overloading it to very good order, that is correct. It is a very good assumption. That's correct.

Q. Is that a good assumption here in the context of the '736 patent?

MR. CARTER: Objection to form.

A. There is no discussion of any secondary effects of changing voltages, changing the capacitance. That is not in play here.

Q. Just to be clear, you are saying that it is a good assumption in the context of the '736 patent that changing the voltage to the plates of the capacitor doesn't change the capacitance of the capacitor, is that right?

MR. CARTER: Objection.

Bravman

A. If you say of the capacitor and that's probably understood, I would agree with that. Under those assumptions, I would agree. The capacitor has to be of course well defined, hence, in the exercise you gave me, I was talking about a hypothetical region of space.

Q. Is it a good assumption in the context of the '736 patent that changing the voltage to the wiring -- sorry, across -- let me withdraw that.

In the context of the '736 patent, is it a good assumption to assume that changing the voltage between the wiring and the substrate does not change the parasitic capacitance of the structure?

A. The parasitic capacitance as properly modeled would not be dependent on the voltage most likely.

Q. Is your understanding that the purpose of the dielectric film in the '736 patent is to reduce the capacitance -- sorry -- the parasitic capacitance between the wire and the substrate?

A. It is -- that is one of the posited

Bravman

solutions to the problem, which the patent addresses, which is parasitic capacitance in a specific region in service of the overall goal of improving the speed of the chip.

Q. So one of the posited solutions to the problem, which the patent addresses, is to reduce the capacitance between the wire and the substrate using a dielectric film?

A. In the isolation regions, the patent, as I recall, uses the phrase isolation regions or just region as contributing to a reduction of the overall parasitic capacitance experienced by every conducting wire and the totality of the substrate, and so it limits itself in my read to the isolation regions, but in service of that known problem.

Q. So one of the purposes of the dielectric film in the context of the '736 patent is to reduce parasitic capacitance in the isolation region? Is that right?

A. Yes. The contribution of that region of the chip or the device to the overall calculation of parasitic capacitance between any given wire that happens to run over an isolation

Bravman

region.

Q. And in particular, the particular purpose of the '736 patent dielectric film is to reduce the capacitance between the wire and the substrate in the isolation region, correct?

A. Right. The particular solution posited to the stated problem of increasing speeds is limited in my read to the isolation region.

Q. So a benefit of the dielectric film in the '736 patent is to reduce capacitance between the wire and the substrate, correct?

A. Yes, and particularly again the contribution of the parasitic capacitance between a wire and the substrate that is made by the wire over the substrate in the isolation region.

Q. And similarly, a benefit of the resistor film in the '736 patent is to reduce capacitance between the wire and the substrate, correct?

A. Yes. By reducing the capacitance of the wire substrate structure in the isolation region, it contributes to an overall reduction in the wire substrate capacitance and therefore

Bravman

increases -- contributes to increasing the speed of the chip.

Q. So Intel's proposed construction of dielectric film repeats the words "a dielectric film" and then adds "a benefit of the dielectric film" as used in the '736 patent as the construction?

A. I'm sorry, could you ask that question again. I thought the two posited constructions were the same except for --

Q. Right. Yeah. Let's just focus on dielectric film first. Okay?

A. Okay.

Q. I don't want to ask you about two different things because you might have two different answers.

A. Sure.

Q. So let's just focus on the dielectric film.

A. Okay.

Q. Intel's proposed construction of a dielectric film repeats the words "a dielectric film" and then adds "a benefit of the dielectric film" as used in the '736 patent. Is that right?

Bravman

A. So I don't see the word "benefit" in the posited claim construction.

Q. Well, we just discussed a benefit of the dielectric film in the '736 patent is to reduce the capacitance between the wire and the substrate. Right?

A. Yes. I'm sorry, I thought you were saying that word "benefit."

Q. Oh, no. I didn't mean literally. I just want to understand where the construction comes from.

A. Right, and I think that is a very important point, because again the patent is speaking to making chips faster, and it does that by addressing the capacitance of a wire and the substrate, and then it further goes on to where a wire is above a substrate in the isolation region, here's two methods for reducing that region's contribution to the overall parasitic capacitance.

This is how a worker of skill reads it, relative to the substrate in service of the stated problem.

Q. So I think there is a bit of back and

Bravman

forth there. I want to make sure the record is clear between the question and the answer.

Intel's proposed construction of a dielectric film repeats the words "a dielectric film," and then adds to it "a benefit of the dielectric film" as used in the '736 patent, is that right?

MR. CARTER: Objection to form.

A. Well, again, as you just said, not literally. It says "a dielectric film" means "a dielectric film for reducing the capacitance between the wire and the substrate."

Q. And reducing the capacitance between the wire and the substrate is a benefit of the dielectric film in the '736 patent, correct?

A. Yes. It is a benefit in service of the stated problem of chip speed.

(Recess taken from 10:42 a.m. to 10:56 a.m.)

BY MR. MIDDLETON:

Q. During the break, Dr. Bravman, did you speak to counsel about the substance of your testimony?

A. I did not.

Bravman

Q. Turning to paragraph 47 of your declaration.

A. Okay.

Q. You state, the first sentence says "There were well-known uses for dielectric films in semiconductor fabrication processes before the '736 patent that were unrelated to affecting parasitic capacitance."

A. Yes.

Q. And then the second sentence says "For example, dielectric films have commonly been used between adjacent metal layers in a semiconductor device to insulate those layers from each other," right?

A. Yes.

Q. Wouldn't the dielectric film -- wouldn't that structure with the dielectric film between adjacent metal layers have a parasitic capacitance?

A. All structures and air and free space have the potential of creating parasitic capacitances, yes.

Q. And in this example that you have given, the dielectric film that is used between

Bravman

adjacent metal layers in a semiconductor device to insulate those layers from each other, wouldn't that create parasitic capacitance?

A. Yes.

Q. So wouldn't that affect the parasitic capacitance of the device?

A. It would, but what I am explaining here is that dielectric films, as it says well-known uses and in the employ of those materials for those uses, parasitic capacitance is well known to be a factor, but dielectrics are used for building capacitors. They are used for insulators, as I illustrate here. They are used for other process steps. They are used for hermetic seals on the top of a chip.

Like all materials, they have a permittivity which affects parasitic capacitance as well.

Q. If a dielectric film is used as an insulator, does that mean it can't be the dielectric film of the '736 patent?

A. The dielectric film or films in the '736 has to be an insulator. Otherwise it wouldn't serve the purposes that the '736 clearly

Bravman

articulates.

Q. And if the dielectric film of the '736 patent were used to assist in insulating between metal layers -- well, let me withdraw that.

If a dielectric film were used in part to insulate between the wiring and the substrate, would that dielectric film necessarily not -- sorry. I will withdraw that.

If an insulating film were used in part to insulate between the wiring and the substrate, would that insulating film necessarily not be a dielectric film as used in the '736 patent?

MR. CARTER: Objection to form.

A. Boy, I'm sorry. That is a convoluted question. Would it necessarily not be a dielectric film described as being added to a structure to reduce capacitance? There is many dielectric films present in the '736 patent, so I just want to make sure I am understanding the same of what you are speaking of precisely.

Q. So the term "dielectric film" in the '736 patent, the way that that term is used,

Bravman

okay, if an insulating film were used in part to insulate between the wiring and the substrate, could that insulating film be a dielectric film as the term is used in the '736 patent?

MR. CARTER: Objection to form.

A. The dielectric film in the '736 patent is an insulator, and so it would contribute. It would be part of providing an insulating layer necessarily.

Q. Can you turn to paragraph 53 of your declaration.

A. Yes. Okay.

Q. Can you explain what you mean by the first sentence in paragraph 53?

A. That the patent is not claiming to invent anything outside of the use of the known properties of a dielectric for decreasing the capacitance between the wire and the substrate in an isolation region. That is what the claim is about. What the patent is about.

It is teaching as it says there to add the claimed dielectric film to an otherwise standard structure, STI structure. I don't read anywhere where he is making a claim that asserts

Bravman

a purpose for decreasing, sorry, a purpose for adding the dielectric film other than for the purpose as stated.

Q. Okay. So when you say that was already known in the prior art, you are referring to the STI structure only, not to the stated or implied teaching to add the claimed dielectric film?

A. The patent describes the alleged invention in terms of an STI structure, and he is not claiming the inclusion of this new dielectric film structure for anything except as it says the purpose of decreasing capacitance.

Q. What if a designer of a chip designs it with a dielectric film that was added for a different purpose, but unknown to the designer because they weren't paying attention, it also decreased capacitance compared to a previously designed structure. Would that be a dielectric film of the claim?

MR. CARTER: Objection to form.

A. Well, the physics of a structure is a function of its materials and configurations. The reader or the person of skill understands

Bravman

with that being true what the patent owner is claiming as his invention in a well-articulated narrow scope.

Q. I guess my question is a little bit different, because we were talking about the purpose for including dielectric film, and my question is, if a dielectric film were added, not for the purpose of affecting parasitic capacitance, but in fact it did decrease parasitic capacitance compared to a previously designed structure, would that be a dielectric film of the claim?

MR. CARTER: Objection to form.

A. I'm not sure how to answer that because it sounds like to me again what you are really creating is a hypothetical. Here is a structure, and if I hear your question as, if the structure is form A or form B, and form B includes this thing that has been added, yeah, in both cases you can calculate direct or parasitic capacitances.

The teaching, however, of the patent, which is what I understand is my obligation to try and explicate, is the inclusion of another

Bravman

structure for the expressly stated purpose of reducing parasitic capacitance.

Many people are involved, many people, large numbers of people are involved in designing and validating and building chips.

Q. So if you are looking at a product, how do you determine if the purpose of including the dielectric film in that product is to reduce parasitic capacitance?

A. Well, I think a worker of skill, for instance, would look at let's say starting with figure 19, the prior art. A worker of skill is going to know that layer 12, for instance, is going to have to be designed such that it has a given set of materials properties, its permittivity, relative permittivity, and dimensions and thickness, and if one saw that in this isolation region, because that is what the patent speaks about, that there was another structure or 12 was thicker than it was outside, where the designer is generally going to know it is going to be the minimum thickness required to within stated margins have the chip function as best it can, I think a worker of skill would say,

Bravman

oh, it is thicker there, oh, there is another structure there, why would it be there, understand that that would map onto the patent.

Q. And what if the thickness didn't change in the chip of this layer 12, could that be a dielectric film in the context of the '736 patent?

MR. CARTER: Objection to form.

A. Layer 12 is stated to be a dielectric film. It is an insulator. It therefore has dielectric properties.

Q. Now what if a designer has a chip that he decides he wants to sacrifice some sort of operation, is willing to allow for a higher parasitic capacitance, so he redesigns his chip so that it has a dielectric film that underlies an insulating film, but now he just decreased the thickness of the dielectric film so that he can maintain whatever purpose he wants for it. Could that dielectric film be the dielectric film of the '736 patent?

MR. CARTER: Objection to form.

A. If I am understanding your question correctly, no, because you are saying he is

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reducing 12, the thickness of 12, while implementing a dielectric film. Those two things would seem to be running counter.

Q. Okay. Now suppose that you were looking at the device, and you have no information about how the designer came about choosing that thickness for that layer. Then how would you determine whether that dielectric film is dielectric film in the context of the '736 patent?

MR. CARTER: Objection to form.

A. I think a worker of skill trying to understand if the '736 patent read on the observed structure would need to know if any material present comported with the clear reading of the claims of the patent in light of the intrinsic record, because that is going to be a legal question.

You are asking me I think in part a legal question. Is it the film of the patent, and the dielectric film of the patent as claimed and described in the full intrinsic record a worker of skill would understand had characteristics to it, and so I think to answer

Bravman

your question in this legal context that is what you would have to know.

Q. Generally speaking, the term "resistor film," is that a term that would be understood without clarification?

A. Yeah. It is a bit of, in my opinion, it is a bit of an odd term, resistor film, but a worker of skill understands that a structure for the purposes of having a known resistance would be covered by that kind of claim or that kind of language. Yes.

Q. Can you turn to paragraph 56 of your declaration.

A. Yes.

Q. In paragraph 56, you say that "The resistor film is added to the prior art STI structure to reduce the voltage applied to the top and bottom faces of the insulating film and therefore decrease wire-to-substrate capacitance."

Correct? At the very end of the block quote.

A. Yes.

Q. Now, in that block quote that you

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provide, there is no statement that the wire-to-substrate capacitance is decreased, correct?

A. So in the patent, my opinion, the proper read and a consistent read of the patent, the patentee includes the following: The patentee clearly is describing modifications to prior art structures in isolation regions, and at one point in the patent he clearly says there are two physically correct ways of doing this.

One is to in that region decrease the capacitance between the wire and the substrate in the isolation region or to reduce the charge stored in the capacitor structure in that region. Both of those reduce the wiring to substrate capacitance of the device, and throughout the patent starting at the very beginning the patentee talks about reducing the wiring-substrate capacitance to improve the performance of the device, and the worker of skill then goes on to read and understand that he provides two means of making a contribution to that, and that is to work within this isolation region with the two mechanisms I cited a moment

Bravman

ago, and that is why I agree with the claim construction, because in terms of a semiconductor device, which I take to read and I think a worker of skill would understand is the point here. You don't talk about increasing speed of the wiring in isolation region. You talk about speed of the device or certain circuits within, and that to me is the consistent story the patent tells.

Q. In your opinion, when the resistor film reduces the amount of charge accumulated in the region of the substrate, sorry, of the semiconductor device containing the resistor film, that that necessarily reduces the wiring to substrate capacitance in that region?

A. No, he doesn't say in that region. He is very clear that in that region here are two phenomena we can consider, and they are both in service of reducing the parasitic capacitance of the device, sorry, of increasing the speed of the device by making a contribution to improved parasitics. His physics is correct.

Q. So just yes or no ,do you agree or disagree when the resistor film reduces the amount of charge accumulated in the region of the

Bravman

semiconductor device containing the resistor film that that necessarily reduces the wiring-to-substrate capacitance in that region? Yes or no?

A. I don't think that is a yes or no question, but the patentee speaks to that.

Q. Well, let me withdraw that question.

A. Okay.

Q. Do you agree or disagree when the resistor film reduces the amount of charge accumulated in the region of the semiconductor device containing the resistor film, that that necessarily reduces the resistor to substrate, sorry, the wiring-to-substrate capacitance in that region? Yes or no?

A. No, the patentee says, and I take it as a worker of skill he is saying, you know, even when the capacitance in that region is not changed but the charge stored is, that is a contribution to the speed improvement, because the charge buildup and draining can occur faster.

I mean he is right about that, but that physical phenomenon that he cites to, when the resistance film is included, contributes to a

Bravman

reduction overall in the parasitic capacitance of the wires to the substrate, and again he is talking about in the region.

The speed, however, the chip is controlled by a myriad of factors, and he is talking about improving the speed of the device, and again here is a way to contribute to that. That is how I read this patent.

Q. Now going back to paragraph 56 of your declaration.

A. Yes.

Q. That quoted text. I want to make sure that I have this right. The quoted text in paragraph 56 does not say that the resistor film is added to decrease wire-to-substrate capacitance. Is that right?

A. In this quoted text here, no. Here he is getting closer to the ultimate description at the last clause, which is "The time required for charging or discharging between the wiring and high resistor is reduced resulting in the semiconductor device operating at a higher speed."

Again, that is the purpose of -- I

Bravman

read that is the purpose of the alleged invention is to make that operative, and I know as a worker of skill that that results from an overall reduction in parasitic capacitances.

Q. One embodiment of the '736 patent is illustrated in figure 12, right?

A. Yes.

Q. In figure 12, a wire 13 is formed on an interlayer insulating film 12, correct?

A. Yes.

Q. And the interlayer insulating film 12 is formed on an underlying interlayer insulating film 81, right?

A. Yes. Let me just look and make sure that comports with my memory. Yes, it says that in column 10, an underlying insulating film formed beneath an interlayer insulating film.

Q. And the insulating film 81 is formed on dummy semiconductor regions 9?

A. Yes. The figure illustrates that in the cross-section.

Q. In figure 12 of the '736 patent, the capacitor -- withdrawn. Then another embodiment of the '736 patent is illustrated in figure 5,

Bravman

correct?

A. Figure 5 illustrates another embodiment. That's right.

Q. In figure 5, a wire is formed on an interlayer insulating film 12, correct?

A. Yes. That is structure 13.

Q. Okay, and the interlayer insulating film 12 is formed on a resistor film 53?

A. That's correct.

Q. And in this structure the parasitic capacitor is formed in which the wire 13 and the resistor film 53 are the plates of the capacitor, and the interlayer insulating film 12 forms a dielectric between the plates?

A. Well, that is what was posited by Mr. Healey in his report. The patent does not explicitly say that to be the case. I understand the patent, when it makes the assumptions that it does, it is as Mr. Healey says, it disregards other capacitances. It doesn't say any basis that I'm saying he says explicitly 53 is the second plate of a capacitor.

I don't recall seeing that in the specification. It does describe it, however, in

Bravman

terms of materials as you stated.

Q. So you disagree that a capacitor is formed by layers 13, 12 and 53 in figure 5?

A. No, I didn't say that. I am just saying that, because the patent clearly says -- let's just -- it is sufficient I think is the word it uses to consider 13, 12 and 53, but it doesn't as a textbook might explain under what conditions it is sufficient and why it is sufficient.

If the entire capacitance of that region is included or accounted for by 13 and 12 and 53, I don't know why you would use the word "sufficient," and I don't know why he would talk about the full voltage drop from wire 13 to the substrate as occurring in these two pieces, the two pieces being 13 to 53 and then 53 to the substrate.

Q. I think I understand the issue now. Okay. So I understand there is 52 and 51 there. I want to work my way through this.

If you are looking at a problem like this, would you agree that it makes sense to try to figure out what the components are

Bravman

individually before you start looking at the -- trying to solve the whole problem?

A. Well, sure.

Q. Right, so let's focus in on 13, 12 and 53, recognizing that there are other structures here. I'm not talking about the entire wiring-to-substrate capacitance. I just want to ask or focus in on 13, 12 and 53, and my question is do you agree that layers 13, 12 and 53 form a parasitic capacitor?

A. If 12 is not floating freely surrounded by dielectric, it would present a parasitic capacitance. It is a little more complicated if it is completely surrounded by dielectric, but the elements of a capacitor two plates conducting and is separated by a dielectric are clearly there.

Q. You said if 12 is not floating freely. Do you mean 12 or 53?

A. Thank you. 53.

Q. When you say that if 53 is not floating freely, then it is a little bit more complicated?

A. If it is completely surrounded by

Bravman

dielectric, if it is floating freely.

Q. Okay.

A. It could be a bit more complicated. I haven't thought about that completely, but, yes. It is like a gigantic EEPROM device with the wrong dimensions to work.

Q. Is that because you don't know if or how much charge might be within the region 53?

A. Yeah. I mean, if 53 is not connected to anything else, electrically connected, the only way to get charge on it is to tunnel it through the insulator 12, and if insulator 12 is thick, as this kind of indicates, you would not expect a significant charge to accumulate there.

Q. Okay. Now the resistor film 53 is formed on a silicon oxide film 52, correct?

A. Yes. Let me see if it says 52 is oxide or just dielectric. I don't recall. Yes. It says silicon oxide 52.

Q. And you would agree that the silicon oxide film 52 is a dielectric film?

A. Yes.

Q. And the silicon oxide film 52 is formed on a dummy gate 51?

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A. That is what it describes, yes.

Q. Now the resistor film 53, silicon oxide film 52 and the dummy gate 51 formed a capacitor, correct?

A. Well, again, the same types of questions. It is not clear if 51 is electrically connected to anything else that is conducting, and so a capacitor, a device, I don't see here that you can say unequivocally that it is or is not a device, a capacitor.

One can model the capacitance between 53 and 51 with 52 intervening with the right assumptions.

Q. What assumptions are those?

A. Well, again, is it really a plate, or is it a free-floating dielectrically surrounded metal plate, but the same answer as before. The elements of a capacitor structure are present.

If I knew, for instance, that 51 and 53 were held at the same potential, the elements of the capacitor are there, but there is no charge storage, so those are the kind of details you would want to answer especially in a legal context what exactly is meant. The patent

Bravman

doesn't say one way or the other, to my reading.

Q. Is there a capacitance between layers 51 and 53?

A. Capacitance is a physical phenomenon, and as drawn here, there is no indication that 51 and 53 are tied electrically. If they were tied electrically, however, I guess I would say there is no capacitance there, because you de facto could not maintain a field, electric field, across the gap, 51 to 53, that was occupied by dielectric 52.

Q. If you had, if you went to a store and bought a capacitor, and you were to look at that structure, would you be able to tell me what the capacitance of the capacitor was?

A. The capacitance again is a function of the materials and the dimensions, as we have talked about.

Q. Okay. So is that a yes or a no?

A. Well, if I had all the information about the materials and geometries, yeah.

Q. Okay. Now, if I were to tie both ends of that capacitor to the same voltage, would that affect the capacitance of the capacitor?

A. Well, that is an interesting question, because the capacitance by the formulas, the simple formulas we have been using, sure, that would be unchanged, but, with the wires, the two ends tied together, I would say, well, under this configuration, the only way to access that capacitance is to untie them, but the dielectric constant doesn't change. The distance doesn't change. I get that.

Q. So the capacitance itself wouldn't change. It is just whether you can make use of that capacitor's changes, right?

A. Inherent in that formula is the fact that, and it is, first of all, we know that it only obtains in the idealized case of parallel plate capacitors, inherent in that, and if you say that is the capacitance, I mean a worker of skill understands that, if you don't have two parallel plates that are separated by a dielectric, if they are connected by a wire or to each other, they are not separated by a dielectric, not electrically.

Q. Let's ignore the wiring in and out.

A. Okay.

Bravman

Q. And just look at the structure of the capacitor that you have purchased.

A. Yes.

Q. Does the fact that you tied the two ends together affect the capacitance of the capacitor that you purchased?

A. I understand your question clearly, but it gets back to, if you don't have knowledge, a worker of skill says, okay, here is the capacitor, here is the materials, here is the configurations. I can estimate the capacitance. He or she is clearly assuming that the parallel plates are not electrically connected. They are separated by a dielectric, and so that formula, as with all formulas and all models, is based upon a set of assumptions, and the assumption is the parallel plates are not electrically tied. That is why, for instance, in the most simple case, one starts learning about RC circuits, because now they are tied with the resistance between them, et cetera.

So that is the correct formula for estimating capacitance in a set, a structure, but there is assumptions behind it, and one is the

Bravman

plates are separated electrically and physically by a dielectric.

Q. I am handing you Exhibit 6, another blank paper. Can you draw the circuit diagram of the capacitor that you purchased with its ends connected by a wire.

(Bravman Exhibit 6, Blank piece of paper, was so marked for identification, as of this date.)

A. Well, schematically, because I don't know what the configuration is, but the typical circuit symbol for a capacitor is two parallel lines, and assuming this is a wire, the two plates are now electrically tied and therefore at the same potential.

Q. Okay. Those two parallel lines you drew, is that the schematic symbol for a capacitor?

A. Yes.

Q. And what is the capacitance -- does the capacitance of that capacitor that you pointed to with the arrow, does that change depending on whether the wires are connected?

A. Well, you have to understand then the

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context for the word "capacitance," because in this configuration this device has no capacitance electrically speaking, because if I connect this to some other circuit out here, all this circuit is going to see is a dead short across the capacitor.

So in any sense that a worker of skill would understand it, if you did this, that capacitor has no capacitance.

Q. But it is still a capacitor?

A. It is still a capacitor.

Q. Okay. So let's go back to layers 53, 52 and 51. Regardless of how they are connected, layers 53 and 52 and 51 in figure 5 form a capacitor, correct?

A. They have the elements of a capacitor. You know, one is an actual device. All the elements again are present. In this drawing, I clearly see two parallel conducting structures separated by a dielectric. If they are electrically tied, I wouldn't call it a capacitor, because it has no ability to store charge or energy.

Q. But when you drew it there in your

Bravman

circuit, you drew it as a capacitor. Why did you draw it as a capacitor?

A. Because you instructed me to.

Q. I asked you to draw the setup as you would in a schematic diagram. I didn't say that you had to draw the capacitor, but you still drew it there, didn't you?

MR. CARTER: Objection to form.

A. I drew the capacitor as I stated it and as you correctly queried me about what's the standard symbol for a capacitor.

Q. No, I asked you what that symbol was, and you used the standard symbol for a capacitor.

MR. CARTER: I object to the form again.

Q. Correct?

A. We can read back your exact question, but it is the standard symbol for a capacitor.

Q. That is because the capacitor exists regardless of how the ends are connected, correct?

A. The capacitor exists.

Q. Right.

A. I have not destroyed it.

Bravman

Q. And in the same way, layers 51, 52 and 53 in figure 5 form a capacitor. Isn't that right?

A. You said if I go down to the hardware store and buy a capacitor. When I look at a structure in a semiconductor device like this, I would not necessarily give the same answer. You, I believe, said you go and buy a capacitor, and I have again said this has clearly in this cross-section the elements of a capacitor for the reasons I have said, but under the right circumstances, it could store a charge, but there is conditionality there.

Q. All right. Let's assume that layers 51 and 53 are not connected.

A. Okay.

Q. Layers 51, 52 and 53 form a capacitor, correct?

A. There is a capacitance that would be associated with that structure. Again, I don't know if 51 is actually connected to anything or free-floating, but under the right circumstances, that region of the device would have the ability to store a charge.

Bravman

Q. Regardless of whether layer 51 is connected to anything, as long as it is not connected to layer 53, there is a capacitance between layers 1 and 53, correct?

MR. CARTER: Objection to form.

A. Between -- now you added 1. The substrate?

Q. Layers 51 and 53.

A. Oh, okay. Yes. One could calculate the capacitance. Again, if it was free-floating, I think the calculation would be not as easy, but again the elements of a capacitor are there, but it still depends on what else is going on.

Q. So if the relative voltages between 53 and 51 -- well, let me withdraw that. If the voltage difference between layers 53 and 51 were some value -- let me withdraw that.

There are some disclosures in the '736 patent that include a resistor film like resistor film 53, but are not described as including a silicon oxide film 52 and a dummy gate 51. Is that right?

A. Yes. I think we just looked at one a little while ago. The previous figure you

Bravman

directed me to.

Q. Is that figure 12?

A. Yes.

Q. Is it your understanding that layer 81 in figure 12 could be a resistor film?

A. Let me just clarify that. No. Figure 12, 81, is an insulating film.

Q. If 81 were a resistor film, would it satisfy the resistor film requirements in claim 13?

MR. CARTER: Objection to form.

A. I haven't thought about that, because that is not within the scope of the patent. I would not expect to see a resistor film laying on top of a substrate as this is showing here.

Q. Can you look at claims --

(Bravman Exhibit 7, Claim 13 of '736 patent, was so marked for identification, as of this date.)

Q. You have been handed Bravman Exhibit 7. On Exhibit 7 is claim 13 of the '736 patent.

A. Yes. That's right.

Q. And Exhibit 2, which I previously handed to you, that is claim 6 of the '736

Bravman

patent.

A. Yes.

Q. Can you compare these claims, and let me know what the differences are between these two claims.

A. I believe the first five elements are the same, and in the final sixth element, we changed the asserted structure from a dielectric film to a resistor film, and it gives the configurations.

Q. Are the configurations of the resistor film and the dielectric film different?

A. Well, it uses somewhat different language. Interposed and formed under. So the language is not exactly the same. It doesn't say, for instance, directly under. One would not expect a resistor film to be contacting the wire.

So one assumes there is going to be an insulator dielectric between them, and dielectric film interposed between at least, so it has got some nuances, and it makes some assumptions, but a worker of skill can understand the configuration.

Q. Okay. Now, going back to figure 12,

Bravman

if you keep those claims in front of you as well, figure 12 illustrates an embodiment of claim 6, is that right?

A. Yes. The patent calls that in column 23 the eighth embodiment.

Q. And in figure 6, it has the first five elements of claim 6, correct?

A. Figure 6 or figure 12?

Q. Let me withdraw that. In figure 12, it has the first five elements of claim 6, correct?

A. Yes.

Q. And figure 12 also has the first five elements of claim 13, correct?

A. It has to, because the words are the same.

Q. Okay. Figure 6 also has the dielectric film, sorry, withdrawn. Figure 12 also has the dielectric film of claim 6, correct?

A. If 81 is a dielectric film, those words describe the image. Yes.

Q. Okay. Now suppose 81 were a resistor film.

A. Okay.

Bravman

Q. Would it satisfy the last limitation of claim 13?

A. Yes. The words in 13 with the elements in figure 12, described as they are in the text, they would also describe that if 81 was a resistor film.

Q. What structure would you compare figure 12 to in order to determine whether the dielectric film 81 reduces capacitance between the wire and the substrate?

A. So the thought experiment would be the structure of figure 12 with and without 81 in place.

Q. And when you do that comparison, does the thickness of layer 12 change?

A. In the first approximation, no, but of course it is a variable, but if you want to compare including a new structure in this case 81, you would at least start with not changing other values, but of course you could.

Q. Well, how would you know what to do?

A. Well, I would assume that 12 is the thickness, knowing how these chips are built, that is specified for the purposes of serving as

Bravman

an insulating layer between conductors and other conducting elements below it, and I would assume that that thickness is specified. It is specified.

If the posit would be in just this region, 12 was change thickness, that could be built, but then I could see that, and I would want to understand why that was the case, assuming I had either the process recipes or good enough teardowns.

Q. What if you didn't have the process recipe?

A. Well --

Q. Or good enough teardowns?

A. Well, still, since we are talking in the context of this patent, I would compare it to the prior art, figure 19, and although I know figures, unless scaled, are not to scale or dispositive, the figure of the prior art, the figure of 12, the text of the patent, the teaching of the patent, the assertion of the patent clearly is in this instance the insertion of structure 81 into the chip differentiating it from the prior art for the clearly expressed purposes of the patent, knowing that in the real world you don't insert 81.

You redesign the recipe, and you build it there, but what the patentee is taking the reader through is a set of exercises, a set of embodiments that address a problem. So 81 is clearly there for the purposes stated.

Q. Suppose that you are looking at a device that has this exact structure, figure 12, and you are not shown figure 19 for that device, and you are not given figure 19 of the '736 patent. How would you determine whether that structure has a dielectric film that satisfies Intel's construction?

A. Well, either you have enough information by one mechanism or not to answer a question of a given level of detail. If you give me the drawing of figure 12 and don't tell me what the materials are, but said, hey, this involves an isolation region, I think most workers of skill would recognize this as a portion of a chip where there were active devices.

There were isolation regions

Bravman

separating active device from isolation regions, that I see what almost certainly has to be an insulating layer 12, because of its role in the active device 3, and so one would go through those steps, and then one would say, well, if I just look at this drawing, I understand things may not be included, but my first posit would be that 81 covering the semiconductor portions of region 7, the isolation region, you know, I would not expect that to be a conductor.

I would expect that to be an insulator, and so a worker of skill would start making these assumptions, but if you hypothesize pulling out one assumption after another, it ends up being just lines on a page.

Q. All right. Let's assume that 13 is a wire, 9 is dummy semiconductor regions, 8 is isolation, 12 is an insulating film, and 81 is an insulating material.

If you weren't given figure 19 of the '736 patent, how would you determine whether layer 81 is a dielectric film as that term is construed by Intel?

A. Looking at this diagram and with the

Bravman

suppositions that you gave me, I would and I think a worker of skill would say why is 81 there? Why would they bother doing the lithography there? They have got 12 in place just like a worker of skill would know figure 19 illustrates. Gee, why is 81 there? Oh, it is a dielectric. Oh, capacitance, parasitic capacitance is a problem. This is also well known. The patent admits that easily.

So why is that extra dielectric there? I don't think it is unreasonable at all that a worker of skill would say, oh, it is to address the well-known problem of parasitic capacitance. I don't think that is a stretch at all.

Q. Suppose layer 81 extended to the left over the top of the structure of 3 and off to the edge of that figure. In that instance, would layer 81 be a dielectric film in the context of Intel's construction?

MR. CARTER: Objection to form.

A. Very broad hypothetical, but, and again there are lots of circumstances where it may become less clear, just looking at a very

Bravman

limited set of facts, what it was, but one would immediately understand that, but for the presence of 81 in the isolation region, the capacitance would be altered. That is a fact.

So I think in a legal context my understanding is the worker of skill trying to understand if a claim reads on a process or a device or something else, I mean you are obligated to understand just as much as you can, and if you are saying, well, if I just take this little slice, yeah, maybe you can box out an unambiguous understanding, but I don't think that is what we are trying to do.

We are trying to understand a claim in terms of the intrinsic record and see if it reads on a variety of structures.

There may come a time when that is very easy, and other things that, no, I don't have enough information. I can't say one way or the other.

Q. You said that the presence of layer 81 alters the capacitance.

A. The parasitic capacitance between 13 and the substrate.

Bravman

Q. All right, so layer 81 is in figure 12, the '736 patent. Under the assumption that layer 81 extends to the left side of the figure, you say that it alters the parasitic capacitance, and my question is alters it compared to what?

A. If it wasn't there.

Q. Well, if it wasn't there, are you suggesting layer 12 would be identical to what is in the current figure 12?

A. The claims talk about the wire, 13, laying on said interlayer insulating film, which is 12, and then goes on in the last element to say now let's add. It also includes a dielectric film. I mean it is a separate element, and here is where it is. It is between at least said dummy semiconductor portions of said isolation region and said interlayer insulating film.

So that configuration is met by element 81 in figure 12, and because it says at least said dummy semiconductor portions, it could in fact extend beyond the dummy semiconductor portions. The claim 6 gives that latitude.

Q. I don't think you answered my question. If it wasn't there, layer 12, are you

Bravman

suggesting that -- withdraw that.

If layer 81 wasn't there for the purposes of your comparison, are you suggesting that layer 12 would be identical to what is in the current figure 12?

A. As I said before, at least as a first step, if one is contemplating the change in capacitance of this overall structure with 81 there or not, you would not change other geometries, material parameters and what have you and especially in light of reading claim element, the last claim element of claim 6, there is no direction to maintain or change the structures and materials, and so, in context of the whole intrinsic record, again, the patentee is telling the reader to assume 81 now has been included to alter the capacitance between 13 and the substrate, the parasitic capacitance, and that is the basis of -- one basis of the claimed invention.

Q. Now you prefaced that with at least as a first step. Can you imagine a second or third step in determining whether layer 81 is a dielectric film in the context of Intel's

Bravman

construction?

A. No. I am just answering your question that, you know, what calculation would you do, because if claim 6 clearly requires this dielectric film in a specific position between the dummy semiconductor portions and said interlayer insulating film, I don't see how a worker of skill doesn't read that as another structure, and if you say with it there, without it there, a worker of skill reads that last element and goes through the thought experiment that I just did.

(Lunch recess: 12:03 p.m.)

Bravman

Afternoon Session

12:42 p.m.

Dr. J O H N B R A V M A N, having been previously duly sworn, was examined and testified further as follows:

EXAMINATION (Continued)

BY MR. MIDDLETON:

Q. Good afternoon, Dr. Bravman.

A. Good afternoon.

Q. Did you speak with your attorneys about the substance of your testimony during the break?

A. No.

Q. Turning to figure 5 of the '736 patent.

A. Okay.

Q. Figure 5 illustrates an embodiment of claim 13 of the '736 patent, is that right?

A. Yes. Let me just verify that. Yes.

Q. In figure 5, layer 53 is a resistor film, correct?

A. That's what it's described as, yes.

Q. Layer 52 is an insulating film?

A. Yes.

Bravman

Q. And layer 51, that is a dummy gate?

A. Yes.

Q. Now claim 13 doesn't require layers 51 and 52, correct?

A. Correct.

Q. How does the resistor film 53 in figure 5 reduce capacitance?

A. As the patentee explains, by reducing the charge stored in the structure comprising elements 13, 12 and 53. The capacitance of the wire in its length, which extends beyond the isolation region, otherwise it wouldn't be a wire, as I said many times, is a contribution to reducing that capacitance, parasitic capacitance.

Q. Now we were talking about before how the capacitance is a material property of the device, correct?

A. Yes. We have been talking about that, and let me answer, please, but --

Q. I think you answered my question. I just asked you if we were talking about, and you said, yes, we had been talking about it.

A. Yes. We had been talking about it.

Q. So, just looking at the structure,

Bravman

how is it that the layer, the resistor film 53 reduces capacitance?

A. As the patent explains, by having the voltage drop between 13 and 53, which is a fraction of the total voltage drop, the charge stored in that region is reduced, which means that region's contribution to the parasitics of the wire 13 goes down.

Q. How is it that the resistor film 53 reduces capacitance between the wire 13 and the substrate?

A. Because the wire 13 extends outwardly, and as the patent explains, in this region with this configuration there is a supposition that the capacitance may not change or doesn't change. In his supposition, I think he is very clearly trying to build a structure or schematically build a structure here that comports with one of his two physics explanations of how to make a device faster.

One is by reducing the parasitic capacitance of wire substrate in this very region, which of course drops the parasitic effect of 13 as it extends and is part of the

Bravman

entire device, and/or he also explains that in this region one can reduce the charge stored on this capacitor, and that also increases the speed of the device potentially.

Q. Isn't it true that because the wire 13 and the high resistor film 53 separated by interlayer insulating film 12 acts as a capacitor in series with the second capacitor comprising high resistor film 53 and the substrate 1, that that is why you think the overall capacitance between the wire 13 and the substrate 1 decreases? Yes or no?

MR. CARTER: Objection to form.

A. I did not posit that. What I did posit was to you this morning --

Q. Okay. Thank you.

A. I would like to answer.

Q. You did. You said "I did not posit that."

A. That is not a total answer to your question, but it is on the record now.

Q. What structure are you comparing figure 5 with in order to determine if the capacitance was reduced?

Bravman

A. Well, this would be the same types of questions and answers I believe that we were talking about just before our lunch break that reading claim 13 in this instance, we have already agreed that the first five elements are the same, and neither party has posited that there is anything inventive there.

It is the final element, which in this case includes a resistor film, and it says where it is just like it said where the dielectric is within certain bounds, and the worker of skill understands that the teaching of the patent in light of the intrinsic record is to implement, create and place this resistor film where it says, and so if you are doing a comparison, you would compare, you know, with and without it to the purposes and actually not the purposes, but the assertions and the teachings of the patent.

Q. So are you comparing the figure 5 structure with a structure without layer 53, but everything else being the same?

A. Well, layer 53 with and without would certainly be a start. We know that this differs

Bravman

from the asserted prior art in other ways as well, in particular, the inclusion of 51 and 52, and a complete analysis of the effect on parasitic capacitance would of course have to include all those structures.

Q. What structure would you be comparing figure 5 with in order to determine whether layer 53 is a resistor film under Intel's proposed construction of resistor film?

A. Well, in this particular embodiment I believe it would be again in that thought experiment with and without 53. I mean that is what the patent is describing in this particular embodiment.

Q. Now, as you mentioned, 52 and 51 aren't required by the claim. Correct?

A. That's correct.

Q. Now assume that layers 52 and 51 -- well, actually there appears to be an insulating film of some material below 51, correct?

A. Yes.

Q. All right. I want you to assume that 52, 51 and that other insulating film that, instead of having those in that place, there is

Bravman

an insulating film formed of the same material as layer 12.

A. In place of 52, 51 and that thin oxide underneath?

Q. Yes.

A. Okay.

Q. In that structure, would layer 53 be an insulating film?

A. Insulating or resistive?

Q. Oh, I'm sorry. Thank you. In that structure, would layer 53 be a resistor film under Intel's construction?

A. Yeah, it meets the geometric requirements of the last element, and again we have talked a lot about the meaning of these elements in light of the whole patent, but it gives enough geometric information. Yes.

Q. Okay, and would its inclusion reduce the capacitance between the wire and the substrate, because the resistor film is a common plate between two capacitors in the series?

A. Well, we know in general two capacitors in a series, all things else being equal, you decrease the capacitance. Yes. That

Bravman

is just simple circuitry.

Q. Okay. So if you removed layer 53, it will reduce capacitance between the wire and the substrate, all else being equal?

MR. CARTER: Objection to form.

A. If I removed 53 --

Q. I'm sorry. Let me reask that question. I think it is backwards. If you remove layer 53, it would result in an increase in capacitance between the wire and the substrate, all else being equal. Is that right?

A. That would certainly be my first assumption just because as you say all things else being equal, 12 would be the same material. The distance between the wire 13 and the substrate would drop, and so I would expect an increase in capacitance.

Q. Now can you turn to paragraph 36 of your declaration.

A. Okay.

Q. So is that reduction in capacitance because of the second formula that you illustrate at the very bottom of page 11?

A. Yes. The capacitance of an in series

Bravman

set of capacitors is equal to the reciprocal of the sum of the reciprocals.

Q. Okay. So let's look at, go back to figure 5.

A. Okay.

Q. Let's just look at the portion -- I marked Exhibit 8 a blank piece of paper.

(Bravman Exhibit 8, Blank piece of paper, was so marked for identification, as of this date.)

Q. Before you start putting anything on the paper, so keeping in mind the assumption that layers 52, 51 and the underlying insulating film, they have been replaced with an insulating material of the same composition as layer 12.

A. Okay.

Q. And using the same assumptions you used when I think it was Exhibit 2 when you wrote out the formula, can you and let's call this everything like A prime. A prime, C prime.

A. Yes.

Q. What would be the capacitance in the leftmost region 9 between the wiring 13 and the substrate? And if you want to look at Exhibit 2

Bravman

just to remind yourself of the assumptions you made there as well, that's fine.

A. It was actually Exhibit 5.

Q. I'm sorry, you're right. Exhibit 5. Before you write down the next thing, what are you going to put in place of 52, 51 and the insulating material?

A. I am assuming 52 and 51 are replaced by 12.

Q. Oh, okay. You're going to call it 12. Do you want to call it 12 prime?

A. 12 prime is fine. So figure 5 also I believe includes this.

Q. Right, so that is part of number 12?

A. No. This region here.

Q. All right. Let's assume there is no -- what is that?

A. Implant region. It is a different --

Q. Assume there is no implant region as well.

A. No differing implant.

Q. Right. Just before you continue, does the inclusion or exclusion of the implant region affect whether claim 13 is infringed?

Bravman

A. No, it is speaking to another embodiment. So 53, 12, and I will state on the record I think we are both ignoring the very thin layer underneath the current 51?

Q. Right. We can include that thin layer as part of 12 prime, if you want.

A. Yeah. Right. 1 is the substrate.

Q. Right.

A. So these are in series. So you make use of this formula here, so in this thought experiment where you are looking just at this perfect little cube you have cut out, you're not worrying about anything else. So let's just call this C1 and C2. Is that okay?

Q. That's fine. They will be different exhibits. It is CA1 as well, so it is different.

A. Yeah. So C total.

Q. Yes.

A. Is given by the formula of 1 over 1 plus C1 plus 1 over C2 with assumptions as before. Okay.

Q. Do you want to say in Exhibit 5?

A. Exhibit 5.

Q. To make sure it is clear. Okay. Now

Bravman

obviously there are distances there for each of them. Is the area the same?

A. Well, I am doing this hypothetical assuming we have got this equal areas.

Q. Right. So the areas are going to be the same, and epsilon is going to be the same, because it is the same material, correct?

A. 12, yes.

Q. So let's say that the one distance for 12 is D1, and the other distance for 12 prime is D2. Okay?

A. Sure.

Q. With those assumptions, can you finish writing out the formula for C sub 1.

A. C total. So it is going to be epsilon 12, because that's relative.

Q. Okay. That's fine.

A. Then it is A over D, and so then it is C total equals epsilon naught epsilon 12. No, sorry. My bad. Let me turn the page over, or let me have another page, please. I will mark it page 2 of Exhibit 8.

Q. Yes. Can you simplify that.

A. You can take out in the reciprocals

Bravman

here, I don't want to do it in my head.

Q. Okay. Well, if A1 is equal to A2?

A. Yeah, I can certainly write A1 here.

Q. Okay.

A. And I can take A1 out.

Q. Yeah. So make that A1. If you want to rewrite it as a new line.

A. I can live with that. I wrote it right here.

Q. Okay. Now can you take a common denominator from that denominator? Sorry. A common factor from the denominator?

A. Yes. It would be epsilon naught epsilon 1, 2, A1.

Q. Can you pull that out front in the denominator. Okay. Now can you form a common denominator on that bracket in the bottom. So it's D1 times D2?

A. Yes. You have to change the numerator then.

Q. Right. Can you do that and show what that equals to in a more simplified form?

A. Is that what you wanted?

Q. Right. Okay. Then, with that

Bravman

understanding, can you show the entire equation again, but with the common denominator, the full common denominator out in the numerator? So it should be I think -- actually I think it should just be D1 plus D2.

A. I'm sorry.

Q. Wait a minute. That 1 over D1 plus 1 over D2 should also be under a 1 as well, right?

A. You are multiplying this by this. It is completely separate from that, right?

Q. Right, but the D1 and D2 are 1 over D1. Do you mind if I just -- you have a 1 on the top, and you have a 1 over top of this, but then this is also the same as 1 over 1 over 1 over D1, so there should be a 1 over top of that. 1 over D1 plus 1 over D2 should all be underneath the 1. Correct?

A. Yes. That's correct.

Q. So that should all be under 1.

A. Yes. Like that.

Q. Okay. So that is the same thing as D1 times D2 over D1 plus D2, correct?

A. Right. It reverses. That's correct.

Q. Can you write on the next page CT

equals that simplification.

A. So it is all going to be 1 over, and this is equal to, right, times that, so.

Q. Can you simplify that?

A. Well, since this is 1 over multiplies out, it inverted again, right?

Q. Yes.

MR. MIDDLETON: Let's just take a short break.

(Recess taken from 1:11 p.m. to 1:17 p.m.)

BY MR. MIDDLETON:

Q. I think there is a mistake on the second page. At the very bottom there where we put back in that 1?

A. Yes.

Q. When we did that, we did that improperly.

A. That's what I thought.

Q. Yeah. I think the 1 needs to be there, but you have to put 1 over 1 over D1 plus 1 over 1 over D2, because in the previous equation they were kept separately.

A. You are correct. That is why I was

Bravman

confused.

Q. Yes.

A. So --

Q. You can put an X through that and say it is a mistake.

A. This is correct though, right?

Q. No.

A. Okay. Sorry. So it is 1 over 1 over D1 plus 1 over 1 over D2.

Q. So that just becomes D1 plus D2, correct?

A. This?

Q. Yes.

A. Becomes what?

Q. D1 plus D2.

A. Yes. Of course.

Q. Right.

A. Yes.

Q. All right. So then what the equation really -- so that is a mistake too, because it is all based off of that.

A. Right. Okay.

Q. So what we have got is CT is equal to --

Bravman

A. This still comes out and over D1 plus D2, which makes sense, given the assumptions we made.

Q. Can you put a circle around the final CT just so that there is no confusion. There was a little bit of crossing out and so forth. Okay.

Now, in the structure in figure 5, if layers 51, 52 and that insulating layer below it were replaced with an insulating film with the same material as layer 12, if you remove layer 53, what would be the capacitance between the wiring and the substrate in region 9?

A. So if you assume the thickness of D3 since D1 and D2 are measured from the plate surfaces, you have to assume that the thickness of 53 was gone, and in that circumstance D1 and D2, it would be the same.

Q. So the capacitance wouldn't change, if you removed layer 53 from the structure in figure 5, correct?

A. If you collapse the structure, yes, by eliminating the thickness of 53.

Q. So when you say --

A. You basically have said you have got

Bravman

a capacitor with plate 13, plate 1 and a thickness of dielectric 12. I mean you just have rewritten it, so you get this intended result.

Q. The way I asked my question and the answer may have been confusing. Just so the record is clear, if you removed layer 53 from figure 5?

A. Yes.

Q. And under the assumption that 51 and 52 are insulating material the same as layer 12, then the removal of 53, would that affect the capacitance in region 9?

MR. CARTER: Objection to the form.

A. And that is why I was trying to understand. If 53 was left as a gap, the capacitance would not be the final capacitance on Exhibit 8, page 3. If I use the word "collapse," if the film 12 above the substrate took the place of without increasing its total thickness in 53, you would have a simple parallel plate capacitor with those two measurements added together, D1 plus D2. You've just broken up the dielectric into two regions.

Q. So if you remove 53 and don't put

Bravman

anything in its place, so there is a collapse, then the capacitance would be the same as what you show on page 3 of Exhibit 8, correct?

MR. CARTER: Objection to form.

A. Yeah, if I understand your question, if the whole thing just collapsed, you would just have a simple parallel plate capacitor, and assuming that D1 plus D2 were specified such that their sum is now the distance between the bottom of 13 and the top of 1, that is just the parallel plate formula.

MR. MIDDLETON: Thank you. I have no further questions.

MR. CARTER: Nothing from me.

(Time noted: 1:23 p.m.)

____

Dr. John Bravman

Subscribed and sworn to
before me this____day of______, 2018.

____

C E R T I F I C A T I O N

I, JOSEPH R. DANYO, a Shorthand Reporter and Notary Public, within and for the State of New York, do hereby certify:

That I reported the proceedings in the within entitled matter, and that the within transcript is a true record of such proceedings.

I further certify that I am not related, by blood or marriage, to any of the parties in this matter and that I am in no way interested in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand this 13th day of June, 2018.

____

JOSEPH R. DANYO

I N D E X

E X H I B I T S

~oOo~

ERRATA SHEET

Case Name:

Deposition Date:

Deponent:

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Signature of Deponent

SUBSCRIBED AND SWORN BEFORE ME

THIS ____ DAY OF __________, 2018.

____

(Notary Public) MY COMMISSION EXPIRES:__________