

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS
AMERICA, INC., AND SAMSUNG SEMICONDUCTOR, INC.
Petitioner

v.

TESSERA ADVANCED TECHNOLOGIES, INC.
Patent Owner

U.S. Patent No. 6,954,001

**PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 6,954,001**

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1018	H.H. Manko, <i>Solders and Soldering</i> (2001)
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I. INTRODUCTION

Samsung Electronics Co., Ltd, Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (collectively “Samsung”) request *inter partes* review (“IPR”) of Claims 1-18 of U.S. Patent No. 6,954,001 (“the ’001 Patent”; Ex-1001), assigned to Tessera Advanced Technologies, Inc. (“Patent Owner”).

The ’001 Patent claims a “semiconductor device” comprising four components: (1) “a semiconductor element,” (2) “a first electrode portion formed on the semiconductor element,” (3) “a second electrode portion formed on the semiconductor element,” and (4) “a diffusion layer formed between said first electrode portion and said second electrode portion.” Ex-1001, Claim 1. Claim 1 also requires that the diffusion layer comprise a combination of the metal components in the first and second electrode portions. *Id.* During prosecution, there was no dispute that the prior art disclosed a “semiconductor device” comprising a “semiconductor element” and a “first electrode portion.” Ex-1004, 118-123 (Office Action Response dated 2/14/05).¹ Rather the applicant disputed that the prior art disclosed a diffusion layer of a specified composition or the limitation of diffusion layer thickness added in Claim 10. *Id.* at 119-121. The

¹ All citations to Ex-1004 are to the repaginated page numbers applied to the File History by Samsung.

Examiner accepted Applicant's arguments and allowed the '001 Patent to issue.

Id., 126-132 (Notice of Allowance dated 4/8/05).

This Petition presents three non-cumulative grounds of invalidity based on four prior art references that the PTO did not consider during prosecution. Each ground relies on prior art references that disclose a semiconductor device having a semiconductor element and a diffusion layer as required by the '001 Patent. These grounds are each likely to prevail, and this Petition, accordingly, should be granted on all grounds, and the challenged claims should be cancelled. The petition is further supported by the Declaration of Dr. Miltiadis Hatalis, an expert in the subject matter claimed by the '001 Patent. *See, e.g.*, Ex-1002, ¶¶1-20; Ex-1003.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Samsung identifies the following real parties-in-interest: Samsung Electronics Co., Ltd, Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

Related Matters: Patent Owner has asserted that Samsung infringes the '001 Patent in two separate matters: (1) the Matter of *Certain Wafer-Level Packaging Semiconductor Devices And Products Containing Same (Including Cellular Phones, Tablets, Laptops, And Notebooks) And Components Thereof*, Inv. No. 337-TA-1080, USITC (2017); (2) *Tessera Advanced Technologies, Inc. v. Samsung Electronics America, Inc., and Samsung Electronics Co., Ltd.*, Civ. No.

2:17-cv-07621-JLL-JAD (D.N.J.) (both of which were filed on September 28, 2017, and served shortly thereafter). Patent owner has additionally asserted the '001 Patent against Broadcom Corporation in *Tessera, Inc. et al v. Broadcom Corp.*, Div. No. 1:16-cv-00380-LPS-CJB (D. Del.).

Broadcom filed a petition for *inter partes* review against the '001 Patent that was instituted as case IPR2017-01486. Samsung has challenged U.S. Patent No. 6,784,557, which is related to the '001 Patent in IPR2018-00466. Samsung has challenged the '001 Patent in another, simultaneously-filed petition.

Lead and Back-Up Counsel:

Pursuant to 37 C.F.R. § 42.8(b)(3), Samsung identifies the following lead and back-up counsel:

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Service Information: Samsung may be served at the addresses provided above for lead and back-up counsel. Samsung consents to electronic service at the address: TESSERASAMSUNGOMM@omm.com.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

In accordance with 37 C.F.R. § 42.103(a), the Office is authorized to charge an amount in the sum of \$23,000 to Deposit Account No. 50-2862 for the fee set forth in 37 C.F.R. § 42.15(a), and any additional fees that may be due.

IV. GROUNDS FOR STANDING

Pursuant to 37 C.F.R. § 42.104(a), Samsung certifies that the '001 Patent is available for *inter partes* review and that Samsung is not barred or otherwise estopped from requesting *inter partes* review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED

Samsung respectfully requests review of Claims 1-18 (the "Challenged

Claims”) of the ’001 Patent, and cancellation of these claims, based on the grounds listed below. *See, e.g.*, Ex-1002, Sections VII.B.16, VII.C.4, and VII.D.4.

- Ground 1: Claims 1-4, 6-8, 10-13, and 15-17 are obvious under 35 U.S.C. § 103 over Furuya in view of Takizawa;
- Ground 2: Claims 5 and 14 are obvious under 35 U.S.C. § 103 over Furuya in view of Takizawa and further in view of the knowledge of a POSA, as evidenced by Yaguchi; and
- Ground 3: Claims 9 and 18 are obvious under 35 U.S.C. § 103 over Furuya in view of Takizawa and further in view of the knowledge of a POSA, as evidenced by Nozawa.

Samsung notes that IPR2017-01486, filed by Broadcom, relied on Takizawa as the primary reference. By contrast, the instant petition relies on Furuya as the primary reference, along with Yaguchi and Nozawa for some grounds, none of which were considered in IPR2017-01486.

VI. OVERVIEW OF THE RELEVANT TECHNOLOGY²

The ’001 Patent specification provides an overview of the relevant technology. It explains that certain semiconductor devices, the pitch of the wiring

² This section is supported by Ex-1002, ¶¶24-36.

electrode is greater than that of the electrodes of the semiconductor element, and, as a result, metal wirings are formed to electrically connect these electrodes. Ex-1001, 1:23-39. Part of each metal wiring on the semiconductor element is used as an external electrode. *Id.*, 1:34-39. Figure 15A shows a perspective plan view of a semiconductor device where electrodes 2 are formed on the surface of the semiconductor element and connected by metal wirings 4 to ball electrodes 6. *Id.*, 1:43-67.

FIG. 15A
Prior Art

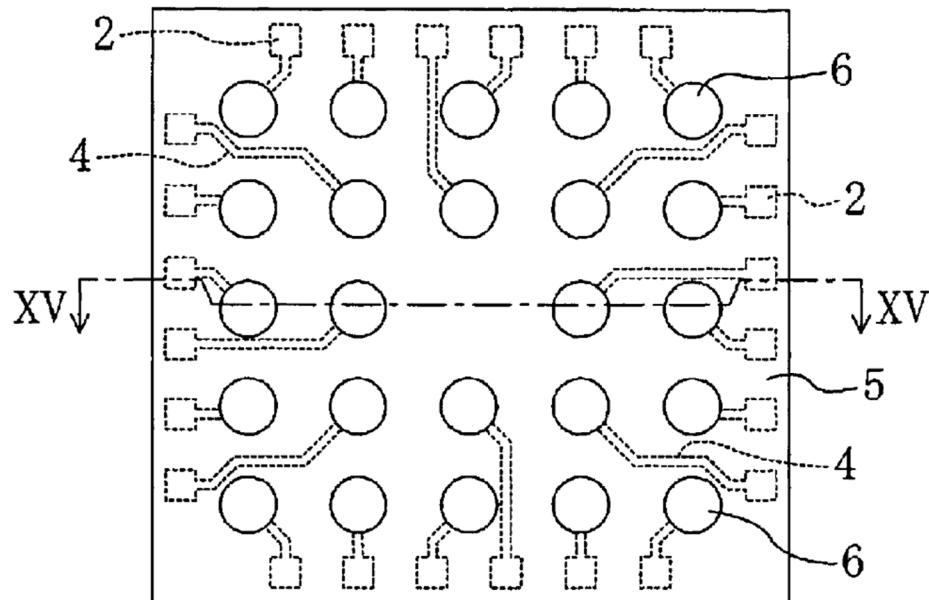


Figure 15B shows a cross-sectional view, shown in Figure 15A. Figure 15B shows that the electrodes formed on the surface of the semiconductor element are connected to a metal wiring, part of which forms an external electrode and is

connected to a ball electrode. *Id.*

FIG. 15B
Prior Art

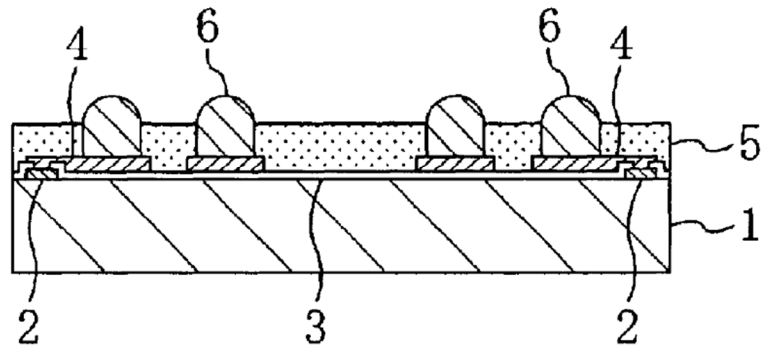
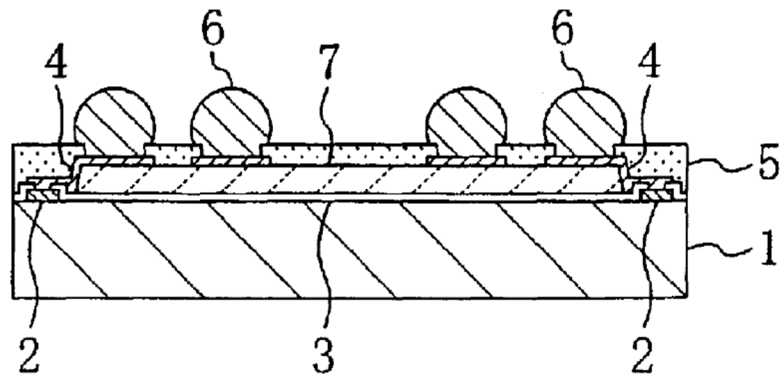


Figure 15C shows an insulating resin layer 7 is formed between the semiconductor element 1 and the metal wirings 4. *Id.*, 2:1-3.

FIG. 15C
Prior Art



The '001 Patent further explains that the metal wirings attached to the electrode are formed of copper (Cu), while the ball electrode is formed of solder containing tin (Sn). *Id.*, 2:4-9, 2:15-18. When the two are joined, a “metal junction of Cu (the metal wirings 4) and solder (the ball electrodes 6) is formed at the boundary between the metal wirings 4 and the ball electrode 6.” *Id.*, 2:9-14. The '001 Patent explains that it was well known in the prior art that this junction

was formed by bringing molten solder containing tin into contact with the metal, i.e., copper, of the external electrode portion. *Id.* 1:60-67.³ This results in a Sn-Cu alloy forming at the metal wiring portion of the semiconductor device. Ex-1001, 2:15-21. The '001 Patent states that this alloy layer is brittle and can be broken by stresses resulting from later processing (heating and cooling) of the semiconductor device. *Id.*, 2:22-32.

Relatedly, it was well-known to POSAs that 1) conventional solders comprise tin (Sn); 2) a Sn-Cu alloy is formed when molten tin comes into contact with a copper metal electrode; 3) the Sn-Cu alloy layer forms the “junction” or metallurgical bond that joins and electrically connects the semiconductor device to the substrate, e.g., PCB board; and 4) the Sn-Cu alloy is “weak and hard” and thus brittle and will perform better in certain thickness ranges. *See*, Ex-1002, ¶¶32-36. *See also*, e.g., Ex-1018, 68, 71; Ex-1019, 60, 398, 403, 405; Ex-1020, 42, 52-55, 60-61.

³ This text incorrectly cites reference number 3 as referring to the solder resist film and should instead cite to reference number 5. In context, this error would be apparent to a POSA. Ex-1002, ¶29, n.1.

VII. THE '001 PATENT⁴

A. The Patent Specification

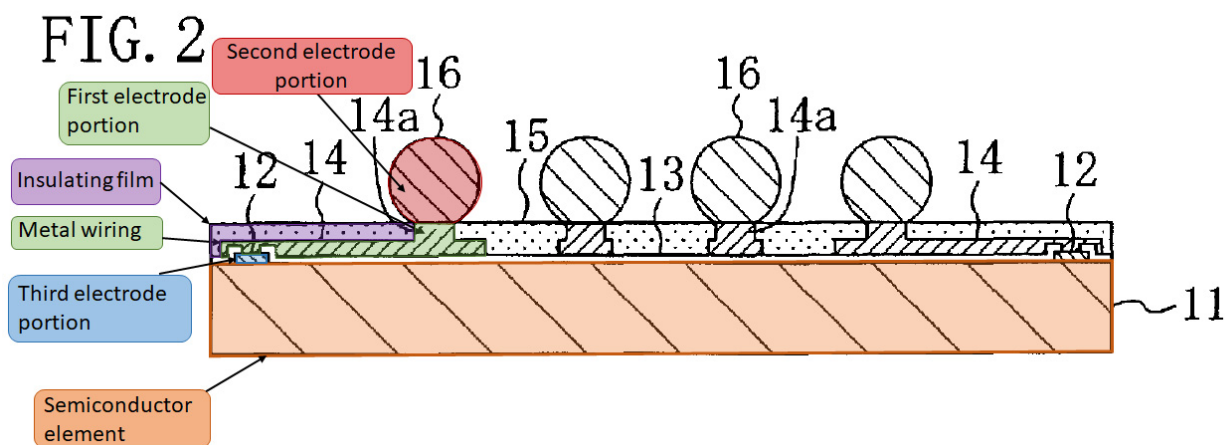
The '001 Patent, entitled “Semiconductor Device Including A Diffusion Layer,” was filed on August 17, 2004, issued on October 11, 2005, and claims priority as a division to U.S. Patent No. 6,784,557, filed December 2, 2002, which claims the benefit under § 119 to JP 2001-387051, filed in Japan on December 20, 2001.⁵ The '001 Patent relates to semiconductor devices built on a semiconductor chip and wired so as to connect with other semiconductor devices. The '001 Patent describes the purported invention as relating to “a semiconductor device in which a metal wiring is formed so as to be electrically connected to an electrode of a semiconductor element and a part of the metal wiring is used as an external

⁴ This section is supported by Ex-1002, ¶¶37-52.

⁵ Samsung reserves the right to argue that the '001 Patent is not entitled to a priority date based on the Japanese application because the '001 Patent claims a specific range of the total thickness of the first electrode portion combined with the diffusion layer. However, neither the Japanese application nor the disclosure of the parent '557 Patent discloses a combined thickness value of 10 μm to 20 μm for the diffusion layer and the first electrode portion. Because the prior art predates the foreign and U.S. filings, the Board need not reach this issue.

electrode.” Ex-1001, 1:9-13.

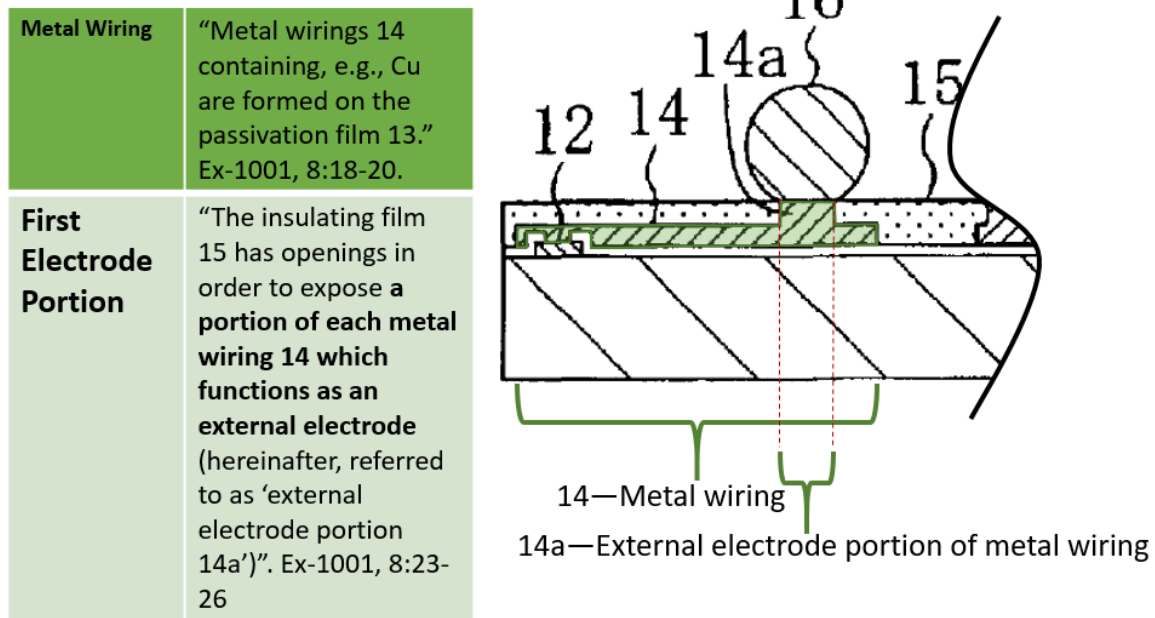
The '001 Patent describes a semiconductor device that includes a semiconductor element 11, an electrode 12, metal wiring 14 with a portion of the metal wiring that acts as an external electrode 14a, an insulating film 15, and an insulating resin layer 17 (not shown in the annotated Figure 1 below). Ex-1001, 11:50-67, Fig. 4. Ball electrodes 16 are mounted on the external electrodes and provide connection to a semiconductor substrate. Ex-1001, 11:67-12:10. As an example, Figure 2 is annotated below with labels corresponding to the language used in the '001 Patent's claims.



The '001 Patent discloses that it was known in the prior art that when the ball electrode is mounted, an alloy layer is formed between the external electrode portion and the ball electrode: “Sn contained in solder of the ball electrode diffuses into Cu contained in the metal wiring, whereby a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion.” Ex-

1001, 2:59-64. The claims of the '001 Patent refer to a “diffusion layer” that, though not shown in the annotated figure above, would be formed between the first and second electrode portion. According to the first embodiment, a semiconductor device includes additional elements and layers formed on a semiconductor element. Ex-1001, 8:13-15. The '001 Patent describes electrodes formed on the semiconductor element connected to metal wirings formed, for example, of copper. Ex-1001, 8:18-21. The metal wiring may have increased thickness at its terminal end (by adding a “metal-material embedded portion”) and the '001 Patent describes this portion of the wiring as being an “external electrode portion,” which is an example of a “first electrode portion.” Ex-1001, 8:21-55. The metal wiring and external electrode portion of the metal wiring are illustrated below in the enlarged, annotated portion of Figure 2.

FIG. 2



In one embodiment, the patent discloses, “the thickness of the external electrode portion 14a of the metal wiring 14 (e.g., the total thickness of the non-electrode portion of the metal wiring 14 and the metal-material embedded portion) is preferably in the range of 10 μm to 20 μm .” Ex-1001, 9:36-40. On top of the metal wiring, an insulating film is formed, leaving a hole over the external electrode portion of the metal wiring. Ex-1001, 8:21-27. The '001 Patent explains:

It is preferable that the exposed surface of the external electrode portion 14a is flush with or higher than the surface of the insulating film 15 (in the specification, the term “flush” also includes “approximately flush”)...The

reason for this is as follows: if the external electrode portion 14a is thinner than the insulating film 15, the ball electrode 16 cannot be mounted to the external electrode portion 14a (that is, the opening of the insulating film 15) without producing a gap therebetween. As a result, sufficient junction between the ball electrode 16 and the external electrode portion 14a cannot be ensured.

Ex-1001, 10:22-35.

Ball electrodes are formed from solder and connected to the external electrodes through the hole in the insulating film. Ex-1001, 8:28-38. When ball electrodes are mounted, tin in the solder “diffuses into Cu contained in the metal wiring,” which forms an alloy having low strength. Ex-1001, 8:63-9:1. However, according to the '001 Patent, the thickness of the external electrode portion is sufficient to prevent the alloy from growing through its entire thickness, preserving the strength of the metal wiring. Ex-1001, 9:1-12.

Another embodiment further includes an insulating resin layer on which the metal wirings are formed. Ex-1001, 11:45-58. The '001 Patent states:

[T]he insulating resin layer 17, which is formed from an epoxy resin having low elasticity or the like, is formed between the metal wirings 14 each electrically connected

to a corresponding one of the electrodes 12 of the semiconductor element 11 and the passivation film 13 formed over the surface of the semiconductor element 11.

Ex-1001, 12:17-22. The '001 Patent explains that the insulating resin absorbs stresses created when the temperature is varied to melt the ball electrodes when mounting the semiconductor device to the substrate, preventing breakage of the metal wiring. Ex-1001, 12:23-35. An example of the insulating resin and previously described features) is shown in the annotated Figure 5, below.

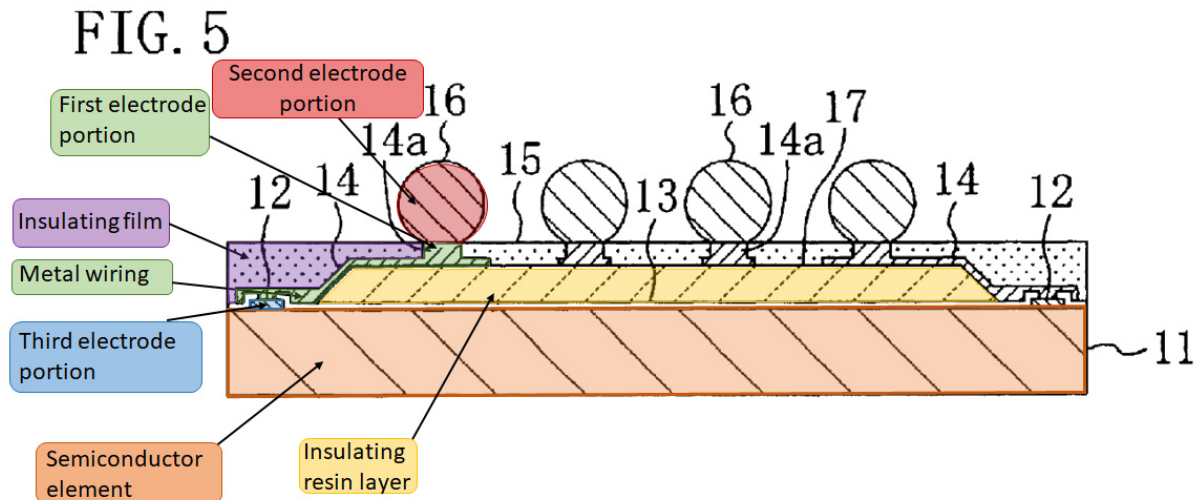
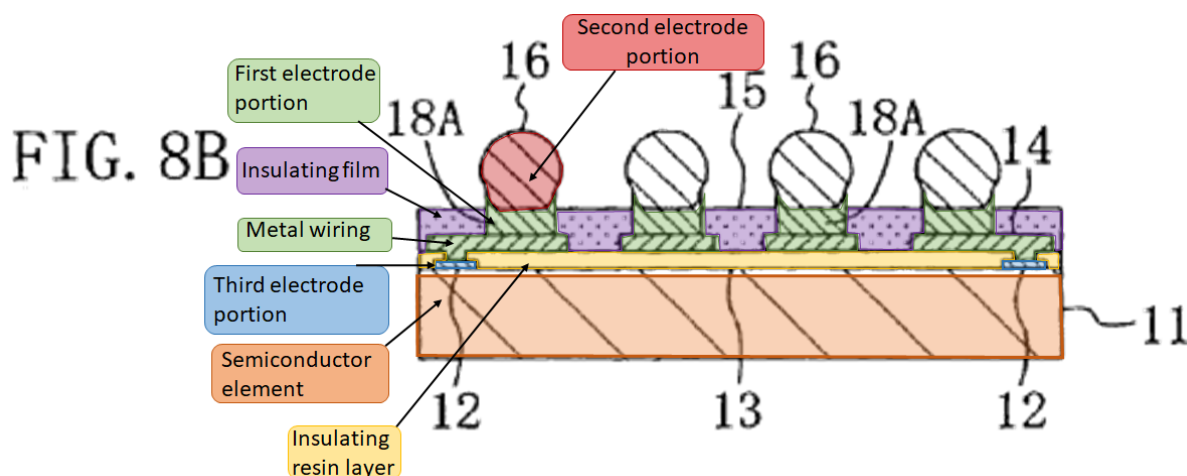


Figure 8B, annotated below, shows another embodiment described in the '001 Patent.



Here, many of the elements are the same as described above (and indicated by the same numerals). However, element 18A is described as a “metal material embedded portion ... (i.e., the external electrode portion of each metal wiring).”

B. Prosecution History

⁶ Throughout this petition all emphasis to quoted language has been added, unless otherwise noted.

10/919,402, as a divisional of the application that resulted in the '557 Patent, which was filed on December 2, 2002. Ex-1004, 1; Ex-1001, Cover. On November 16, 2004, the Examiner issued an Office Action rejecting all claims as being anticipated under 35 U.S.C. § 102 or rendered obvious under 35 U.S.C. § 103 by U.S. Pub. No. 2002/0108781 A1 ("Mune"). Ex-1004, 99-106. The Examiner found that Mune disclosed or rendered obvious a semiconductor device meeting all of the limitations claimed by the '001 Patent. *Id.*

In response, the applicant argued that Mune did not disclose the material comprising the first or second electrode portions or that any diffusion layer was formed between the first and second electrode portions. *Id.*, 119. The applicant further argued that the claims were patentable because, *inter alia*, the claimed range of thicknesses for the electrode portion and diffusion layer of 10 μm to 20 μm "has criticality and provides new and unexpected results at **both** the upper and lower limit thereof." *Id.*, 120 (emphasis in original). The applicant argued that electrodes with a thickness less than the lower thickness limit of 10 μm are susceptible to being disconnected, while those with a thickness greater than the upper thickness limit of 20 μm can lead to pattern deformation among other flaws. *Id.*, 120-122. On April 8, 2005, the Examiner issued a Notice of Allowance for all of the pending claims. *Id.*, 126-132.

VIII. LEGAL STANDARDS

A. Claim Construction

In the context of an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification in which they appear. 37 C.F.R. § 42.100(b); *see also* *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2134-35 (2016). Should institution be granted, the '001 Patent would not expire before a final written decision, and its claims should therefore be given their broadest reasonable interpretation.

Samsung notes that in IPR2017-01486, which also involved the '001 Patent, Patent Owner sought to construe “first electrode portion” to mean “‘external electrode portion’ or, alternatively, ‘portion of metal wiring that serves as an electrode, and that has greater thickness than the non-electrode portion of the metal wiring.’” Ex-1009, 7-9. Although the Board did not identify a construction for this term, in its institution decision the Board rejected Patent Owner’s constructions as incorrect:

Based on the current record and for purposes of institution, we determine that “first electrode portion” is not limited to an “external electrode portion” or a “portion of metal wiring that serves as an electrode, and that has a greater thickness than the non-electrode portion of the metal

wiring.”⁷

Id. Although the parties to that IPR also identified several additional terms for construction, the Board found that it did “not need to construe any other claim term or phrase to determine whether or not to institute *inter partes* review.” *Id.*, 8.

Similarly, for purposes of this proceeding, Samsung does not believe any term needs construction.⁸

B. Level Of Ordinary Skill In The Art

A person of ordinary skill in the art at the time of the alleged invention of

⁷ Although Samsung does not believe a construction of “first electrode portion” is required for purposes of this IPR, Samsung believes the PTAB correctly rejected Tessera’s proposed construction of “first electrode portion” as unduly limited. Patent Owner has now abandoned its proposed alternative construction in the concurrent ITC action, attached as Ex-1016. As discussed below, the grounds in the present petition invalidate the Challenged Claims under all constructions that have been proposed by Patent Owner.

⁸ Because the claim construction standard in this proceeding differs from the standard applicable in district court litigation, *see In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364, 1369 (Fed. Cir. 2004), Samsung expressly reserves the right to assert in litigation a different construction for any claim term in the ’001 Patent.

the '001 Patent ("POSA") would have had (i) a bachelor-level degree in mechanical engineering, materials science, electrical engineering, or a related field and 3–5 years of experience in the design/development of semiconductor packages; (ii) a Master's-level degree in mechanical engineering, materials science, electrical engineering, or a related field and 1–3 years of experience in the design/development of semiconductor packages; or (iii) a Ph.D.-level degree in mechanical engineering, materials science, electrical engineering, or a related field and some experience in the area of semiconductor packaging. Ex-1002, ¶¶21-23.

IX. OVERVIEW OF PRIOR ART⁹

A. Japanese Unexamined Patent Application Bulletin No. JP-2001-053184-A ("Furuya") (Ex. 1006)¹⁰

Furuya was published by the Japanese Patent Office on February 23, 2001, as Patent Application Publication No. 2001-53184 and was publicly available as of that date. Ex-1006, Cover. Furuya qualifies as prior art under § 102(a). In

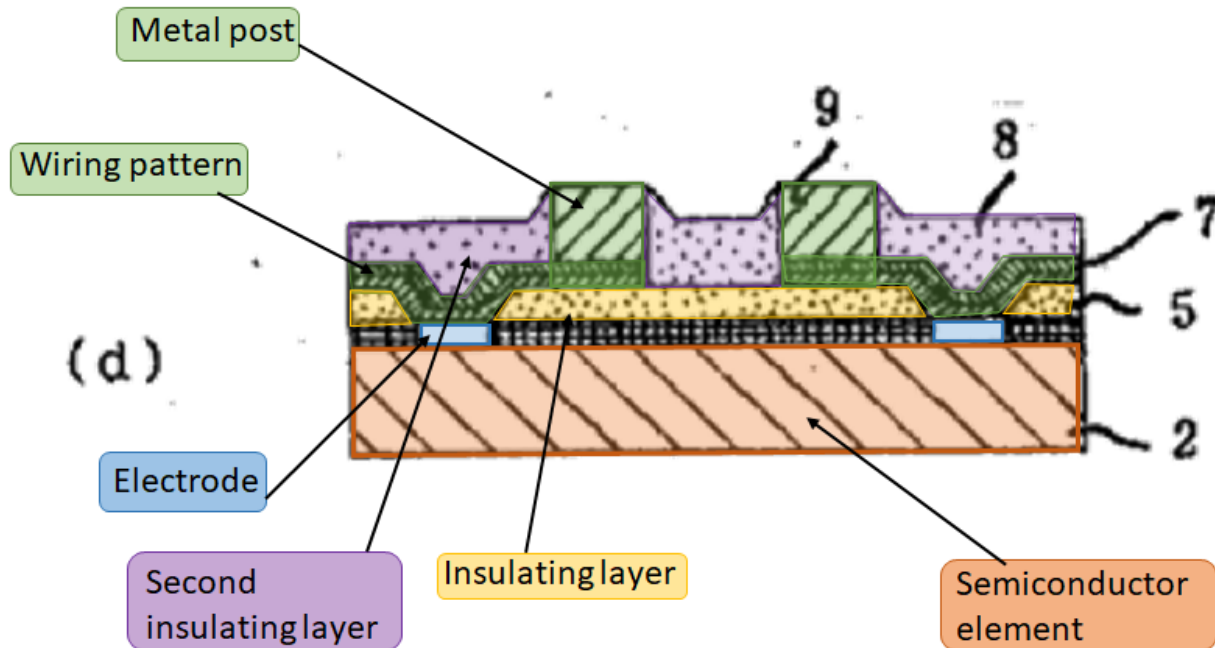
⁹ This section is supported by Ex-1002, ¶¶55-81.

¹⁰ Throughout this Petition, Samsung refers to the certified translation of Furuya. A copy of Furuya in the original Japanese is attached as Ex-1005. A declaration by the translator Martin Cross is also attached as Ex. 1013 certifying that Ex. 1006 is a true and correct translation of Ex. 1005.

addition, Furuya qualifies as a statutory bar under § 102(b) and pre-AIA 35 U.S.C. § 119(a) because Furuya was published more than a year before the '001 application for patent in the United States. Furuya was neither considered during the prosecution of the '001 Patent nor relied upon by Broadcom in IPR2017-01486.

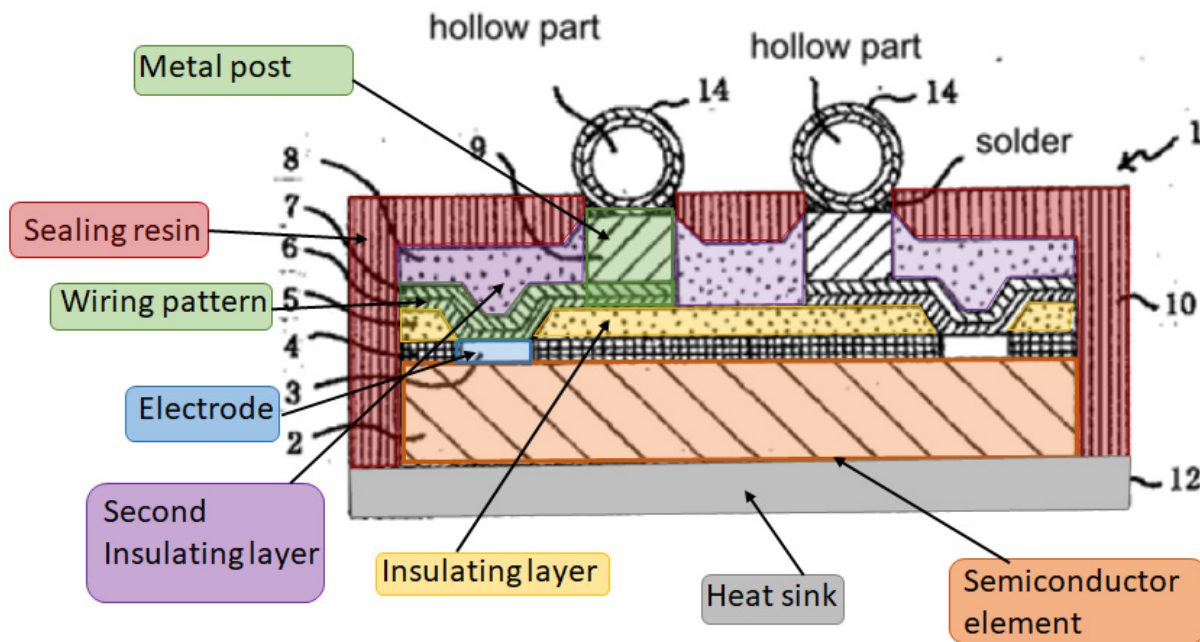
Furuya discloses a semiconductor device that includes an electrode that formed on a semiconductor element. Ex-1006, [0016]. A wiring pattern connects the electrode to a metal post for external connection. *Id.* Furuya also discloses an insulation layer formed on top of the wiring pattern that covers the side face of the metal post, but not the top surface. *Id.*

Furuya is directed to improving the connection strength between a metal post and a wiring pattern and improving the reliability of external connections. Ex-1006, [0015]. Furuya teaches accomplishing this objective by first forming electrodes on a semiconductor element, which are exposed by holes formed in a first insulating layer. Ex-1006 [0027]. Next, on the first insulating layer a wiring pattern is formed that connects the electrodes with metal posts, and a second insulating layer is formed on top so as to not cover the top surface of the metal posts. *Id.*, [0016]-[0017]. Figure 4(d), annotated below, illustrates these features.



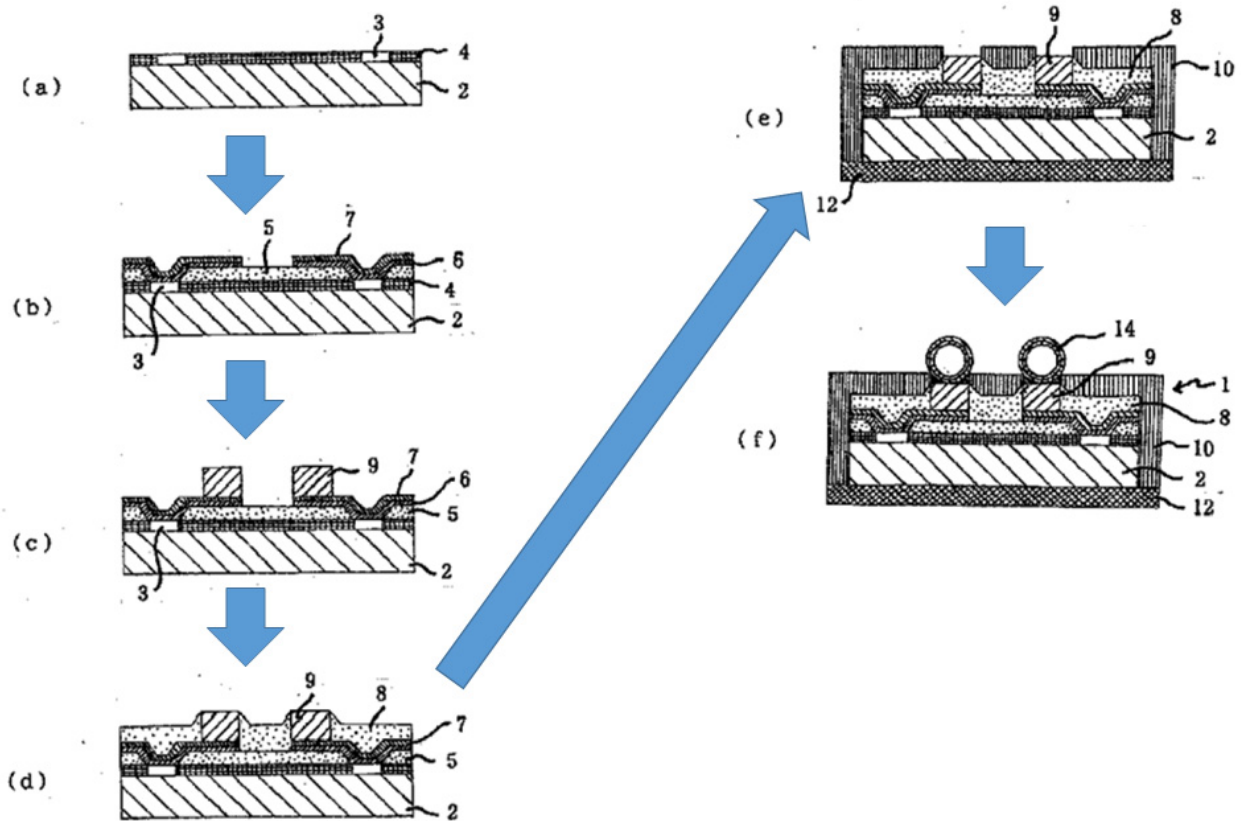
Furuya optimized the height of the second insulating layer 8 and the metal post 9 to enhance the connection strength between the metal post and the wiring pattern, thereby preventing disconnection. Ex-1006, [0028]-[0029]. Furuya explains that additional elements are added after dicing the wafer, such as a heatsink for improving heat dissipation and a sealing resin to protect the device from moisture absorption. Ex-1006, [0064]. Figure 1, annotated below, shows these features.

[FIG. 1]



Furuya describes each of the intermediate states in the manufacturing pathway to the final device. Ex-1006, [0051]-[0055]. These are shown in the progression of Figure 4(a)-(f), annotated below.

FIGURE 4



Furuya teaches that copper may be used for the material of the wiring pattern, in which case, “it is preferable to form a metal barrier layer 6 made of a TiW alloy...as an undercoat layer, and then form the wiring pattern 7 on the metal barrier layer 6.” Ex-1006, [0035]. Furuya teaches that the metal posts are formed on the wiring pattern and are also made of copper. Ex-1006, [0053].

Furuya discloses in one embodiment that “a 2000 Å [0.2 μm] thick TiN layer and a 5000 Å [0.5 μm] thick Cu layer were sequentially laminated on the first insulating layer 5 by sputtering” to produce the resulting metal barrier layer and wiring pattern discussed above. Ex-1006, [0052]. The metal posts are formed to a

height of 15 μm , in addition to the wiring layer on which they are formed. Ex-1006, [0053]. “[T]he second insulating layer 8 was given a film thickness of 10 μm , so as to be lower than the top face of the metal post 9.” *Id.*

When the metal post is joined to the solder ball by reflow, Furuya describes diffusion layer forming “if high temperatures of, for example, 180°C to 250°C are reached,” because “**some of the metal post 69 will dissolve and dissipate in the solder.**” Ex-1006, [0007]. A POSA would have understood that this dissolution of the metal post into the solder results in a diffusion layer. Although Furuya teaches this diffusion layer with respect to Figure 6, which is described as prior art, a POSA would have understood that the same principle would result in a diffusion layer forming between the external electrical connection 14 and the metal post 9 in Figure 1, considering that similar materials and techniques are used to connect the metal post and mounting board. Furuya, however, does not state the thickness of such a diffusion layer.

**B. Japanese Patent Application Publication No. 2000-260894,
published September 22, 2000 (“Takizawa”) (Ex. 1015)¹¹**

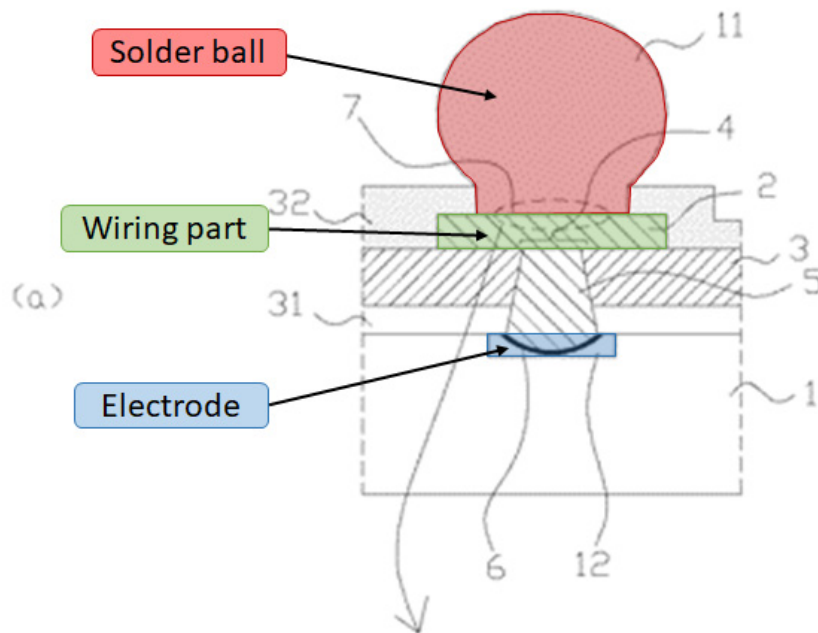
Takizawa was published by the Japanese Patent Office on September 22, 2000, as Patent Application No. H11-61912 and was publicly available as of that date. Ex. 1015, Cover. Takizawa qualifies as prior art under §102(b) as it was published more than a year before the earliest claimed priority date for the '001 Patent of December 20, 2001, and more than a year before the United States filing of the '001 Patent. Broadcom relied upon the German application corresponding to Takizawa in IPR2017-01486 as an anticipatory reference for claims 1-7, 9-16 and 18 and is attached as Ex-1017.

Takizawa discloses a semiconductor device with a semiconductor chip 1 that includes an electrode 12, where the electrode is connected to a solder ball 11 through a wiring part 2. Ex-1015, [0034] (“As illustrated in FIG. 1(a), the semiconductor device according to the present embodiment has the wiring part 2 containing Cu that is connected to a semiconductor chip 1 and the solder ball 11 containing Sn that is connected to the wiring part 2.”). Takizawa explains that the

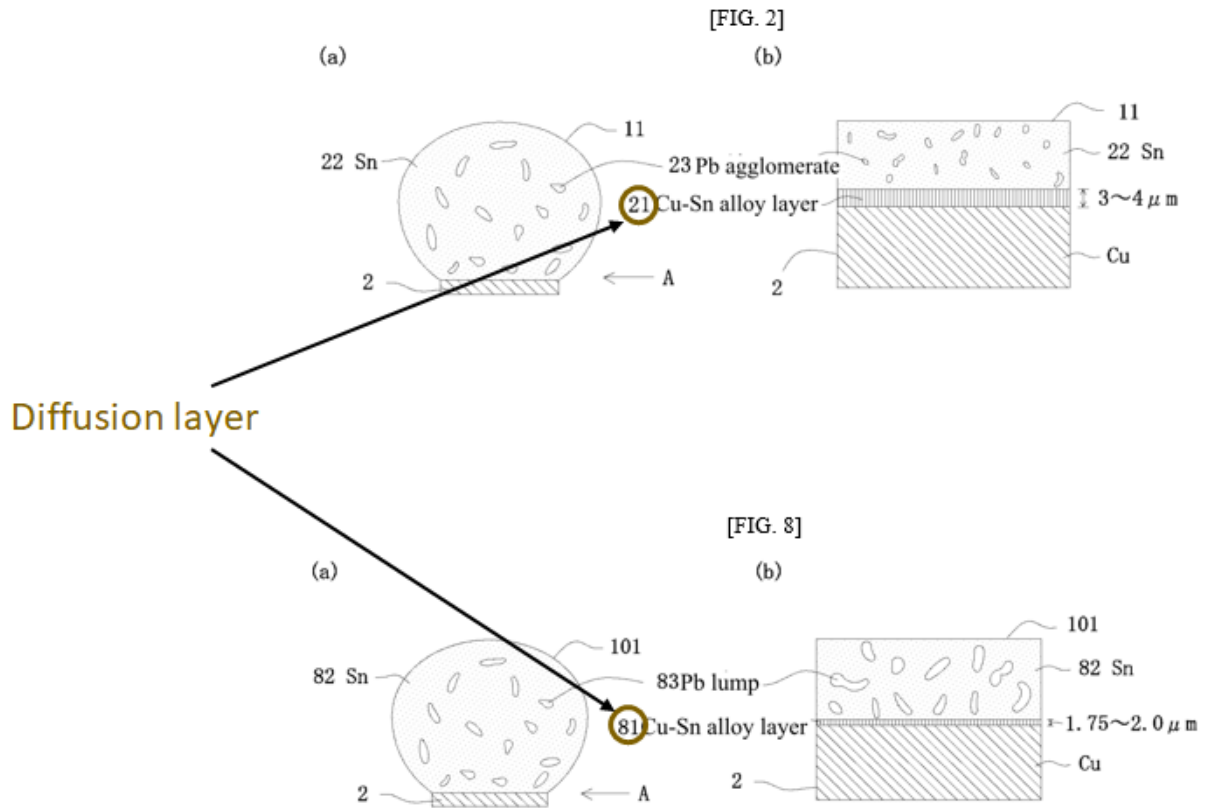
¹¹ Throughout this Petition, Samsung refers to the certified translation of Takizawa. A copy of Takizawa in the original Japanese is attached as Ex. 1014. A declaration by the translator, Dwaine Palmer, is attached as the first page of Ex. 1015.

wiring part 2 contains copper, while the solder ball contains tin. *Id.*, [0033]-[0035], [0040]-[0042]. Takizawa discloses that a variety of materials, including copper, can be paired with tin and used as a solder ball. *Id.* [0035], [0044]. Figure 1A, annotated below, shows these features as described in Takizawa.

[FIG. 1]



Takizawa also discloses a Sn-Cu alloy diffusion layer formed between its wiring part and solder ball. Ex-1015, [0020]; [0035]. Takizawa teaches an optimal diffusion layer is between 1.87 μm and 4 μm thick, which “prevent[s] detachment of the solder ball.” *Id.*, [0020], [0035], [0040]. Figs. 2B and 8B show the diffusion layer 21/81. Takizawa also discloses a method of manufacturing a semiconductor device with a stronger bond between the solder ball and the wiring part. *Id.*, [0019].



C. PCT Application Number PCT/JP00/01550, Publication Number WO00/55910 (“Yaguchi”) (Ex. 1011)¹²

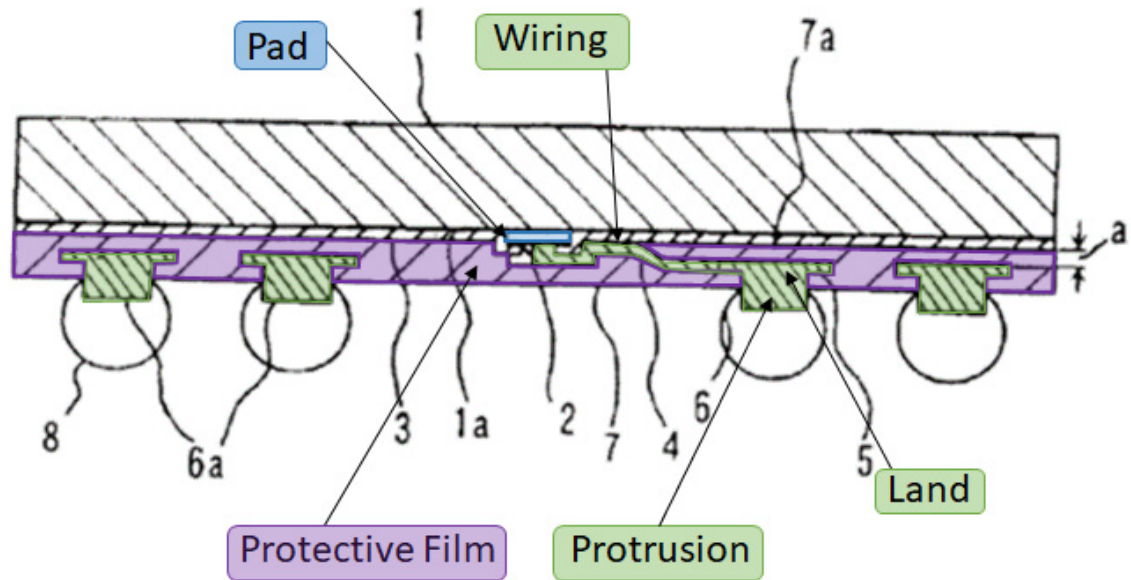
Yaguchi was filed on March 14, 2000, and published by the World

¹² Throughout this Petition, Samsung refers to the certified translation of Yaguchi. A copy of Yaguchi in the original Japanese is attached as Ex. 1010. A declaration by the translator Michael Fletcher is also attached as the first page of the translation certifying that Ex. 1011 is a true and correct translation of Ex. 1010.

Intellectual Property Organization on September 21, 2000, as PCT Publication No. WO00/55910 and was publicly available as of that date. Ex-1011, Cover. The U.S. counterpart to Yaguchi later issued as Patent No. 6,927,489. Yaguchi is prior art under § 102(a), (b), and (e). Yaguchi was neither considered during the prosecution of the '001 Patent, nor relied on by Broadcom in IPR2017-01486.

Yaguchi describes a semiconductor device that includes a semiconductor element, a pad, conductive wiring connected to a land, a protrusion provided on the land and an external terminal joined to the protrusion. Ex-1011, 9:5-19. Yaguchi explains that there are various passivation and insulation layers, including a protective film formed on the conductive wiring, land, and protrusions. *Id.* However, Yaguchi teaches that the protrusion is not completely covered by the protective film. Rather, “[a] part of the protrusion 6 protrudes through the protective film 7 and this protruding part 6a is bonded to the external terminal 8.” *Id.* Figure 1(a) illustrates semiconductor element 1, pad 2, conductive wiring line 4, land 5, protrusion 6, and protective film 7:

FIG. 1(a)



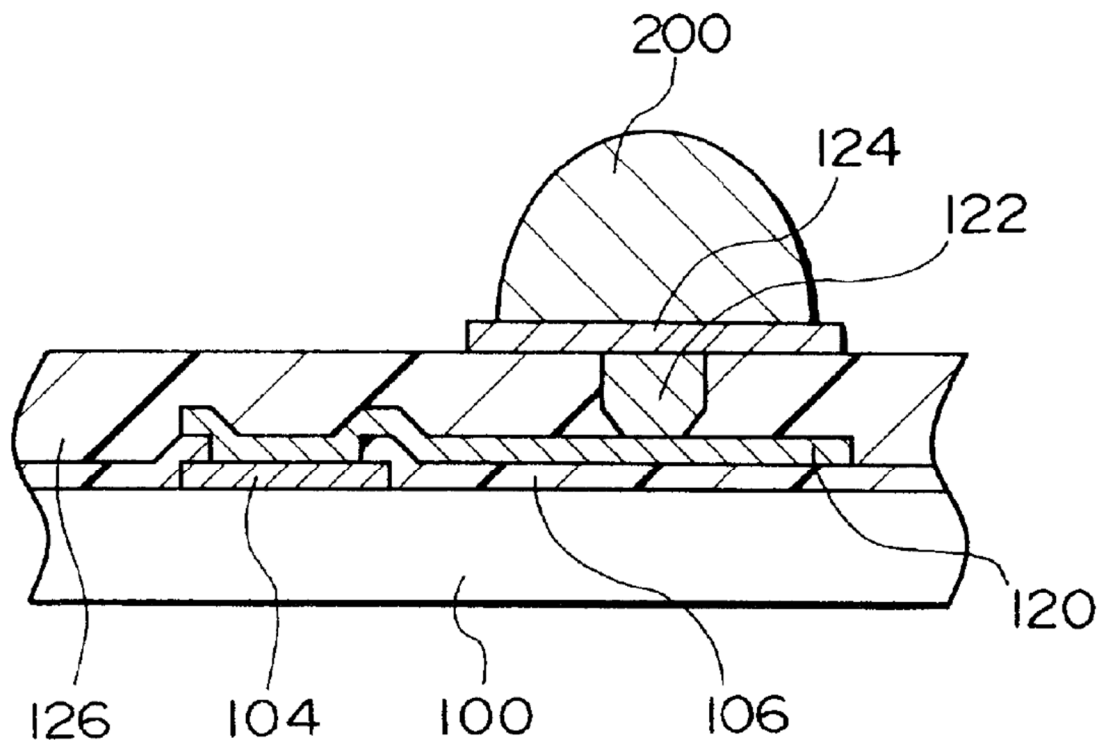
D. U.S. Patent No. 6,181,010 to Nozawa (“Nozawa”) (Ex. 1012)

Nozawa was filed on March 19, 1999, as PCT/JP99/01410 with a corresponding U.S. Application Number 09/424,484. Nozawa was first published by the World Intellectual Property Organization on October 7, 1999, as PCT Publication No. WO99/50907 and was publicly available as of that date. Ex-1012, Cover. Nozawa later issued as U.S. Patent No. 6,181,010 on January 30, 2001. Nozawa is prior art under § 102(a) and (e). Nozawa was neither considered during the prosecution of the '001 Patent, nor relied on by Broadcom in IPR2017-01486.

Nozawa describes a semiconductor device comprising a semiconductor chip 100 having electrodes 104 with an interconnect layer 120 connected to the

electrodes. Ex-1012, 1:51-56; 4:33-45. Nozawa further describes a conducting layer 122 formed on the interconnect layer, an underlying metal layer 124 formed on the conducting layer, a bump 200 formed on the underlying metal layer, and a resin layer 126, or insulating protection layer, formed around the conducting layer. Ex-1012, 1:56-64; 4:25-5:20. Nozawa teaches that its device allows for a reliable connection to be formed directly between the semiconductor device and the substrate resulting in electronic instruments that are more compact and lightweight. Ex-1012, 1:41-48. These features are illustrated in Nozawa's Figure 1. *Id.*, 4:33-45.

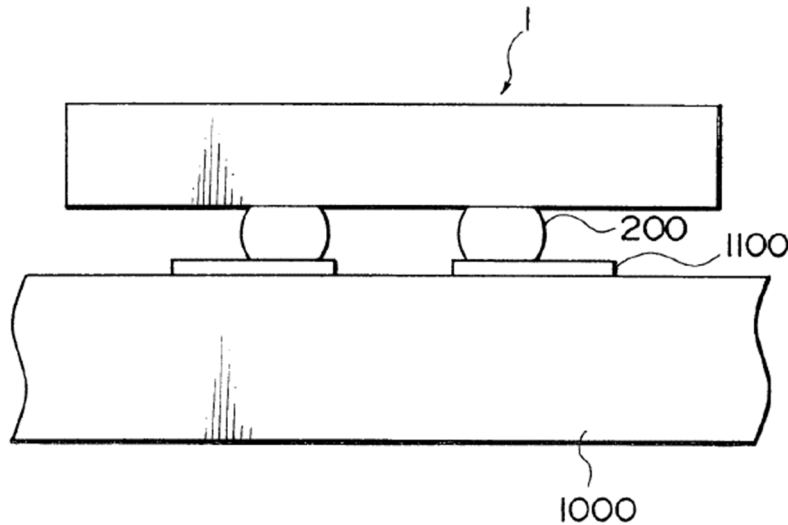
FIG. 1



Nozawa also teaches that the semiconductor device, described above, is connected to an electrode on the circuit board substrate.

Ex-1012, 8:30-44. Figure 9 below illustrates the connection between semiconductor device 1 and circuit board 1000.

FIG. 9



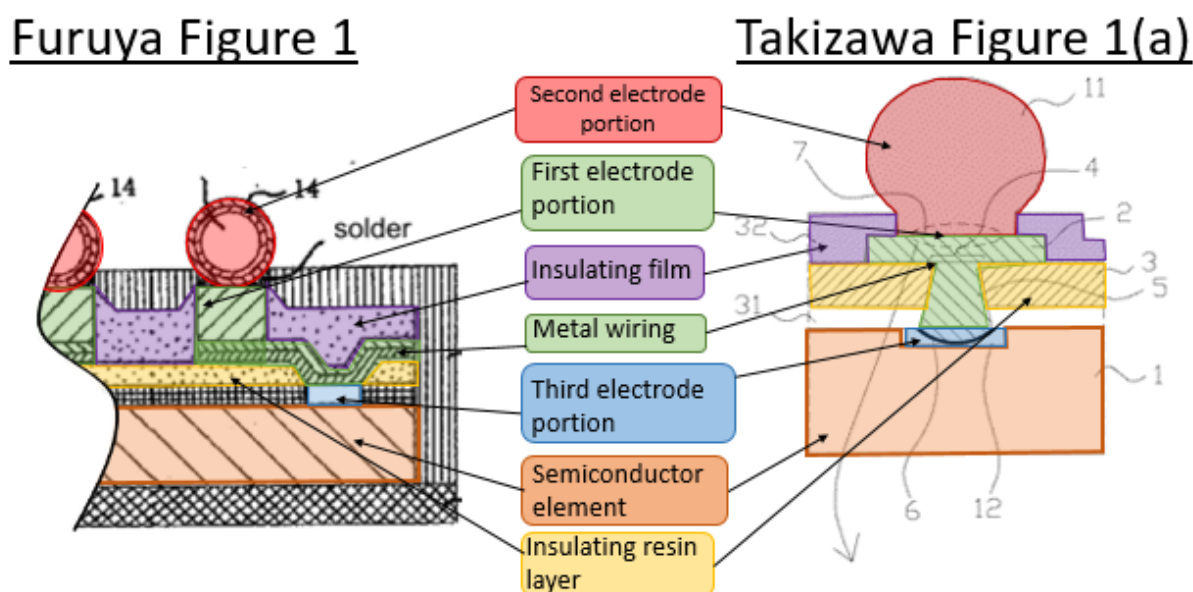
X. EXPLANATION OF GROUNDS FOR INVALIDITY

A. Ground 1: Furuya In View Of Takizawa Renders Obvious Challenged Claims 1-4, 6-8, 10-13, and 15-17

1. Reasons To Combine Furuya And Takizawa

A POSA would have been motivated to improve the semiconductor device disclosed in Furuya by incorporating Takizawa's teaching to improve the connection reliability between a solder ball and a metal wire by forming a copper-

tin diffusion layer between the wiring and the solder ball in the optimum thickness range of 1.87 μm to 4 μm . Ex-1002, ¶82. Both Furuya and Takizawa are in the same field of technology and were filed around the same time. *Id.* Furuya and Takizawa are directed toward very similar semiconductor devices that operate in a similar manner, as shown in the annotated figure below.¹³ Ex-1006, [Abstract]; Ex-1015, Abstract; Ex-1002, ¶83.



Furthermore, Furuya “is directed to providing a highly reliable chip-size

¹³ A POSA would have recognized that Takizawa and Furuya use different terminology to refer to elements that are the same. For ease of reference, the labels below are those used by the claims of the '001 Patent. Ex-1002, ¶83 n.6.

package type semiconductor device in which the connection strength between the metal post and the wiring pattern is high and the reliability of the electrical connection with the outside is high...” Ex-1006, [0015]. *See also, id.*, [0008]; Ex-1002, ¶84. Similarly, Takizawa’s invention “reduce[s] detachment of the solder ball caused by breaking or cracking in order to be able to reduce the occurrence of fractures and cracks near the bonding part by providing a wiring part containing copper connected to a semiconductor chip, and a solder ball containing tin bonded to the wiring part...[thereby] increase[ing] the reliability of the bonding part and increas[ing] the productivity of the semiconductor device.” Ex-1015, [0010]. *See also id.*, [0006]-[0009]; Ex-1002, ¶84.

Thus, both Furuya and Takizawa address the same problem of forming reliable electrical connections that can withstand the stress or strain on the semiconductor device due to differences in thermal expansion coefficients between the silicon material of the semiconductor device and the material on which the printed circuit board is made. Ex-1002, ¶85.

A POSA would have been motivated to combine Furuya with a reference such as Takizawa that teaches that reliability is improved by employing a diffusion layer of a specified thickness, i.e., between 1.87 μm and 4 μm thick. Ex-1002, ¶86. As discussed in Section IX.A, although Furuya discloses a diffusion layer (the formation of which was also well known to POSAs), it does not disclose the

optimal thickness—a known problem. Ex-1002, ¶86. *See also* Ex-1020 at 52-53; Ex-1002, ¶35. Takizawa examined the relationship between the thickness of the Cu-Sn alloy layer and the connection reliability of the resulting semiconductor device, finding that “[f]orming the Cu-Sn alloy layer with a thickness of at least 1.87 μm or more was preferable in order to prevent detachment of the solder ball 11.” Ex-1015[0040] (also finding that this thickness reduced fracturing and increased yield). Accordingly, combining the thicker alloy layer of Takizawa to the semiconductor of Fuyura would have been obvious to a POSA and would have led a POSA to conclude that the combination would yield a predictable and successful result. Ex-1002, ¶86.

2. Claim 1

- a. Furuya discloses “[a] semiconductor device, comprising” (1[pre])

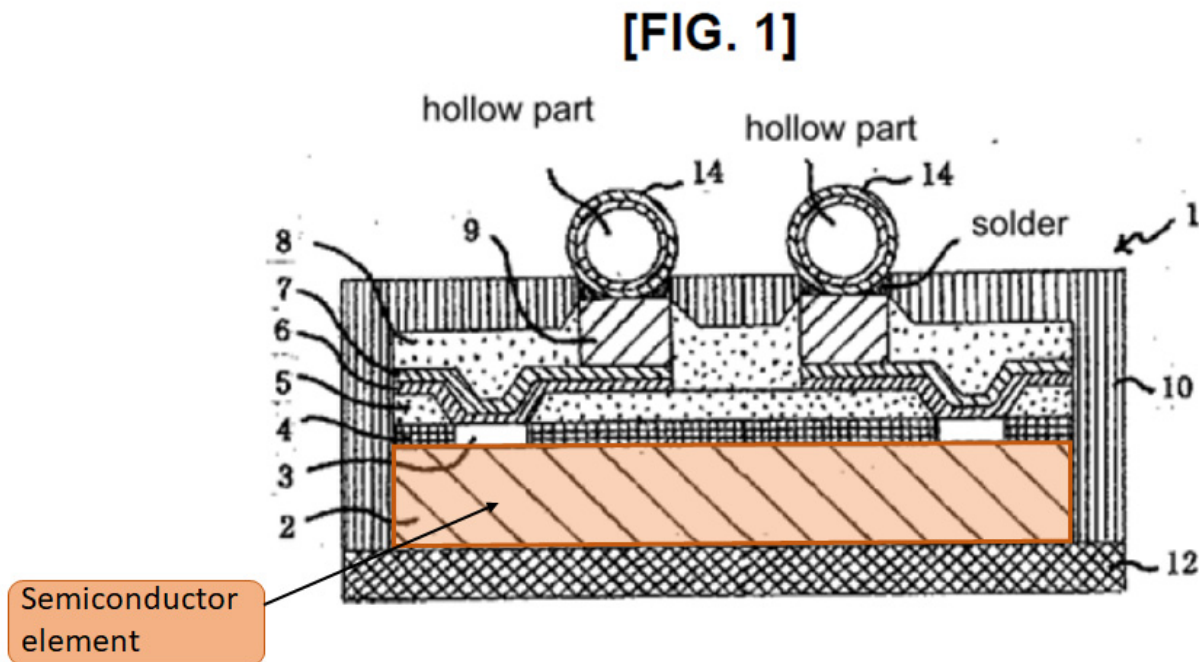
To the extent limiting, Furuya discloses the preamble because it “relates to [] **semiconductor devices** ... in which a wiring layer is formed on a semiconductor element.” Ex-1006, [0001]; Ex-1002, ¶87. The title of Furuya is “Semiconductor Device and Method of Manufacturing Same.” Ex-1006, Cover; *see also* Abstract (“[a] semiconductor device characterized in that”).

Thus, Furuya discloses each aspect of the preamble. Ex-1002, ¶88.

- b. Furuya discloses “a semiconductor element” (1[a])

Furuya discloses that a “semiconductor element” forms the base of the

semiconductor device on which other elements and layers are formed. Ex-1006, [0001], [0027]; Ex-1002, ¶89. For example, Furuya discloses that “the semiconductor device is characterized in that a first insulating layer...is formed on the passivation film, which has been formed **on a semiconductor element.**” Ex-1006, [0016]; Ex-1002, ¶89. *See also* Ex-1006, [0001], [0027], (“semiconductor element 2”), Fig. 1.



Furuya explains that the “semiconductor element 2 [is] produced by conventionally known means, which is incorporated into a semiconductor device 1 of the present invention.” Ex-1006, [0051]; Ex-1002, ¶90. *See also* Ex-1006, [0037] (“the semiconductor element 2 ... is formed of silicon or the like.”).

Thus, Furuya discloses each aspect of this limitation. Ex-1002, ¶91.

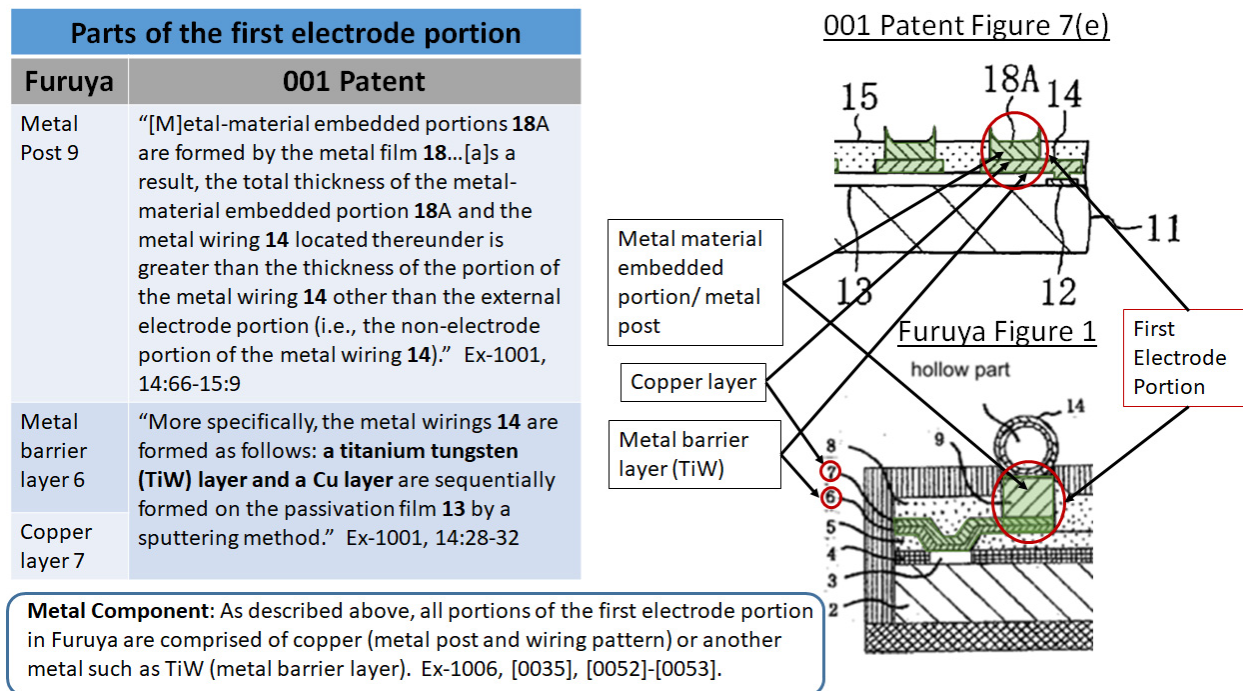
- c. Furuya discloses “a first electrode portion formed on the semiconductor element, said first electrode portion comprising a first metal component” (1[b])

Furuya teaches a first electrode portion comprising a metal post formed on top of a portion of the wiring pattern, which in turn is formed on top of a metal barrier layer. The metal post, wiring pattern, and metal barrier layer collectively act as the first electrode portion and serve to create external electrical connections. Ex-1006, [0052]-[0053]; Ex-1002, ¶92. Furuya describes the method for forming various layers on the semiconductor device that result in the claimed structure as follows:

[A] step of ... **forming a wiring pattern 7** having a predetermined shape, which is connected with the electrodes 3, on the first insulating layer 5, so as to produce [the] state in FIG. 4 (b); **a step of forming a metal post 9 for external connection, in a predetermined position of the wiring pattern 7**,... Note that, in the example in FIG. 4, prior to forming the wiring pattern 7, **the metal barrier layer 6 is formed as an undercoat layer.**

Ex-1006, [0046]; Ex-1002, ¶92. *See also* Ex-1006, [0052]-[0053]. The combination of three elements—the metal post, wiring pattern, and metal barrier layer—as the claimed “first electrode portion” parallels the discussion of this same

element in the '001 Patent as shown in the figure and citations below. Ex-1002, ¶¶93-95.



In IPR2017-01486, Patent Owner argued that Claim 1 was patentable over the prior art on the purported basis that: (1) the applied art failed to disclose or suggest the first electrode portion under its rejected construction; and (2) the wiring layer in the prior art was not formed on the semiconductor element. Neither argument can be credibly made as to the Furuya reference presented in the instant petition. As for argument (1), Patent Owner's flawed construction should be rejected as in the prior institution decision. Ex-1009, 7-9. Even if adopted, the thicknesses disclosed in Furuya meet this limitation. As for argument (2), the wiring pattern 7/metal barrier layer 6 are formed on electrode 3 of semiconductor

element 2 in the same manner as disclosed in the '001 Patent. Ex-1006, [0052]-[0053]; Ex-1002, ¶96.

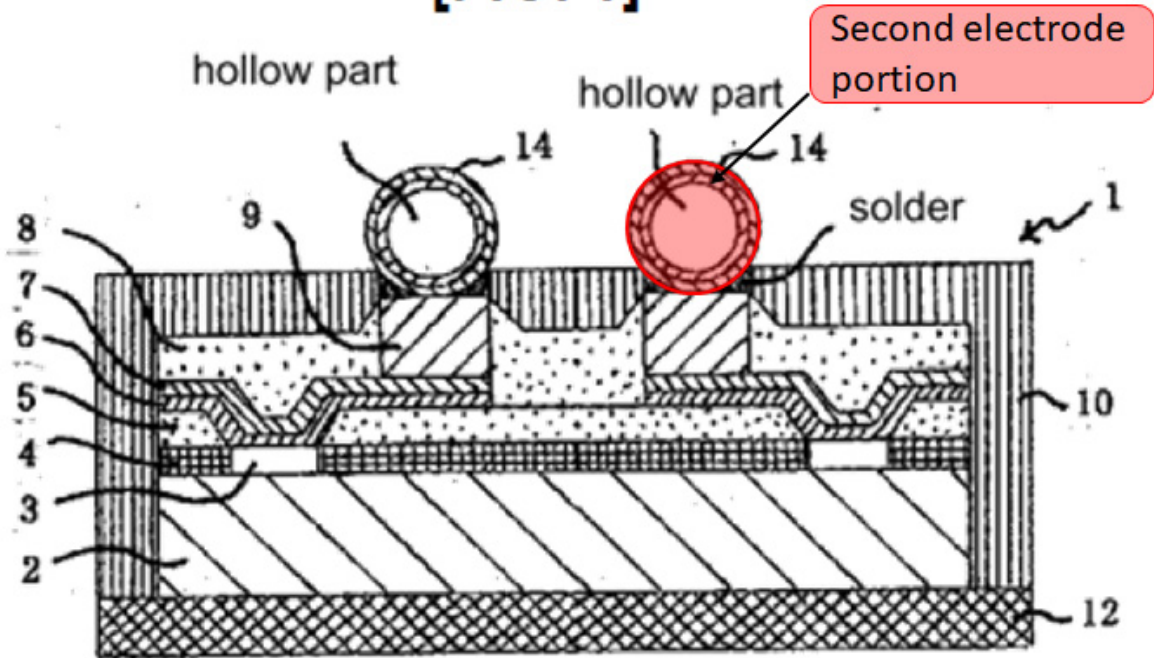
- d. Furuya and Takizawa both disclose “a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal component” (1[c])

Furuya discloses an external connection terminal (i.e., a second electrode portion) placed at the tip end of the metal post (i.e., the top of a first electrode portion), which external connection terminal is formed of a soldering metal component such as tin. Ex-1006, [0036]; Ex-1002, ¶97. For example, Furuya teaches:

[A] characteristic of the semiconductor device 1 of the present invention, as shown in FIG. 1, is that **an external connection terminal 14 that makes an external electrical connection** (for example, to a mounting board) is placed at the tip end of the metal post 9....

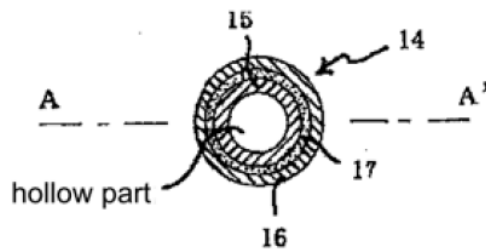
Ex-1006, [0036]. Figure 1, annotated below shows the external connection terminal 14. Ex-1002, ¶97.

[FIG. 1]



Furuya teaches that this external connection terminal (second electrode portion) is actually composed of multiple layers, as shown in Figure 2, below.

[FIG. 2]



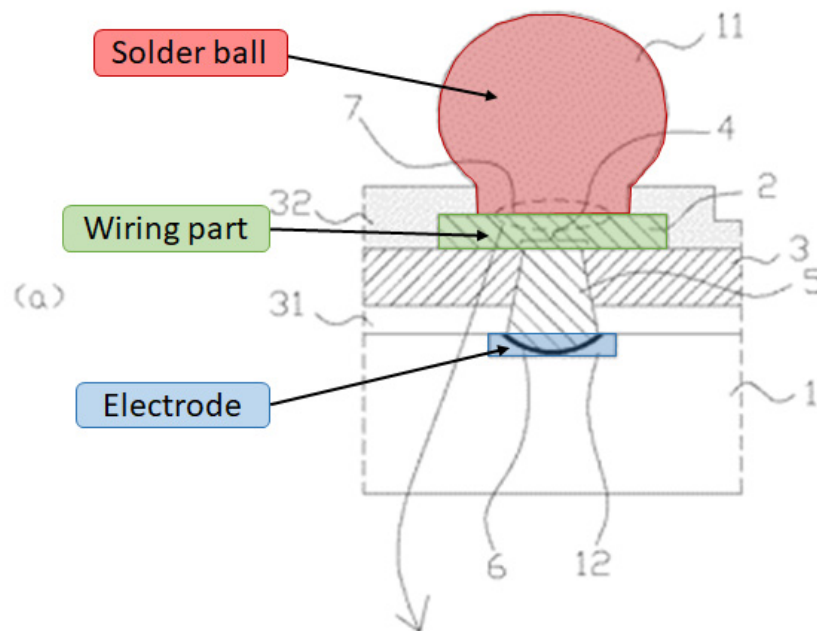
Furuya explains that the outer layer 16 is composed of an electroconductive material that “must perform fixation with the outside and allow for electrical connection with the outside.” Ex-1006 [0043]. Furuya also notes, with respect to

the prior art, that the second electrode portion may be a solder ball: “[I]f necessary, as shown in FIG. 6, a solder ball 71 or the like is sometimes formed as an external connection terminal 74 on the top face of the metal post 69.” *Id.*, [0006]. Ex-1002, ¶¶98-99.

One of the conductive materials Furuya discloses for use as solder is “a low melting point alloy having tin or lead as a principal component” and that use of tin as a principle component has several benefits. *Id.*, [0043]-[0044]. Thus, the second electrode portion is comprised of a second metal component that includes tin, which is different from the first metal component of the first electrode portion that includes copper. Ex-1002, ¶100.

Takizawa also discloses a second electrode portion comprising a second metal component because it employs a solder ball (i.e., second electrode portion) that comprises tin and is mounted on a copper wiring layer (i.e., first electrode portion). Ex-1015, [0003], [0009], [0019]-[0020], [0033]-[0035]; Ex-1002, ¶101. This is shown in Figure 1(a), annotated below. Ex-1002, ¶101. Moreover, “the material for solder ball 11...was Sn-Pb eutectic solder, but the material for the solder ball 11 is not restricted to this, and can be any material as long as the material **contains Sn.**” Ex-1015, [0044].

[FIG. 1]



Thus, Furuya and Takiwaza disclose each aspect of this limitation. Ex-1002, ¶102.

- e. Furuya and Takizawa both disclose “a diffusion layer formed between said first electrode portion and said second electrode portion,” (1[d])

Furuya discloses that when a connection is made between the metal post (i.e., first electrode portion) and mounting board using solder (i.e., second electrode portion), that some of the metal post will “dissolve and dissipate” into the solder, creating a diffusion layer. Ex-1006, [0007], Ex-1002, ¶103. For example, Furuya teaches:

In many cases, the connection between the metal post 69 and the outside (for example, the mounting board) is made

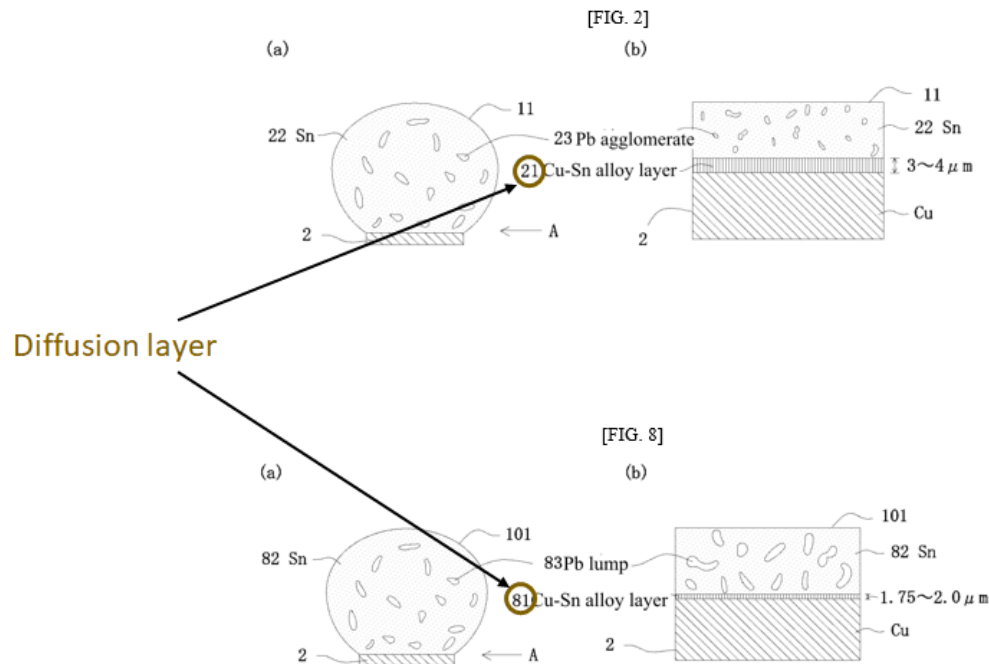
by thermocompression bonding using solder, but at this time, if high temperatures of, for example, 180°C to 250°C are reached, **some of the metal post 69 will dissolve and dissipate in the solder.**

Ex-1006, [0007]. A POSA would have understood that this dissolution of the metal post into the solder results in a diffusion layer. Ex-1002, ¶104. Although Furuya teaches this diffusion layer with respect to the prior art Figure 6, a POSA would have understood that the same principle results in a diffusion layer forming between the external electrical connection 14 and the metal post in Figure 1 as well, considering that similar materials and techniques are used to connect the metal post and mounting board. Ex-1002, ¶104. *See also*, Ex-1006, [0055]-[0056]. As described above in Section VI, and as discussed in the '001 Patent, a POSA would have known that a diffusion layer forms in these circumstances. Ex-1002, ¶104.

Takizawa also discloses a diffusion layer, formed between its wiring and solder ball. Ex-1002, ¶¶105-106. For example, Takizawa teaches:

As illustrated in FIG. 1(b), a strong Cu-Sn alloy layer is formed on the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 portion on which the solder ball 11 is placed on the wiring part 2.

Ex-1015, [0035]. This layer is formed by diffusion between the solder ball and the metal wiring. *See, id.*, [0034]. Annotated Figures 2B and 8B illustrate this diffusion layer. Ex-1002, ¶106.



Thus, Furuya and Takizawa disclose each aspect of this limitation. Ex-1002, ¶107.

- f. Furuya and Takizawa disclose “wherein said diffusion layer comprises said first metal component and said second metal component” (1[e])

As described above in claim elements [1b] and [1c], Furuya discloses a first metal component, i.e., copper, in the first electrode portion and a second metal component, i.e., tin, in the second electrode portion. Moreover, Furuya describes a soldering process in which a molted eutectic solder containing tin is in direct contact with a copper metal external electrode. Ex-1006, [0055]-[0056]. In view

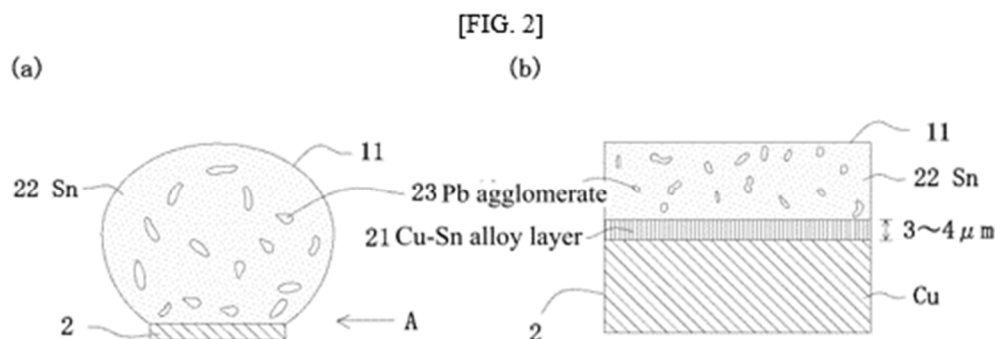
of the knowledge of a POSA, as confirmed by the '001 Patent, when **solder containing tin (Sn) is connected in a molten state to a copper electrode (Cu), the tin and copper form a Sn-Cu diffusion layer.** Ex-1001, 2:12-29; Ex-1002, ¶108. Therefore, a POSA would have recognized that Furuya discloses a process which results in a diffusion layer comprising both a first metal component and second metal component, i.e., copper and tin. Ex-1002, ¶108.

To the extent that the Board nevertheless finds Furuya's does not sufficiently disclose this limitation, a POSA would have been motivated to combine Furuya with Takizawa for the reasons discussed above to incorporate the composition of the diffusion layer disclosed in Takizawa. Ex-1002, ¶109.

As discussed with reference to claim element 1[d], Takizawa discloses a diffusion layer that forms between the first and second electrode portions. Takizawa further discloses that the diffusion layer comprises the first metal component (from the first electrode portion) and the second metal component (from the second electrode portion). Ex-1015, [0033]-[0034]; Ex-1002, ¶110. For example, Takizawa teaches that the wiring is comprised of copper (first metal component), while the solder ball is comprised of tin (second metal component). *See, e.g.*, Ex-1015, [0003], [0009], [0019]-[0020], [0033]-[0035], [0042], Figures 2, 8; Ex-1002, ¶110. Moreover, Takizawa teaches that a diffusion layer—"Cu-Sn alloy layer 21"—is "formed on the bonding part between the solder ball 11 and the

wiring part 2”. Ex-1015, [0035]. *See also id.*, [0003], [0009], [0033]-[0035].

These composition of the diffusion layer is shown in Figure 2, reproduced below, which shows the solder ball as Sn and the wiring part as Cu, while the diffusion layer is a Cu-Sn alloy. Ex-1002, ¶110-111.



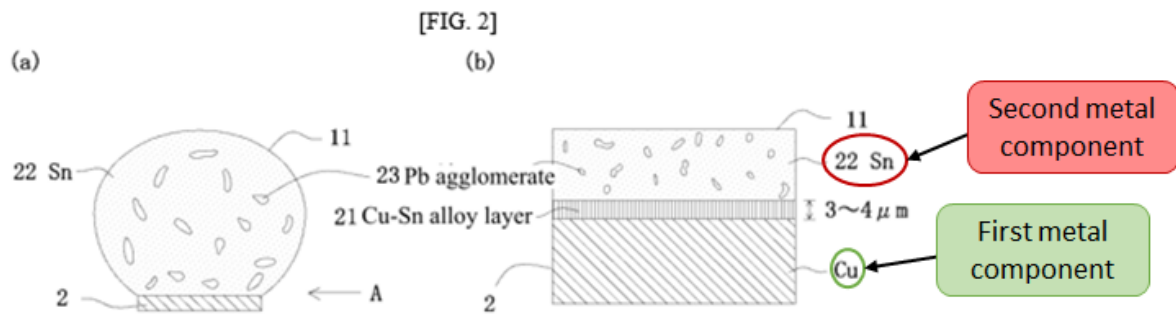
If this limitation requires all of the elements in the solder to be present in the diffusion layer, Takizawa teaches a tin-copper solder material. “[T]he material for the solder ball 11...can be any material **as long as the material contains Sn,...and Pb free solders or the like containing Ag, Cu, Zn, Cd, Ni, S, As, or Bi** can be used.” Ex-1015, [0044]. *See also id.*, [0035]. In this case, both the first metal component (copper) and the second metal component (tin-copper) would be present in the disclosed Cu-Sn diffusion layer. Ex-1002, ¶112. Thus, Takizawa also discloses each aspect of this limitation. Ex-1002, ¶113.

Accordingly, Furuya in view of Takizawa renders obvious Claim 1.

3. **Claim 2: “The semiconductor device of claim 1, wherein said first metal component includes copper and said second metal component includes tin”**

Furuya and Takizawa both disclose that the first metal component includes copper and the second metal component includes tin. For example, as described above with reference to limitation 1[b], Furuya teaches that the metal post and wiring layer of the first electrode portion both comprise copper. *See, e.g.*, Ex-1006, [0035] (“the material for the wiring pattern 7 is desirably a material with good conductivity and, **for example, copper**...can be used”); [0053] (“Next, metal posts 9 **made of copper** (height 15 μm) were formed on the wiring pattern 7...”). Furuya teaches that the second metal component that comprises the outer layer of the external connection may be “a low melting point alloy having tin or lead as a principal component.” Ex-1006, [0043]. *See also, id.*, [0042] (explaining that a solder alloy having tin or lead as a main component is preferable). Ex-1002, ¶114.

This element is also disclosed by Takizawa, where the first metal component includes copper and the second metal component includes tin. For example, “the wiring part 2 containing Cu that is connected to a semiconductor chip 1 and the solder ball 11 containing Sn that is connected to the wiring part 2.” Ex-1015, [0034]. Figure 2, annotated below, illustrates that the first metal component contains copper, while the second metal component contains tin. Ex-1002, ¶115. *See also*, Ex-1015, [0003], [0009], [0033]-[0035], [0042].



Thus, Furuya and Takizawa disclose each aspect of this limitation. Ex-1002, ¶116. Accordingly, Furuya in view of Takizawa renders obvious Claim 2.

4. **Claim 3: “The semiconductor device of claim 1, further comprising a third electrode portion formed on a surface of the semiconductor element and a metal wiring formed on the semiconductor element, said metal wiring electrically connecting the first electrode portion to the third electrode portion”**

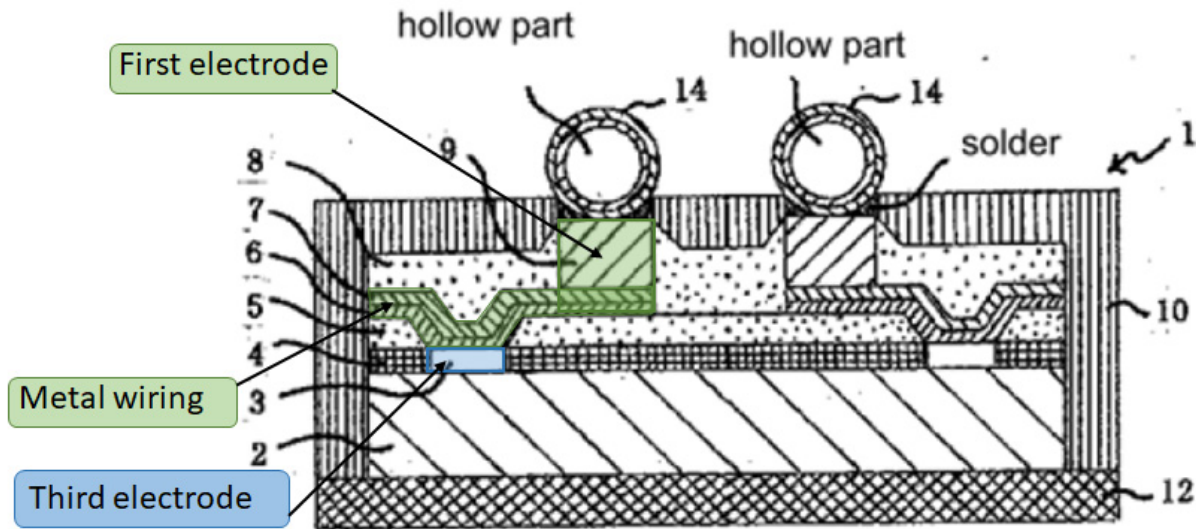
Furuya discloses a metal wiring that electrically connects an electrode (i.e. third electrode portion) on the surface of the semiconductor element to the metal post of the “first electrode portion.” For example, Furuya discloses a semiconductor device “with an electrode, which has been formed on the semiconductor element, exposed; a wiring pattern, which is connected with the electrode of the semiconductor element, is formed on the first insulating layer; a metal post for external connection is formed on the wiring pattern.” Ex-1006, [0016]; Ex-1002, ¶117. Furuya notes:

[A] first insulating layer 5, which has substantially the same shape as a passivation film 4, is formed on the

passivation film 4, **in a manner so as to expose electrodes 3, which have been formed on a semiconductor element 2. Then, a wiring pattern 7 (wiring layer) that is connected with the electrodes 3 is formed on the first insulating layer 5, and metal posts 9 for external connection, having a height of approximately 3 μm to 50 μm , are formed at predetermined positions on the wiring pattern 7.**

Ex-1006, [0027]. *See also* Ex-1006, [0051]-[0052], Fig. 4. Figure 1, annotated below, shows a third electrode portion (electrode 3) formed on a surface of the semiconductor element (element 2) and a metal wiring (wiring pattern 7) formed on the semiconductor element, said metal wiring electrically connecting the first electrode portion to the third electrode portion. Ex-1002, ¶117.

[FIG. 1]

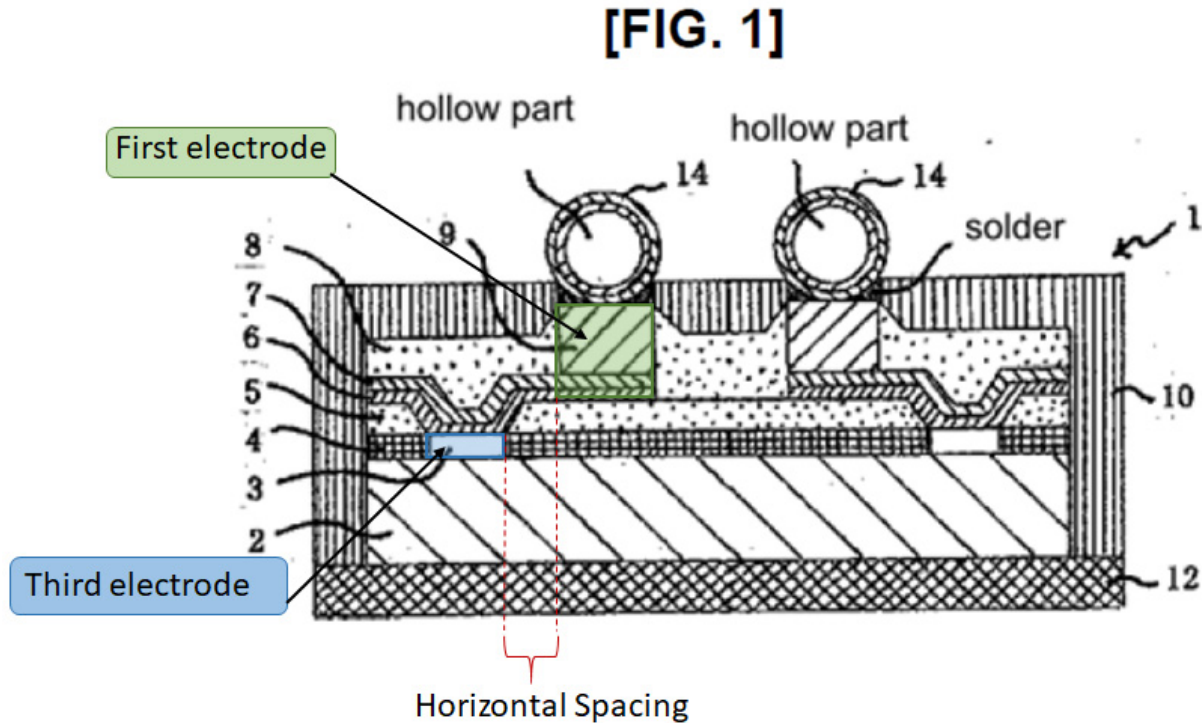


Moreover, Furuya discloses that “wiring pattern 7” is formed using electrically-conductive metal materials such as TiN and copper. Ex-1006, [0052] (“Next, a 2000 Å [0.2 μm] thick TiN layer and a 5000 Å [0.5 μm] thick Cu layer were sequentially laminated on the first insulating layer 5 by sputtering...to produce a wiring pattern 7.”). Thus, “wiring pattern 7” is a metal wiring formed on the semiconductor element that electrically connects the first electrode portion to the third electrode portion. Ex-1002, ¶118.

Thus, Furuya discloses the subject matter of Claim 3. Ex-1002, ¶119.
Accordingly, Furuya in view of Takizawa renders obvious Claim 3.

5. **Claim 4: “The semiconductor device of claim 3, wherein the first and third electrode portion are horizontally spaced apart with respect to the semiconductor element”**

Furuya teaches a semiconductor device where the first electrode portion and third electrode portion are horizontally spaced apart with respect to the semiconductor element. For example, Furuya discloses that the wiring pattern is formed on the third electrode, and the metal posts (a portion of the first electrode) are “formed **at predetermined positions on the wiring pattern 7.**” Ex-1006, [0027]; Ex-1002, ¶120. *See also* Ex-1006, [0053]. This description indicates that there is an intervening horizontal space between the two electrodes that is bridged by the wiring pattern, which electrically connects the two electrode portions. Ex-1002, ¶120. Figure 1, annotated below, confirms this horizontal spacing with respect to the semiconductor element. Ex-1002, ¶120.



Moreover, a POSA would have recognized that the depiction in Figure 1 as a redistribution structure and would expect some metal posts, i.e., first electrodes, to be separated from their corresponding third electrode(s) by significant distances. Ex-1002, ¶121. Thus, Furuya discloses the subject matter of Claim 4. *Id.*, ¶122. Accordingly, Furuya in view of Takizawa renders obvious Claim 4.

6. Claim 6: “The semiconductor device of claim 3, wherein the metal wiring includes copper”

Furuya discloses that both the metal posts and the wiring pattern include copper. Ex-1006, [0035]; Ex-1002, ¶123. Furuya teaches that “the material for the wiring pattern 7 is desirably a material with good conductivity and, **for example, copper**, silver, aluminum, alloys thereof, other metals that are good conductors or

the like can be used.” Ex-1006, [0035]. In one embodiment, Furuya discloses that “a 2000 Å [0.2 µm] thick TiN layer and a 5000 Å [0.5 µm] thick **Cu layer** were sequentially laminated on the first insulating layer 5 by sputtering” to form the metal wiring. *Id.*, [0052]. Similarly, Furuya teaches that the metal posts may also be made of copper: “Next, **metal posts 9 made of copper** (height 15 µm) were formed on the wiring pattern 7...” *Id.*, [0053].

Thus, Furuya discloses the subject matter of Claim 6. Ex-1002, ¶124.

Accordingly, Furuya in view of Takizawa renders obvious Claim 6.

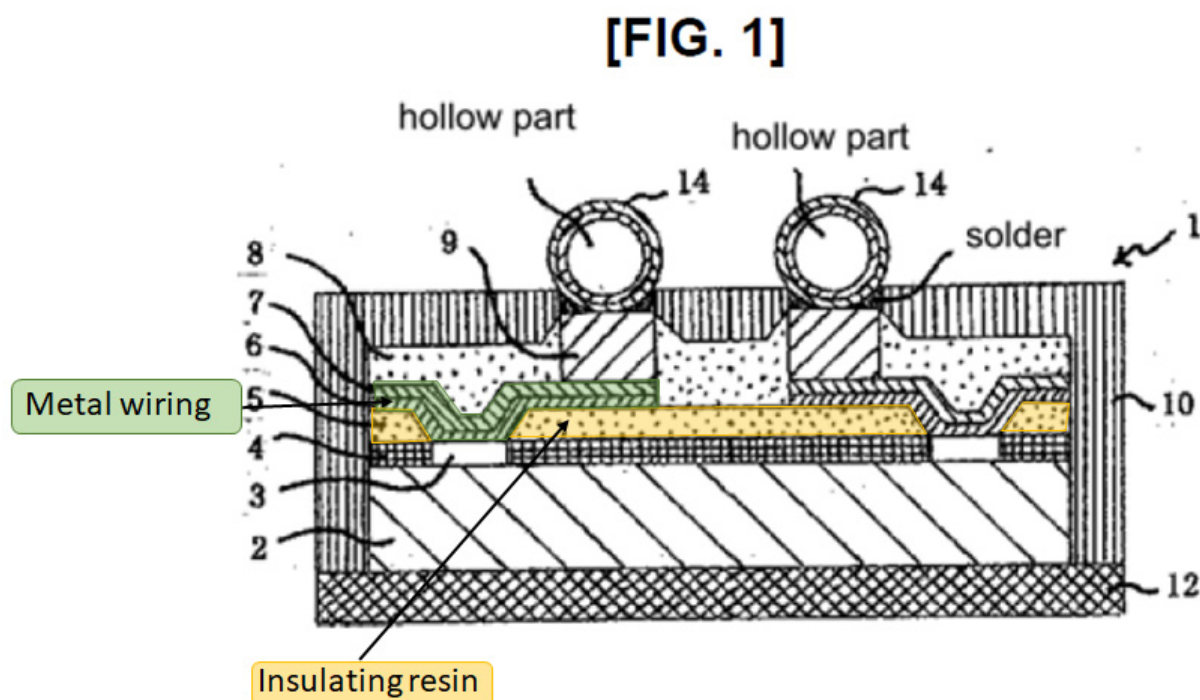
7. Claim 7

- a. Furuya discloses “[t]he semiconductor device of claim 3, further comprising an insulating resin layer formed between the surface of the semiconductor element and the metal wiring,”(7[a])

Furuya discloses a first insulating layer formed between the semiconductor element and the metal wiring. Ex-1006, [0046]; Ex-1002, ¶125. For example, Furuya teaches a method of manufacturing a semiconductor device including:

[A] step of forming a **first insulating layer 5**, which has substantially the same shape as a passivation film 4, **on a semiconductor element 2**, ...and then **forming a wiring pattern 7** having a predetermined shape, which is connected with the electrodes 3, **on the first insulating layer 5**, so as to produce [the] state in FIG. 4 (b)...

Ex-1006, [0046]. *See also*, Ex-1006, [0004], [0027], [0033], [0063]. This is shown in Figure 1, annotated below. Ex-1002, ¶125.



Furuya further discloses that “insulating layer 5” is formed of an insulating resin material. For example, Furuya discloses forming “insulating layer 5” using a photosensitive polyimide material, which Furuya describes as a type of resin material. *Id.*, [0021] (“an engineering plastic comprising a **resin selected from polyimide ...**”), [0052]; Ex-1002, ¶126.

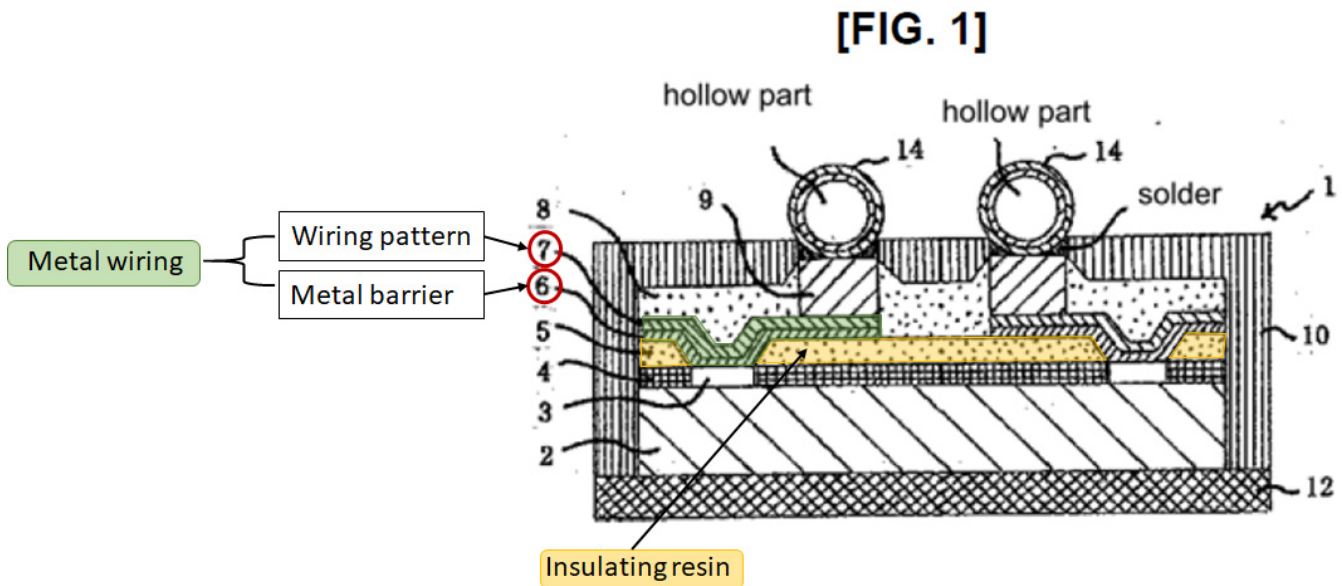
Thus, Furuya discloses each aspect of this limitation. Ex-1002, ¶127.

- b. Furuya discloses “wherein the metal wiring is formed along a surface of the insulating resin layer”(7[b])

Furuya discloses the first insulating layer discussed with reference to

element 7[a] is used as a surface along which the metal wiring is formed. Ex-1006, [0046]; Ex-1002, ¶128. For example, regarding the formation of the wiring pattern, Furuya teaches, “then forming a wiring pattern 7 having a predetermined shape, which is connected with the electrodes 3, on the first insulating layer 5, so as to produce state in FIG. 4 (b).” Ex-1006, [0046]. *See also* Ex-1006, [0004]. Although Furuya describes two separate layers, a wiring pattern and a metal barrier layer as being formed along the surface of the insulating resin layer, a POSA would view the combination of these two layers as corresponding to the “metal wiring” described in the ’001 Patent. Ex-1002, ¶128. For example, the ’001 Patent explains that “the metal wirings 14 are formed as follows: a titanium tungsten (TiW) layer and a Cu layer are sequentially formed on the passivation film 13 by a sputtering method.” Ex-1001, 14:28-32.

This formation of the metal wiring on the insulating resin layer is shown in Figure 1 where the wiring pattern is depicted as formed along the insulating resin layer. Ex-1002, ¶129.



Thus, Furuya discloses each aspect of this limitation. Accordingly, Furuya in view of Takizawa renders obvious Claim 7. Ex-1002, ¶130.

8. Claim 8: “The semiconductor device of claim 3, wherein the metal wiring has a thickness in the range of 0.01 μm to 8 μm ”

Furuya discloses this limitation because the wiring pattern combined with the metal barrier layer forms a metal wiring that has a thickness of 7,000 Å or 0.7 μm . Ex-1006, [0052]; Ex-1002, ¶131. In discussing the wiring layer, Furuya teaches: “Next, a 2000 Å [0.2 μm] thick TiN layer and a 5000 Å [0.5 μm] thick **Cu layer** were sequentially laminated on the first insulating layer 5 by sputtering.” Ex-1006, [0052]. As described above in Section X.A.7, the metal barrier layer

plus the wiring pattern meets the claimed “metal wiring” of the ’001 Patent.¹⁴

Compare Ex-1001, 14:25-31 *with* Ex-1006, [0035]. “When a patent claims a range, as in this case, that range is anticipated by a prior art reference if the reference discloses a point within the range.” *Ineos USA LLC v. Berry Plastics Corp.*, 783 F.3d 865, 869 (Fed. Cir. 2015). *See also Atofina v. Great Lakes Chem. Corp.*, 441 F.3d 991, 999 (Fed. Cir. 2006).

Thus, Furuya discloses the subject matter of Claim 8. Ex-1002, ¶132.

Accordingly, Furuya in view of Takizawa renders obvious Claim 8.

9. Claim 10

- a. Furuya discloses “[a] semiconductor device, comprising” (10[pre])

Furuya discloses this element as discussed in claim element 1[pre]. Ex-1002, ¶133.

¹⁴ Note that the ’001 Patent is clear that the metal wiring includes the first electrode portion, which is thicker than the 8 μm required by this claim. Ex-1001, 8:39-55. This petition maps Furuya to the disclosed embodiments of the ’001 Patent which include thinner non-electrode portions of the metal wiring falling within this claim range. Ex-1001, 9:25-35.

- b. Furuya discloses “a semiconductor element” (10[a])

Furuya discloses this element as discussed in claim element 1[a]. Ex-1002, ¶134.

- c. Furuya discloses “a first electrode portion formed on the semiconductor element, said first electrode portion comprising a first metal component” (10[b])

Furuya discloses this element as discussed in relation to claim element 1[b]. Ex-1002, ¶135.

- d. Furuya and Takizawa both disclose “a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal component” (10[c])

Furuya and Takizawa disclose this element as discussed in relation to claim element 1[c]. Ex-1002, ¶136.

- e. Furuya and Takizawa both disclose “a diffusion layer formed between said first electrode portion and said second electrode portion,” (10[d])

Furuya and Takizawa disclose this element as discussed in relation to claim element 1[d]. Ex-1002, ¶137.

- f. Takizawa discloses “wherein said diffusion layer comprises said first metal component and said second metal component” (10[e])

Takizawa discloses this element as discussed in relation to claim element 1[e]. Ex-1002, ¶138.

- g. Furuya in view of Takizawa discloses that “said first electrode portion and said diffusion layer have a combined thickness in the range of 10 μm to 20 $[\mu]\text{m}$ ” (10[f])

Furuya in view of Takizawa discloses this limitation because the thickness of the “first electrode portion” disclosed by Furuya plus the thickness of the diffusion layer taught by Takizawa is between 10 μm and 20 μm . Ex-1002, ¶139. As described above with reference to claim element 1[b], the first electrode portion in Furuya is formed by the combination of a portion of the metal barrier layer, a portion of the wiring pattern, and the metal post. Ex-1002, ¶139.

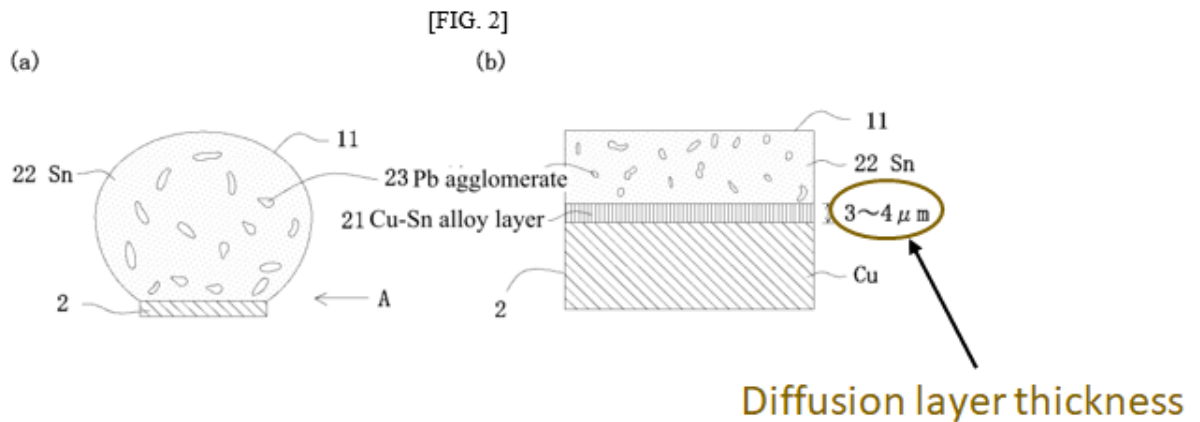
Furuya discloses that the metal post portion of the first electrode portion is 15 μm . Ex-1006, [0053]. As described with respect to Claim 8, the wire portion of the first electrode portion disclosed in Furuya is 0.7 μm thick. Ex-1006, [0052]. As a result, the entire thickness of the first electrode portion in Furuya is 15.7 μm . Ex-1002, ¶140. As discussed above with reference to claim element 1[d], Furuya discloses a diffusion layer that forms between the first electrode portion and the second electrode portion. However, Furuya does not disclose the thickness of the diffusion layer.

Takizawa also discloses a diffusion layer formed between the wire part and the solder ball, as described above with reference to claim element 1[d]. Takizawa further teaches advantages to a specific thickness of the diffusion layer. Ex-1002, ¶140. Takizawa states:

As shown in FIG. 2,...**1.87 to 4.0 μm of the Cu-Sn alloy layer was formed on each solder ball 11**, and in particular, many solder balls were formed with 3.0 to 4.0 μm of the Cu-Sn alloy layer...**Forming the Cu-Sn alloy layer with a thickness of at least 1.87 μm or more** was preferable in order to prevent detachment of the solder ball 11.

Ex-1015, [0040]. *See also id.*, [0009]-[0012], [0035], Figures 2, 8. Ex-1002, ¶140.

Figure 2, reproduced below, shows an exemplary diffusion layer thickness:



The combination of the optimized diffusion layer thickness of Takizawa with the thickness of the first electrode portion of Furuya yields a combined

thickness that falls within the 10 μm to 20 μm range as claim 10 requires.¹⁵ Ex-1002, ¶141. The diffusion layer will form partially into the first electrode portion and partly above the first electrode portion. Ex-1002, ¶141. However, taking the extreme case where the diffusion layer forms entirely above the first electrode portion, the maximum combined thickness would equal 19.7 μm (15.7 μm from the first electrode portion plus 4.0 μm from the diffusion layer). Ex-1002 ¶141. Taking the other extreme, where the diffusion layer is formed entirely into the first electrode portion, the minimum combined thickness would be 15.7 μm —the height of the first electrode portion. Ex-1002, ¶141. Thus, at most, the combined thickness would equal 19.7 μm while at a minimum the thickness would equal 15.7

¹⁵ A POSA combining Furuya and Takizawa would have recognized that the optimum diffusion layer thickness taught in Takizawa does not depend on using the first electrode portion thickness (18 μm) taught in Takizawa. Ex-1002, ¶141, n.8. Takizawa does not indicate that it optimized the first electrode portion thickness. Thus, it would have been natural for a POSA to keep the first electrode thickness taught in Furuya (15.7 μm) and only incorporate the diffusion layer thickness from Takizawa. Ex-1002, ¶141, n.8.

μm. Ex-1002, ¶141.^{16, 17} “When a patent claims a range, as in this case, that range is anticipated by a prior art reference if the reference discloses a point within the range.” *Ineos*, 783 F.3d at 869. *See also Atofina*, 441 F.3d at 999 (“an earlier species reference anticipates a later genus claim”). Thus, because Furuya in view of Takizawa discloses a thickness range that falls entirely within the claimed range of 10-20 μm, Furuya in view of Takizawa discloses each aspect of this limitation. *Id.*; Ex-1002, ¶141. Accordingly, Furuya in view of Takizawa renders obvious

¹⁶ The actual thickness range would likely be narrower than in this example because a portion of the diffusion layer would be created into the solder ball while the rest of its thickness would be created into the first electrode portion. Ex-1002, ¶141 n.9. However, even the extreme cases shown above fall entirely within the claimed range. *Id.*

¹⁷ Note that Figure 3 indicates that the thickness of the wiring part in Takizawa is 18 μm. Thus, Takizawa also discloses a thickness within the claim range (for example taking the 1.87 μm thickness disclosed by Takizawa as the minimum accepted thickness for achieving the purpose of the invention yields a total combined thickness of 19.7 μm assuming the diffusion layer is formed only above the wiring part). Ex-1002, ¶141 n.10.

Claim 10.

- 10. Claim 11: “The semiconductor device of claim 10, wherein said first metal component includes copper and said second metal component includes tin”**

Furuya in view of Takizawa disclose this claim for the same reasons discussed in relation to Claim 2. Ex-1002, ¶142. Accordingly, Furuya in view of Takizawa renders obvious Claim 11.

- 11. Claim 12: “The semiconductor device of claim 10, further comprising a third electrode portion formed on a surface of the semiconductor element and a metal wiring formed on the semiconductor element, said metal wiring electrically connecting the first electrode portion to the third electrode portion”**

Furuya discloses this claim as discussed in relation to Claim 3. Ex-1002, ¶143. Accordingly, Furuya in view of Takizawa renders obvious Claim 12.

- 12. Claim 13: “The semiconductor device of claim 12, wherein the first electrode portion and the third electrode portion are horizontally spaced apart with respect to the semiconductor element.”**

Furuya discloses this element as discussed in relation to Claim 4. Ex-1002, ¶144. Accordingly, Furuya in view of Takizawa renders obvious Claim 13.

- 13. Claim 15: “The semiconductor device of claim 12, wherein the metal wiring includes copper”**

Furuya discloses this claim as discussed in relation to Claim 6. Ex-1002, ¶145. Accordingly, Furuya in view of Takizawa renders obvious Claim 15.

14. Claim 16

- a. Furuya discloses “[t]he semiconductor device of claim 12, further comprising an insulating resin layer formed between the surface of the semiconductor element and the metal wiring”(16[a])

Furuya discloses this element as discussed in relation to claim element 7[a].

Ex-1002, ¶146.

- b. Furuya discloses “wherein the metal wiring is formed along a surface of the insulating resin layer”(16[b])

Furuya discloses this element as discussed in relation to claim element 7[b].

Ex-1002, ¶147. Accordingly, Furuya in view of Takizawa renders obvious Claim 16.

15. Claim 17: “The semiconductor device of claim 12, wherein the metal wiring has a thickness in the range of 0.01 μm to 8 μm ”

Furuya discloses this claim as discussed in relation to Claim 8. Ex-1002, ¶148. Accordingly, Furuya in view of Takizawa renders obvious Claim 17.

B. Ground 2: Furuya In View Of Takizawa And Further In View Of The Knowledge Of A POSA (as evidenced by Yaguchi) Renders Obvious Challenged Claims 5 and 14¹⁸

1. Reasons To Combine Furuya And Takizawa With Yaguchi

A POSA would have been motivated to combine Furuya and Takizawa for the reasons above in relation to Ground 1. A POSA would have been motivated to further combine these references with Yaguchi for the reasons described below. Ex-1002, ¶149.

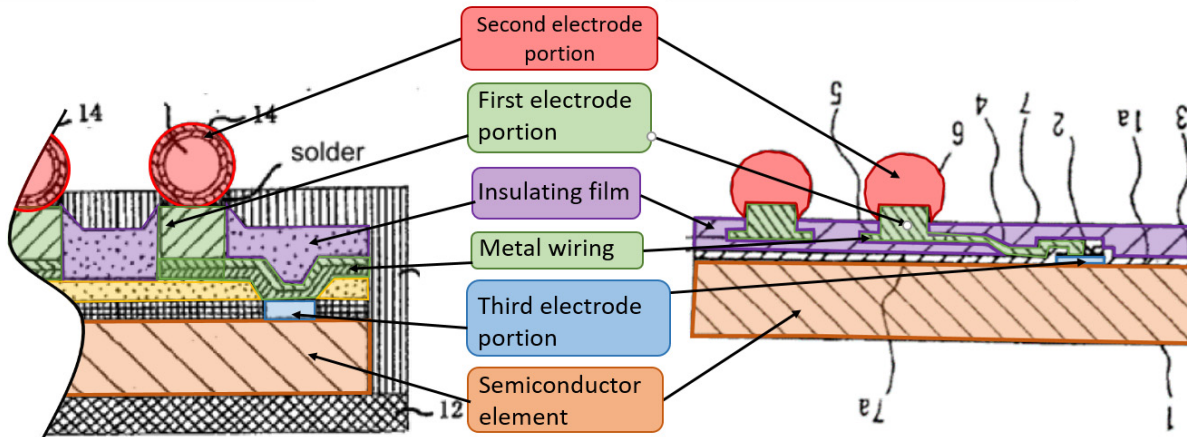
A POSA would have been motivated to improve the semiconductor device disclosed in Furuya by looking to the teachings of Yaguchi for improving the connection reliability for a semiconductor mounted on a printed wiring board (i.e., PCB). Ex-1002, ¶150. Both Furuya and Yaguchi are in the same field of technology and were filed around the same time. *Id.* Furuya and Yaguchi are directed toward very similar chip-size package devices that operate in a similar

¹⁸Claims 5 and 14 are dependent on Claims 1 and 10 respectively and, as a result, incorporate limitations for which this petition relies on Takizawa. Thus, although the subject matter of Claims 5 and 14 is fully disclosed by Furuya and Yaguchi, Takizawa is nevertheless included as part of this ground that renders these claims obvious.

manner, as shown in the annotated figure below.¹⁹ Ex-1006, [Abstract]; Ex-1011, 9:6-10; Ex-1002, ¶151.

Furuya Figure 1

Yaguchi Figure 1(a)



Furthermore, Furuya is directed toward providing high reliability in semiconductor devices “in which the connection strength between the metal post and the wiring pattern is high and the reliability of the electrical connection with the outside is high...” Ex-1006, [0015]. Yaguchi is directed to a similar problem—the disconnection of semiconductor devices from a substrate due to

¹⁹ A POSA would have recognized that Yaguchi and Furuya use different terminology to refer to elements that are the same. For ease of reference, the labels below are those used by the claims of the '001 Patent. Ex-1002, ¶151 n.12. The Figure in Yaguchi has also been inverted so that the elements are oriented as in Furuya.

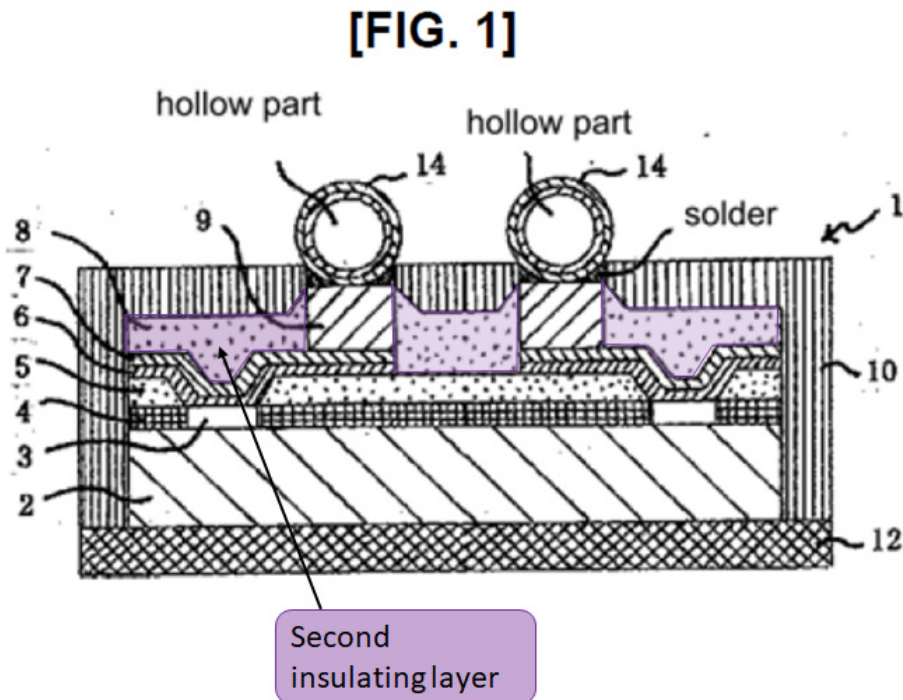
temperature changes. Ex-1011, 2:7-3:8; Ex-1002, ¶152. Yaguchi “is effective in preventing disconnection of the external terminal of a semiconductor device, particularly, a semiconductor device of a chip size...” so “high reliability can therefore be provided.” Ex-1011, 24:5-8. Yaguchi teaches increasing the reliability by “[h]aving a protrusion formed on the land to which the external terminal is bonded,” which “protrudes through the protective film” and is bonded to the external terminal. *See, e.g., id.*, 4:18-20; 9:13-19. Both references address means to form reliable electrical connections by forming structures that can withstand the stress or strain that is applied to the semiconductor device due to differences in thermal expansion coefficients between the silicon material of the semiconductor device and the material of which the printed circuit board is made. *See, e.g.,* Ex-1006, [0008]; Ex-1011, 2:7-3:26; Ex-1002, ¶153.

As a result, a POSA would have been motivated to add a protrusion that extended above the insulating film in Furuya to ensure a better connection, as taught by Yaguchi. Ex-1011, 4:18-29; Ex-1002, ¶154. Because such a combination would be nothing more than applying known techniques to similar systems, a POSA would have expected the combination to yield a predictable result and be successful. Ex-1002, ¶154.

2. Claim 5

- a. Furuya discloses “[t]he semiconductor device of claim 3, further comprising an insulating film formed on said metal wiring” (5[a])

Furuya discloses a second insulating layer formed on top of the wiring pattern. For example, Furuya teaches that after forming the wiring pattern 7, “a second insulating layer 8 is formed, which is in close contact with the wiring pattern 7.” Ex-1006, [0027]; Ex-1002, ¶155. *See also* Ex-1006, [0016]. Furuya elaborates that “the second insulating layer 8 is formed in a manner so as to cover the wiring pattern 7.” Ex-1006, [0063]. This second insulating layer is shown in Figure 1, annotated below.

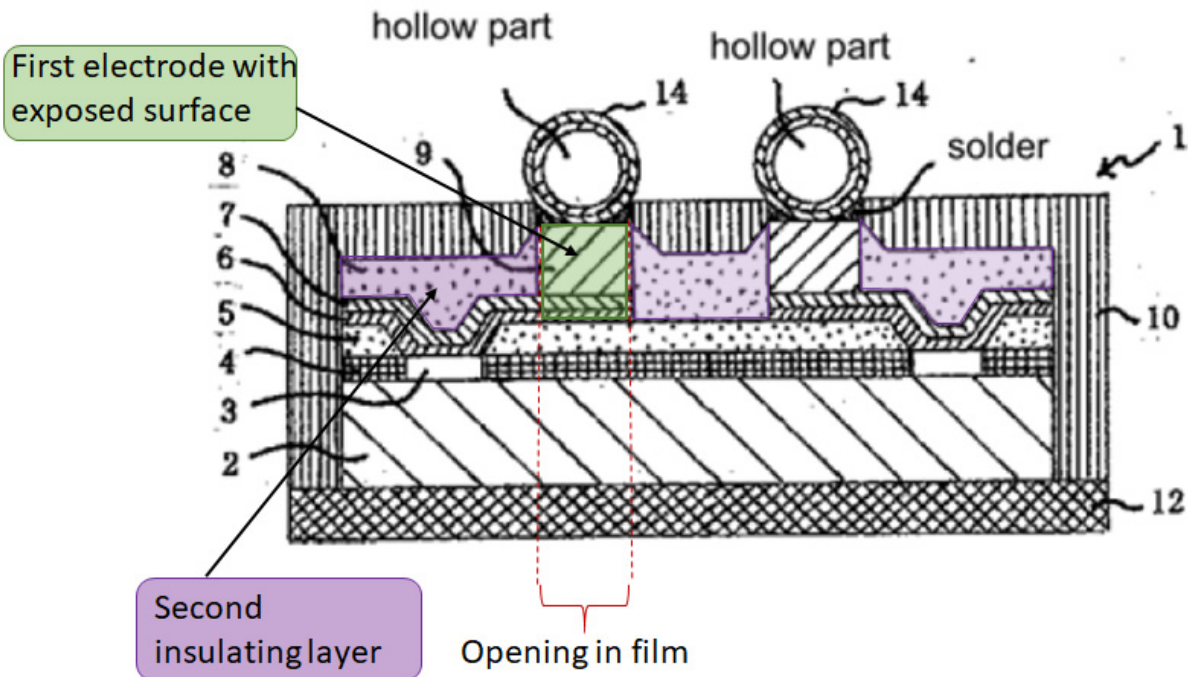


Thus, Furuya discloses each aspect of this limitation. Ex-1002, ¶155.

- b. Furuya discloses that “an opening of said insulating film exposes a surface of the first electrode portion” (5[b])

Furuya discloses the second insulating layer is formed such that the tip of the metal post, the distal portion of the first electrode, is exposed in order to provide an external connection point. Ex-1002, ¶156. Furuya states, “the second insulating layer 8 **exposed the top face of the metal post 9** and covered the side face of the metal post 9.” Ex-1006, [0053]. *See also* Ex-1006, [0024] - [0024], [0027], [0062]. Furuya also teaches “**removing the insulating resin from the tip region** of the metal post 9 for connecting to the outside.” *Id.*, [0046]. Thus, Furuya discloses forming an opening in insulating layer 8 to expose a surface of the first electrode portion. Thus, as shown in the annotated Figure 1 below, Furuya discloses creating an opening in the insulating film. Ex-1002, ¶157.

[FIG. 1]



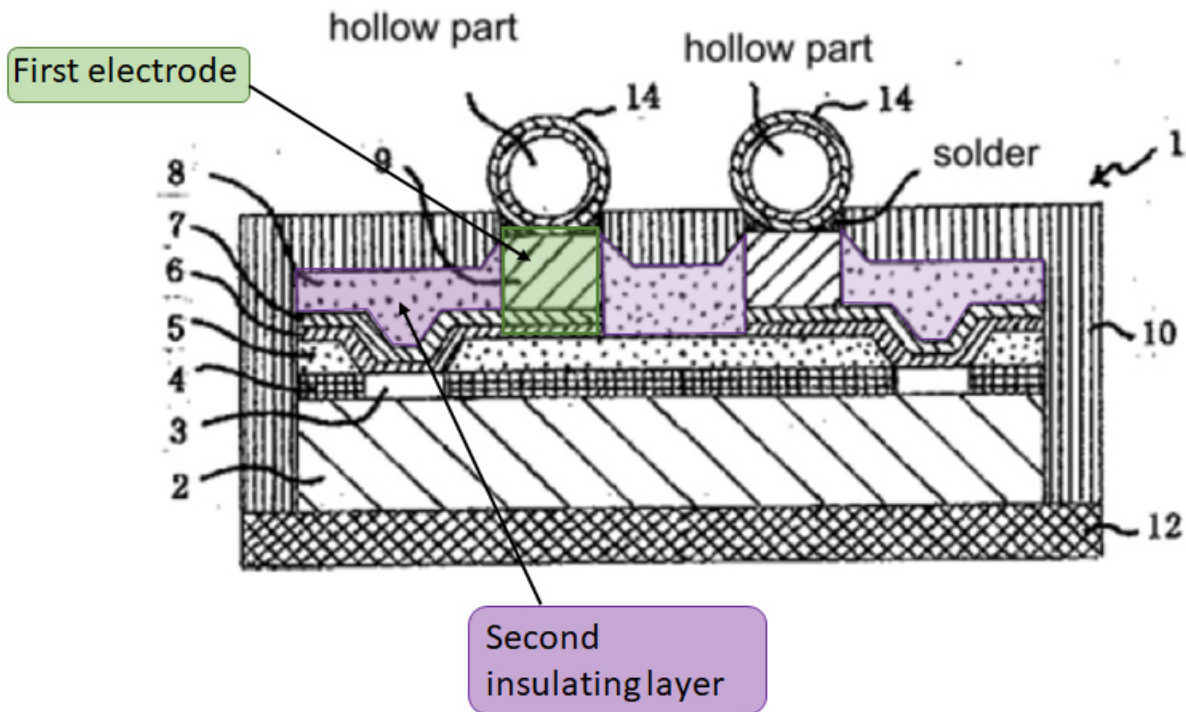
Thus, Furuya discloses each aspect of this limitation. Ex-1002, ¶157.

- c. Furuya in view of knowledge of a POSA as evidenced by Yaguchi discloses that “said surface of the first electrode portion is flush with or higher than a surface of the insulating film” (5[c])

Furuya discloses the insulating film is formed at a lower level than the metal post, which post is a portion of the first electrode, and, as described above, the top of the metal post is exposed. Ex-1002, ¶158. For example, Furuya teaches that the metal posts 9 have a thickness of 15 μm above the wiring pattern, while the “second insulating layer 8 was given a film thickness of 10 μm , **so as to be lower than the top face of the metal post 9.**” Ex-1006, [0053]. See also Ex-1006,

[0062]-[0063]. This structure is shown in Figure 1, annotated below. Ex-1002, ¶158.

[FIG. 1]



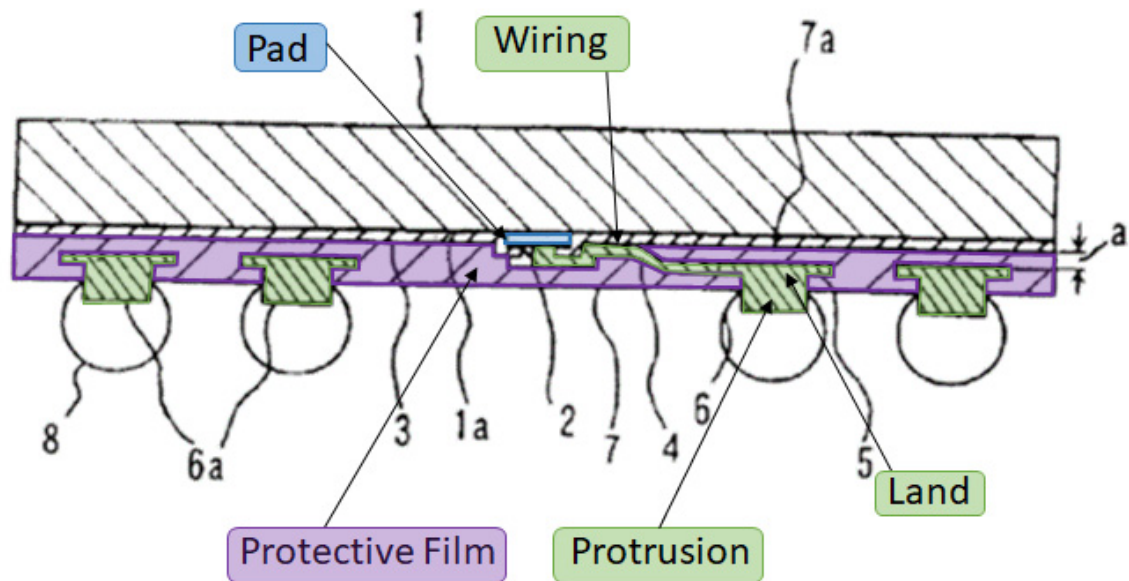
Furuya teaches that “after the metal post 9 is formed, the second insulating layer 8 is formed, using the insulating resin that has been applied and formed, and at this time, this is formed **so that the height of the second insulating layer 8, excluding the side face of the metal post 9, is such as to be a position that is lower than the height of the tip surface of the metal post 9.**” Ex-1006, [0047]. *See also id.*, [0017], [0029], [0031]-[0032]. Thus, although the sides of the metal post are covered by the insulating film at a greater height than the remainder of the

film, a POSA would have understood that the exposed top indicates that the insulating film is at most flush with (or approximately flush as the '001 Patent uses the term), and generally lower than, the top surface of the metal post. Ex-1002, ¶¶159-162. Moreover, a POSA would have recognized that the sealing resin 10 is an optional element and that the “second insulating layer 8” is the only layer that corresponds to the claimed insulating layer. *Id.* See also Ex-1006, [0048]-[0049]. Even when used, the sealing resin is “close” to the surface of the metal post and therefore meets the “flush with” requirement. Ex-1006, [0032]; Ex-1002, ¶162.

To the extent the Board finds Furuya’s disclosure of the insulating film being flush with or lower than the first electrode portion insufficient, a POSA would have been motivated to combine Furuya with Yaguchi for the reasons discussed above. Yaguchi explicitly discloses that the first electrode portion is flush with or higher than the insulating film because it explains the first electrode portion is composed of a “land,” i.e., enlarged portion of conductor material for making an electrical connection, connected to the conductive wiring and a protrusion formed on the land. Ex-1011, 4:18-29; Ex-1002, ¶163. This first electrode portion parallels the disclosure of the first electrode portion described above for Furuya. Ex-1002, ¶163. These elements are used in conjunction with an external terminal to create an electrical connection between the pad and an external substrate. Ex-1011, 9:5-19. These elements are illustrated in Figure 1(a),

including the protrusion 6, the pad 2, the wiring 4, and the land 5.

FIG. 1(a)



Yaguchi further explains that a protective film, labeled 7 in the figure above, “covers a part of the passivation film 3, conductive wiring line 4, land 5, and protrusion 6 on the semiconductor element surface.” Ex-1011, 9:13-16; Ex-1002, ¶164. This protective film is an insulating layer made of “a poly[i]mide resin...or the like.” Ex-1011, 9:26-28. Yaguchi explains that although some of the protrusion 6 is covered by the protective film, “[a] part of the protrusion 6 protrudes through the protective film 7 and this protruding part 6a is joined to the external terminal 8.” Ex-1011, 9:16-17. Thus, because protruding part 6a extends beyond the protective film, or insulating layer, Yaguchi teaches that the first

electrode portion is higher than the insulating film. Ex-1002, ¶164.

Thus, Furuya in view of knowledge of a POSA as evidenced by Yaguchi discloses this claim element. Accordingly, Furuya in view of Takizawa and further in view of the knowledge of a POSA as evidenced by Yaguchi renders obvious Claim 5. Ex-1002, ¶165.

3. Claim 14

- a. Furuya discloses “[t]he semiconductor device of claim 12, further comprising an insulating film formed on said metal wiring” (14[a])

Furuya discloses this element as discussed in relation to claim element 5[a].
Ex-1002, ¶166.

- b. Furuya discloses “wherein an opening of said insulating film exposes a surface of the first electrode portion” (14[b])

Furuya discloses this element as discussed in relation to claim element 5[b].
Ex-1002, ¶167.

- c. Furuya in view of knowledge of a POSA as evidenced by Yaguchi discloses “wherein said surface of the first electrode portion is flush with or higher than a surface of the insulating film” (14[c])

Furuya in view of knowledge of a POSA as evidenced by Yaguchi discloses this claim element as discussed in relation to claim element 5[c]. Ex-1002, ¶168.
Accordingly, Furuya in view of Takizawa and further in view of the knowledge of a POSA as evidenced by Yaguchi renders obvious Claim 14.

C. Ground 3: Furuya In View Of Takizawa And Further In View Of The Knowledge Of A POSA (as evidenced by Nozawa) Renders Obvious Challenged Claims 9 and 18²⁰

1. Reasons To Combine Furuya And Takizawa With Nozawa

A POSA would have been motivated to combine Furuya and Takizawa for the reasons above in relation to Ground 1. A POSA would have known that semiconductor devices like those disclosed in Furuya and Takizawa must be connected through wiring electrodes to other semiconductor devices in order to be useful. Ex-1002, ¶169. This understanding is confirmed by Nozawa. A POSA would have known that applying the teaching of Nozawa to the device described in Furuya would provide benefits including integration with a wide variety of PCBs for a wide range of applications. Ex-1002, ¶169. For example, Nozawa teaches that it allows for a reliable connection to be formed directly between the solder bumps and a substrate, allowing for more compact and lightweight electronic devices. Ex-1012, 1:20-31; 1:41-48. Additionally, Nozawa teaches that its device

²⁰Claims 9 and 18 are dependent on Claims 1 and 10 respectively and, as a result, incorporate limitations for which this petition relies on Takizawa. Thus, although the subject matter of claims 9 and 18 is fully disclosed by Furuya and Nozawa, Takizawa is nevertheless included as part of this ground that renders these claims obvious.

allows connection with a wider range of substrates, including those with much greater thermal expansion coefficients, which would allow the device of Furuya to be used in a wider variety of circumstances. Ex-1012, 8:32-40; Ex-1002, ¶170.

Moreover, Nozawa reflects that a POSA would have known to connect the second electrode portion in Furuya to the wiring electrode of an external substrate. Nozawa explains that such a substrate would include wiring for the connection and provides an illustration of the semiconductor device connecting with the substrate. Ex-1012, 8:30-44, Fig. 9. This is consistent with the understanding a POSA would have had that a chip-scale packaging device (CSP), such as Furuya, is only useful to the extent it is connected externally. Ex-1002, ¶171. Such a connection allows the device to receive power, connect with other semiconductor devices, become integrated as part of a larger device, and serve a useful function. Nozawa, also a CSP, provides an example of how this is done.

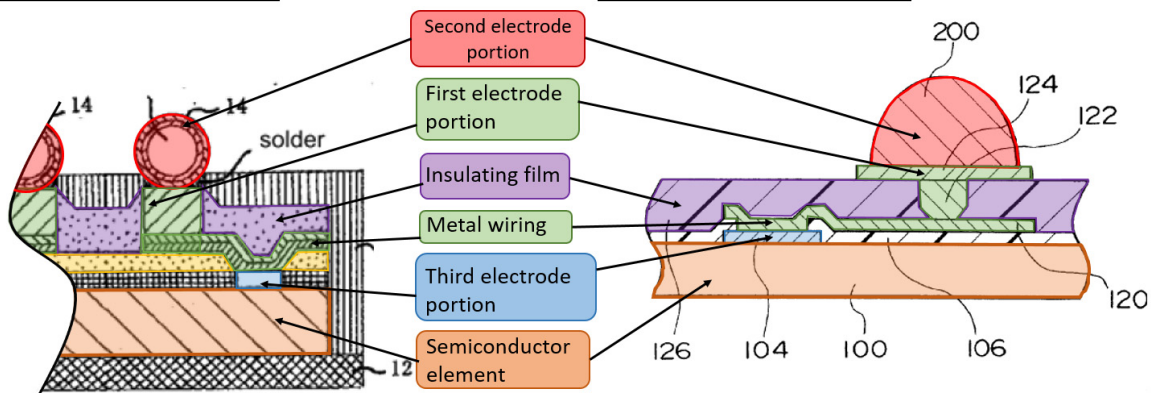
Both Furuya and Nozawa are in the same field of technology and were filed around the same time. Furuya and Nozawa are directed toward very similar

systems that operate in a similar manner as shown in the annotated figure below.²¹

Ex-1006, [Abstract]; Ex-1012, 1:53-64; Ex-1002, ¶172.

Furuya Figure 1

Nozawa Figure 1



Because the devices are so similar, applying the teachings of Nozawa to the device in Furuya would have been natural to a POSA. Ex-1002, ¶173. Because such a combination would be nothing more than applying known techniques to similar system, a POSA would have expected the combination to yield a predictable, successful result. *Id.*

²¹ A POSA would have recognized that Nozawa and Furuya use different terminology to refer to elements that are the same. For ease of reference, the labels below are those used by the claims of the '001 Patent. Ex-1002, ¶172 n.13.

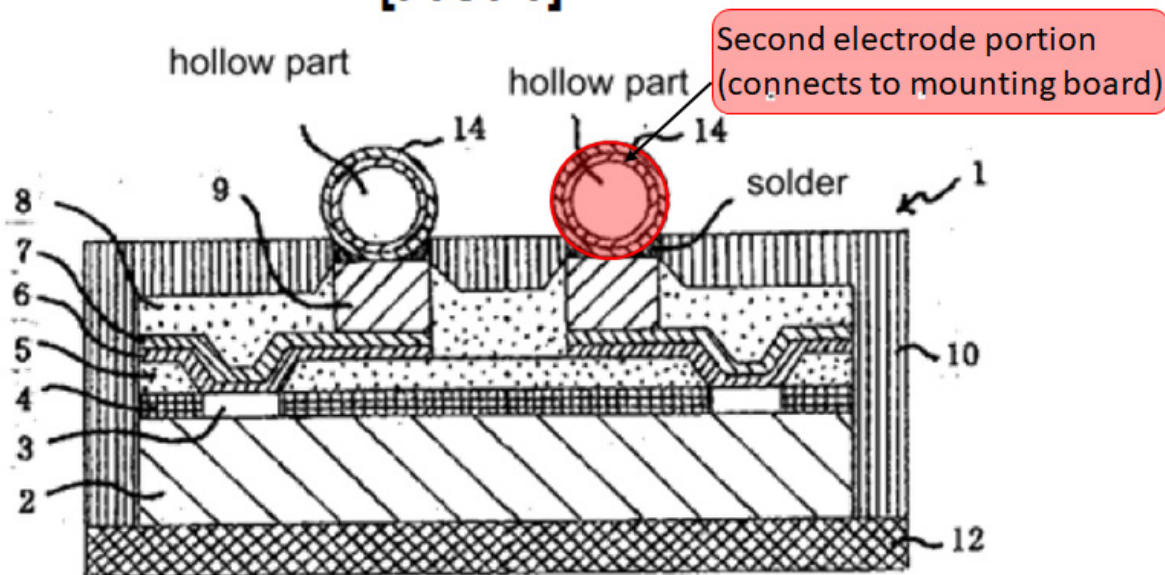
2. Claim 9: “The semiconductor device of claim 1, further comprising a substrate having a wiring electrode, wherein said wiring electrode is electrically connected to said second electrode portion”

Furuya discloses this limitation because the external connection terminal (i.e., second electrode portion) forms an external electrical connections with electrodes on a mounting board or PCB (i.e., wiring electrode). Ex-1002, ¶174; Ex-1006, [0006]. *See also, e.g.*, Ex-1001, 1:23-35, 2:4-15.

Furuya teaches that “a characteristic of the semiconductor device 1 of the present invention, as shown in FIG. 1, is that an **external connection terminal 14 that makes an external electrical connection (for example, to a mounting board)** is placed at the tip end of the metal post 9.” Ex-1006, [0036]. *See also id.*, [0006]-[0009], [0029], [0039], [0043]. These external connection terminals, corresponding to the “second electrode portion” of the ’001 Patent, are shown in Figure 1, annotated below, though the connection to the mounting board on the external substrate is not shown (as is also the case in the figures for the ’001 Patent). Ex-1002, ¶¶174-177. Furuya describes testing performed to validate the advantages of the CSP semiconductor device when the device is mounted onto a substrate. *See, e.g.*, Ex-1006, [0056]-[0058]; Ex-1002, ¶175. Thus, just like the ’001 Patent, Furuya teaches that the second electrode portion (which includes “metal post 9”) is electrically connected to a wiring electrode (i.e., the electrode on the substrate or “mounting board”). If the device in Furuya was not connected in

this manner, the described “external electrical connection” would not be possible.

[FIG. 1]



This disclosure of wiring electrode in Furuya is commensurate in detail to the '001 Patent's disclosure. Ex-1002, ¶177. For example, in the embodiments disclosed in the '001 Patent, a “wiring electrode” of the “substrate” refers to an external electrical connection on the not-shown circuit board to which the disclosed semiconductor device is mounted. Ex-1001, 1:60-67. *See also* Ex-1002, ¶177; Ex-1001, 8:59-63 (“The external electrode portions 14a and the wiring electrodes of the substrate on which the semiconductor device is mounted are respectively connected to each other by the ball electrodes 16.”). Thus, Patent Owner cannot distinguish this reference over an alleged lack of technical description. *Lockwood v. Am. Airlines*, 107 F.3d 1565, 1570 (Fed. Cir. 1997)

(rejecting Patent Owner’s criticism of prior art because “[p]atent itself does not disclose the level of detail that [the PO] would have us require of the prior art.”). Moreover, the applicant admitted that establishing this connection was known in the applicant admitted prior art. Ex-1001, 1:60-67. *See also* Riverwood Int’l Corp. v. R.A. Jones & Co., 324 F.3d 1346, 1354 (Fed. Cir. 2003).

To the extent the Board nevertheless finds Furuya’s disclosure of a wiring electrode to be insufficient, a POSA would have known that the device in Furuya would have been of limited use unless electrically connected to another device. Ex-1002, ¶¶178-179. This is confirmed by Nozawa , as discussed above, because Nozawa explicitly discloses a substrate having a wiring electrode that is electrically connected to the second electrode portion. Ex-1002, ¶179. In fact, one of the stated goals of Nozawa is to establish a “direct connection to a substrate” from a semiconductor device. Ex-1012, 1:46-47.

After describing a semiconductor device similar to the device disclosed in Furuya, Nozawa teaches that the semiconductor device is connected to a substrate:

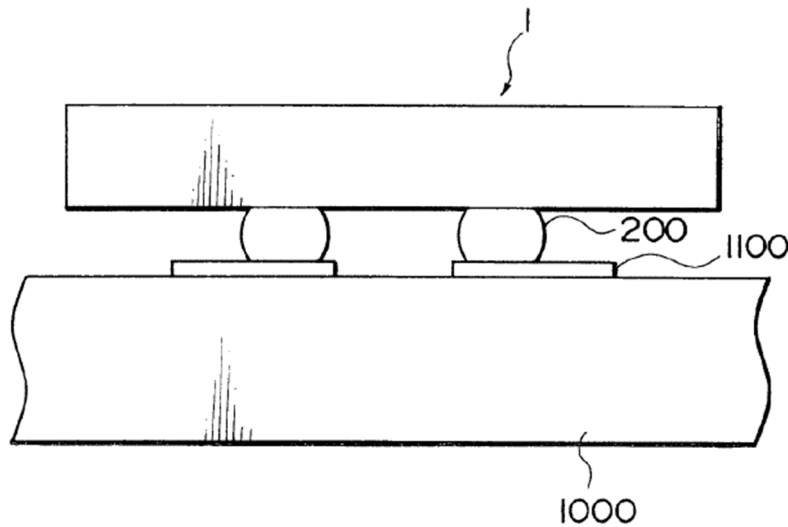
In FIG. 9 is shown a circuit board 1000 on which is mounted this embodiment of the semiconductor device

1. For the circuit board 1000 is generally used an organic substrate such as a glass epoxy substrate or the like. On the circuit board 1000, an interconnect pattern 1100 of

for example copper is formed to constitute a desired circuit, and by mechanical connection of the interconnect pattern thereof to the bumps 200 forming the external electrodes of the semiconductor device 1, electrical connection is achieved.

Ex-1012, 8:30-44. Figure 9 below illustrates the connection between the semiconductor device and the circuit board. Ex-1002, ¶180.

FIG. 9



To the extent that Patent Owner argues that the “wiring electrode” should instead be mapped to the electrode formed on the silicon substrate (e.g., depicted as numeral 12 in Ex-1001, Fig. 5), Furuya also discloses this same wiring electrode

for the reasons discussed above in Section X.A.4. Ex-1002, ¶181.

Thus, Furuya in view of the knowledge of a POSA as evidenced by Nozawa discloses the subject matter of Claim 9. Ex-1002, ¶182. Accordingly, Furuya in view of Takizawa and further in view of the knowledge of a POSA as evidenced by Nozawa renders obvious Claim 9.

3. Claim 18: “The semiconductor device of claim 10, further comprising a substrate having a wiring electrode, wherein said wiring electrode is electrically connected to said second electrode portion.”

Furuya in view of Nozawa discloses this claim as discussed in relation to Claim 9. Ex-1002, ¶183. Accordingly, Furuya in view of Takizawa and further in view of the knowledge of a POSA as evidenced by Nozawa renders obvious Claim 18.

XI. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

Samsung is aware of no evidence of secondary considerations or objective indicia of non-obviousness that have the requisite nexus to the claimed features that were not already known in the art as of December 20, 2001. Ex-1002, ¶184.

**XII. THIS PETITION IS NOT CUMULATIVE TO SAMSUNG’S
SIMULTANEOUSLY FILED PETITION OR TO IPR2017-01486
FILED BY BROADCOM**

Samsung’s simultaneously-filed petition challenging Claims 1-4, 6-13, and 15-18 relies on Japanese Unexamined Patent Application Bulletin No. JP-2001-118957-A (“Kimura”) as a primary reference while the present IPR petition relies

on Furuya as a primary reference. These grounds are distinct and non-redundant bases for finding the Challenged Claims of the '001 Patent invalid. Furuya and Kimura are not redundant because certain features disclosed in one reference may be disclosed more explicitly in the other reference.

For example, although Furuya discloses an embodiment in which the first electrode portion has a total thickness of 15.7 μm , where the metal post is 15 μm , it discloses a broad range of possible thicknesses for the post, some of which would cause the total thickness of the first electrode portion and the diffusion layer to fall outside of the claimed range. By contrast Kimura teaches a smaller range, which is entirely contained within the 10 μm to 20 μm range recited in certain claims of the '001 Patent. However, Furuya provides advantages over Kimura because it discloses a semiconductor device with a layer structure and organization that is identical to the '001 Patent, while Kimura discloses additional layers.

The Board has outlined seven factors for exercising its discretion to deny follow-on petitions. *See e.g., NVIDIA Corp. v. Samsung Elec. Co.*, Case IPR2016-00134, Paper 9 at 6-7 (PTAB May 4, 2016); *General Plastic Industrial Co., Ltd., v. Canon Kabushiki Kaisha*, Case IPR2016-01357, et al., Paper 19 at 16-21. As a whole, these factors tip in favor of instituting the current petition. Samsung has filed a simultaneous petition also challenging the '001 Patent, but has not previously filed any other petition directed to the same claims. Thus, institution of

this IPR petition would not create unfair prejudice to the Patent Owner.

Samsung's present petition is also not cumulative to Broadcom's IPR petition IPR2017-01486 nor untimely in view of Broadcom's IPR. First, Samsung was not a party to IPR2017-01486 and was not in litigation with Patent Owner at the time that Broadcom filed its petition. Second, Samsung has advanced materially different grounds than Broadcom. While Samsung agrees with the Board's conclusion that Broadcom was likely to prevail in showing invalidity over the German application that corresponds to Takizawa, which is indeed a very strong reference, Samsung believes that the references relied upon in the instant petition provide an even stronger basis to reject the claims. Third, IPR2017-01486 was instituted and thus this scenario differs from those in which a second petition effectively attempts to remedy shortcomings pointed out by the Board. Finally, Broadcom's petition has now been withdrawn, so there is no longer any pending petition, other than Samsung's simultaneously-filed petition.

Neither is the present petition cumulative of the Broadcom IPR under the *NVIDIA* test. The first five factors each assume that the follow-on petition is submitted by the same petitioner as the original petition, whereas here the two petitioners are unrelated. *Id.* Factors 6 ("the finite resources of the Board") and 7 ("the requirement under 35 U.S.C. § 316(a)(11) to issue a final determination not later than 1 year after the date on which the Director notices institution of review")

also weigh in favor of granting the instant petition because Samsung is an unrelated petitioner and because the Broadcom IPR has been terminated. *Id.* For all these reasons and in view of the substantive strength of the instant petition, Samsung respectfully requests that the Board view the instant petition as entirely proper and meritorious.

XIII. CONCLUSION

For the reasons given above, Samsung requests institution of IPR for Claims 1-18 of the '001 Patent based on each of the grounds specified in this Petition. Ex-1002, ¶185.

Dated: March 16, 2018

By: /John Kappos/
John Kappos (Reg. No. 37,861)

Certification of Word Count

Pursuant to 37 C.F.R. § 42.24(d), Samsung certifies that this petition includes 13,996 words, as measured by Microsoft Word, plus words in figures and diagrams, exclusive of the table of contents, mandatory notices under § 42.8, certificates of service, and word count, and exhibits.

CERTIFICATE OF SERVICE

The undersigned certifies pursuant to 37 C.F.R. § 42.6(e) and § 42.105 that on March 16, 2018, a true and correct copy of the **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,954,001** was served via express mail on the Patent Owner at the following correspondence address of record:

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