

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS
AMERICA, INC., AND SAMSUNG SEMICONDUCTOR, INC.
Petitioner

v.

TESSERA ADVANCED TECHNOLOGIES, INC.
Patent Owner

U.S. Patent No. 6,954,001

**DECLARATION OF MILTIADIS K. HATALIS, PH.D.
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 6,954,001**

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1. I, Miltiadis K. Hatalis, declare as follows:

I. INTRODUCTION

2. I have been retained by Samsung Electronics Co., Ltd, Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (collectively “Samsung”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”).

3. I have been asked to consider whether certain references teach or suggest the features recited in Claims 1-18 (the “Challenged Claims”) of U.S. Patent No. 6,954,001 (“the ’001 Patent”) (Ex. 1001), which I understand is allegedly owned by Tessera Advanced Technologies, Inc. (“Patent Owner”). My opinions and the bases for my opinions are set forth below. In forming my opinions, I have reviewed and relied upon the exhibits attached to the present ’001 IPR Petition.

4. I am being compensated at my ordinary and customary consulting rate of \$350 per hour for my work.

5. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

II. BACKGROUND AND EXPERIENCE

A. Qualifications

6. I have been a Professor in the Department of Electrical and Computer Engineering at Lehigh University since 1987. I have over 30 years of experience, as a professor, and practitioner, in fields of semiconductor and microelectronics technology. My background and qualifications are set forth in my curriculum vitae, attached as Exhibit 1003.

7. As set forth in my curriculum vitae, I received a Doctor of Philosophy degree in Electrical and Computer Engineering from Carnegie Mellon University in 1987. The topic of my PhD dissertation research was "Crystallization of Amorphous Silicon Films and its Application in Bipolar and Thin Film Transistors." I received a Master of Science degree in Electrical and Computer Engineering from State University of New York at Buffalo in 1984 and I received a Bachelor of Science degree in Physics from Aristotle University of Thessaloniki in Greece in 1982.

8. Upon receiving my PhD, I joined the faculty of Lehigh University in the Department of Electrical and Computer Engineering as an Assistant Professor. I was promoted to Associate Professor with tenure in 1991 and to Professor in 1995. From 1987-92, I served as Associate Director of Lehigh's Microelectronics Research Laboratory.

9. In 1992, I founded, and became Director of, the "Display Research Laboratory," which was the first academic laboratory in the United States dedicated to research and development of electronic thin film materials and devices, including Thin Film Transistors, for flat panel displays, flexible electronics and novel large area microelectronic system applications. As Director of Lehigh's Display Research Laboratory, I have raised over \$13 million through research contracts and grants to support the laboratory's research activities. These contracts and grants were funded by the Defense Advanced Research Program Agency (DARPA), the Army Research Laboratory (ARL), the National Science Foundation (NSF), the National Aeronautics and Space Administration (NASA), the State of Pennsylvania, and a variety of industrial companies including IBM, Kodak, Sharp, Northrop Grumman, and others.

10. From 1987 to present I have conducted research in microelectronics, including semiconductors, electronic materials, devices and circuits for integrated circuits and integrated microsystems. My research mainly focuses on electronic thin film materials and devices, microelectronic fabrication processes, novel electronic circuits and integrated microsystems. My research group pioneered the development of electronic materials, devices and circuits on flexible substrates, active matrix organic light emitting diode displays, and addressable arrays for

integrated sensor applications such as fingerprint sensors for biometrics and multichannel gas sensors.

11. As a faculty member, I supervised the research of twenty PhD dissertations in the technical field of semiconductors/microelectronics. Upon graduating, all twenty of my PhD graduate students moved either to industrial positions in the electronic industry including Apple, IBM, Intel, TSMC, and Motorola or into academic positions in US or abroad. I have also supervised the research of several post-doctoral researchers and research associates at Lehigh. Moreover, I have supervised a large number of graduate student Master's theses and numerous undergraduate research projects. I have been an invited lecturer at numerous universities, industrial laboratories and conferences in the United States and overseas.

12. I have been an author or co-author of 175 technical publications which include two book chapters, 76 peer-reviewed publications in peer-reviewed journals, and 97 papers published in conference proceedings. My papers received over 3700 citations and I have an H-index of 26. The list of peer-reviewed journals in which my papers were published include Solid State Electronics, Journal of Applied Physics, Journal of the Society for Information Display, Journal of Materials Science, and multiple IEEE journals including the IEEE Journal of Display Technology, IEEE Transactions on Electronic Devices, IEEE Solid State

Circuits and IEEE Electron Device Letters. The technical conference where my papers were presented have been organized by scientific societies including: Society of Information Display (SID), Materials Research Society (MRS), Electrochemical Society (ECS) and Institute of Electrical and Electronics Engineers (IEEE).

13. I am also a named inventor on U.S. Patent No. 8,390,536, directed at controlling current to pixels in an active matrix display by adjusting voltage on the data lines and two international patents associated with the above invention one issued in Korea and one in Japan.

14. I have taught a number of different undergraduate and graduate level courses in the Electrical and Computer Engineering department at Lehigh University. These courses have generally centered on physics, technology, and the design and fabrication of solid-state devices and integrated circuits. I have also introduced several new courses which include "Introduction to VLSI Design," "Semiconductor Material and Device Characterization," and "Introduction to Photovoltaic Energy Systems." I also regularly teach the "Electronic Circuits" and "Introduction to VLSI Circuits" courses.

15. As part of my research, I utilize much of the same equipment and many of the same microfabrication processes that are in use by the semiconductor industry including: Plasma-Enhanced Chemical Vapor Deposition (PECVD) for the

deposition of silicon nitride and silicon dioxide films; sputter and e-beam deposition tools for aluminum, copper, tungsten, titanium, gold, tantalum and other metallic thin films; photolithographic tools for defining photoresist patterns on the substrates; as well as reactive ion etching or wet etching tools for removing various thin film materials from the substrates. I also utilize several tools for the characterization of the materials and structures used in microelectronic devices including: optical microscopes, Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), and Atomic Force Microscopy (AFM). I further utilize a variety of electrical characterization techniques and instruments for testing the electrical performance of completed electronic circuits and systems.

16. As part of my research, I pioneered a technique for crystallizing amorphous silicon. Similar techniques have been used in the manufacture of integrated circuits and flat panel displays. In addition, my research group at Lehigh pioneered the fabrication of electronic devices and circuits on novel flexible substrates and the development of integrated microsystems flexible substrates, including active matrix organic light emitting diode displays, and addressable arrays for integrated sensor applications such as fingerprint sensors for biometrics and multichannel gas sensors. Many industrial and academic laboratories currently pursue similar research activities. Such research flows from the accomplishments of my research group in this technical field.

17. My industrial experience includes work at the XEROX Palo Alto Research Laboratory and various consulting projects with semiconductor companies. All of these projects were related to electronic materials, semiconductor devices and their application to microelectronic systems.

18. I am a member of several professional organizations including the Electron Device Society of the Institute of Electrical and Electronics Engineers (IEEE) and the Society for Information Display (SID). I have also been the chair or co-chair at numerous national and international conferences and symposiums, including several SID-sponsored Workshops on Active Matrix Liquid Crystal Displays and a Materials Research Society Symposium on Flat Panel Displays. I have co-authored two book chapters, one dealing with the "Polysilicon TFT Technology" and another on the application of "Polysilicon TFTs in AMOLED Displays." I have served as a reviewer for technical papers submitted to several scientific journals and have also served as a reviewer for several years for the National Science Foundation Small Business Innovative Research (SBIR) program.

19. A detailed list of my publications, education and professional experience, research grants, PhD dissertations for which I served as advisor, publications and litigation cases in which I served as a technical expert, can be found in my curriculum vitae attached and submitted as Exhibit 1003.

B. Previous Testimony

20. In the previous five years, I have testified as an expert at trial or by deposition or have submitted declarations in the following cases:

- *MiiCs & Partners America, et al. v. Toshiba, et al.*, No. 1:14-cv-00803-RGA (D. Del. 2016)
- *MiiCs & Partners America, et al. v. Funai, et al.*, No. 1:14-cv-00804-RGA (D. Del. 2016)
- *Round Rock Research LLC v. Ricoh Corporation*, No. 1:15-cv-00157-SLR (D. Del. 2016)
- *ChiMei Innolux Corp. v. Semiconductor Energy Laboratory Co., Ltd*, Multiple IPRs including: IPR2013-00060, IPR2013-00038, IPR2013-00068, IPR2013-00028, IPR2013-00066
- *Samsung Electronics Co., Ltd., et al. v. Tessera Advanced Technologies, Inc.*, Case IPR2018-00466

III. LEVEL OF ORDINARY SKILL IN THE ART

21. Based on my review of the '001 Patent specification, claims, file history, and prior art, I believe a person of ordinary skill in the art around the time of the alleged invention of the '001 Patent would have had i) a bachelor-level degree in mechanical engineering, materials science, electrical engineering, , or a related field and 3–5 years of experience in the design/development of

semiconductor packages; ii) a Master's-level degree in mechanical engineering, materials science, electrical engineering, or a related field and 1–3 years of experience in the design/development of semiconductor packages, or iii) a PhD-level degree in mechanical engineering, materials science, electrical engineering, or a related field and some experience in the area of semiconductor packaging.

22. In determining the level of ordinary skill in the art, I was asked to consider, for example, the type of problems encountered in the art, prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field.

23. My opinions concerning the '001 Patent claims and the prior art are from the perspective of a person of ordinary skill in the art ("POSA"), as set forth above.

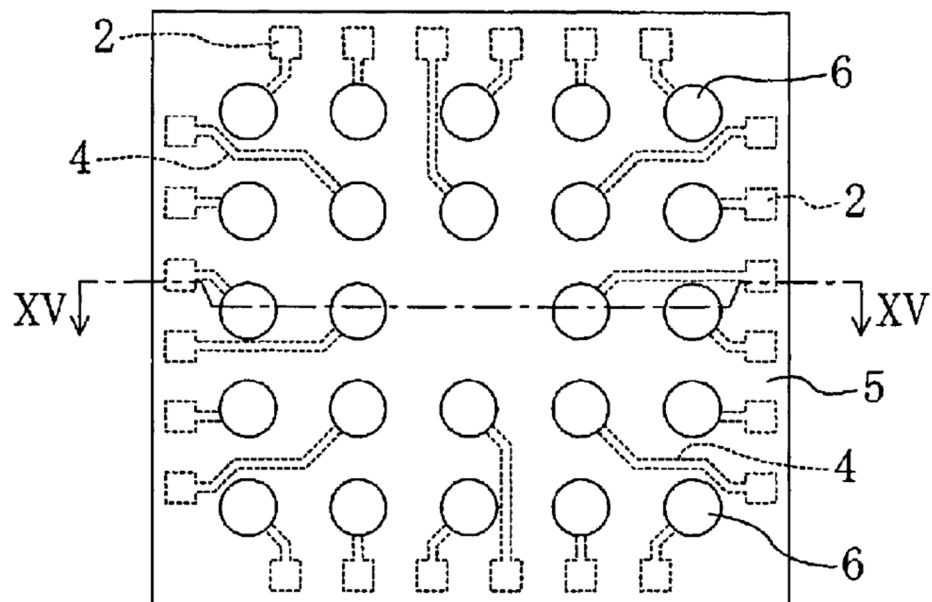
IV. TECHNOLOGICAL BACKGROUND

24. The '001 Patent specification provides an overview of the relevant technology. It explains that "in a CSP (Chip Size Package) type semiconductor device, electrodes of a semiconductor element are formed by a dry etching method in a diffusion process, whereas wiring electrodes of a substrate on which the semiconductor element is mounted are formed by a wet etching method in an assembling process." Ex-1001, 1:23-28. As a result, the pitch of the wiring

electrode is greater than that of the electrodes of the semiconductor element, and metal wirings are formed on the semiconductor device to electrically connect these electrodes. *Id.*, 1:28-39.

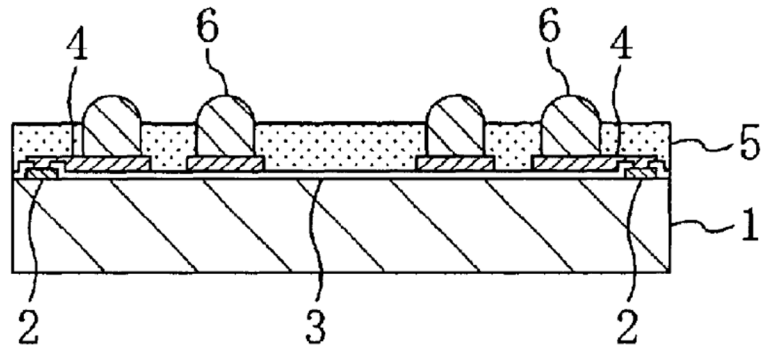
25. In particular, part of each metal wiring on the semiconductor element is used as an external electrode in order to increase the distance between the external electrodes. *Id.*, 1:34-39. Figure 15A shows a perspective plan view of a semiconductor device where electrodes 2 are formed on the surface of the semiconductor element 1 and connected by metal wirings 4 to ball electrodes 6. *Id.*, 1:43-67.

FIG. 15A
Prior Art



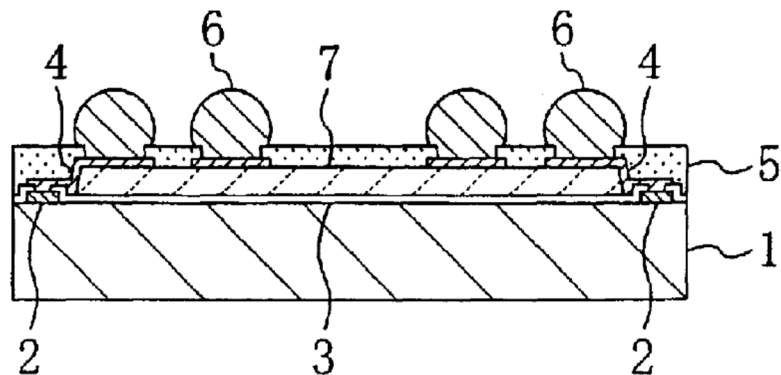
26. Figure 15B shows a cross-sectional view along section line XV shown in Figure 15A. Figure 15B shows that the electrodes formed on the surface of the semiconductor element are connected to a metal wiring, part of which forms into an external electrode and is connected to a ball electrode. *Id.*

FIG. 15B
Prior Art



27. Figure 15C shows a similar device, except an insulating resin layer 7 is formed between the passivation film 3 on the semiconductor element 1 and the metal wirings 4. *Id.*, 1:65-67.

FIG. 15C
Prior Art



28. The '001 Patent explains that the metal wirings attached to the electrode are formed of copper, while the ball electrode is formed of a tin-

containing solder. *Id.*, 2:4-9, 2:15-18. Thus, when the two are joined, a “metal junction of Cu (the metal wirings 4) and solder (the ball electrodes 6) is formed at the boundary between the metal wirings 4 and the ball electrode 6.” *Id.*, 2:9-14.

29. The ‘001 Patent explicitly discloses that the formation of this “metal junction” was well understood in the prior art. *Id.*, 1:60-67. Specifically, the ’001 Patent explains that in order to form this “metal junction,” which results in an electrical connection, first the molten solder containing tin, comes in contact with the metal, i.e., copper, of the external electrode portion:

In order to electrically connect the electrodes 2 formed on the surface of the semiconductor element 1 to wiring electrodes of a substrate (not shown) on which the semiconductor element 1 is mounted, respectively, **a ball electrode 6 formed from solder is connected in a molten state** to each opening of the solder resist film 3 [sic: 5], that is, **to the external electrode portion of each metal wiring 4.**

Id., 1:60-67,¹ (emphasis added).

¹ This text incorrectly cites reference number 3 as referring to the solder resist film and should instead cite to reference number 5. In context, this error would be apparent to a POSA.

30. When tin (Sn) from molten solder is in contact with the copper (Cu) metal of the external electrode portion, tin and copper form a diffusion layer:

In the above conventional semiconductor device, however, **tin (Sn) contained in the solder of the ball electrode 6 diffuses into Cu of the metal wiring 4 to form a Sn-Cu alloy.**

Id., 2:15-18, (emphasis added).

31. The '001 Patent states that “[t]he Sn-Cu alloy layer is weak and hard” in other words it is brittle and because it “grows in the most part of the metal wiring,” it can be broken by the stresses resulting from later processing (heating and cooling) of the semiconductor device. *Id.*, 2:15-21. Breakage occurs because the substrate and the semiconductor element have different thermal expansion coefficients, heating and cooling will cause different amounts of expansion in each component, which causes stress between components that can further contribute to failure of the device. *Id.*, 2:22-31.

32. As the '001 Patent acknowledges, it was well known to POSAs that: 1) conventional solders comprise tin (Sn); 2) a Sn-Cu alloy is formed when molten tin comes into contact with a copper metal electrode; 3) the Sn-Cu alloy layer forms the “junction” or metallurgical bond that joins and electrically connects the semiconductor device to the substrate, e.g., PCB board; and 4) the Sn-Cu alloy is “weak and hard” and thus brittle.

33. For example, it was well known that “tin-lead alloys are the most widespread solder alloys.” *See, e.g.* Ex-1018, H.H. Manko, *Solders and Soldering* 68 (2001). In fact, “[t]o many people, the term solder has become synonymous with the tin-lead alloy system.” *Id.*, 71. Furthermore, various compositions of tin-lead solders were well-known, including the eutectic tin-lead alloy: 63wt%Sn/37wt%Pb. *See, e.g.*, Ex-1019, J.S. Hwang, *Modern Solder Technology for Competitive Electronics Manufacturing*, 60 (1999).

34. It was also well-known that “metallurgical bonding occurs, in a solder joint, between the solder and the substrate at a boundary area termed the interface. This interface consists of a thin layer of an alloy formed during the soldering process. The alloy – termed intermetallic is generated by metals from both the solder and the substrate.” *See*, Ex-1020, *Mechanics of Solder Alloy Interconnects* 42 (eds. D.R. Frear, et al., 1994). Furthermore, “tin-based solders on a copper substrate form two Cu/Sn intermetallic compounds with two distinct stoichiometries at room temperature: Cu_6Sn_5 (η -phase) and Cu_3Sn (ϵ -phase).” *Id.*, 54-55. The physical properties of these materials were also well known, for example “[t]he hardness is greater for the intermetallics, indicating their greater brittleness.” *Id.*, 60-61.

35. It was also well understood that “[w]hile the presence of intermetallic compounds are an indication that a good metallurgical bond has formed, the fact

that these compounds are brittle may also make them deleterious to a joint's mechanical integrity. . . . In addition, if these intermetallic compounds become too thick, the reliability of the joint can be jeopardized due to cracking. This can be a problem especially if the joint is exposed to any mechanical forces, such as expansion or contraction of the printed wiring board (PWB) laminate caused by variations in temperature. . . . It appears that **there is some optimal thickness** of these intermetallics, below which a good metallurgical bond has not been achieved, and above which they become a liability to the system.” *Id.*, 52-53 (emphasis added). In the case of a eutectic tin-lead alloy, i.e. 63 Sn / 37 Pb, “[t]he **generally accepted thickness falls in the range of 1 to 5 μm .**” *See, e.g.*, Ex-1019, 403 (emphasis added).

36. As stated above, it was well known that “[t]he adverse effect of intermetallic compounds on solder joint integrity is believed to be attributed to the brittle nature of such compounds and to the thermal expansion property, which normally differ from the bulk solder. The differential thermal expansion could contribute to internal stress development.” *Id.*, 405. Therefore, “[w]hen an appreciable amount of intermetallics is developed along the solder-substrate interface, cracks are often initiated around the interfacial area under stressful conditions.” *Id.*, 403. “The existence of intermetallic compounds has been

observed at or near the interface of the solder and the substrate as well as in the bulk of the solder joint.” *Id.*, 398.

V. THE '001 PATENT

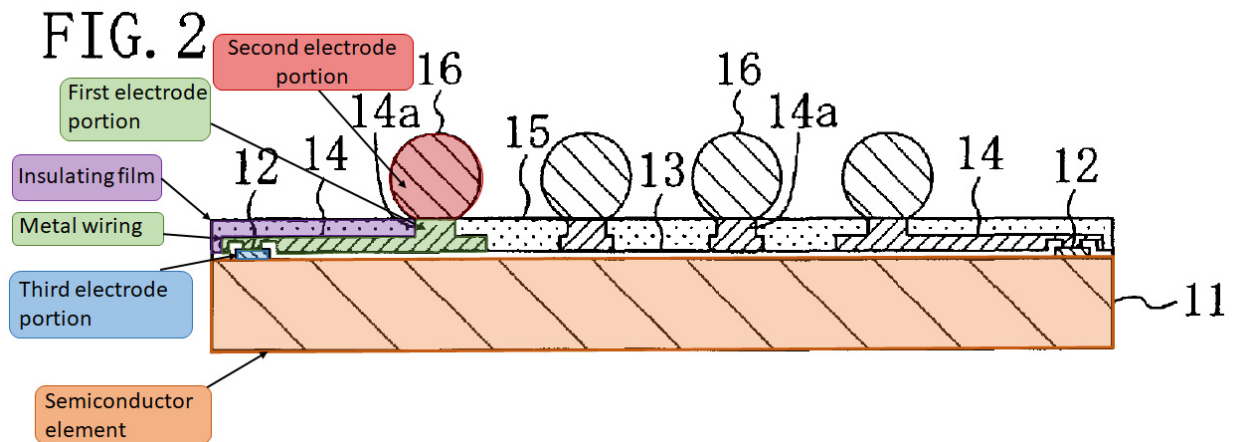
A. The Patent Specification

37. The '001 Patent, entitled “Semiconductor Device Including A Diffusion Layer Formed Between Electrode Portions,” and relates to semiconductor devices built on a semiconductor chip and wired so as to connect with other semiconductor devices. The '001 Patent describes the alleged invention as relating to “a semiconductor device in which a metal wiring is formed so as to be electrically connected to an electrode of a semiconductor element and a part of the metal wiring is used as an external electrode.” Ex-1001, 1:9-13.

38. The '001 Patent describes a semiconductor device that includes a semiconductor element 11, an electrode 12, metal wiring 14, a portion of the metal wiring that acts as an external electrode 14a, an insulating film 15, and an insulating resin layer 17 (not shown in the annotated Figure 1 below). Ex-1001, 11:50-67, Fig. 4. Ball electrodes 16 are mounted on the external electrodes and provide connection to a semiconductor substrate. Ex-1001, 11:67-12:10.

39. The '001 Patent discloses that when the ball electrode is mounted, an alloy layer is formed between the external electrode portion and the ball electrode: “[W]hen the metal wiring contain, e.g., Cu (which is a commonly used metal wiring

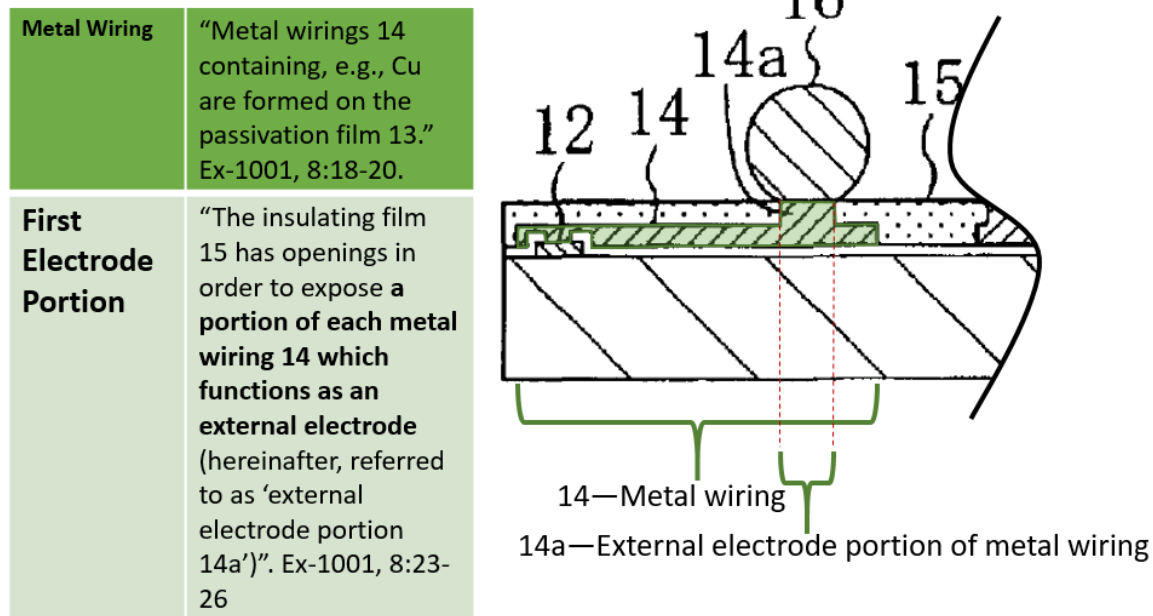
material), Sn contained in solder of the ball electrode diffuses into Cu contained in the metal wiring, whereby a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion.” Ex-1001, 2:59-64. One example of many of these features, specifically those described in the first embodiment of the '001 Patent, are shown in Figure 2, annotated below with labels corresponding to the language used in the '001 Patent's claims. The “diffusion layer” is not shown in the annotated figure below but would be formed between the first and second electrode portion.



40. According to the first embodiment, a semiconductor device includes additional elements and layers formed on a semiconductor element. Ex-1001, 8:13-15. The '001 Patent describes electrodes formed on the semiconductor element. *Id.* Each electrode connects to a metal wiring formed, for example, of copper. Ex-1001, 8:18-21.

41. The metal wiring may have increased thickness at its terminal end (by adding a “metal-material embedded portion”) and the '001 Patent describes this portion of the wiring as being an “external electrode portion,” which is an example of a “first electrode portion.” Ex-1001, 8:21-55. The metal wiring and external electrode portion of the metal wiring are illustrated below in an enlarged, annotated portion of Figure 2.

FIG. 2



42. In one embodiment, the patent discloses, “the thickness of the external electrode portion 14a of the metal wiring 14 (e.g., the total thickness of the non-electrode portion of the metal wiring 14 and the metal-material embedded portion) is preferably in the range of 10 μm to 20 μm .” Ex-1001, 9:36-40.

43. On top of the metal wiring, an insulating film is formed, leaving a hole over the external electrode portion of the metal wiring. Ex-1001, 8:21-27. The '001 Patent explains:

It is preferable that the exposed surface of the external electrode portion 14a is flush with or higher than the surface of the insulating film 15 (in the specification, the term “flush” also includes “approximately flush”). In other words, it is preferable that the thickness of the external electrode portion 14a is equal to or greater than that of the insulating film 15 (in the specification, the term “equal” also includes “approximately equal”). The reason for this is as follows: if the external electrode portion 14a is thinner than the insulating film 15, the ball electrode 16 cannot be mounted to the external electrode portion 14a (that is, the opening of the insulating film 15) without producing a gap therebetween. As a result, sufficient junction between the ball electrode 16 and the external electrode portion 14a cannot be ensured.

Ex-1001, 10:22-35.

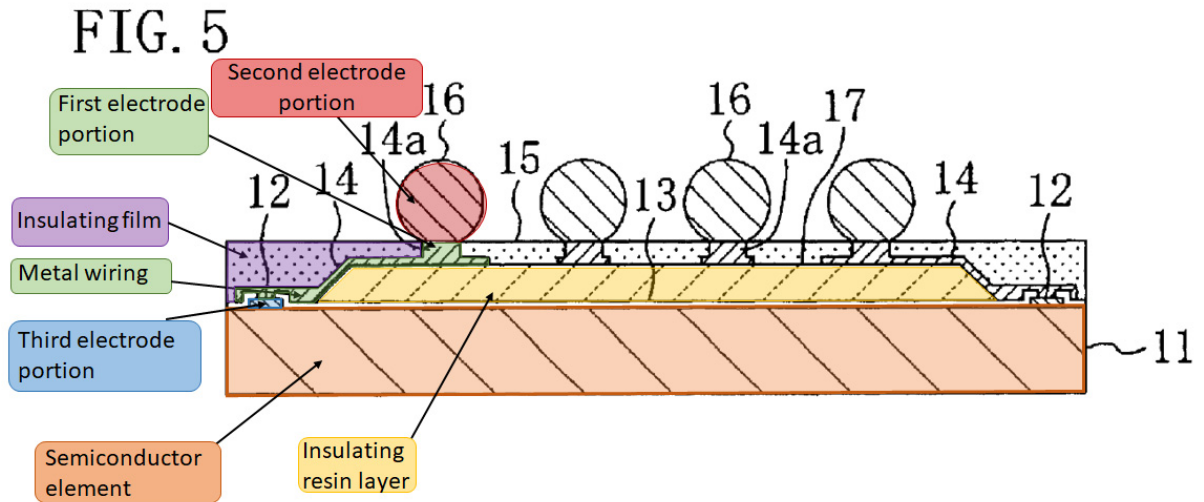
44. Ball electrodes are formed from solder and connected to the external electrodes through the hole in the insulating film. Ex-1001, 8:28-38. The patent explains that when ball electrodes are mounted, tin in the solder “diffuses into Cu contained in the metal wiring,” which forms an alloy having low strength. Ex-1001, 8:63-9:1. However, according to the '001 Patent, the thickness of the external electrode portion is sufficient to prevent the alloy from growing through its entire thickness, thus preserving the strength of the metal wiring. Ex-1001, 9:1-12.

45. The '001 Patent describes another embodiment that includes the same elements as the embodiment described above. Ex-1001, 11:45-49. In addition, this embodiment further includes an insulating resin layer on which the metal wirings are formed. Ex-1001, 11:54-58. The '001 Patent states:

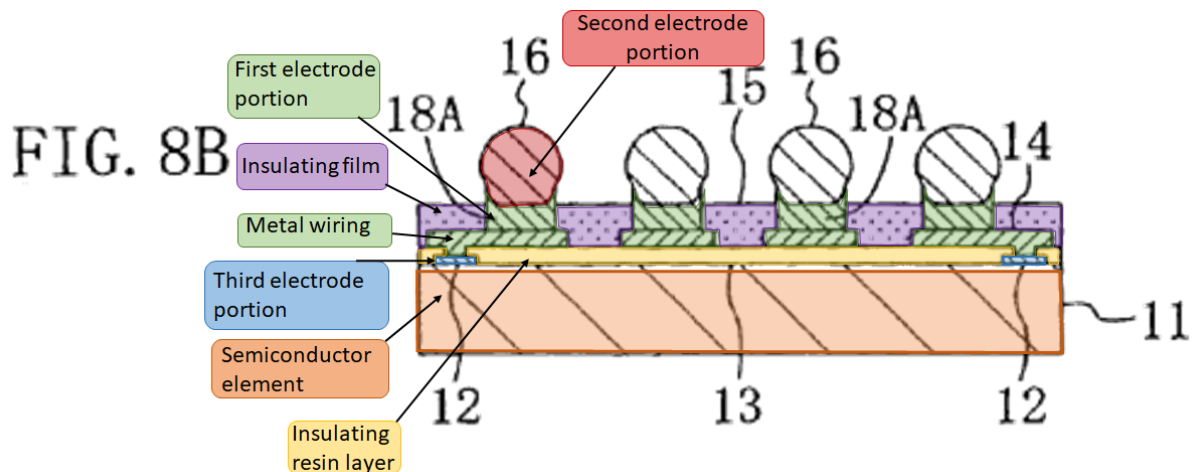
[T]he insulating resin layer 17, which is formed from an epoxy resin having low elasticity or the like, is formed between the metal wirings 14 each electrically connected to a corresponding one of the electrodes 12 of the semiconductor element 11 and the passivation film 13 formed over the surface of the semiconductor element 11.

Ex-1001, 12:17-22. The '001 Patent explains that the insulating resin absorbs stresses created when the temperature is varied to melt the ball electrodes when mounting the semiconductor device to the substrate, preventing breakage of the

metal wiring. Ex-1001, 12:23-35. The insulating resin (along with other key features of the second embodiment) is shown in the annotated Figure 5, below.



46. Figure 8B, annotated below, shows another embodiment described in the '001 Patent.



47. Here, many of the elements are the same as described above (and indicated by the same numerals). However, element 18A is described as a “metal material embedded portion ... (i.e., the external electrode portion of each metal

wiring).” *Id.*, 15:18-24. Additionally, with reference to Figure 8, the patent indicates that the metal wiring may be comprised of two separate layers—a conductive copper layer and a titanium-tungsten layer: “[T]he metal wirings 14 are formed as follows: **a titanium tungsten (TiW) layer and a Cu layer are sequentially formed** on the passivation film 13 by a sputtering method.” *Id.*, 14:26-32.

B. Prosecution History

48. The '001 Patent was filed August 17, 2004 as Application Serial No. 10/919,402, as a divisional of the application that resulted in the U.S. Patent No. 6,784,557, which was filed on December 2, 2002. Ex-1004, 87; Ex-1001, Cover.

49. On November 16, 2004, the Examiner issued an Office Action rejecting all claims as being anticipated under 35 U.S.C. § 102 or rendered obvious under 35 U.S.C. § 103 by U.S. Pub. No. 2002/0108781 A1 (“Mune”). Ex-1004, 99-106. The Examiner found that Mune disclosed a semiconductor device comprising a semiconductor chip, having a first electrode portion comprised of Cu and a second electrode portion/solder ball electrically connected to the first electrode portion and comprised of tin. *Id.* The Examiner further found that Mune disclosed a diffusion layer is formed between the first electrode portion and the second electrode portion that comprised both tin and copper. *Id.* Additionally, the Examiner found that Mune also disclosed a third electrode horizontally spaced from the first electrode

and connected to the first electrode by a metal wiring, and an insulating film formed on the metal wiring, exposing the external electrode and being flush with or lower than the first electrode. *Id.*

50. The Examiner further determined that it would have been obvious to vary the thicknesses of the metal wiring and diffusion layer in order to discover the optimum values for those layers. *Id.* Finally, the Examiner noted that although Mune does not disclose an insulating resin layer, it would have been obvious to incorporate the teachings of the applicant admitted prior art to modify the teaching of Mune to include this layer. *Id.*

51. In response to the Office Action, the applicant amended the application to rewrite one claim and add several new claims. *Id.*, 112-117. The applicant argued that Mune did not in fact disclose the material comprising either the first or second electrode portions that any diffusion layer was formed between the first or second electrode portions. *Id.*, 119.

52. The applicant further argued that the claims were patentable because, *inter alia*, the claimed range of thicknesses for the electrode portion and diffusion layer of 10 μm to 20 μm “has criticality and provides new and unexpected results at ***both*** the upper and lower limit thereof.” *Id.*, 120 (emphasis in original). The applicant argued that electrodes with a thickness less than the lower thickness limit of 10 μm are susceptible to being disconnected, while those with a thickness greater

than the upper thickness limit of 20 μm can lead to pattern deformation among other flaws. *Id.*, 120-122. On April 8, 2005, the Examiner issued a Notice of Allowance for all of the pending claims. *Id.*, 128-132.

VI. SUMMARY OF OPINIONS

53. In preparing this declaration, I have reviewed at least the documents labeled Exhibits 1001-1020 and other materials referred to here. In addition to these materials, I have relied on my education, experience, and my knowledge of practices and principles in the relevant field, e.g., semiconductor design. My opinions have also been guided by my appreciation of how one of ordinary skill in the art would have understood the claims and specification of the '001 Patent around the time of the alleged invention, which I have been asked to assume is the earliest claimed priority date of December 20, 2001.

54. Based on my experience and expertise, it is my opinion that certain references teach or suggest all the features recited in Claims 1-18 of the '001 Patent, as explained in detail below. Specifically, it is my opinion that:

- Claims 1-4, 6-8, 10-13, and 15-17 are disclosed by Japanese Unexamined Patent Application Bulletin No. JP-2001-053184-A ("Furuya") in view of Japanese Patent Application Publication No. 2000-260894, published September 22, 2000 ("Takizawa");-

- Claims 5 and 14 are disclosed by Furuya in view of Takizawa and further in view of the knowledge of a POSA (as evidenced by PCT Application Number PCT/JP00/01550, Publication Number WO00/55910 (“Yaguchi”)); and
- Claims 9 and 18 are disclosed by Furuya in view of Takizawa and further in view of the knowledge of a POSA (as evidenced by U.S. Patent No. 6,181,010 to Nozawa (“Nozawa”))

VII. THE PRIOR ART TEACHES OR SUGGESTS EVERY STEP AND FEATURE OF THE CHALLENGED CLAIMS OF THE '001 PATENT

A. Overview Of The Prior Art References

1. Japanese Unexamined Patent Application Bulletin No. JP-2001-053184-A (“Furuya”) (Ex. 1006)²

55. Furuya was published by the Japanese Patent Office on February 23, 2001, as Patent Application Publication No. 2001-52184. Furuya was not considered during the prosecution of the '001 Patent. Furuya discloses a semiconductor device that includes an electrode that has been formed on a semiconductor element. Ex-1006, [0016]. A wiring pattern connects the electrode of the semiconductor element to a metal post, for external connection. *Id.* Furuya also discloses an insulation layer, formed on top of the wiring pattern in a manner to

² Throughout this Declaration, I refer to the certified translation of Furuya.

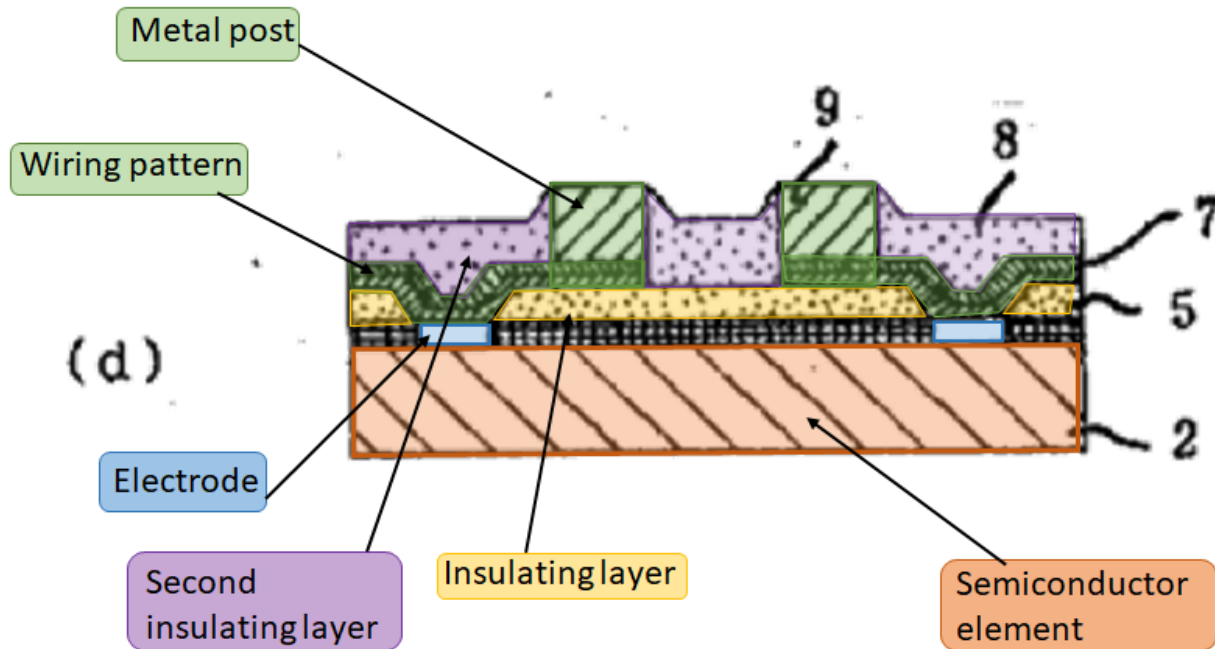
cover the side face of the metal post excluding the tip surface of the metal post.

Id.

56. Furuya recognizes that in the prior art the metal post interacts with the solder, specifically “the connection between the metal post 69 and the outside (for example, the mounting board) is made by thermocompression bonding using solder but at this time, if high temperatures ... are reached some of the metal post will dissolve and dissipate in the solder.” *Id.*, [0007]. Furuya also notes that in prior art “the connection strength between the metal post 69 and wiring pattern 67 was insufficient” and thus thermal stresses could pose reliability problems because they could lead to the formation of “cracks” and “wire breakage.” *Id.*, [0008]. Such thermal stresses are developed due the difference in thermal expansion coefficient between the semiconductor substrate and the board. *Id.*

57. Furuya is directed to improving the connection strength between a metal post and a wiring pattern and improving the reliability of the electrical connection with the outside, i.e. with a printed circuit board. Ex-1006, [0015]. Furuya teaches accomplishing this objective by first forming electrodes on a semiconductor element, which are exposed by holes formed in a first insulating layer. Next, on the first insulating layer a wiring pattern is formed that connects the electrodes with metal posts, which are formed at predetermined locations on the wiring pattern. A second insulating layer is then formed on top of the wiring

pattern, having a thickness less than that of the metal post and formed in a manner that covers the side faces of the metal post but it does not cover the top surface of the metal posts. Ex-1006 [0016], [0017], [0027]. I have annotated Figure 4(d) below to illustrate these features.

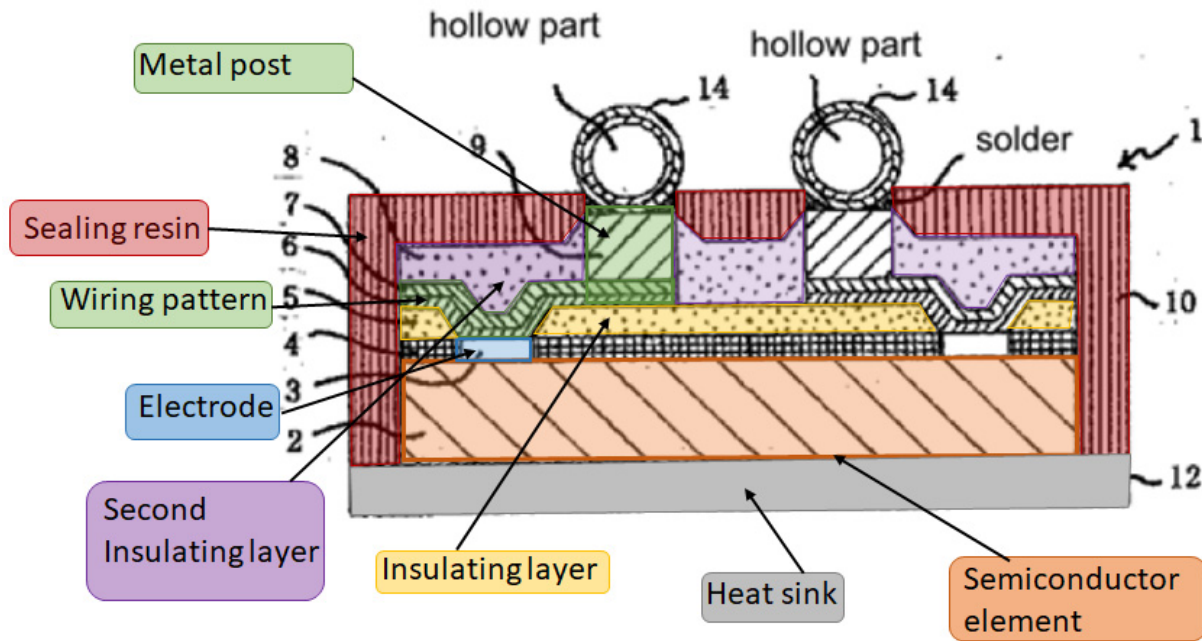


58. Furuya optimized the height of the second insulating layer 8 and the metal post 9 so the connection strength between the metal post 9 and the wiring pattern 7 is improved so disconnection between the metal post 9 and the wiring pattern 7 can be prevented. Ex-1006 [0028]. Specifically, Furuya teaches “...the height of the second insulating layer 8, excluding the location where this covers the side face of the metal post 9, is at a position lower than the height of the tip surface of the metal post 9.” Ex-1006 [0017], [0029]. Moreover, Furuya teaches the complete removal of the second insulating layer 8 from the tip surface of the metal

post for enabling a connection to the outside, i.e. a “printed board.” Ex-1006, [0046]-[0048].

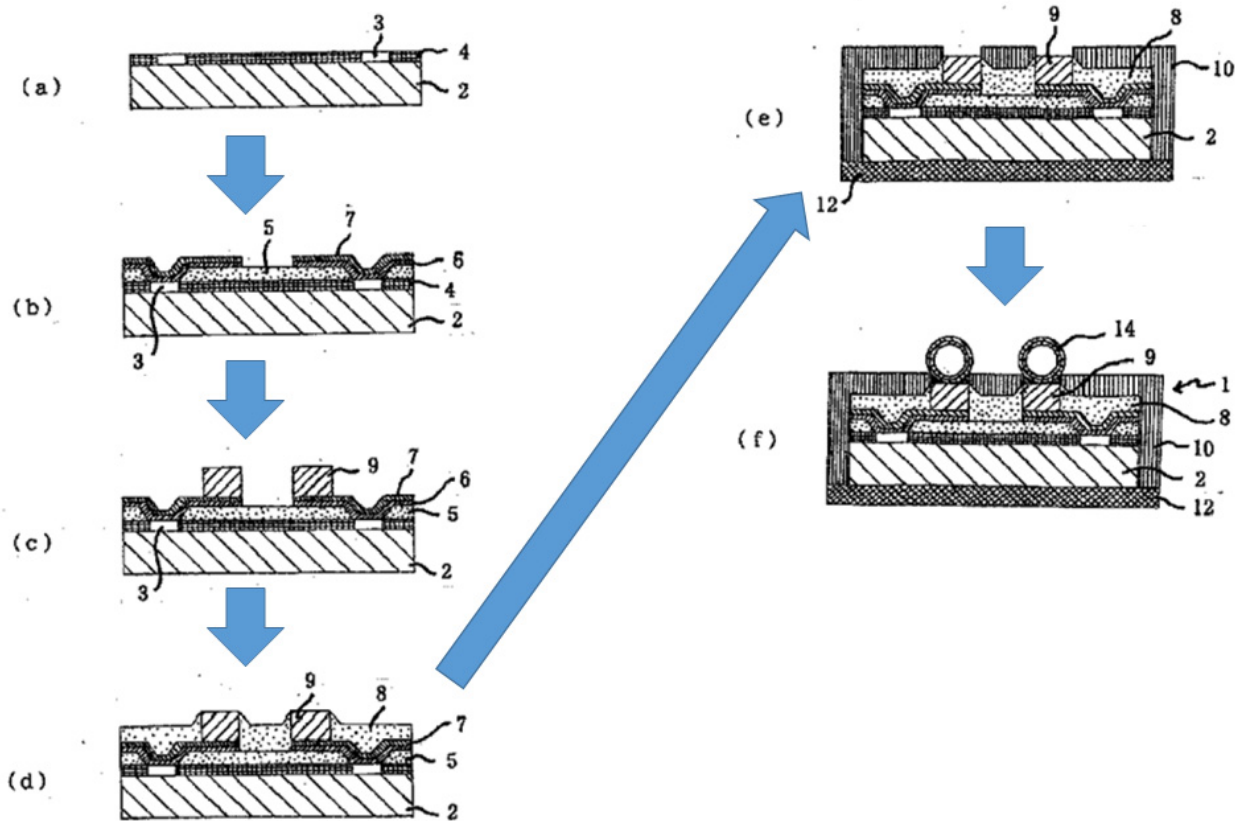
59. Furuya, also teaches and describes additional elements having additional benefits including a heat sink for heat dissipation and a sealing resin for preventing moisture absorption. Specifically, Furuya describes that if a heat sink is attached to the back face of the semiconductor element after dicing excellent heat dissipation can be achieved. Ex-1006 [0064]. Moreover, Furuya describes that sealing resin added after dicing protects the semiconductor device from moisture absorption; the resin sealing excludes the tip surface of the metal post. *Id.* I have annotated Figure 1 of Furuya below to show all of the elements incorporated into the final device; I have labelled these elements the same way that are referred by Furuya.

[FIG. 1]



60. In addition to describing the final semiconductor device, Furuya explains each of the intermediate states in the manufacturing pathway to the final device. I have annotated a sequence of Figure 4(a)-(f) below.

FIGURE 4



61. As shown above, “FIG. 4 (a) is a semiconductor element 2 ... which is incorporated into a semiconductor device 1 [with] [e]lectrode 3 made of aluminum [that is] formed on the semiconductor element 2 with a silicon wafer as a substrate.” Ex-1006, [0051]. In Figure 4(b), a photosensitive polyimide is applied and formed into a first insulating layer 5, having a film thickness of approximately 10 μm followed by a TiN layer (6) and a Cu layer 7, which are formed into a wiring pattern using a photoetching method. *Id.*, [0052]. Next, in Figure 4(c), “a metal post 9 [is] formed on the wiring pattern 7.” In Figure 4(d), another insulating layer, i.e. “second insulating layer 8”, is formed over the entire chip. Furuya teaches that

the second insulating layer exposes the top face of the metal post but covers the side face of the metal post and at other locations is lower than the top face of the metal post. *Id.*, [0053].

62. Moreover, Furuya teaches several methods that can be used to remove the second insulating layer 8 from the tip surface of the metal post including photolithography, laser, dry etching, reverse sputtering or the like. Ex. 1006, [0048]. Furuya, describes that this removal step is performed for the purpose of connecting to the outside, i.e. “printed board,” and after the removal of the insulating film from the tip region of the metal post, the device formed is at the state depicted in Figure 4(d). *Id.*, [0046]

63. Furuya explains that “after producing 4(d), dicing was performed on the silicon wafer ... so as to divide this into individual semiconductor elements,” after which, resin molding is performed with a sealing resin in a manner that exposes the top face of the metal posts, as shown in Figure 4(e). *Id.*, [0054]. In Figure 4(f), “the external connection terminal is provided on the metal post to produce the semiconductor device 1.” *Id.*, [0055]. Throughout this petition, I have relied primarily on Figure 4(d), as most of the claim limitations correspond to the pre-diced semiconductor device; however, as discussed above, each of these elements is also shown in the final device depicted by Furuya in Figure 4(f) (and Figure 1).

64. Returning to the specific layers described in Furuya, Furuya teaches that the metal wiring pattern should be formed of a material having good conductivity, such as copper, silver, or aluminum. Ex-1006, [0035]. Furuya teaches that if copper is used for the material of the wiring pattern, “it is preferable to form a metal barrier layer 6 made of a TiW alloy...as an undercoat layer and then form the wiring pattern 7 on the metal barrier layer 6.” *Id.* Furuya teaches that the metal posts are formed on the wiring pattern and are also made of copper. Ex-1006, [0053].

65. Furuya also discloses the thicknesses of these layers. For example, one embodiment notes that “a 2000 Å [0.2 μm] thick TiN layer and a 5000 Å [0.5 μm] thick Cu layer were sequentially laminated on the first insulating layer 5 by sputtering” to produce the resulting metal barrier layer and wiring pattern discussed above. Ex-1006, [0052]. Similarly, Furuya discloses that the metal posts are formed to a height of 15 μm, in addition to the wiring layer on which they are formed. Ex-1006, [0053]. By contrast, “the second insulating layer 8 was given a film thickness of 10 μm, so as to be lower than the top face of the metal post.” *Id.*

66. When the metal post is joined to the solder ball by reflow, Furuya explains that a diffusion layer forms as a result of the high-temperature joining process described by the prior art:

[I]f high temperatures of, for example, 180°C to 250°C are reached, **some of the metal post 69 will dissolve and dissipate in the solder.** In consideration for this dissolution and dissipation, the height of the metal post 69 is generally approximately 3 μm to 50 μm .

Ex-1006, [0007]. A POSA would have understood that this dissolution of the metal post into the solder results in a diffusion layer.

67. Although Furuya teaches this diffusion layer with respect to Figure 6, which is described as prior art, a POSA would have understood that the same principle would result in a diffusion layer forming between the external electrical connection 14 and the metal post 9 in Figure 1 as well, considering that similar materials and techniques are used to connect the metal post and mounting board. For example, as described in the following paragraphs, Furuya discloses a soldering process in which a molted eutectic solder containing tin is brought in direct contact with a copper metal external electrode. Ex-1006, [0043]-[0044], [0055]-[0056]. In view of what the '001 Patent describes as conventionally known (summarized in the Technological Background section above), when **solder containing tin (Sn) is connected in a molten state to a copper electrode, the tin and copper form a diffusion layer.** Ex-1001, 2:12-29. Accordingly, a POSA would have understood

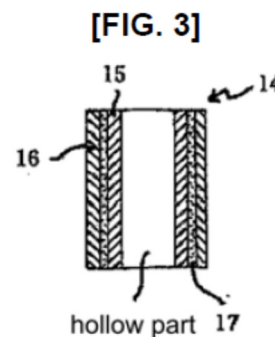
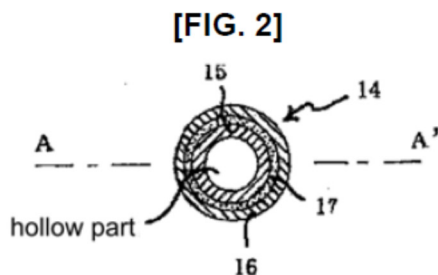
that Furuya also discloses a process in which a diffusion layer of Sn-Cu is formed.

Furuya, however, does not state the thickness of such a diffusion layer.

68. More specifically, Furuya discloses that the external connection terminal 14, shown in both Figure 1 and Figure 4f (and which is equivalent to a solder ball as described in [0006]), performs the “fixing,” i.e., bonding, and provides the external electrical link, for example with a mounting board:

Next, the semiconductor device 1 of the present invention performs fixation and electrical connection with the outside (for example, to a mounting board) by way of the external connection terminal 14, and an electroconductive material 16 is provided on the surface of the support 15 comprised by the external connection terminal 14.

Ex-1006, [0043]. The structure of the external terminal 14 of Furuya is depicted schematically in Figure 2 and Figure 3 of Furuya, shown below.



69. Furuya further explains that:

The electroconductive material 16 must perform fixation with the outside and allow for electrical connection with the outside. Conductive materials 16 that satisfy such conditions are preferably selected from among the following (1) to (3):

- (1) a dispersion of graphite, carbon or metal fine particles;
- (2) gold, silver, copper, aluminum or nickel alone, or an alloy containing two or more of said metals; and
- (3) a low melting point alloy having tin or lead as a principal component.**

Ex-1006, [0043] (emphasis added). Furuya further teaches that:

[S]older alloy having tin or lead as a main component is preferable from the viewpoint of manufacturing costs and the like. Eutectic solder or high melting point solder with an increased lead ratio can suitably be used as the solder alloy

Ex-1006, [0044].

70. In the preferred embodiment described by Furuya, a eutectic alloy was used and the bonding or soldering process was performed at 220°C for 8 seconds.

See Ex-1006, [0055]-[0056]. A POSA would have known that a commonly used

60/40 tin-lead solder melts at 188°C while the eutectic 63/37 tin-lead solder melts at 183°C. Thus, the tin-containing solder will be in the molten state and in contact with the copper metal post during the soldering process, which is performed at 220°C. Therefore, based on Furuya's technical disclosures and the prior art knowledge at the time of Furuya's invention, a POSA would have readily recognized that Furuya discloses the formation of a diffusion layer.

2. Japanese Patent Application Publication No. 2000-260894, published September 22, 2000 ("Takizawa") (Ex. 1015)³

71. Takizawa discloses a semiconductor device with a semiconductor chip 1 that includes an electrode 12, where the electrode is connected to a solder ball 11 through a wiring part 2.

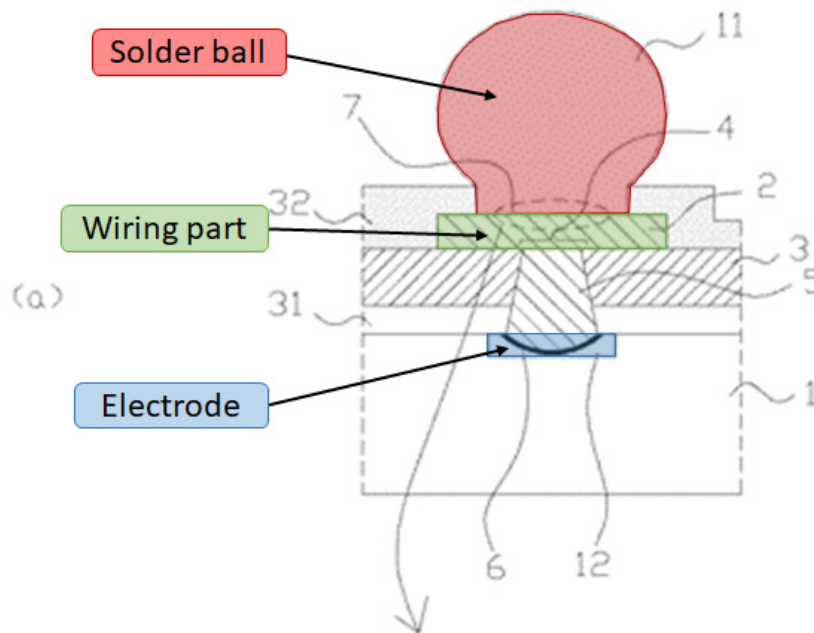
As illustrated in FIG. 1(a), the semiconductor device according to the present embodiment has the wiring part 2 containing Cu that is connected to a semiconductor chip 1 and the solder ball 11 containing the solder ball 11 containing Sn that is connected to the wiring part 2.

Ex-1015, [0034].

³ Throughout this Petition, I refer to the certified translation of Takizawa.

72. Takizawa explains that the wiring part 2 contains copper, while the solder ball contains tin. *Id.* I have annotated Figure 1A below to show these features as described in Takizawa.

[FIG. 1]



73. Takizawa also discloses a Sn-Cu alloy layer formed by diffusion between its wiring 2 and solder ball 11 (Figs. 2 and 8, reproduced below). Ex-1015, [0020].

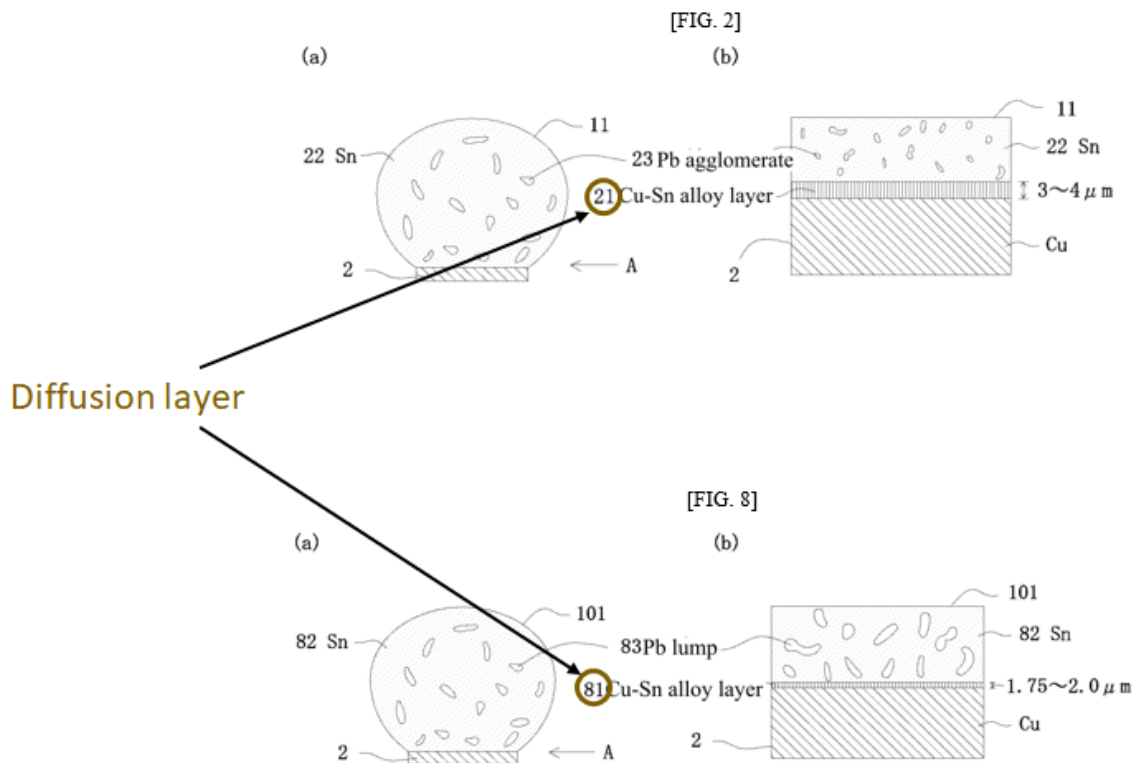
As illustrated in FIG. 1(b), a strong Cu-Sn alloy layer is formed on the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 portion on which the solder ball 11 is placed on the wiring part 2. As

described above, detachment of the solder ball 11 caused by fractures and cracks can be reduced by reducing the occurrence of fractures and cracks near the bonding part by providing the Cu-Sn alloy layer on the bonding part between solder ball 11 and the wiring part 2. As a result, productivity of the semiconductor device can be improved, and yield can be further increased.

Id., [0035].

74. Takizawa teaches a diffusion layer between 1.87 μm and 4 μm thick.

Id., [0035], [0040]. Figs. 2B and 8B show the diffusion layer 21/81.



75. Takizawa discloses that when the Cu-Sn alloy layer has a “sufficient thickness” it can “prevent detachment of the solder ball” thereby “increas[ing] the strength of the bonding parts” and “reduc[ing] the occurrence rate of fractures and cracks near the bonding part.” *Id.*, [0020]. Takizawa also discloses an optimal thickness range between 1.87 μm and 4 μm . *Id.*, [0035], [0040].

76. Moreover, Takizawa discloses a method of manufacturing a semiconductor device with a stronger bond between the solder ball and the wiring part by:

disposing a solder ball containing Sn on a land provided
on the wiring part; and maintaining an inert environment
or a reducing environment at a temperature above the
melting point of the solder ball for a predetermined
period of time.

See id., [0019].

77. Takizawa discloses a variety of solder ball materials that contain Sn. For example, the solder balls in the two preferred embodiments contain tin as a primary component. *See id.*, [0033], [0040]-[0042].⁴ Further, Takizawa discloses that a variety of materials, including copper, can be paired with Sn and used for a solder ball. *See id.*, [0035], [0044] (“**as long as the material contains Sn**, and can, for example, have Sn-Ag alloy or Sn **as a main component**, and a Pb free solders or the like containing Ag, **Cu**, Zn, Cd, Ni, S, As, or Bi can be used.”).

3. PCT Application Number PCT/JP00/01550, Publication Number WO00/55910 (“Yaguchi”) (Ex. 1011)⁵

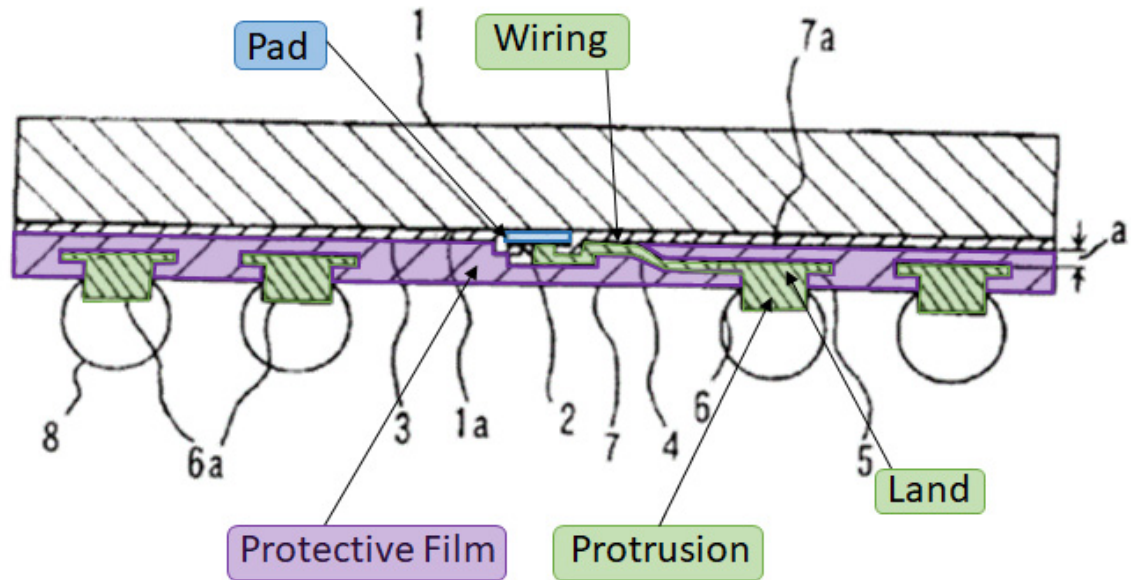
78. Yaguchi was filed on March 14, 2000 and published by the World Intellectual Property Organization on September 21, 2000 as PCT Publication No.

⁴ Note, a POSA would have recognized that Takizawa’s example two mistakenly refers to Sn-Cu as the solder material. In context, a POSA would have recognized that this should read Sn-Pb eutectic, which has a melting point of 183° C.

⁵ Throughout this Declaration, I have referred to the certified translation of Yaguchi.

WO00/55910. Yaguchi describes a semiconductor device that includes a semiconductor element, a pad, conductive wiring connected to a land, a protrusion provided on the land and an external terminal joined to the protrusion. Ex-1011, 9:5-19. Yaguchi further explains that there are various passivation and insulation layers, including a protective film formed on the conductive wiring, land, and protrusions. *Id.* However, Yaguchi teaches that the protrusion is not completely covered by the protective film. Rather, “[a] part of the protrusion 6 protrudes through the protective film 7 and this protruding part 6a is joined to the external terminal 8.” *Id.* These elements are illustrated in Figure 1(a), below where the semiconductor element 1, pad 2, conductive wiring line 4, land 5, protrusion 6, and protective film 7. I have annotated Figure 1(a) below to reflect these labels as found in Yaguchi:

FIG. 1 (a)



4. U.S. Patent No. 6,181,010 to Nozawa (“Nozawa”) (Ex. 1012)

79. Nozawa was filed on March 19, 1999 as PCT/JP99/01410 with a U.S. Application number 09/424,484. Nozawa describes a semiconductor device that includes many of the conventional components described above with reference to the other prior art references. For example, Nozawa describes the semiconductor device comprising a semiconductor chip having electrodes with an interconnect layer connected to the electrodes. Ex-1012, 1:51-56. Nozawa further describes a conducting layer formed on the interconnect layer, an underlying metal layer formed on the conducting layer, a bump formed on the underlying metal layer, and

a resin layer, or insulating protection layer, formed around the conducting layer.

Ex-1012, 1:56-64; 4:25-5:20.

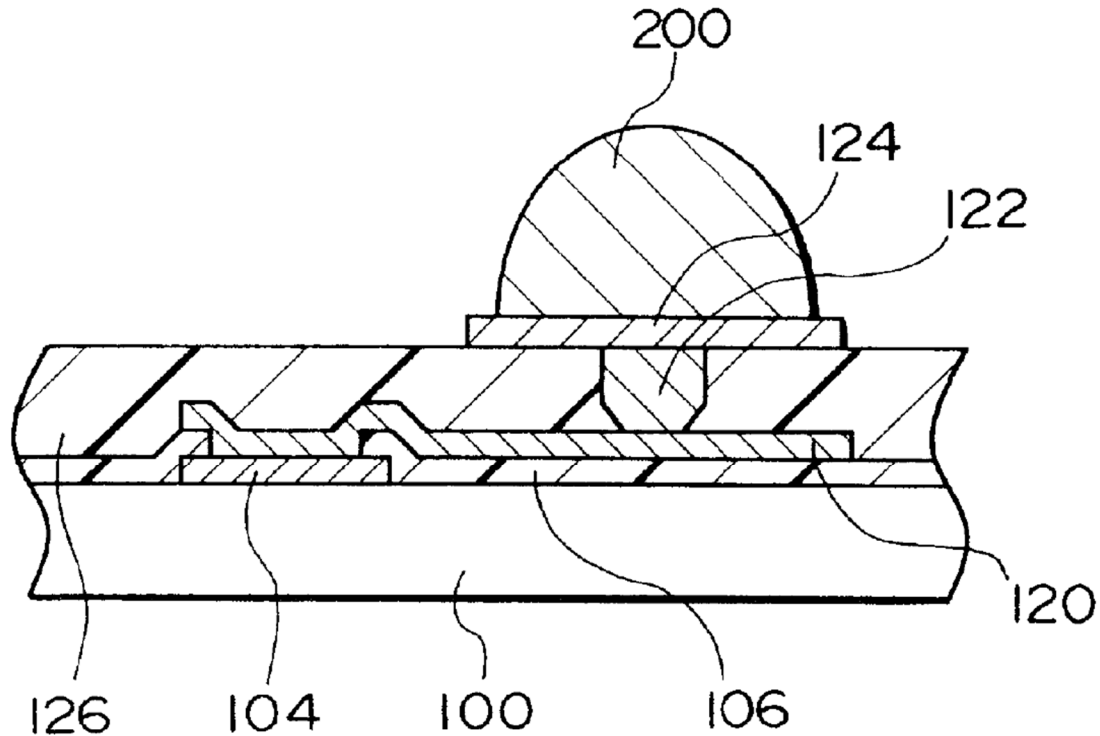
80. Nozawa teaches that its device allows for a reliable connection to be formed directly between the semiconductor device and the substrate resulting in electronic instruments that are more compact and lightweight. Ex-1012, 1:41-48.

Nozawa describes these features in relation to Figure 1 as follows:

The semiconductor chip 100 comprises a plurality of elements such as gates (not shown in the drawings). On the semiconductor chip 100, a plurality of electrodes 104 are formed. On the surface of the semiconductor chip 100 on which the electrodes 104 are formed, an insulating layer 106 is formed, avoiding the area where the electrodes 104 are provided. The insulating layer 106 may be formed as a silicon oxide film. It should be noted that, as other examples, a silicon nitride film, or polyimide, or the like may be used. To the electrodes 104 are connected an interconnect layer 120 is connected, and the interconnect layer 120 extends into a region avoiding the electrodes 104. The interconnect layer 120 is formed on the insulating layer 106.

Ex-1012, 4:33-45. Figure 1 below illustrates these elements.

FIG. 1



81. Nozawa also teaches the manner in which the semiconductor device, described above, is connected to the substrate:

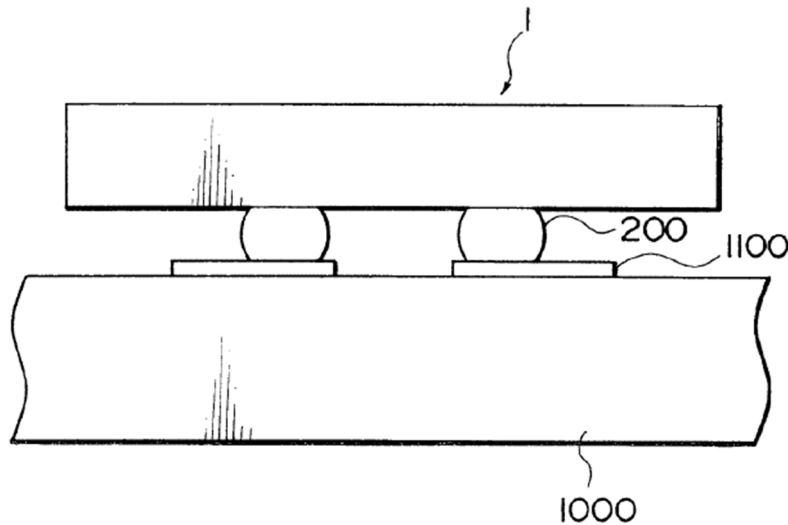
In FIG. 9 is shown a circuit board 1000 on which is mounted this embodiment of the semiconductor device 1.

For the circuit board 1000 is generally used an organic substrate such as a glass epoxy substrate or the like. On the circuit board 1000, an interconnect pattern 1100 of for example copper is formed to constitute a desired circuit,

and by mechanical connection of the interconnect pattern thereof to the bumps 200 forming the external electrodes of the semiconductor device 1, electrical connection is achieved.

Ex-1012, 8:30-44. Figure 9 below illustrates the connection between semiconductor device 1 and circuit board 1000.

FIG. 9



B. Ground 1: Furuya In View Of Takizawa Renders Obvious Claims 1-4, 6-8, 10-13, and 15-17

1. Reasons To Combine Furuya And Takizawa

82. A POSA would have been motivated to improve the semiconductor device disclosed in Furuya by incorporating Takizawa's teaching to improve the

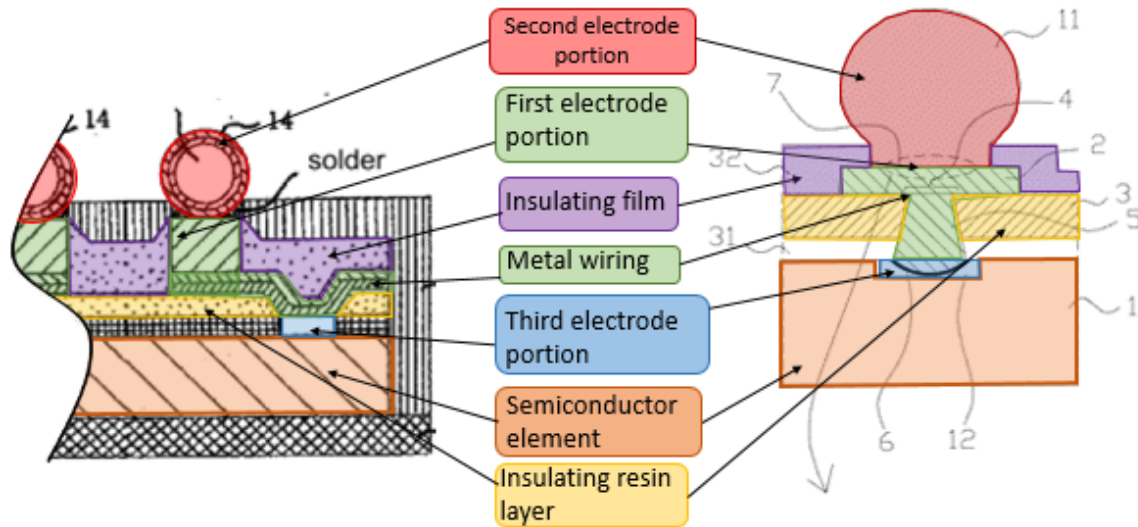
connection reliability between a solder ball and a metal wire by forming a copper-tin diffusion layer between the wiring and the solder ball in the optimum thickness range of 1.87 μm to 4 μm . Both Furuya and Takizawa are in the same field of technology and were filed around the same time. Furuya and Takizawa are directed toward very similar semiconductor devices that operate in a similar manner.

83. For example, Furuya teaches a semiconductor device that has “a semiconductor element, with an electrode, which has been formed on the semiconductor element, ... a wiring pattern, which is connected with the electrode of the semiconductor element, is formed on the first insulating layer; a metal post for external connection is formed on the wiring pattern; [and] a second insulating layer, which is in close contact with the wiring pattern.” Ex-1006, Abstract. Similarly, Takizawa describes a “semiconductor device... [that] has a wiring part 2 containing copper connected to a semiconductor chip, and a solder ball 11 containing tin bonded to the wiring part 2, wherein a Cu-Sn alloy layer 21 with a thickness of approximately 1.87 μm or more is formed on the bonding part of the solder ball 11 and the wiring part 2.” Ex-1015, Abstract. Thus, both references are

directed to very similar semiconductor devices, as shown in the annotated figure below.⁶

Furuya Figure 1

Takizawa Figure 1(a)



84. Furthermore, Furuya “is directed to providing a highly reliable chip-size package type semiconductor device in which the connection strength between the metal post and the wiring pattern is high and the reliability of the electrical connection with the outside is high...” Ex-1006, [0015]. Likewise, Takizawa is directed toward improving the reliability of electrical connections between the metal wiring and the external electrode or solder ball. Ex-1015, [0006]-[0010]. Takizawa’s invention “reduce[s] detachment of the solder ball caused by breaking

⁶ A POSA would have recognized that Takizawa and Furuya use different terminology to refer to elements that are the same. For ease of reference, I have used labels corresponding to the language in the claims of the '001 Patent.

or cracking in order to be able to reduce the occurrence of fractures and cracks near the bonding part by providing a wiring part containing copper connected to a semiconductor chip, and a solder ball containing tin bonded to the wiring part [thereby] enhance increas[ing] the reliability of the bonding part and increase[ing] the productivity of the semiconductor device.” Ex-1015, [0010].

85. Thus, both Furuya and Takizawa address the same problem of forming reliable electrical connections that can withstand the stress or strain on the semiconductor device due to differences in thermal expansion coefficients between the silicon material of the semiconductor device and the material on which the printed circuit board is made. *See, e.g.*, Ex-1006, [0008]; Ex-1015 [0006]-[0010].

86. A POSA would have been motivated to combine Furuya with a reference such as Takizawa that teaches that there are advantages gained by employing a diffusion layer of a specified thickness, i.e., between 1.87 μm and 4 μm thick. Takizawa examined the relationship between the thickness of the Cu-Sn alloy layer and the connection reliability of the resulting semiconductor device, finding:

Forming the Cu-Sn alloy layer with a thickness of at least 1.87 or more was preferable in order to prevent detachment of the solder ball 11. Thereby, the occurrence ratio of fractures and cracks in the vicinity of the bonding

part could be reduced since strength of the bonding part between the solder ball 11 and the wiring part 2 was strengthened by forming the Cu-Sn alloy layer with sufficient thickness in the vicinity of the bonding part. Thereby, a device with favorable yield could be provided since the occurrence of defective parts caused by the occurrence of fractures and cracks could be reduced.

Ex-1015, [0040]. Accordingly, combining the thicker alloy layer of Takizawa to the semiconductor of Furuya would have been obvious to a POSA and would have led a POSA to conclude that the combination would yield a predictable and successful result.

2. Claim 1

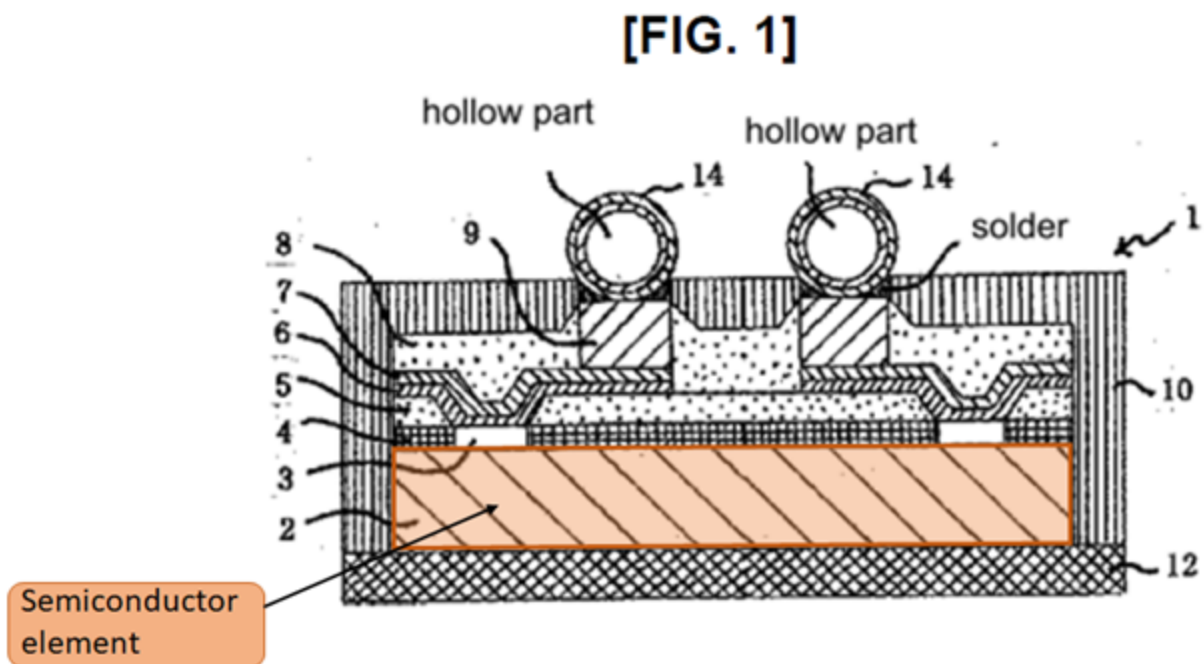
a) [1 pre]: A semiconductor device, comprising

87. Furuya discloses the preamble because it “relates to [] **semiconductor devices** ... in which a wiring layer is formed on a semiconductor element.” Ex-1006, [0001]. For example, the title of Furuya is “Semiconductor Device and Method of Manufacturing Same.” Ex-1006, Cover. The abstract similarly notes that the means for solving the problem is “[a] semiconductor device characterized in that ...” *Id.*

88. In view of the foregoing, persons of ordinary skill in the art would have understood that Furuya discloses “a semiconductor device.”

b) [1 a]: a semiconductor element

89. Furuya discloses that its semiconductor device includes at least a semiconductor element, which forms the base on which other elements and layers are formed. For example, Furuya discloses that “the semiconductor device is characterized in that a first insulating layer...is formed on the passivation film, which has been formed **on a semiconductor element.**” Ex-1006, [0016]. *See also* Ex-1006, [0001], [0027], Fig. 4(a). The semiconductor element is depicted as numeral 2 in Figure 4(d), annotated below. Ex-1006, [0027] (“semiconductor element 2”).



90. Furuya explains that the “semiconductor element 2 [is] produced by conventionally known means, which is incorporated into a semiconductor device 1 of the present invention.” Ex-1006, [0051]. *See also* Ex-1006, [0037] (the semiconductor element 2 ... is formed of silicon or the like.”).

91. In view of the foregoing, persons of ordinary skill in the art would have understood that Furuya discloses a semiconductor device that comprises “a semiconductor element.”

c) **[1 b]: a first electrode portion formed on the semiconductor element, said first electrode portion comprising a first metal component**

92. Furuya discloses a semiconductor device that includes a first electrode portion formed on the semiconductor element because it teaches a metal post formed on top of a portion of the wiring pattern, which in turn is formed on top of a metal barrier layer, all of which collectively act as the first electrode portion and serve to create external electrical connections. For example, Furuya describes the method for forming various layers on the semiconductor device that result in the claimed structure as follows:

[A] step of ... **forming a wiring pattern 7** having a predetermined shape, which is connected with the electrodes 3, on the first insulating layer 5, so as to produce [the] state in FIG. 4 (b); **a step of forming a metal post 9**

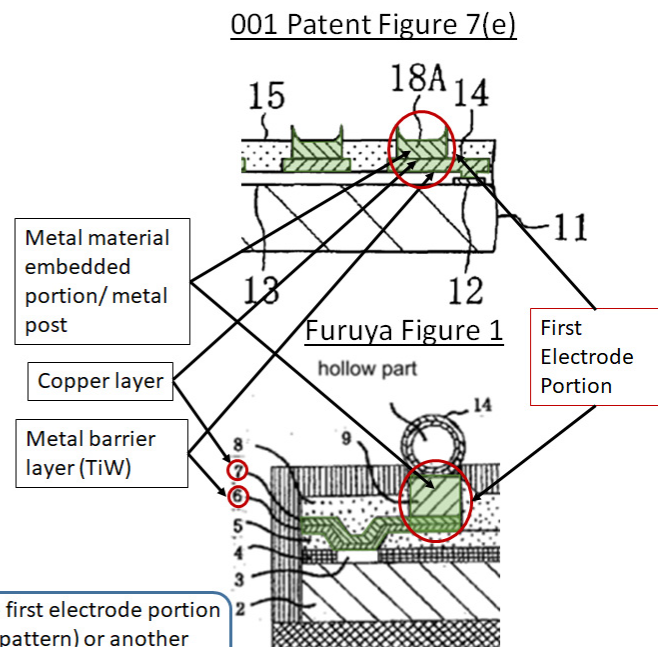
**for external connection, in a predetermined position of
the wiring pattern 7,...** Note that, in the example in FIG.
4, prior to forming the wiring pattern 7, **the metal barrier
layer 6 is formed as an undercoat layer.**

Ex-1006, [0046]. *See also* Ex-1006, [0052] - [0053] (“Next, metal posts 9 made of copper (height 15 μm) were formed on the metal wiring pattern 7.”).

93. The combination of three elements—the metal post, wiring pattern, and metal barrier layer—as the claimed “first electrode portion” parallels the discussion of this same element in the ’001 Patent as shown in the figure and citations below.

Parts of the first electrode portion	
Furuya	001 Patent
Metal Post 9	“[M]etal-material embedded portions 18A are formed by the metal film 18 ...[a]s a result, the total thickness of the metal-material embedded portion 18A and the metal wiring 14 located thereunder is greater than the thickness of the portion of the metal wiring 14 other than the external electrode portion (i.e., the non-electrode portion of the metal wiring 14).” Ex-1001, 14:66-15:9
Metal barrier layer 6	“More specifically, the metal wirings 14 are formed as follows: a titanium tungsten (TiW) layer and a Cu layer are sequentially formed on the passivation film 13 by a sputtering method.” Ex-1001, 14:28-32
Copper layer 7	

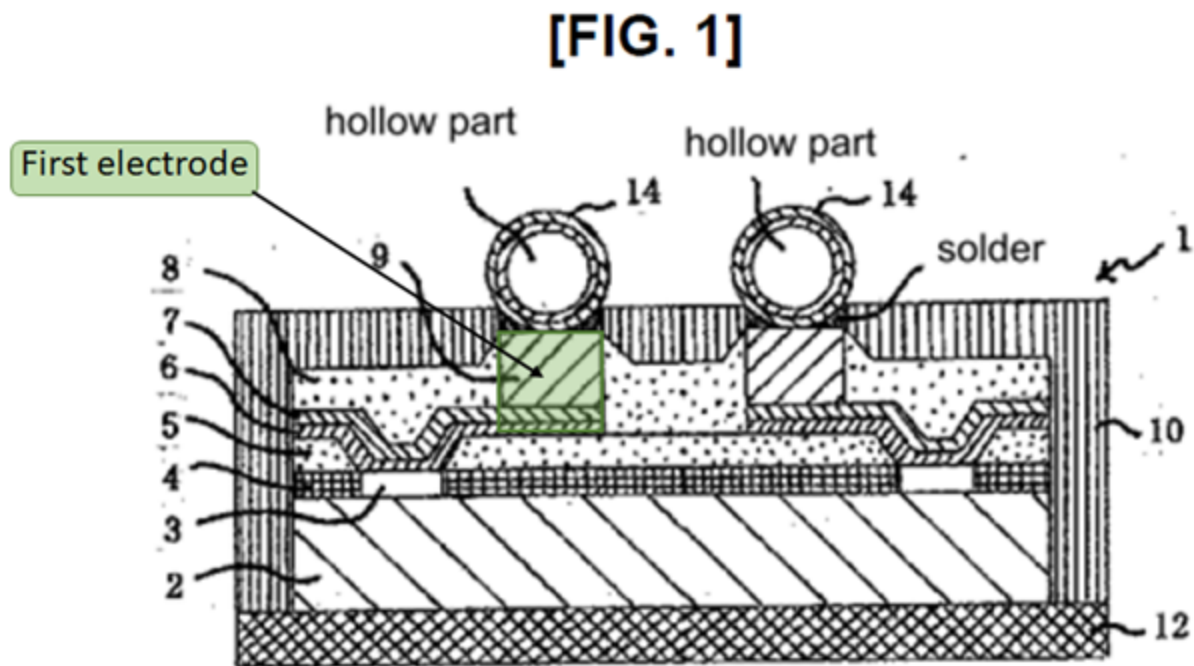
Metal Component: As described above, all portions of the first electrode portion in Furuya are comprised of copper (metal post and wiring pattern) or another metal such as TiW (metal barrier layer). Ex-1006, [0035], [0052]-[0053].



94. Furuya also teaches that the first electrode, described above, is used for external connections:

Then, a **wiring pattern 7 (wiring layer)** that is **connected with** the electrodes 3 is formed on the first insulating layer 5, **and metal posts 9 for external connection**, having a height of approximately 3 μm to 50 μm , are formed at predetermined positions on the wiring pattern 7.

Ex-1006, [0027]. *See also* Ex-1006, [0016], [0035]. Figure 1, annotated below, depicts the first electrode portion as a combination of element 9 “metal post” and a portion of element 7 “wiring pattern.”



95. The first electrode portion is comprised of a first metal component as inasmuch as Furuya discloses that the wiring pattern and the metal post are comprised of copper, while the metal barrier layer is also disclosed to be a metal, such as TiW. Thus, Furuya explicitly discloses that the first metal component comprises of copper material. Ex-1006, [0035], [0052]-[0053].

96. In view of the foregoing, persons of ordinary skill in the art would have understood that Furuya discloses or renders obvious a semiconductor device that comprises “a first electrode portion formed on the semiconductor element, said first electrode comprising a first metal component.”

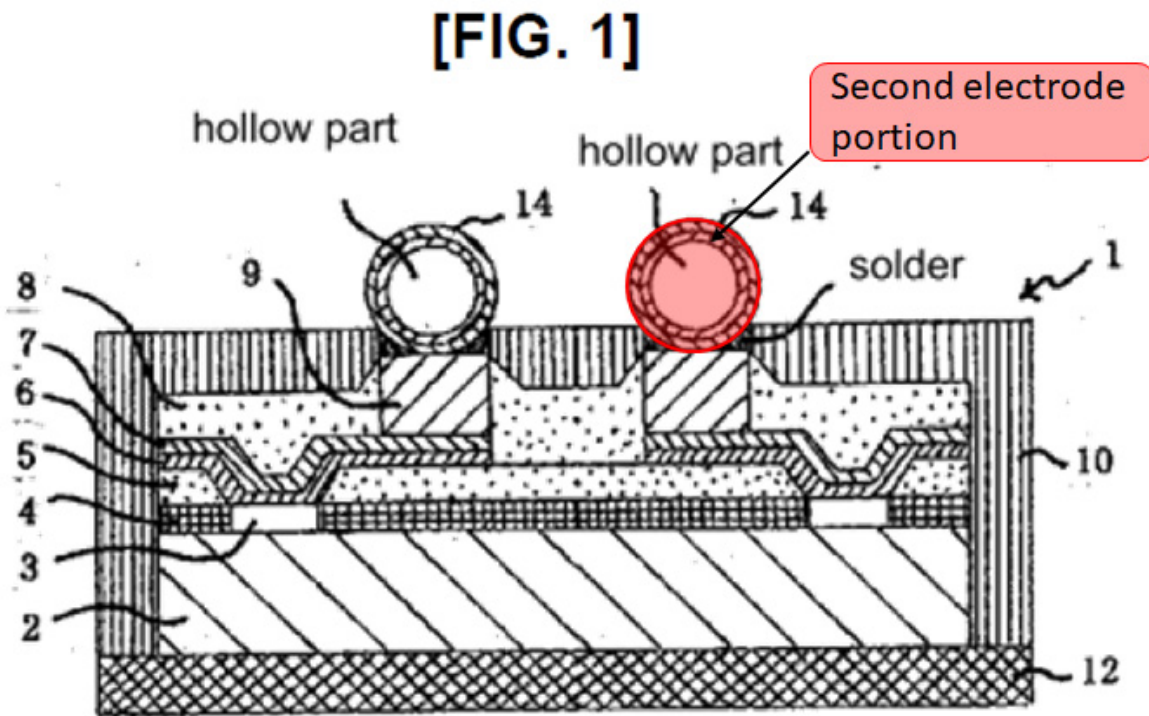
d) **[1 c]: a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal component**

97. Furuya discloses an external connection terminal (i.e. a second electrode portion) placed at the tip end of the metal post (i.e. the top portion of a first electrode portion), which external connection terminal is formed of a soldering metal component such as tin, which is used to create external electrical connections for example to a mounting board. Ex-1006, [0036]. For example, Furuya teaches:

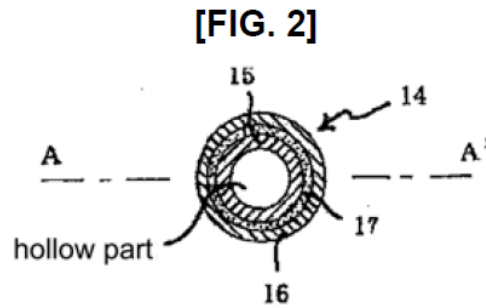
[A] characteristic of the semiconductor device 1 of the present invention, as shown in FIG. 1, is that **an external connection terminal 14 that makes an external**

electrical connection (for example, to a mounting board)
is placed at the tip end of the metal post 9, the external
connection terminal 14 being configured with an
electroconductive material provided on the surface of a
support having a hollow part opened to the outside.

Ex-1006, [0036]. Figure 1, annotated below shows the external connection
terminal 14.



98. Furuya teaches that this external connection terminal (second
electrode portion) is actually composed of multiple layers, as shown in Figure 2,
below.



99. Furuya explains that the outer layer 16 is composed of an electroconductive material that “must perform fixation with the outside and allow for electrical connection with the outside.” Ex-1006 [0043]. Furuya also notes, with respect to the prior art, that the second electrode portion may be a solder ball: “[I]f necessary, as shown in FIG. 6, a solder ball 71 or the like is sometimes formed as an external connection terminal 74 on the top face of the metal post 69.” *Id.*, [0006].

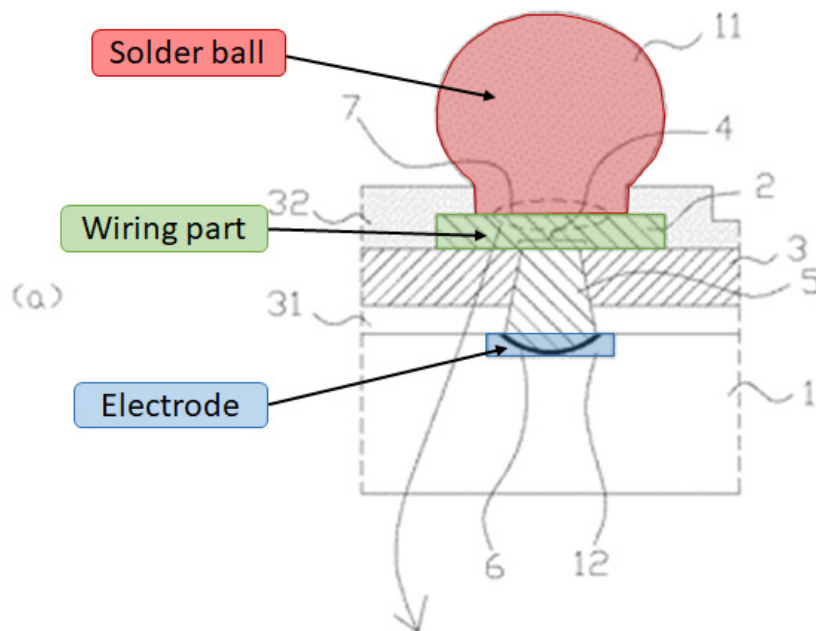
100. One of the conductive materials that Furuya discloses for use as solder is “a low melting point alloy having tin or lead as a principal component.” Ex-1006 [0043]. Furuya also teaches that:

[S]older alloy having tin or lead as a main component is preferable from the viewpoint of manufacturing costs and the like. Eutectic solder or high melting point solder with an increased lead ration can suitably be used as the solder alloy

Ex-1006, [0044]. This “eutectic” solder is used in the embodiment described by Furuya in detail. Ex-1006, [0055]. Thus, the second electrode portion is comprised of a second metal component that includes tin, which is different from the first metal component of the first electrode portion, which, as stated above, includes copper.

101. Takizawa also discloses a second electrode portion comprising a second metal component because it employs a solder ball (i.e., second electrode portion) that comprises tin and is mounted on a copper wiring layer (i.e., first electrode portion). Ex-1015, [0003], [0009], [0019]-[0020], [0033]-[0035]. Moreover, Takizawa discloses “[n]ote the material for the solder ball 11 in the present example was Sn-Pb eutectic solder, but the material for the solder ball 11 is not restricted to this, and can be any material as long as the material **contains Sn**, and can, for example have Sn-Ag or Sn **as a main component**...” *Id.* [0044] (emphasis added). This is shown in Figure 1(a), annotated below.

[FIG. 1]



102. Thus, Furuya and Takizawa disclose each aspect of this limitation.

e) **[1 d]: a diffusion layer formed between said first electrode portion and said second electrode portion**

103. Furuya discloses that when a connection is made between the metal post (i.e., first electrode portion) and mounting board using solder (i.e., second electrode portion), that some of the metal post will “dissolve and dissipate” into the solder, creating a diffusion layer. Ex-1006, [0007]. For example, Furuya teaches:

In many cases, the connection between the metal post 69 and the outside (for example, the mounting board) is made by thermocompression bonding using solder, but at this time, if high temperatures of, for example, 180°C to 250°C

are reached, **some of the metal post 69 will dissolve and dissipate in the solder.** In consideration for this dissolution and dissipation, the height of the metal post 69 is generally approximately 3 μm to 50 μm .

Ex-1006, [0007].

104. A POSA would have understood that this dissolution of the metal post into the solder results in a diffusion layer. To be clear, Furuya teaches this diffusion layer with respect to Figure 6, which Furuya describes as prior art. However, a POSA would have understood that the same principle results in a diffusion layer forming between the external electrical connection 14 and the metal post in Figure 1 as well, considering that similar materials and techniques are used to connect the metal post and mounting board. As stated above, Furuya discloses a “first electrode portion” comprised of copper and a “second electrode portion” comprised of tin. Furuya, further discloses that the “second electrode portion” may be a low melting point lead-tin alloy—specifically a “eutectic alloy”—and that the soldering process is performed at 220° C for 8 seconds. *See* Ex-1006, [0055]-[0056]. A POSA would have known that the commonly used (63/37) eutectic tin-lead alloy melts at 183° C. Thus, during the soldering process, molten solder would be in contact with the copper metal post. Therefore, based on Furuya’s technical disclosures and the conventional knowledge of a POSA at the time of Furuya’s invention (as discussed

in the Technical Background section above), Furuya discloses “a diffusion layer formed between said first electrode portion and second electrode portion.”

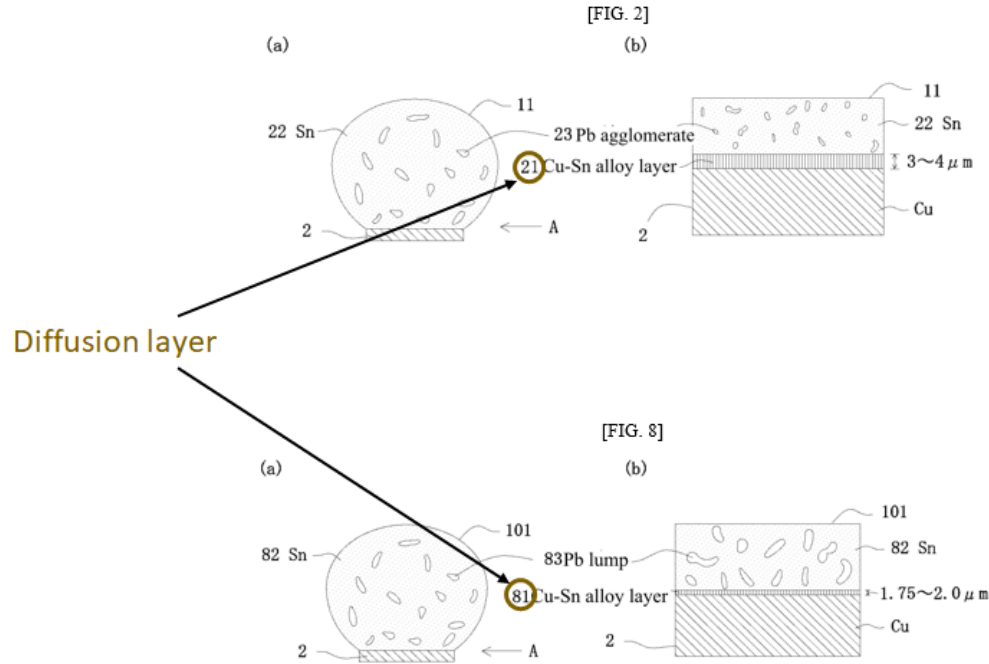
105. To the extent that the Board nevertheless finds Furuya’s disclosure of a “diffusion layer” to be insufficient, a POSA would have been motivated to combine Furuya with Takizawa for the reasons discussed above.

106. Takizawa explicitly discloses a diffusion layer, formed between its wiring and solder ball. For example, Takizawa teaches:

As illustrated in FIG. 1(b), a strong Cu-Sn alloy layer is formed on the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 portion on which the solder ball 11 is placed on the wiring part 2. As described above, detachment of the solder ball 11 caused by fractures and cracks can be reduced by reducing the occurrence of fractures and cracks near the bonding part by providing the Cu-Sn alloy layer on the bonding part between the solder ball 11 and the wiring part 2. As a result, productivity of the semiconductor device can be improved, and yield can be further increased.

Ex-1015, [0035]. *See also, id.*, [0003] (discussing Cu-Sn alloy layer 81 in prior art figures). This layer is formed by diffusion between the solder ball and the metal

wiring. *See, id.*, [0034]. Annotated Figures 2B and 8B illustrate this diffusion layer.



107. Thus, Furuya and Takizawa disclose each aspect of this limitation.

f) **[1 e]: wherein said diffusion layer comprises said first metal component and said second metal component**

108. As described above with reference to claim elements [1b] and [1c], Furuya discloses a first metal component, i.e., copper, in the first electrode portion and a second metal component, i.e., tin, in the second electrode portion. Moreover, Furuya describes a soldering process in which a molted eutectic solder containing tin is in direct contact with a copper metal external electrode. Ex-1006, [0055]-[0056]. In view of the knowledge of a POSA, as confirmed by the '001 Patent, (summarized in the Technological Background section above), when **solder**

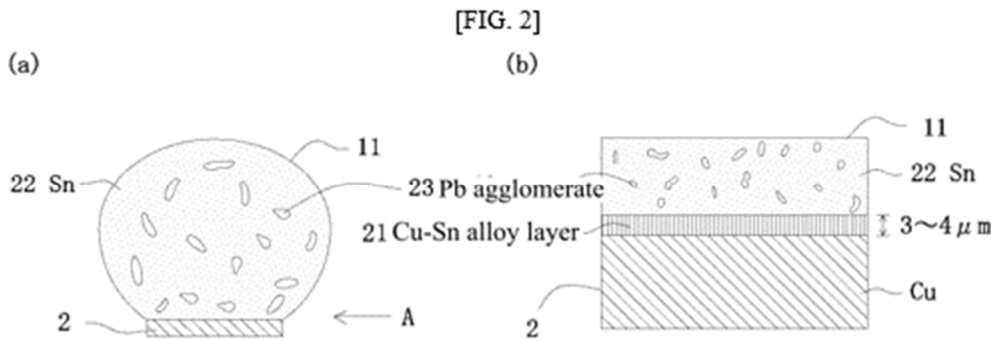
containing tin (Sn) is connected in a molten state to a copper electrode (Cu) metal, the tin and copper form a Sn-Cu diffusion layer. Ex-1001, 2:12-29.

Therefore, a POSA would have recognized that Furuya discloses a process which results in a diffusion layer comprising both a first metal component and second metal component, i.e., copper and tin.

109. To the extent that the Board nevertheless finds Furuya does not sufficiently disclose that “said diffusion layer comprises [a] first metal component and [a] second metal component,” a POSA would have been motivated to combine Furuya with Takizawa for the reasons discussed above to incorporate the composition of the diffusion layer disclosed in Takizawa.

110. Takizawa explicitly discloses a diffusion layer that forms between the first and second electrode portions. Takizawa further discloses that the diffusion layer comprises copper from the first electrode portion (i.e., the first metal component) and tin from the second electrode portion (i.e., the second metal component). Ex-1015, [0033]-[0034]. For example, Takizawa teaches that the wiring is comprised of copper (first metal component), while the solder ball is comprised of tin (second metal component). *See* Ex-1015, *See, e.g.*, Ex-1015, [0003], [0009], [0019]-[0020], [0033]-[0035], Figures 2, 8. In regards to the material of the solder ball, Takizawa explicitly discloses that the solder ball “can be any material as long as the material contains Sn...as a main component.” *Id.*

[0042]. Moreover, Takizawa teaches that a diffusion layer—“Cu-Sn alloy layer 21”—is “formed on the bonding part between the solder ball 11 and the wiring part 2.” Ex-1015, [0035]. *See also id.*, [0003], [0009], [0033]-[0035]. These two components are shown clearly in Figure 2, reproduced below, which shows the solder ball as tin (Sn) and the wiring part as copper (Cu), while the diffusion layer contains both copper and tin (Cu-Sn alloy layer).



111. Thus, the diffusion layer comprises an alloy containing both the first metal component (copper) and the second metal component (tin). Both Furuya and Takizawa disclose each aspect of this limitation.

112. To the extent “second metal component” is construed to require all of the elements in the material comprising the solder ball, Takizawa meets this construction. Takizawa teaches that the solder may be a tin-copper solder:

Note, the material for the solder ball 11 in the present example was Sn-Pb eutectic solder, but the material for the solder ball 11 is not restricted to this, and can be any

material **as long as the material contains Sn**, and can, for example, have Sn-Ag alloy or Sn as a main component, and **Pb free solders or the like containing Ag, Cu, Zn**, Cd, Ni, S, As, or Bi can be used.

Ex-1015, [0044]. *See also, id.*, [0035]. In this example the first metal component (copper) and the second metal component (tin-copper) would both be present in the disclosed tin-copper diffusion layer. Thus, under any construction for “metal component,” Takizawa discloses this limitation.

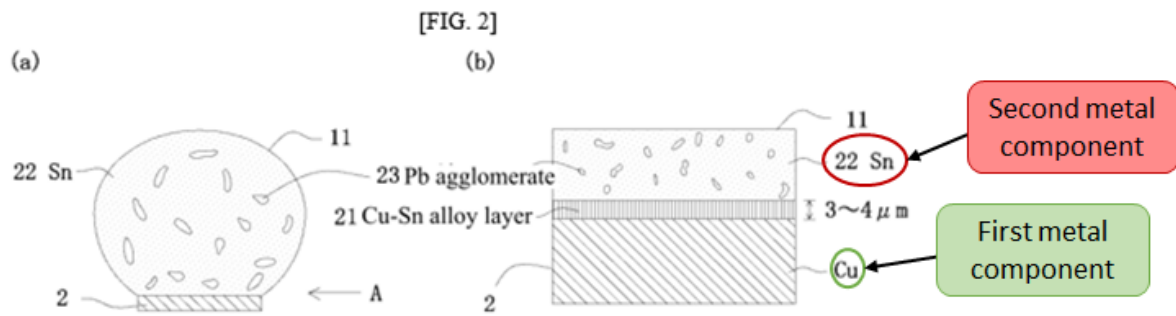
113. Accordingly, a person of ordinary skill in the art would have understood that all limitations of Claim 1 are rendered obvious by Furuya in view of Takizawa, and, as a result, Claim 1 is invalid.

3. Claim 2: The semiconductor device of claim 1, wherein said first metal component includes copper and said second metal component includes tin

114. Furuya and Takizawa both disclose that the first metal component includes copper and the second metal component includes tin. For example, as described above with reference to limitation 1[b], Furuya teaches that the first electrode (comprised of the first metal component) is composed of a metal post, wiring pattern, and metal barrier layer. Both the metal post and the wiring pattern comprise copper. *See, e.g.*, Ex-1006, [0035] (“the material for the wiring pattern 7 is desirably a material with good conductivity and, for example, copper...can be

used”); [0053] (“Next, metal posts 9 made of copper (height 16 μm) were formed on the wiring pattern 7...”). Similarly, Furuya teaches that the second metal component that comprises the outer layer of the external connection may be “a low melting point alloy having tin or lead as a principal component.” Ex-1006, [0043]. Moreover, Furuya discloses that “a solder alloy having tin or lead as a main component is preferable from the viewpoint of manufacturing costs and the like. Eutectic solder or high-melting point solder with an increased lead ratio can suitable be used as the solder alloy.” Ex-1006, [0044].

115. This is also shown by Takizawa, which discloses that the first metal component includes copper and the second metal component includes tin. For example, Takizawa discloses “the wiring part 2 containing Cu that is connected to a semiconductor chip 1 and the solder ball (11 containing Sn) that is connected to the wiring part 2.” Ex-1015, [0034]. Moreover, in regards to the material of the solder ball, Takizawa explicitly discloses that the solder ball “...can be any material as long as the material **contains Sn...as a main component.**” *Id.*, [0044]. Other embodiments in Takizawa,, such as that disclosed in Figures 2 and 8 similarly teach the first metal component comprising copper and the second metal component comprising tin. Figure 2B, annotated below, illustrates that the first metal component contains copper, while the second metal component contains tin. *See, e.g.,* Ex-1015, [0003], [0009], [0033]-[0035].



116. Thus, Furuya and Takizawa disclose each aspect of this limitation.

Accordingly, Furuya in view of Takizawa renders obvious Claim 2.

4. **Claim 3: The semiconductor device of claim 1, further comprising a third electrode portion formed on a surface of the semiconductor element and a metal wiring formed on the semiconductor element, said metal wiring electrically connecting the first electrode portion to the third electrode portion**

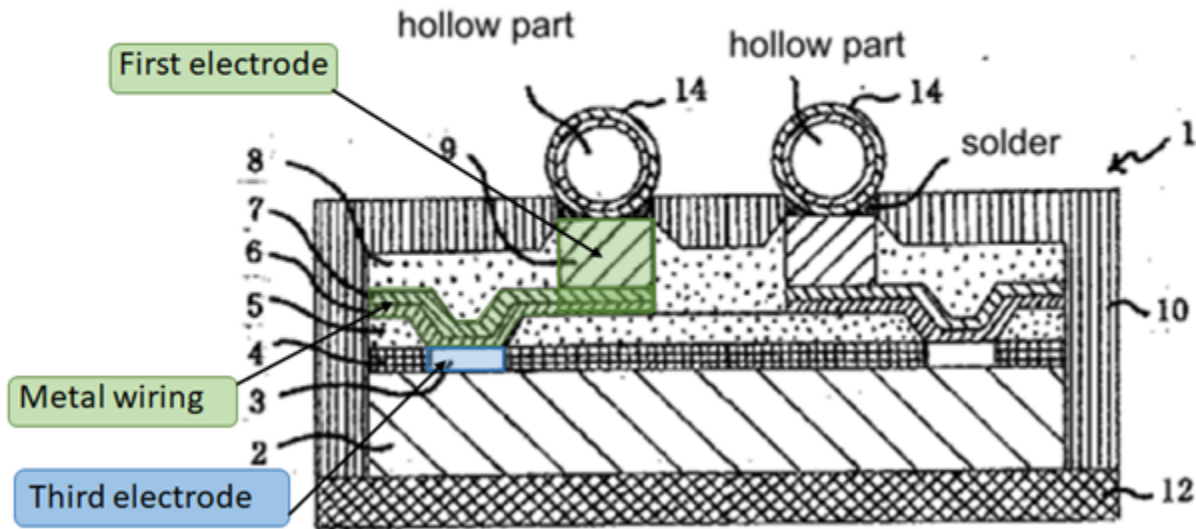
117. Furuya discloses a metal wiring that electrically connects an electrode (i.e. third electrode portion) on the surface of the semiconductor element to the metal post of the “first electrode portion” described above for Claim 1. For example, Furuya discloses a semiconductor device “with **an electrode, which has been formed on the semiconductor element, exposed; a wiring pattern, which is connected with the electrode of the semiconductor element**, is formed on the first insulating layer; a metal post for external connection is formed on the wiring pattern.” Ex-1006, [0016]. Furuya notes:

[A] first insulating layer 5, which has substantially the same shape as a passivation film 4, is formed on the

passivation film 4, **in a manner so as to expose electrodes 3, which have been formed on a semiconductor element 2. Then, a wiring pattern 7 (wiring layer) that is connected with the electrodes 3 is formed on the first insulating layer 5, and metal posts 9 for external connection, having a height of approximately 3 μm to 50 μm , are formed at predetermined positions on the wiring pattern 7.**

Ex-1006, [0027]. *See also* Ex-1006, [0051] - [0052], Fig. 4. Figure 1, annotated below, shows a third electrode portion (electrode 3) formed on a surface of the semiconductor element (element 2) and a metal wiring (wiring pattern 7) formed on the semiconductor element (element 2), said metal wiring electrically connecting the first electrode portion to the third electrode portion.

[FIG. 1]



118. Moreover, Furuya discloses that “wiring pattern 7” is formed using electrically-conductive metal materials such as TiN and copper. Ex-1006, [0052] (“Next, a 2000 Å [0.2 μm] thick TiN layer and a 5000 Å [0.5 μm] thick Cu layer were sequentially laminated on the first insulating layer 5 by sputtering. Next, a patterning process was performed on the TiN layer and the Cu layer, using a known photoetching method, to produce a wiring pattern 7, which is electrically connected to the electrode 3 (FIG. 4 (b)).”). Thus, “wiring pattern 7” is a metal wiring formed on the semiconductor element that electrically connects the first electrode portion to the third electrode portion.

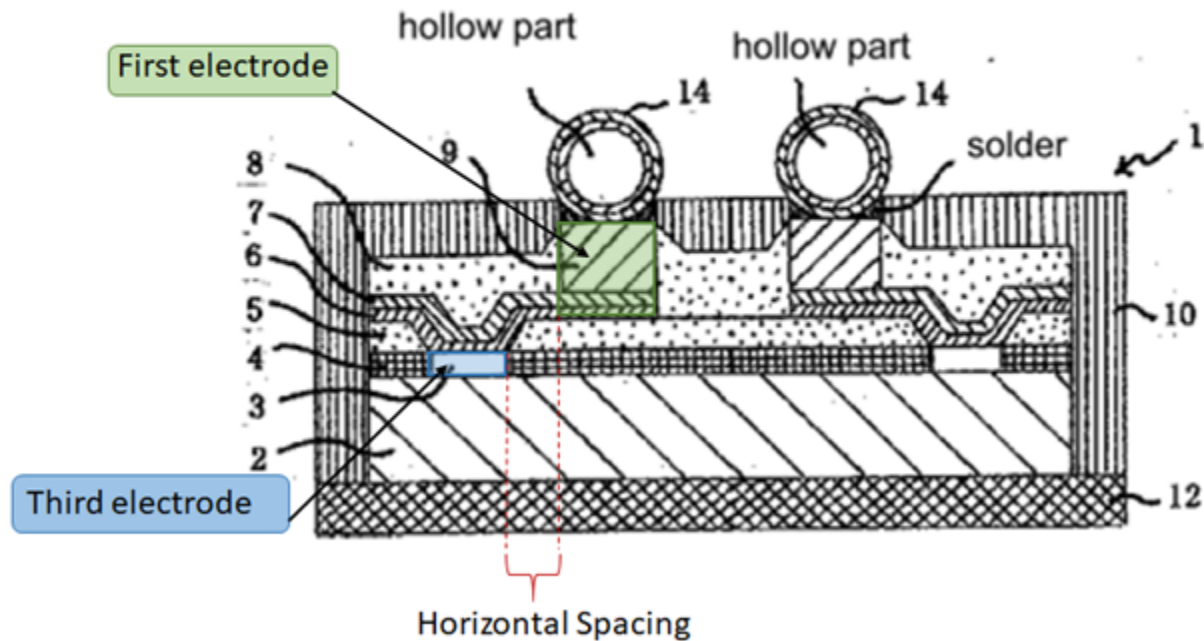
119. In view of the foregoing, persons of ordinary skill in the art would have understood that Furuya discloses a semiconductor device comprising “a third

electrode portion formed on a surface of the semiconductor element and a metal wiring formed on the semiconductor element, said metal wiring electrically connecting the first electrode portion to the third electrode portion.” Accordingly, Claim 3 is invalid.

5. Claim 4: The semiconductor device of claim 3, wherein the first and third electrode portion are horizontally spaced apart with respect to the semiconductor element

120. Furuya discloses teaches a semiconductor device where the first electrode portion and third electrode portion are horizontally spaced apart with respect to the semiconductor element. For example, Furuya discloses that the wiring pattern is formed on the third electrode and metal posts (a portion of the first electrode) are “formed **at predetermined positions on the wiring pattern 7.**” Ex-1006, [0027]. *See also* Ex-1006, [0053]. This description indicates that there is an intervening horizontal space between the two electrodes that is bridged by the wiring pattern, which electrically connects the two electrode portions. Figure 1, annotated below, confirms this horizontal spacing with respect to the semiconductor element. *See* Ex-1006, Fig. 1.

[FIG. 1]



121. A POSA would have recognized that the depiction in Figure 1 as further described in the specification is just one example of how the first and third electrodes are spaced in what is commonly known as a redistribution structure, and would have recognized that the electrodes would be distributed on the die in such a way that in some instances the metal posts, i.e., first electrodes, would be separated from their corresponding third electrode(s) by significant distances. In paragraph 1 Furuya states that his invention relates to a chip scale package (CSP) and in paragraphs 2-5 describes the principles of CSP. Based on this description and the prior art on CSP a POSA would have recognized the following: a) the third electrodes are in general located in the periphery of each individual semiconductor

element, b) the first electrodes are distributed across the area of the semiconductor element, and c) each metal wire is used to connect a third electrode located at the perimeter of the semiconductor element to a corresponding first electrode located at some horizontal distance away on the front face of the semiconductor element.

Furuya summarizes the CSP structure by stating, “[t]he metal posts 69 are electrically connected to the electrodes 63 by way of wiring 67.” Ex-1006, [0006]. As discussed above Furuya’s “metal post 69” and “electrodes 63” are examples of what the ’001 Patent refers to as “first electrode portions” and “third electrode portions” respectively. Since all Furuya’s metal posts and electrodes are formed on the surface, the use of wiring 67 to electrically connect each metal post 69 to a corresponding electrode 63 would imply that all of the metal posts 69 and their corresponding electrodes 63 are horizontally spaced apart, hence the need to utilize wiring to electrically connect them.

122. In view of the foregoing, persons of ordinary skill in the art would have understood that Furuya discloses a semiconductor device “wherein the first and third electrode portion are horizontally spaced apart with respect to the semiconductor element.” Accordingly, Claim 4 is invalid.

6. Claim 6: The semiconductor device of claim 3, wherein the metal wiring includes copper

123. Furuya discloses that both the metal posts and the wiring pattern each includes copper. Ex-1006, [0035]. For example, Furuya teaches that “the material

for the wiring pattern 7 is desirably a material with good conductivity and, **for example, copper**, silver, aluminum, alloys thereof, other metals that are good conductors or the like can be used.” Ex-1006, [0035]. In one embodiment, Furuya discloses that “a 2000 Å [0.2 µm] thick TiN layer and a 5000 Å [0.5 µm] thick **Cu layer** were sequentially laminated on the first insulating layer 5 by sputtering” to form the metal wiring. *Id.*, [0052]. Similarly, Furuya teaches that the metal posts may also be made of copper: “Next, **metal posts 9 made of copper** (height 15 µm) were formed on the wiring pattern 7...” *Id.*, [0053].

124. In view of the foregoing, persons of ordinary skill in the art would have understood that Furuya discloses “the semiconductor device of claim 3, wherein the metal wiring includes copper.” Accordingly, Claim 6 is invalid.

7. Claim 7

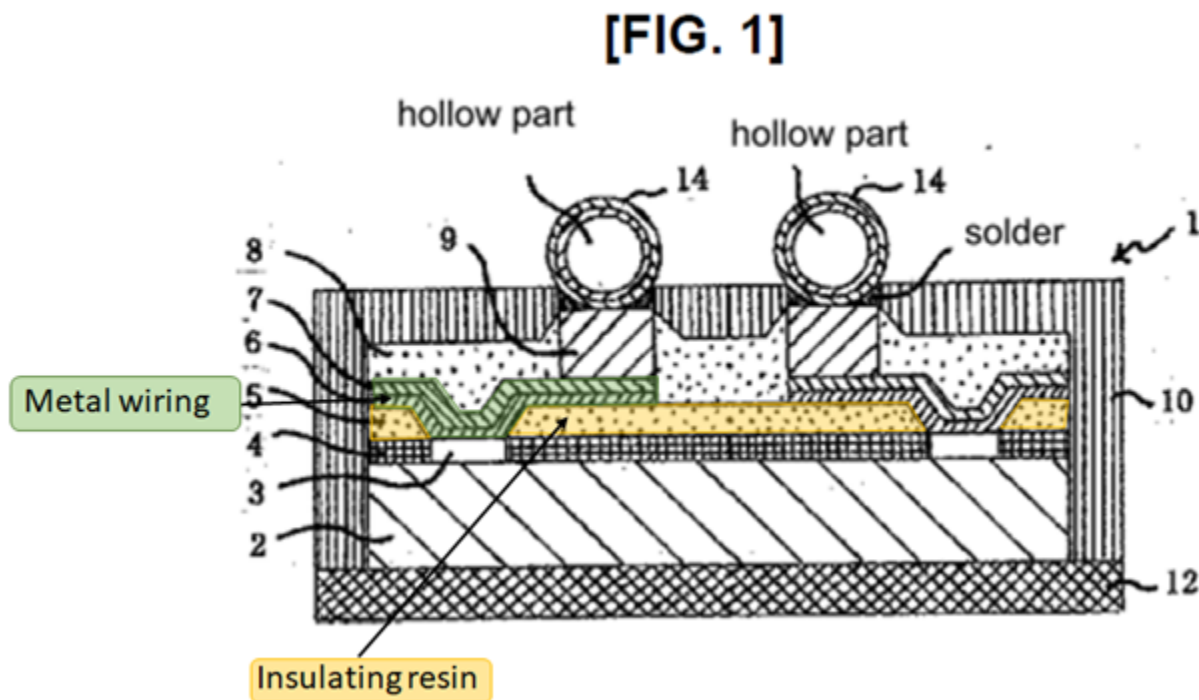
- a) **[7a]: The semiconductor device of claim 3, further comprising an insulating resin layer formed between the surface of the semiconductor element and the metal wiring**

125. Furuya discloses a first insulating layer formed between the semiconductor element and the metal wiring. Ex-1006, [0046]. For example, Furuya teaches a method of manufacturing a semiconductor device including:

[A] step of **forming a first insulating layer 5**, which has substantially the same shape as a passivation film 4, on a semiconductor element 2, on the surface of which the

passivation film 4 has been formed, in a manner so as to expose the electrodes 3, and then forming a wiring pattern 7 having a predetermined shape, which is connected with the electrodes 3, on the first insulating layer 5, so as to produce [the] state in FIG. 4 (b)...

Ex-1006, [0046]. *See also*, Ex-1006, [0004], [0027], [0033], [0063]. This is shown in Figure 1, annotated below.



126. Furuya further discloses that “insulating layer 5” is formed of an insulating resin material. For example, Furuya discloses forming “insulating layer 5” using a photosensitive polyimide material. *Id.*, [0052] (“Next, a photosensitive polyimide (trade name ‘Pimel’, made by Asahi Kasei Corp.) was applied to the

semiconductor element 2, whereafter a known photoetching method was used to perform pattern exposure, development and the like, and a first insulating layer 5 having a film thickness of approximately 10 μm was formed, which exposed the electrodes 3.”). Furuya also teaches that polyimide is a type of resin material. *Id.*, [0021] (“an engineering plastic comprising a **resin selected from polyimide ...**”).

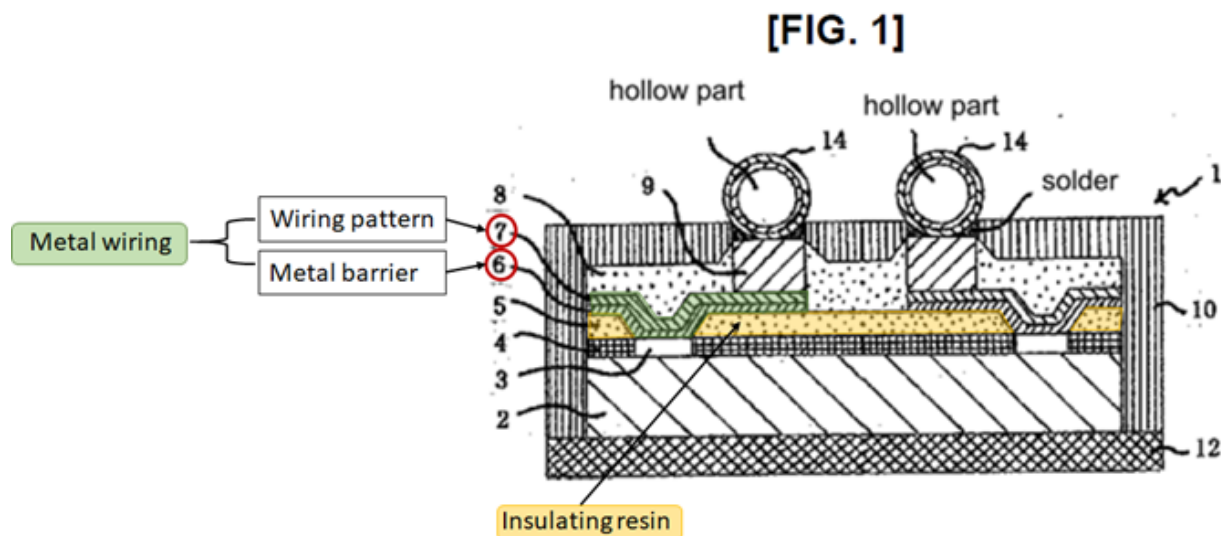
127. In view of the foregoing, persons of ordinary skill in the art would have understood that Furuya discloses “the semiconductor device of claim 3, further comprising an insulating resin layer formed between the surface of the semiconductor element and the metal wiring.”

b) **[7b]: wherein the metal wiring is formed along a surface of the insulating resin layer**

128. Furuya discloses the first insulating layer discussed with reference to element 7[a] is used as a surface along which the metal wiring is formed. Ex-1006, [0046]. For example, regarding the formation of the wiring pattern, Furuya teaches, “then forming a wiring pattern 7 having a predetermined shape, which is connected with the electrodes 3, on the first insulating layer 5, so as to produce state in FIG. 4 (b).” Ex-1006, [0046]. *See also* Ex-1006, [0004]. Although Furuya describes two separate layers, a wiring pattern and a metal barrier layer as being formed along the surface of the insulating resin layer, a POSA would view the combination of these two layers as corresponding to the “metal wiring” disclosed in the ’001 Patent. For example, the ’001 Patent explains that “the metal wirings 14 are formed as follows:

a titanium tungsten (TiW) layer and a Cu layer are sequentially formed on the passivation film 13 by a sputtering method.” *Id.*, 14:28-32.

129. I have shown this metal wiring on the insulating resin layer in Figure 1, annotated below where the wiring pattern is depicted as formed along the insulating resin layer.



130. In view of the foregoing, persons of ordinary skill in the art would have understood that Furuya discloses a semiconductor device “wherein the metal wiring is formed along a surface of the insulating resin layer.” Accordingly, Claim 7 is invalid.

8. Claim 8: The semiconductor device of claim 3, wherein the metal wiring has a thickness in the range of 0.01 μm to 8 μm

131. Furuya discloses this limitation because the wiring pattern combined with the metal barrier layer form a metal wiring that has a thickness of 7,000 Å or

0.7 μm . Ex-1006, [0052]. In discussing the formation of these layers, Furuya teaches:

Next, a 2000 Å [0.2 μm] thick TiN layer and a 5000 Å [0.5 μm] thick Cu layer were sequentially laminated on the first insulating layer 5 by sputtering. Next, a patterning process was performed on the TiN layer and the Cu layer, using a known photoetching method, to produce a wiring pattern 7, which is electrically connected to the electrode 3 (FIG. 4 (b)). Note that the TiN layer between the first insulating layer 5 and the wiring pattern 7 is formed as a barrier metal layer 6.

Ex-1006, [0052]. As described above in Section VII.B.7, the metal barrier layer plus the wiring pattern is meets the claimed “metal wiring” of the '001 Patent.⁷ *Compare* Ex-1001, 14:25-32 *with* Ex-1006, [0035].

132. In view of the foregoing, persons of ordinary skill in the art would have understood that Furuya discloses “the semiconductor device of claim 3,

⁷ Note that the '001 Patent is clear that the metal wiring includes the first electrode portion, which is thicker than the 8 μm required by this claim. Ex-1001, 8:39-55. This petition maps Furuya to the disclosed embodiments of the '001 Patent which include thinner non-electrode portions of the metal wiring falling within this claim range. Ex-1001, 9:25-35.

wherein the metal wiring has a thickness in the range of 0.01 μm to 8 μm .”

Accordingly, Claim 8 is invalid.

9. Claim 10

a) [10 pre]: A semiconductor device, comprising

133. Claim element [10 pre] is worded identically to [1 pre] and is disclosed for the reasons discussed with reference to that claim element.

b) [10 a]: a semiconductor element

134. Claim element [10 a] is worded identically to [1 a] and is disclosed for the reasons discussed with reference to that claim element.

c) [10 b]: a first electrode portion formed on the semiconductor element, said first electrode portion comprising a first metal component

135. Claim element [10 b] is worded identically to [1 b] and is disclosed for the reasons discussed with reference to that claim element.

d) [10 c]: a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal component

136. Claim element [10 c] is worded identically to [1 c] and is disclosed for the reasons discussed with reference to that claim element.

- e) **[10 d]: a diffusion layer formed between said first electrode portion and said second electrode portion**

137. Claim element [10 d] is worded identically to [1 d] and is disclosed for the reasons discussed with reference to that claim element.

- f) **[10 e]: wherein said diffusion layer comprises said first metal component and said second metal component**

138. Claim element [10 e] is worded identically to [1 e] and is disclosed for the reasons discussed with reference to that claim element.

- g) **[10 f]: said first electrode portion and said diffusion layer have a combined thickness in the range of 10 μ m to 20 μ m**

139. Furuya in view of Takizawa discloses this limitation because the thickness of the “first electrode portion” disclosed by Furuya plus the thickness of the diffusion layer taught by Takizawa is between 10 μ m and 20 μ m. As described above with reference to claim element 1[b], the first electrode portion in Furuya is formed by the combination of a portion of the metal barrier layer, a portion of the wiring pattern, and the metal post.

140. As discussed above with reference to claim element 1[d], Furuya discloses a diffusion layer that forms between the first electrode portion and the second electrode portion. However, although Furuya discloses a thickness for the first electrode portion, it does not disclose the thickness of the diffusion layer. Takizawa also discloses a diffusion layer formed between the wire part and the

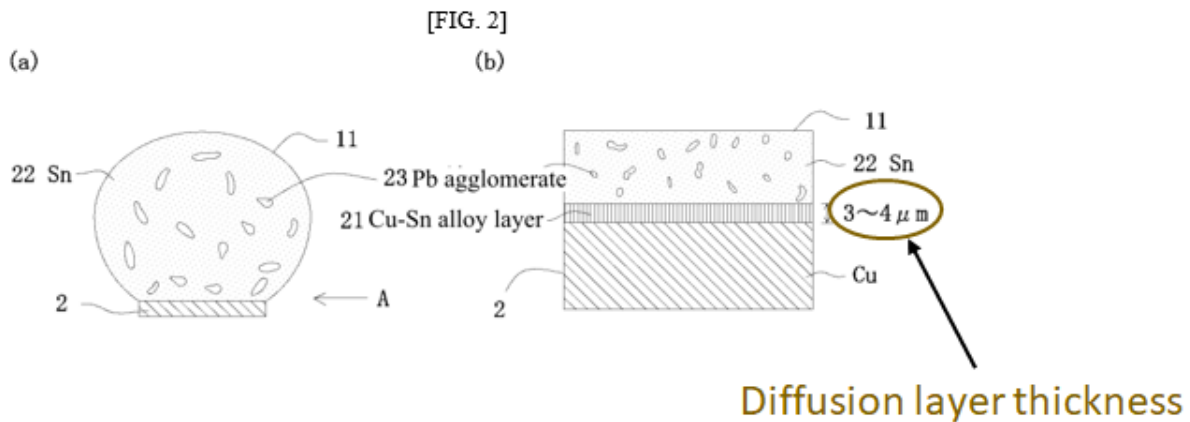
solder ball, as described above with reference to claim element 1[d]. Takizawa further teaches advantages to a specific thickness of the diffusion layer.

Specifically, Takizawa states:

As shown in FIG. 2, a Cu-Sn alloy layer was formed in the vicinity of the bonding part between the solder ball 11 and the wiring part 2. In regards to the solder ball 11 provided on the semiconductor device of the present invention illustrated in FIG. 2, 1.87 to 4.0 μm of the Cu-Sn alloy layer was formed on each solder ball 11, and in particular, many solder balls were formed with 3.0 to 4.0 μm of the Cu-Sn alloy layer. On the other hand, 1.00 to 1.50 μm of the Cu-Sn alloy layer was formed on the solder ball 101 placed on the conventional semiconductor device illustrated in FIG. 8. Thereby, it was revealed that the semiconductor device of the present invention illustrated in FIG. 2 was formed with a strong Cu-Sn alloy layer that was thicker. Forming the Cu-Sn alloy layer with a thickness of at least 1.87 μm or more was preferable in order to prevent detachment of the solder ball 11.

Ex-1015, [0040]. *See also id.*, [0009]-[0012], [0035], Figures 2, 8. Figures 2 and

8, reproduced below, shows an exemplary thickness of the diffusion layer:



141. The combination of the optimized diffusion layer thickness of Takizawa with the thickness of the first electrode portion of Furuya yields a combined thickness that falls within the 10 μm to 20 μm range as claim 10 requires.⁸ Furuya discloses that the metal post portion of the first electrode portion is 15 μm. Ex-1006, [0053]. As described with respect to Claim 8, the wire portion of the first electrode portion disclosed in Furuya is 0.7 μm thick. Ex-1006, [0052]. As a result, the entire thickness of the first electrode portion in Furuya is 15.7 μm. The diffusion layer will form partially into the first electrode portion and partly above the first electrode portion. However, taking the extreme case where the

⁸ A POSA combining Furuya and Takizawa would have recognized that the optimum diffusion layer thickness taught in Takizawa does not depend on using the first electrode portion thickness (18 μm) taught in Takizawa. Takizawa does not indicate that it optimized the first electrode portion thickness. Thus, it would have been natural for a POSA to keep the first electrode thickness taught in Furuya (15.7 μm) and only incorporate the diffusion layer thickness from Takizawa.

diffusion layer forms entirely above the first electrode portion, the maximum combined thickness would equal 19.7 μm (15.7 μm from the first electrode portion plus 4.0 μm from the diffusion layer). Taking the other extreme, where the diffusion layer is formed entirely into the first electrode portion, the minimum combined thickness would be 15.7 μm —the height of the first electrode portion. At most the combined thickness would equal 19.7 μm while at a minimum the thickness would equal 15.7 μm .^{9, 10} Thus, because Furuya in view of Takizawa discloses a thickness range that falls entirely within the claimed range of 10-20 μm , Furuya in view of Takizawa discloses each aspect of this limitation. *Id.*

Accordingly, Claim 10 is invalid.

10. Claim 11: The semiconductor device of claim 10, wherein said first metal component includes copper and said second metal component includes tin

142. Claim 11 is worded identically to Claim 2 and is disclosed for the reasons discussed with reference to that claim.

⁹ The actual thickness range would likely be narrower than in this example because a portion of the diffusion layer would be created into the solder ball while the rest of its thickness would be created into the first electrode portion. However, even the extreme cases shown above fall entirely within the claimed range.

¹⁰ Note that Figure 3 indicates that the thickness of the wiring part in Takizawa is 18 μm . Thus, Takizawa also discloses a thickness within the claim range (for example taking the 1.87 μm thickness disclosed by Takizawa as the minimum accepted thickness for achieving the purpose of the invention yields a total combined thickness of 19.7 μm assuming the diffusion layer is formed only above the wiring part).

- 11. Claim 12: The semiconductor device of claim 10, further comprising a third electrode portion formed on a surface of the semiconductor element and a metal wiring formed on the semiconductor element, said metal wiring electrically connecting the first electrode portion to the third electrode portion**

143. Claim 12 is worded identically to Claim 3 and is disclosed for the reasons discussed with reference to that claim.

- 12. Claim 13: The semiconductor device of claim 12, wherein the first and third electrode portion are horizontally spaced apart with respect to the semiconductor element**

144. Claim 13 is worded identically to Claim 4 and is disclosed for the reasons discussed with reference to that claim.

- 13. Claim 15: The semiconductor device of claim 12, wherein the metal wiring includes copper**

145. Claim 15 is worded identically to Claim 6 and is disclosed for the reasons discussed with reference to that claim.

14. Claim 16

- a) [16a]: The semiconductor device of claim 12, further comprising an insulating resin layer formed between the surface of the semiconductor element and the metal wiring**

146. Claim element [16 a] is worded identically to [7 a] and is disclosed for the reasons discussed with reference to that claim element.

b) **[16b]: wherein the metal wiring is formed along a surface of the insulating resin layer**

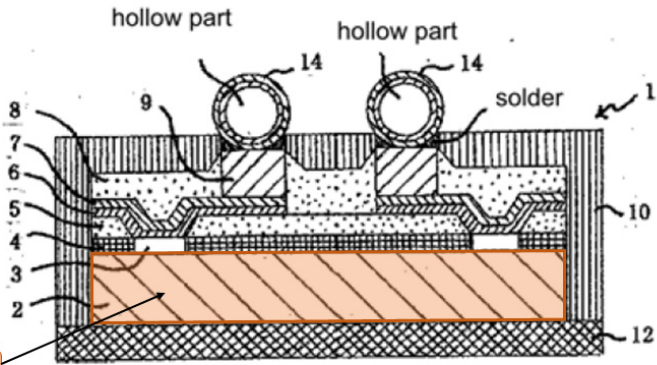
147. Claim element [16 b] is worded identically to [7 b] and is disclosed for the reasons discussed with reference to that claim element.

15. **Claim 17: The semiconductor device of claim 12, wherein the metal wiring has a thickness in the range of 0.01 μm to 8 μm**

148. Claim 17 is worded identically to 8 and is disclosed for the reasons discussed with reference to that claim.

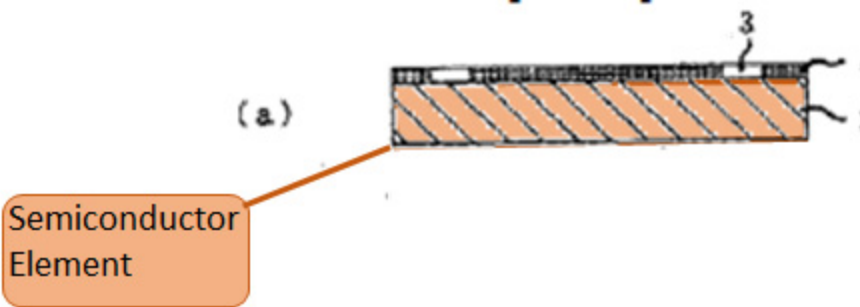
16. **Claim Chart**

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	Claim 1	
1P	A semiconductor device, comprising:	<p>Furuya, Title (“<i>Semiconductor Device</i> and Method of Manufacturing Same”)</p> <p>Furuya, [Abstract] (“<i>A semiconductor device</i> characterized in that a first insulating layer having substantially the same shape as a passivation film is formed on the passivation film, which has been formed on a semiconductor element, with an electrode, which has been formed on the semiconductor element, exposed; a wiring pattern, which is connected with the electrode of the semiconductor element, is formed on the first insulating layer; a metal post for external connection is formed on the wiring pattern; a second insulating layer, which is in close contact with the wiring pattern, is formed in a manner so as to cover a side face of the metal post excluding the tip of the metal post; and after sealing resin has been [applied] in a manner so as to expose the tip of the metal post, an external connection terminal is provided at the tip of the metal post.”)</p>

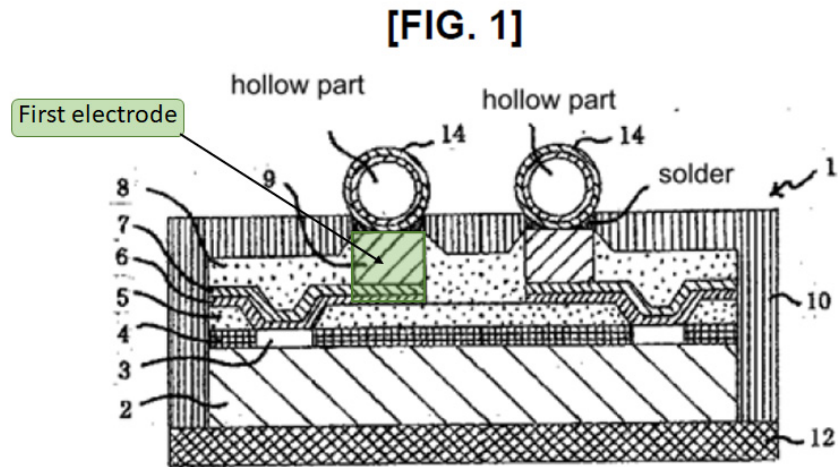
	U.S. Patent No. 6,954,001	Furuya in view of Takizawa
		<p>Furuya, [0001] (“The present invention relates to a semiconductor devices, which are known as a chip size packages (CSPs), in which a wiring layer is formed on a semiconductor element, and to a method for manufacturing the same.”)</p>
1A	a semiconductor element;	<p>Furuya, Figure 1 (reproduced and annotated below) of Furuya depicts “a semiconductor element” (designated numeral 2 “semiconductor element” and shaded orange).</p> <p style="text-align: center;">[FIG. 1]</p>  <p>Furuya, [Abstract] (“A semiconductor device characterized in that a first insulating layer having substantially the same shape as a passivation film is formed on the passivation film, which has been formed on a semiconductor element, with an electrode, which has been formed on the semiconductor element, exposed; a wiring pattern, which is connected with the electrode of the semiconductor element, is formed on the first insulating layer; a metal post for external connection is formed on the wiring pattern; a second insulating layer, which is in close contact with the wiring pattern, is formed in a manner so as to cover a side face of the metal post excluding the tip of the metal post; and after sealing</p>

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	<p>resin has been [applied] in a manner so as to expose the tip of the metal post, an external connection terminal is provided at the tip of the metal post.”)</p> <p>Furuya, [0001] (“The present invention relates to a semiconductor devices, which are known as a chip size packages (CSPs), in which a wiring layer is formed on <i>a semiconductor element</i>, and to a method for manufacturing the same.”)</p> <p>Furuya, [0005] (“Note that, in cases where a plurality of <i>semiconductor elements</i> 62 are formed laid out on one Si (silicon) wafer, if [operations] up to the formation of the second insulating layer 68 are performed on the Si wafer, and then the Si wafer is diced so as to be cut into individual semiconductor elements 62, semiconductor devices 61 (CSP) having substantially the same size as the individual semiconductor elements 62 can be obtained.”)</p> <p>Furuya, [0016] (“[Means for Solving the Problems] In order to achieve the aforementioned object, the present inventors undertook earnest study and arrived at the present invention. That is to say, in claim 1, the semiconductor device is characterized in that a first insulating layer having substantially the same shape as a passivation film is formed on the passivation film, which has been formed <i>on a semiconductor element</i>, with an electrode, which has been formed <i>on the semiconductor element</i>, exposed; a wiring pattern, which is connected with the electrode <i>of the semiconductor element</i>, is formed on the first insulating layer; a metal post for external connection is formed on the wiring pattern; a second insulating layer, which is in close contact with the wiring pattern, is formed in a manner so as to cover a side face of the metal post excluding a tip surface of the metal</p>

U.S. Patent No. 6,954,001	Furuya in view of Takizawa
	<p>post; resin sealing is performed with sealing resin in a manner so as to expose the tip surface of the metal post; and an external connection terminal is provided at the tip surface of the metal post.”)</p> <p>Furuya, [0027] (“Hereafter, modes of embodiment of the present invention are described based on the drawings. In the semiconductor device 1 (CSP) of the present invention, as shown in FIG. 1, a first insulating layer 5, which has substantially the same shape as a passivation film 4, is formed on the passivation film 4, in a manner so as to expose electrodes 3, which have been formed on a <i>semiconductor element 2</i>. ...”)</p> <p>Furuya, [0037] (“The matters set forth above will be explained. As described above, when the semiconductor device 1 is mounted on the mounting board, stress is caused in the semiconductor device 1 as a result of the difference in the thermal expansion coefficients between <i>the semiconductor element 2, which is formed of silicon or the like</i> (for example, having a thermal expansion coefficient of approximately 3 ppm) and the mounting board (for example, a printed circuit board made of epoxy resin, having a thermal expansion coefficient of approximately 40 to 200 ppm and exceeding 200 ppm at or above the Tg point). ...”)</p> <p>Fig. 4a (reproduced and annotated below) of Furuya discloses a “semiconductor element” (designated numeral 2 and shaded orange).</p>

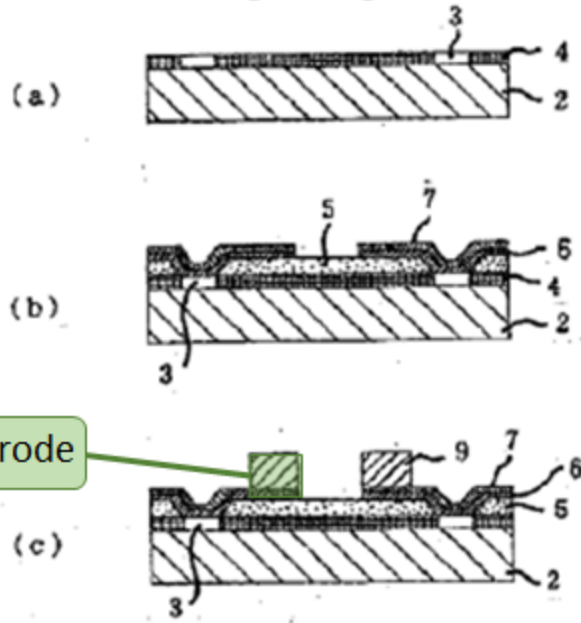
U.S. Patent No. 6,954,001		Furuya in view of Takizawa
		<p style="text-align: right;">[FIG. 4]</p>  <p>Furuya, [0051] <Embodiments> (“FIG. 4 (a) is a semiconductor element 2 produced by conventionally known means, which is incorporated in a semiconductor device 1 of the present invention. Electrodes 3 made of aluminum are formed on the semiconductor element 2 with a silicon wafer as a substrate, and a passivation film 4 is formed on the semiconductor element 2 in a manner so as to expose the electrodes 3. Note that, in the present embodiment, a plurality of semiconductor elements 2 are laid out on a single silicon wafer, but for convenience of description, one semiconductor element 2 from among these is shown.”)</p>
1B	a first electrode portion formed on the semiconductor element, said first electrode portion comprising a first metal component;	<p>Furuya, Figure 1 (reproduced and annotated below) of Furuya depicts “a first electrode portion formed on the semiconductor element” (designated by a combination of numerals 6 “metal barrier layer,” 7 “wiring pattern,” and 9 “metal post,” collectively shaded green).</p>

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Furuya, [0016] (“[Means for Solving the Problems] In order to achieve the aforementioned object, the present inventors undertook earnest study and arrived at the present invention. That is to say, in claim 1, the semiconductor device is characterized in that a first insulating layer having substantially the same shape as a passivation film is formed on the passivation film, which has been formed on a semiconductor element, with an electrode, which has been formed on the semiconductor element, exposed; ***a wiring pattern, which is connected with the electrode of the semiconductor element, is formed on the first insulating layer; a metal post for external connection is formed on the wiring pattern;*** a second insulating layer, which is in close contact with the wiring pattern, is formed in a manner so as to cover a side face of the metal post excluding a tip surface of the metal post; resin sealing is performed with sealing resin in a manner so as to expose the tip surface of the metal post; and an external connection terminal is provided at the tip surface of the metal post.”)

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	<p>the semiconductor device 1 (CSP) of the present invention, as shown in FIG. 1, a first insulating layer 5, which has substantially the same shape as a passivation film 4, is formed on the passivation film 4, in a manner so as to expose electrodes 3, which have been formed on a semiconductor element 2. Then, a wiring pattern 7 (wiring layer) that is connected with the electrodes 3 is formed on the first insulating layer 5, and metal posts 9 for external connection, having a height of approximately 3 μm to 50 μm, are formed at predetermined positions on the wiring pattern 7. Next, a second insulating layer 8 is formed, which is in close contact with the wiring pattern 7 and the first insulating layer 5, and which covers the side face of the metal post 9 excluding the tip surface of the metal post 9. Next, the semiconductor element is resinsealed with sealing resin 10 in a manner so as to expose the tip surface of the metal post 9, and an external connection terminal 14 is provided on the metal post 9”)</p> <p>Furuya, [0035] (“Next, the material for the wiring pattern 7 is desirably a material with good conductivity and, for example, copper, silver, aluminum, alloys thereof, other metals that are good conductors or the like can be used. If copper, silver, or the like is used as the material for the wiring pattern 7, prior to the formation of the wiring pattern 7, it is preferable to form a metal barrier layer 6 made of a TiW alloy, TiN, TaN, W, Cr or the like as an undercoat layer, and then form the wiring pattern 7 on the metal barrier layer 6.”)</p> <p>Figure 4(a)-(c) (reproduced and annotated below) of Furuya depicts “a first electrode portion formed on the semiconductor element” (designated by a combination of numerals 6 “metal barrier layer,” 7 “wiring pattern,” and 9 “metal post,” collectively shaded green).</p>

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	<p data-bbox="966 394 1096 441">[FIG. 4]</p>  <p data-bbox="519 1113 1396 1869">Furuya, [0046] (“Next, in the claim 8 set forth above, a method for manufacturing the semiconductor device 1 of the present invention is proposed. That is to say, this is a method of manufacturing a semiconductor device in which electrodes 3, which provide electrical connections with the outside, and are produced by way of a conventionally known manufacturing method, are formed as shown in FIG. 4 (a), and which has at least: a step of forming a first insulating layer 5, which has substantially the same shape as a passivation film 4, on a semiconductor element 2, on the surface of which the passivation film 4 has been formed, in a manner so as to expose the electrodes 3, and <i>then forming a wiring pattern 7 having a predetermined shape, which is connected with the electrodes 3, on the first insulating layer 5, so as to produce state in FIG. 4 (b); a step of forming a metal post 9 for external connection, in a predetermined position of the wiring pattern 7, at a</i></p>

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	<p><i>predetermined height (approximately 3 μm to 50 μm), so as to produce FIG. 4 (c); a step of applying an insulating resin on the first insulating layer 5 including the metal post 9, and then removing the insulating resin from the tip region of the metal post 9 for connecting to the outside, so as to make the second insulating layer 8 and produce the state in FIG. 4 (d); a step of resin sealing with the sealing resin 10 so as to produce FIG. 4 (e); and a step of placing the external connection terminal 14 so as to produce FIG. 4 (f). Note that, in the example in FIG. 4, prior to forming the wiring pattern 7, the metal barrier layer 6 is formed as an undercoat layer.")</i></p> <p>Furuya, [0052]-[0053] ("Next, a photosensitive polyimide (trade name "Pimel", made by Asahi Kasei Corp.) was applied to the semiconductor element 2, whereafter a known photoetching method was used to perform pattern exposure, development and the like, and a first insulating layer 5 having a film thickness of approximately 10 μm was formed, which exposed the electrodes 3. Next, a 2000 Å thick TiN layer and a 5000 Å thick Cu layer were 8 sequentially laminated on the first insulating layer 5 by sputtering. Next, a patterning process was performed on the TiN layer and the Cu layer, using a known photoetching method, to produce a wiring pattern 7, which is electrically connected to the electrode 3 (FIG. 4 (b)). Note that the TiN layer between the first insulating layer 5 and the wiring pattern 7 is formed as a barrier metal layer 6.</p> <p>Next, as shown in FIG. 4(c), a metal post 9 was formed on the wiring pattern 7, ... Note that a mask plating method is used for forming the metal post 9, and the steps for the mask plating method are described below. Specifically, after producing FIG. 4 (b), a photosensitive resist layer having a film thickness of 20 μm was formed</p>

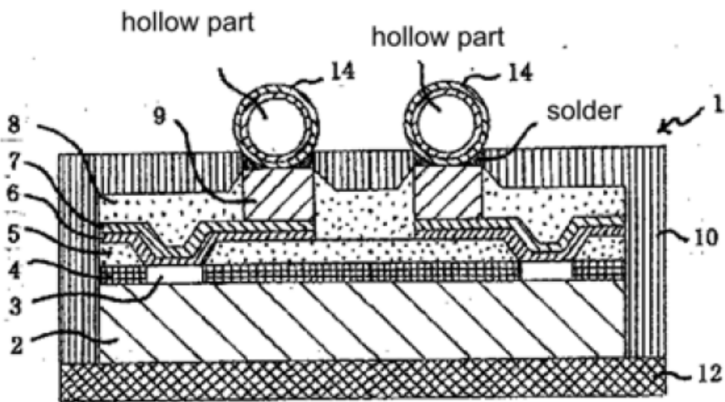
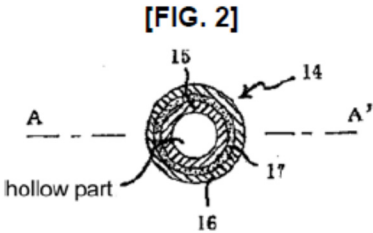
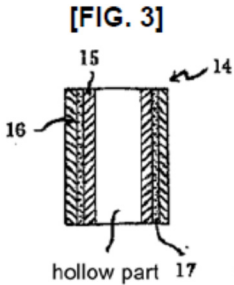
U.S. Patent No. 6,954,001		Furuya in view of Takizawa
		on the first insulating layer 5 and the wiring pattern 7, whereafter, using a known photoetching method, a plating mask 13 was formed, in which the wiring pattern 7 was exposed at the location where the metal posts were to be formed (FIG. 5 (a)). <i>Next, metal posts 9 made of copper (height 15 μm) were formed on the wiring pattern 7,</i> which was exposed by the plating mask 13, using an electrolytic plating method (FIG. 5 (d)[sic]). Next, the plating mask 13 was peeled off producing that inFIG. 4 (c).”)
1C	a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal component; and	<p>Furuya discloses a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal component.</p> <p>Furuya, [0027] (“Hereafter, modes of embodiment of the present invention are described based on the drawings. In the semiconductor device 1 (CSP) of the present invention, as shown in FIG. 1, Then, a wiring pattern 7 (wiring layer) that is connected with the electrodes 3 is formed on the first insulating layer 5, and metal posts 9 for external connection, having a height of approximately 3 μm to 50 μm, are formed at predetermined positions on the wiring pattern 7. Next, a second insulating layer 8 is formed, which is in close contact with the wiring pattern 7 and the first insulating layer 5, and which covers the side face of the metal post 9 excluding the tip surface of the metal post 9. Next, the semiconductor element is resin-sealed with sealing resin 10 in a manner so as to expose the tip surface of the metal post 9, and an external connection terminal 14 is provided on the metal post 9.”)</p> <p>Furuya, [0029] (“Furthermore, as set forth in the foregoing claim 2, the surface of the second insulating layer 8 is formed in a manner so as be at a position lower</p>

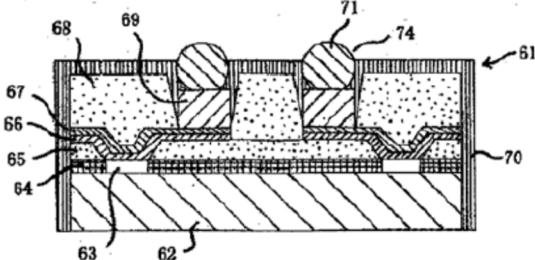
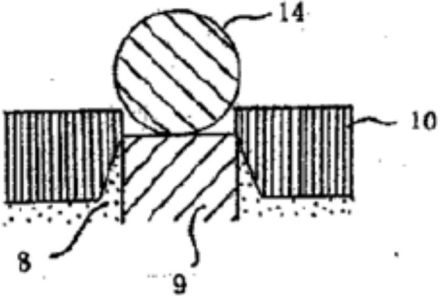
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	<p>than the tip surface of the metal post 9, so as not to present an obstacle when mounting the external connection terminal 14 to the outside (for example, on a mounting board).”)</p> <p>Furuya, [0036] (“Next, a characteristic of the semiconductor device 1 of the present invention, as shown in FIG. 1, is that an external connection terminal 14 that makes an external electrical connection (for example, to a mounting board) is placed at the tip end of the metal post 9, the external connection terminal 14 being configured with an electroconductive material provided on the surface of a support having a hollow part opened to the outside. That is to say, this is characterized in that stress applied to the semiconductor device due to the difference in the thermal expansion coefficients between the mounting board and the semiconductor device after mounting is mitigated by the external connection terminal 14, in which the electroconductive material 16 is provided on the surface of the support 15 having the hollow part opened to the outside, as shown in FIGS. 1, 2 and 3. Note that FIG. 2 is a view, seen from the side, of one example of the external connection terminal 14 according to the present invention, and FIG. 3 is a sectional view in which a section at the line A-A’ in FIG. 2 is seen from above (for example, seen from the mounting board side).”)</p> <p>Furuya, [0039] (“The present inventors conducted earnest study directed to preventing this and, as a result, discovered that, if the external connection terminal 14 is provided with a stress mitigating function, the stress produced by the difference the thermal expansion coefficients can be mitigated by the external connection terminal 14, whereby it is possible to prevent cracks and wire breakage from occurring in the semiconductor</p>

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	<p>device 1. That is to say, in order to provide a stress mitigating function, the external connection terminal 14 according to the present invention has an electroconductive material 16 formed on the surface of a hollow support 15. Because the hollow support 15 has a flexible structure, even if the mounting board that is connected to the external connection terminal 14 repeatedly thermally expands and contracts by a considerable amount, the stress generated can be absorbed and thus mitigated. Consequently, it is possible to prevent cracks from occurring, and to prevent wire breakage due to cracks in the insulating layer at the interface between and the sealing resin and the external connection terminal 14.”)</p> <p>Furuya, [0042] - [0043] (“Generally, when these are mounted and electrically connected to the outside (for example, to a mounting board), semiconductor devices such as CSPs and BGAs are mounted by thermocompression bonding with solder, a low melting point alloy, an anisotropic conductive film or the like. For this reason, the material for the support 15 comprised by the external connection terminal 14 according to the present invention is preferably a heat resistant engineering plastic. Here, engineering plastic refers to plastic that is heat resistant at 100°C or more, has a strength of 49 MPa or more, and has a flexural modulus of 2.4 Gpa or more. Materials satisfying the aforementioned conditions include polyimide, polyamide imide,</p> <p>Next, the semiconductor device 1 of the present invention performs fixation and electrical connection with the outside (for example, to a mounting board) by way of the external connection terminal 14, and an electroconductive material 16 is provided on the surface of the support 15 comprised by the external connection terminal 14. The</p>

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	<p>electroconductive material 16 must perform fixation with the outside and allow for electrical connection with the outside. Conductive materials 16 that satisfy such conditions are preferably selected from among the following (1) to (3):</p> <p>(1) a dispersion of graphite, carbon or metal fine particles;</p> <p>(2) gold, silver, copper, aluminum or nickel alone, or an alloy containing two or more of said metals; and</p> <p>(3) a low melting point alloy having tin or lead as a principal component.”)</p> <p>Furuya, [0044] (“Note that the low melting point alloys mentioned above include those employing metals such as mercury, gallium, or indium, but a solder alloy having tin or lead as a main component is preferable from the viewpoint of manufacturing costs and the like. Eutectic solder or high-melting point solder with an increased lead ratio can suitably be used as the solder alloy, and if necessary bismuth, cadmium, antimony, zinc, manganese, indium, tin, silver and the like may be added. Note that, in order to improve the adhesion between the support 15 and the electroconductive material 16, as shown in FIG. 2 and FIG. 3, a bonding layer 17 may be formed on the surface of the support 15, prior to providing the conductive material 16 thereon.”)</p> <p>Furuya, [0045] (“As an example of the external connection terminal 14 according to the present invention, an example may be cited in which a cylindrical polyimide having a hollow part and having an outer diameter of 100 μm to 1000 μm is used as the support 15, and a solder alloy having a thickness of several microns to several tens of microns is bonded on the surface of the support 15 as an electroconductive material 16, so as to form the</p>

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	<p>external connection terminal 14. Prior to bonding the electroconductive material 16 thereon, a bonding metal layer may be formed on the surface of the tube, as a bonding layer 17. Furthermore, the thickness of the electroconductive material 16 may be increased as necessary, and the length and diameter of the support 15 may be appropriately established to suit the specifications of the semiconductor device 1 and the like.”)</p> <p>Furuya, [0055] (“Next, the external connection terminal 14 was provided on the metal post 9 to produce the semiconductor device 1 (FIG. 4(f)). As shown in FIG. 2, the external connection terminal 14 used in the present embodiment is one in which eutectic solder is formed as the electroconductive material 16 on the surface of the hollow support 15, which is made of thermoplastic polyimide and is produced by the steps described below. First, a hollow thermoplastic polyimide tube having an inner diameter of 0.15 mm and a thickness of 50 μm was purchased in a long format. Next, metallic chromium and copper were sequentially laminated so as to form films on the tube surface (outside surface). Metallic chromium and copper serve as a bonding layer 17 when laminating the electroconductive material, and the films were formed by spluttering so as to produce a metallic chromium film thickness of 0.2 μm, and a copper film thickness of 0.4 μm. After forming the bonding layer 17, a plating was formed with eutectic solder having a film thickness of approximately 20 μm, as the electroconductive material 16. Next, after forming the eutectic solder, the long thermoplastic polyimide tube was cut to individual lengths of approximately 0.3 mm to produce the external connection terminals 14 shown in FIG. 2 and FIG. 3.”)</p> <p>Furuya, [Claim 7] (“The semiconductor device according to claim 3, 4, 5 or 6, characterized in that the</p>

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		<p>electroconductive material comprised by the external connection terminal is selected from among the following (1) to (3):</p> <p>(1) a dispersion of graphite, carbon or metal fine particles;</p> <p>(2) gold, silver, copper, aluminum or nickel alone, or an alloy containing two or more of said metals; and</p> <p>(3) a low melting point alloy having tin or lead as a principal component.”)</p> <p>Furuya, Figs. 1-3, 4(a)-(f), and 6-8.</p> <p>[FIG. 1]</p>  <p>[FIG. 2]</p>  <p>[FIG. 3]</p> 

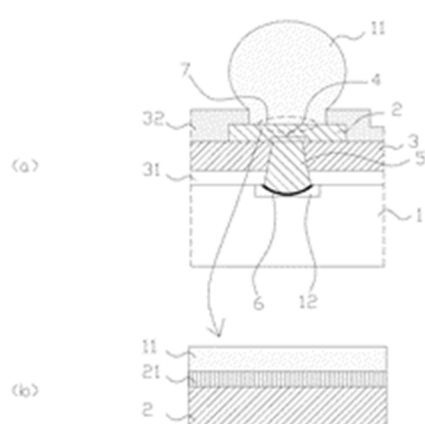
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	<p data-bbox="776 367 863 394">[FIG. 6]</p>  <p data-bbox="706 741 831 772">[FIG. 7]</p>  <p data-bbox="524 1144 1364 1350">Takizawa also discloses a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal component.</p> <p data-bbox="524 1396 1383 1860">Takizawa, [0003] (“As illustrated in FIG. 7(a), a conventional semiconductor device, includes: a wiring part 2 containing copper connected to a semiconductor chip 1, a solder ball 101 containing tin bonded to a land 7 formed on a surface of the wiring part 2, and a film substrate 3 that contacts the wiring part 2 on an opposite side surface as the bonding surface between the wiring part 2 and the solder ball 101, wherein a hole 4 is provided that passes through the film substrate 3 from the wiring part 2 to the surface on the opposite side as the bonding surface to the wiring part 2 of the film</p>

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	<p>substrate 3, a metal 5 is filled into the hole 4, and a gold layer 6 is formed on the metal 5 surface of the opening part of the hole 4. Furthermore, the land 7 is a hole provided on the wiring part 2 by shaving a predetermined location of the resist 32 in order to dispose a solder ball 101, and a Au layer 8 is formed on the surface of the land 7. Note that the Au layer 8 is illustrated in FIG. 7, but this Au layer 8 is thought to diffuse into the solder ball 101 by heat treatment of temperature cycle testing or the like performed after manufacturing this device, and it is hypothesized that the Au layer is not disposed on the wiring part 8 [Translator's note: presumably wiring part 2] after heat treatment. FIG. 8 illustrates an expanded view of the on the part between the wiring part 2 and the solder ball 101 illustrated in FIG. 7(a). Note that FIG. 8 illustrates an example (schematic diagram) of a conventional semiconductor device where the solder ball 101 is formed from a Sn-Pb eutectic solder (Sn content: 63%, Pb content: 37%). With the conventional semiconductor device illustrated in FIG. 7(a), the solder ball 101 and the printed board 34 are bonded as illustrated in FIG. 7(c).")</p> <p>Takizawa, [0009] ("MEANS FOR SOLVING THE PROBLEMS The first invention of the present application provided to resolve the aforementioned problem is a semiconductor device, comprising: a wiring part 2 containing copper connected to a semiconductor chip, and a solder ball 11 containing tin bonded to the wiring part 2; wherein a Cu-Sn alloy layer 21 with a thickness of approximately 1.87 μm or more is formed on the bonding part of the solder ball 11 and the wiring part 2.")</p> <p>Takizawa, [0033]-[0035] ("[0033]</p>

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	<p>DESCRIPTION OF THE PREFERRED EMBODIMENTS</p> <p>The semiconductor device according to the embodiment of the present invention is described below while referring to the drawings, but the following embodiments are only an example of the semiconductor device of the present invention. FIG. 1 is a cross-sectional view showing the semiconductor device according to one embodiment of the present invention. In regards to the semiconductor device shown in FIG. 1, FIG. 2 is an enlarged cross-sectional view of a solder ball part 11 when using a solder ball made from an eutectic solder (SN content ratio: 63%, PB content ratio: 37%) as the solder ball 11. FIG. 3 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 4 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 5 is a figure showing measurement results of the shear strength for a bonding part between a wiring part 7 and the solder ball 11 after bonding a printed board and the solder ball according to a process illustrated in FIG. 4(i) after maintaining the device provided by the process illustrated in FIG. 3 and FIG. 4 (a) to (g) in an N₂ environment for a predetermined time at a temperature above the melting point of the solder ball according to a process illustrated in FIG. 4 (h) using the solder ball made from the Sn-Cu eutectic solder as the solder ball 11. FIG. 6 is a figure showing one example of the measurement method of the shear strength shown in FIG. 5.</p> <p>[0034]</p> <p>As illustrated in FIG. 1(a), the semiconductor device according to the present embodiment has the wiring part 2 containing Cu that is connected to a semiconductor chip 1</p>

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	<p>and the solder ball 11 containing Sn that is connected to the wiring part 2.</p> <p>In other words, the semiconductor device according to the present embodiment has the wiring part 4 containing Cu that is connected to the semiconductor chip 1, the solder ball 11 containing Sn connected to a main surface of the wiring part 4, and a film substrate 3 that is connected to the wiring part 2 that is the opposite side surface of the bonding surface between the wiring part 2 and the solder ball 11, is provided with a hole 4 that passes through the film substrate 3 from the wiring part 2 to the opposite side surface of the bonding part between the film substrate 3 and the wiring part 2, a metal 5 is filled in the hole 4, and an Au layer 6 is formed on a surface of the metal 5 of an opening part of the hole 4.</p> <p>Note, the hole 4 is placed directly above an electrode part 12 that is placed on the semiconductor chip 1 on the semiconductor device according to the present embodiment, and the solder ball 11 and the electrode part 12 are connected by the metal 5 filled in the hole 4, but the solder ball 11 does not have to be placed directly above the electrode part 12. Furthermore, as illustrated in FIG. 1(c), the solder ball 11 and the printed board 34 are connected in the semiconductor device according to the present embodiment illustrated in FIG. 1(a).</p> <p>[0035]</p> <p>Furthermore, SN is a main component in the solder ball, and the solder ball is formed, for example, using Pb free solder or the like containing Ag, Cu, An, Bi, Ni, Cd, S, As, Zn, and the like with Sn-Pb alloy, Sn-Ag alloy, or Sn as a main constituent. Furthermore, in regards to FIG. 1(a), a figure in which the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 vicinity is illustrated enlarged in FIG. 1(b). As illustrated in FIG. 1(b), a strong Cu-Sn alloy layer is</p>

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	<p>formed on the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 portion on which the solder ball 11 is placed on the wiring part 2. As described above, detachment of the solder ball 11 caused by fractures and cracks can be reduced by reducing the occurrence of fractures and cracks near the bonding part by providing the Cu-Sn alloy layer on the bonding part between the solder ball 11 and the wiring part 2. As a result, productivity of the semiconductor device can be improved, and yield can be further increased. The Cu-Sn alloy layer preferably has a thickness of 1.87 μm or more, more preferably a thickness of 2 μm or more, and even more preferably a thickness of 3 μm or more, in order to reduce the occurrence of fractures and cracks in the vicinity of the bonding part.”)</p> <p>Takizawa, [0037] (“Next, a manufacturing process of the semiconductor device illustrated in FIG. 1 is described while referring to FIG. 3 and FIG. 4. First, one manufacturing process in which the wiring part 2 is placed on the film substrate 3 is described while referring to FIG. 3. As illustrated in FIG. 3(a), the wiring part 2 containing Cu is placed on one main surface of the film substrate. Furthermore, an adhesive is applied on the opposite side surface of the wiring part 2 of the film substrate 3. A material such as polyimide or the like that can withstand temperatures of 250°C or higher is used as the film substrate 3 and a polyimide is used for the adhesive agent 31. Next, the wiring part 2 on the film substrate 3 illustrated in FIG. 3(a) is patterned with a predetermined shape (refer to FIG. 3(b)), and a resist 32 is applied to a surface that is exposed on the outer part of the film substrate and the wiring part 2 (refer to FIG. 3 (c)). The hole 4 that passes through the film substrate 3 is formed from the adhesive 31 to the wiring part 2. A tool</p>

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		<p>such as a laser or the like is used to form the hole 4. A metal 5 such as Cu or Al is filled in the hole 4 (refer to FIG. 3(e)), and the Au layer 6 is formed on the surface of the metal 5 at the opening part of the hole 4 (refer to FIG. 3 (f)). A tape substrate 33 having the film substrate 3 on which the wiring part 2 is formed on one main surface is provided by the aforementioned process. Note, FIG. 3 illustrates one enlarged land 7 provided on the film substrate 3, and a plurality of lands 7 for placing the solder ball 101 are provided on the film substrate 3 in a later process.”)</p> <p>Takizawa, [0044] (“Note, the material for the solder ball 11 in the present example was Sn-Pb eutectic solder, but the material for the solder ball 11 is not restricted to this, and can be any material as long as the material contains Sn, and can, for example, have Sn-Ag alloy or Sn as a main component, and Pb free solders or the like containing Ag, Cu, Zn, Cd, Ni, S, As, or Bi can be used.”)</p> <p>Takizawa, Figures 1a-1c; 2a-2b:</p> <p>[FIG. 1]</p>  <p>FIG. 1 consists of two cross-sectional views, (a) and (b). View (a) shows a solder ball 11 positioned on a wiring part 2 of a tape substrate 33. The tape substrate 33 is shown with a film substrate 3 and a land 7. The wiring part 2 is formed on the film substrate 3. The solder ball 11 is in contact with the wiring part 2. View (b) shows a cross-section of the solder ball 11 and the wiring part 2, with labels 11, 21, and 2 indicating different layers or components.</p>

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		<p>(c)</p> <p>[FIG. 2]</p> <p>(a) (b)</p> <p>22 Sn 11 23 Pb agglomerate 21 Cu-Sn alloy layer 2 3 4 5 6 7 12 31 32 33 34</p>
1D	a diffusion layer formed between said first electrode portion and said second electrode portion	<p>Furuya discloses a diffusion layer formed between said first electrode portion and said second electrode portion:</p> <p>Furuya, [0007] (“In many cases, the connection between the metal post 69 and the outside (for example, the mounting board) is made by thermocompression bonding using solder, but at this time, if high temperatures of, for example, 180°C to 250°C are reached, some of the metal post 69 will dissolve and dissipate in the solder. In consideration for this dissolution and dissipation, the height of the metal post 69 is generally approximately 3 μm to 50 μm.”)</p> <p>Furuya, [0042]-[0043] (“Generally, when these are mounted and electrically connected to the outside (for example, to a mounting board), semiconductor devices such as CSPs and BGAs are mounted by thermocompression bonding with solder, a low melting point alloy, an anisotropic conductive film or the like. For</p>

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	<p>this reason, the material for the support 15 comprised by the external connection terminal 14 according to the present invention is preferably a heat resistant engineering plastic. Here, engineering plastic refers to plastic that is heat resistant at 100°C or more, has a strength of 49 MPa or more, and has a flexural modulus of 2.4 Gpa or more. Materials satisfying the aforementioned conditions include polyimide, polyamide imide,</p> <p>Next, the semiconductor device 1 of the present invention performs fixation and electrical connection with the outside (for example, to a mounting board) by way of the external connection terminal 14, and an electroconductive material 16 is provided on the surface of the support 15 comprised by the external connection terminal 14. The electroconductive material 16 must perform fixation with the outside and allow for electrical connection with the outside. Conductive materials 16 that satisfy such conditions are preferably selected from among the following (1) to (3):</p> <p>(1) a dispersion of graphite, carbon or metal fine particles;</p> <p>(2) gold, silver, copper, aluminum or nickel alone, or an alloy containing two or more of said metals; and</p> <p>(3) a low melting point alloy having tin or lead as a principal component.”)</p> <p>Takizawa also discloses a diffusion layer formed between said first electrode portion and said second electrode portion:</p> <p>Takizawa, [0003] (“As illustrated in FIG. 7(a), a conventional semiconductor device, includes: a wiring part 2 containing copper connected to a semiconductor chip 1, a solder ball 101 containing tin bonded to a land 7 formed on a surface of the wiring part 2, and a film substrate 3 that contacts the wiring part 2 on an opposite</p>

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	<p>side surface as the bonding surface between the wiring part 2 and the solder ball 101, wherein a hole 4 is provided that passes through the film substrate 3 from the wiring part 2 to the surface on the opposite side as the bonding surface to the wiring part 2 of the film substrate 3, a metal 5 is filled into the hole 4, and a gold layer 6 is formed on the metal 5 surface of the opening part of the hole 4. Furthermore, the land 7 is a hole provided on the wiring part 2 by shaving a predetermined location of the resist 32 in order to dispose a solder ball 101, and a Au layer 8 is formed on the surface of the land 7. Note that the Au layer 8 is illustrated in FIG. 7, but this Au layer 8 is thought to diffuse into the solder ball 101 by heat treatment of temperature cycle testing or the like performed after manufacturing this device, and it is hypothesized that the Au layer is not disposed on the wiring part 8 [Translator's note: presumably wiring part 2] after heat treatment. FIG. 8 illustrates an expanded view of the on the part between the wiring part 2 and the solder ball 101 illustrated in FIG. 7(a). Note that FIG. 8 illustrates an example (schematic diagram) of a conventional semiconductor device where the solder ball 101 is formed from a Sn-Pb eutectic solder (Sn content: 63%, Pb content: 37%). With the conventional semiconductor device illustrated in FIG. 7(a), the solder ball 101 and the printed board 34 are bonded as illustrated in FIG. 7(c).</p> <p>Takizawa, [0008]-[0010] (“[0008] In order to resolve the aforementioned problems, the present inventors performed extensive research related to improving the strength of the bonding part between the solder ball and the land ... Furthermore, the present inventors conceived of a method of manufacturing the semiconductor device of the present invention based on a concept that a Cu-Sn alloy layer with sufficient thickness</p>

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	<p>to prevent detachment of the solder ball can be formed on the bonding part by maintaining the semiconductor device with a solder ball provided on a land provided on the wiring part in an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.</p> <p>[0009]</p> <p>MEANS FOR SOLVING THE PROBLEMS</p> <p>The first invention of the present application provided to resolve the aforementioned problem is a semiconductor device, comprising: a wiring part 2 containing copper connected to a semiconductor chip, and a solder ball 11 containing tin bonded to the wiring part 2; wherein a Cu-Sn alloy layer 21 with a thickness of approximately 1.87 μm or more is formed on the bonding part of the solder ball 11 and the wiring part 2.</p> <p>[0010]</p> <p>Herein, if the Cu-Sn alloy layer formed on the bonding part of the wiring part of the solder ball has a thickness that is less than approximately 1.87 μm, the bonding part between the solder ball and the wiring part cannot have sufficient strength, there will be a possibility of breaking or cracking occurring to the bonding part during temperature cycle testing or the like, and preventing detachment of the solder ball will not be possible, so it is conceivable that the yield will drop. The semiconductor device of the first invention of the present application having the aforementioned configuration can reduce detachment of the solder ball caused by breaking or cracking in order to be able to reduce the occurrence of fractures and cracks near the bonding part by providing a wiring part containing copper connected to a semiconductor chip, and a solder ball containing tin bonded to the wiring part; wherein a Cu-Sn alloy layer with a thickness of approximately 1.87 μm or more is</p>

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	<p>formed on the bonding part of the solder ball and the wiring part, and has a wiring part containing Cu connected to the semiconductor chip and a solder ball containing Sn bonded to the wiring part. Thereby, a semiconductor device can be obtained with favorable yield and that increases the reliability of the bonding part and increases the productivity of the semiconductor device.”)</p> <p>Takizawa, [0020] (“Herein, the predetermined time refers to the time sufficient for increasing the strain of the bonding part between the solder ball and the wiring part. The method of manufacturing the semiconductor device the sixth invention of the present application with the aforementioned configuration can cause the Sn in the solder ball to liquid phase diffuse to the Cu in the wiring part and form a Cu-SN alloy layer with sufficient thickness to prevent detachment of the solder ball neared the bonding part, and therefore can increase the strength of the bonding parts, and can reduce the occurrence rate of fractures and cracks near the bonding part by disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time. Thereby the occurrence of defects due to the occurrence of raking and cracking can be reduced so the productivity of the semiconductor device can be enhanced.”)</p> <p>Takizawa, [0033]-[0035] (“[0033] DESCRIPTION OF THE PREFERRED EMBODIMENTS</p>

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	<p>The semiconductor device according to the embodiment of the present invention is described below while referring to the drawings, but the following embodiments are only an example of the semiconductor device of the present invention. FIG. 1 is a cross-sectional view showing the semiconductor device according to one embodiment of the present invention. In regards to the semiconductor device shown in FIG. 1, FIG. 2 is an enlarged cross-sectional view of a solder ball part 11 when using a solder ball made from an eutectic solder (SN content ratio: 63%, PB content ratio: 37%) as the solder ball 11. FIG. 3 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 4 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 5 is a figure showing measurement results of the shear strength for a bonding part between a wiring part 7 and the solder ball 11 after bonding a printed board and the solder ball according to a process illustrated in FIG. 4(i) after maintaining the device provided by the process illustrated in FIG. 3 and FIG. 4 (a) to (g) in an N₂ environment for a predetermined time at a temperature above the melting point of the solder ball according to a process illustrated in FIG. 4 (h) using the solder ball made from the Sn-Cu eutectic solder as the solder ball 11. FIG. 6 is a figure showing one example of the measurement method of the shear strength shown in FIG. 5.</p> <p>[0034]</p> <p>As illustrated in FIG. 1(a), the semiconductor device according to the present embodiment has the wiring part 2 containing Cu that is connected to a semiconductor chip 1 and the solder ball 11 containing Sn that is connected to the wiring part 2.</p>

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	<p>In other words, the semiconductor device according to the present embodiment has the wiring part 4 containing Cu that is connected to the semiconductor chip 1, the solder ball 11 containing Sn connected to a main surface of the wiring part 4, and a film substrate 3 that is connected to the wiring part 2 that is the opposite side surface of the bonding surface between the wiring part 2 and the solder ball 11, is provided with a hole 4 that passes through the film substrate 3 from the wiring part 2 to the opposite side surface of the bonding part between the film substrate 3 and the wiring part 2, a metal 5 is filled in the hole 4, and an Au layer 6 is formed on a surface of the metal 5 of an opening part of the hole 4.</p> <p>Note, the hole 4 is placed directly above an electrode part 12 that is placed on the semiconductor chip 1 on the semiconductor device according to the present embodiment, and the solder ball 11 and the electrode part 12 are connected by the metal 5 filled in the hole 4, but the solder ball 11 does not have to be placed directly above the electrode part 12. Furthermore, as illustrated in FIG. 1(c), the solder ball 11 and the printed board 34 are connected in the semiconductor device according to the present embodiment illustrated in FIG. 1(a).</p> <p>[0035]</p> <p>Furthermore, SN is a main component in the solder ball, and the solder ball is formed, for example, using Pb free solder or the like containing Ag, Cu, An, Bi, Ni, Cd, S, As, Zn, and the like with Sn-Pb alloy, Sn-Ag alloy, or Sn as a main constituent. Furthermore, in regards to FIG. 1(a), a figure in which the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 vicinity is illustrated enlarged in FIG. 1(b). As illustrated in FIG. 1(b), a strong Cu-Sn alloy layer is formed on the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 portion on which the solder ball 11 is placed on the wiring part 2.</p>

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	<p>As described above, detachment of the solder ball 11 caused by fractures and cracks can be reduced by reducing the occurrence of fractures and cracks near the bonding part by providing the Cu-Sn alloy layer on the bonding part between the solder ball 11 and the wiring part 2. As a result, productivity of the semiconductor device can be improved, and yield can be further increased. The Cu-Sn alloy layer preferably has a thickness of 1.87 μm or more, more preferably a thickness of 2 μm or more, and even more preferably a thickness of 3 μm or more, in order to reduce the occurrence of fractures and cracks in the vicinity of the bonding part.”)</p> <p>Takizawa, [0038] (“Next, one manufacturing process for providing the solder ball 11 using the tape substrate 33 provided by the process illustrated in FIG. 3 is described while referring to FIG. 4. The tape substrate 33 provided by the process illustrated in FIG. 3 is provided on the surface where the Au layer 6 was provided (refer to FIG. 4(a)), and a stiffener 41 made from Cu, stainless steel, or the like is attached to both ends of the tape substrate 33 (refer to FIG. 4 (b)). The semiconductor chip 1 is provided between the 2 stiffeners 41, and the Au layer 6 and the electrode part made from Al or the like placed on the semiconductor chip 1 are bonded (refer to FIG. 4(c)). The connection is performed by combining heat and ultrasound using a bonding tool. Next, as needed, reinforcement of the bonding part between the tape substrate 33 and the semiconductor chip 1 is performed (refer to FIG. 4(d)) by injecting reinforcement resin 42 between the tape substrate 33 and the semiconductor chip 1 in order to cure. Liquid resin such as epoxy resin or the like is used as the reinforcement resin 42. In regards to the semiconductor chip 1, a lid part 43 made from Cu, Al, Si, C, or the like is placed on a surface that is on the</p>

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	<p>opposite side of the surface connected to the tape substrate 33, and sealing is performed under normal pressure (refer to FIG. 4(e)). When this occurs, a conductive adhesive 44 such as Ag paste, Cu paste, or the like is applied on the surface of the lid part 43 connected to the semiconductor chip 1, and sealing under normal pressure is performed using a belt furnace or an oven while heat curing the related conductive adhesive 44 by sealing. The land 7 (not illustrated in the figures) for placing the solder ball 11 is provided by forming a groove by performing etching or the like on a predetermined location of the resist 32 placed on the film substrate 3 of the tape substrate 33, the solder ball 11 is attached (refer to FIG. 4(f)) to</p> <p>each land 7 which are on the wiring part 2 placed on the tape substrate 33 while performing decompression suctioning, a flux (not illustrated in the figures) is applied to the surrounding of the bonding part between the solder ball 11 and the land 7, and the land 7 and the solder ball 11 are connected by reflowing the solder ball 11. Next, if necessary, the flux used in the aforementioned process is washed off. The device provided by the aforementioned processes (refer to FIG. 4(g)) is maintained for a predetermined time at a temperature that is above the melting point of the solder ball 11 that is in an inert environment or a reducing environment (refer to FIG. 4(h)). Sorting, inspection, and the like are performed on the device provided by the process above after performing temperature cycle testing in order to determine operating characteristics and durability towards physical damage and the like, the device is mounted to the printed board 34 by bonding the printed board 34 and the solder ball 11 by reflowing the solder ball 11 (refer to FIG. 4(i)) in order to provide the semiconductor device which is the final product. As described above, Sn in the solder ball 11 and Cu in the land 7 are alloyed and Cu-Sn alloy is formed in</p>

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	<p>the vicinity of the bonding part between the solder ball 11 and the land 7 by maintaining the device illustrated in FIG. 4(g) at a temperature that is above the melting point of the solder ball 11 in an inert environment or a reducing environment for a predetermined amount of time. Herein, inert environment refers to a gas that does not react with the solder ball 11 and the land part 7, such as, N₂, Ar, He, Ne, and the like, or a mixture of these, and a reducing environment refers to gas that has reducibility, such as CO, H₂, or the like. As described above, the occurrence rate of fractures and cracks in the vicinity of the bonding part between the solder ball 11 that is also connected to the printed board 34 and the wiring part 2 can be reduced since the solder ball 11 can improve strength of the bonding part between the solder ball 11 and the wiring part 2 in the process illustrated in FIG. 4(i) since Sn in the solder ball 11 is liquid phase diffused into a Cu matrix of the wiring part 2 and a Cu-Sn alloy layer that has a thickness sufficient to prevent detachment of the solder ball 11 in the vicinity of the bonding part by maintaining the device for a predetermined period of time at a temperature that is above the melting point of the solder ball 11 in an inert environment or a reducing environment. Thereby, productivity of the semiconductor device can be improved since the occurrence of defective parts due to the occurrence of fractures and cracks can be reduced.”)</p> <p>Takizawa, [0040] (“[Example 1] The semiconductor device of the present embodiment illustrated in FIG. 1 is an example using a solder ball made from Sn-Pb eutectic solder (Sn content ratio: 63%, Pb content ratio: 37%) as the solder ball 11. FIG. 2 illustrates an enlarged view of the solder ball 11 portion according to the present example. As shown in FIG. 2, a Cu-Sn alloy layer was formed in the vicinity of the</p>

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	<p>bonding part between the solder ball 11 and the wiring part 2. In regards to the solder ball 11 provided on the semiconductor device of the present invention illustrated in FIG. 2, 1.87 to 4.0 μm of the Cu-Sn alloy layer was formed on each solder ball 11, and in particular, many solder balls were formed with 3.0 to 4.0 μm of the Cu-Sn alloy layer. On the other hand, 1.00 to 1.50 μm of the Cu-Sn alloy layer was formed on the solder ball 101 placed on the conventional semiconductor device illustrated in FIG. 8. Thereby, it was revealed that the semiconductor device of the present invention illustrated in FIG. 2 was formed with a strong Cu-Sn alloy layer that was thicker. Forming the Cu-Sn alloy layer with a thickness of at least 1.87 μm or more was preferable in order to prevent detachment of the solder ball 11. Thereby, the occurrence ratio of fractures and cracks in the vicinity of the bonding part could be reduced since strength of the bonding part between the solder ball 11 and the wiring part 2 was strengthened by forming the Cu-Sn alloy layer with sufficient thickness in the vicinity of the bonding part. Thereby, a device with favorable yield could be provided since the occurrence of defective parts caused by the occurrence of fractures and cracks could be reduced.”)</p> <p>Takizawa, Figures 1a-1c; 2a-2b:</p>

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		<p>[FIG. 1]</p> <p>[FIG. 2]</p>
1E	wherein said diffusion layer comprises said first metal component and said	<p>Furuya discloses said diffusion layer comprises said first metal component and said second metal component</p> <p>Furuya, [0007] (“In many cases, the connection between the metal post 69 and the outside (for example, the mounting board) is made by thermocompression bonding using solder, but at this time, if high temperatures of, for example, 180°C to 250°C are reached, some of the metal post 69 will dissolve and dissipate in the solder. In</p>

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	second metal component	<p>consideration for this dissolution and dissipation, the height of the metal post 69 is generally approximately 3 μm to 50 μm.”)</p> <p>Furuya, [0042]-[0043] (“Generally, when these are mounted and electrically connected to the outside (for example, to a mounting board), semiconductor devices such as CSPs and BGAs are mounted by thermocompression bonding with solder, a low melting point alloy, an anisotropic conductive film or the like. For this reason, the material for the support 15 comprised by the external connection terminal 14 according to the present invention is preferably a heat resistant engineering plastic. Here, engineering plastic refers to plastic that is heat resistant at 100°C or more, has a strength of 49 MPa or more, and has a flexural modulus of 2.4 Gpa or more. Materials satisfying the aforementioned conditions include polyimide, polyamide imide,</p> <p>Next, the semiconductor device 1 of the present invention performs fixation and electrical connection with the outside (for example, to a mounting board) by way of the external connection terminal 14, and an electroconductive material 16 is provided on the surface of the support 15 comprised by the external connection terminal 14. The electroconductive material 16 must perform fixation with the outside and allow for electrical connection with the outside. Conductive materials 16 that satisfy such conditions are preferably selected from among the following (1) to (3):</p> <p>(1) a dispersion of graphite, carbon or metal fine particles;</p> <p>(2) gold, silver, copper, aluminum or nickel alone, or an alloy containing two or more of said metals; and</p> <p>(3) a low melting point alloy having tin or lead as a principal</p>

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	<p>component.”)</p> <p>Takizawa also discloses wherein said diffusion layer comprises said first metal component and said second metal component.</p> <p>Takizawa, [0003] (“As illustrated in FIG. 7(a), a conventional semiconductor device, includes: a wiring part 2 containing copper connected to a semiconductor chip 1, a solder ball 101 containing tin bonded to a land 7 formed on a surface of the wiring part 2, and a film substrate 3 that contacts the wiring part 2 on an opposite side surface as the bonding surface between the wiring part 2 and the solder ball 101, wherein a hole 4 is provided that passes through the film substrate 3 from the wiring part 2 to the surface on the opposite side as the bonding surface to the wiring part 2 of the film substrate 3, a metal 5 is filled into the hole 4, and a gold layer 6 is formed on the metal 5 surface of the opening part of the hole 4. Furthermore, the land 7 is a hole provided on the wiring part 2 by shaving a predetermined location of the resist 32 in order to dispose a solder ball 101, and a Au layer 8 is formed on the surface of the land 7. Note that the Au layer 8 is illustrated in FIG. 7, but this Au layer 8 is thought to diffuse into the solder ball 101 by heat treatment of temperature cycle testing or the like performed after manufacturing this device, and it is hypothesized that the Au layer is not disposed on the wiring part 8 [Translator’s note: presumably wiring part 2] after heat treatment. FIG. 8 illustrates an expanded view of the on the part between the wiring part 2 and the solder ball 101 illustrated in FIG. 7(a). Note that FIG. 8 illustrates an example (schematic diagram) of a conventional semiconductor device where the solder ball 101 is formed from a Sn-Pb eutectic solder (Sn content: 63%, Pb content: 37%). With the conventional</p>

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	<p>semiconductor device illustrated in FIG. 7(a), the solder ball 101 and the printed board 34 are bonded as illustrated in FIG. 7(c).</p> <p>Takizawa, [0008]-[0010] (“[0008] In order to resolve the aforementioned problems, the present inventors performed extensive research related to improving the strength of the bonding part between the solder ball and the land ... Furthermore, the present inventors conceived of a method of manufacturing the semiconductor device of the present invention based on a concept that a Cu-Sn alloy layer with sufficient thickness to prevent detachment of the solder ball can be formed on the bonding part by maintaining the semiconductor device with a solder ball provided on a land provided on the wiring part in an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time. [0009] MEANS FOR SOLVING THE PROBLEMS The first invention of the present application provided to resolve the aforementioned problem is a semiconductor device, comprising: a wiring part 2 containing copper connected to a semiconductor chip, and a solder ball 11 containing tin bonded to the wiring part 2; wherein a Cu-Sn alloy layer 21 with a thickness of approximately 1.87 μm or more is formed on the bonding part of the solder ball 11 and the wiring part 2.</p> <p>[0010] Herein, if the Cu-Sn alloy layer formed on the bonding part of the wiring part of the solder ball has a thickness that is less than approximately 1.87 μm, the bonding part between the solder ball and the wiring part cannot have sufficient strength, there will be a possibility of breaking or cracking occurring to the bonding part during</p>

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	<p>temperature cycle testing or the like, and preventing detachment of the solder ball will not be possible, so it is conceivable that the yield will drop. The semiconductor device of the first invention of the present application having the aforementioned configuration can reduce detachment of the solder ball caused by breaking or cracking in order to be able to reduce the occurrence of fractures and cracks near the bonding part by providing a wiring part containing copper connected to a semiconductor chip, and a solder ball containing tin bonded to the wiring part; wherein a Cu-Sn alloy layer with a thickness of approximately 1.87 μm or more is formed on the bonding part of the solder ball and the wiring part, and has a wiring part containing Cu connected to the semiconductor chip and a solder ball containing Sn bonded to the wiring part. Thereby, a semiconductor device can be obtained with favorable yield and that increases the reliability of the bonding part and increases the productivity of the semiconductor device.”)</p> <p>Takizawa, [0020] (“Herein, the predetermined time refers to the time sufficient for increasing the strain of the bonding part between the solder ball and the wiring part. The method of manufacturing the semiconductor device the sixth invention of the present application with the aforementioned configuration can cause the Sn in the solder ball to liquid phase diffuse to the Cu in the wiring part and form a Cu-SN alloy layer with sufficient thickness to prevent detachment of the solder ball neared the bonding part, and therefore can increase the strength of the bonding parts, and can reduce the occurrence rate of fractures and cracks near the bonding part by disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball</p>

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	<p>containing Sn on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time. Thereby the occurrence of defects due to the occurrence of raking and cracking can be reduced so the productivity of the semiconductor device can be enhanced.”)</p> <p>Takizawa, [0033]-[0035] (“[0033] DESCRIPTION OF THE PREFERRED EMBODIMENTS The semiconductor device according to the embodiment of the present invention is described below while referring to the drawings, but the following embodiments are only an example of the semiconductor device of the present invention. FIG. 1 is a cross-sectional view showing the semiconductor device according to one embodiment of the present invention. In regards to the semiconductor device shown in FIG. 1, FIG. 2 is an enlarged cross-sectional view of a solder ball part 11 when using a solder ball made from an eutectic solder (SN content ratio: 63%, PB content ratio: 37%) as the solder ball 11. FIG. 3 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 4 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 5 is a figure showing measurement results of the shear strength for a bonding part between a wiring part 7 and the solder ball 11 after bonding a printed board and the solder ball according to a process illustrated in FIG. 4(i) after maintaining the device provided by the process illustrated in FIG. 3 and FIG. 4 (a) to (g) in an N2 environment for a predetermined time at a temperature above the melting point of the solder ball according to a process illustrated</p>

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	<p>in FIG. 4 (h) using the solder ball made from the Sn-Cu eutectic solder as the solder ball 11.</p> <p>FIG. 6 is a figure showing one example of the measurement method of the shear strength shown in FIG. 5.</p> <p>[0034]</p> <p>As illustrated in FIG. 1(a), the semiconductor device according to the present embodiment has the wiring part 2 containing Cu that is connected to a semiconductor chip 1 and the solder ball 11 containing Sn that is connected to the wiring part 2.</p> <p>In other words, the semiconductor device according to the present embodiment has the wiring part 4 containing Cu that is connected to the semiconductor chip 1, the solder ball 11 containing Sn connected to a main surface of the wiring part 4, and a film substrate 3 that is connected to the wiring part 2 that is the opposite side surface of the bonding surface between the wiring part 2 and the solder ball 11, is provided with a hole 4 that passes through the film substrate 3 from the wiring part 2 to the opposite side surface of the bonding part between the film substrate 3 and the wiring part 2, a metal 5 is filled in the hole 4, and an Au layer 6 is formed on a surface of the metal 5 of an opening part of the hole 4.</p> <p>Note, the hole 4 is placed directly above an electrode part 12 that is placed on the semiconductor chip 1 on the semiconductor device according to the present embodiment, and the solder ball 11 and the electrode part 12 are connected by the metal 5 filled in the hole 4, but the solder ball 11 does not have to be placed directly above the electrode part 12. Furthermore, as illustrated in FIG. 1(c), the solder ball 11 and the printed board 34 are connected in the semiconductor device according to the present embodiment illustrated in FIG. 1(a).</p> <p>[0035]</p>

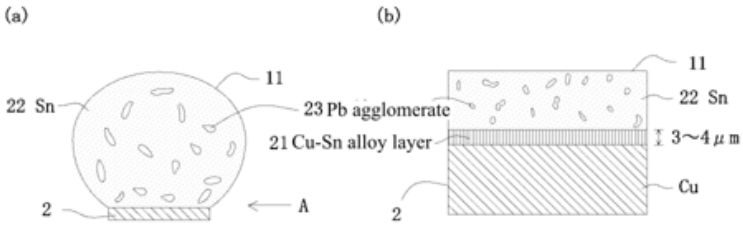
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	<p>Furthermore, SN is a main component in the solder ball, and the solder ball is formed, for example, using Pb free solder or the like containing Ag, Cu, An, Bi, Ni, Cd, S, As, Zn, and the like with Sn-Pb alloy, Sn-Ag alloy, or Sn as a main constituent. Furthermore, in regards to FIG. 1(a), a figure in which the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 vicinity is illustrated enlarged in FIG. 1(b). As illustrated in FIG. 1(b), a strong Cu-Sn alloy layer is formed on the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 portion on which the solder ball 11 is placed on the wiring part 2. As described above, detachment of the solder ball 11 caused by fractures and cracks can be reduced by reducing the occurrence of fractures and cracks near the bonding part by providing the Cu-Sn alloy layer on the bonding part between the solder ball 11 and the wiring part 2. As a result, productivity of the semiconductor device can be improved, and yield can be further increased. The Cu-Sn alloy layer preferably has a thickness of 1.87 μm or more, more preferably a thickness of 2 μm or more, and even more preferably a thickness of 3 μm or more, in order to reduce the occurrence of fractures and cracks in the vicinity of the bonding part.”)</p> <p>Takizawa, [0038] (“Next, one manufacturing process for providing the solder ball 11 using the tape substrate 33 provided by the process illustrated in FIG. 3 is described while referring to FIG. 4. The tape substrate 33 provided by the process illustrated in FIG. 3 is provided on the surface where the Au layer 6 was provided (refer to FIG. 4(a)), and a stiffener 41 made from Cu, stainless steel, or the like is attached to both ends of the tape substrate 33 (refer to FIG. 4 (b)). The semiconductor chip 1 is provided between the 2 stiffeners 41, and the Au layer 6</p>

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	<p>and the electrode part made from Al or the like placed on the semiconductor chip 1 are bonded (refer to FIG. 4(c)). The connection is performed by combining heat and ultrasound using a bonding tool. Next, as needed, reinforcement of the bonding part between the tape substrate 33 and the semiconductor chip 1 is performed (refer to FIG. 4(d)) by injecting reinforcement resin 42 between the tape substrate 33 and the semiconductor chip 1 in order to cure. Liquid resin such as epoxy resin or the like is used as the reinforcement resin 42. In regards to the semiconductor chip 1, a lid part 43 made from Cu, Al, Si, C, or the like is placed on a surface that is on the opposite side of the surface connected to the tape substrate 33, and sealing is performed under normal pressure (refer to FIG. 4(e)). When this occurs, a conductive adhesive 44 such as Ag paste, Cu paste, or the like is applied on the surface of the lid part 43 connected to the semiconductor chip 1, and sealing under normal pressure is performed using a belt furnace or an oven while heat curing the related conductive adhesive 44 by sealing. The land 7 (not illustrated in the figures) for placing the solder ball 11 is provided by forming a groove by performing etching or the like on a predetermined location of the resist 32 placed on the film substrate 3 of the tape substrate 33, the solder ball 11 is attached (refer to FIG. 4(f)) to each land 7 which are on the wiring part 2 placed on the tape substrate 33 while performing decompression suctioning, a flux (not illustrated in the figures) is applied to the surrounding of the bonding part between the solder ball 11 and the land 7, and the land 7 and the solder ball 11 are connected by reflowing the solder ball 11. Next, if necessary, the flux used in the aforementioned process is washed off. The device provided by the aforementioned processes (refer to FIG. 4(g)) is maintained for a predetermined time at a temperature that is above the</p>

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	<p>melting point of the solder ball 11 that is in an inert environment or a reducing environment (refer to FIG. 4(h)). Sorting, inspection, and the like are performed on the device provided by the process above after performing temperature cycle testing in order to determine operating characteristics and durability towards physical damage and the like, the device is mounted to the printed board 34 by bonding the printed board 34 and the solder ball 11 by reflowing the solder ball 11 (refer to FIG. 4(i)) in order to provide the semiconductor device which is the final product. As described above, Sn in the solder ball 11 and Cu in the land 7 are alloyed and Cu-Sn alloy is formed in the vicinity of the bonding part between the solder ball 11 and the land 7 by maintaining the device illustrated in FIG. 4(g) at a temperature that is above the melting point of the solder ball 11 in an inert environment or a reducing environment for a predetermined amount of time. Herein, inert environment refers to a gas that does not react with the solder ball 11 and the land part 7, such as, N₂, Ar, He, Ne, and the like, or a mixture of these, and a reducing environment refers to gas that has reducibility, such as CO, H₂, or the like. As described above, the occurrence rate of fractures and cracks in the vicinity of the bonding part between the solder ball 11 that is also connected to the printed board 34 and the wiring part 2 can be reduced since the solder ball 11 can improve strength of the bonding part between the solder ball 11 and the wiring part 2 in the process illustrated in FIG. 4(i) since Sn in the solder ball 11 is liquid phase diffused into a Cu matrix of the wiring part 2 and a Cu-Sn alloy layer that has a thickness sufficient to prevent detachment of the solder ball 11 in the vicinity of the bonding part by maintaining the device for a predetermined period of time at a temperature that is above the melting point of the solder ball 11 in an inert environment or a reducing environment. Thereby, productivity of the semiconductor</p>

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	<p>device can be improved since the occurrence of defective parts due to the occurrence of fractures and cracks can be reduced.”)</p> <p>Takizawa, [0040] (“[Example 1] The semiconductor device of the present embodiment illustrated in FIG. 1 is an example using a solder ball made from Sn-Pb eutectic solder (Sn content ratio: 63%, Pb content ratio: 37%) as the solder ball 11. FIG. 2 illustrates an enlarged view of the solder ball 11 portion according to the present example. As shown in FIG. 2, a Cu-Sn alloy layer was formed in the vicinity of the bonding part between the solder ball 11 and the wiring part 2. In regards to the solder ball 11 provided on the semiconductor device of the present invention illustrated in FIG. 2, 1.87 to 4.0 μm of the Cu-Sn alloy layer was formed on each solder ball 11, and in particular, many solder balls were formed with 3.0 to 4.0 μm of the Cu-Sn alloy layer. On the other hand, 1.00 to 1.50 μm of the Cu-Sn alloy layer was formed on the solder ball 101 placed on the conventional semiconductor device illustrated in FIG. 8. Thereby, it was revealed that the semiconductor device of the present invention illustrated in FIG. 2 was formed with a strong Cu-Sn alloy layer that was thicker. Forming the Cu-Sn alloy layer with a thickness of at least 1.87 μm or more was preferable in order to prevent detachment of the solder ball 11. Thereby, the occurrence ratio of fractures and cracks in the vicinity of the bonding part could be reduced since strength of the bonding part between the solder ball 11 and the wiring part 2 was strengthened by forming the Cu-Sn alloy layer with sufficient thickness in the vicinity of the bonding part. Thereby, a device with favorable yield could be provided since the occurrence of defective parts caused by the occurrence of fractures and cracks could be reduced.”)</p>

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		<p>Takizawa, [0044] (“Note, the material for the solder ball 11 in the present example was Sn-Pb eutectic solder, but the material for the solder ball 11 is not restricted to this, and can be any material as long as the material contains Sn, and can, for example, have Sn-Ag alloy or Sn as a main component, and Pb free solders or the like containing Ag, Cu, Zn, Cd, Ni, S, As, or Bi can be used.”)</p> <p>Takizawa, Figures 1a-1c; 2a-2b:</p> <p>[FIG. 1]</p> <p>FIG. 1 consists of three cross-sectional views labeled (a), (b), and (c). View (a) shows a solder ball 11 on a substrate 1. The substrate 1 has a central opening 12. A solder ball 11 is positioned on a layer 2, which is on top of a layer 3. Layer 3 is on top of a layer 4, which is on top of a layer 5. Layer 5 is on top of a layer 6, which is on top of a layer 7. A layer 12 is on top of the solder ball 11. A layer 31 is on top of the solder ball 11. A layer 32 is on top of the solder ball 11. A layer 4 is on top of the solder ball 11. A layer 5 is on top of the solder ball 11. A layer 6 is on top of the solder ball 11. A layer 7 is on top of the solder ball 11. A layer 12 is on top of the solder ball 11. A layer 31 is on top of the solder ball 11. A layer 32 is on top of the solder ball 11. View (b) shows a cross-section of the solder ball 11 on a substrate 2. The solder ball 11 is on a layer 21, which is on top of a layer 2. View (c) shows a cross-section of the solder ball 11 on a substrate 34. The solder ball 11 is on a layer 1, which is on top of a layer 2. Layer 2 is on top of a layer 3. Layer 3 is on top of a layer 4. Layer 4 is on top of a layer 5. Layer 5 is on top of a layer 6. Layer 6 is on top of a layer 7. A layer 12 is on top of the solder ball 11. A layer 31 is on top of the solder ball 11. A layer 32 is on top of the solder ball 11. A layer 4 is on top of the solder ball 11. A layer 5 is on top of the solder ball 11. A layer 6 is on top of the solder ball 11. A layer 7 is on top of the solder ball 11. A layer 12 is on top of the solder ball 11. A layer 31 is on top of the solder ball 11. A layer 32 is on top of the solder ball 11.</p>

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		<p style="text-align: center;">[FIG. 2]</p> 
	Claim 2	
2	<p>The semiconductor device of claim 1, wherein said first metal component includes copper and said second metal component includes tin</p>	<p>Furuya discloses wherein said first metal component includes copper and said second metal component includes tin.</p> <p>Furuya, [0035] (“Next, the material for the wiring pattern 7 is desirably a material with good conductivity and, for example, copper, silver, aluminum, alloys thereof, other metals that are good conductors or the like can be used. If copper, silver, or the like is used as the material for the wiring pattern 7, prior to the formation of the wiring pattern 7, it is preferable to form a metal barrier layer 6 made of a TiW alloy, TiN, TaN, W, Cr or the like as an undercoat layer, and then form the wiring pattern 7 on the metal barrier layer 6.”)</p> <p>Furuya, [0042]-[0043] (“Generally, when these are mounted and electrically connected to the outside (for example, to a mounting board), semiconductor devices such as CSPs and BGAs are mounted by thermocompression bonding with solder, a low melting point alloy, an anisotropic conductive film or the like. For this reason, the material for the support 15 comprised by the external connection terminal 14 according to the present invention is preferably a heat resistant engineering plastic. Here, engineering plastic refers to plastic that is heat resistant at 100°C or more, has a strength of 49 MPa or more, and has a flexural modulus of 2.4 Gpa or more. Materials satisfying the</p>

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	<p>aforementioned conditions include polyimide, polyamide imide,</p> <p>Next, the semiconductor device 1 of the present invention performs fixation and electrical connection with the outside (for example, to a mounting board) by way of the external connection terminal 14, and an electroconductive material 16 is provided on the surface of the support 15 comprised by the external connection terminal 14. The electroconductive material 16 must perform fixation with the outside and allow for electrical connection with the outside. Conductive materials 16 that satisfy such conditions are preferably selected from among the following (1) to (3):</p> <p>(1) a dispersion of graphite, carbon or metal fine particles;</p> <p>(2) gold, silver, copper, aluminum or nickel alone, or an alloy</p> <p>containing two or more of said metals; and</p> <p>(3) a low melting point alloy having tin or lead as a principal component.”)</p> <p>Furuya, [0044] (“Note that the low melting point alloys mentioned above include those employing metals such as mercury, gallium, or indium, but a solder alloy having tin or lead as a main component is preferable from the viewpoint of manufacturing costs and the like. Eutectic solder or high-melting point solder with an increased lead ratio can suitably be used as the solder alloy, and if necessary bismuth, cadmium, antimony, zinc, manganese, indium, tin, silver and the like may be added. Note that, in order to improve the adhesion between the support 15 and the electroconductive material 16, as shown in FIG. 2 and FIG. 3, a bonding layer 17 may be formed on the surface of the support 15, prior to providing the conductive material 16 thereon.”)</p>

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	<p>Furuya, [0052]-[0053] (“Next, a photosensitive polyimide (trade name "Pimel", made by Asahi Kasei Corp.) was applied to the semiconductor element 2, whereafter a known photoetching method was used to perform pattern exposure, development and the like, and a first insulating layer 5 having a film thickness of approximately 10 μm was formed, which exposed the electrodes 3. Next, a 2000 Å thick TiN layer and a 5000 Å thick Cu layer were sequentially laminated on the first insulating layer 5 by sputtering. Next, a patterning process was performed on the TiN layer and the Cu layer, using a known photoetching method, to produce a wiring pattern 7, which is electrically connected to the electrode 3 (FIG. 4 (b)). Note that the TiN layer between the first insulating layer 5 and the wiring pattern 7 is formed as a barrier metal layer 6.</p> <p>Next, as shown in FIG. 4(c), a metal post 9 was formed on the wiring pattern 7, ... Note that a mask plating method is used for forming the metal post 9, and the steps for the mask plating method are described below.</p> <p>Specifically, after producing FIG. 4 (b), a photosensitive resist layer having a film thickness of 20 μm was formed on the first insulating layer 5 and the wiring pattern 7, whereafter, using a known photoetching method, a plating mask 13 was formed, in which the wiring pattern 7 was exposed at the location where the metal posts were to be formed (FIG. 5 (a)). Next, metal posts 9 made of copper (height 15 μm) were formed on the wiring pattern 7, which was exposed by the plating mask 13, using an electrolytic plating method (FIG. 5 (d)[sic]). Next, the plating mask 13 was peeled off producing that in FIG. 4 (c).”)</p> <p>Furuya, [0055] (“Next, the external connection terminal 14 was provided on the metal post 9 to produce the semiconductor device 1 (FIG. 4(f)). As shown in FIG. 2,</p>

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	<p>the external connection terminal 14 used in the present embodiment is one in which eutectic solder is formed as the electroconductive material 16 on the surface of the hollow support 15, which is made of thermoplastic polyimide and is produced by the steps described below. First, a hollow thermoplastic polyimide tube having an inner diameter of 0.15 mm and a thickness of 50 μm was purchased in a long format. Next, metallic chromium and copper were sequentially laminated so as to form films on the tube surface (outside surface). Metallic chromium and copper serve as a bonding layer 17 when laminating the electroconductive material, and the films were formed by spluttering so as to produce a metallic chromium film thickness of 0.2 μm, and a copper film thickness of 0.4 μm. After forming the bonding layer 17, a plating was formed with eutectic solder having a film thickness of approximately 20 μm, as the electroconductive material 16. Next, after forming the eutectic solder, the long thermoplastic polyimide tube was cut to individual lengths of approximately 0.3 mm to produce the external connection terminals 14 shown in FIG. 2 and FIG. 3.”)</p> <p>Takizawa, [0003]-[0004] (“[0003] As illustrated in FIG. 7(a), a conventional semiconductor device, includes: a wiring part 2 containing copper connected to a semiconductor chip 1, a solder ball 101 containing tin bonded to a land 7 formed on a surface of the wiring part 2, and a film substrate 3 that contacts the wiring part 2 on an opposite side surface as the bonding surface between the wiring part 2 and the solder ball 101, wherein a hole 4 is provided that passes through the film substrate 3 from the wiring part 2 to the surface on the opposite side as the bonding surface to the wiring part 2 of the film substrate 3, a metal 5 is filled into the hole 4, and a gold layer 6 is formed on the metal 5 surface of the opening part of the hole 4. Furthermore, the land 7 is a</p>

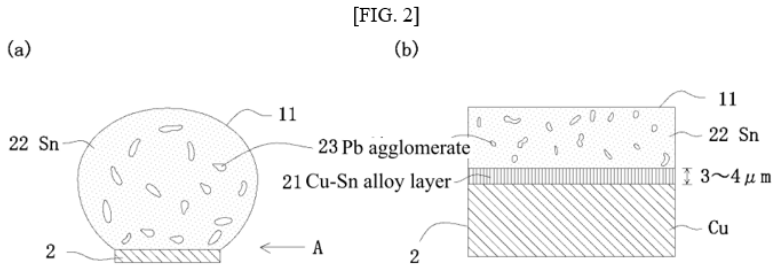
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	<p>hole provided on the wiring part 2 by shaving a predetermined location of the resist 32 in order to dispose a solder ball 101, and a Au layer 8 is formed on the surface of the land 7. Note that the Au layer 8 is illustrated in FIG. 7, but this Au layer 8 is thought to diffuse into the solder ball 101 by heat treatment of temperature cycle testing or the like performed after manufacturing this device, and it is hypothesized that the Au layer is not disposed on the wiring part 8 [Translator's note: presumably wiring part 2] after heat treatment. FIG. 8 illustrates an expanded view of the on the part between the wiring part 2 and the solder ball 101 illustrated in FIG. 7(a). Note that FIG. 8 illustrates an example (schematic diagram) of a conventional semiconductor device where the solder ball 101 is formed from a Sn-Pb eutectic solder (Sn content: 63%, Pb content: 37%). With the conventional semiconductor device illustrated in FIG. 7(a), the solder ball 101 and the printed board 34 are bonded as illustrated in FIG. 7(c).</p> <p>[0004]</p> <p>Furthermore, the conventional semiconductor device illustrated in FIG. 7 is manufactured by the steps illustrated in FIG. 9 and FIG. 10. First, the first manufacturing step of forming a land 7 after attaching the wiring part 2 to the film substrate 3 is described while referring to FIG. 9. FIG. 9(a) through FIG. 9(h) are all cross-sectional diagrams of a portion where the solder ball 101 is disposed in a subsequent step on the film substrate 3. As illustrated in FIG. 9(a), a wiring part 2 containing Cu is disposed on a main surface of the film substrate 3. Furthermore, an adhesive 31 is applied to the surface on the opposite side as the surface where the wiring part 2 of the film substrate 3 is disposed. The film substrate 3 is made of a material that can withstand temperature conditions of 250°C or higher such as polyimide or the like, and the adhesive 31 is made of a</p>

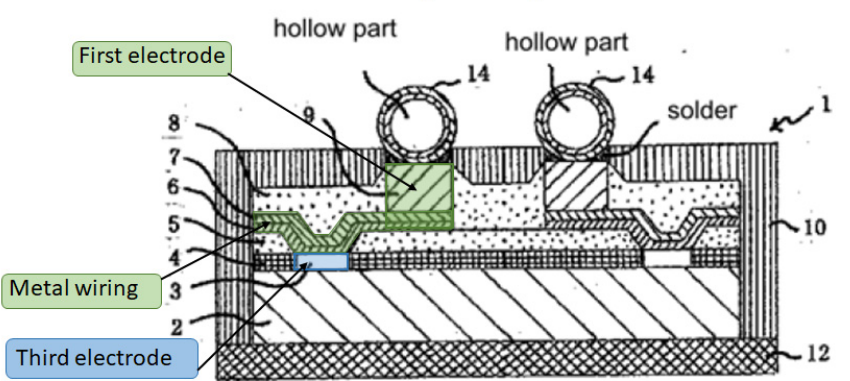
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	<p>polyimide system. Next, a wiring part 2 is patterned to a predetermined shape on the film substrate 3 illustrated in FIG. 9 (a) (refer to FIG. 9 (b)), and then a resist 32 is applied to the externally exposed surface of the wiring part 2 and the film substrate 3 (refer to FIG. 9(c)). Next, a hole 4 is formed passing through the film substrate 3 from the adhesive 31 to the wiring part 2 (refer to FIG. 9(d)). Formation of this hole 4 is formed using a tool such as laser or the like. Furthermore, a metal 5 such as Cu or Al or the like is filled into the hole 4 (refer to FIG. 9(e)), and then an Au layer 6 is formed on the surface of the metal 5 supposed at the opening part of the hole 4 (FIG. 9(f)). Furthermore, a land 7 for placing a solder ball in a subsequent step is disposed by providing a hole on the surface of the wiring part 2 (refer to FIG. 9(g)). Next, a thin film made of an Au layer 8 is formed on the surface of the land 7 (refer to FIG. 9(h)). The aforementioned steps provide a tape substrate 93 with a film substrate 3 on which the wiring part 2 is formed on a main surface. Note that FIG. 9 illustrates an expanded view of one land 7 portion provided on the film substrate 3, where the film substrate 3 has a tape-like shape, and a plurality of lands 7 for providing the solder ball 101 in a subsequent step are formed on the film substrate 3.”)</p> <p>Takizawa, [0009] (“[0009] MEANS FOR SOLVING THE PROBLEMS The first invention of the present application provided to resolve the aforementioned problem is a semiconductor device, comprising: a wiring part 2 containing copper connected to a semiconductor chip, and a solder ball 11 containing tin bonded to the wiring part 2; wherein a Cu-Sn alloy layer 21 with a thickness of approximately 1.87 μm or more is formed on the bonding part of the solder ball 11 and the wiring part 2.”)</p>

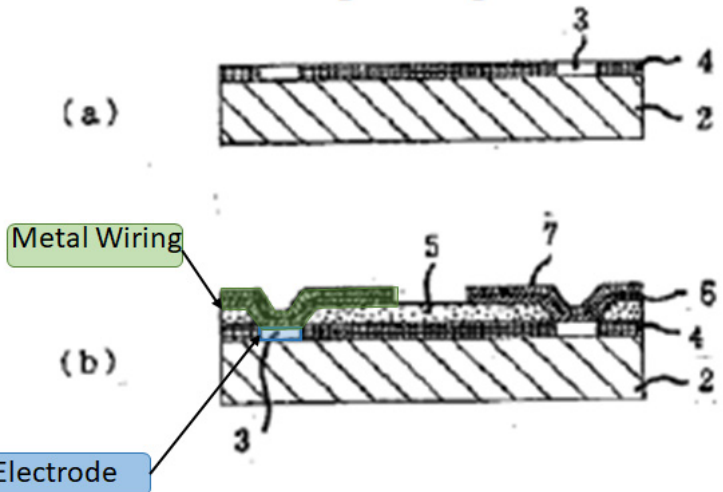
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	<p>Takizawa, [0019]-[0020] (“[0019] Furthermore, the sixth invention of the present application is a method of manufacturing a semiconductor device, including disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn on a land provided on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time. [0020] Herein, the predetermined time refers to the time sufficient for increasing the strain of the bonding part between the solder ball and the wiring part. The method of manufacturing the semiconductor device the sixth invention of the present application with the aforementioned configuration can cause the Sn in the solder ball to liquid phase diffuse to the Cu in the wiring part and form a Cu-SN alloy layer with sufficient thickness to prevent detachment of the solder ball neared the bonding part, and therefore can increase the strength of the bonding parts, and can reduce the occurrence rate of fractures and cracks near the bonding part by disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time. Thereby the occurrence of defects due to the occurrence of raking and cracking can be reduced so the productivity of the semiconductor device can be enhanced.”)</p>

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	<p>Takizawa, [0033]-[0035] (“[0033] DESCRIPTION OF THE PREFERRED EMBODIMENTS</p> <p>The semiconductor device according to the embodiment of the present invention is described below while referring to the drawings, but the following embodiments are only an example of the semiconductor device of the present invention. FIG. 1 is a cross-sectional view showing the semiconductor device according to one embodiment of the present invention. In regards to the semiconductor device shown in FIG. 1, FIG. 2 is an enlarged cross-sectional view of a solder ball part 11 when using a solder ball made from an eutectic solder (SN content ratio: 63%, PB content ratio: 37%) as the solder ball 11. FIG. 3 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 4 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 5 is a figure showing measurement results of the shear strength for a bonding part between a wiring part 7 and the solder ball 11 after bonding a printed board and the solder ball according to a process illustrated in FIG. 4(i) after maintaining the device provided by the process illustrated in FIG. 3 and FIG. 4 (a) to (g) in an N2 environment for a predetermined time at a temperature above the melting point of the solder ball according to a process illustrated in FIG. 4 (h) using the solder ball made from the Sn-Cu eutectic solder as the solder ball 11. FIG. 6 is a figure showing one example of the measurement method of the shear strength shown in FIG. 5.</p> <p>[0034]</p> <p>As illustrated in FIG. 1(a), the semiconductor device according to the present embodiment has the wiring part 2 containing Cu that is connected to a semiconductor chip 1 and the solder ball 11 containing Sn that is connected to</p>

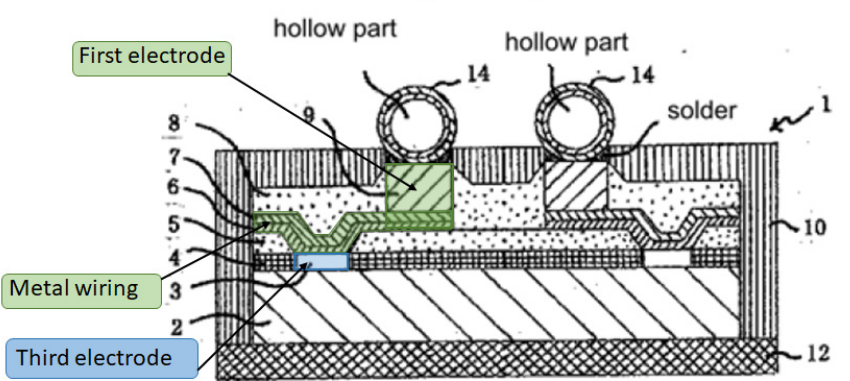
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	<p>the wiring part 2. In other words, the semiconductor device according to the present embodiment has the wiring part 4 containing Cu that is connected to the semiconductor chip 1, the solder ball 11 containing Sn connected to a main surface of the wiring part 4, and a film substrate 3 that is connected to the wiring part 2 that is the opposite side surface of the bonding surface between the wiring part 2 and the solder ball 11, is provided with a hole 4 that passes through the film substrate 3 from the wiring part 2 to the opposite side surface of the bonding part between the film substrate 3 and the wiring part 2, a metal 5 is filled in the hole 4, and an Au layer 6 is formed on a surface of the metal 5 of an opening part of the hole 4. Note, the hole 4 is placed directly above an electrode part 12 that is placed on the semiconductor chip 1 on the semiconductor device according to the present embodiment, and the solder ball 11 and the electrode part 12 are connected by the metal 5 filled in the hole 4, but the solder ball 11 does not have to be placed directly above the electrode part 12. Furthermore, as illustrated in FIG. 1(c), the solder ball 11 and the printed board 34 are connected in the semiconductor device according to the present embodiment illustrated in FIG. 1(a).</p> <p>[0035]</p> <p>Furthermore, SN is a main component in the solder ball, and the solder ball is formed, for example, using Pb free solder or the like containing Ag, Cu, An, Bi, Ni, Cd, S, As, Zn, and the like with Sn-Pb alloy, Sn-Ag alloy, or Sn as a main constituent. Furthermore, in regards to FIG. 1(a), a figure in which the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 vicinity is illustrated enlarged in FIG. 1(b). As illustrated in FIG. 1(b), a strong Cu-Sn alloy layer is formed on the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 portion</p>

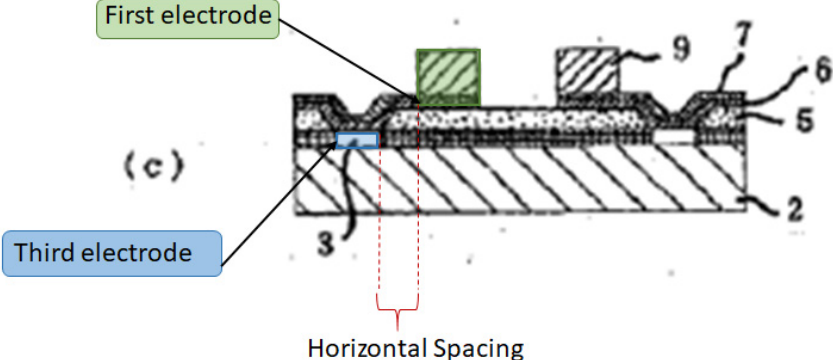
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		<p>on which the solder ball 11 is placed on the wiring part 2. As described above, detachment of the solder ball 11 caused by fractures and cracks can be reduced by reducing the occurrence of fractures and cracks near the bonding part by providing the Cu-Sn alloy layer on the bonding part between the solder ball 11 and the wiring part 2. As a result, productivity of the semiconductor device can be improved, and yield can be further increased. The Cu-Sn alloy layer preferably has a thickness of 1.87 μm or more, more preferably a thickness of 2 μm or more, and even more preferably a thickness of 3 μm or more, in order to reduce the occurrence of fractures and cracks in the vicinity of the bonding part.”)</p> <p>Takizawa, Figures 2a-2b</p>  <p>[FIG. 2]</p> <p>(a) (b)</p> <p>22 Sn 11 23 Pb agglomerate 21 Cu-Sn alloy layer 2 A</p> <p>11 22 Sn 3~4 μm Cu 2</p>
	Claim 3	
3	The semiconductor device of claim 1, further comprising a third electrode portion formed on a	Furuya, Figure 1 (reproduced and annotated below) of Furuya depicts “a third electrode portion formed on a surface of the semiconductor element” (designated numeral 3 “electrode,” shaded blue) and further depicts “a metal wiring formed on the semiconductor element . . . electrically connecting the first electrode portion to the third electrode portion,” (the wiring is designated with numerals 6 “metal barrier layer” and 7 “wiring pattern,” collectively shaded green).

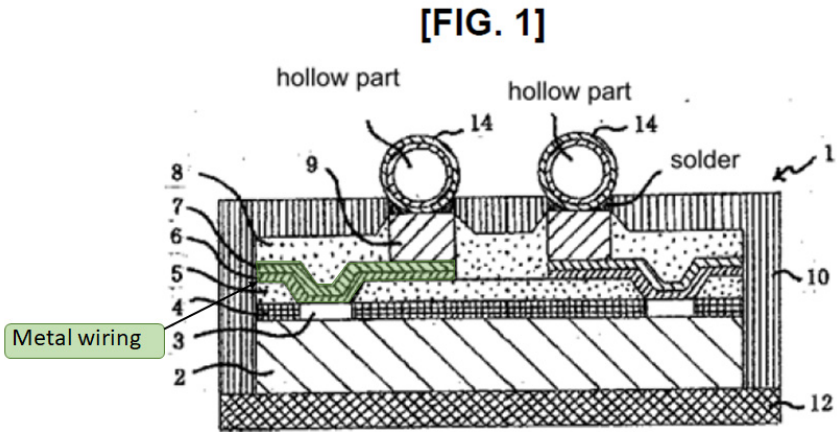
U.S. Patent No. 6,954,001	Furuya in view of Takizawa
<p>surface of the semiconductor element and a metal wiring formed on the semiconductor element, said metal wiring electrically connecting the first electrode portion to the third electrode portion.</p>	<p style="text-align: center;">[FIG. 1]</p>  <p>Furuya, [0016] (“[Means for Solving the Problems] In order to achieve the aforementioned object, the present inventors undertook earnest study and arrived at the present invention. That is to say, in claim 1, the semiconductor device is characterized in that a first insulating layer having substantially the same shape as a passivation film is formed on the passivation film, which has been formed on a semiconductor element, with <i>an electrode, which has been formed on the semiconductor element, exposed; a wiring pattern, which is connected with the electrode of the semiconductor element</i>, is formed on the first insulating layer; a metal post for external connection is formed on the wiring pattern; a second insulating layer, which is in close contact with the wiring pattern, is formed in a manner so as to cover a side face of the metal post excluding a tip surface of the metal post; resin sealing is performed with sealing resin in a manner so as to expose the tip surface of the metal post; and an external connection terminal is provided at the tip surface of the metal post.”)</p> <p>Furuya, [0027] (“Hereafter, modes of embodiment of the present invention are described based on the drawings. In the semiconductor device 1 (CSP) of the present</p>

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		<p>invention, as shown in FIG. 1, a first insulating layer 5, which has substantially the same shape as a passivation film 4, is formed on the passivation film 4, <i>in a manner so as to expose electrodes 3, which have been formed on a semiconductor element 2. Then, a wiring pattern 7 (wiring layer) that is connected with the electrodes 3 is formed on the first insulating layer 5, and metal posts 9 for external connection, having a height of approximately 3 μm to 50 μm, are formed at predetermined positions on the wiring pattern 7. ...</i>")</p> <p>Furuya, Figures 4(a)-(b) (reproduced and annotated below) of Furuya depicts "a third electrode portion formed on a surface of the semiconductor element" (designated numeral 3 "electrode," shaded blue) and further depicts "a metal wiring formed on the semiconductor element . . . electrically connecting the first electrode portion to the second electrode portion," (the wiring is designated with numerals 6 "metal barrier layer" and 7 "wiring pattern," collectively shaded green).</p> <p style="text-align: center;">[FIG. 4]</p>  <p>(a)</p> <p>(b)</p> <p>Metal Wiring</p> <p>Third Electrode</p>

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		<p>Furuya, [0051] (“FIG. 4 (a) is a semiconductor element 2 produced by conventionally known means, which is incorporated in a semiconductor device 1 of the present invention. <i>Electrodes 3 made of aluminum are formed on the semiconductor element 2</i> with a silicon wafer as a substrate, and a passivation film 4 is formed on the semiconductor element 2 in a manner so as to expose the electrodes 3.”)</p> <p>Furuya, [0052] (“Next, a photosensitive polyimide (trade name "Pimel", made by Asahi Kasei Corp.) was applied to the semiconductor element 2, whereafter a known photoetching method was used to perform pattern exposure, development and the like, and a first insulating layer 5 having a film thickness of approximately 10 μm was formed, which exposed the electrodes 3. Next, a 2000 Å thick TiN layer and a 5000 Å thick Cu layer were sequentially laminated on the first insulating layer 5 by sputtering. Next, a patterning process was performed on the TiN layer and the Cu layer, using a known photoetching method, <i>to produce a wiring pattern 7, which is electrically connected to the electrode 3</i> (FIG. 4 (b)). Note that the TiN layer between the first insulating layer 5 and the wiring pattern 7 is formed as a barrier metal layer 6.”)</p>
	Claim 4	
4	The semiconductor device of claim 3, wherein the first and third electrode portion are horizontally	<p>Furuya, Figure 1 (reproduced and annotated below) of Furuya depicts “the first and third electrode portions are horizontally spaced apart with respect to the semiconductor element” (the first electrode portion is shaded green and the third electrode portion is shaded blue).</p>

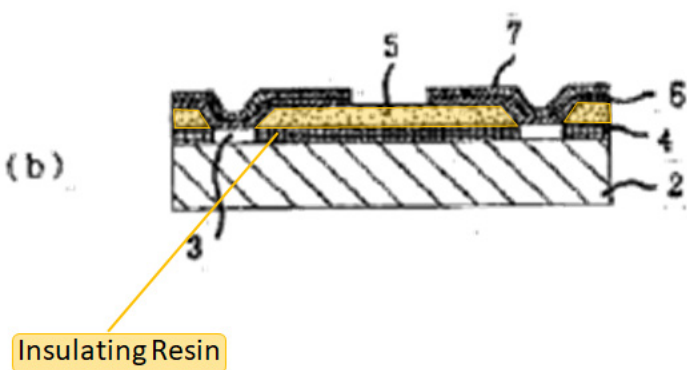
U.S. Patent No. 6,954,001	Furuya in view of Takizawa
<p>spaced apart with respect to the semiconductor element.</p>	<p style="text-align: center;">[FIG. 1]</p>  <p>Furuya, [0027] (“Hereafter, modes of embodiment of the present invention are described based on the drawings. In the semiconductor device 1 (CSP) of the present invention, as shown in FIG. 1, a first insulating layer 5, which has substantially the same shape as a passivation film 4, is formed on the passivation film 4, in a manner so as to expose electrodes 3, which have been formed on a semiconductor element 2. <i>Then, a wiring pattern 7 (wiring layer) that is connected with the electrodes 3 is formed on the first insulating layer 5, and metal posts 9 for external connection, having a height of approximately 3 μm to 50 μm, are formed at predetermined positions on the wiring pattern 7.</i> Next, a second insulating layer 8 is formed, which is in close contact with the wiring pattern 7 and the first insulating layer 5, and which covers the side face of the metal post 9 excluding the tip surface of the metal post 9. Next, the semiconductor element is resinsealed with sealing resin 10 in a manner so as to expose the tip surface of the metal post 9, and an external connection terminal 14 is provided on the metal post 9.”)</p> <p>Figure 4(c) (reproduced and annotated below) of Furuya depicts “the first and second electrode portions are horizontally spaced apart with respect to the</p>

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	<p>semiconductor element” (the first electrode portion is shaded green and the third electrode portion is shaded blue).</p> <p style="text-align: center;">[FIG. 4]</p>  <p>Furuya, [0053] (“Next, as shown in FIG. 4(c), a metal post 9 was formed on the wiring pattern 7, whereafter photosensitive polyimide (trade name "Pimel", made by Asahi Kasei Corp.) was applied on the first insulating layer 5 by spin coating, whereafter the excess polyimide was removed by photoetching, excluding the top face [sic] and side face portions of the metal post 9, to produce a second insulating layer 8 (FIG. 4(d)). ... Specifically, after producing FIG. 4 (b), a photosensitive resist layer having a film thickness of 20 μm was formed on the first insulating layer 5 and the wiring pattern 7, whereafter, using a known photoetching method, a plating mask 13 was formed, <i>in which the wiring pattern 7 was exposed at the location where the metal posts were to be formed (FIG. 5 (a)).</i> Next, metal posts 9 made of copper (height 15 μm) were formed on the wiring pattern 7, which was exposed by the plating mask 13, using an electrolytic plating method (FIG. 5 (d) [sic]). Next, the plating mask 13 was peeled off producing that in FIG. 4 (c).”)</p>
Claim 6	

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6	The semiconductor device of claim 3, wherein the metal wiring includes copper.	<p>Furuya, Figure 1 (reproduced and annotated below) of Furuya depicts “the metal wiring” depicted as numerals 6 and 7.</p> <p style="text-align: center;">[FIG. 1]</p>  <p>Furuya, [0035] (“<i>Next, the material for the wiring pattern 7 is desirably a material with good conductivity and, for example, copper, silver, aluminum, alloys thereof, other metals that are good conductors or the like can be used. If copper, silver, or the like is used as the material for the wiring pattern 7, prior to the formation of the wiring pattern 7, it is preferable to form a metal barrier layer 6 made of a TiW alloy, TiN, TaN, W, Cr or the like as an undercoat layer, and then form the wiring pattern 7 on the metal barrier layer 6.</i>”)</p> <p>Furuya, [0052] (“Next, a photosensitive polyimide (trade name "Pimel", made by Asahi Kasei Corp.) was applied to the semiconductor element 2, whereafter a known photoetching method was used to perform pattern exposure, development and the like, and a first insulating layer 5 having a film thickness of approximately 10 μm was formed, which exposed the electrodes 3. Next, a 2000 Å thick TiN layer and <i>a 5000 Å thick Cu layer</i> were sequentially laminated on the first insulating layer 5 by sputtering. Next, a patterning process was performed on</p>

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		the TiN layer and the Cu layer, using a known photoetching method, to produce a wiring pattern 7, which is electrically connected to the electrode 3 (FIG. 4 (b)). Note that the TiN layer between the first insulating layer 5 and the wiring pattern 7 is formed as a barrier metal layer 6.”)
	Claim 7	
7A	The semiconductor device of claim 3, further comprising an insulating resin layer formed between the surface of the semiconductor element and the metal wiring,	<p>Furuya, Figure 1 (reproduced and annotated below) of Furuya depicts “an insulating resin layer formed between the surface of the semiconductor element and the metal wiring” (depicted as numerals 5 “first insulating layer” and shaded yellow).</p> <p style="text-align: center;">[FIG. 1]</p> <p>Furuya, [0004] (“As shown in FIG. 6, a passivation film 64 is formed on a semiconductor element 62, on which electrodes 63 (connection pads) made of aluminum or the like have been formed, in a manner so as to expose the electrodes 63. <i>Next, a first insulating layer 65 made of an insulating resin or the like is formed on the passivation film 64 in a manner so as to expose the electrodes 63. Furthermore, a wiring pattern 67 (wiring layer), which is connected to the electrodes 63, is formed on the first insulating layer 65, and metal posts 69 made</i></p>

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	<p>of copper or the like are provided on the wiring pattern 67. Note that, in the example in FIG. 6, a metal barrier layer 66 is formed below the wiring pattern 67. Next, a second insulating layer 68 is formed above the wiring pattern 67 and the first insulating layer 65, in a manner so as to expose the metal posts 69. Furthermore, resin sealing is performed with a sealing resin 70 in a manner so as to expose the metal posts 69.”)</p> <p>Furuya, [0027] (“Hereafter, modes of embodiment of the present invention are described based on the drawings. In the semiconductor device 1 (CSP) of the present invention, as shown in FIG. 1, a first insulating layer 5, which has substantially the same shape as a passivation film 4, is formed on the passivation film 4, in a manner so as to expose electrodes 3, which have been formed on a semiconductor element 2.”)</p> <p>Furuya, [0033] (“Here, there is no particular limitation on the material used for the first insulating layer 5, so long as it has good heat resistance and adhesion, and has no influence on the semiconductor element 2, but as this touches the semiconductor element 2, it is preferable that this be of a high purity. Furthermore, a material with a low dielectric constant is preferable, and polyimide can be said to be preferable from the viewpoint of obtaining high purity, while from the point of view of manufacturing, a photosensitive polyimide material or a photosensitive polyimide siloxane composition or the like is suitable. Furthermore, a lower coefficient of thermal expansion is better, and those having a coefficient of thermal expansion of approximately 60 ppm (60×10^{-6} in/in/°C) or less are desirable in practical terms.”)</p> <p>Furuya, Figure 4(b) (reproduced and annotated below) of Furuya depicts “an insulating resin layer formed between</p>

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		<p>the surface of the semiconductor element and the metal wiring” (depicted as numerals 5 and shaded yellow).</p> <p style="text-align: center;">[FIG. 4]</p>  <p>Furuya, [0046] (“Next, in the claim 8 set forth above, a method for manufacturing the semiconductor device 1 of the present invention is proposed. That is to say, this is a method of manufacturing a semiconductor device in which electrodes 3, which provide electrical connections with the outside, and are produced by way of a conventionally known manufacturing method, are formed as shown in FIG. 4 (a), and <i>which has at least: a step of forming a first insulating layer 5, which has substantially the same shape as a passivation film 4, on a semiconductor element 2, on the surface of which the passivation film 4 has been formed, in a manner so as to expose the electrodes 3, and then forming a wiring pattern 7 having a predetermined shape, which is connected with the electrodes 3, on the first insulating layer 5, so as to produce state in FIG. 4 (b); ...</i>”)</p> <p>Furuya, [0063] Furthermore, the second insulating layer 8 is formed in a manner so as to cover the wiring pattern 7 and to form a region lower than the tip surfaces of the metal posts 9, excluding the side faces of the metal posts</p>

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		<p>9. Thereby, when curing so as to form the second insulating layer 8 (for example, when heating is performed at 400°C for 1 hour in a high temperature oven), even if residual gas is generated <i>in the resin that constitutes the first insulating layer 5</i>, the residual gas will escape by way of the location in the second insulating layer 8 where the film thickness is low (region on the wiring pattern 7). Therefore, it is possible to prevent wire breakage in the wiring pattern 7 due to the resin part swelling because of bubbles caused by the residual gas.”)</p>
7B	wherein the metal wiring is formed along a surface of the insulating resin layer.	<p>Furuya, Figure 1 (reproduced and annotated below) of Furuya depicts “the metal wiring is formed along a surface of the insulating resin layer”.</p> <div data-bbox="521 1087 1369 1459" data-label="Image"> <p style="text-align: center;">[FIG. 1]</p> </div> <p>Furuya, [0046] (“Next, in the claim 8 set forth above, a method for manufacturing the semiconductor device 1 of the present invention is proposed. That is to say, this is a method of manufacturing a semiconductor device in which electrodes 3, which provide electrical connections with the outside, and are produced by way of a conventionally known manufacturing method, are formed as shown in FIG. 4 (a), and which has at least: a step of</p>

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		forming a first insulating layer 5, which has substantially the same shape as a passivation film 4, on a semiconductor element 2, on the surface of which the passivation film 4 has been formed, in a manner so as to expose the electrodes 3, and then <i>forming a wiring pattern 7 having a predetermined shape, which is connected with the electrodes 3, on the first insulating layer 5</i> , so as to produce state in FIG. 4 (b); a step of forming a metal post 9 for external connection, in a predetermined position of the wiring pattern 7, at a predetermined height (approximately 3 μm to 50 μm), so as to produce FIG. 4 (c); a step of applying an insulating resin on the first insulating layer 5 including the metal post 9, and then removing the insulating resin from the tip region of the metal post 9 for connecting to the outside, so as to make the second insulating layer 8 and produce the state in FIG. 4 (d); a step of resin sealing with the sealing resin 10 so as to produce FIG. 4 (e); and a step of placing the external connection terminal 14 so as to produce FIG. 4 (f). Note that, in the example in FIG. 4, prior to forming the wiring pattern 7, the metal barrier layer 6 is formed as an undercoat layer.”)
	Claim 8	
8	The semiconductor device of claim 3, wherein the metal wiring has a thickness in the range of 0.01 μm to 8 μm .	Furuya, Figure 4(b) (reproduced and annotated below) of Furuya depicts “the metal wiring” depicted as numerals 6 “metal barrier layer” and 7 “wiring pattern.”

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		<p>[FIG. 1]</p> <p>Furuya, [0052] ("Next, a photosensitive polyimide (trade name "Pimel", made by Asahi Kasei Corp.) was applied to the semiconductor element 2, whereafter a known photoetching method was used to perform pattern exposure, development and the like, and a first insulating layer 5 having a film thickness of approximately 10 μm was formed, which exposed the electrodes 3. Next, a 2000 Å thick TiN layer and a 5000 Å thick Cu layer were sequentially laminated on the first insulating layer 5 by sputtering. Next, a patterning process was performed on the TiN layer and the Cu layer, using a known photoetching method, to produce a wiring pattern 7, which is electrically connected to the electrode 3 (FIG. 4 (b)). Note that the TiN layer between the first insulating layer 5 and the wiring pattern 7 is formed as a barrier metal layer 6.")</p>
10P	A semiconductor device comprising:	See Claim Element 1P.
10A	a semiconductor element;	See Claim Element 1A.

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10B	a first electrode portion formed on the semiconductor element, said first electrode portion comprising a first metal component;	See Claim Element 1B.
10C	a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal	See Claim Element 1C.

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	component; and	
10D	a diffusion layer formed between said first electrode portion and said second electrode portion,	<i>See Claim Element 1D.</i>
10E	wherein said diffusion layer comprises said first metal component and said second metal component, and	<i>See Claim Element 1E</i>
10E	said first electrode portion and said diffusion layer have a combined thickness in the range of 10 μm to 20 μm .	<p>Furuya in view of Takizawa discloses said first electrode portion and said diffusion layer have a combined thickness in the range of 10 μm to 20 μm.</p> <p><i>See, e.g., disclosures for claim elements 1[b] and 1[d].</i></p> <p>Takizawa, [0003] (“As illustrated in FIG. 7(a), a conventional semiconductor device, includes: a wiring part 2 containing copper connected to a semiconductor chip 1, a solder ball 101 containing tin bonded to a land 7 formed on a surface of the wiring part 2, and a film</p>

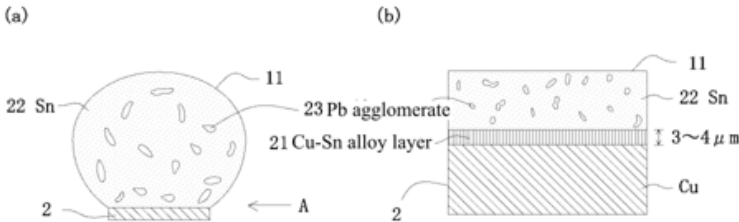
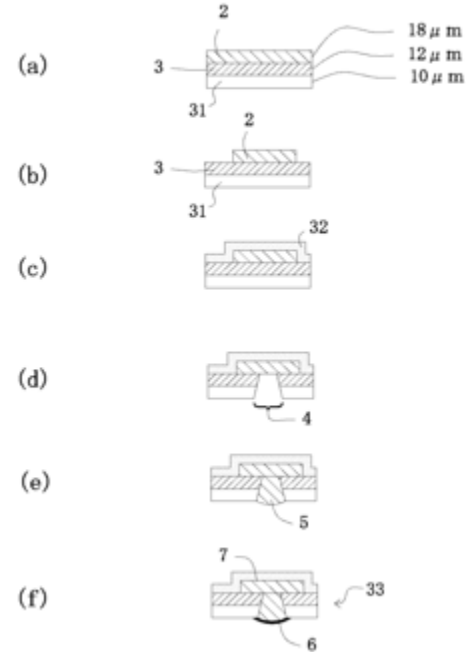
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	<p>substrate 3 that contacts the wiring part 2 on an opposite side surface as the bonding surface between the wiring part 2 and the solder ball 101, wherein a hole 4 is provided that passes through the film substrate 3 from the wiring part 2 to the surface on the opposite side as the bonding surface to the wiring part 2 of the film substrate 3, a metal 5 is filled into the hole 4, and a gold layer 6 is formed on the metal 5 surface of the opening part of the hole 4. Furthermore, the land 7 is a hole provided on the wiring part 2 by shaving a predetermined location of the resist 32 in order to dispose a solder ball 101, and a Au layer 8 is formed on the surface of the land 7. Note that the Au layer 8 is illustrated in FIG. 7, but this Au layer 8 is thought to diffuse into the solder ball 101 by heat treatment of temperature cycle testing or the like performed after manufacturing this device, and it is hypothesized that the Au layer is not disposed on the wiring part 8 [Translator's note: presumably wiring part 2] after heat treatment. FIG. 8 illustrates an expanded view of the on the part between the wiring part 2 and the solder ball 101 illustrated in FIG. 7(a). Note that FIG. 8 illustrates an example (schematic diagram) of a conventional semiconductor device where the solder ball 101 is formed from a Sn-Pb eutectic solder (Sn content: 63%, Pb content: 37%). With the conventional semiconductor device illustrated in FIG. 7(a), the solder ball 101 and the printed board 34 are bonded as illustrated in FIG. 7(c).")</p> <p>Takizawa, [0004] ("Furthermore, the conventional semiconductor device illustrated in FIG. 7 is manufactured by the steps illustrated in FIG. 9 and FIG. 10. First, the first manufacturing step of forming a land 7 after attaching the wiring part 2 to the film substrate 3 is described while referring to FIG. 9. FIG. 9(a) through FIG. 9(h) are all cross-sectional diagrams of a portion</p>

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	<p>where the solder ball 101 is disposed in a subsequent step on the film substrate 3. As illustrated in FIG. 9(a), a wiring part 2 containing Cu is disposed on a main surface of the film substrate 3. Furthermore, an adhesive 31 is applied to the surface on the opposite side as the surface where the wiring part 2 of the film substrate 3 is disposed. The film substrate 3 is made of a material that can withstand temperature conditions of 250°C or higher such as polyimide or the like, and the adhesive 31 is made of a polyimide system. Next, a wiring part 2 is patterned to a predetermined shape on the film substrate 3 illustrated in FIG. 9 (a) (refer to FIG. 9 (b)), and then a resist 32 is applied to the externally exposed surface of the wiring part 2 and the film substrate 3 (refer to FIG. 9(c)). Next, a hole 4 is formed passing through the film substrate 3 from the adhesive 31 to the wiring part 2 (refer to FIG. 9(d)). Formation of this hole 4 is formed using a tool such as laser or the like. Furthermore, a metal 5 such as Cu or Al or the like is filled into the hole 4 (refer to FIG. 9(e)), and then an Au layer 6 is formed on the surface of the metal 5 supposed at the opening part of the hole 4 (FIG. 9(f)). Furthermore, a land 7 for placing a solder ball in a subsequent step is disposed by providing a hole on the surface of the wiring part 2 (refer to FIG. 9(g)). Next, a thin film made of an Au layer 8 is formed on the surface of the land 7 (refer to FIG. 9(h)). The aforementioned steps provide a tape substrate 93 with a film substrate 3 on which the wiring part 2 is formed on a main surface. Note that FIG. 9 illustrates an expanded view of one land 7 portion provided on the film substrate 3, where the film substrate 3 has a tape-like shape, and a plurality of lands 7 for providing the solder ball 101 in a subsequent step are formed on the film substrate 3.</p>

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		<p>Takizawa, [0009] (“MEANS FOR SOLVING THE PROBLEMS</p> <p>The first invention of the present application provided to resolve the aforementioned problem is a semiconductor device, comprising: a wiring part 2 containing copper connected to a semiconductor chip, and a solder ball 11 containing tin bonded to the wiring part 2; wherein a Cu-Sn alloy layer 21 with a thickness of approximately 1.87 μm or more is formed on the bonding part of the solder ball 11 and the wiring part 2.”)</p> <p>Takizawa, [0033] (“DESCRIPTION OF THE PREFERRED EMBODIMENTS</p> <p>The semiconductor device according to the embodiment of the present invention is described below while referring to the drawings, but the following embodiments are only an example of the semiconductor device of the present invention. FIG. 1 is a cross-sectional view showing the semiconductor device according to one embodiment of the present invention. In regards to the semiconductor device shown in FIG. 1, FIG. 2 is an enlarged cross-sectional view of a solder ball part 11 when using a solder ball made from an eutectic solder (SN content ratio: 63%, PB content ratio: 37%) as the solder ball 11. FIG. 3 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 4 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 5 is a figure showing measurement results of the shear strength for a bonding part between a wiring part 7 and the solder ball 11 after bonding a printed board and the solder ball according to a process illustrated in FIG. 4(i) after maintaining the device provided by the process illustrated in FIG. 3 and FIG. 4 (a) to (g) in an N₂ environment for a predetermined time at a temperature above the melting</p>

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	<p>point of the solder ball according to a process illustrated in FIG. 4 (h) using the solder ball made from the Sn-Cu eutectic solder as the solder ball 11.</p> <p>FIG. 6 is a figure showing one example of the measurement method of the shear strength shown in FIG. 5.”)</p> <p><i>See, e.g.,</i> Takizawa, [0035] (“Furthermore, SN is a main component in the solder ball, and the solder ball is formed, for example, using Pb free solder or the like containing Ag, Cu, An, Bi, Ni, Cd, S, As, Zn, and the like with Sn-Pb alloy, Sn-Ag alloy, or Sn as a main constituent. Furthermore, in regards to FIG. 1(a), a figure in which the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 vicinity is illustrated enlarged in FIG. 1(b). As illustrated in FIG. 1(b), a strong Cu-Sn alloy layer is formed on the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 portion on which the solder ball 11 is placed on the wiring part 2. As described above, detachment of the solder ball 11 caused by fractures and cracks can be reduced by reducing the occurrence of fractures and cracks near the bonding part by providing the Cu-Sn alloy layer on the bonding part between the solder ball 11 and the wiring part 2. As a result, productivity of the semiconductor device can be improved, and yield can be further increased. The Cu-Sn alloy layer preferably has a thickness of 1.87 μm or more, more preferably a thickness of 2 μm or more, and even more preferably a thickness of 3 μm or more, in order to reduce the occurrence of fractures and cracks in the vicinity of the bonding part.”)</p> <p>Takizawa, [0040] (“[Example 1] The semiconductor device of the present embodiment illustrated in FIG. 1 is an example using a solder ball</p>

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	<p>made from Sn-Pb eutectic solder (Sn content ratio: 63%, Pb content ratio: 37%) as the solder ball 11. FIG. 2 illustrates an enlarged view of the solder ball 11 portion according to the present example. As shown in FIG. 2, a Cu-Sn alloy layer was formed in the vicinity of the bonding part between the solder ball 11 and the wiring part 2. In regards to the solder ball 11 provided on the semiconductor device of the present invention illustrated in FIG. 2, 1.87 to 4.0 μm of the Cu-Sn alloy layer was formed on each solder ball 11, and in particular, many solder balls were formed with 3.0 to 4.0 μm of the Cu-Sn alloy layer. On the other hand, 1.00 to 1.50 μm of the Cu-Sn alloy layer was formed on the solder ball 101 placed on the conventional semiconductor device illustrated in FIG. 8. Thereby, it was revealed that the semiconductor device of the present invention illustrated in FIG. 2 was formed with a strong Cu-Sn alloy layer that was thicker. Forming the Cu-Sn alloy layer with a thickness of at least 1.87 μm or more was preferable in order to prevent detachment of the solder ball 11. Thereby, the occurrence ratio of fractures and cracks in the vicinity of the bonding part could be reduced since strength of the bonding part between the solder ball 11 and the wiring part 2 was strengthened by forming the Cu-Sn alloy layer with sufficient thickness in the vicinity of the bonding part. Thereby, a device with favorable yield could be provided since the occurrence of defective parts caused by the occurrence of fractures and cracks could be reduced.”)</p> <p><i>See, e.g., Figures 2-3</i></p>

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		<p>[FIG. 2]</p>  <p>[FIG. 3]</p>  <p><i>See also, e.g., Takizawa [0042]-[0043]; Claim 1</i></p>
	Claim 11	
	The semiconductor device of claim 10, wherein said first metal component	<i>See Claim 2.</i>

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	includes copper and said second metal component includes tin.	
	Claim 12	
	The semiconduc tor device of claim 10, further comprising a third electrode portion formed on a surface of the semiconduc tor element and a metal wiring formed on the semiconduc tor element, said metal wiring electrically connecting the first electrode portion to the third	<i>See Claim 3.</i>

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	electrode portion.				
	Claim 13				
	The semiconductor device of claim 12, wherein the first electrode portion and the third electrode portion are horizontally spaced apart with respect to the semiconductor element.		See Claim 4.		
	Claim 15				
	The semiconductor device of claim 12, wherein the metal wiring includes copper.		See Claim 6.		
	Claim 16				
16A	The semiconductor device of claim 12, further		See Claim Element 7A.		

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	comprising an insulating resin layer formed between the surface of the semiconductor element and the metal wiring,				
16B	wherein the metal wiring is formed along a surface of the insulating resin layer.		See Claim Element 7B.		
	Claim 17				
17	The semiconductor device of claim 12, wherein the metal wiring has a thickness in the range of 0.01 μm to 8 μm .		See Claim 8.		

C. Ground 2: Furuya In View Of Takizawa And Further In View Of Knowledge Of A POSA (as evidenced by Yaguchi) Renders Obvious Claims 5 and 14

1. Reasons To Combine Furuya And Takizawa With Yaguchi

149. A POSA would have been motivated to combine Furuya and Takizawa for the reasons above in relation to Ground 1. A POSA would have been motivated to further combine these references with Yaguchi for the reasons described below.

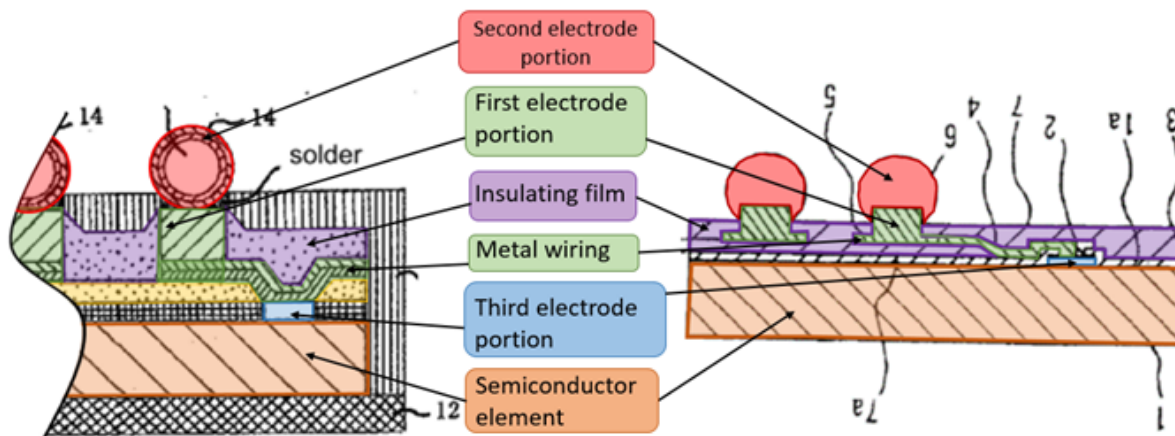
150. A POSA would have been motivated to improve the semiconductor device disclosed in Furuya by looking to the teachings of Yaguchi for improving the connection reliability for a semiconductor mounted on a printed wiring board (i.e. PCB). Both Furuya and Yaguchi are in the same field of technology and were filed around the same time. Furuya and Yaguchi are directed toward very similar devices, i.e. chip-size package (CSP) semiconductor devices, that are formed and operate in a similar manner.

151. For example, Furuya teaches a semiconductor device that has “a semiconductor element, with an electrode, which has been formed on the semiconductor element, exposed; a wiring pattern, which is connected with the electrode of the semiconductor element, is formed on the first insulating layer; a metal post for external connection is formed on the wiring pattern; [and] a second insulating layer, which is in close contact with the wiring pattern.” Ex-1006,

Abstract. Similarly, Yaguchi describes a “semiconductor device [that] ... comprises a semiconductor element, a passivation film formed so the surface of a pad on the semiconductor device surface is exposed, a conductive wiring line connected to the pad, a land connected to the conductive wiring line, a protective film, a protrusion provided on the land, and an external terminal.”¹¹ Ex-1011, 9:6-10. Thus, both references are directed to very similar semiconductor devices as shown in the annotated figure below. as shown in the annotated figure below.¹²

Furuya Figure 1

Yaguchi Figure 1(a)



¹¹ Numbers referencing Figures 1 and 2 omitted.

¹² A POSA would have recognized that Yaguchi and Furuya use different terminology to refer to elements that are the same. For ease of reference, the labels below are those used by the claims of the '001 Patent. The Figure in Yaguchi has also been inverted so that the elements are oriented as in Furuya.

152. Furthermore, Furuya is directed toward providing high reliability in semiconductor devices “in which the connection strength between the metal post and the wiring pattern is high and the reliability of the electrical connection with the outside is high...” Ex-1006, [0015]. Yaguchi is directed to a similar problem—the disconnection of semiconductor devices from a substrate due to temperature changes. Ex-1011, 2:7-3:8. Yaguchi “is effective in preventing disconnection of the external terminal of a semiconductor device, particularly, a semiconductor device of a chip size...” so “high reliability can therefore be provided.” Ex-1011, 24:5-8. Yaguchi teaches increasing the reliability by “having a protrusion formed on the land to which the external terminal is bonded,” which “protrudes through the protective film” and is bonded to the external terminal. *See, e.g., id.*, 4:18-20; 9:13-19.

153. Thus, both references are directed to very similar semiconductor devices, i.e. chip size package (CSP) semiconductor devices. Both references address means to form reliable electrical connections by forming structures that can withstand the stress or strain that is applied to the semiconductor device due to differences in thermal expansion coefficients between the silicon material of the semiconductor device and the material of which the printed circuit board is made. *See, e.g.,* Ex-1006, [0008] and Ex-1011, 2:7-3:26.

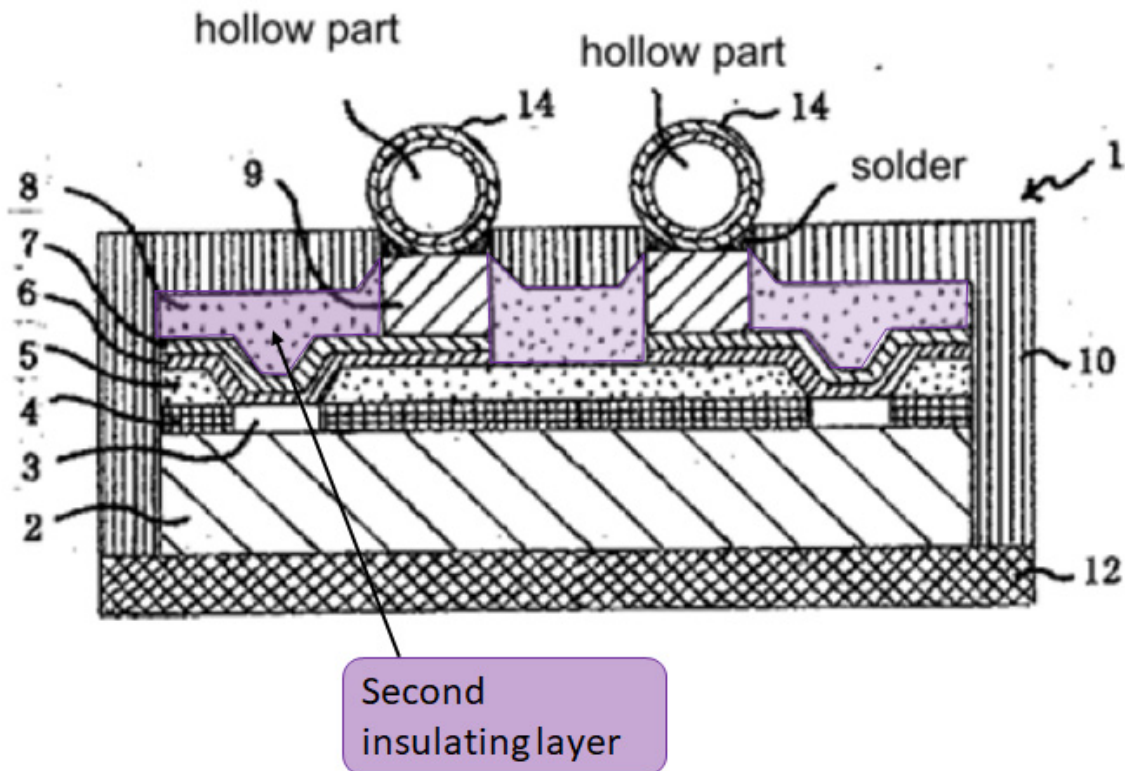
154. As a result, a POSA would have been motivated to add a protrusion, as described by Yaguchi, so that it extended above the insulating film in Furuya to ensure a better connection. Ex-1011, 4:18-29. Furthermore, a POSA would have been motivated either to forego utilizing a sealing resin as per Yaguchi's first embodiment. Ex-1011, 9:5-19. In case a sealing resin is used, a POSA would ensure that the protrusions, i.e., metal posts in Furuya's structure, protrude through the sealing resin as per Yaguchi's teaching. Ex-1011, 4:18-29; 9:5-19. Because such a combination would be nothing more than applying known techniques to similar systems, a POSA would have expected the combination to yield a predictable result and be successful.

2. Claim 5

- a) **[5 a]: The semiconductor device of claim 3, further comprising an insulating film formed on said metal wiring**

155. Furuya discloses a second insulating layer formed on top of the wiring pattern. For example, Furuya teaches that after forming the wiring pattern 7, “[n]ext, a second insulating layer 8 is formed, which is in close contact with the wiring pattern 7.” Ex-1006, [0027]. *See also* Ex-1006, [0016]. Furuya elaborates that “the second insulating layer 8 is **formed in a manner so as to cover the wiring pattern 7.**” Ex-1006, [0063]. This second insulating layer is shown in Figure 1, annotated below.

[FIG. 1]



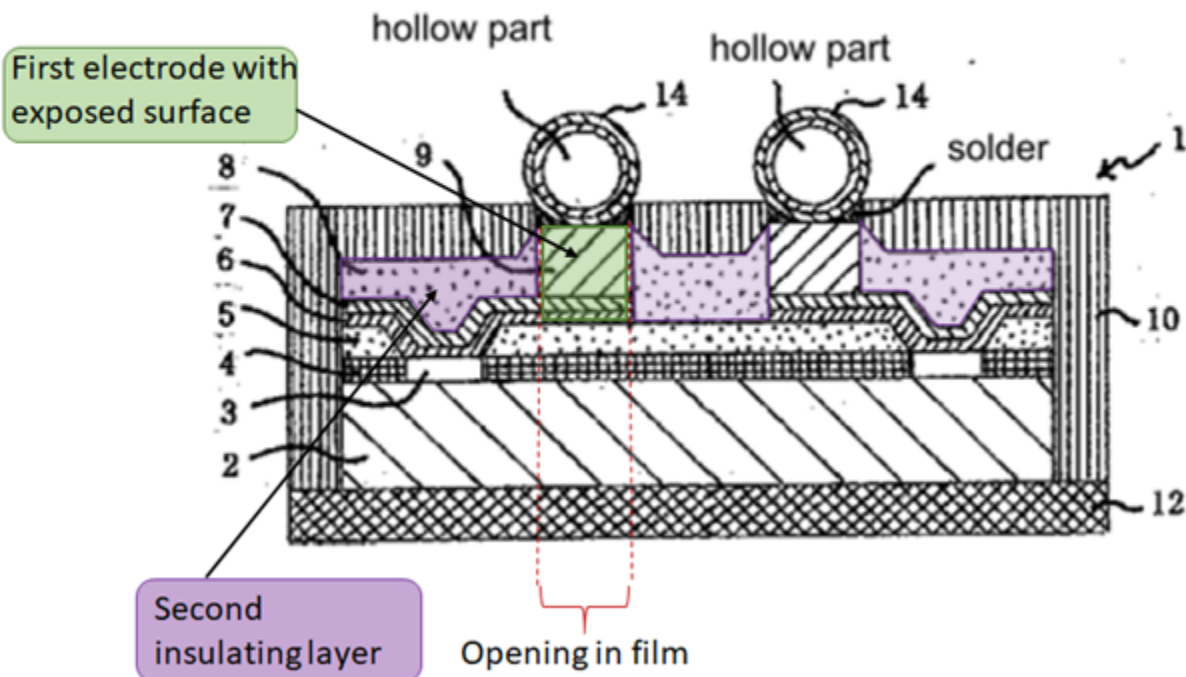
b) **[5 b]: wherein an opening of said insulating film exposes a surface of the first electrode portion**

156. Furuya discloses the second insulating layer is formed such that the tip of the metal post, the upper portion of the first electrode, is exposed in order to provide an external connection point. For example, Furuya teaches that “the second insulating layer 8 exposed the top face of the metal post 9 and covered the side face of the metal post 9.” Ex-1006, [0053]. *See also* Ex-1006, [0024] - [0024], [0027], [0062]. Furuya also teaches “**removing the insulating resin from the tip region**

of the metal post 9 for connecting to the outside.” *Id.*, [0046]. Thus, Furuya discloses forming an opening in insulating layer 8 to expose a surface of the first electrode portion.

157. Because the “top face” or “tip region” of the first electrode (which includes metal post 9) is exposed, a POSA would have recognized the desirability of making an opening in the insulating film to expose a surface of the first electrode portion, as shown in the annotated Figure 4(d) reproduced below. As stated in paragraph 57 of this report, Furuya teaches several methods that can be used to remove the second insulating layer 8 from the tip surface of the metal post and thus forming “an opening in said insulating film.” These methods as taught by Furuya include: photolithography, laser, dry etching, reverse sputtering or the like. Ex. 1006, [0048]. Furuya, describes that after the removal of the insulating film from the tip region of the metal post, the device formed is at the state depicted in Figure 4(d). *Id.*, [0046]

[FIG. 1]



- c) **[5 c]: wherein said surface of the first electrode portion is flush with or higher than a surface of the insulating film**

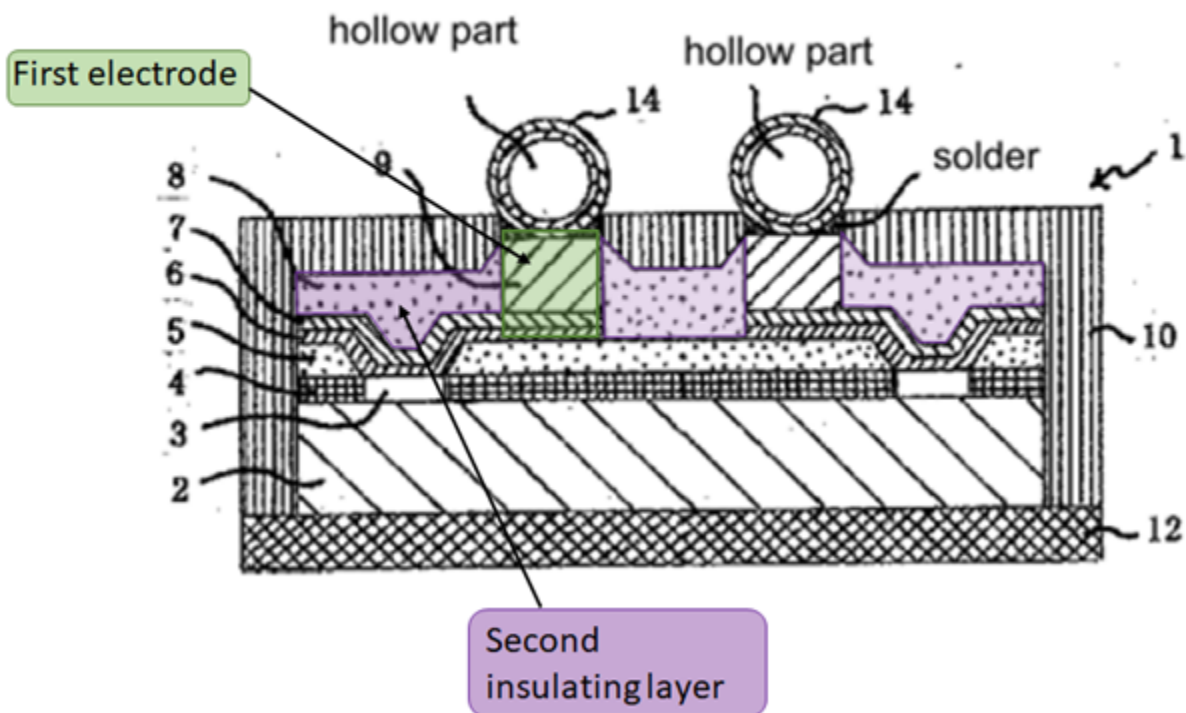
158. Furuya discloses the insulating film is formed at a lower level than the metal post, which post is a portion of the first electrode, and, as described above, the top of the metal post is exposed. For example, Furuya teaches that the metal posts 9 have a thickness of 15 μm above the wiring pattern, while the second insulating layer 8 only has a thickness of 10 μm above the wiring layer:

As shown in FIG. 4(d), the second insulating layer 8 exposed the top face of the metal post 9 and covered the side face of the metal post 9, and at other locations the

second insulating layer 8 was given a film thickness of 10 μm , so as to be lower than the top face of the metal post 9. ... Next, metal posts 9 made of copper (height 15 μm) were formed on the wiring pattern 7...

Ex-1006, [0053]. *See also* Ex-1006, [0062] - [0063]. This structure is shown in Figure 1, annotated below:

[FIG. 1]



159. Furuya also discusses these relative heights in connection with the description of the complete semiconductor device shown in Figure 1. For example, Furuya teaches that “after the metal post 9 is formed, the second insulating layer 8

is formed, using the insulating resin that has been applied and formed, and at this time, this is formed **so that the height of the second insulating layer 8, excluding the side face of the metal post 9, is such as to be a position that is lower than the height of the tip surface of the metal post 9.**” Ex-1006, [0047]. *See also id.*, [0017], [0029], [0031] - [0032]. The sides of the metal post are covered by the insulating film at a greater height than the remainder of the film for the sole purpose of improving the mechanical strength of the metal post. *Id.*, [0061]. Based on Furuya’s explicit teaching on how the structure depicted in Figure 4 (d) is formed, a POSA would understand that the exposed top indicates that the insulating film is at most flush with (or approximately flush as the ’001 Patent uses the term), and generally lower than, with the top surface of the metal post.

160. It is important to note in Furuya that the “second insulating layer 8” is the only disclosed insulating layer, i.e. a layer of material that is electrically insulating (in other words does not conduct electrical current). Specifically, Furuya discloses:

A known application means such as spin coating, curtain coating, screen printing or slit-and-spin coating may be used for applying the **insulating** resin that serves as the second insulating layer 8.

Ex-1006, [0048] (emphasis added).

161. Furuya discloses that an additional layer, i.e. “a sealing resin,” may be formed above the insulating layer. Specifically, Furuya discloses that “a cooling heatsink 12 for cooling the semiconductor element 2 is **sometimes** required.” In such cases:

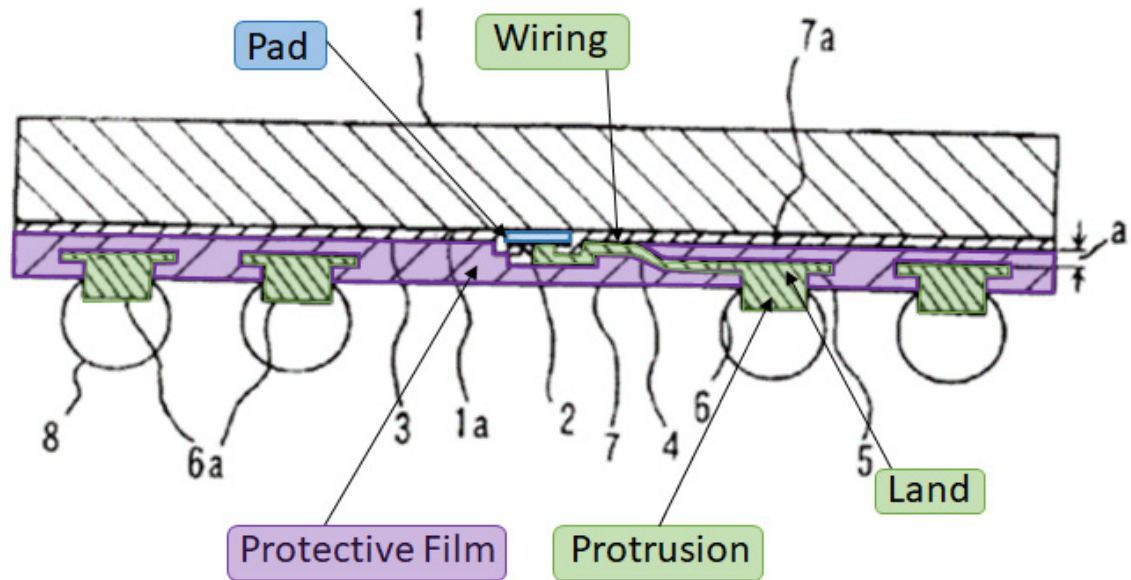
[A]fter affixing the cooling heatsink 12 to the semiconductor element, which has been formed up to the second insulating layer 8 shown in FIG. 4(d), this is sealed with the sealing resin 10 in a manner so as to expose the tip surface of the metal post 9 and the surface of the cooling heatsink 12.

Ex-1006, [0049] (emphasis added). Based on Furuya’s disclosures, a POSA would have readily understood that the “heatsink 12” and the “sealing resin 10” are optional elements that do not serve as an “insulating film.”

162. Moreover, Furuya shows that even when a sealing resin is used, the lower height of the insulating film compared to the height of the tip of the surface of the metal post, will result in a structure having the surface of the sealing resin being “close” to the surface of the metal post, “so that electrical connection failures between the metal post 9 and the external connection terminal 14 can be prevented.” Ex-1006, [0032].

163. To the extent the Board finds that Furuya's disclosure of the insulating film being flush with or lower than the first electrode portion insufficient, a POSA would have been motivated to combine Furuya with Yaguchi for the reasons discussed above. Yaguchi explicitly discloses that the first electrode portion is flush with or higher than the insulating film because it explains the first electrode portion is composed of a "land," i.e., enlarged portion of conductor material for making an electrical connection, connected to the conductive wiring and a protrusion formed on the land. Ex-1011, Ex-1011, 4:18-29. This first electrode portion parallels the disclosure of the first electrode portion described above for Furuya. These elements are used in conjunction with an external terminal to create an electrical connection between the pad and an external substrate. Ex-1011, 9:5-19. These elements are illustrated in Figure 1(a) where the protrusion is labeled 6, the pad is labeled 2, the wiring is labeled 4, and the land is labeled 5. I have annotated Figure 1(a) below to include these labels from Yaguchi.

FIG. 1(a)



164. Yaguchi further explains that a protective film, labeled 7 in the figure above, “covers a part of the passivation film 3, conductive wiring line 4, land 5, and protrusion 6 on the semiconductor element surface.” Ex-1011, 9:13-16. This protective film is an insulating layer made of “a poly[i]mide resin or the like.” Ex-1011, 9:26-28. Yaguchi explains that although some of the protrusion 6 is covered by the protective film, “[a] part of the protrusion 6 protrudes through the protective film 7 and this protruding part 6a is joined to the external terminal 8.” Ex-1011, 9:16-17. Thus, because protruding part 6a extends beyond the protective film, or insulating layer, Yaguchi teaches that the first electrode portion is higher than the insulating film.

165. Thus Furuya in view of Yaguchi discloses the subject matter of Claim 5 and Claim 5 is invalid.

3. Claim 14

- a) **[14 a]: The semiconductor device of claim 12, further comprising an insulating film formed on said metal wiring**

166. Claim element [14 a] is worded identically to claim element [5 a] and is disclosed for the reasons discussed with reference to that claim element.

- b) **[14 b]: wherein an opening of said insulating film exposes a surface of the first electrode portion**

167. Claim element [14 b] is worded identically to claim element [5 b] and is disclosed for the reasons discussed with reference to that claim element.

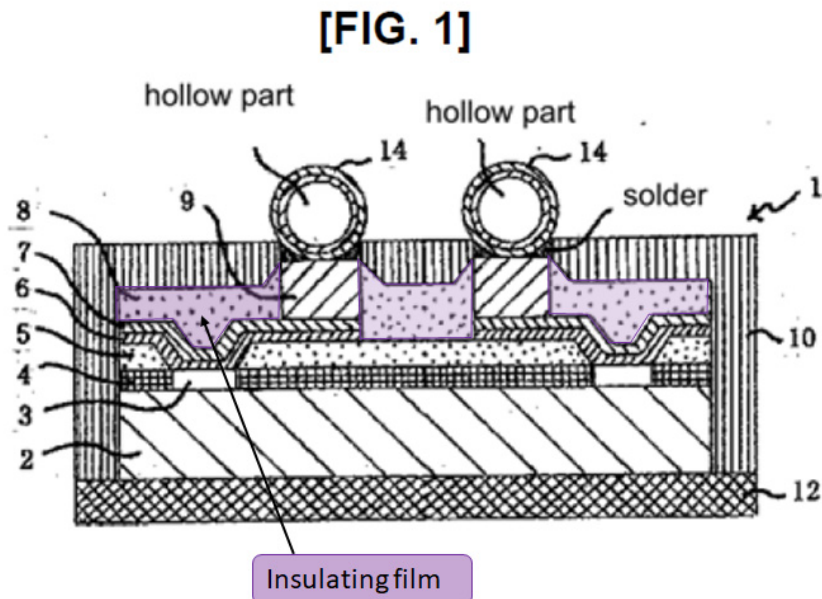
- c) **[14 c]: wherein said surface of the first electrode portion is flush with or higher than a surface of the insulating film**

168. Claim element [14 c] is worded identically to claim element [5 c] and is disclosed for the reasons discussed with reference to that claim element.

4. Claim Chart

U.S. Patent No. 6,954,001		Furuya in view of Takizawa and further in view of Yaguchi
	Claim 5	
5A	The semiconductor device of claim 3, further comprising an insulating film	Furuya, Figure 1 (reproduced and annotated below) depicts “an insulating film formed on said metal wiring” (designated numeral 8, “second insulating layer” and shaded purple).

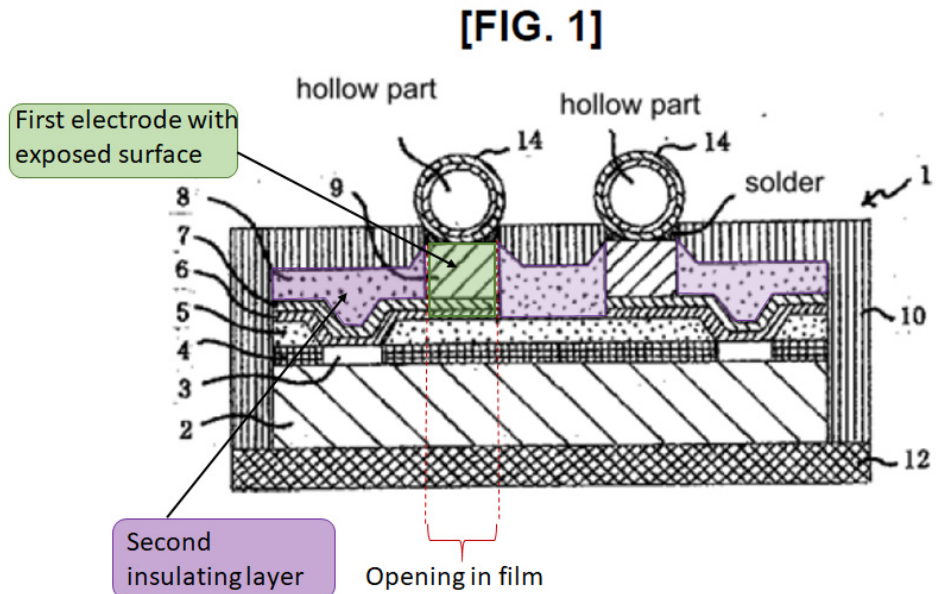
formed on said
metal wiring,



Furuya, [0016] (“[Means for Solving the Problems] In order to achieve the aforementioned object, the present inventors undertook earnest study and arrived at the present invention. That is to say, in claim 1, the semiconductor device is characterized in that a first insulating layer having substantially the same shape as a passivation film is formed on the passivation film, which has been formed on a semiconductor element, with an electrode, which has been formed on the semiconductor element, exposed; a wiring pattern, which is connected with the electrode of the semiconductor element, is formed on the first insulating layer; a metal post for external connection is formed on the wiring pattern; **a second insulating layer, which is in close contact with the wiring pattern**, is formed in a manner so as to cover a side face of the metal post excluding a tip surface of the metal post; resin sealing is performed with sealing resin in a manner so as to expose the tip surface of the metal post; and an external connection terminal is provided at the tip surface of the metal post.”)

Furuya, [0027] (“Hereafter, modes of embodiment of the present invention are described based on the drawings. In the semiconductor device 1 (CSP) of the present invention, as shown in FIG. 1, a first insulating layer 5, which has substantially the same shape as a passivation film 4, is formed on the passivation film 4, in a manner so as to expose electrodes 3, which have been formed on a

		<p>semiconductor element 2. Then, a wiring pattern 7 (wiring layer) that is connected with the electrodes 3 is formed on the first insulating layer 5, and metal posts 9 for external connection, having a height of approximately 3 μm to 50 μm, are formed at predetermined positions on the wiring pattern 7. <i>Next, a second insulating layer 8 is formed, which is in close contact with the wiring pattern 7</i> and the first insulating layer 5, and which covers the side face of the metal post 9 excluding the tip surface of the metal post 9.”)</p> <p>Furuya, [0028] (“<i>The structure of the semiconductor device 1 of the present invention is such as to prioritize adhesion between the second insulating layer 8 and the metal post 9</i> in the part of the metal post 9 that is lower than the tip end (closer to the semiconductor element). That is to say, the second insulating layer 8 is formed in a manner so as to cover the side face of the metal post 9 excluding the tip end part. As a result, the adhesion between the second insulating layer 8 and the metal post 9 is reinforced and, in conjunction therewith, the connection strength between the metal post 9 and the wiring pattern 7 is also improved, such that disconnection between the metal post 9 and the wiring pattern 7 can be prevented.”)</p> <p>Furuya, [0063] (“<i>Furthermore, the second insulating layer 8 is formed in a manner so as to cover the wiring pattern 7</i> and to form a region lower than the tip surfaces of the metal posts 9, excluding the side faces of the metal posts 9. ...”)</p>
5B	wherein an opening of said insulating film exposes a surface of the first electrode portion, and	Furuya, Figure 1 (reproduced and annotated below) depicts “an opening of said insulating film exposes a surface of the first electrode portion.”

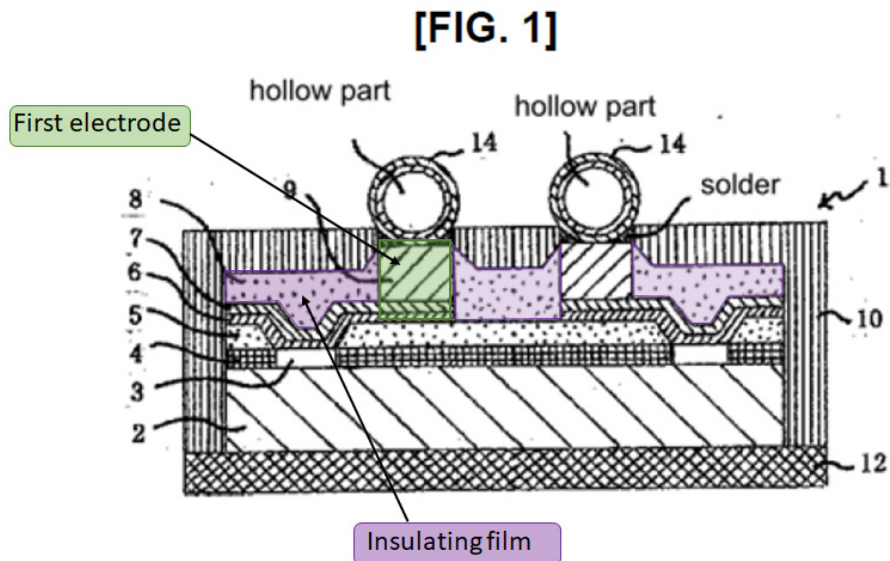


Furuya, [0053] (“Next, as shown in FIG. 4(c), a metal post 9 was formed on the wiring pattern 7, whereafter photosensitive polyimide (trade name "Pimel", made by Asahi Kasei Corp.) was applied on the first insulating layer 5 by spin coating, *whereafter the excess polyimide was removed by photoetching, excluding the top face [sic] and side face portions of the metal post 9, to produce a second insulating layer 8 (FIG. 4(d)). As shown in FIG. 4(d), the second insulating layer 8 exposed the top face of the metal post 9 and covered the side face of the metal post 9, and at other locations the second insulating layer 8 was given a film thickness of 10 μm, so as to be lower than the top face of the Metal post 9. ...*”)

Furuya, [0062] (“*Further, when the second insulating layer 8 is formed, spin coating is used, and for removal of unnecessary resin, including at the upper parts of the metal posts 9, photoetching is used.* This makes it possible to form the surface of the second insulating layer lower than the top face of the metal post, excluding the side faces of the metal posts 9. This allows the thickness of the semiconductor device 1 to be reduced, and allows electrical connection failure between the external connection terminal and the metal post caused by contact with the sealing resin to be prevented.”)

		<p>Furuya, [0023] (“Further, in claim 8, a method for manufacturing the semiconductor device according to claim 1, 2, 3, 4, 5, 6 or 7 is characterized by having, at least: a step of forming a first insulating layer on a passivation film, which has been formed on a semiconductor element in such a manner as to expose an electrode formed on the semiconductor element, in such a manner as to expose the electrode; a step of forming a wiring pattern, which is connected with the electrode, on the first insulating layer; a step of forming a metal post for external connection at a predetermined height, in a predetermined position on the wiring pattern; a step of forming a second insulating layer in which, after applying an insulating resin in a manner so as to include the metal post, <i>the insulating resin is removed from the region of the tip surface of the metal post that connects with the outside; a step of performing resin sealing with sealing resin in a manner so as to expose the tip surface of the metal post</i>; and a step of providing an external connection terminal at the tip surface of the metal post.”)</p> <p>Furuya, [0024] (“Furthermore, in claim 9, the method for manufacturing a semiconductor device according to claim 8 is characterized in that photolithography is used as a means for <i>removing the insulating resin from the region of tip surface of the metal post that connects with the outside</i>; and in claim 10, the method for manufacturing a semiconductor device according to claim 8 or 9 is characterized in that spin coating is used as a means for applying an insulating resin serving as the second insulating layer.”)</p> <p>Furuya, [0027] (“Hereafter, modes of embodiment of the present invention are described based on the drawings. In the semiconductor device 1 (CSP) of the present invention, as shown in FIG. 1 <i>Next, a second insulating layer 8 is formed</i>, which is in close contact with the wiring pattern 7 and the first insulating layer 5, and <i>which covers the side face of the metal post 9 excluding the tip surface of the metal post 9</i>.”)</p>
5C	wherein said surface of the first electrode	Furuya, Figure 1 (reproduced and annotated below) depicts “wherein said surface of the first electrode portion is flush with or higher than a surface of the insulating film”

portion is flush with or higher than a surface of the insulating film.



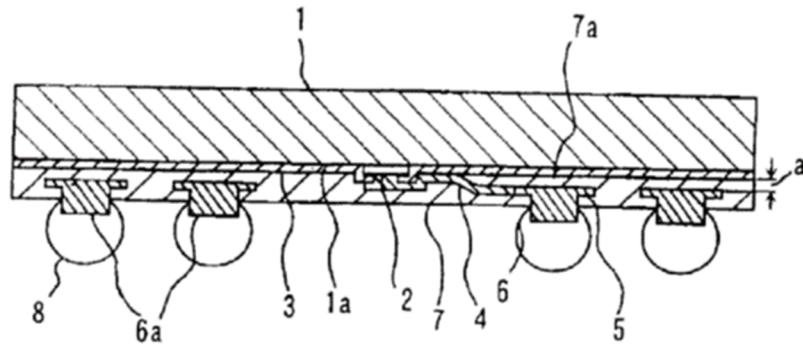
Furuya, [0053] (“Next, as shown in FIG. 4(c), a metal post 9 was formed on the wiring pattern 7, whereafter photosensitive polyimide (trade name "Pimel", made by Asahi Kasei Corp.) was applied on the first insulating layer 5 by spin coating, whereafter the excess polyimide was removed by photoetching, excluding the top face [sic] and side face portions of the metal post 9, to produce a second insulating layer 8 (FIG. 4(d)). As shown in FIG. 4(d), the second insulating layer 8 exposed the top face of the metal post 9 and covered the side face of the metal post 9, and at other locations the second ***insulating layer 8 was given a film thickness of 10 μm, so as to be lower than the top face of the metal post 9.*** Note that a mask plating method is used for forming the metal post 9, and the steps for the mask plating method are described below. Specifically, after producing FIG. 4 (b), a photosensitive resist layer having a film thickness of 20 μm was formed on the first insulating layer 5 and the wiring pattern 7, whereafter, using a known photoetching method, a plating mask 13 was formed, in which the wiring pattern 7 was exposed at the location where the metal posts were to be formed (FIG. 5 (a)). Next, ***metal posts 9 made of copper (height 15 μm)*** were formed on the wiring pattern 7, which was exposed by the plating mask 13, using an electrolytic plating method (FIG. 5 (d) [sic]). Next, the plating mask 13 was peeled off producing that in FIG. 4 (c).”)

	<p>Furuya, [0062] - [0063] (“Further, when the second insulating layer 8 is formed, spin coating is used, and for removal of unnecessary resin, including at the upper parts of the metal posts 9, photoetching is used. <i>This makes it possible to form the surface of the second insulating layer lower than the top face of the metal post</i>, excluding the side faces of the metal posts 9. This allows the thickness of the semiconductor device 1 to be reduced, and allows electrical connection failure between the external connection terminal and the metal post caused by contact with the sealing resin to be prevented.</p> <p>Furthermore, the second insulating layer 8 is formed in a manner so as to cover the wiring pattern 7 and to form a region lower than the tip surfaces of the metal posts 9, excluding the side faces of the metal posts 9. ...”)</p> <p>Furuya, [0017] (“Furthermore, in claim 2, the semiconductor device according to claim 1 is characterized in that <i>the height of the surface of the second insulating layer excluding the region of the side face of the metal post is established at a position lower than the tip surface of the metal post.</i>”)</p> <p>Furuya, [0047] (“<i>As described above, after the metal post 9 is formed, the second insulating layer 8 is formed, using the insulating resin that has been applied and formed, and at this time, this is formed so that the height of the second insulating layer 8, excluding the side face of the metal post 9, is such as to be a position that is lower than the height of the tip surface of the metal post 9.</i> For this purpose, it is preferable to use a photolithography method, in which a photosensitive insulating resin is used, and application, pattern exposure, development and the like are performed so as to remove the insulating resin in unnecessary parts.”)</p> <p>Furuya, [0029] (“Furthermore, as set forth in the foregoing claim 2, the surface of the second insulating layer 8 is formed in a manner so as to be at a position lower than the tip surface of the metal post 9, so as not to present an obstacle when mounting the external connection terminal 14 to the outside (for example, on a mounting board).”)</p>
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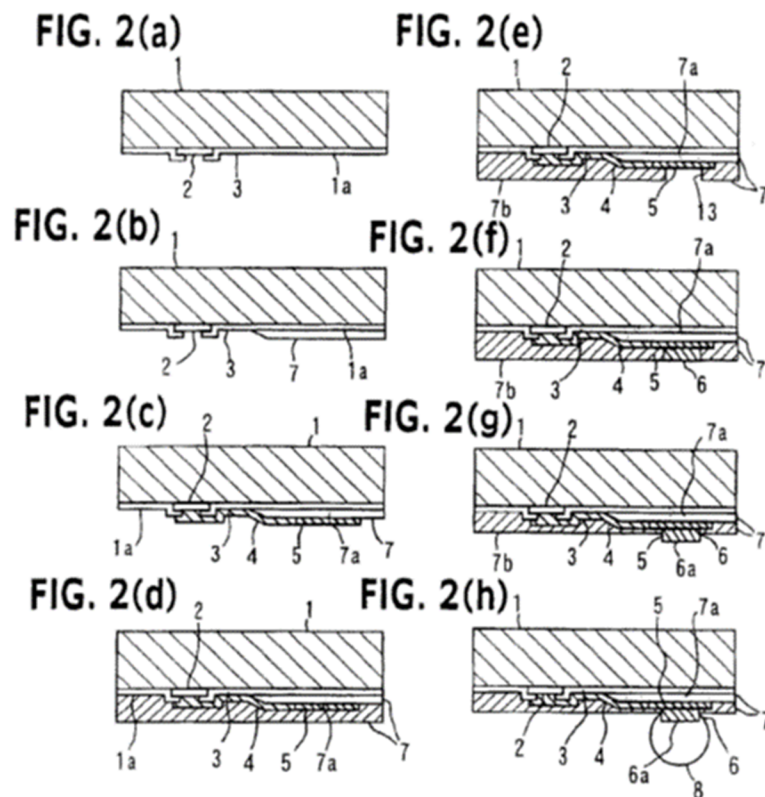
Furuya, [0031] - [0032] ("That is to say, as shown in FIG. 1, *it is proposed that the second insulating layer 8 be formed so that the height of the second insulating layer 8, excluding the location where this covers the side face of the metal post 9, is at a position lower than the height of the tip surface of the metal post 9. ...*

Yaguchi, Figure 1(a)

FIG. 1(a)



Yaguchi, Figure 2



Yaguchi, Resolution Means("A protrusion is formed on the land of the external terminal connector of the semiconductor device and the protruding part of the protrusion is connected to the external terminal. Also, a protective film intervening part made up of a resin material if formed between the land and the semiconductor terminal.")

Yaguchi, 4:18-29 ("(1) Having a protrusion formed on the land to which the external terminal is bonded, this protrusion being bonded to the external terminal made of solder material or the like, and a protective film being formed between the passivation film and the land.

The protrusion is preferably bonded to the external terminal so that the protrusion protrudes into the inside of the external terminal. The land of the semiconductor device is formed out of metal material such as copper (Cu). This material has a higher rigidity than that of solder used as the material for the external terminal and that of the protective film that covers the semiconductor element surface. As the protrusion and external terminal are bonded together in the manner described above, deformation of the external terminal near the bond

	<p>part on the semiconductor device side is constrained by the protrusion. Thus, the thermal distortion that occurs on the external terminal near the bond on the semiconductor device side can be reduced.”)</p> <p>Yaguchi, 9:5-28 (“As shown in FIG. 1 and FIG. 2 the semiconductor device of embodiment 1 of the present invention comprises a semiconductor element 1, a passivation film 3 formed so the surface of a pad 2 on the semiconductor device surface 1a is exposed, a conductive wire line 4 connected to the pad 2, a land 5 connected to the conductive wire line 4, a protective film 7, a protrusion 6 provided on the land 5, and an external terminal 8.</p> <p>The pad 2 is arranged vertically in the center of the semiconductor element surface and the conductive wiring line 4 connected to the pad 2 extends to the land 5 on which the protrusion 6 is formed on the semiconductor element surface 1a. The protective film 7 covers a part of the passivation film 3, conductive wiring line 4, land 5, and protrusion 6 on the semiconductor element surface 1a and is also provided between the land 5 and passivation film 3 and forms the intervening portion 7a of the protective film. A part of the protrusion 6 protrudes through the protective film 7 and this protruding part 6a is joined to the external terminal 8. The pad 2 of the semiconductor element 1 and external terminal 8 are electrically connected via the conductive wiring line 4, land 5, and protrusion 6.</p> <p>The conductive wire line 4 is made up of a single or alloy of a plurality of materials out of copper (Cu), aluminum (Al), gold (Au), or silver (Ag) or the like. In addition, there are also cases where a plating of nickel (Ni) or chromium (Cr) is applied to the surface. The land 5 connected to the conductive wire line 4 is also formed of the same material as the conductive wire described above.</p> <p>Solder material (for example Pb-Sn system eutectic solder or sn-Ag-Cu system solder) or the like is used where a spherical shaped piece of material or paste type solder material is placed on protruding part of the protrusion where it is melted and bonded to the land. Examples of materials that can be used for the protective film 7 include liquid or film type polyamide resin, polyether imide resin, acrylic denatured</p>
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	<p>epoxy resin, epoxy resin mixed with rubber, or silicon resin or the like.”)</p> <p>Yaguchi, 11:8-27 (“The protective film 7 of polyamide resin or the like is formed on the pad 2 and the surface 1a (a) of the semiconductor element 1 form with a passivation film 3 formed covering the semiconductor element surface 1a with a part of the pad 2 exposed using the potting method, printing method, or pasting of a film type material (b). The conductive wiring line 3 [sic] is formed through the surface of the protective film 7 while in addition, the land 5 is provided on the surface of the protective film 7 (c). The conductive wiring line 3 [sic] are formed using a plating method or sputtering method. The protective film 7 provided on top of the semiconductor element surface 1a is between the land 5 and semiconductor element surface 1a becoming the intervening part 7a of the protective film. Furthermore, the protective film 7 is formed so as to cover the conductive wiring line 4 and land 5 on the surface of the semiconductor element 1a (d). An opening 13 is formed on the surface 7b of the protective film 7 exposing the surface of the land 5 (e). The opening 13 is formed by masking the area where the opening is not formed, forming the opening using an etching method, and then removing the mask or using a hole forming method using a laser.</p> <p>The opening 13 is filled with a metal material such as copper (Cu) using a sputter method or plating method to form a protrusion 6 on the land 5 (f). The protective film 7 is removed from the surface 7b using etching, the protruding part 6a is formed such that a part of the protrusion 6 is caused to protrude from the surface 7a of the protective film 7 (9). The protruding part 6a of the protrusion 6 is bonded to the external terminal 8 made up of solder material (h). This is cut to prescribed size to obtain the semiconductor device shown in embodiment 1 of the present invention.”)</p> <p>Yaguchi, 18:3-6 (“In Fig. 9, the structure of the semiconductor device is basically the same as the semiconductor device of embodiment 3 shown in Fig. 7 and a point of difference is that a protrusion 6 is formed on a land 5 and a protrusion part 6a protruding from the protective film 15 is bonded to the external terminal 8.”)</p>
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		Yaguchi, 24:1-8 (“As described above, according to the semiconductor device and semiconductor module of the present invention, strain generated in the external terminal due to the difference in coefficients of linear thermal expansion between a printed wiring board and the semiconductor device mounted on the printed wiring board can be reduced and disconnection of the external terminal can be prevented. The invention is effective in preventing disconnection of the external terminal of a semiconductor device, particularly, a semiconductor device of a chip size to be manufactured by wafer processes. A small semiconductor device and a semiconductor module having a high reliability can therefore be provided.”))
14A	The semiconductor device of claim 12, further comprising an insulating film formed on said metal wiring,	<i>See Claim Element 5A</i>
14B	wherein an opening of said insulating film exposes a surface of the first electrode portion, and	<i>See Claim Element 5B</i>
14C	wherein said surface of the first electrode portion is flush with or higher than a surface of the insulating film.	<i>See Claim Element 5C</i>

D. Ground 3: Furuya In View Of Knowledge Of A POSA (as evidenced by Nozawa) Renders Obvious Claims 9 and 18

1. Reasons To Combine Furuya And Nozawa

169. A POSA would have been motivated to combine Furuya and Takizawa for the reasons above in relation to Ground 1. A POSA would have known that semiconductor devices like those disclosed in Furuya and Takizawa must be connected through wiring electrodes to other semiconductor devices in order to be useful. This understanding of the importance of connecting semiconductor devices is confirmed by Nozawa. A POSA would have known that applying the teaching of Nozawa to the device described in Furuya would provide benefits including integration with a wide variety of PCBs for a wide range of applications.

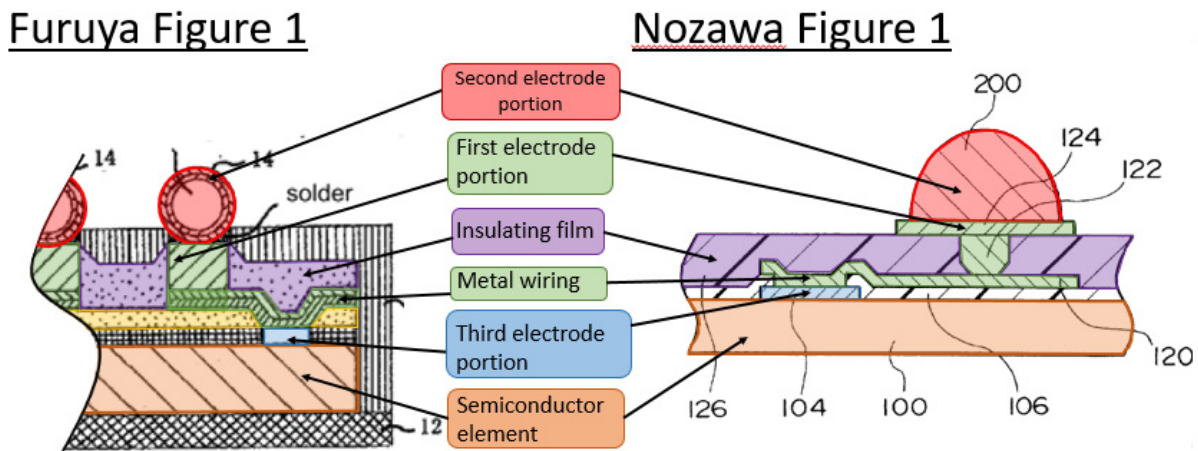
170. For example, Nozawa teaches that it allows for a reliable connection to be formed directly between the solder bumps and a substrate, allowing for more compact and lightweight electronic devices. Ex-1012, 1:20-31; 1:41-48. Additionally, Nozawa teaches that its device allows connection with a wider range of substrates, including those with much greater thermal expansion coefficients, which would allow the device of Furuya to be used in a wider variety of circumstances. Ex-1012, 8:32-40.

171. Moreover, Nozawa reflects that a POSA would have known to connect the second electrode portion in Furuya to the wiring electrode of an

external substrate. Nozawa explains that such a substrate would include wiring for the connection and provides an illustration of the semiconductor device connecting with the substrate. Ex-1012, 8:30-44, Fig. 9. This is consistent with the understanding a POSA would have that a chip-scale packaging device (CSP), such as Furuya, is only useful to the extent it is connected to an external substrate. Such a connection allows the device to receive power, connect with other semiconductor devices, become integrated as part of a larger device, and serve a useful function. Nozawa, also a CSP, provides an example of how this is to be done.

172. Both Furuya and Nozawa are in the same field of technology and were filed around the same time. Furuya and Nozawa are directed toward very similar systems that operate in a similar manner. For example, Furuya teaches a semiconductor device that has “a semiconductor element, with an electrode, which has been formed on the semiconductor element, exposed; a wiring pattern, which is connected with the electrode of the semiconductor element, is formed on the first insulating layer; a metal post for external connection is formed on the wiring pattern; [and] a second insulating layer, which is in close contact with the wiring pattern.” Ex-1006, Abstract. Similarly, Nozawa describes a semiconductor device comprising “a semiconductor chip having electrodes; an interconnect layer connected to the electrodes; a conducting layer formed on the interconnect layer, ... a bump formed on the underlying metal layer; and a resin layer (insulating

protection layer) formed around the conducting layer.” Ex-1012, 1:53-64. Thus, both references are directed to very similar semiconductor devices as shown in the annotated figure below.¹³



173. Because the devices are so similar, applying the teachings of Nozawa to the device in Furuya would have been natural to a POSA. Because such a combination would be nothing more than applying known techniques to similar

¹³ A POSA would have recognized that Nozawa and Furuya use different terminology to refer to elements that are the same. For ease of reference, the labels below are those used by the claims of the '001 Patent.

system, a POSA would have expected the combination to yield a predictable result and be successful. *Id.*

2. Claim 9: The semiconductor device of claim 1, further comprising a substrate having a wiring electrode, wherein said wiring electrode is electrically connected to said second electrode portion

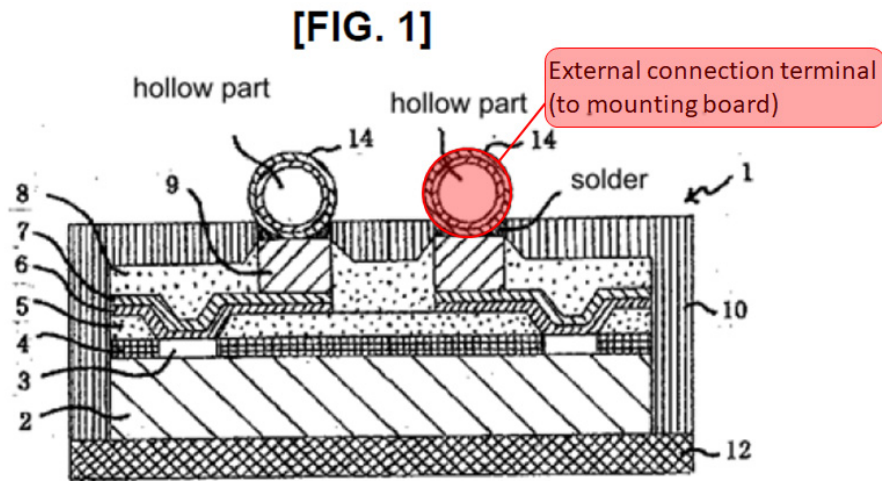
174. Furuya discloses this limitation because the metal posts (i.e., first electrode portion) are connected to an external connection terminal (i.e., second electrode portion) to form external electrical connections with other electrodes, for example wiring electrodes on a mounting board or PCB (i.e., wiring electrode). Ex-1006, [0006]. *See also, e.g.,* Ex-1001, 1:20-32, 2:1-11. Moreover, Furuya refers to CSP and a POSA would have understood that the problems overcome by Furuya, such as the thermal stresses as a result of the difference in the thermal expansion coefficient arise in the context of mounting the semiconductor device to a substrate, or as it referred by Furuya “mounting board;” such stresses also develop during thermal cycling. Ex-1006, [0001], [0006], [0008], [0009], [0011].

175. In Furuya there is ample description of testing performed to validate the advantages of the CSP semiconductor device when such device is mounted onto a substrate. Specifically, Furuya discloses that “[t]he semiconductor device 1 produced in the present embodiment was mounted on a printed board.” Ex-1006, [0056]. Moreover, Furuya discloses that “[t]he printed board on which the semiconductor device 1 according to the present embodiment was mounted was

subjected to a temperature cycle test of -45°C to +125°C to evaluate reliability, and no disconnections occurred even after a 1000 cycle test was performed.” *Id.*, [0058]. Since Furuya’s objective was to improve the reliability of the “electrical connections with a mounting board on which the semiconductor device is mounted,” and since such improvements are explicitly disclosed in Furuya as a result of the disclosed tests that were performed, a POSA would have understand that such “mounting board” or “printed board” would comprise a wiring electrode which is electrically connected to second electrode portion. Otherwise Furuya would not have been able to perform these reliability tests.

176. Furuya teaches that “a characteristic of the semiconductor device 1 of the present invention, as shown in FIG. 1, is that an **external connection terminal 14 that makes an external electrical connection (for example, to a mounting board)** is placed at the tip end of the metal post 9.” Ex-1006, [0036]. *See also id.*, [0006], [0029], [0039], [0043]. These external connection terminals 14, which correspond to the “second electrode portion” of the ’001 Patent, are shown in Figure 1, annotated below, though the connection to the mounting board on the external substrate is not shown (as is also the case in the figures for the ’001 Patent). Thus, just like the ’001 Patent, Furuya teaches that the first electrode portion (which includes “metal post 9”) is electrically connected to a wiring electrode (i.e., the electrode on the substrate or “mounting board”) and this

electrical connection is made through the external connection terminal 14 (i.e., second electrode portion). If the device in Furuya was not connected in this manner, the described “external electrical connection” would not be possible. See *id.*



177. This disclosure of wiring electrode in Furuya is similar in scope to what is disclosed by the '001 Patent. For example, in the embodiments disclosed by the '001 Patent, a “wiring electrode” of the “substrate” refers to an external electrical connection on the circuit board on which the disclosed semiconductor device is mounted:

In order to electrically connect the electrodes 2 formed on the surface of the semiconductor element 1 **to wiring electrodes of a substrate (not shown)** on which the semiconductor element 1 is mounted, 60 respectively, a

ball electrode 6 formed from solder is connected in a molten state to each opening of the solder resist film 3, that is, to the external electrode portion of each metal wiring 4.

Ex-1001, 1:57-64. *See also* Ex-1001, 8:56-60 (“The external electrode portions 14a and the wiring electrodes of the substrate on which the semiconductor device is mounted are respectively connected to each other by the ball electrodes 16.”).

178. To the extent Patent Owner argues that Furuya does not explicitly or implicitly disclose electrically connecting the second electrode portion to a wiring electrode of a substrate, establishing an electrical connection to a substrate having a wiring electrode is obvious to a person of ordinary skill in the art because it provides the electrical connection necessary for the semiconductor device to function. Establishing this electrical connection is admitted by the applicant of the ’557 Patent to be known in the prior art. *See* Ex-1001, 1:60-67. Moreover, establishing an electrical connection to a wiring electrode of a substrate through an external electrode on a semiconductor device is well within the knowledge and skill of a person of ordinary skill in the art.

179. To the extent the Board finds Furuya’s disclosure of wiring electrode to be insufficient, a POSA would have known that the device in Furuya would have been of limited use unless electrically connected to another device via the wiring on a substrate, e.g., mounting board or printed circuit board (PCB). This is confirmed

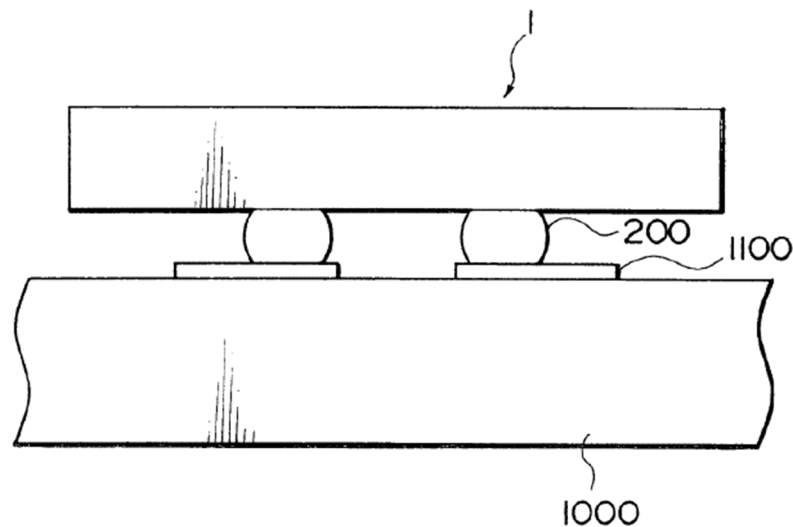
by Nozawa, as discussed above, because Nozawa explicitly discloses a substrate having a wiring electrode that is electrically connected to the second electrode portion. In fact, one of the stated goals of Nozawa is to establish a “direct connection to a substrate” from a semiconductor device. Ex-1012, 1:46-47.

180. After describing a semiconductor device similar to the device disclosed in Furuya, Nozawa teaches that the semiconductor device is connected to a substrate:

In FIG. 9 is shown a circuit board 1000 on which is mounted this embodiment of the semiconductor device 1. For the circuit board 1000 is generally used an organic substrate such as a glass epoxy substrate or the like. On the circuit board 1000, an interconnect pattern 1100 of for example copper is formed to constitute a desired circuit, and by mechanical connection of the interconnect pattern thereof to the bumps 200 forming the external electrodes of the semiconductor device 1, electrical connection is achieved.

Ex-1012, 8:30-44. Figure 9 below illustrates the connection between the semiconductor device and the circuit board.

FIG. 9



181. To the extent that Patent Owner argues that the “wiring electrode” should instead be mapped to the electrode formed on the silicon substrate (e.g., depicted as numeral 12 in Ex-1001, Fig. 5), Furuya also discloses this wiring electrode for the reasons discussed above in Section VII.B.4.

182. In view of the foregoing, persons of ordinary skill in the art would have understood that Furuya in view of Nozawa, discloses “the semiconductor device of claim 1, further comprising a substrate having a wiring electrode, wherein said wiring electrode is electrically connected to said second electrode portion.” Accordingly, Claim 9 is invalid.

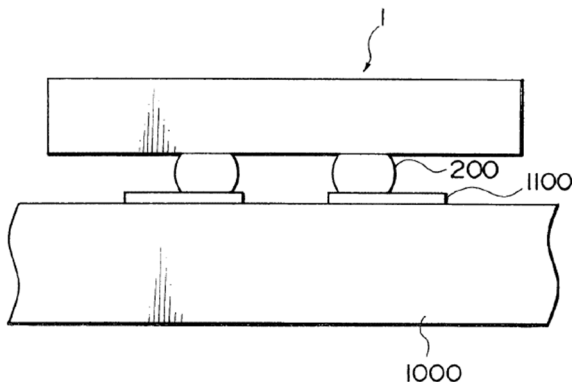
3. **Claim 18: The semiconductor device of claim 10, further comprising a substrate having a wiring electrode, wherein said wiring electrode is electrically connected to said second electrode portion**

183. Claim 18 is worded identically to Claim 9 and is disclosed for the reasons discussed with reference to that claim.

4. **Claim Chart**

U.S. Patent No. 6,954,001		Furuya in view of Takizawa and further in view of Nozawa
	Claim 9	
9	The semiconductor device of claim 1, further comprising a substrate having a wiring electrode, wherein said wiring electrode is electrically connected to said second electrode portion.	<p>Furuya, Figure 1, (reproduced and annotated below) implicitly depicts “a substrate having a wiring electrode, wherein said wiring electrode is electrically connected to said second electrode portion” by showing the external connection terminals for the semiconductor device.</p> <p style="text-align: center;">[FIG. 1]</p> <p>Furuya, [0006] (“The metal posts 69 are electrically connected to the electrodes 63 by way of the wiring pattern 67, and electrical connections between the semiconductor device 61 and the outside, for example, <i>electrical connections with a mounting board on which the semiconductor device 61 is mounted, are made by way of the metal posts 69.</i> Note that, if necessary, as shown in FIG. 6, a solder ball 71 or the like is sometimes formed as</p>

U.S. Patent No. 6,954,001	Furuya in view of Takizawa and further in view of Nozawa
	<p>an external connection terminal 74 on the top face of the metal post 69.”)</p> <p>Furuya, [0029] (“Furthermore, as set forth in the foregoing claim 2, the surface of the second insulating layer 8 is formed in a manner so as be at a position lower than the tip surface of the metal post 9, so as not to present an obstacle <i>when mounting the external connection terminal 14 to the outside (for example, on a mounting board).</i>”)</p> <p>Furuya, [0036] (“Next, a characteristic of the semiconductor device 1 of the present invention, as shown in FIG. 1, is that an external connection terminal 14 that makes <i>an external electrical connection (for example, to a mounting board)</i> is placed at the tip end of the metal post 9, the external connection terminal 14 being configured with an electroconductive material provided on the surface of a support having a hollow part opened to the outside.”)</p> <p>Furuya, [0039] (“... Because the hollow support 15 has a flexible structure, even <i>if the mounting board that is connected to the external connection terminal 14</i> repeatedly thermally expands and contracts by a considerable amount, the stress generated can be absorbed and thus mitigated. Consequently, it is possible to prevent cracks from occurring, and to prevent wire breakage due to cracks in the insulating layer at the interface between and the sealing resin and the external connection terminal 14.”)</p> <p>Furuya, [0043] (“Next, the semiconductor device 1 of the present invention <i>performs fixation and electrical connection with the outside (for example, to a mounting board) by way of the external connection terminal 14</i>, and an electroconductive material 16 is provided on the surface</p>

U.S. Patent No. 6,954,001	Furuya in view of Takizawa and further in view of Nozawa
	<p>of the support 15 comprised by the external connection terminal 14.”)</p> <p>Nozawa, Figure 9 depicts the mounting of a semiconductor device to a substrate having a wiring electrode:</p> <p style="text-align: center;">FIG. 9</p>  <p>Nozawa, 1:6-8 (“The present invention relates to a Semiconductor device and method of manufacturing the Same, a circuit board and an electronic instrument.”)</p> <p>Nozawa, 1:20-48 (“In recent years, with the more compact design of electronic instruments, there has been an active move toward directly connecting a semiconductor device having solder bumps to the substrate, to provide even more compact and lightweight electronic instruments. In view of this, there is an increasing demand for a reliable connection of the semiconductor chip to a substrate with a greatly differing coefficient of thermal expansion. For example, as disclosed in Japanese Patent Publication No. 7-105586, a construction has been proposed whereby the underlying metal of substantially the same size as the solder bumps is formed as a multilayer metal layer providing stress relief.</p>

U.S. Patent No. 6,954,001	Furuya in view of Takizawa and further in view of Nozawa
	<p>However, for the actual connection of the semiconductor device, there are problems of the process becoming complicated or additional materials cost being incurred, because for example the mounting is on a substrate restricted to having a coefficient of thermal expansion close to that of the semiconductor chip, or the semiconductor chip is limited in size, or after the connection an additional step of injecting resin is required.</p> <p>The present invention solves the above problems, and has as its object the provision of a semiconductor device and method of manufacture thereof, a circuit board and an electronic instrument such that without requiring selection of the substrate material or additional steps after connection, connection reliability can be assured, direct connection to a substrate is possible, and further an electronic instrument can be made more compact and lightweight.”)</p> <p>Nozawa, 8:30-44 (“In FIG. 9 is shown a circuit board 1000 on which is mounted this embodiment of the semiconductor device 1. For the circuit board 1000 is generally used an organic substrate such as a glass epoxy substrate or the like. On the circuit board 1000, an interconnect pattern 1100 of for example copper is formed to constitute a desired circuit, and by mechanical connection of the interconnect pattern thereof to the bumps 200 forming the external electrodes of the semiconductor device 1, electrical connection is achieved. The semiconductor device 1 is provided with a function to relieve thermal stress generated as a result of the difference between the coefficient of thermal expansion of the circuit board 1000 and the coefficient of thermal expansion of the semiconductor chip.”)</p>
18	<p>The semiconductor</p> <p><i>See Claim 9.</i></p>

U.S. Patent No. 6,954,001		Furuya in view of Takizawa and further in view of Nozawa
	or device of claim 10, further comprising a substrate having a wiring electrode, wherein said wiring electrode is electrically connected to said second electrode portion.	

VIII. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

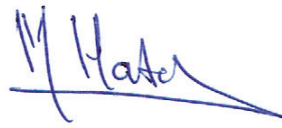
184. I am unaware of any evidence of secondary considerations or objective indicia of non-obviousness that have the requisite nexus to the claimed features that were not already known in the art as of December 20, 2001.

Accordingly, I am unaware of any secondary considerations that would suggest Claims 1-18 of the '001 Patent were not obvious to persons of ordinary skill in the art as of that date.

IX. CONCLUSION

185. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: March 16, 2018



Miltiadis K. Hatalis