

REQUEST FORM FOR **APPLICATION UNDER 37 CFR 1.53(b)**

DOCKET NUMBER: 60188-932

Prior Application:

Art Unit:

9454

Examiner:

Andy HUYNH

Box NEW APPLICATIONS FEE Mail Stop NEW APPLICATIONS Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

This is a Request for filing a Divisional application under 37 CFR 1.53(b) of pending prior application

Serial No. 10/307,450, filed on December 2, 2002, entitled SEMICONDUCTOR DEVICE AND

MANUFACTURING METHOD THEREOF, by the following named inventors: Yoshifumi NAKAMURA,

Ryuichi SAHARA, Nozomi SHIMOISHIZAKA, Kazuyuki KAINOU, Keiji MIKI, Kazumi WATASE and

Yasutake YAGUCHI.

- 1. I hereby state that the enclosed application contains no new matter.
- 2. Oath or Declaration
 - Newly executed (original or copy) a.
 - \boxtimes Copy from a prior application (37 CFR 1.63(d)) b.
 - Deletion of inventor(s)

Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR

1.63(d)(2) and 1.33(b).

3. Incorporation By Reference (useable if Box 2b is checked)

> The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 2b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

- 4. Preliminary Amendment is enclosed.
- 5. An Information Disclosure Statement and PTO1449 Form are submitted herewith.
- 6. Cancel claims 2-13.

DOCKET NUMBER: 60188-932

7. The filing fee is calculated on the basis of the claims existing in the prior application as amended at 4 and 6 above:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
	CLAIMS		CLAINIS	RAIL	AMOUNT
Total Claims	10	-20	0	\$18.00 =	\$0.00
Independent Claims	1	-3	0	\$86.00 =	\$0.00
	\$770.00				
	\$0.00				
	\$770.00				
	\$0.00				
	\$770.00				
AMOU	\$770.00				

- 7a. Enclosed is a Verified Statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- 7b. A verified Statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 was filed in prior application and such status is still proper and desired.
- 8a. PLEASE CHARGE DEPOSIT ACCOUNT 500417 in the amount of \$ 770.00
- 8b. The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 which may be required, including any extension of time fees to maintain the pendency of the parent application Serial No. 10/307,450 or credit any overpayment to Deposit Account No. 500417.
- 9. Amend the specification by inserting before the first line the sentence:
 - -- This application is a divisional of Application Serial No. 10/307,450 filed December 2, 2002.--.
- 10. Priority of Application Serial No. 2001-387051 filed on December 20, 2001, in Japan is claimed under 35 USC 119. The certified priority document(s) were filed in Serial No. 10/307,450 on December 2, 2002.
- 11. The prior application is assigned of record to

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. Osaka, JAPAN

12. The power of attorney in the prior application is to:

McDermott, Will & Emery

- 13. Also enclosed:
 - Copy of transmittal of Revocation of Power of Attorney and Request for change of Address in Parent Application

DOCKET NUMBER: 60188-932

14. A petition, fee and response has been filed to extend the term in the pending prior application until.

Address all future communications to: (May only be completed by applicant, or attorney or agent of record)

McDermott Will & Emery LLP 600 13th Street, N.W. Washington, D. C. 20005-3096

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty Registration No. 36,139

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Date: August 17, 2004

Customer Number 20277

WDC99 964608-1.060188.0932

Attorne, Docket No.: 60188-370

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Group Art Unit: 2811

Yoshifumi NAKAMURA, et al.

: Examiner: Not Yet Assigned

Serial No.: 10/307,450

:

Filed: December 2, 2002

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

TRANSMITTAL OF REVOCATION OF POWER OF ATTORNEY AND REQUEST FOR CHANGE OF ADDRESS

Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

Sir:

For:

Enclosed is a Revocation of Power of Attorney, Appointment and Certification Under 37 CFR 3.373(B) for the above referenced application.

Please change the USPTO records to reflect our Docket Number as noted above.

Also, please address all future correspondence to:

McDermott, Will & Emery 600 13th Street, N.W. Washington, D.C. 20005-3096 20277

Respectfully submitted,

McDERMOTT, WILL & EMERY

Dated:

By:

Michael E, Fogarty

Registration No. 36,139

600 13th Street, N.W., Suite 1200 Washington, D.C. 20005-3096

Tel: (202) 756-8000 Fax: (202) 756-8087



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Group Art Unit: 2811

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SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

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Dated:

By:

Michael E, Fogarty

Registration No. 36,139

600 13th Street, N.W., Suite 1200 Washington, D.C. 20005-3096

Tel: (202) 756-8000 Fax: (202) 756-8087

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

The present invention generally relates to a semiconductor device in which a metal wiring is formed so as to be electrically connected to an electrode of a semiconductor element and a part of the metal wiring is used as an external electrode, and a manufacturing method of the same. More particularly, the present invention relates to a semiconductor device having excellent junction reliability between a metal wiring and a ball electrode mounted to an external electrode portion of the metal wiring, and a manufacturing method of the same.

With recent reduction in size and improvement in functions of electronic equipments, an increasing number of input/output (I/O) pins is formed in a semiconductor element, and therefore the pitch of electrodes is reduced.

Especially in a CSP (Chip Size Package) type semiconductor device, electrodes of a semiconductor element are formed by a dry etching method in a diffusion process, whereas wiring electrodes of a substrate on which the semiconductor element is mounted are formed by a wet etching method in an assembling process. Accordingly, the pitch of the wiring electrodes of the substrate on which the semiconductor element is mounted is necessarily greater than that of the electrodes of the semiconductor element. In view of this, a semiconductor device is increasingly developed which deals with the difference between the electrode pitch of the semiconductor element and the wiring-electrode pitch of the substrate. In such a semiconductor device, metal wirings are formed so as to be electrically connected to the respective electrodes of the semiconductor element and a part of each metal wiring is used as an external electrode in order to increase the distance between the external electrodes.

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Hereinaster, a conventional semiconductor device will be described with reference to the figures.

FIG. 15A is a perspective plan view of the conventional semiconductor device.

FIG. 15B shows an example of the cross-sectional structure taken along line XV-XV of FIG. 15A. FIG. 15C shows another example of the cross-sectional structure taken along line XV-XV of FIG. 15A.

As shown in FIGs. 15A and 15B, electrodes 2 are formed on the surface of a semiconductor element 1. A passivation film 3 is formed over the surface of the semiconductor element 1. The passivation film 3 is formed from silicon nitride (SiN) or the like, and has an opening on each electrode 2. Metal wirings 4 are formed on the passivation film 3. Each metal wiring 4 is formed from copper (Cu) and electrically connected to a corresponding one of the electrodes 2. A solder resist film 5 is formed on the metal wirings 4 and the passivation film 3. The solder resist film 5 has an opening on a portion of each metal wiring 4 which functions as an external electrode (hereinafter, referred to as "external electrode portion"). In order to electrically connect the electrodes 2 formed on the surface of the semiconductor element 1 to wiring electrodes of a substrate (not shown) on which the semiconductor element 1 is mounted, respectively, a ball electrode 6 formed from solder is connected in a molten state to each opening of the solder resist film 3, that is, to the external electrode portion of each metal wiring 4.

As shown in FIG. 15C, an insulating resin layer 7 may be formed between the semiconductor element 1 having the passivation film 3 thereon and the metal wirings 4.

In each of the forms of the conventional semiconductor device described above, the wiring electrodes of the substrate on which the semiconductor device is mounted are respectively connected to the metal wirings 4 of Cu formed on the surface of the semiconductor element 1 through the ball electrodes 6 formed from solder. In other

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words, when the metal wirings 4 are formed from Cu (which is a commonly used metal wiring material), metal junction of Cu (the metal wirings 4) and solder (the ball electrodes 6) is formed at the boundary between the metal wiring 4 and the ball electrode 6.

In the above conventional semiconductor device, however, tin (Sn) contained in solder of the ball electrode 6 diffuses into Cu of the metal wiring 4 to form a Sn-Cu alloy layer. As a result, in the portion of the metal wiring 4 on which the ball electrode 6 is mounted (i.e., the external electrode portion) and the portion near the external electrode portion, the Sn-Cu alloy grows in the most part of the metal wiring 4. The Sn-Cu alloy is weak and hard. The semiconductor device 1, the resin film covering the surface of the semiconductor element 1 and the substrate have different thermal expansion coefficients. Accordingly, when the temperature is varied to melt the ball electrodes in the process of mounting the semiconductor device onto the substrate, stresses are generated due to such a difference in thermal expansion coefficient. Accordingly, the Cu-Sn alloy layer formed in the portion of the metal wiring 4 to which the ball electrode 6 is mounted is likely to be broken by the stresses.

SUMMARY OF THE INVENTION

In view of the above problems, it is an object of the present invention to provide a semiconductor device having a metal wiring electrically connected to an electrode of a semiconductor element, and having improved junction reliability between the metal wiring and a ball electrode mounted on an external electrode portion of the metal wiring.

According to one aspect of the present invention, a semiconductor device includes a semiconductor element having an electrode formed on a surface thereof, and a metal wiring formed on the surface of the semiconductor element and electrically connected to the electrode. The metal wiring has an external electrode portion functioning as an

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external electrode. A thickness of the external electrode portion is greater than that of a non-electrode portion of the metal wiring, i.e., a portion of the metal wiring other than the external electrode portion.

According to the above semiconductor device, in the metal wiring electrically connected to the electrode of the semiconductor element, the thickness of the external electrode portion is greater than that of the non-electrode portion. The external electrode portion of the metal wiring and a wiring electrode of a substrate on which the semiconductor device is mounted may be connected to each other by a ball electrode formed from solder. In this case, when the metal wiring contain, e.g., Cu (which is a commonly used metal wiring material). Sn contained in solder of the ball electrode diffuses into Cu contained in the metal wiring, whereby a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion. However, since the thickness of the external electrode portion of the metal wiring is greater than that of the non-electrode portion of the metal wiring, this Sn-Cu alloy layer can be prevented from growing through the entire thickness of the external electrode portion. In other words, it is ensured that the thickness of the low-strength Sn-Cu alloy layer in the external electrode portion of the metal wiring is smaller than the thickness of the external electrode portion. Since a part of the external electrode portion is left unchanged into the Sn-Cu alloy layer, the strength of the metal wiring can be maintained even if Cu is used as a metal wiring material. The semiconductor element, the resin film covering the surface of the semiconductor element, and the substrate have different thermal expansion coefficients. Therefore, when the temperature is varied in the process of hardening the resin film covering the surface of the semiconductor element or the process of mounting the semiconductor device onto the substrate, stresses are generated due to such a difference in thermal expansion coefficient. However, the above structure can prevent disconnection

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of the metal wiring even if such stresses are generated.

According to the above semiconductor device, the thickness of the non-electrode portion of the metal wiring is smaller than that of the external electrode portion to which the ball electrode is mounted. The metal wiring having a small thickness facilitates formation of fine wirings by etching. As a result, the width of the metal wiring or the pitch of the metal wirings can be reduced, enabling reduction in size of the semiconductor device.

Preferably, the semiconductor device further includes an insulating film formed on the metal wiring and the surface of the semiconductor element, and having an opening exposing the external electrode portion. An exposed surface of the external electrode portion is preferably flush with or higher than a surface of the insulating film.

This prevents a wiring or electrode of a substrate on which the semiconductor device is mounted from contacting the non-electrode portion of the metal wiring of the semiconductor device. Moreover, the exposed surface of the external electrode portion is flush with or higher than the surface of the insulating film. Therefore, the ball electrode can be mounted to the external electrode portion without producing a gap therebetween. As a result, sufficient junction between the ball electrode and the external electrode portion can be ensured. When the exposed surface of the external electrode portion is higher than the surface of the insulating film, a substantial thickness of a metal portion of the external electrode portion is increased. Therefore, the following effects can be obtained: when Sn contained in solder of the ball electrode diffuses into Cu contained in the metal wiring, a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion. As described above, however, since the substantial thickness of the metal portion of the external electrode portion is increased, it is ensured that a greater part of the external electrode portion is left unchanged into the Sn-Cu alloy in the thickness

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direction of the external electrode portion. When the temperature is varied in a process such as the process of mounting the semiconductor device onto the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, the above structure can more reliably prevent disconnection of the metal wiring even if such stresses are generated. Note that, when the exposed surface of the external electrode portion is higher than the surface of the insulating film, the external electrode portion may be bonded to the wiring electrode of the substrate by solder without using the ball electrode. In this case, the same effects as those described above can be obtained.

Preferably, the metal wiring is formed from a metal containing copper.

This enables reduction in resistance of the metal wiring.

Preferably, the above semiconductor device further includes an insulating resin layer formed between the surface of the semiconductor element and the metal wiring.

The metal wiring is preferably formed along a surface of the insulating resin layer.

When the temperature is varied to melt the ball electrode in the process of mounting the semiconductor device to the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, these stresses can be absorbed by the insulating resin layer. As a result, the stresses are reduced, whereby the external electrode portion of the metal wiring to which the ball electrode is connected can be prevented from being broken by the stresses.

Preferably, the thickness of the external electrode portion is in a range of 10 μm to 20 μm .

In this case, the metal wiring can be reliably prevented from being disconnected at the external electrode portion, and pattern deformation generated in the process of forming the external electrode portion having a greater thickness by etching can be suppressed.

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According to another aspect of the present invention, a method for manufacturing a semiconductor device includes: a first step of forming, on a surface of a semiconductor element having an electrode formed thereon, a metal wiring electrically connected to the electrode; a second step of forming, on the surface of the semiconductor element and the metal wiring, an insulating film having an opening which exposes a region of the metal wiring layer where an external electrode is to be formed; and a third step of forming a metal-material embedded portion in the opening so that a surface of the metal-material embedded portion is flush with or higher than a surface of the insulating film.

According to the above manufacturing method, the metal wiring is formed so as to be electrically connected to the electrode of the semiconductor element. The insulating film is then formed so as to have an opening which exposes the region of the metal wiring where an external electrode is to be formed. Thereafter, the metal-material embedded portion is embedded in the opening so that the surface of the metal-material embedded portion is flush with or higher than the surface of the insulating film. As a result, the thickness of the external electrode portion (i.e., the total thickness of the metal-material embedded portion embedded in the opening and the metal wiring located under the metal-material embedded portion) is greater than the thickness of a non-electrode portion of the metal wiring, that is, the portion of the metal wiring other than the external electrode portion. Accordingly, the same effects as those of the semiconductor device of the present invention can be obtained.

According to the above manufacturing method, the non-electrode portion of the metal wiring (i.e., the portion of the metal wiring other than the external electrode portion) is covered with the insulating film. This prevents a wiring or electrode of a substrate on which the semiconductor device is mounted from contacting the non-electrode portion of the metal wiring of the semiconductor device. Moreover, the surface of the metal-

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material embedded portion, that is, the exposed surface of the external electrode portion, is flush with or higher than the surface of the insulating film. Therefore, a ball electrode can be mounted to the external electrode portion without producing a gap therebetween. As a result, sufficient junction between the ball electrode and the external electrode portion can be ensured. When the exposed surface of the external electrode portion is higher than the surface of the insulating film, a substantial thickness of a metal portion of the external electrode portion is increased. Therefore, the following effects can be obtained: when Sn contained in solder of the ball electrode diffuses into Cu contained in the metal wiring, a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion. As described above, however, since the substantial thickness of the metal portion of the external electrode portion is increased, it is ensured that a greater part of the external electrode portion is left unchanged into the Sn-Cu alloy in the thickness direction of the external electrode portion. When the temperature is varied in a process such as the process of mounting the semiconductor device onto the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, the above structure can more reliably prevent disconnection of the metal wiring even if such stresses are generated. Note that, when the exposed surface of the external electrode portion (i.e., the surface of the metalmaterial embedded portion) is higher than the surface of the insulating film, the external electrode portion may be bonded to the wiring electrode of the substrate by solder without using the ball electrode. In this case, the same effects as those described above can be obtained.

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Preferably, the above manufacturing method further includes, before the first step, the step of forming an insulating resin film on the surface of the semiconductor element except the electrode. The first step preferably includes the step of forming the metal

wiring along a surface of the insulating resin layer.

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When the temperature is varied to melt a ball electrode in the process of mounting the semiconductor device to the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. According to the above manufacturing method, however, these stresses can be absorbed by the insulating resin layer. As a result, the stresses are reduced, whereby the external electrode portion of the metal wiring to which the ball electrode is connected can be prevented from being broken by the stresses.

In the above manufacturing method, the third step may include the step of forming a metal film on the insulating film so as to completely fill the opening, forming a mask pattern which covers a region of the metal film located on the opening, removing a region of the metal film located outside the mask pattern, and removing the mask pattern.

In the above manufacturing method, the third step may include the step of forming a first metal film on the surface of the insulating film so as to partially fill the opening, forming a mask pattern which covers a region of the first metal film located outside the opening, forming a second metal film on a region of the first metal film located in the opening, and removing the mask pattern and the region of the first metal film located outside the opening.

In the above manufacturing method, the semiconductor element may be provided in each of a plurality of chip regions of a semiconductor wafer, which are defined by a dicing line. The method may further include, after the third step, the step of dicing the semiconductor wafer along the dicing line by a rotating blade in order to divide the semiconductor wafer into chips of the semiconductor elements.

According to still another aspect of the present invention, a method for manufacturing a semiconductor device includes: a first step of forming, on a surface of a

semiconductor element having an electrode formed thereon, a metal wiring electrically connected to the electrode; a second step of forming a projecting electrode on a region of the metal wiring where an external electrode is to be formed; and a third step of forming an insulating film on the surface of the semiconductor element and the metal wiring so as to expose at least a top portion of the projecting electrode.

According to the above manufacturing method, the metal wiring is formed so as to be electrically connected to the electrode of the semiconductor element. The projecting electrode is then formed on the region of the metal wiring where an external electrode is to be formed. Thereafter, the insulating film is formed so as to expose at least the top portion of the projecting electrode. As a result, the thickness of the external electrode portion (i.e., the total thickness of the projecting electrode and the metal wiring located thereunder) is greater than the thickness of a non-electrode portion of the metal wiring, that is, the portion of the metal wiring other than the external electrode portion. Accordingly, the same effects as those of the semiconductor device of the present invention can be obtained.

According to the above manufacturing method, the non-electrode portion of the metal wiring (i.e., the portion of the metal wiring other than the external electrode portion) is covered with the insulating film. This prevents a wiring or electrode of a substrate on which the semiconductor device is mounted from contacting the non-electrode portion of the metal wiring of the semiconductor device. Moreover, the surface of the top portion of the projecting electrode, that is, the exposed surface of the external electrode portion, is higher than the surface of the insulating film. Therefore, a ball electrode can be mounted to the external electrode portion without producing a gap therebetween. As a result, sufficient junction between the ball electrode and the external electrode portion can be ensured. Moreover, since the exposed surface of the external electrode portion is higher

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than the surface of the insulating film, a substantial thickness of a metal portion of the external electrode portion is increased. Therefore, the following effects can be obtained: when Sn contained in solder of the ball electrode diffuses into Cu contained in the metal wiring, a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion. As described above, however, since the substantial thickness of the metal portion of the external electrode portion is increased, it is ensured that a greater part of the external electrode portion is left unchanged into the Sn-Cu alloy in the thickness direction of the external electrode portion. When the temperature is varied in a process such as the process of mounting the semiconductor device onto the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, the above structure can more reliably prevent disconnection of the metal wiring even if such stresses are generated. Note that, when the exposed surface of the external electrode portion (i.e., the top portion of the projecting electrode) is higher than the surface of the insulating film, the external electrode portion may be bonded to the wiring electrode of the substrate by solder without using the ball electrode. In this case, the same effects as those described above can be obtained.

Preferably, the above manufacturing method further includes, before the first step, the step of forming an insulating resin film on the surface of the semiconductor element except the electrode. The first step preferably includes the step of forming the metal wiring along a surface of the insulating resin layer.

When the temperature is varied to melt a ball electrode in the process of mounting the semiconductor device to the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. According to the above manufacturing method, however, these stresses can be absorbed by the insulating resin layer. As a result, the stresses are reduced, whereby the external

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electrode portion of the metal wiring to which the ball electrode is connected can be prevented from being broken by the stresses.

In the above manufacturing method, the semiconductor element may be provided in each of a plurality of chip regions of a semiconductor wafer, which are defined by a dicing line. The above manufacturing method may further includes, after the third step, the step of dicing the semiconductor wafer along the dicing line by a rotating blade in order to divide the semiconductor wafer into chips of the semiconductor elements.

BRIEF DESCRIPTION OF THE DRAWINGS

- FIG. 1 is a cross-sectional view of a semiconductor device according to a first embodiment of the present invention;
 - FIG. 2 is a cross-sectional view of the semiconductor device according to the first embodiment of the present invention;
- FIG. 3 is a cross-sectional view of a semiconductor device according to a modification of the first embodiment of the present invention;
 - FIG. 4 is a cross-sectional view of a semiconductor device according to a second embodiment of the present invention;
 - FIG. 5 is a cross-sectional view of the semiconductor device according to the second embodiment of the present invention;
- FIG. 6 is a cross-sectional view of a semiconductor device according to a modification of the second embodiment of the present invention;
 - FIGs. 7A, 7B, 7C, 7D and 7E illustrate the steps of a method for manufacturing a semiconductor device according to a third embodiment of the present invention;
- FIGs. 8A and 8B illustrate the steps of the method for manufacturing a semiconductor device according to the third embodiment of the present invention;

FIGs. 9A, 9B, 9C and 9D illustrate the steps of a method for manufacturing a semiconductor device according to a fourth embodiment of the present invention;

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FIGs. 10A, 10B and 10C illustrate the steps of the method for manufacturing a semiconductor device according to the fourth embodiment of the present invention;

FIGs. 11A, 11B, 11C, 11D and 11E illustrate the steps of a method for manufacturing a semiconductor device according to a fifth embodiment of the present invention;

FIGs. 12A, 12B and 12C illustrate the steps of the method for manufacturing a semiconductor device according to the fifth embodiment of the present invention;

FIGs. 13A, 13B, 13C and 13D illustrate the steps of a method for manufacturing a semiconductor device according to a sixth embodiment of the present invention;

FIGs. 14A and 14B illustrate the steps of the method for manufacturing a semiconductor device according to the sixth embodiment of the present invention; and

FIG. 15A is a perspective plan view of a conventional semiconductor device, FIG. 15B shows an example of the cross-sectional structure taken along line XV-XV of FIG. 15A, and FIG. 15C shows another example of the cross-sectional structure taken along line XV-XV of FIG. 15A.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

20 (First Embodiment)

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Hereinaster, a semiconductor device according to the first embodiment of the present invention will be described with reference to the figures.

FIGs. 1 and 2 are cross-sectional views of the semiconductor device of the first embodiment.

As shown in FIG. 1, electrodes 12 are formed on the surface of a semiconductor

element 11. A passivation film 13 is formed over the surface of the semiconductor element 11. The passivation film 13 is formed from, e.g., SiN, and has an opening on each electrode 12. The passivation film 13 protects the surface of the semiconductor element 11. Metal wirings 14 containing, e.g., Cu are formed on the passivation film 13. Each metal wiring 14 is electrically connected to a corresponding one of the electrodes 12. An insulating film 15 is formed on the metal wirings 14 and the passivation film 13. The insulating film 15 has openings in order to expose a portion of each metal wiring 14 which functions as an external electrode (hereinafter, referred to as "external electrode portion 14a"). For example, the insulating film 15 is a resin film formed from solder resist or the like. As shown in FIG. 2, in order to electrically connect the electrodes 12 formed on the surface of the semiconductor element 11 to wiring electrodes of a substrate (not shown) on which the semiconductor element 11 is mounted, ball electrodes 16, which are formed from solder, are connected in a molten state to the openings of the insulating film 15, that is, the external electrode portions 14a of the metal wirings 14, respectively. electrodes 12 of the semiconductor element 11 and the wiring electrodes of the substrate are thus respectively connected to each other through the metal wirings 14 and the ball electrodes 16.

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The present embodiment is characterized in that the thickness (e.g., 14 µm) of the external electrode portion 14a of the metal wiring 14 is greater than that of the other portion of the metal wiring 14 (hereinafter, referred to as "non-electrode portion"). For example, such external electrode portions 14a having a greater thickness is formed by the following method: first, the insulating film 15 is formed. Openings are formed in the insulating film 15 at positions where the ball electrodes 16 are to be mounted on the Cucontaining metal wirings 14, respectively. Thereafter, the openings are filled with a metal material (more specifically, Cu). The external electrode portions 14a having a greater

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thickness are thus formed. In this case, the thickness of the external electrode portion 14a is equal to the total thickness of the metal wiring 14 and the portion filled with the metal material (hereinafter, referred to as "metal-material embedded portion").

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According to the first embodiment, in each metal wiring 14 electrically connected to a corresponding one of the electrodes 12, the thickness of the external electrode portion 14a is greater than that of the non-electrode portion. The external electrode portions 14a and the wiring electrodes of the substrate on which the semiconductor device is mounted are respectively connected to each other by the ball electrodes 16. When the metal wirings 14 contain, e.g., Cu (which is a commonly used metal wiring material), Sn contained in solder of the ball electrode 16 diffuses into Cu contained in the metal wiring 14, whereby a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion 14a. However, since the thickness of the external electrode portion 14a of the metal wiring 14 is greater than that of the non-electrode portion of the metal wiring 14, this Sn-Cu alloy layer can be prevented from growing through the entire thickness of the external electrode portion 14a. In other words, it is ensured that the thickness of the Sn-Cu alloy layer in the external electrode portion 14a is smaller than the thickness of the external electrode portion 14a. Since a part of the external electrode portion 14a is left unchanged into the Sn-Cu alloy layer, the strength of the metal wiring 14 can be maintained even if Cu is used as a metal wiring material. The semiconductor element 11, the resin film covering the surface of the semiconductor element 11, and the substrate have different thermal expansion coefficients. Therefore, when the temperature is varied in the process of hardening the resin film covering the surface of the semiconductor element 11 or the process of mounting the semiconductor device onto the substrate, stresses are generated due to such a difference in thermal expansion coefficient. Even if such stresses are generated, however, the above structure of the first embodiment

can prevent the Sn-Cu alloy layer having low strength from being broken and thus can prevent disconnection of the metal wirings 14.

More specifically, in the first embodiment, the thickness of the non-electrode portion of the metal wiring 14 is preferably in the range of 0.01 μ m to 8 μ m, and more preferably in the range of 0.01 μ m to 4 μ m. The reason for this is as follows: if the thickness of the metal wiring 14 is less than 0.01 μ m, the strength of the metal wiring 14 is reduced, causing disconnection and the like. If the thickness of the metal wiring 14 is greater than 8 μ m, it is difficult to etch the metal film for forming the metal wirings 14. This makes it difficult to reduce the size of the wiring pattern of the metal wirings 14.

In the first embodiment, the thickness of the external electrode portion 14a of the metal wiring 14 (e.g., the total thickness of the non-electrode portion of the metal wiring 14 and the metal-material embedded portion) is preferably in the range of 10 µm to 20 µm. The reason for this is as follows: the inventors fabricated a plurality of semiconductor device samples so that the external electrode portion 14a of each metal wiring 14 has a greater thickness than the non-electrode portion of the metal wiring 14. Such external electrode portions 14a were formed by forming the metal-material embedded portion in each opening of the insulating film 15 (i.e., on each region where an external electrode is to be formed; hereinafter, referred to as "external-electrode formation region"). In these semiconductor device samples, the thickness of the external electrode portion 14a was 5 um, 7 um, 9 um and 11 um, respectively. After each semiconductor device sample was mounted on a substrate, a temperature cycle test (environment reliability test) was conducted in order to determine whether or not each semiconductor device sample is capable of preventing disconnection of the metal wirings 14. In the temperature cycle test, each semiconductor device sample mounted on the substrate was repeatedly subjected to the temperatures of -40° C and 80° C. In this experimentation, 1,000 cycles were

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conducted in the temperature cycle test. In each cycle, the temperature was varied from -40°C to 80°C and then reduced back to -40°C. The following result was obtained by the temperature cycle test: when the thickness of the external electrode portion 14a (the total thickness of the metal wiring 14 and the metal-material embedded portion) is 5 µm, the metal wiring 14 was disconnected at 50 cycles. For 7 µm, the metal wiring 14 was disconnected at 200 cycles. For 9 µm, the metal wiring 14 was disconnected at 700 For 11 µm, the metal wiring 14 was not disconnected. cycles. The above experimentation result shows that the thicker the external electrode portion 14a is, the less the metal wiring 14 is likely to be disconnected. More specifically, the metal wiring 14 is less likely to be disconnected when the thickness of the external electrode portion 14a is about 10 µm or more. Note that the external electrode portion 14a having a greater thickness than the non-electrode portion of the metal wiring 14 is herein formed using the metal-material embedded portion. In this case, if the thickness of the external electrode portion 14a exceeds 20 µm, greater pattern deformation would be generated in the process of forming the metal-material filling portion by a wet etching method.

According to the first embodiment, the portion of the metal wiring 14 other than the external electrode portion 14a (i.e., the non-electrode portion of the metal wiring 14) is covered with the insulating film 15. This prevents wirings or electrodes of the substrate on which the semiconductor device is mounted from contacting the non-electrode portions of the metal wirings 14 of the semiconductor device. It is preferable that the exposed surface of the external electrode portion 14a is flush with or higher than the surface of the insulating film 15 (in the specification, the term "flush" also includes "approximately flush"). In other words, it is preferable that the thickness of the external electrode portion 14a is equal to or greater than that of the insulating film 15 (in the specification, the term "equal" also includes "approximately equal"). The reason for this is as follows: if the

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external electrode portion 14a is thinner than the insulating film 15, the ball electrode 16 cannot be mounted to the external electrode portion 14a (that is, the opening of the insulating film 15) without producing a gap therebetween. As a result, sufficient junction between the ball electrode 16 and the external electrode portion 14a cannot be ensured.

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Note that, in the first embodiment, the material of the metal wirings 14 is not specifically limited. For example, a material mainly containing Cu, titanium (Ti), tungsten (W), chromium (Cr), aluminum (Al) or the like may be used. Alternatively, another conductive metal material may be used. However, forming the metal wiring 14 from a Cu-containing metal enables reduction in resistance of the metal wiring 14.

(Modification of First Embodiment)

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Hereinafter, a semiconductor device according to a modification of the first embodiment will be described with reference to the figures.

FIG. 3 is a cross-sectional view of the semiconductor device according to the modification of the first embodiment. Note that, in the modification of the first embodiment, the same elements as those of the semiconductor device of the first embodiment in FIG. 1 are denoted with the same reference numerals and characters, and description thereof is omitted.

As shown in FIG. 3, electrodes 12 are formed on the surface of a semiconductor element 11. A passivation film 13 is formed over the surface of the semiconductor element 11. The passivation film 13 has an opening on each electrode 12. Metal wirings 14 are formed on the passivation film 13. Each metal wiring 14 is electrically connected to a corresponding one of the electrodes 12. An insulating film 15 is formed on the metal wirings 14 and the passivation film 13. The insulating film 15 has openings in order to expose a portion of each metal wiring 14 which functions as an external electrode (hereinafter, referred to as "external electrode portion 14b").

The modification of the first embodiment is different from the first embodiment in that each external electrode portion 14b has a mushroom-like projection over a corresponding one of the openings of the insulating film 15. The mushroom-like projection is larger than the opening of the insulating film 15. Therefore, the exposed surface of the external electrode portion 14b is higher than the surface of the insulating film 15. As a result, a substantial thickness of a metal portion of the external electrode portion 14b is larger than that of the external electrode portion 14a of the first embodiment in FIG. 1. Therefore, the following effects can be obtained: when the external electrode portions 14b and wiring electrodes of a substrate on which the semiconductor device is mounted are respectively connected to each other by ball electrodes formed from solder. Sn contained in solder of the ball electrode diffuses into Cu contained in the metal wiring 14. As a result, a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion 14b. As described above, however, the substantial thickness of the metal portion of the external electrode portion 14b is larger than that of the external electrode portion 14a of the first embodiment in FIG. 1. It is therefore ensured that a greater part of the external electrode portion 14b is left unchanged into the Sn-Cu alloy in the thickness direction of the external electrode portion 14b. temperature is varied in a process such as the process of mounting the semiconductor device onto the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, the above structure of the modification of the first embodiment can more reliably prevent disconnection of the metal wirings 14 even if such stresses are generated.

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Note that, in the modification of the first embodiment, the external electrode portions 14b may be bonded to the wiring electrodes of the substrate by solder without using the ball electrodes. In this case, the same effects as those described above can be

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(Second Embodiment)

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Hereinafter, a semiconductor device according to the second embodiment of the present invention will be described with reference to the figures.

FIGs. 4 and 5 are cross-sectional views of the semiconductor device of the second embodiment. Note that, in the second embodiment, the same elements as those of the semiconductor device of the first embodiment in FIG. 1 are denoted with the same reference numerals and characters, and description thereof is partly omitted.

As shown in FIG. 4, electrodes 12 are formed on the surface of a semiconductor element 11. A passivation film 13 is formed over the surface of the semiconductor element 11. The passivation film 13 has an opening on each electrode 12. An insulating resin layer 17 is formed on the passivation film 13 excluding the regions near the electrodes 12. For example, the insulating resin layer 17 is formed from an epoxy resin having low elasticity. Metal wirings 14 are formed along the surface of the insulating resin layer 17. Each metal wiring 14 is electrically connected to a corresponding one of the electrodes 12. An insulating film 15 is formed on the metal wirings 14, the insulating resin layer 17 and the passivation film 13. The insulating film 15 has openings in order to expose a portion of each metal wiring 14 which functions as an external electrode (hereinafter, referred to as "external electrode portion 14a"). For example, the insulating film 15 is a resin film formed from solder resist or the like. As shown in FIG. 5, in order to electrically connect the electrodes 12 formed on the surface of the semiconductor element 11 to wiring electrodes of a substrate (not shown) on which the semiconductor element 11 is mounted, ball electrodes 16, which are formed from solder, are connected in a molten state to the openings of the insulating film 15, that is, the external electrode portions 14a of the metal wirings 14, respectively. The electrodes 12 of the semiconductor element 11 and the wiring electrodes of the substrate are thus respectively connected to each other through the metal wirings 14 and the ball electrodes 16.

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A first characteristic of the second embodiment is that, like the first embodiment, the thickness of the external electrode portion 14a of the metal wiring 14 is greater than that of the other portion of the metal wiring 14 (i.e., the non-electrode portion).

A second characteristic of the second embodiment is that, as descried above, the insulating resin layer 17, which is formed from an epoxy resin having low elasticity or the like, is formed between the metal wirings 14 each electrically connected to a corresponding one of the electrodes 12 of the semiconductor element 11 and the passivation film 13 formed over the surface of the semiconductor element 11.

According to the second embodiment, the following effects can be obtained in addition to the effects of the first embodiment (which are obtained by the first characteristic): when the temperature is varied to melt the ball electrodes 16 in the process of mounting the semiconductor device to the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, these stresses can be absorbed by the insulating resin layer 17. As a result, the stresses are reduced, whereby the external electrode portion 14a of the metal wiring 14 to which the ball electrode 16 is connected can be prevented from being broken by the stresses.

According to the second embodiment, the portion of the metal wiring 14 other than the external electrode portion 14a (i.e., the non-electrode portion of the metal wiring 14) is covered with the insulating film 15. This prevents wirings or electrodes of the substrate on which the semiconductor device is mounted from contacting the non-electrode portions of the metal wirings 14 of the semiconductor device. It is preferable that the exposed surface of the external electrode portion 14a is flush with or higher than the surface of the

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electrode portion 14a is equal to or greater than that of the insulating film 15 on the insulating resin layer 17. The reason for this is as follows: if the external electrode portion 14a is thinner than the insulating film 15 on the insulating resin layer 17, the ball electrode 16 cannot be mounted to the external electrode portion 14a (that is, the opening of the insulating film 15) without a gap therebetween. As a result, sufficient junction between the ball electrode 16 and the external electrode portion 14a cannot be ensured.

Note that, in the second embodiment, the material of the metal wirings 14 is not specifically limited. For example, a material mainly containing Cu, Ti, W, Cr, Al or the like may be used. Alternatively, another conductive metal material may be used. However, forming the metal wiring 14 from a Cu-containing metal enables reduction in resistance of the metal wiring 14.

(Modification of Second Embodiment)

Hereinafter, a semiconductor device according to a modification of the second embodiment will be described with reference to the figures.

FIG. 6 is a cross-sectional view of the semiconductor device according to the modification of the second embodiment. Note that, in the modification of the second embodiment, the same elements as those of the semiconductor device of the first embodiment in FIG. 1 or the semiconductor device of the second embodiment in FIG. 4 are denoted with the same reference numerals and characters, and description thereof is partly omitted.

As shown in FIG. 6, electrodes 12 are formed on the surface of a semiconductor element 11. A passivation film 13 is formed over the surface of the semiconductor element 11. The passivation film 13 has an opening on each electrode 12. An insulating resin layer 17 is formed on the passivation film 13 excluding the regions near the

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electrodes 12. For example, the insulating resin layer 17 is formed from an epoxy resin having low elasticity. Metal wirings 14 are formed along the surface of the insulating resin layer 17. Each metal wiring 14 is electrically connected to a corresponding one of the electrodes 12. An insulating film 15 is formed on the metal wirings 14, the insulating resin layer 17 and the passivation film 13. The insulating film 15 has openings in order to expose a portion of each metal wiring 14 which functions as an external electrode (hereinafter, referred to as "external electrode portion 14b").

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The modification of the second embodiment is different from the second embodiment in that each external electrode portion 14b has a mushroom-like projection over a corresponding one of the openings of the insulating film 15. The mushroom-like projection is larger than the opening of the insulating film 15. Therefore, the exposed surface of the external electrode portion 14b is higher than the surface of the insulating film 15. As a result, a substantial thickness of a metal portion of the external electrode portion 14b is larger than that of the external electrode portion 14a of the second embodiment in FIG. 4. Therefore, the following effects can be obtained: when the external electrode portions 14b and wiring electrodes of a substrate on which the semiconductor device is mounted are respectively connected to each other by ball electrodes formed from solder, Sn contained in solder of the ball electrode diffuses into Cu contained in the metal wiring 14. As a result, a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion 14b. As described above, however, the substantial thickness of the metal portion of the external electrode portion 14b is larger than that of the external electrode portion 14a of the second embodiment in FIG. 4. It is therefore ensured that a greater part of the external electrode portion 14b is left unchanged into the Sn-Cu alloy in the thickness direction of the external electrode portion 14b. When the temperature is varied in a process such as the process of

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mounting the semiconductor device onto the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, the above structure of the modification of the second embodiment can more reliably prevent disconnection of the metal wirings 14 even if such stresses are generated.

Note that, in the modification of the second embodiment, the external electrode portions 14b may be bonded to the wiring electrodes of the substrate by solder without using the ball electrodes. In this case, the same effects as those described above can be obtained.

(Third Embodiment)

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Hereinaster, a method for manufacturing a semiconductor device according to the third embodiment of the present invention will be described with reference to the figures.

Note that the manufacturing method of the third embodiment is a method for manufacturing the semiconductor device of the first embodiment.

FIGs. 7A to 7E and FIGs. 8A, 8B illustrate the steps of the method for manufacturing a semiconductor device according to the third embodiment. FIGs. 7A and 8A are perspective views, and FIGs. 7B to 7E and FIG. 8B are cross-sectional views. In the third embodiment, the same elements as those of the semiconductor device of the first embodiment in FIGs. 1 and 2 are denoted with the same reference numerals and characters.

As shown in FIG. 7A, a semiconductor wafer 10 having a plurality of semiconductor elements 11 formed thereon is prepared. The semiconductor wafer 10 has a plurality of chip regions \mathbf{R}_{chip} defined by dicing lines 10a. Each semiconductor element 11 is provided in a corresponding one of the plurality of chip regions \mathbf{R}_{chip} of the semiconductor wafer 10. The following description will be given for the semiconductor element 11 provided in one of the plurality of chip regions \mathbf{R}_{chip} .

As shown in FIG. 7B, a passivation film 13 is formed over the surface of the semiconductor element 11 having electrodes 12 formed thereon. For example, the passivation film 13 is formed from SiN. The passivation film 13 has an opening on each electrode 12. Metal wirings 14 containing, e.g., Cu are then formed on the passivation film 13 so as to be electrically connected to the electrodes 12, respectively. More specifically, the metal wirings 14 are formed as follows: a titanium tungsten (TiW) layer and a Cu layer are sequentially formed on the passivation film 13 by a sputtering method. The TiW layer and the Cu layer are then etched by using a mask which covers the regions where the metal wirings are to be formed (hereinafter, referred to as metal-wiring formation regions). The mask is formed from a photoresist material. The metal wirings 14 having a desired pattern are thus formed. The resist mask is then removed.

As shown in FIG. 7C, an insulating film 15 is formed on the passivation film 13 and the metal wirings 14. Openings are then formed in the insulating film 15 so as to expose a predetermined region of each metal wiring 14 (a region where an external electrode is to be formed; hereinafter, referred to as "external-electrode formation region") by an etching method using a resist material (not shown). For example, the insulating film 15 is a resin film having a thickness of 12 µm, and is formed from solder resist or the like. In the present embodiment, the insulating film 15 is formed from a photosensitive material. Therefore, the opening pattern of the insulating film 15 is formed by using a photolithography method capable of forming a fine pattern.

As shown in FIG. 7D, a metal film 18 is formed on the insulating film 15 by, e.g., an electroplating method so as to completely fill the openings of the insulating film 15. For example, the metal film 18 is formed from Ti and Cu. A resist mask 19 is then formed so as to cover the regions of the metal film 18 on the openings of the insulating film 15.

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When the electroplating method is used in the step of FIG. 7D, wirings (not shown) formed in the dicing lines 10a of the semiconductor wafer 10 in FIG. 7A serve as a power feeding point of the electroplating method. These wirings are formed simultaneously with the metal wirings 14 by e.g., a sputtering method.

As shown in FIG. 7E, the portion of the metal film 18 located outside the resist mask 19 (i.e., the exposed portion of the metal film 18) is removed by, e.g., a wet etching method. As a result, metal-material embedded portions 18A are formed by the metal film 18 embedded in the openings of the insulating film 15. The resist mask 19 is then removed. Note that the surface of the metal-material embedded portions 18A is flush with or higher than the surface of the insulating film 15. As a result, the total thickness of the metal-material embedded portion 18A and the metal wiring 14 located thereunder is greater than the thickness of the portion of the metal wiring 14 other than the external electrode portion (i.e., the non-electrode portion of the metal wiring 14).

As shown in FIG. 8A, after the semiconductor elements 11 in the respective chip regions $\mathbf{R_{chip}}$ of the semiconductor wafer 10 are subjected to the steps of FIGs. 7B to 7E, the semiconductor wafer 10 is diced along the dicing lines 10a into individual chips by a rotating blade 20. In this step, the wirings serving as a power feeding point in the electroplating method in the step of FIG. 7D are also cut in order to discontinue current application through the wirings.

As shown in FIG. 8B, in order to electrically connect the electrodes 12 formed on the surface of the semiconductor element 11 to respective wiring electrodes of a substrate (not shown) on which the semiconductor element 11 is mounted, a ball electrode 16 is mounted on each metal-material embedded portion 18A (i.e., the external electrode portion of each metal wiring 14). For example, the ball electrodes 16 are formed from solder or Cu. The ball electrodes 16 may be formed from solder by printing solder paste to the

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metal-material embedded portions 18A by, e.g., a screen printing method and then reflowing the solder paste.

As has been described above, according to the third embodiment, the metal wirings 14 are formed so as to be electrically connected to the electrodes 12 of the semiconductor element 11, respectively. The insulating film 15 is then formed, and openings are formed in the insulating film 15 so as to expose the external-electrode formation regions of the metal wirings 14. Thereafter, the metal-material embedded portions 18A are embedded in the respective openings so that the surface of the metal-material embedded portions 18A is flush with or higher than the surface of the insulating film 15. Accordingly, the thickness of the external electrode portion of the metal wiring 14 (i.e., the total thickness of the metal-material embedded portion 18A embedded in the opening of the insulating film 15 and the metal wiring 14 located under the metal-material embedded portion 18A) is greater than the thickness of the portion of the metal wiring 14 other than the external electrode portion (i.e., the non-electrode portion of the metal wiring 14). As a result, the same effects as those of the semiconductor device of the first embodiment can be obtained. More specifically, the metal-material embedded portions 18A, that is, the external electrode portions, and the wiring electrodes of the substrate on which the semiconductor device is mounted are respectively connected to each other by the ball electrodes 16. When the metal wirings 14 contain, e.g., Cu (which is a commonly used metal wiring material), Sn contained in solder of the ball electrode 16 diffuses into Cu contained in the metal-material embedded portion 18A or the metal wiring 14, whereby a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion. However, since the thickness of the external electrode portion of the metal wiring 14 is greater than that of the non-electrode portion of the metal wiring 14, this Sn-Cu alloy layer can be prevented from growing through the entire thickness of the external electrode

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portion. In other words, it is ensured that the thickness of the Sn-Cu alloy layer in the external electrode portion is smaller than the thickness of the external electrode portion. Since a part of the external electrode portion is left unchanged into the Sn-Cu alloy layer, the strength of the metal wiring 14 can be maintained even if Cu is used as a metal wiring material. The semiconductor element 11, the resin film covering the surface of the semiconductor element 11, and the substrate have different thermal expansion coefficients. Therefore, when the temperature is varied in the process of hardening the resin film covering the surface of the semiconductor element 11 or the process of mounting the semiconductor device onto the substrate, stresses are generated due to such a difference in thermal expansion coefficient. Even if such stresses are generated, however, the above structure of the third embodiment can prevent the Sn-Cu alloy layer having low strength from being broken and thus can prevent disconnection of the metal wirings 14.

According to the third embodiment, the portion of the metal wiring 14 other than the external electrode portion (i.e., the non-electrode portion of the metal wiring 14) is covered with the insulating film 15. This prevents wirings or electrodes of the substrate on which the semiconductor device is mounted from contacting the non-electrode portions of the metal wirings 14 of the semiconductor device. The surface of the metal-material embedded portion 18A, that is, the exposed surface of the external electrode portion, is flush with or higher than the surface of the insulating film 15. In other words, the thickness of the external electrode portion (the total thickness of the metal-material embedded portion 18A and the metal wiring 14 located thereunder) is equal to or greater than that of the insulating film 15. Therefore, the following effects can be obtained: the ball electrode 16 can be mounted to the external electrode portion (the metal-material embedded portion 18A) without producing a gap therebetween. As a result, sufficient junction between the ball electrode 16 and the external electrode portion can be ensured.

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In the third embodiment, the exposed surface of the external electrode portion (the surface of the metal-material embedded portion 18A) may be higher than the surface of the insulating film. In this case, a substantial thickness of a metal portion of the external electrode portion is increased. Accordingly, the following effects can be obtained: when Sn contained in solder of the ball electrode 16 diffuses into Cu contained in the metalmaterial embedded portion 18A or the metal wiring 14, a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion. As described above, however, since the substantial thickness of the metal portion of the external electrode portion is increased, it is ensured that a greater part of the external electrode portion is left unchanged into the Sn-Cu alloy in the thickness direction of the external electrode portion. When the temperature is varied in a process such as the process of mounting the semiconductor device onto the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the However, the above structure of the third embodiment can more reliably prevent disconnection of the metal wirings 14 even if such stresses are generated. Note that, when the exposed surface of the external electrode portion (the surface of the metalmaterial embedded portion 18A) is higher than the surface of the insulating film 15, the external electrode portions may be bonded to the wiring electrodes of the substrate by solder without using the ball electrodes 16. In this case, the same effects as those described above can be obtained.

Note that, in the third embodiment, the material of the metal wirings 14 is not specifically limited. For example, a material mainly containing Cu, Ti, W, Cr, Al or the like may be used. Alternatively, another conductive metal material may be used. However, forming the metal wiring 14 from a Cu-containing metal enables reduction in resistance of the metal wiring 14.

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In the third embodiment, the TiW layer and the Cu layer for forming the metal wirings 14 are sequentially formed by a sputtering method. However, the TiW layer and the Cu layer may alternatively be formed by a plating method, a screen printing method or the like.

In the third embodiment, the insulating film 15 is formed from a photosensitive material, and the opening pattern of the insulating film 15 is formed by a photolithography method capable of forming a fine pattern. However, the insulating film 15 may alternatively be formed from a non-photosensitive material, and the opening pattern of the insulating film 15 may alternatively be formed by a screen printing method or the like.

In the third embodiment, the metal film 18, that is, the metal-material embedded portions 18A, are formed from Ti and Cu. However, the metal film 18, that is, the metal-material embedded portions 18A, may alternatively be formed from a material mainly containing TiW, Cr, nickel (Ni), gold (Au) or the like. If the metal film 18 is formed by an electroplating method, the metal film 18, that is, the metal-material embedded portions 18A, may be formed from a material mainly containing Au, silver (Ag), palladium (Pd), lead (Pb), Ni or the like.

In the third embodiment, the surface of the metal-material embedded portions 18A is flush with or higher than the surface of the insulating film 15. In other words, the thickness of the external electrode portion (i.e., the total thickness of the metal-material embedded portion 18A and the metal wiring 14 located thereunder) is equal to or greater than the thickness of the insulating film 15. More specifically, the thickness of the external electrode portion is preferably in the range of 10 μ m to 20 μ m. If the thickness of the external electrode portion exceeds 20 μ m, greater pattern deformation would be generated in the process of forming the metal-material embedded portions by a wet etching method.

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In the third embodiment, the metal film 18 is formed by an electroplating method. However, the metal film 18 may alternatively be formed by an electroless plating method, a screen printing method or the like.

In the third embodiment, it is preferable to form an insulating resin layer on the passivation film 13 excluding the regions near the electrodes 12 before the metal wirings 14 are formed, and to form the metal wirings 14 along the surface of the insulating resin layer. In this case, the following effects can be obtained: when the temperature is varied to melt the ball electrodes 16 in the process of mounting the semiconductor device to the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, these stresses can be absorbed by the insulating resin layer. As a result, the stresses are reduced, whereby the external electrode portion of the metal wiring 14 to which the ball electrode 16 is connected can be prevented from being broken by the stresses.

(Fourth Embodiment)

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Hereinafter, a method for manufacturing a semiconductor device according to the fourth embodiment of the present invention will be described with reference to the figures.

Note that the manufacturing method of the fourth embodiment is a method for manufacturing the semiconductor device of the modification of the second embodiment.

FIGs. 9A to 9D and FIGs. 10A to 10C illustrate the steps of the method for manufacturing a semiconductor device according to the fourth embodiment. FIGs. 9A and 10B are perspective views, and FIGs. 9B to 9D and FIGs. 10A, 10C are cross-sectional views. In the fourth embodiment, the same elements as those of the third embodiment in FIGs. 7A to 7E and FIGs. 8A, 8B are denoted with the same reference numerals and characters, and description thereof is partly omitted.

As shown in FIG. 9A, a semiconductor wafer 10 having a plurality of

semiconductor elements 11 formed thereon is prepared. The semiconductor wafer 10 has a plurality of chip regions R_{chip} defined by dicing lines 10a. Each semiconductor element 11 is provided in a corresponding one of the plurality of chip regions R_{chip} of the semiconductor wafer 10. The following description will be given for the semiconductor element 11 provided in one of the plurality of chip regions R_{chip} .

As shown in FIG. 9B, a passivation film 13 is formed over the surface of the semiconductor element 11 having electrodes 12 formed thereon. For example, the passivation film 13 is formed from SiN. The passivation film 13 has an opening on each electrode 12. An insulating resin layer 17 is then formed on the passivation film 13 excluding the regions near the electrodes 12. For example, the insulating resin layer 17 is formed from an epoxy resin having low elasticity. In the present embodiment, the low-elasticity resin material of the insulating resin layer 17 is a photosensitive material. The insulating resin layer 17 having a desired pattern is formed by patterning a film of the photosensitive material by a photolithography method.

As shown in FIG. 9C, metal wirings 14 are formed along the surface of the insulating resin layer 17 so as to be electrically connected to the electrodes 12, respectively. For example, the metal wirings 14 have a thickness of 5 μ m and are formed from Cu. More specifically, a Cu layer is formed on the insulating resin layer 17 by a sputtering method.

As shown in FIG. 9D, an insulating film 15 is formed on the passivation film 13, the insulating resin layer 17 and the metal wirings 14. Openings are then formed in the insulating film 15 so as to expose a predetermined region (external-electrode formation region) of each metal wiring 14. For example, the insulating film 15 is a resin film formed from solder resist or the like.

As shown in FIG. 10A, metal-material embedded portions 21 are formed in the

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openings of the insulating film 15 so as to be connected to the metal wirings 14, respectively. The thickness of the metal-material embedded portions 21 is greater than that of the insulating film 15. More specifically, the metal-material embedded portions 21 are formed from Cu, and formed by an electroless plating method. As a result, the top portions of the metal-material embedded portions 21 projecting from the surface of the insulating film 15 serve as projecting electrodes. The thickness of the external electrode portion (the total thickness of the metal-material embedded portion 21 and the metal wiring 14 located thereunder) is larger than that of the portion of the metal wiring 14 other than the external electrode portion (the non-electrode portion of the metal wiring 14).

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As shown in FIG. 10B, after the semiconductor elements 11 in the respective chip regions R_{chip} of the semiconductor wafer 10 are subjected to the steps of FIGs. 9B to 9D and FIG. 10A, the semiconductor wafer 10 is diced along the dicing lines 10a by a rotating blade 20. As a result, individual chips of the semiconductor elements 11 are obtained as shown in FIG. 10C.

As has been described above, according to the fourth embodiment, the following effects can be obtained in addition to the effects of the third embodiment: when the temperature is varied to melt the ball electrodes in the process of mounting the semiconductor device to the substrate (the ball electrodes are mounted to the external electrode portions of the metal wirings 14, and each external electrode portion is formed by the metal-material embedded portion 21 and the metal wiring 14 located thereunder), stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, these stresses can be absorbed by the insulating resin layer 17. As a result, the stresses are reduced, whereby the external electrode portion of the metal wiring 14 to which the ball electrode is connected can be prevented from being broken by the stresses.

According to the fourth embodiment, the portion of the metal wiring 14 other than the external electrode portion (i.e., the non-electrode portion of the metal wiring 14) is covered with the insulating film 15. This prevents wirings or electrodes of the substrate on which the semiconductor device is mounted from contacting the non-electrode portions of the metal wirings 14 of the semiconductor device. The surface of the metal-material embedded portion 21, that is, the exposed surface of the external electrode portion, is higher than the surface of the insulating film 15. In other words, the thickness of the external electrode portion is greater than that of the insulating film 15. Therefore, the following effects can be obtained: the ball electrode can be mounted to the external electrode portion (the metal-material embedded portion 21) without producing a gap therebetween. As a result, sufficient junction between the ball electrode and the external electrode portion can be ensured. Moreover, when Sn contained in solder of the ball electrode diffuses into Cu contained in the metal-material embedded portion 21 or the metal wiring 14, a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion. According to the above structure of the fourth embodiment, however, it is ensured that a greater part of the external electrode portion is left unchanged into the Sn-Cu alloy in the thickness direction of the external electrode portion. When the temperature is varied in a process such as the process of mounting the semiconductor device onto the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, the above structure of the fourth embodiment can more reliably prevent disconnection of the metal wirings 14 even if such stresses are generated. Note that, when the exposed surface of the external electrode portion (the surface of the metalmaterial embedded portion 21) is higher than the surface of the insulating film 15, the external electrode portions may be bonded to the wiring electrodes of the substrate by

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solder without using the ball electrodes. In this case, the same effects as those described above can be obtained.

Note that, in the fourth embodiment, the material of the metal wirings 14 is not specifically limited. For example, a material mainly containing Cu, Ti, W, Cr, Al or the like may be used. Alternatively, another conductive metal material may be used. However, forming the metal wiring 14 from a Cu-containing metal enables reduction in resistance of the metal wiring 14.

In the fourth embodiment, the Cu layer for forming the metal wirings 14 is formed by a sputtering method. However, the Cu layer may alternatively be formed by a plating method, a screen printing method or the like.

In the fourth embodiment, the metal-material embedded portions 21 are formed from Cu. However, another metal material (e.g., a metal material used in another embodiment) may alternatively be used.

In the fourth embodiment, the metal-material embedded portions 21 are formed by an electroless plating method. However, the metal-material embedded portions 21 may alternatively be formed by, e.g., an electroplating method.

In the fourth embodiment, the surface of the metal-material embedded portions 21 is higher than the surface of the insulating film 15. However, the surface of the metal-material embedded portions 21 may alternatively be flush with the surface of the insulating film 15. In this case, a semiconductor device having the same structure as that of the semiconductor device of the second embodiment is obtained. Note that the thickness of the external electrode portion (the total thickness of the metal-material embedded portion 21 and the metal wiring 14 located thereunder) is preferably in the range of 10 µm to 20 µm.

(Fifth Embodiment)

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Hereinafter, a method for manufacturing a semiconductor device according to the fifth embodiment of the present invention will be described with reference to the figures. Note that, like the third embodiment, the manufacturing method of the fifth embodiment is a method for manufacturing the semiconductor device of the first embodiment.

FIGs. 11A to 11E and FIGs. 12A to 12C illustrate the steps of the method for manufacturing a semiconductor device according to the fifth embodiment. FIGs. 11A and 12B are perspective views, and FIGs. 11B to 11E and FIGs. 12A, 12C are cross-sectional views. In the fifth embodiment, the same elements as those of the semiconductor device of the third embodiment in FIGs. 7A to 7E and FIGs. 8A, 8B are denoted with the same reference numerals and characters.

As shown in FIG. 11A, a semiconductor wafer 10 having a plurality of semiconductor elements 11 formed thereon is prepared. The semiconductor wafer 10 has a plurality of chip regions $\mathbf{R}_{\mathbf{chip}}$ defined by dicing lines 10a. Each semiconductor element 11 is provided in a corresponding one of the plurality of chip regions $\mathbf{R}_{\mathbf{chip}}$ of the semiconductor wafer 10. The following description will be given for the semiconductor element 11 provided in one of the plurality of chip regions $\mathbf{R}_{\mathbf{chip}}$.

As shown in FIG. 11B, a passivation film 13 is formed over the surface of the semiconductor element 11 having electrodes 12 formed thereon. For example, the passivation film 13 is formed from SiN. The passivation film 13 has an opening on each electrode 12. Metal wirings 14 containing, e.g., Cu are then formed on the passivation film 13 so as to be electrically connected to the electrodes 12, respectively. More specifically, the metal wirings 14 are formed as follows: a TiW layer and a Cu layer are sequentially formed on the passivation film 13 by a sputtering method. The TiW layer and the Cu layer are then etched by using a mask which covers the regions where the metal wirings are to be formed (i.e., the metal-wiring formation regions). The mask is formed

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from a photoresist material. The metal wirings 14 having a desired pattern are thus formed. The resist mask is then removed.

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As shown in FIG. 11C, an insulating film 15 is formed on the passivation film 13 and the metal wirings 14. Openings are then formed in the insulating film 15 so as to expose a predetermined region of each metal wiring 14 (a region where an external electrode is to be formed, i.e., an external-electrode formation region). For example, the insulating film 15 is a resin film having a thickness of 12 µm, and is formed from solder resist or the like. In the present embodiment, the insulating film 15 is formed from a photosensitive material. Therefore, the opening pattern of the insulating film 15 is formed by using a photolithography method capable of forming a fine pattern.

As shown in FIG. 11D, a first metal film 22 containing, e.g., Cu is formed on the insulating film 15 so that each opening of the insulating film 15 is partially filled with the first metal film 22. More specifically, the first metal film 22 is formed by sequentially forming a TiW layer and a Cu layer on the insulating film 15 by a sputtering method. Thereafter, a resist mask 23 is formed so as to cover the region of the insulating film 15 located outside the openings. In other words, the resist mask 23 is formed so as to expose the openings of the insulating film 15.

As shown in FIG. 11E, a second metal film 24 is formed on the exposed regions of the first metal film 22 by, e.g., an electroplating method so as to completely fill the openings of the insulating film 15. The exposed regions of the first metal film 22 are the regions of the first metal film 22 located within the openings of the insulating film 15 and surrounded by the resist mask 23. For example, the second metal film 24 is formed from Cu.

As shown in FIG. 12A, the resist mask 23 is removed, and the portion of the first metal film 22 located outside the openings of the insulating film 15 are removed by an

etching method. As a result, metal-material embedded portions 25 are formed by the first and second metal films 22, 24 embedded in the openings of the insulating film 15. Note that the surface of the metal-material embedded portions 25 is flush with or higher than the surface of the insulating film 15. In other words, the thickness of the external electrode portion (the total thickness of the metal-material embedded portion 25 and the metal wiring 14 located thereunder) is equal to or greater than that of the insulating film 15. As a result, the thickness of the external electrode portion is greater than the thickness of the portion of the metal wiring 14 other than the external electrode portion (i.e., the non-electrode portion of the metal wiring 14).

As shown in FIG. 12B, after the semiconductor elements 11 in the respective chip regions R_{chip} of the semiconductor wafer 10 are subjected to the steps of FIGs. 11B to 11E and FIG. 12A, the semiconductor wafer 10 is diced along the dicing lines 10a by a rotating blade 20. As a result, individual chips of the semiconductor elements 11 are obtained as shown in FIG. 12C.

As has been described above, according to the fifth embodiment, the metal wirings 14 are formed so as to be electrically connected to the electrodes 12 of the semiconductor element 11, respectively. The insulating film 15 is then formed, and openings are formed in the insulating film 15 so as to expose the external-electrode formation regions of the metal wirings 14. Thereafter, the metal-material embedded portions 25 are embedded in the respective openings so that the surface of the metal-material embedded portions 25 is flush with or higher than the surface of the insulating film 15. Accordingly, the thickness of the external electrode portion (i.e., the total thickness of the metal-material embedded portion 25 embedded in the opening of the insulating film 15 and the metal wiring 14 located under the metal-material embedded portion 25) is greater than the thickness of the portion of the metal wiring 14 other than the external electrode portion (i.e., the non-

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electrode portion of the metal wiring 14). As a result, the same effects as those of the manufacturing method of the third embodiment can be obtained.

According to the fifth embodiment, the portion of the metal wiring 14 other than the external electrode portion (i.e., the non-electrode portion of the metal wiring 14) is covered with the insulating film 15. This prevents wirings or electrodes of a substrate on which the semiconductor device is mounted from contacting the non-electrode portions of the metal wirings 14 of the semiconductor device. The surface of the metal-material embedded portion 25, that is, the exposed surface of the external electrode portion, is flush with or higher than the surface of the insulating film 15. In other words, the thickness of the external electrode portion (the total thickness of the metal-material embedded portion 25 and the metal wiring 14 located thereunder) is equal to or greater than that of the insulating film 15. Therefore, the following effects can be obtained: a ball electrode can be mounted to the external electrode portion (the metal-material embedded portion 25) without producing a gap therebetween. As a result, sufficient junction between the ball electrode and the external electrode portion can be ensured.

In the fifth embodiment, the exposed surface of the external electrode portion (the surface of the metal-material embedded portion 25) may be higher than the surface of the insulating film. In this case, a substantial thickness of a metal portion of the external electrode portion is increased. Accordingly, the following effects can be obtained: when Sn contained in solder of the ball electrode diffuses into Cu contained in the metal-material embedded portion 25 or the metal wiring 14, a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion. As described above, however, since the substantial thickness of the metal portion of the external electrode portion is increased, it is ensured that a greater part of the external electrode portion is left unchanged into the Sn-Cu alloy in the thickness direction of the external electrode portion.

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When the temperature is varied in a process such as the process of mounting the semiconductor device onto the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, the above structure of the fifth embodiment can more reliably prevent disconnection of the metal wirings 14 even if such stresses are generated. Note that, when the exposed surface of the external electrode portion (the surface of the metalmaterial embedded portion 25) is higher than the surface of the insulating film 15, the external electrode portions may be bonded to the wiring electrodes of the substrate by solder without using the ball electrodes. In this case, the same effects as those described above can be obtained.

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Note that, in the fifth embodiment, the material of the metal wirings 14 is not specifically limited. For example, a material mainly containing Cu, Ti, W, Cr, Al or the like may be used. Alternatively, another conductive metal material may be used. However, forming the metal wiring 14 from a Cu-containing metal enables reduction in resistance of the metal wiring 14.

In the fifth embodiment, the TiW layer and the Cu layer for forming the metal wirings 14 are sequentially formed by a sputtering method. However, the TiW layer and the Cu layer may alternatively be formed by a plating method, a screen printing method or the like.

In the fifth embodiment, the insulating film 15 is formed from a photosensitive material, and the opening pattern of the insulating film 15 is formed by a photolithography method capable of forming a fine pattern. However, the insulating film 15 may alternatively be formed from a non-photosensitive material, and the opening pattern of the insulating film 15 may alternatively be formed by a screen printing method or the like.

In the fifth embodiment, the material of the first metal film 22 is not specifically

limited. For example, a material mainly containing Cu, Ti, W, Cr, Al or the like may be used. Alternatively, another conductive metal material may be used.

In the fifth embodiment, the TiW layer and the Cu layer for forming the first metal film 22 are sequentially formed by a sputtering method. However, the TiW layer and the Cu layer may alternatively be formed by a plating method, a screen printing method or the like.

In the fifth embodiment, the second metal film 24 is formed from Cu. However, the second metal film 24 may alternatively be formed from a material mainly containing Ni, Ag, Au, Sn, Pd or the like.

In the fifth embodiment, the metal-material embedded portion 25 having its top portion larger than the opening of the insulating film 15 may be formed by a screen printing method or the like so that the top portion of the metal-material embedded portion 25 projecting from the surface of the insulating film 15 serves as a mushroom-like projecting electrode. In this case, a semiconductor device having the same structure as that of the semiconductor device of the modification of the first embodiment is formed. In the fifth embodiment, the second metal film 24 is formed by an electroplating method. However, the second metal film 24 may alternatively be formed by an electroless plating method, a screen printing method or the like.

In the fifth embodiment, the surface of the metal-material embedded portions 25 is flush with or higher than the surface of the insulating film 15. In other words, the thickness of the external electrode portion (i.e., the total thickness of the metal-material embedded portion 25 and the metal wiring 14 located thereunder) is equal to or greater than the thickness of the insulating film 15. More specifically, the thickness of the external electrode portion is preferably in the range of 10 µm to 20 µm. If the thickness of the external electrode portion exceeds 20 µm, it is difficult to form the resist mask 23

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having a sufficient thickness (see FIG. 11D) near the openings (i.e., stepped portions) of the insulating film 15.

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In the fifth embodiment, it is preferable to form an insulating resin layer on the passivation film 13 excluding the regions near the electrodes 12 before the metal wirings 14 are formed, and to form the metal wirings 14 along the surface of the insulating resin layer. In this case, the following effects can be obtained: when the temperature is varied to melt the ball electrodes in the process of mounting the semiconductor device to the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, these stresses can be absorbed by the insulating resin layer. As a result, the stresses are reduced, whereby the external electrode portion of the metal wiring 14 to which the ball electrode is connected can be prevented from being broken by the stresses.

(Sixth Embodiment)

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Hereinafter, a method for manufacturing a semiconductor device according to the sixth embodiment of the present invention will be described with reference to the figures.

FIGs. 13A to 13D and FIGs. 14A, 14B illustrate the steps of the method for manufacturing a semiconductor device according to the sixth embodiment. FIGs. 13A and 14A are perspective views, and FIGs. 13B to 13D and FIG. 14B are cross-sectional views. In the sixth embodiment, the same elements as those of the third embodiment in FIGs. 7A to 7E and FIGs. 8A, 8B are denoted with the same reference numerals and characters.

As shown in FIG. 13A, a semiconductor wafer 10 having a plurality of semiconductor elements 11 formed thereon is prepared. The semiconductor wafer 10 has a plurality of chip regions R_{chip} defined by dicing lines 10a. Each semiconductor element 11 is provided in a corresponding one of the plurality of chip regions R_{chip} of the

semiconductor wafer 10. The following description will be given for the semiconductor element 11 provided in one of the plurality of chip regions R_{chip} .

As shown in FIG. 13B, a passivation film 13 is formed over the surface of the semiconductor element 11 having electrodes 12 formed thereon. For example, the passivation film 13 is formed from SiN. The passivation film 13 has an opening on each electrode 12. Metal wirings 14 containing, e.g., Cu are then formed on the passivation film 13 so as to be electrically connected to the electrodes 12, respectively. More specifically, the metal wirings 14 are formed as follows: a TiW layer and a Cu layer are sequentially formed on the passivation film 13 by a sputtering method. The TiW layer and the Cu layer are then etched by using a mask which covers the regions where the metal wirings are to be formed (i.e., the metal-wiring formation regions). The mask is formed from a photoresist material. The metal wirings 14 having a desired pattern are thus formed. The resist mask is then removed.

As shown in FIG. 13C, projecting electrodes 26 having a thickness of about 20 µm are formed as follows: conductive resin paste is applied with a desired pattern to a predetermined region of each metal wiring 14 (a region where an external electrode is to be formed, i.e., an external-electrode formation region) by a screen printing method or the like. For example, powdered Ag added to a thermosetting epoxy resin is used as the resin paste.

As shown in FIG. 13D, an insulating film 15 having a thickness of about 15 µm is formed on the passivation film 13 and the metal wirings 14 (i.e., over the surface of the semiconductor wafer 10). As a result, the top portions of the projecting electrodes 26 are exposed from the surface of the insulating film 15. For example, the insulating film 15 is a resin film formed from solder resist or the like, and is formed by a spin coating method or the like.

Note that, in the present embodiment, the top portions of the projecting electrodes

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26 may be cleaned by etching the surface of the semiconductor wafer 10 by a dry etching method using oxygen gas after the insulating film 15 is formed. This improves conductivity between the projecting electrodes 26 of the semiconductor device and the wiring electrodes of a substrate on which the semiconductor device is mounted.

As shown in FIG. 14A, after the semiconductor elements 11 in the respective chip regions $\hat{\mathbf{R}}_{chip}$ of the semiconductor wafer 10 are subjected to the steps of FIGs. 13B to 13D, the semiconductor wafer 10 is diced along the dicing lines 10a by a rotating blade 20. As a result, individual chips of the semiconductor elements 11 are obtained as shown in FIG. 14B.

As has been described above, according to the sixth embodiment, the metal wirings 14 are formed so as to be electrically connected to the electrodes 12 of the semiconductor element 11, respectively. Thereafter, the projecting electrodes 26 are respectively formed on the external-electrode formation regions of the metal wirings 14, and the insulating film 15 is then formed so as to expose the top portions of the projecting electrodes 26. Accordingly, the thickness of the external electrode portion (i.e., the total thickness of the projecting electrode 26 and the metal wiring 14 located thereunder) is greater than the thickness of the portion of the metal wiring 14 other than the external electrode portion (i.e., the non-electrode portion of the metal wiring 14). As a result, the same effects as those of the semiconductor device of the third embodiment can be obtained.

According to the sixth embodiment, the portion of the metal wiring 14 other than the external electrode portion (i.e., the non-electrode portion of the metal wiring 14) is covered with the insulating film 15. This prevents wirings or electrodes of the substrate on which the semiconductor device is mounted from contacting the non-electrode portions of the metal wirings 14 of the semiconductor device. The surface of the projecting electrode 26, that is, the exposed surface of the external electrode portion, is higher than

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the surface of the insulating film 15. In other words, the thickness of the external electrode portion is greater than that of the insulating film 15. Therefore, the following effects can be obtained: a ball electrode can be mounted to the external electrode portion (the projecting electrode 26) without producing a gap therebetween. As a result, sufficient junction between the ball electrode and the external electrode portion can be ensured. Moreover, when Sn contained in solder of the ball electrode diffuses into Cu contained in the projecting electrode 26 or the metal wiring 14, a Sn-Cu alloy layer having low strength grows in the thickness direction of the external electrode portion. According to the above structure of the sixth embodiment, however, it is ensured that a greater part of the external electrode portion is left unchanged into the Sn-Cu alloy in the thickness direction of the external electrode portion. When the temperature is varied in a process such as the process of mounting the semiconductor device onto the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, the above structure of the sixth embodiment can more reliably prevent disconnection of the metal wirings 14 even if such stresses are generated. Note that, when the exposed surface of the external electrode portion (the surface of the projecting electrode 26) is higher than the surface of the insulating film 15, the external electrode portions may be bonded to the wiring electrodes of the substrate by solder without using the ball electrodes. In this case, the same effects as those described above can be obtained.

Note that, in the sixth embodiment, the material of the metal wirings 14 is not specifically limited. For example, a material mainly containing Cu, Ti, W, Cr, Al or the like may be used. Alternatively, another conductive metal material may be used. However, forming the metal wiring 14 from a Cu-containing metal enables reduction in resistance of the metal wiring 14.

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In the sixth embodiment, the TiW layer and the Cu layer for forming the metal wirings 14 are sequentially formed by a sputtering method. However, the TiW layer and the Cu layer may alternatively be formed by a plating method, a screen printing method or the like.

In the sixth embodiment, a conductive component of the resin paste for forming the projecting electrodes 26 is not specifically limited. For example, Ni, Cu, Au, Ag, Sn, Pd or the like may be used as the conductive component.

In the sixth embodiment, the insulating film 15 is formed by a spin coating method.

However, the insulating film 15 may alternatively be formed by a curtain coating method.

In the sixth embodiment, it is preferable to form an insulating resin layer on the passivation film 13 excluding the regions near the electrodes 12 before the metal wirings 14 are formed, and to form the metal wirings 14 along the surface of the insulating resin layer. In this case, the following effects can be obtained: when the temperature is varied to melt the ball electrodes in the process of mounting the semiconductor device to the substrate, stresses are generated due to the difference in thermal expansion coefficient between the semiconductor device and the substrate. However, these stresses can be absorbed by the insulating resin layer. As a result, the stresses are reduced, whereby the external electrode portion of the metal wiring 14 to which the ball electrode is connected can be prevented from being broken by the stresses.

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WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor element having an electrode formed on a surface thereof; and

a metal wiring formed on the surface of the semiconductor element and electrically connected to the electrode, wherein

the metal wiring has an external electrode portion functioning as an external electrode, and

a thickness of the external electrode portion is greater than that of a non-electrode portion of the metal wiring, i.e., a portion of the metal wiring other than the external electrode portion.

2. The semiconductor device according to claim 1, further comprising:

an insulating film formed on the metal wiring and the surface of the semiconductor element, and having an opening exposing the external electrode portion, and

an exposed surface of the external electrode portion is flush with or higher than a surface of the insulating film.

- 3. The semiconductor device according to claim 1, wherein the metal wiring is formed from a metal containing copper.
 - 4. The semiconductor device according to claim 1, further comprising:

an insulating resin layer formed between the surface of the semiconductor element and the metal wiring, and

the metal wiring is formed along a surface of the insulating resin layer.

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- 5. The semiconductor device according to claim 1, wherein the thickness of the external electrode portion is in a range of 10 μm to 20 μm .
 - 6. A method for manufacturing a semiconductor device, comprising:

a first step of forming, on a surface of a semiconductor element having an electrode formed thereon, a metal wiring electrically connected to the electrode;

a second step of forming, on the surface of the semiconductor element and the metal wiring, an insulating film having an opening which exposes a region of the metal wiring layer where an external electrode is to be formed; and

a third step of forming a metal-material embedded portion in the opening so that a surface of the metal-material embedded portion is flush with or higher than a surface of the insulating film.

7. The method according to claim 6, further comprising before the first step the step

forming an insulating resin film on the surface of the semiconductor element except the electrode, wherein

the first step includes the step of forming the metal wiring along a surface of the insulating resin layer.

8. The method according to claim 6, wherein the third step includes the step of forming a metal film on the insulating film so as to completely fill the opening, forming a mask pattern which covers a region of the metal film located on the opening, removing a region of the metal film located outside the mask pattern, and removing the mask pattern.

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of:

9. The method according to claim 6, wherein the third step includes the step of forming a first metal film on the surface of the insulating film so as to partially fill the opening, forming a mask pattern which covers a region of the first metal film located outside the opening, forming a second metal film on a region of the first metal film located in the opening, and removing the mask pattern and the region of the first metal film located outside the opening.

10. The method according to claim 6, wherein

the semiconductor element is provided in each of a plurality of chip regions of a semiconductor wafer, which are defined by a dicing line,

the method further comprising after the third step the step of:

dicing the semiconductor wafer along the dicing line by a rotating blade in order to divide the semiconductor wafer into chips of the semiconductor elements.

11. A method for manufacturing a semiconductor device, comprising:

a first step of forming, on a surface of a semiconductor element having an electrode formed thereon, a metal wiring electrically connected to the electrode;

a second step of forming a projecting electrode on a region of the metal wiring where an external electrode is to be formed; and

a third step of forming an insulating film on the surface of the semiconductor element and the metal wiring so as to expose at least a top portion of the projecting electrode.

12. The method according to claim 11, further comprising before the first step the step of:

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forming an insulating resin film on the surface of the semiconductor element except the electrode, wherein

the first step includes the step of forming the metal wiring along a surface of the insulating resin layer.

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13. The method according to claim 11, wherein

the semiconductor element is provided in each of a plurality of chip regions of a semiconductor wafer, which are defined by a dicing line,

the method further comprising after the third step the step of:

dicing the semiconductor wafer along the dicing line by a rotating blade in order to divide the semiconductor wafer into chips of the semiconductor elements.

ABSTRACT OF THE DISCLOSURE

The semiconductor device includes a semiconductor element having an electrode formed on a surface thereof, and a metal wiring formed on the surface of the semiconductor element and electrically connected to the electrode. The metal wiring has an external electrode portion functioning as an external electrode. A thickness of the external electrode portion is greater than that of a non-electrode portion of the metal wiring, i.e., a portion of the metal wiring other than the external electrode portion.

FIG. 1

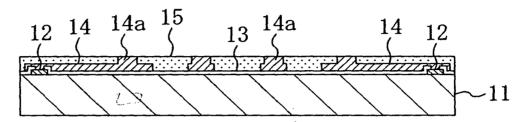


FIG. 2

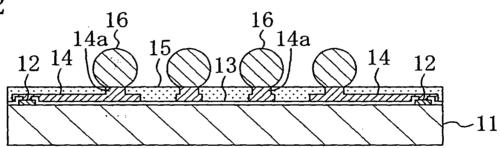


FIG. 3

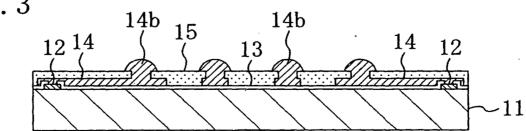


FIG. 4

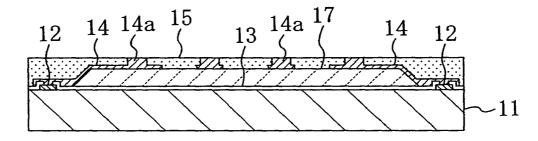


FIG. 5

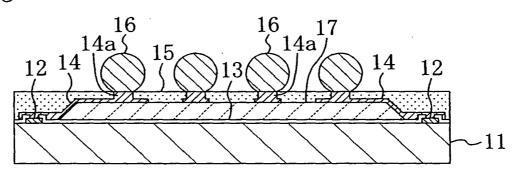
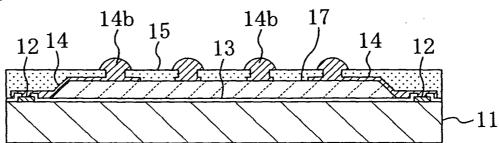


FIG. 6



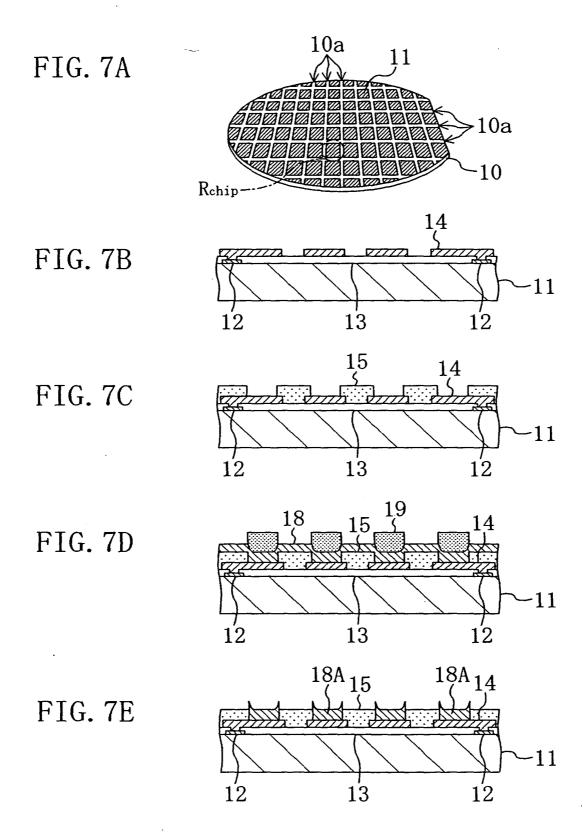


FIG. 8A

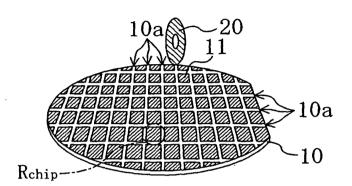


FIG. 8B

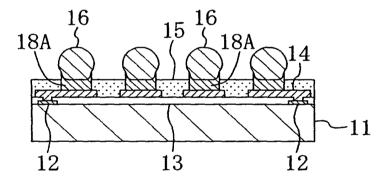


FIG. 9A

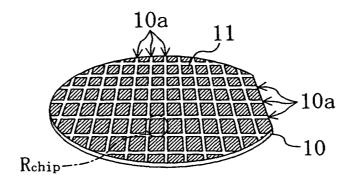


FIG. 9B

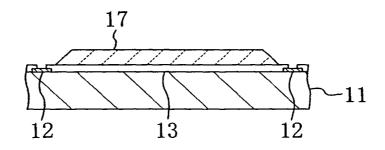


FIG. 9C

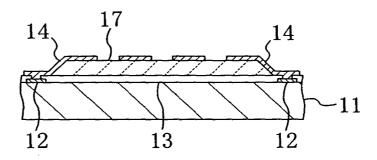


FIG. 9D

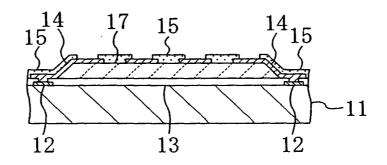


FIG. 10A

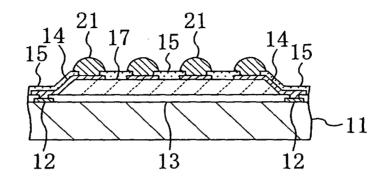


FIG. 10B

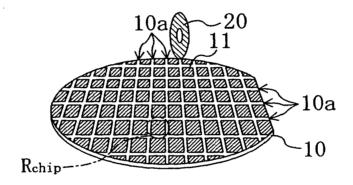
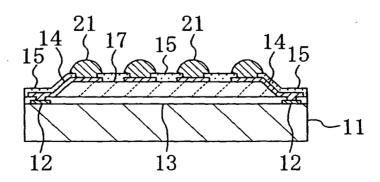


FIG. 10C



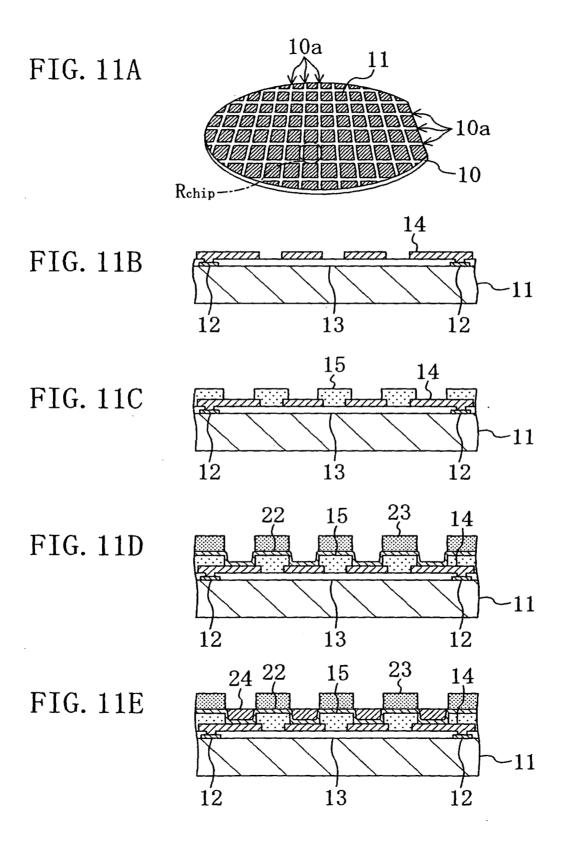


FIG. 12A

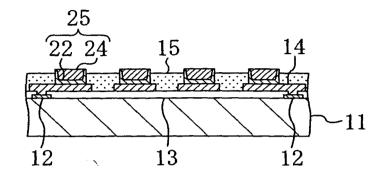


FIG. 12B

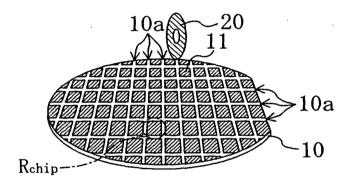


FIG. 12C

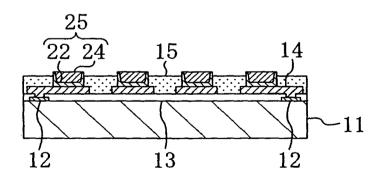


FIG. 13A

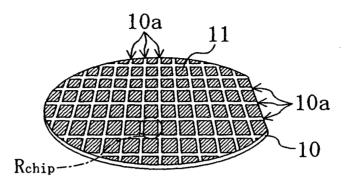


FIG. 13B

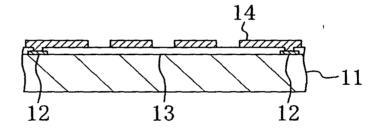


FIG. 13C

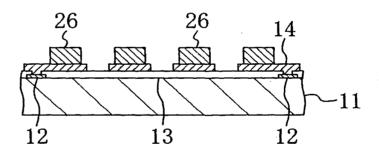


FIG. 13D

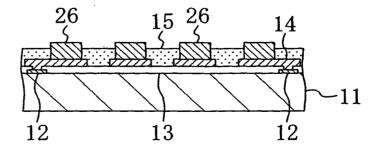


FIG. 14A

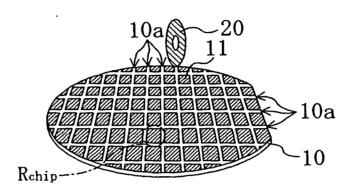


FIG. 14B

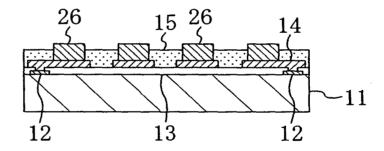


FIG. 15A Prior Art

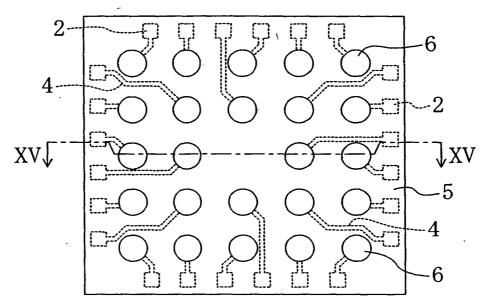


FIG. 15B Prior Art

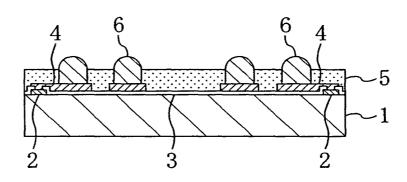
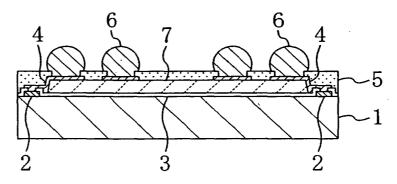


FIG. 15C Prior Art



Docket No.: 740819-924 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yoshifumi NAKAMURA, Ryuichi SAHARA, Nozomi SHIMOISHIZAKA, Kazuyuki KAINOU, Keiji MIKI, Kazumi WATASE, Yasutake YAGUCHI

Serial No.:

10/307,450

Filed:

December 2, 2002

For. SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

REVOCATION OF POWER OF ATTORNEY, APPOINTMENT AND CERTIFICATION UNDER 37 CFR 3.73(B)

Commissioner for Patents Washington, DC 20231

Sir:

The undersigned assignee of the above-identified application hereby revokes all previous Powers of Attorney and appoints the following attorneys with full power to prosecute the application, to make alterations and amendments therein, and to transact all business in the United States Patent Office connected therewith.

I hereby appoint the following attorney(s) and/or agent(s): Steven W. Allis, Reg. No. 50,532; Stephen A. Becker, Reg. No. 26,527; John G. Bisbikis, Reg. No. 37,095; Daniel Bucca, Reg. No. 42,368; Kenneth L. Cage, Reg. No. 26,151; Jennifer Chen, Reg. No. 42,404; Bernard P. Codd, Reg. No. 46,429; Lawrence T. Cullen, Reg. No. 44,489; Paul Devinsky, Reg. No. 28,553; Margaret M. Duncan, Reg. No. 30,879; Shamita De. Etienne-Cummings, Reg. No. 46,072; Ramyar M. Farid, Reg. No. 46,692; Brian E. Ferguson, Reg. No. 36,801; Michael E. Fogarty, Reg. No. 36,139; John R. Fuisz, Reg. No. 37,327; Willem F. Gadiano, Reg. No. 37,136; Keith E. George, Reg. No. 34,111; John A. Hankins, Reg. No. 32,029; Eric J. Kraus, Reg. No. 36,190; Catherine Krupka, Reg. No. 46,227; Jack Q. Lever, Reg. No. 28,149; Raphael V. Lupo, Reg. No. 28,363; Burman Y. Mathis III, Reg. No. 44,907; Michael A. Messina, Reg. No. 33,424; Dawn L. Palmer, Reg. No. 41,238; Joseph H. Paquin, Jr., Reg. No. 31,647; Scott D. Paul, Reg. No. 42,984; William D. Pegg, Reg. No. 42,988; Robert L. Price, Reg. No. 22,685; Gene Z. Rubinson, Reg. No. 33,351; Brian K. Seidleck, Reg. No. 51,321; Joy Ann G. Serauskas, Reg. No. 27,952; Jiri F. Smetana, Reg. No. 52,456; David A. Spenard, Reg. No. 37,449; Arthur J. Steiner, Reg. No. 26,106; Wesley Strickland, Reg. No. 44,363;

Serial No.:

10/307,450

Michael D. Switzer, Reg. No. 39,552; David M. Tennant, Reg. No. 48,362; Judith L. Toffenetti, Reg. No. 39,048; Daniel S. Trainor, Reg. No. 43,959; Shival P. Virmani, Reg. No. 45,032; Kelli N. Watson, Reg. No. 47,170; Cameron K. Weiffenbach, Reg. No. 44,488; Aaron Weisstuch, Reg. No. 41,557; Edward J. Wise, Reg. No. 34,523; Jeffrey A. Woller, Reg. No. 48,041; Alexander V. Yampolsky, Reg. No. 36,324; Robert W. Zelnick, Reg. No. 36,976; and Wei-Chen Chen, admitted under 37 CFR 10.9(b) all of

McDERMOTT, WILL & EMERY 600 13th Street, N.W. Washington, DC 20005-3096

with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and all future correspondence should be addressed to them.

CERTIFICATE UNDER 37 CFR 3.73(b)

MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD., a corporation of 1006, Oaza Kadoma, Kadoma-shi, Osaka 571-8501, Japan, certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of:

An Assignment from the inventor(s) of the patent application identified above. A copy of the executed assignment is attached herewith.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

The undersigned further declares that all statements made herein of its own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States

WDC99 725640-1,060188,0011

Serial No.:

10/307,450

Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully submitted,

MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD.

Name:

Isamu SHIMURA

Title:

Director, IP Development Center

Authorized Signing Officer

Signature:

Date:

04.17.2003

-1-

DECLARATION AND POWER OF ATTORNEY	
FOR PATENT APPLICATION	

Attorney Docket No.	
---------------------	--

, the specification of which is attached hereto unless the following box is check [] The specification was filed on	below) or a joint SEMICONDUCT	e; that I verily be	hereby declare that: my lieve that I am the origin plural inventors an AND MANUFACTURE	nal, first and sol	e inventor (if on	ly one nan	e is listed
and was assigned Serial No. and was amended on		, the	specification of which i	s attached hereto	unless the follow	wing box is	checked:
I hereby state that I have reviewed and understand the contents of the above-identified specification, include the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application accordance with Title 37, Code of Federal Regulations, § 1.56. I do not know and do not believe the same was ever known or used in the United States of America before or our invention thereof, or patented or described in any printed publication in any country before my or our inventhereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made subject of an inventor's certificate issued before the date of this application in any country foreign to the United St of America on an application filed by me or my legal representatives or assigns more than twelve months prior to application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, example to the United States of America prior to this application by me or my legal representatives or assigns, example the distribution of the United States of America prior to this application by me or my legal representatives or assigns, example the United States of America prior to this application by me or my legal representatives or assigns, example the United States of America prior to this application by me or my legal representatives or assigns, example the United States of America prior to this application by me or my legal representatives or assigns, example the United States of America prior to this application by me or my legal representatives or assigns are the United States of America prior to this application by me or my legal representatives or assigns are the U	[]	and was assign	ed Serial No.	(if known)			
I do not know and do not believe the same was ever known or used in the United States of America before or our invention thereof, or patented or described in any printed publication in any country before my or our inventhereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made subject of an inventor's certificate issued before the date of this application in any country foreign to the United St of America on an application filed by me or my legal representatives or assigns more than twelve months prior to application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, excas follows: I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any for application(s) for patent or inventor's certificate listed below and checked at right: Priority Claimed Yes No	-			`	ove-identified sp	ecification	including
or our invention thereof, or patented or described in any printed publication in any country before my or our inventhereof, or more than one year prior to this application, that the same was not in public use or on sale in the Un States of America more than one year prior to this application, that the invention has not been patented or made subject of an inventor's certificate issued before the date of this application in any country foreign to the United St of America on an application filed by me or my legal representatives or assigns more than twelve months prior to application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, excas follows: I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any for application(s) for patent or inventor's certificate listed below and checked at right: Priority Claimed Yes No Priority Claimed Yes No	_	•		is material to the	he examination of	of this app	lication in
(Number) (Country) (Month/Day/Year Filed)	or our invention thereof thereof, or more than of States of America more subject of an inventor's of America on an apple application, and that no foreign to the United S	of, or patented or one year prior to the than one year prior to see than one year prior to the than one year.	described in any printed this application, that the prior to this application, d before the date of this are or my legal representa patent or inventor's cert prior to this application	publication in an e same was not that the invention application in an tives or assigns dificate on this in	ny country before in public use or on has not been y y country foreign more than twelve evention has been regal representative	e my or our on sale in patented or to the Un e months p in filed in a	r invention the United r made the ited States rior to this ny country
2001-387051 JAPAN 12/20/2001 X						119 of a	ny foreign
	application(s) for pater	nt or inventor's ce ation(s)	ertificate listed below and	d checked at righ		Priority	Claimed
All foreign applications, if any, for any Patent or Inventor's Certificate filed more than 12 months prior to filing date of this application:	Prior Foreign Application(s)	ation(s)	ertificate listed below and	d checked at righ		Priority Yes	Claimed
Country Application No. Date of Filing (Month/Day/Year)	Prior Foreign Application(s) for pater (Number) 2001-387051 All foreign application (s) for pater	ation(s) JAPA plications, if any,	ertificate listed below and y) (Month/Da AN	d checked at right y/Year Filed) 12/20/2001	at:	Priority Yes	Claimed No
	Prior Foreign Application(s) for pater Prior Foreign Application (Number) 2001-387051 All foreign applifiling date of this application (s) for pater	JAPA plications, if any, ication:	(Month/Da	d checked at right y/Year Filed) 12/20/2001 tor's Certificate	filed more than 1	Priority Yes X 2 months	Claimed No

I hereby claim the benefit under Title 35, United States Code, § 119(e) or § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112. I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status: patented, pending, abandoned

I hereby appoint the following attorneys to prosecute this application and/or any international application and to transact all business in the Patent and Trademark Office connected therewith:

Daniel W. Sixbey, (Reg. No. 20,932)

Charles M. Leedom, Jr. (Reg. No. 26,477)

David S. Safran (Reg. No. 27,997)

Tim L. Brackett (Reg. No. 36,092)

Robert M. Schulman (Reg. No. 31,196)

Stuart J. Friedman (Reg. No. 24,312)

Gerald J. Ferguson, Jr. (Reg. No. 23,016)

Thomas W. Cole (Reg. No. 28,290)

Donald R. Studebaker (Reg. No. 32,815) Jeffrey L. Costellia (Reg. No. 35,483)

Eric J. Robinson (Reg. No. 38,285)

Thomas M. Blasey (Reg. No. 33,475)

Send Correspondence to:

Donald R. Studebaker

Nixon Peabody LLP

8180 Greensboro Drive, Suite 800

McLean, Virginia 22102 Telephone: (703) 790-9110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

The undersigned hereby authorize any U.S. attorney or agent named herein to accept and follow instructions Maeda Patent Office as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

FULL NAME OF SOLE OR FIRST INVENTOR Yoshifumi NAKAMURA	DIVENTOR'S SIGNATURE)	DATE Nov. 15, 2002		
RESIDENCE (City, State & Country) Osaka, Japan		CITIZENSHIP Japan		
POST OFFICE ADDRESS (Complete Address including City, State & Country) 2-2-34, Machikuzuha, Hirakata-shi, Osaka 573-1106, Japan				

-3-

FULL NAME OF SECOND JOINT INVENTOR (if any) Ryuichi SAHARA	INVENTOR'S SIGNATURE Rejuichi Suhara	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Osaka, Japan		CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Cit 6-10-2-304, Korigaoka, Hirakata-shi, Osaka 573	• • • • • • • • • • • • • • • • • • • •	
FULL NAME OF THIRD JOINT INVENTOR (if any) Nozomi SHIMOISHIZAKA	INVENTOR'S SIGNATURE Mozomi Shimouhizaha	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Kyoto, Japan		CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Cit 42-2, Sagadaikakuji-monzenrokudo-cho, Ukyo-l	- · · · · · · · · · · · · · · · · · · ·	
FULL NAME OF FOURTH JOINT INVENTOR (if any) Kazuyuki KAINOU	INVENTOR'S SIGNATURE Kazuyuki Kainou	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Osaka, Japan		CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Cit 2-15-20-407, Nasuzukuri, Hirakata-shi, Osaka 5	••	
FULL NAME OF FIFTH JOINT INVENTOR (if any) Keiji MIKI	INVENTOR'S SIGNATURE Keijù Miki	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Kyoto, Japan		CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Cit 10-31, Matsugasaki-icchoda-cho, Sakyo-ku,	ty, State & Country) Kyoto-shi, Kyoto 606-0954, Japan	
FULL NAME OF SIXTH JOINT INVENTOR (if any) Kazumi WATASE	INVENTOR'S SIGNATURE Kazumi Watase	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Kyoto, Japan		CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Ci 2-10-13, Oe-kitafukunishi-cho, Nishikyo-ku, Ky		-
FULL NAME OF SEVENTH JOINT INVENTOR (if any) Yasutake YAGUCHI	inventor's signature Yasutake Yaguchi	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Osaka, Japan	0 0	CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Ci 2-36-13-202, Miyata-cho, Takatsuki-shi, Osaka		

Docket No.: 740819-924 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yoshifumi NAKAMURA, Ryuichi SAHARA, Nozomi SHIMOISHIZAKA, Kazuyuki KAINOU, Keiji MIKI, Kazumi WATASE, Yasutake YAGUCHI

Serial No.:

10/307,450

Filed:

December 2, 2002

For. SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

REVOCATION OF POWER OF ATTORNEY, APPOINTMENT AND CERTIFICATION UNDER 37 CFR 3.73(B)

Commissioner for Patents Washington, DC 20231

Sir:

The undersigned assignee of the above-identified application hereby revokes all previous Powers of Attorney and appoints the following attorneys with full power to prosecute the application, to make alterations and amendments therein, and to transact all business in the United States Patent Office connected therewith.

I hereby appoint the following attorney(s) and/or agent(s): Steven W. Allis, Reg. No. 50,532; Stephen A. Becker, Reg. No. 26,527; John G. Bisbikis, Reg. No. 37,095; Daniel Bucca, Reg. No. 42,368; Kenneth L. Cage, Reg. No. 26,151; Jennifer Chen, Reg. No. 42,404; Bernard P. Codd, Reg. No. 46,429; Lawrence T. Cullen, Reg. No. 44,489; Paul Devinsky, Reg. No. 28,553; Margaret M. Duncan, Reg. No. 30,879; Shamita De. Etienne-Cummings, Reg. No. 46,072; Ramyar M. Farid, Reg. No. 46,692; Brian E. Ferguson, Reg. No. 36,801; Michael E. Fogarty, Reg. No. 36,139; John R. Fuisz, Reg. No. 37,327; Willem F. Gadiano, Reg. No. 37,136; Keith E. George, Reg. No. 34,111; John A. Hankins, Reg. No. 32,029; Eric J. Kraus, Reg. No. 36,190; Catherine Krupka, Reg. No. 46,227; Jack Q. Lever, Reg. No. 28,149; Raphael V. Lupo, Reg. No. 28,363; Burman Y. Mathis III, Reg. No. 44,907; Michael A. Messina, Reg. No. 33,424; Dawn L. Palmer, Reg. No. 41,238; Joseph H. Paquin, Jr., Reg. No. 31,647; Scott D. Paul, Reg. No. 42,984; William D. Pegg, Reg. No. 42,988; Robert L. Price, Reg. No. 22,685; Gene Z. Rubinson, Reg. No. 33,351; Brian K. Seidleck, Reg. No. 51,321; Joy Ann G. Serauskas, Reg. No. 27,952; Jiri F. Smetana, Reg. No. 52,456; David A. Spenard, Reg. No. 37,449; Arthur J. Steiner, Reg. No. 26,106; Wesley Strickland, Reg. No. 44,363;

Serial No.:

10/307,450

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McDERMOTT, WILL & EMERY 600 13th Street, N.W. Washington, DC 20005-3096

with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and all future correspondence should be addressed to them.

CERTIFICATE UNDER 37 CFR 3.73(b)

MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD., a corporation of 1006, Oaza Kadoma, Kadoma-shi, Osaka 571-8501, Japan, certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of:

An Assignment from the inventor(s) of the patent application identified above. A copy of the executed assignment is attached herewith.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

The undersigned further declares that all statements made herein of its own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States

WDC99 725640-1,060188,0011

Serial No.:

10/307,450

Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully submitted,

MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD.

Name:

Isamu SHIMURA

Title:

Director, IP Development Center

Authorized Signing Officer

Signature:

Date:

04.17.2003

-1-

DECLARATION AND POWER OF ATTORNEY	
FOR PATENT APPLICATION	

Attorney Docket No	·
--------------------	---

As a below named investated next to my name; that I below) or a joint inver	verily believe that I	am the origina	l, first and sole	inventor (if on	ly one nan	ne is listed
	, the specificati	on of which is	attached hereto u	nless the follow	wing box i	s checked:
and w	pecification was filed as assigned Serial N was amended on	lo	(if known)			
I hereby state that I hat the claims, as amended by any			(e-identified sp	ecification	, including
I acknowledge the duraccordance with Title 37, Cod			material to the	examination of	of this app	olication in
I do not know and do or our invention thereof, or parthereof, or more than one year States of America more than or subject of an inventor's certific of America on an application of application, and that no application foreign to the United States of as follows: I hereby claim foreign application(s) for patent or inventories.	tented or described in prior to this application pear prior to this attention is attentional pear prior to the filed by me or my legistation for patent or it. America prior to the gn priority benefits	n any printed pration, that the samplication, the date of this apgal representation ventor's certificial application to the samplication to the sa	same was not in any same was not in nat the invention plication in any eves or assigns me icate on this invention or my legal 35, United Sta	country before public use or has not been p country foreign ore than twelve ention has been al representative	e my or ou on sale in patented on to the Ur e months particled in a ves or assignment of a	r invention the United r made the nited States prior to this ny country gns, except ny foreign
Prior Foreign Application(s) (Number)	(Country)	(Month/Day/)	'ear Filed)		Priority Yes	Claimed No
2001-387051	JAPAN		12/20/2001		х	
All foreign application filing date of this application:	ns, if any, for any Pa	atent or Invento Application No.	r's Certificate file		2 months	

I hereby claim the benefit under Title 35, United States Code, § 119(e) or § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112. I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, & 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status: patented, pending, abandoned

I hereby appoint the following attorneys to prosecute this application and/or any international application and to transact all business in the Patent and Trademark Office connected therewith:

Daniel W. Sixbey, (Reg. No. 20,932)

Charles M. Leedom, Jr. (Reg. No. 26,477)

David S. Safran (Reg. No. 27,997) Donald R. Studebaker (Reg. No. 32,815) Jeffrey L. Costellia (Reg. No. 35,483)

Tim L. Brackett (Reg. No. 36,092)

Robert M. Schulman (Reg. No. 31,196)

Stuart J. Friedman (Reg. No. 24,312)

Gerald J. Ferguson, Jr. (Reg. No. 23,016)

Thomas W. Cole (Reg. No. 28,290)

Eric J. Robinson (Reg. No. 38,285)

Thomas M. Blasey (Reg. No. 33,475)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

The undersigned hereby authorize any U.S. attorney or agent named herein to accept and follow instructions Maeda Patent Office as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

FULL NAME OF SOLE OR FIRST INVENTOR Yoshifumi NAKAMURA	pryentors signature	DATE Nov. 15, 2002		
RESIDENCE (City, State & Country) Osaka, Japan		CITIZENSHIP Japan		
POST OFFICE ADDRESS (Complete Address including City, State & Country) 2-2-34, Machikuzuha, Hirakata-shi, Osaka 573-1106, Japan				

-3-

FULL NAME OF SECOND JOINT INVENTOR (if any) Ryuichi SAHARA	INVENTOR'S SIGNATURE Rejuichi Suhara	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Osaka, Japan		CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Cit 6-10-2-304, Korigaoka, Hirakata-shi, Osaka 573	• • • • • • • • • • • • • • • • • • • •	
FULL NAME OF THIRD JOINT INVENTOR (if any) Nozomi SHIMOISHIZAKA	INVENTOR'S SIGNATURE Mozomi Shimouhizaha	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Kyoto, Japan		CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Cit 42-2, Sagadaikakuji-monzenrokudo-cho, Ukyo-l	- · · · · · · · · · · · · · · · · · · ·	
FULL NAME OF FOURTH JOINT INVENTOR (if any) Kazuyuki KAINOU	INVENTOR'S SIGNATURE Kazuyuki Kainou	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Osaka, Japan		CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Cit 2-15-20-407, Nasuzukuri, Hirakata-shi, Osaka 5	••	
FULL NAME OF FIFTH JOINT INVENTOR (if any) Keiji MIKI	INVENTOR'S SIGNATURE Keijù Miki	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Kyoto, Japan		CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Cit 10-31, Matsugasaki-icchoda-cho, Sakyo-ku,	ty, State & Country) Kyoto-shi, Kyoto 606-0954, Japan	
FULL NAME OF SIXTH JOINT INVENTOR (if any) Kazumi WATASE	INVENTOR'S SIGNATURE Kazumi Watase	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Kyoto, Japan		CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Ci 2-10-13, Oe-kitafukunishi-cho, Nishikyo-ku, Ky		-
FULL NAME OF SEVENTH JOINT INVENTOR (if any) Yasutake YAGUCHI	inventor's signature Yasutake Yaguchi	DATE Nov. 15, 2002
RESIDENCE (City, State & Country) Osaka, Japan	0 0	CITIZENSHIP Japan
POST OFFICE ADDRESS (Complete Address including Ci 2-36-13-202, Miyata-cho, Takatsuki-shi, Osaka		

PATENT	APPLICATION	SERIAL	, NO.

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE FEE RECORD SHEET

08/19/2004 FMETEKI1 00000002 500417 10919402 01 FC:1001 770.00 DA

> PTO-1556 (5/87)

*U.S. Government Printing Office: 2002 --- 489-267/69033

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	PATENT	• • •		ber 1, 2003	rion reco	ORD	10	9	194	002
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F	OR .		NUMBER	R FILED NUM	BER EXTRA	BASIC	EE 385.00	OR	BASIC FE	770.00
TO	OTAL CHARGE	ABLE CLAIMS	10 m	inus 20= • /		XS 9	=	OR	X\$18=	
IN	DEPENDENT C	CLAIMS	1 m	ninus 3 = 2	3	X43=	:	OR	X86=	
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	(LAIMS AS A (Column 1)	AMENDE	(Column 2)	(Column 3)	SMAL	L ENTITY	OR	OTHER SMALL	
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
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AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
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Docket No.: 60188-932 <u>PATENT</u>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

NAKAMURA, YOSHIFUMI, et al. : Customer No.: 20277

Serial No.: Divisional of : Group Art Unit: To be assigned

Application No. 10/307,450

Filed: August 17, 2004 : Examiner: To be assigned

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

PRELIMINARY AMENDMENT

Mail Stop NEW APPLICATIONS Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

AMENDMENT TO THE SPECIFICATION

Please amend the paragraph beginning on page 21, line 6 as follows:

--A second characteristic of the second embodiment is that, as [[descried]] <u>described</u> above, the insulating resin layer 17, which is formed from an epoxy resin having low elasticity or the like, is formed between the metal wirings 14 each electrically connected to a corresponding one of the electrodes 12 of the semiconductor element 11 and the passivation film 13 formed over the surface of the semiconductor element 11.--

AMENDMENT TO THE CLAIMS

1-13. (Canceled)

14. (New) A semiconductor device, comprising:

a semiconductor element;

a first electrode portion formed on the semiconductor element, said first electrode portion comprising a first metal component;

a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal component; and

a diffusion layer formed between said first electrode portion and said second electrode portion,

wherein said diffusion layer comprises said first metal component and said second metal component.

15. (New) The semiconductor device of claim 14,

wherein said first electrode portion and said diffusion layer have a combined thickness in the range of $10\mu m$ to $20\mu m$.

16. (New) The semiconductor device of claim 14, wherein said first metal component includes copper and said second metal component includes tin.

- 17. (New) The semiconductor device of claim 14, further comprising a third electrode portion formed on a surface of the semiconductor element and a metal wiring formed on the semiconductor element, said metal wiring electrically connecting the first electrode portion to the third electrode portion.
- 18. (New) The semiconductor device of claim 17, wherein the first and third electrode portion are horizontally spaced apart with respect to the semiconductor element.
- 19. (New) The semiconductor device of claim 17, further comprising an insulating film formed on said metal wiring,

wherein an opening of said insulating film exposes a surface of the first electrode portion, and

wherein said surface of the first electrode portion is flush with or higher than a surface of the insulating film.

- 20. (New) The semiconductor device of claim 17, wherein the metal wiring includes copper.
- 21. (New) The semiconductor device of claim 14, further comprising a substrate having a wiring electrode,

wherein said wiring electrode is electrically connected to said second electrode portion.

22. (New) The semiconductor device of claim 17, further comprising an insulating resin layer formed between the surface of the semiconductor element and the metal wiring, wherein the metal wiring is formed along a surface of the insulating resin layer.

23. The semiconductor device of claim 17, wherein the metal wiring has a thickness in the range of $0.01\mu m$ to $8\mu m$.

REMARKS

This amendment is necessary to incorporate the amendment in the specification made in parent application Serial No. 10/307,450, as well as to cancel claims 1-13 and replace them with new claims 14-23.

Entry of this amendment is respectfully requested.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty

Registration No. 36,139

600 13th Street, N.W. Washington, DC 20005-3096 202.756.8000 MEF:BD Facsimile: 202.756.8087

Date: August 17, 2004

WDC99 964611-1.060188.0932

Docket No.: 60188-932 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277

NAKAMURA, YOSHIFUMI, et al. : Confirmation Number: To be assigned

Serial No.: Divisional of : Group Art Unit: To be assigned

Application No. 10/307,450

Filed: August 17, 2004 : Examiner: To be assigned

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

INFORMATION DISCLOSURE STATEMENT

Mail Stop NEW APPLICATIONS Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial No. 10/307,450, filed December 2, 2002, which is relied upon for an

Serial No.: Divisional of Application No. 10/307,450

earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR 1.98(d).

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty

Registration No. 36,139

600 13th Street, N.W. Washington, DC 20005-3096 202.756.8000 MEF:BD

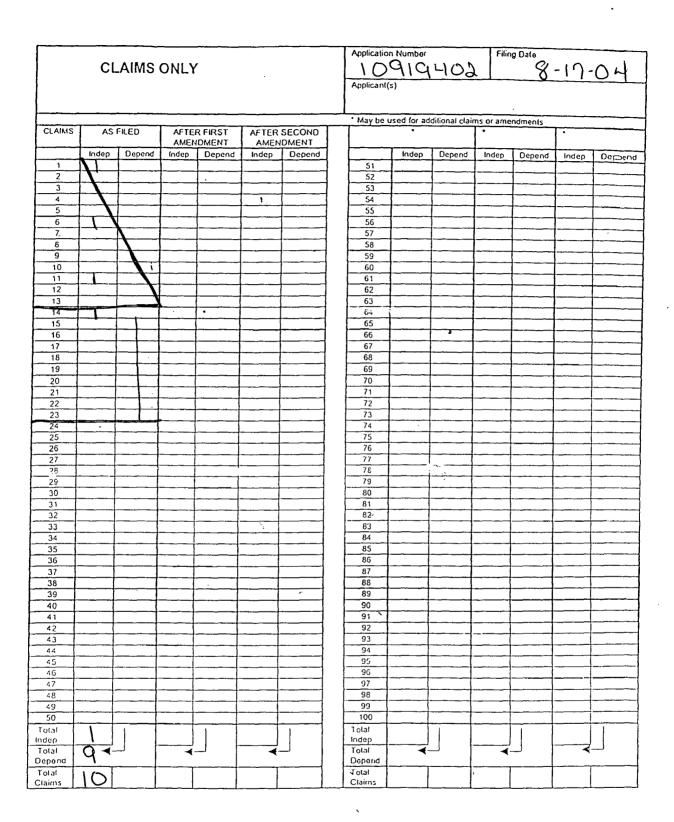
Facsimile: 202.756.8087 **Date: August 17, 2004**

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SHEET 1 OF 1

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INFORMA	ATIC		ISCLOSURE (IN AN	CITATION	ATTY. DOCKET NO. 60188-932		RIAL NO. ivisional of 10/307,450
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					APPLICANT Yoshfumi NAKAMUR	IA, et al.	
		(P7	rO-1449)		FILING DATE August 17, 2004		ROUP o be assigned
!				U.S. PATENT	T DOCUMENTS		
EXAMINER'S			Document Number	Publication Date	Name of Patentee or Applic	ant of Cited	Pages, Columns, Lines, Where Relevant
INITIALS	CITE NO.		-Kind Code2 (# known)	MM-DD-YYYY	Document		Passages or Relevant Figures Appear
		US	5,719,439	02/17/1998	lwasaki et a	1.	
		US	5,892,273	04/06/1999	lwasaki et a	1.	
		US	2002/0108781A1	8/2002	Mune et al		
		US	6,587,353	7/2003	Sumikawa et	al	
		US	6,512,298	1/2003	Sahara et a	1	
		US	6,475,896	11/2002	Hashimoto)	
		US	6,414,390	7/2002	Nozawa		
		US	6,396,157	5/2002	Nakanishi et	al	
		US	5,604,379	2/1997	Mori		
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EXAMINER'S INITIALS	CITE NO.		oreign Patent Document puntry Codes -Number a -Kind Codes (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation 9 Yes No
		J	P 2001-291733 A	10/19/2001	CASIO COMPUT CO LTD		JAPAN (w/ English Abstract and Partial English Translation)
		J	P 2001-118956 A	04/27/2001	MATSUSHITA ELECTRONICS INDUSTRY		JAPAN (w/ English Abstract and Partial English Translation)
		J	P 2001-291721 A	10/19/2001	NEC CORP.		JAPAN (w/ English Abstract and Partial English Translation)
			JP 9- 129772 A	05/16/1997	TOSHIBA CORP.		JAPAN (w/ English Abstract and Partial English Translation)
		J	P 2000-299405 A	10/24/2000	ROHM CO LTD.		JAPAN (w/ English Abstract and Partial English Translation)
			JP 10079362	3/11998	Fukazawa et al		
			JP 3137322	12/2000			
EVANINESIS	T				r, Title, Date, Pertinent Pages, Etc.		
EXAMINER'S INITIALS	CITE NO.		de name of the author (in CA al, symposium, catalog, etc.),	APITAL LETTERS), tit date, page(s), volume	le of the article (when appropriate), e-issue number(s), publisher, city a	, title of the ite nd/or country	m (book, magazine, journal, where published.
	l	E	KAMINER			DATE CONS	SIDERED

ļ	PATENT APPLICATION FEE DETERMINATION RECORD Effective October 1, 2003 Application of Docker Number 10919407												
-		CLAIMS	AS FILED			umn 2)		SMALL TYPE	ENTITY	Of Of		R THAN ENTITY	
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AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHE NUMB PREVIO	ER USLY	PRESENT EXTRA		RATE	ADDI- TIONAL FEE	.] .	RATE	ADDI- TIONAL FEE	
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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
Li	0	09/626,891	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 11:25
L2	1	"09626891"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 12:06
L3	5	"10079362"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 12:36
L4	17	"3137322"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 12:11
L5	0	"43137322"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 12:11
L6	0	"403137322"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 12:11
L7	0	JP3137322	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 12:16
L8	26517	257/669,770,673,674,676,688,692-697, 728-752,735-739,758,773-776,780-786. ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 12:18

L9	3638	8 and (electrode\$1 with metal)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 14:25
L15	286	9 and ((diffus\$3 near (layer film junction)) with electrode\$1)	US-PGPUB, USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 14:26
L17	153	10 and thick	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 14:26
L18	2	("6662442") PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2004/11/12 13:29
L19	4	("5246817" "5323520" "6162580" "6255039").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2004/11/12 14:23
L20	373110	"257"/\$.ccls: "438"/\$.ccls: "29"/\$.ccls:	US-PGPUB; USPAT; USOCR	OR	ON	2004/11/12 14:23
L21	40981	20 and (electrode\$1 with metal)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 15:07
L22	800	9 and (diffus\$3 with electrode\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 15:08
L23	701	22 and thick\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 15:08
1.24	83	23 and (metal with (copper Cu) with (tin Ti))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 14:49

L25	64	23 and (metal with (copper Cu) with (tin Sn))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR ·	ON	2004/11/12 15:08
L26	249014	(electrode\$1 with metal)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 15:07
L27	21286	26 and (diffus\$3 with electrode\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 15:08
L28	15095	27 and thick\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 15:08
L29	735	28 and (metal with (copper Cu) with (tin Sn))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 15:09
L30	128	29 and (metal near wir\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 15:10
L31	. 18	30 and (insulat\$3 near resin)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 15:16
L32	215	28 and (insulat\$3 near resin)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 15:17
L33	172	32 and wir\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2004/11/12 15:17



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Alexandria, Virgin www.uspto.gov	ia 22313-1450
www.uspio.gov	

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/919,402	08/17/2004	Yoshifumi Nakamura	60188-932	6102
20277 7	7590 11/16/2004		EXAM	INER
MCDERMOT	TT WILL & EMERY LI	LP .	HUYNH	, ANDY
	N, DC 20005-3096		ART UNIT	PAPER NUMBER
	,		2818	
			DATE MAIL ED. 11/16/200	4

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
		Applicant(s)
Office Action Summan	10/919,402	NAKAMURA ET AL.
Office Action Summary	Examiner	Art Unit
	Andy Huynh	2818
The MAILING DATE of this communication apperiod for Reply	pears on the cover sheet with th	e correspondence address
A SHORTENED STATUTORY PERIOD FOR REPL THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.1 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a rep If NO period for reply is specified above, the maximum statutory period Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailin earned patent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may a reply be ly within the statutory minimum of thirty (30) will apply and will expire SIX (6) MONTHS fr e, cause the application to become ABANDO	e timely filed days will be considered timely. om the mailing date of this communication. NED (35 U.S.C. § 133).
Status		
1) Responsive to communication(s) filed on 17.4	August 2004.	
· · · · ·	s action is non-final.	
3) Since this application is in condition for allowa closed in accordance with the practice under the condition of the condit	nnce except for formal matters,	
Disposition of Claims		
4) Claim(s) 14-23 is/are pending in the application 4a) Of the above claim(s) is/are withdra 5) Claim(s) is/are allowed. 6) Claim(s) 14-23 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or	awn from consideration.	
Application Papers		
9) The specification is objected to by the Examine 10) The drawing(s) filed on 17 August 2004 is/are: Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the E	a) \boxtimes accepted or b) \square objects drawing(s) be held in abeyance. Stion is required if the drawing(s) is	See 37 CFR 1.85(a). objected to. See 37 CFR 1.121(d).
Priority under 35 U.S.C. § 119		
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority documen 2. Certified copies of the priority documen 3. Copies of the certified copies of the priority application from the International Burea * See the attached detailed Office action for a list	its have been received. Its have been received in Application of the process of t	cation No. <u>10/307,450</u> . vived in this National Stage
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08 Paper No(s)/Mail Date 08/17/2004.	4) Interview Summ Paper No(s)/Mai 5) Notice of Inform 6) Other:	

DETAILED ACTION

In the Preliminary Amendment filed 08/17/2004, the specification is amended, claims 1-13 are canceled and new claims 14-23 are added is acknowledged. Accordingly, claims 14-23 are pending in the application, which is a divisional of Application No. 10/307,450 filed 12/02/2002, USP 6.784,557.

Priority

Acknowledgment is made of applicants' claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in Parent Application No. 10/307,450, filed 12/02/2002.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed 08/17/004. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Application/Control Number: 10/919,402 Page 3

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Claims **14 and 16-20** are rejected under 35 U.S.C. 102(e) as being anticipated by Mune et al. (Pub. No. US 2002/0108781, which is DIV of application No. 09/626,891 filed 07/27/2000, hereinafter referred to as "Mune").

Regarding claims **14 and 16**, Mune discloses in Fig. 1 and the corresponding texts as set forth in [0026]-[0059], a semiconductor device, comprises:

a semiconductor element/a semiconductor chip (18);

a first electrode portion/an outer electrode (31) formed on the semiconductor element/the semiconductor chip, said first electrode portion/the outer electrode comprising a first metal component (Cu);

a second electrode portion/a solder ball (26) formed on the semiconductor element/the semiconductor chip and electrically connected to said first electrode portion/the outer electrode, said second electrode portion/the solder ball comprising a second metal component (Sn) different from said first metal component; and

a diffusion layer formed between said first electrode portion/the outer electrode and said second electrode portion/the solder ball,

wherein said diffusion layer comprises said first metal component and said second metal component.

Regarding claim 17, Mune discloses in Fig. 1 the semiconductor device further comprises a third electrode portion/an inner electrode (27) formed on a surface of the semiconductor element/the semiconductor chip and a metal wiring/a conductor layer (21) formed on the semiconductor element, said metal wiring/the conductor layer electrically connecting the first electrode portion/the outer electrode to the third electrode portion/the inner electrode.

Application/Control Number: 10/919,402

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Regarding claim 18, Mune discloses in Fig. 1 the semiconductor device wherein the first/the outer and third electrode portion/the inner are horizontally spaced apart with respect to the semiconductor element/the semiconductor chip.

Regarding claim 19, Mune discloses in Fig. 1 the semiconductor device further comprises an insulating film (22) formed on said metal wiring/the conductor layer, wherein an opening (24) of said insulating film exposes a surface of the first electrode portion/the outer electrode, and wherein said surface of the first electrode portion/the outer electrode is flush with or higher than a surface of the insulating film.

Regarding claim 20, Mune discloses the semiconductor device wherein the metal wiring/the conductor layer includes copper (see [0045]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mune et al. (Pub. No. US 2002/0108781, which is DIV of application No. 09/626,891 filed 07/27/2000, hereinafter referred to as "Mune").

Mune discloses the claimed limitations except for the semiconductor device wherein said first electrode portion and said diffusion layer have a combined thickness in the range of 10µm to

Page 4

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20μm, and wherein the metal wiring has a thickness in the range of 0.01μm to 8μm. Mune discloses the thickness of the outer insulator layer (22) suitably ranges from 5 to 50 μm as set forth in [0033], and the outer electrode (31) having same thickness as the outer insulator layer, and the metal wiring/the conductor layer has a thickness in the range of 5μm to 15μm. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the first electrode portion and the diffusion layer have a combined thickness in the range of 10μm to 20μm, and the metal wiring has a thickness in the range of 0.01μm to 8μm, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims **21 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mune et al. (Pub. No. US 2002/0108781, which is DIV of application No. 09/626,891 filed 07/27/2000, hereinafter referred to as "Mune") in view of Fig. 15C Prior Art, Applicant admitted prior art (AAPA).

Mune discloses the claimed limitations except for the semiconductor device further comprises a substrate having a wiring electrode, wherein said wiring electrode is electrically connected to said second electrode portion; and further comprising an insulating resin layer formed between the surface of the semiconductor element and the metal wiring, wherein the metal wiring is formed along a surface of the insulating resin layer. Fig. 15C Prior Art (AAPA) teaches that the semiconductor device comprises a substrate/a insulating resin layer (7) having a wiring electrode (4), wherein said wiring electrode is electrically connected to said second electrode portion (6). It would have been obvious to one of ordinary skill in the art at the time of

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the invention was made to incorporate the teachings of Fig. 15C Prior Art (AAPA) into Mune's structure to modify and form the semiconductor device further comprising a substrate/a insulating resin layer having a wiring electrode, wherein said wiring electrode is electrically connected to said second electrode portion and the metal wiring is formed along a surface of the insulating resin layer, since it was known in the art and the selection of any of these conventional semiconductor device would be within the level of ordinary skill in the art.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

Page 6

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Art Unit: 2818

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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11/12/04

Patent Examiner

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	E	US-2002/0079575	06-2002	Hozoji et al.	257/734
	F	US-2002/0108781	08-2002	Mune et al.	174/264
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NON-PATENT DOCUMENTS

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"A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office PTO-892 (Rev. 01-2001)

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Part of Paper No. 111204

SHEET 1 OF 1

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Application No.	Applicant(s)	
10/919,402	NAKAMURA ET AL.	
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Andy Huynh	2818	

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Docket No.: 60188-932





ES PATENT AND TRADEMARK OFFICE

In re Application of

Customer Number: 20277

NAKAMURA, YOSHIFUMI, et al.

Confirmation Number: 6102

Application No.: 10/919,402

Group Art Unit: 2818

Filed: August 17, 2004

Examiner: Huynh, Andy

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

Mail Stop Amendment Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

 \boxtimes

Transmitted herewith is an Amendment in the above-identified application.

No additional fee is required.

Applicant is entitled to small entity status under 37 CFR 1.27

Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	18	20	0	\$50.00 =	\$0.00
Independent Claims	2	3	0	\$200.00 =	\$0.00
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Please charge my Deposit Account No. 500417 in the amount of \$0.00. An additional copy of this transmittal sheet is submitted herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

McDERMOT WILL & EMERY LLP

Michael E. Fogarty Registration No 36,139

Please recognize our Customer No. 20277 as our

correspondence address.

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Page 112 of 199

Docket No.: 60188-932

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277

NAKAMURA, YOSHIFUMI, et al. : Confirmation Number: 6102

Application No.: 10/919,402 : Group Art Unit: 2818

Filed: August 17, 2004 : Examiner: HUYNH, ANDY

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

AMENDMENT UNDER 37 C.F.R. § 1.111

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated November 16, 2004, having a shortened statutory period for response set to expire February 16, 2005, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

1-13. (Cancelled)

14. (Previously presented) A semiconductor device, comprising:

a semiconductor element;

a first electrode portion formed on the semiconductor element, said first electrode portion

comprising a first metal component;

a second electrode portion formed on the semiconductor element and electrically

connected to said first electrode portion, said second electrode portion comprising a second metal

component different from said first metal component; and

a diffusion layer formed between said first electrode portion and said second electrode

portion,

wherein said diffusion layer comprises said first metal component and said second metal

component.

15. (Currently amended) A [[The]] semiconductor device [[of claim 14,]] comprising:

a semiconductor element;

a first electrode portion formed on the semiconductor element, said first electrode portion

comprising a first metal component;

a second electrode portion formed on the semiconductor element and electrically

connected to said first electrode portion, said second electrode portion comprising a second metal

component different from said first metal component; and

a diffusion layer formed between said first electrode portion and said second electrode

portion,

wherein said diffusion layer comprises said first metal component and said second metal

component, and

said first electrode portion and said diffusion layer have a combined thickness in the

range of 10 μ m to 20 μ m.

16. (Previously presented) The semiconductor device of claim 14, wherein said first

metal component includes copper and said second metal component includes tin.

17. (Previously presented) The semiconductor device of claim 14, further comprising a

third electrode portion formed on a surface of the semiconductor element and a metal wiring

formed on the semiconductor element, said metal wiring electrically connecting the first

electrode portion to the third electrode portion.

18. (Previously presented) The semiconductor device of claim 17, wherein the first and

third electrode portion are horizontally spaced apart with respect to the semiconductor element.

19. (Previously presented) The semiconductor device of claim 17, further comprising an

insulating film formed on said metal wiring,

wherein an opening of said insulating film exposes a surface of the first electrode portion,

and

wherein said surface of the first electrode portion is flush with or higher than a surface of

the insulating film.

20. (Previously presented) The semiconductor device of claim 17, wherein the metal

wiring includes copper.

21. (Previously presented) The semiconductor device of claim 14, further comprising a

substrate having a wiring electrode,

wherein said wiring electrode is electrically connected to said second electrode portion.

22. (Previously presented) The semiconductor device of claim 17, further comprising an

insulating resin layer formed between the surface of the semiconductor element and the metal

wiring,

wherein the metal wiring is formed along a surface of the insulating resin layer.

23. (Previously presented) The semiconductor device of claim 17, wherein the metal

wiring has a thickness in the range of 0.01 μ m to 8 μ m.

24. (New) The semiconductor device of claim 15, wherein said first metal component

includes copper and said second metal component includes tin.

25. (New) The semiconductor device of claim 15, further comprising a third electrode

portion formed on a surface of the semiconductor element and a metal wiring formed on the

semiconductor element, said metal wiring electrically connecting the first electrode portion to the

third electrode portion.

26. (New) The semiconductor device of claim 25, wherein the first electrode portion and

the third electrode portion are horizontally spaced apart with respect to the semiconductor

element.

27. (New) The semiconductor device of claim 25, further comprising an insulating film

formed on said metal wiring,

wherein an opening of said insulating film exposes a surface of the first electrode portion,

and

wherein said surface of the first electrode portion is flush with or higher than a surface of

the insulating film.

28. (New) The semiconductor device of claim 25, wherein the metal wiring includes

copper.

29. (New) The semiconductor device of claim 15, further comprising a substrate having a wiring electrode,

wherein said wiring electrode is electrically connected to said second electrode portion.

30. (New) The semiconductor device of claim 25, further comprising an insulating resin layer formed between the surface of the semiconductor element and the metal wiring,

wherein the metal wiring is formed along a surface of the insulating resin layer.

31. (New) The semiconductor device of claim 25, wherein the metal wiring has a

REMARKS

I. <u>Introduction</u>

In response to the Office Action dated November 16, 2004, Applicants have rewritten

claim 15 into independent format. Also, Applicants have added new claims 24-31. Support for

these amendments can be found, for example, in Figs. 1 and 2, and their corresponding sections

of the specifications. No new matter has been added.

Furthermore, it is noted that prior art reference, JP 3137322, which was submitted in the

Information Disclosure Statement "IDS" filed on August 17, 2004, has not yet been indicated to

have been considered by the Examiner. It is respectfully requested that the Examiner initial this

reference on the PTO-1449 form that was submitted with the IDS and return the form to the

Applicants so that they can confirm that the reference has been considered. Although a copy of

the foregoing reference was previously submitted with the IDS, an additional copy is enclosed

herewith for the Examiner's convenience.

For the reasons set forth below, Applicants respectfully submit that all pending claims are

patentable over the cited prior art references.

II. The Rejection Of Claims 14 and 16-20 Under 35 U.S.C. § 102

Claims 14 and 16-20 are rejected under 35 U.S.C. § 102(e) as being anticipated by US

Pub No. 2002/0108781 to Mune. Applicants respectfully traverse this rejection for at least the

following reasons.

Claim 14 recites in-part a semiconductor device, comprising a first electrode portion and

a diffusion layer, wherein the diffusion layer comprises the first metal component and the second

metal component.

In accordance with one embodiment of the present invention, a diffusion layer (e.g. Sn-Cu alloy layer) is formed between the first electrode portion (e.g. external electrode portion 14a) comprising the first metal component (e.g. Cu) and the second electrode portion (e.g. ball electrode 16) comprising the second metal component (e.g. Sn) different from the first metal component, and the diffusion layer is an alloy layer comprising both the first metal component and the second metal component. In this manner, an alloy including the first metal component and the second metal component is not entirely formed in the thickness direction of the first electrode portion. As a result, the present invention advantageously provides a semiconductor device having high reliability in which the strength of the metal of the first electrode portion can be maintained (*see, e.g.*, page 15, lines 8-19 of the specification).

In the pending rejection, the Examiner asserts that the outer electrodes 31 of Mune correspond to the claimed first electrode portion, and the solder ball 26 of Mune corresponds to the claimed second electrode portion.

However, at a minimum, Mune is completely silent as to the materials of the outer electrodes 31 and the solder ball 26, let alone suggest a diffusion layer comprising their respective metal component so as to allow it to be positioned between the outer electrodes 31 and the solder ball 26. Indeed, the Examiner has not identified which element of Muno corresponds to the claimed diffusion layer and the materials therein. As such, if the Examiner continues to maintain the pending rejection in the next Office Action, it is respectfully requested that the Examiner specifically identify the corresponding diffusion layer and the metal components of the outer electrodes 31 and the solder ball 26 in Muno so that the Applicants may further address the Examiner's arguments.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly in inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Mune does not anticipate claims 14 and 15, nor any claim dependent thereon.

III. The Rejection Of Claims 15 and 23 Under 35 U.S.C. § 103

Claims 15 and 23 are rejected under 35 U.S.C. § 103 as being unpatentable over Mune.

Applicants respectfully traverse this rejection for at least the following reasons.

Claim 15 recites a semiconductor device, wherein the first electrode portion and the diffusion layer have a combined thickness in the range of 10 μ m to 20 μ m.

In accordance with one exemplary embodiment of the present invention, an electrode portion has a thickness in the range of 10μ m to 20μ m. It is respectfully submitted that the foregoing claimed range provides new and unexpected results over the relied on range of 5μ m to 50μ m of Mune. In particular, it is respectfully submitted that "the claims are directed to a narrow range, [and] the reference [Mune] teaches a broad range, and there is evidence of unexpected results within the claimed narrow range" so that Mune does not disclose or suggest the claimed narrow range with "sufficient specificity." The Examiner is directed to **MPEP §** 2131.03 under the heading "Prior Art ... With Sufficient Specificity" for the applicable standard.

In the instant case, it is respectfully submitted that such a range has <u>criticality and</u>

provides new and unexpected results at **both** the upper and lower limit thereof. As discussed in detail on page 16, line 10 – page 17, line 15 of Applicants' specification, Applicants have

discovered that an electrode thickness less than $10\mu m$ is susceptible to being disconnected while a thickness more than $20\mu m$ can lead to greater pattern deformation. Applicants have further discovered that if the thickness of the external electrode portion exceeds $20\mu m$, it is difficult to form the resist mask 23 having a sufficient thickness (see FIG. 11D) near the openings (i.e., stepped portions) of the insulating film 15 (see page 41, line 24 – page 42, line 2 of Applicants' specification). Even further, Applicants have discovered that a thickness over $20\mu m$ can cause wafer bending which may decrease a yield rate of the semiconductor devices.

Only Applicants' have discovered the dual benefits set at both range limits for the electrode thickness. It should be noted that the "disconnection occurrence at thicknesses less than $10 \mu m$ " and "pattern deformations/decreased yield rate at thicknesses greater than $20 \mu m$ " exemplify results that are *independent* of each other, thereby emphasizing the new and unexpected characteristic thereof. The cited prior art is completely silent as to suggesting a thickness range where the upper and lower limits are determined based on independent factors, let alone the specific factors of "disconnections" and "pattern deformation/yield rate" as disclosed in the present invention.

It should also be recognized that the fact that the prior art could be modified so as to result in the combination defined by the claims at bar would not have made the modification obvious unless the prior art suggests the desirability of the modification. *In re Deminski*, 796 F.2d 436, 230 USPO 313 (Fed. Cir. 1986).

Moreover, recognizing after the fact that such a modification would provide an improvement or advantage, without suggestion thereof by the prior art, rather than dictating a conclusion of obviousness, is an indication of improper application of hindsight considerations.

Simplicity and hindsight are not proper criteria for resolving obviousness. *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

It is only Applicants' disclosure that discloses the foregoing claimed range. Thus, the only motivation of record for the proposed modification of the range of Mune to arrive at the claimed invention is found in Applicants' disclosure which, of course, may not properly be relied upon to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 2271 USPQ2d 1593 (Fed. Cir. 1987).

For all of the foregoing reasons, it is respectfully submitted that claim 15 is patentable over the cited prior art.

IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTZ WILL & EMERY LLP

Michael E Fogarty Registration No. 36,139

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Facsimile: 202.756.8087

Date: February 14, 2005

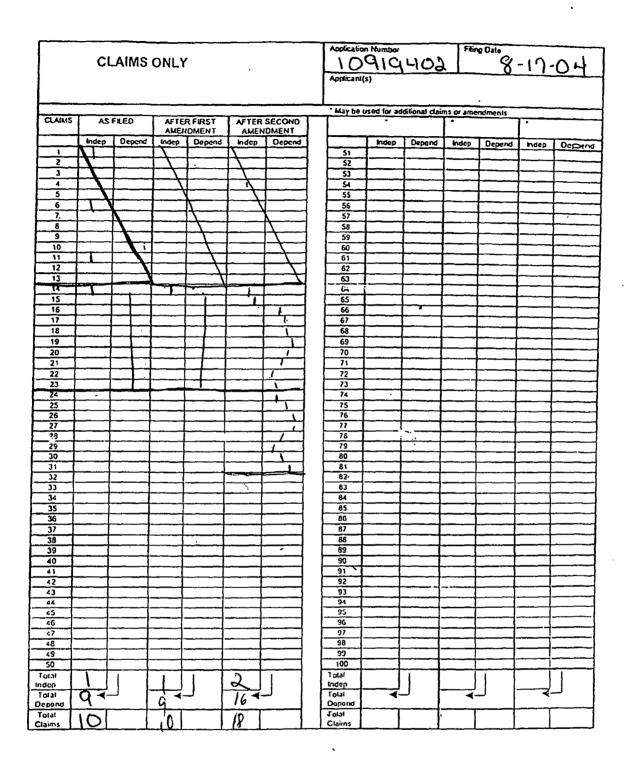
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This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file faird by the suited by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file faird by the suited by 37 CFR 1.14. This collection is estimated to take 12 minutes to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case, Ahy comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

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04/08/2005

MCDERMOTT WILL & EMERY LLP 600 13TH STREET, N.W. WASHINGTON, DC 20005-3096

EXAMINER HUYNH, ANDY

PAPER NUMBER

ART UNIT

DATE MAILED: 04/08/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/919,402	08/17/2004	Yoshifumi Nakamura	60188-932	6102

TITLE OF INVENTION: SEMICONDUCTOR DEVICE INCLUDING A DIFFUSION LAYER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$1700	07/08/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. <u>PROSECUTION ON THE MERITS IS CLOSED</u>. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

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or Fax

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APPLICATION NO.	FILING DATE]	FIRST NAMED INVE	NTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/919,402	08/17/2004		Yoshifumi Nakan	nura	60188-932	6102
TITLE OF INVENTION: S	EMICONDUCTOR DEVICE	E INCLUDING A	DIFFUSION LAYE	R		•
APPLN, TYPE	SMALL ENTITY	ISSUE FE	EE P	UBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/919,402	08/17/2004	Yoshifumi Nakamura	60188-932	6102
20277	7590 04/08/2005		EXAM	INER
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600 13TH STRE WASHINGTON	EET, N.W. J. DC 20005-3096		ART UNIT	PAPER NUMBER
	,		2818	
			DATE MAIL ED. 04/09/2004	.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

	Application No.	Applicant(s)
	10/919,402	NAKAMURA ET AL.
Notice of Allowability	Examiner	Art Unit
	Andy Huynh	2818
The MAILING DATE of this communication apperation all claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in th or other appropriate communic GHTS. This application is subj	is application. If not included cation will be mailed in due course. THIS
1. \boxtimes This communication is responsive to <u>the Amendment dated</u>	d 02/14/05.	
2. The allowed claim(s) is/are <u>14-31</u> .		
3. \boxtimes The drawings filed on <u>17 August 2004</u> are accepted by the	Examiner.	
 4. Acknowledgment is made of a claim for foreign priority un a) All b) Some* c) None of the: 1. Certified copies of the priority documents have 	,	f).
2. Certified copies of the priority documents have	• •	
3. Copies of the certified copies of the priority doc	cuments have been received in	this national stage application from the
International Bureau (PCT Rule 17.2(a)).		
* Certified copies not received:		,
Applicant has THREE MONTHS FROM THE "MAILING DATE" on noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		reply complying with the requirements
5. A SUBSTITUTE OATH OR DECLARATION must be submi INFORMAL PATENT APPLICATION (PTO-152) which give		
6. CORRECTED DRAWINGS (as "replacement sheets") mus	t be submitted.	•
(a) ☐ including changes required by the Notice of Draftspers		PTO-948) attached
1) ☐ hereto or 2) ☐ to Paper No./Mail Date		
(b) including changes required by the attached Examiner's Paper No./Mail Date	Amendment / Comment or in	the Office action of
Identifying indicia such as the application number (see 37 CFR 1. each sheet. Replacement sheet(s) should be labeled as such in the		
 DEPOSIT OF and/or INFORMATION about the depos attached Examiner's comment regarding REQUIREMENT R 		
Attachment(s) 1. ☐ Notice of References Cited (PTO-892)	5. Notice of Inform	nal Patent Application (PTO-152)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)	6. Interview Sumi	mary (PTO-413),
3. ⊠ Information Disclosure Statements (PTO-1449 or PTO/SB/0		il Date endment/Comment
Paper No./Mail Date <u>08/17/2004</u>	,.	
4. Examiner's Comment Regarding Requirement for Deposit		tement of Reasons for Allowance
of Biological Material	9. Other	

DETAILED ACTION

In the Amendment dated February 14, 2005, claims 1-13 are canceled, claim 15 is amended and new claims 24-31 are added are acknowledged. Accordingly, claims 14-31 are pending in this application.

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

The title of the invention has been changed as follows:

-SEMICONDUCTOR DEVICE INCLUDING A DIFFUSION LAYER---

Allowable Subject Matter

Claims 14-31 are allowed.

The following is an examiner's statement of reason for allowance:

Claims 14 and 16-23 are allowable over the prior art of record because the prior art of record does not teach or render obvious a semiconductor device comprises the diffusion layer comprising the first metal component and the second metal component, and in combination with all other features as recited in independent claim 14.

Application/Control Number: 10/919,402 Page 3

Art Unit: 2818

Claims 15 and 24-31 are allowable over the prior art of record because the prior art of record does not teach or render obvious a semiconductor device comprises the diffusion layer comprising the first metal component and the second metal component and the first electrode portion and the diffusion layer have a combined thickness in the range of 10 µm to 20 µm, and in combination with all other features as recited in independent claim 15.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh whose telephone number is (571) 272-1781. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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Art Unit: 2818

Page 4

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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03/24/05

Andy Huynh

andy Mey O

Patent Examiner

SHEET 1 OF 1

INFORM	ATIO]	ISCLOSURE (IN AN LICATION	CITATION	ATTY. DOCKET NO. SERIAL NO. Divisional of 10/307,450					
		VIII	LICATION		APPLICANT Yoshfumi NAKAMURA, et al.					
_		(P)	ГО-1449)		FILING DATE August 17, 2004	FILING DATE GROUP				
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EXAMINER'S INITIALS	CITE NO.	4	Document Number -Kind Code: (/ known)	Publication Date MM-DD-YYYY	Name of Patentee or Applic Document	ant of Cited		Pages, Columns, Lines, Where Passages or Relevant Figures		
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7		US	5,892,273	04/06/1999	lwasaki et a	1.			***************************************	
		US	2002/0108781A1	8/2002	Mune et al	**********				
	+	US	6,587,353	7/2003	Sumikawa et	al			*********	
	1	US	6,512,298	1/2003	Sahara et a	1				
	1	us	6,475,896	11/2002	Hashimoto)				
	1	US	6,414,390	7/2002	Nozawa					
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		j	P 2001-118956 A	04/27/2001	MATSUSHITA ELECTRONICS INDUSTRY			JAPAN (w/ English Abstract and Partial English Translation)		
		J	P 2001-291721 A	10/19/2001	NEC CORP.			JAPAN (w/ English Abstract and Partial English Translation)		
			JP 9- 129772 A	05/16/1997	TOSHIBA CORP.		_	JAPAN (w/ English Abstract and Partial English Translation)		
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			JP 10079362	3/11998	Fukazawa et al					
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EXAMINER'S INITIALS	CITE	= seria	de name of the author (in CA	PITAL LETTERS), titl	, Title, Date, Perlinent Pages, Etc. e of the article (when appropriate), -iasue number(s), publisher, city a	title of the	item (t	pook, magazine, journal, pre published.		
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SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

please issert -> This application is a DIV of 10/307, 450 filed 12/02/2002

BACKGROUND OF THE INVENTION

The present invention generally relates to a semiconductor device in which a metal wiring is formed so as to be electrically connected to an electrode of a semiconductor element and a part of the metal wiring is used as an external electrode, and a manufacturing method of the same. More particularly, the present invention relates to a semiconductor device having excellent junction reliability between a metal wiring and a ball electrode mounted to an external electrode portion of the metal wiring, and a manufacturing method of the same.

With recent reduction in size and improvement in functions of electronic equipments, an increasing number of input/output (I/O) pins is formed in a semiconductor element, and therefore the pitch of electrodes is reduced.

Especially in a CSP (Chip Size Package) type semiconductor device, electrodes of a semiconductor element are formed by a dry etching method in a diffusion process, whereas wiring electrodes of a substrate on which the semiconductor element is mounted are formed by a wet etching method in an assembling process. Accordingly, the pitch of the wiring electrodes of the substrate on which the semiconductor element is mounted is necessarily greater than that of the electrodes of the semiconductor element. In view of this, a semiconductor device is increasingly developed which deals with the difference between the electrode pitch of the semiconductor element and the wiring-electrode pitch of the substrate. In such a semiconductor device, metal wirings are formed so as to be electrically connected to the respective electrodes of the semiconductor element and a part of each metal wiring is used as an external electrode in order to increase the distance between the external electrodes.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address COMMISSIONER FOR PATENTS FO. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

BIBDATASHEET

CONFIRMATION NO. 6102

Bib Data Sheet									
SERIAL NUMBER 10/919,402	FILING DATE 08/17/2004 RULE	(CLASS 257	GRO	OUP ART 2818	ſ UNIT	D	ATTORNEY OCKET NO. 60188-932	
APPLICANTS									
Yoshifumi Naka	mura, Osaka, JAPAN;								
Nozomi Shimois Keiji Miki, Kyoto Kazumi Watase	Ryuichi Sahara, Osaka, JAPAN; Nozomi Shimoishizaka, Kyoto, JAPAN;Kazuyuki Kainou, Osaka, JAPAN; Keiji Miki, Kyoto, JAPAN; Kazumi Watase, Kyoto, JAPAN; Yasutake Yaguchi, Osaka, JAPAN;								
** CONTINUING DATA This application	A ************************************	* 12/02/2	002 PAT 6,784	1,557	<i>Oh</i>				
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Issue Classificat	ion

Application/Control No.	Applicant(s)/Patent under Reexamination
10/919,402	NAKAMURA ET AL.
Examiner	Art Unit
Andy Huynh	2818

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Index of Claims

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Examiner

Andy Huynh

Applicant(s)/Patent under Reexamination

NAKAMURA ET AL.

Art Unit

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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination						
10/919,402	NAKAMURA ET AL.						
Examiner	Art Unit						
Andy Huynh	2818						

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Class	Subclass	Date	Examiner							
257	669,770	11/12/2004	АН							
	673,674									
	676,688	,								
	692-697									
	728-752									
	735-739									
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257	\$.ccls.									
438	\$.ccls.									
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INTERFERENCE SEARCHED									
Class	Subclass	Date	Examiner						
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	693,737								
	738,773								
257/77	75,780	11/12/2004	АН						

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EAST		11/12/2004	АН

Docket No.: 060188-0932



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Customer Number: 20277

Yoshifumi NAKAMURA, et al.

Confirmation Number: 6102

Application No.: 10/919,402

Group Art Unit: 2818

Filed: August 17, 2004

Examiner: Huynh, Andy

For: SEMICONDUCTOR DEVICE INCLUDING A DIFFUSION LAYER (As Amended)

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee.

REQUEST TO CONSIDER REFERENCES AFTER CLOSE OF PROSECUTION AND BEFORE PAYMENT OF ISSUE FEE

The undersigned hereby requests consideration and entry of this Information Disclosure Statement and accompanying references under 37 CFR 1.97(d).

Please charge the processing fee under 1.17(p) of \$180.00 to Deposit Account 500417.

05/05/2005 SZEWDIE1 00000089 500417 10919402

01 FC:1806 180.00 DA



CERTIFICATION PARAGRAPH

The undersigned certifies that each item of information contained in this Information

Disclosure Statement was first cited in a communication from a foreign patent office in a

counterpart foreign application not more than three months prior to the filing of this Information

Disclosure Statement as described in 37 CFR 1.97(e)(1).

Each non-English language reference was cited in a corresponding foreign application office action and its relevance discussed therein. A copy of the foreign office action, together with an English language version thereof, is attached for the Examiner's information.

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Respectfully submitted,

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SHEET 1 OF 1

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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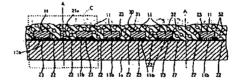
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权利要求书 3 页 说明书 8 页 附图页数 6 页

[54]发明名称 半导体晶片的制造方法、半导体芯片的制 造方法及 IC 卡

[57] 擠要

本发明的半导体晶片制造方法包括将多个电路元件 (41)与基板(1a)做成一体 的工序、在与电路元件(41)导 通的电极区(11b)上形成电极凸点(11)的工序、在基 板 (1a)规定位置形成划线或划线标记(21a)的工序、以及粘 贴各向异性导电膜(30) 以覆盖各电极凸点(11)及划线 或标线标记(21a)的工序。形成各电极凸点(11)的工序 与形成划线或划线标记(21a)的工序同时地进行。电极 凸点(11)及划线或划线标记(21a)最好由金形成。根据 这样的制造方法,即使是将各向异性电膜粘贴在形成 多 个电路元件的半导体晶片上的情况,也能够按照所希望 的那样分割电路元件。



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权 利 要 求 书

1. 一种半导体晶片的制造方法, 其特征在于, 包括

将多个电路元件与基板做成一体的工序,

在与各所述电路元件导通的电极区上形成电极凸点的工序,

在所述基板规定位置上形成划线或划线标记的工序,以及

粘贴各向异性导电膜以覆盖所述各电极凸点及所述划线或划线标记的工序,

将形成各所述电极凸点的所述工序与形成划线或划线标记的所述工序同时 地进行。

2. 如权利要求 1 所述的半导体晶片的制造方法, 其特征在于,

形成各所述电极凸点及所述划线或划线标记的所述工序包括

形成使各所述电极区的上面露出而保护各所述电路元件的绝缘层的工序,

在所述基板上的整个电路元件形成区域上形成阻挡金属层的工序,

形成使各所述电极区的形成区域相对应的部位及应该形成所述划线或划线标记的部位露出的光刻层的工序,

在未形成光刻层的部位形成金属层的工序, 以及

将光刻层及阻挡金属层进行剥离处理的工序.

- 3. 如权利要求1所述的半导体晶片的制造方法,其特征在于,各所述电极凸点及所述划线或划线标记由金形成.
 - 4. 一种半导体晶片, 其特征在于, 包括

在规定位置上形成划线或划线标记并将多个电路元件做成一体的基板,

在与各所述电路元件导通的电极区上与所述划线或划线标记同时形成的电极凸点,以及

粘贴在所述基板上以覆盖各所述电极凸点及所述划线或划线标记的各向异性导电膜.

- 5. 如权利要求 4 所述的半导体晶片, 其特征在于, 各所述电极凸点及所述划线或划线标记由金形成.
 - 6. 一种半导体芯片的制造方法, 其特征在于, 包括



将多个电路元件与基板做成一体的工序,

在与各所述电路元件导通的电极区上形成电极凸点的工序,

在所述基板规定位置上形成划线或划线标记的工序,

粘贴各向异性导电膜以覆盖所述各电极凸点及所述划线或划线标记的工序,以及

将利用以上工序形成的半导体晶片以所述划线或划线标记作为标记分割成 一个一个所述电路元件的工序,

将形成各所述电极凸点的所述工序与形成划线或划线标记的所述工序同时 地进行.

7. 如权利要求 6 所述的半导体芯片的制造方法, 其特征在于,

形成各所述电极凸点及所述划线或划线标记的所述工序包含

形成使各所述电极区的上面露出而保护各所述电路元件的绝缘层的工序,

在所述基板上的整个电路元件形成区域上形成阻挡金属层的工序,

形成使各所述电极区的形成区域相对应的部位及应该形成所述划线或划线 标记的部位露出的光刻层的工序,

在未形成光刻层的部位形成金属层的工序,以及

将光刻层及阻挡金属进行剥离处理的工序,

- 8. 如权利要求 6 所述的半导体芯片的制造方法, 其特征在于, 各所述电极凸点及所述划线或划线标记由金形成.
- 9. 一种半导体芯片, 其特征在于, 是通过将半导体晶片以所述划线或所述划线标记为标记分割成一个一个所述电路元件而得, 而所述半导体晶片包括:

在规定位置形成划线或划线标记并将多个电路元件做成一体的基板,

在与各所述电路元件导通的电极区上与所述划线或划线标记同时形成的电 极凸点,以及

粘贴在所述基板上以覆盖各所述电极凸点及所述划线或划线标记的各向异性导电膜.

- 10. 如权利要求 9 所述的半导体芯片, 其特征在于, 各所述电极凸点及所述划线或划线标记由金形成.
 - 11. 一种 IC 卡, 其特征在于,

是将半导体芯片、安装该半导体芯片的绝缘基板、以及与所述半导体芯片连



接的天线线圈埋入树脂制的卡内的 IC 卡,

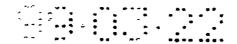
所述半导体芯片是通过将半导体晶片以所述划线或划线标记为标记分割成 一个一个所述电路元件而得,而所述半导体晶体包括:

在规定位置形成划线或划线标记并将多个电路元件做成一体的基板,

在与各所述电路元件导通的电极区上与所述划线或划线标记同时形成的电 极凸点,以及

粘贴在所述基板上以覆盖各所述电极凸点及所述划线或划线标记的各向异性导电膜.

12 如权利要求 11 所述的 IC 卡, 其特征在于, 各所述电极凸点及所述划线或划线标记由金形成。



说 明 书

半导体晶片的制造方法、半导体芯片的制造方法及 IC 卡

技术领域

本发明涉及将电路元件与基板作成一体的半导体晶片的制造方法、利用该方法制造的半导体晶片、由该半导体晶片制造半导体芯片的方法、利用该方法制造的半导体芯片、以及具有该半导体芯片的 IC 卡.

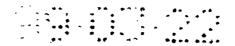
背景技术

图 7 表示以所谓片载板(Chip on board)方式在形成规定布线图形的绝缘基板 20 上安装半导体芯片 10 的状态的放大图. 作为该片载板方式的一个例子,是在形成向上方突出的导体凸点 21 的绝缘基板 20 与形成从其主面 10a 突出的电极凸点 11 的半导体芯片 10 之间夹入各向异性导电膜 30,然后将其加热压接,使导体凸点 21 与电极凸点 11 之间导通连接.

如图 7 所示,非常清楚,各向异性异电膜 30 具有在粘接性的树脂膜 31 内分散有导电粒子 32 的结构,导体凸点 21 与电极凸点 11 之间通过导电粒子 32 导电连接.另外,半导体芯片 10 的主面 10a 中未形成电极凸点 11 的区域与绝缘基板 20 之间,当各向异性导电膜 30 被加热、一旦熔融而固化时,就利用树脂膜 31 具有的粘接性而互相粘接。这时,由于导电粒子 32 分散于树脂膜 31 内处于互相分离的状态,因此该区域保持绝缘性能。这样在前述安装方法中,只要在夹有各向异性导电膜 30 的状态下按压半导体芯片 10 与绝缘基板 20 这样的简单操作,就能仅仅在必要部位实现电气导通,同时将半导体芯片 10 安装在绝缘基板 20 上。因而,与利用所谓芯片焊接及引线键合将半导体芯片 10 安装在绝缘基板 20 上的情况相比,可以说是非常简便的方法。

然而,在利用向各异性导电膜 30 将半导体芯片 10 安装在绝缘基板 20 上的情况下,必须准备与要安装的半导体芯片 10 的大小相应的、例如四边分别为几毫米左右的极小的各向异性导膜 30,数量是要安装的半导体芯片 10 的个数.而且,在半导体芯片 10 安装前,必须将各向异性导电膜 30 一片一片放在绝缘基板

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20 的导体凸点 21 上或粘贴在半导体芯片 10 的主面 10a. 这样,采用以往的各向异性导电膜 30 的安装方法,在安装半导体芯片 10 之前要准备的方面,其作业性很差.

因此提出了下面的方案,在半导体晶片上形成若干个要构成半导体芯片 10 的电路元件,在这样的半导体晶片状态下,将各向异性导电膜 30 粘粘在整个电路元件形成区域,当分割各电路元件时,各向异性导电膜 30 也同时被分割.即采用上述方法的优点是,各电路元件被分割成一个一个半导体芯片 10 的状态一,在其主面 10a 粘贴着各向异性导电膜 30,在安装半导体芯片 10 之前没有必要作特别的准备.

一般地,在半导体晶片上适当的地方形成所谓划线,以该划线作为标记利用 ① 金刚石划刀等分割成一个一个电路元件.划线在例如图形形成钝化膜等工序中同时形成.但是如上所述,各向异性导电膜 30 的结构是将大量导电粒子 32 分散在树脂膜 31 内,因此各向异性导电膜 30 具有乳白色的色彩.因而,对于半导体晶片上粘贴各向异性导电膜 30 的情况,必须透过乳白色的各向异性导电膜识别由SiN 等形成的银色划线.为此,划线难以进行视觉识别,难以分割电路元件得到所希望的半导体芯片 10.

发明概述

本发明的目的在于解决上述以往的问题,即使将各向异性导电膜粘贴在形成 多个电路元件的半导体晶片上,也能**够按照所希望**的那样分割电路元件。

为达到前述目的,在本发明中采取下述的技术手段.

即本发明第1形态的半导体晶片制造方法,其特征在于,包括将多个电路元件与基板作成一体的工序、在与各电路元件导通的电极区上形成电极凸点的工序、在基板规定位置上形成划线或划线标记的工序、以及粘贴各向异性导电膜以覆盖各电极凸点及划线或划线标记的工序,将形成各电极凸点的工序与形成划线或划线标记的工序同时地进行.

在用各向异性导电膜将半导体芯片安装在基板上,必须在与电路元件导通的电极区上形成从半导体芯片主面突出的电极凸点.该电极凸点是在形成包含电极区的规定布线图形后在电极区域上形成.在上述制造方法中,将形成各电极凸点的工序与形成划线或划线标记的工序同时地进行.即设有必要有形成划线或划线



标记的新的工序,在制造半导体晶片必须的工序中,能够在规定部位形成划线或划线标记。

在令人满意的实施形态中,包括形成各电极凸点及划线或划线标记的工序、 形成使电极区的上面露出而保护电路元件的绝缘层的工序、在基板上整个电路元 件形成区域上形成阻挡金属层的工序、使各电极区的形成区域相对应的部位及应 该形成划线或划线标记的部位暴露在外面形成光刻层的工序、在未形成光刻层的 部位形成金属层的工序,以及将光刻层及阻挡金属层进行剥离处理的工序。

在上述制造方法中,例如将形成光刻层的基板浸渍在含有金属离子的区域内,将阻挡金属层作为负电极加以通电,通过这样使未形成光刻层的区域生长金属层,同时形成各电极凸点及划线或划线标记。即形成光刻层时,只是在应该形成划线或划线标记的部位不形成光刻层,就使得与形成电极凸点同时也形成划线或划线标记。

在令人满意的实施形态中还包含,各电极凸点及划线或划线标记由金形成。

如上所述,一般以往的划线是与钝化同时形成,那种情况的划线是利用与钝化相同的材料例如 SiN 形成.因此,在粘贴各向异性导电膜的情况下,必须透过乳白色的各向异性导电膜识别银色的划线,划线难以进行视觉识别.与此不同,如上述令人满意的实施形态那样,通过利用金形成划线或划线标记,即使透明各自异性导电膜,也很容易对划线或划线标记进行视觉识别,也容易将半导体晶生按照所希望的那样分割成一个一个电路元件.

按照本发明上述第1形态的半导体晶片制造方法制造的半导体晶片包括在规定位置形成划线或划线标记并将若干个电路元件做成一体的基板、在与各电路元件导通的电极区上与划线或划线标记同时地形成的电极凸点。以及粘贴在基板上以覆盖各电极凸点及划线或划线标记的各向异性导电膜。

按照这种结构的半导体晶片,利用上述第1形态的制造方法是能够容易形成该划线或划线标记的.另外,当利用金形成划线或划线标记时,特别是透过粘贴的各向异性导电膜也能够容易对划线或划线标记进行视觉识别,当将半导体晶片分割成一个一个电路元件时能够很好地作为标记使用.

本发明第2形态的半导体芯片制造方法,其特征在于,包括将利用上述第1 形态的制造方法形成的半导体晶片以划线或划线标记作为标记分割成一个一个 电路元件的工序。



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如上所述,由于在半导体晶片上形成的划线或划线标记是容易进行视觉识别的,因此不用说,能够容易进行分割成一个一个电路元件的工序,而且能够按照 所希望的那样进行.

另外,在利用该制造方法制造的半导体芯片,在将半导体晶片分割成一个一个电路元件时,已经在其主面上粘贴了各向异性导电膜.因此在将半导体芯片安装在绝缘基板上时,没有必要重新准备数量为要安装的半导体芯片的数量、与要安装的半导体芯片的大小相应的例如四边为几毫米左右的极小的各向异性导电膜.而且没有必要在半导体芯片安装前将各向异性导电膜一片一片放置在绝缘基板的导体凸点上或粘贴在半导体芯片的主面上.这样的优点是,对于半导体芯片,在该半导体芯片安装前没有必要进行特别的准备.

本发明第 3 形态的 IC 卡, 其特征在于, 将利用上述第 2 形态的制造方法形成的半导体芯片安装在绝缘基板上, 在树脂制的卡内埋入装有半导体芯片的绝缘基板及与该半导体芯片连通的天线线圈.

附图简要说明

- 图 1 表示与本发明有关的半导体晶片的一例的整体平面图.
- 图 2 是沿图 1 的 [I II 线的剖视图.
- 图 3A 3F 表示半导体芯片制造工序的一例的主要部分剖视图.
- 图 4 表示与本发明有关的半导体芯片的一例的整体立体图.
- 图 5 表示将半导体芯片安装在绝缘基板上的状态的剖视图.
- 图 6 表示将半导体芯片与绝缘基板相互按压的状态的图.
- 图 7 表示在半导体芯片上形成的电极凸点与在绝缘基板上形成的导体凸点的导通连接状态的主要部分剖视图.
 - 图 8 表示与本发明有关的 IC 卡的一例的分解侧视图.

实施发明的最佳方式

下面参照附图对本发明的理想实施形态具体地进行说明.

如图 1 及图 2 所示, 半导体晶片 1 形成缺口圆片状, 电路元件 41 与例如由 硅等形成的基板 la 形成一体. 在基板 la 的表面, 在规定位置形成划线标记 2 la , 同时形成与电路元件 41 导通的电极区 11b , 在该电极区 11b 上利用电镀等形成



电极凸点 11. 另外, 在形成该电极凸点 11 及划线标记 21a 的基板 1a 上粘贴各向 异性导电膜 30 将其覆盖.

如图 1 虚线围住的部分所示,划线标记 21a 能够在例如形成电极区 11 时同时形成,例如将 4 个电路元件 41 作为一个单元,在各直角部分附近位置 1 形成该电路元件群 1a.另外,划线标记 21a 不限于图 1 所示的十字形,也可以形成直线形的划线.

下面参照图 3A ~ 3F 简单说明半导体晶片 1 的制造方法. 另外, 图 3A ~ 3F 各所示的剖面与图 2 中虚线 c 包围的部分对应.

首先,如图 3A 所示,将电路元件 41 与形成缺口圆片状的例如硅等制成的基板 1a 作成一体,将与该电路元件 41 导通的电极区 11b 与规定的布线图形同时形成.该电极区 11b 是通过例如溅射法或真空蒸镀等手段形成铝等金属薄膜层后再对该金属薄膜层施行刻蚀处理等形成.

接着的图 3B 所示,利用例如 CVD 法形成绝缘膜 22 即钝化膜,以保护电路元件 41 及布线图形等,而使电极区 11b 的上面露出,且覆盖电极区 11b 的边缘部分.

接着如图 3C 所示,形成阻挡金属层 23 以覆盖基板 1a 的整个电路元件 41 形成区域.该阻挡金属层 23 由例如将白金层层叠钛层而构成.这样的钛层形成 2000 埃左右,白金层形成 1000 埃左右.另外,该阻挡金属层 23 也还可以利用例如溅射法或真空蒸镀等手段形成.

接着如图 3D 所示,除了电极区 11b 上应该形成电极凸点 11 的区域及应该形成划线标记 21a 的区域以外,形成光刻层 24. 该光刻层 24 是通过例如在阻挡金属层 23 上层叠感光树脂层后再用规定的掩膜板进行曝光、对感光树脂层进行显影处理而形成。

接着如图 3E 所示,在未形成光刻层 24 的区域即应该形成电极凸点 11 及划线标记 21a 的区域形成例如由金等构成金属层 24A. 该金属层 24A 由例如电镀等形成.即在利用电镀形成金的金属层 24A 时,是通过将形成光刻层 24 的基板 1a 浸渍在含有金离子的溶液内、再接通阻挡金属层 23 作为负电极来进行。这种情况下,未形成光刻层 24 区域的阻挡金属层 23 上生成由金构成的金属层 24A,形成作为电极凸点 11 及划线标记 21a 的金属镀层 24a.

接着如图 3F 所示, 将光刻层 24 进行剥离处理, 使阻挡金属层 23 露出, 再

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通过对该阻挡金属层 23 进行试剂处理, 使绝缘膜 22 露出. 这样, 金属层 24A 就形成为电极凸点 11 及划线标记 21a. 即上述制造方法在形成光刻层 24 时, 仅仅在应该形成划线标记 21a 的部位不形成光刻层 24, 就能够也使划线标记 21a 与电极凸点 11 同时形成, 因而, 不需要划线标记 21a 形成用的新的工序, 在制造半导体晶片 1 必须的工序中, 能够在规定部位进行划线标记 21a.

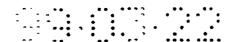
最后,将各向异性导电膜 30 粘贴在半导体晶片 1 的电路元件 41 形成面上,通过这样形成如图 1 及图 2 所示的半导体晶片 1.另外,各向异性导电膜 30 的粘贴,可以用树脂制的粘接剂等,另外也可以对各向异性导电膜 30 加热,利用各向异性导电膜 30 的粘接性来进行.

利用上述制造方法制造的半导体晶片 1 , 沿图 2 点划线所示划线进行切割, 分割成一个一个电路元件 41 , 形成如图 4 所示的一个一个半导体芯片 10 . 半导体晶片 1 的分割是用例如金刚石划刀等以划线标记 21a 作为标记来进行. 该操作,由于划线标记 21a 是由金形成,因此能够容易进行.即如后所述,各向异性导电膜 30 的结构是将导电粒子 32 分散在树脂膜 31 内,具有乳白色的色彩,而如果如上所述,利用金形成划线标记,则与利用 SiN 等形成的情况相比,是非常容易进行视觉识别,容易以该划线标记 21a 为标记按照所希望的那样将半导体晶片 1 分割成一个一个电路元件 41.

如上所述制造的粘贴有各向异性导电膜 30 的半导体芯片 10, 安装在绝缘基板上可用于各种用途. 下面参照图 5 至图 7 对半导体芯片 10 安装至绝缘基板 20 上的安装工序简单地进行说明. 图 5 表示将具有各向异性导电膜 30 的半导体芯片 10 放置在绝缘基板 20 上的状态的示意图, 图 6 表示将半导体芯片 10 与绝缘基板相互按压的状态的示意图, 图 7 是图 6 的主要部分放大图. 另外, 本实施形态中的半导体芯片 10 是将例如半导体存储器或电容器等作成一体, 这里说明的是如后所述的与天线线圈等一起埋入树脂制的卡内、即用于所谓 IC 卡的半导体芯片.

在说明半导体芯片 10 的安装工序前,首先简单说明各向异性导电膜 30 及安装半导体芯片 10 的绝缘基板 20.

如图 5 所示非常清楚,各向异性导电膜 30 具有在绝缘性的树脂膜 31 内分散有导电粒子 32 的结构.作为导电粒子 32,除了使用金属粒子之外,还可以使用例如在树脂制的粒子的表面镀镍的粒子或在镀镍上面再镀金的粒子。各向异性导



电膜 30 在自然状态下的厚度设定为例如 30 ~ $50\mu m$, 导电粒子 32 的粒径设定为例如 $5\mu m$.

应该安装半导体芯片 10 的绝缘基板 20 是利用具有绝缘性能的聚酰亚胺树脂等形成, 其表面形成铜薄膜后, 利用规定的图形刻蚀处理等形成包含天线线圈 20 a 的布线图形(参照图 8). 如图 8 所示, 在绝缘基板 20 的表面还形成导体区使布线图形导通, 该导体区外表进行镀镍及镀金, 露出形成导体 21 . 在这样露出形成导体 21 以外的绝缘基板 20 上的区域通常用聚酰亚胺树脂等绝缘膜覆盖. 如图 5 所示非常清楚, 由于导体 21 具有铜布线图形部分的厚度, 因此相对于绝缘基板 20 的表面呈略微突出形状.

如图 5 及图 6 所示,如上所述制造的具有各向异性导电膜 30 的半导体芯片 10 将各向异性导电膜 30 朝下,并进行定位使电极凸点 11 与绝缘基板 20 的导体 21 相对,同时以规定压力按压。这时,放置绝缘基板 20 的支持台 40 利用其内部 安装的加热器(未图示)加热至例如 180 ℃左右。

如图 6 所示, 半导体芯片 10 在绝缘基板 20 上的按压可以利用例如按压装置 50 进行.

各向异性导电膜 30 若在其所选择的区域沿厚度方向加热加压,则树脂成分软化并被压碎。在上述例子中,由于半导体芯片 10 的电极凸点 11 及绝缘基板 20 的导体凸点 21 都呈突出状,因此各向异性导电膜 30 中在相互相对的电极凸点 11 与导体凸点 21 之间所夹的区域有选择地被压碎,其结果如图 7 所示,树脂中分散的导电粒子 32 与电极凸点 11 及导体凸点 21 接触。各向异性导电膜 30 中的未被电极凸点 11 与导体凸点 21 所夹的区域,由于未被压碎或被压缩的程度较低,因此内部的导电粒子依然处于沿向各向异性导电膜 30 的厚度方向分散的状态。因而半导体芯片 10 与绝缘基板 20 的两表面中的电极凸点 11 及导体凸点 21 以外的区域之间仍然维持绝缘性能。

在本实施形态中,由于是在半导体晶片 1 的状态下粘贴各向异性导电膜并将其分割从而得到的半导体芯片安装在绝缘基板 20 上,因此在安装半导体芯片 10 时,没有必要再准备数量为应该安装的半导体芯片 10 的数量、与应该安装的半导体芯片 10 的大小相应的极小的各向异性导电膜 30.而且在安装半导体芯片 10 之前,没有必要将各自异性导电膜 30 一片一片地放在绝缘基板 20 的导体凸点 21 上或粘贴在半导体芯片 10 的主面 10a 上.这样的优点是,对于如上所述那样制造

的半导体芯片 10, 没有必要在该半导体芯片 10 安装前进行特别的准备.

如图 8 所示非常清楚,如上所述安装半导体芯片 10 的绝缘基板 20 最好是采用环氧树脂等热硬化树脂的连续自动成形成通过利用热可塑性树脂的喷射成形构成树脂封装而形成的模块.

如上所述那样形成树脂封装 4 构成模块化的 IC 模块 5 嵌入利用例如聚对苯二甲酸乙二醇酯树脂(下面叫做"PET")或聚氯乙烯(下面叫做"PVC")等相应于 IC 模块 5 的形状形成贯通孔 71 的树脂制的卡 70A 内. 另外, 在将 IC 模块 5 嵌入树脂制的卡 70A 内时,可以使用例如环氧树脂系的粘接剂等. 这样的嵌入了 IC 模块 5 的树脂制的卡 70A, 在其上下面粘贴由例如 PET 或 PVC 形成的其厚度为 0.05mm 左右的覆盖片 70,通过这样对 IC 卡 7 特别是对 IC 模块 5 加以保护.

另外,在上述实施形态中,安装半导体芯片的绝缘基板 20 是形成树脂封装的,但不限于此,也可以不形成树脂封装,而是将安装了半导体芯片 10 的绝缘基板 20 嵌入树脂制的卡 70A 内构成.

另外,在 IC 卡 7 中,天线线圈 20a 是在绝缘基板 20 上形成图形,但作为天线线圈 20a,也可以利用金属线材圈绕形成单独构成的线绕线圈。



说明书附图

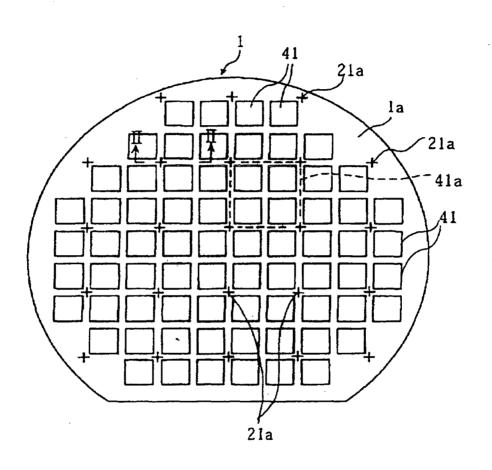
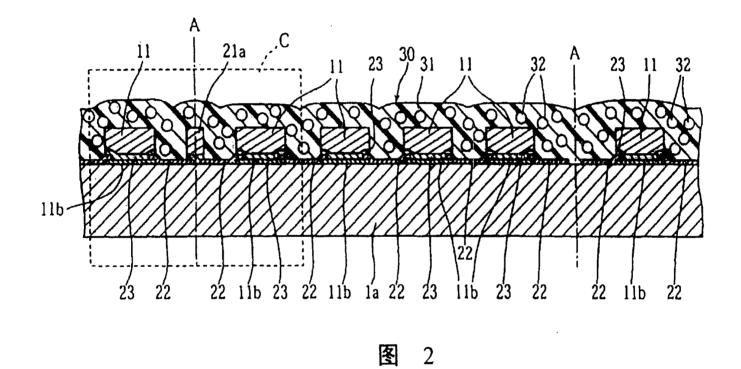
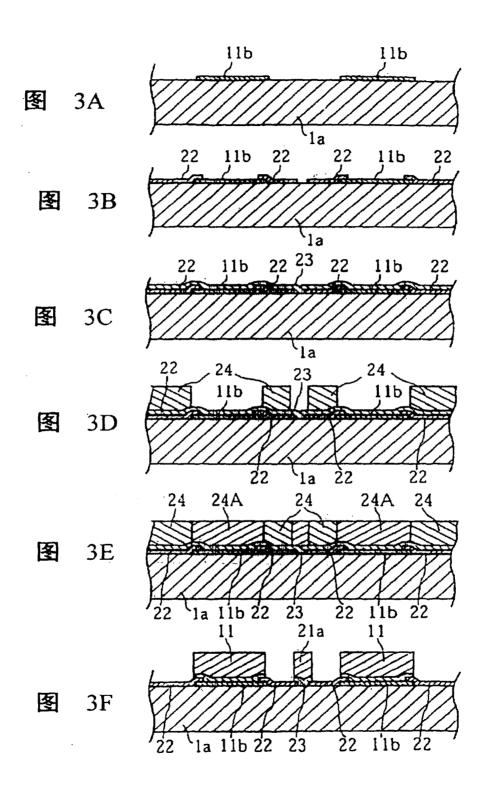
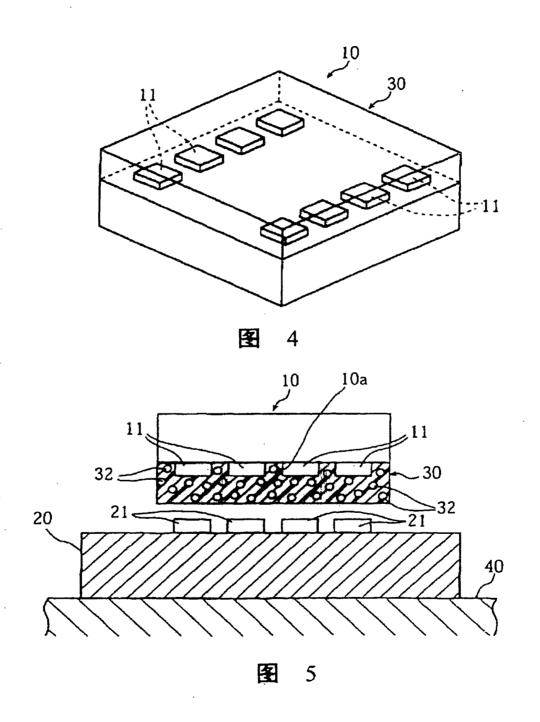
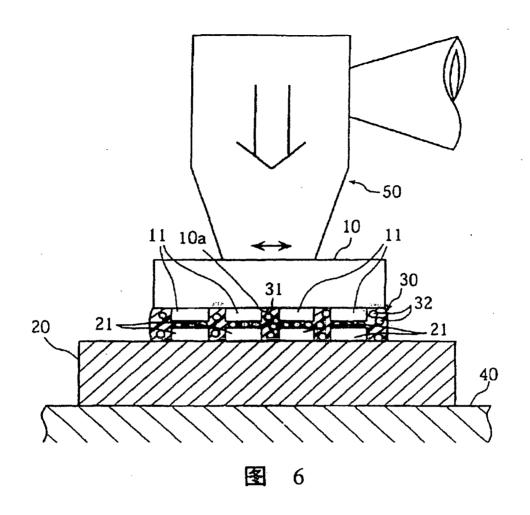


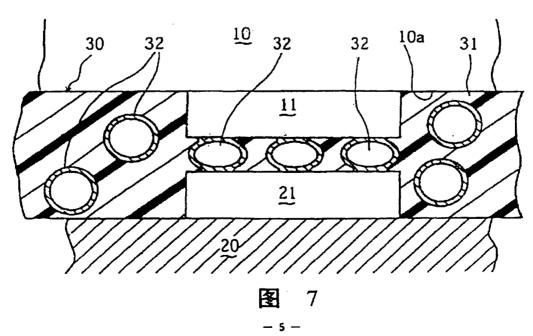
图 1

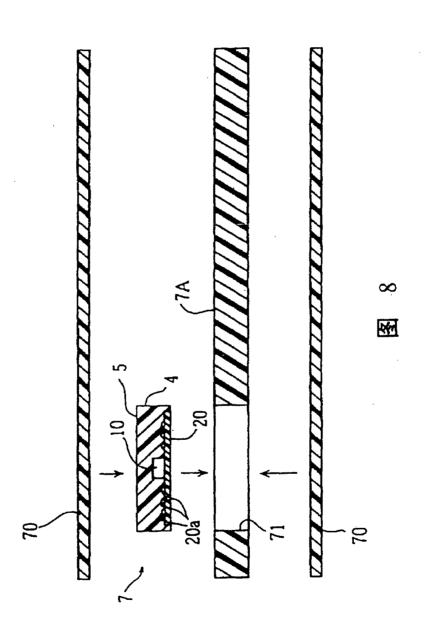












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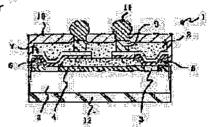
KITAMURA TOMOHITO FUKUYOSHI KENZO

(54) METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a method of manufacturing a semiconductor device (CSP) which has dispensed with the formation of wiring for power feeding for the plating and also with a metal mold for resin sealing.

SOLUTION: A method of manufacturing a semiconductor device, characterized by using a metal thin—film layer as a conductor for power feeding for plating at electrical plating, comprises at least a process for forming a first insulation layer to expose an electrode on the wafer surface where semiconductor elements are formed, a process for forming a metal thin—film layer connected electrically with an electrode, a process for forming a plating mask on the metal thin film layer, a process for forming a metal post with the electrical plating to the metal thin—film layer area exposed from the plating mask, a process for peeling the plating mask, a process to form a wiring layer by patterning the metal thin—film layer and a process for covering the side surface of metal past except for the end face of the metal past and for forming a



except for the end face of the metal past and for forming a second insulation layer closely covering the wiring layer and first insulation layer.

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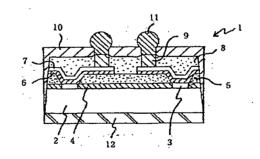
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(54) 【発明の名称】 半導体装置の製造方法

(57)【要約】

【課題】半導体装置(CSP)の製造にあたりメッキ給電用配線の形成を不要とし、また、樹脂封止に金型を不要とした半導体装置(CSP)の製造方法を提供する。 【解決手段】半導体素子が形成されたウェハー面上に電極を露出するよう第一の絶縁層を形成する工程と、電極と電気的に接続する金属薄膜層を一面に形成する工程と、電気メッキによりメッキマスクを形成する工程と、金属薄膜層上にメッキマスクを形成する工程と、当時である工程と、メッキマスクを形成する工程と、メッキマスクを割離する工程と、金属薄膜層をパターニングし配線層とする工程と、メタルポスト先端面を除くメタルポスト側面を被覆し、かつ、配線層および第一の絶縁層に密着被覆する第二の絶縁層を形成する工程とを少なくとも有し、電気メッキの際、金属薄膜層をメッキ給電用の導体としたことを特徴とする半導体装置の製造方法。



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【特許請求の範囲】

【請求項1】電極を有する半導体素子が形成されたウェハー面上に前記電極を露出するよう第一の絶縁層を形成する工程と、前記第一の絶縁層の形成面側に前記電極と電気的に接続する金属薄膜層を一面に形成する工程と、前記金属薄膜層上にメッキマスク用のレジストパターンを形成する工程と、電気メッキにより前記メッキマスクより露出した金属薄膜層部位にメタルポストを形成する工程と、前記メッキマスク用のレジストパターンを剥離する工程と、前記金属薄膜層をパターニングし配線層とする工程と、配線層および第一の絶縁層を被覆し、かつ、前記メタルポスト先端面を露出する第二の絶縁層を形成する工程とを少なくとも有し、前記メタルポスト形成のための電気メッキの際、前記金属薄膜層をメッキ給電用の導体としたことを特徴とする半導体装置の製造方法

【請求項2】前記第二の絶縁層は、表面をメタルポスト 先端面より低く、かつ、メタルポスト先端部近傍のメタ ルポスト側面は被覆するよう形成することを特徴とする 請求項1に記載の半導体装置の製造方法。

【請求項3】半導体素子が複数個面付けして形成されたウェハー上に前記請求項1または2に記載の製造方法にて第二の絶縁層の形成工程まで行った後、冷却用ヒートシンク材をウェハー裏面に貼り付ける工程と、第二の絶縁層形成面側よりウェハーとヒートシンク材との境界までダイシングを行い半導体素子を個片化する工程と、個片化された各半導体素子を覆うよう、かつ、メタルポスト先端面を露出するよう半導体素子を含めたウェハーに樹脂封止を行う工程と、半導体素子側面の封止樹脂を残すようヒートシンク材を含めてダイシングを行い個片化 30する工程とを少なくとも有することを特徴とする半導体装置の製造方法。

【請求項4】ヒートシンク材を含めてダイシングを行い 個片化する前にメタルポスト先端面に応力緩和機能を持 たせた外部接続用端子を配設することを特徴とする請求 項3に記載の半導体装置の製造方法。

【発明の詳細な説明】

[0001]

【発明の属する技術分野】本発明は、半導体素子を搭載 した半導体装置の製造方法に関わり、中でも特に、チップサイズパッケージ(CSP)と呼称される半導体装置 の製造方法に係わる。

[0002]

【従来の技術】近年、電子装置の小型化により、電子装置に組み込まれる(実装される)半導体装置は高密度での実装が行われており、半導体装置には小型化の要求が高まっている。この要求に答える技術として、チップサイズパッケージ(Chip Size Package、以下CSPと記す)と呼称される技術が提案されている。CSPは内部に組み込む半導体素子(ICチッ

プ)と略同等のサイズとすることができ、半導体装置の 小型化にとって有効な技術といえる。CSPの構造、形態は種々のものが提案されているが、以下に、一般的な CSPの形態を模式的に示す図面に基づき、CSPの説明を行う。

【0003】図7に示すように、CSP70内部に組み込 まれる半導体素子72にはアルミ等からなる電極73 (接続 用パッド)が形成されている。なお、一般的な半導体素 子72では、電極73を露出するパッシベーション膜74が形 成されている。ここで、CSP70とするにあたり、半導 体素子72上に電極73を露出するよう絶縁性樹脂等からな る第一の絶縁層75が形成される。また、第一の絶縁層75 上には電極73と接続するCu等の金属からなる配線パタ ーン77(配線層)が形成されており、配線パターン77上 に銅等からなるメタルポスト79を配設している。なお、 図7の例では、配線パターン77の下部に半導体素子72側 へのCu等の金属の流出を防止するため、メタルバリア 層76を形成している。次いで、配線パターン77および第 一の絶縁層75上にはメタルポスト79の先端面を露出する 第二の絶縁層78が形成されており、さらに、メタルポス ト79の先端面を露出するよう封止樹脂80にて樹脂封止が 行われ、CSP70となる。

【0004】なお、半導体装置の熱放散性を向上させるため、半導体素子裏面(電極および半導体集積回路が形成された面と反対面側の半導体素子面)に冷却用のヒートシンク材82を貼り付ける場合もある。

【0005】上述した構成を有するCSPの製造方法につき、以下に図面に基づき説明を行う。なお、以降に記す図面において、同一名称の部位には符号の記入を省略している。図4(a)に示すシリコン(Si)ウェハー上には半導体素子72が複数個面付けして形成されている(図中の矢線が各々1個の半導体素子72領域を示す)。各半導体素子72には外部との電気的接続を行う電極73(接続用パッド)が形成されている。また、各半導体素子72上には電極73を露出するパッシベーション膜74が予め形成されている。

【0006】次いで、CSPの製造にあたり、フォトリソグラフィ法等を用い、電極73を露出するよう第一の絶縁層75を半導体素子72上に形成する(図4(b))。次いで、シリコンウェハー上にメタルバリア層76および金属薄膜層87を積層成膜した後に(図4(c))、フォトエッチング法等によりメタルバリア層76および金属薄膜層87をパターニングし、所定のパターン形状とした配線層77を得る(図4(d))。

【0007】次いで図4(d)とした後、絶縁性樹脂等を素材として用い、フォトリソグラフィ法等により所定の配線層77部位を露出したメッキマスクを形成する(図5(a))。次いで、電気メッキによりメッキマスクより露出した配線層77部位にメタルポスト79を形成した後50メッキマスクを剥膜する(図5(b))。次いで、フォ

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トエッチング法等を用いて各半導体素子72間に形成された余分な配線層77部位を除去した後(図5(c))、フォトリソグラフィ法等により各半導体素子72にメタルポスト79の先端面を露出する第二の絶縁層78を形成する(図5(d))。

【0008】次いで、シリコンウェハーにダイシングを行い、半導体素子72を個片化する(図5(e))。次いで図5(e)で得られた個片化した半導体素子72に各々、半導体素子72を形成した面と反対面側のシリコンウェハー面にヒートシンク材82を貼り付けた後、個片化し 10た半導体素子72を金型を用いて各々封止樹脂樹80にて脂封止する(図6(a))。なお、樹脂封止にあたっては、ヒートシンク材82が露出するよう、また、メタルポスト79先端面が露出するよう樹脂封止が行われる。次いで、外部接続用端子81を各メタルポスト79に設置し、図6(b)および図7に示す半導体装置(CSP70)を得る。

【0009】上述した製造工程で得られた半導体装置 (CSP70)では、外部(例えば実装基板)と電極73と の電気的接続および、外部と半導体装置との固定は外部 接続用端子81にて行われるもので、外部接続用端子81と しては半田(ハンダ)ボール等が用いられる。また、電 極73と接続する配線層77は第一の絶縁層75上に形成さ れ、配線層77は電極73とメタルポスト79との電気的接続 を行う。なお、第一の絶縁層75および第二の絶縁層78は 電気的絶縁を行う他に、半導体装置を実装した後に半導 体装置と実装基板との熱膨張率の差等により生じた応力 が半導体装置にかかった際、この応力を緩和する機能を も有するものであり、この機能により半導体装置にクラ ック等が生じることを防止しようとするものである。 【0010】また、通常は、半導体装置 (CSP) の熱 放散性を向上させるために半導体素子にヒートシンク材 82が貼り付けられる。

【0011】上述したように、半導体素子72が複数個面付して形成されたシリコン(Si)ウェハーに一括して第二の絶縁層78の形成まで行い、その後、ダイシングを行い個々の半導体素子72に個片化することで、CSP70は半導体素子72と略同等のサイズとすることができる。【0012】

【発明が解決しようとする課題】ここで、上述したCS 40 Pの製造方法では、以下の問題点が有るといえる。まず、所定のパターンを有する配線層を形成した後に電気メッキでメタルポストを形成しているため、電気メッキのためのメッキ給電用配線が必要になりCSPの製造工程が煩雑になり不経済になるという問題である。なぜならば、電極とメタルポストとの電気的接続のための配線層に加えて、メタルポスト形成のためのメッキ給電用配線が別途必要となり、このメッキ給電用配線はメタルポスト形成後は不要になるため除去する必要が有るためである。すなわち、最終的な製品としては不要であるメッ 50

キ給電用配線を形成する分、製造工程が煩雑になり不経済になる。

【0013】また、上記メッキ給電用配線を形成する領域が余分に必要となる分、配線層のパターン設計及びパターン配置に制約を受けることになる。さらに、メタルポストの形成部位は複数箇所あるものでメッキ給電用配線は複数本必要となるが、引回しにより各メッキ給電用配線の長さは相違することになる。このため、長さの相違に起因する電気的抵抗の相違等で、電気メッキで形成されるメタルポストの高さはバラツキが生じやすい。さらには、メッキ給電用配線の断線によりメタルポストが形成されない(メッキが不着されない)等の不具合も生じる場合もあり、外部との電気的接続不良が生ずる等、半導体装置の電気的接続性の信頼が低下する要因ともなっていた。

【0014】さらには、半導体素子を個片化する前に、ウェハー状態のまま樹脂封止した場合、半導体素子の保護層である封止樹脂は半導体素子上面に厚く、また、半導体素子側面には薄く形成されやすい。このため個片化し半導体装置とした後は、半導体装置の側面部から吸湿を生じやすく気密性が不十分といえ、パッケージの信頼性が低いものになるといえる。ちなみに、本発明者らが、従来の半導体装置(CSP)を実装基板に実装後、実装基板に温度サイクル試験(-40℃から+1・25℃まで温度を変化させて1サイクルとし、この温度変化を複数回繰り返す試験)を行ったところ、200サイクル~400サイクルの比較的早い時期にパッケージクラックが発生したものである。

【0015】また、従来の半導体装置(CSP)の製造方法では、個片化した各半導体素子を金型を用いて一個ずつ樹脂封止するため製造に時間が掛かり、製造費用も掛かるものであった。

【0016】本発明は上述した問題点に鑑みなされたもので、半導体装置(CSP)の製造にあたりメッキ給電用配線の形成を不要とし、また、樹脂封止に金型を不要とした半導体装置(CSP)の製造方法を提供し、それによりパッケージクラック、電気的接続不良の無い信頼性の高い半導体装置(CSP)を安価に提供することを目的としている。

0 [0017]

【課題を解決するための手段】本発明者らは、上記の課題を達成するために鋭意検討を行い本発明に至ったものである。すなわち請求項1においては、電極を有する半導体素子が形成されたウェハー面上に前記電極を露出するよう第一の絶縁層を形成する工程と、前記第一の絶縁層の形成面側に前記電極と電気的に接続する金属薄膜層を一面に形成する工程と、前記金属薄膜層上にメッキマスク用のレジストパターンを形成する工程と、電気メッキにより前記メッキマスクより露出した金属薄膜層部位にメタルポストを形成する工程と、前記メッキマスク用

のレジストパターンを剥離する工程と、前記金属薄膜層をパターニングし配線層とする工程と、前記メタルポスト先端面を除くメタルポスト側面を被覆し、かつ、配線層および第一の絶縁層に密着被覆する第二の絶縁層を形成する工程とを少なくとも有し、前記メタルポスト形成のための電気メッキの際、前記金属薄膜層をメッキ給電用の導体としたことを特徴とする半導体装置の製造方法としたものである。

【0018】また請求項2においては、前記第二の絶縁層は、表面をメタルポスト先端面より低く、かつ、メタルポスト先端部近傍のメタルポスト側面は被覆するよう形成することを特徴とする請求項1に記載の半導体装置の製造方法としたものである。

【0019】さらに請求項3においては、半導体素子が複数個面付けして形成されたウェハー上に前記請求項1または2に記載の製造方法にて第二の絶縁層の形成工程まで行った後、冷却用ヒートシンク材をウェハー裏面に貼り付ける工程と、第二の絶縁層形成面側よりウェハーとヒートシンク材との境界までダイシングを行い半導体素子を個片化する工程と、個片化された各半導体素子を覆うよう、かつ、メタルポスト先端面を露出するよう半導体素子を含めたウェハーに樹脂封止を行う工程と、半導体素子側面の封止樹脂を残すようヒートシンク材を含めてダイシングを行い個片化する工程とを少なくとも有することを特徴とする半導体装置の製造方法としたものである。

【0020】さらにまた、請求項4においては、ヒートシンク材を含めてダイシングを行い個片化する前にメタルポスト先端面に応力緩和機能を持たせた外部接続用端子を配設することを特徴とする請求項3に記載の半導体30装置の製造方法としたものである。

[0021]

【発明の実施の形態】以下に、本発明の実施形態につき図面に基づき説明する。図2および図3は本発明の半導体装置の製造方法の実施形態の一例を工程順に示す図面である。図2(a)は、従来通りシリコン(Si)ウェハー上に複数個面付けして形成された半導体素子2を示す(図2(a)中の矢線が各半導体素子2の領域を示す)。各半導体素子2には電極3が形成されており、また、電極3を露出するようパッシベーション膜4が形成 40されている。

【0022】本発明の半導体装置の製造方法においては、まず、図2(b)に示すように、電極3を有する半導体素子2が形成されたシリコンウェハー面上に前記電極3を露出するよう第一の絶縁層5を形成する。

【0023】次いで、図2(c)に示すように、第一の 絶縁層5の形成面側に半導体素子2に形成された電極3 と電気的に接続する金属薄膜層17を一面に形成する。 なお、金属薄膜層17は、Cu(銅)、Ag(銀)等の 電気良導体金属の単層構成であっても良く、図2(c) に示すように、Cr、TiW、TiN等のメタルバリア層6上にCu(銅)、Ag(銀)等の電気良導体金属からなる金属薄膜層17を積層した多層構成としても構わない。また、金属薄膜層17の形成手段は、スパッタ法、真空蒸着法、イオンプレーティング法、CVD法、ゾルゲル法、無電解メッキ法等があげられ、適宜選択して構わない。

【0024】次いで、メタルポストを形成すべき金属薄

膜層17部位を露出する、電気メッキの際にメッキマスクとなるレジストパターンを金属薄膜層17上に形成し、図2(d)を得る。次いで、金属薄膜層17をメッキ給電用配線として電気メッキを行い、メッキマスクより露出した金属薄膜層17部位にメタルポスト9を形成した後にメッキマスクを剥膜し、図2(e)を得る。【0025】次いで、シリコンウェハー上に一面に形成された金属薄膜層17およびメタルバリア層6をフォトエッチング法等を用いパターニングし、所定のパターン形状とした配線層7とする(図2(f))。すなわち、本発明の半導体装置の製造方法においては、所定のパターン形状とした配線層7を得る前に、全面に一様に形成された金属薄膜層17をメッキ給電用の導体として利用するものである。

【0026】これにより、従来の半導体装置の製造方法で必要とされた、最終的に不要となるメッキ給電用配線の形成および、メッキ給電用配線の除去を不要としたものであり、製造工程の簡略化が可能となる。また、シリコンウェハー上全面に一様にメッキ給電用配線となる金属薄膜層17を形成しているためメッキ給電用配線の断線が生じにくく、メタルポスト9の不着やメタルポスト9の高さのバラツキを防止でき、信頼性の高い半導体装置を低コストで製造することが可能となる。

【0027】次いで、本発明の半導体装置の製造方法では、図2(f)に示す所定のパターン形状とした配線層7を形成した後、配線層7および第一の絶縁層5を被覆し、かつ、前記メタルポスト9先端面を露出する第二の絶縁層8を形成し、図3(a)を得る。

【0028】ここで、第二の絶縁層8は図1および図3 (a)に示すように、第二の絶縁層8の表面をメタルポスト9先端面より低く形成し、かつ、メタルポスト9先端部近傍のメタルポスト9の側面を被覆するよう形成している。すなわち、メタルポスト9先端より下部(シリコンウェハー方向)において第二の絶縁層8とメタルポスト9との密着性を優先させる構造としている。これにより、第二の絶縁層8とメタルポスト9との密着性が補強され、それにともない、メタルポスト9と配線パターン7との接続強度も向上しメタルポスト9と配線パターン7との断線が防止できる。

【0029】また、後述するように半導体装置においては封止樹脂による樹脂封止が必要となるが、第二の絶縁層8の表面がメタルポスト9先端面の高さと同等もしく

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は高い場合、第二の絶縁層8上に形成される封止樹脂の表面の高さはメタルポスト9先端面より高いものとなる。このため、封止樹脂の開口部より露出したメタルポスト9先端面上に外部接続用端子(例えばハンダボール)を配設しようとしても封止樹脂で邪魔をされ、メタルポスト9先端面と外部接続端子との間に隙間が生じる等、メタルポスト9と外部接続端子との電気的接続不良が生じる

【0030】しかるに図3(a)に示すように、メタルボスト9の側面を被覆する部位を除く第二の絶縁層8の 10 高さをメタルポスト9先端面の高さより低くすれば、封止樹脂表面とメタルポスト9先端面とを近くすることが出来、封止樹脂が邪魔をしないため、外部接続用端子を配設する際にメタルポスト9先端面と外部接続端子との間に隙間が生じず、メタルポスト9と外部接続端子との電気的接続不良を防止できる。また、第二の絶縁層8を薄く形成することで、比較的高価な材質を用いる第二の絶縁層8の使用量を減らすことが出来、半導体装置の製造コストを下げることが可能となる。

【0031】また、メタルポスト9の先端部近傍の側面 20 を除き第二の絶縁層8の高さをメタルポスト9先端面の高さより低い位置になるように形成するには、絶縁性樹脂を感光性のものとし、塗布、パターン露光、現像等を行い不要部の絶縁性樹脂の除去を行うフォトリソグラフィー法を用いることが望ましい。

【0032】第2の絶縁層8とする絶縁性樹脂の塗布に は、スピンコート法、カーテンコート法、スクリーン印 刷法、スリットアンドスピンコート法等の公知の塗布手 段を用いることで構わない。しかし、メタルポスト9の 先端部近傍の側面を除き第二の絶縁層8表面の高さをメ タルポスト9先端面の高さより低い位置になるように形 成することを考慮した場合、スピンコート法が望まし い。すなわち、メタルポスト9の形成後にスピンコート 法にて絶縁性樹脂の塗布を行えば、余分な絶縁性樹脂は 半導体素子の外へ除去される。このため塗布条件を適宜 設定することで、メタルポスト9の先端部近傍の側面部 位を除いた領域ではメタルポスト9先端面の高さより薄 い膜厚にて絶縁性樹脂を塗布でき、かつ、メタルポスト 9の先端部近傍の側面にも絶縁性樹脂を塗布できること になる。なお、メタルポスト9先端面に残った絶縁性樹 脂の除去は、前述したフォトリソグラフィー法の他に、 レーザー、ドライエッチング、逆スパッタ等で選択的に 除去することであっても構わない。

【0033】次いで、図3(a)に示すように第二の絶縁層8を形成した後、本発明の半導体装置の製造方法においては、冷却用ヒートシンク材12を半導体素子を形成した面と反対面側のシリコンウェハー面に貼り付ける。なお、冷却用ヒートシンク材12の素材としては、Ag、Cu、Al等の金属、または、これらの合金等の熱導伝率の高いものが使用可能であり、その中でも特に50

Cu、Cu合金がコスト的に安く、かつ、熱導伝率が高く好ましい。次いで、冷却用ヒートシンク材12を貼り付けた後にダイシングを行うことで、第二の絶縁層8の形成面側よりシリコンウェハーとヒートシンク材12との境界まで切れ目を入れ、半導体素子2を含めてシリコンウェハーを個片化し図3(b)を得る。このとき、個片化された各半導体素子2はダイシングの行われなかった冷却用ヒートシンク材12上に保持、固定される。

【0034】次いで、個片化された各半導体素子2間 (切れ目)を充填し、かつ、メタルポスト9先端面を露出するようシリコンウェハーウェハー上に一様に封止樹脂10にて樹脂封止を行い、図3(c)を得る。なお、樹脂封止はスピンコート法にてメタルポスト9先端面を含めシリコンウェハー上全面に一様に封止樹脂10を塗布した後、メタルポスト9先端面上の樹脂を除去することが簡便で望ましい。また、メタルポスト9先端面上の樹脂の除去は、封止樹脂10を感光性樹脂とし、塗布、パターン露光、現像等を行い不要部の除去を行うフォトリソグラフィー法を用いることが簡便で望ましい。

【0035】次いで、メタルポスト9先端面に外部接続 用端子11を配設し、図3(d)を得る。次いで、各半 導体素子2側面の封止樹脂10を残すようヒートシンク 材12を含めてダイシングを行うことで各半導体素子2 を個片化し、図1および図3(e)に示す半導体装置 (CSP1)を得る。

【0036】CSP1に代表される半導体装置においては、パッケージの信頼性向上、機械的強度向上のため、半導体素子の外周に樹脂封止が必要である。前述したように、従来の半導体装置(CSP)の製造方法では、半導体素子72を金型を用いて1個ずつ樹脂封止を行っていた。このため、半導体素子72の形状が変わる毎に、言い換えれば半導体装置の品種毎に新たな金型を必要としていた。金型の作成は非常にコストが掛かるものであり、半導体装置の品種毎に高価な金型を作ることは不経済といえる。また、金型を用いた樹脂封止では、半導体素子72の上面には封止樹脂80が厚く、半導体素子72側面の封止樹脂80は薄く形成されやすく、半導体素子72側面の機械的強度が弱く、また、気密性にも欠け、信頼性が低いものであった。

【0037】しかるに、本発明の半導体装置の製造方法では、樹脂封止に金型を用いない。すなわち、図3 (c)に示すように、冷却用ヒートシンク材12上に保持、固定された個片化された各半導体素子2の間(切れ目)を充填し、かつ、メタルポスト9先端面を露出するようシリコンウェハー上に一様に封止樹脂10にて樹脂封止を行うものである。さらに、半導体素子2の最終的な個片化は、各半導体素子2側面の封止樹脂10を残すよう冷却用ヒートシンク材12を含めたダイシングで行っている。

【0038】すなわち、本発明の半導体装置の製造方法では、個片化された半導体素子を金型を用い1個ずつ樹脂封止を行うのではなく、冷却用ヒートシンク材12上で保持、固定された各半導体素子2に一括して樹脂封止を行い、しかる後、冷却用ヒートシンク材12を含めてダイシングを行い最終的に個片化するものである。これにより、樹脂封止の際の高価な金型の使用を不要とすることで製造コストの低減が可能となり、また、樹脂封止に要する時間の短縮も可能となる。また、金型を用いることなく樹脂封止を行うため、半導体素子と封止樹脂との密着性も良くなり、半導体装置としての信頼性、機械的強度を向上できる。

【0039】次いで、半導体装置には外部(例えば、実装用基板)との固定、電気的接続を行うために外部接続用端子11を配設するが、本発明の製造方法においては外部接続用端子11に応力緩和機能を持たせたことを特徴としている。

【0040】この点につき説明を行う。半導体装置を実装基板等に実装すると、シリコン等で形成される半導体素子(例えば、熱膨張率が約3ppm程度)と実装基板 20 (例えば、エポキシ系樹脂からなるプリント基板:熱膨張率40~200ppm程度、但してg点以上では200ppmを超える)との熱膨張率の差で生じるストレス(応力)が半導体装置にかかる。このストレス(応力)により半導体装置にクラックや内部断線が発生し、半導体装置の信頼性を低下させていた。

【0041】しかるに、本発明の半導体装置の製造方法では、メタルポスト上に配設する外部接続用端子11に応力緩和機能を持たたものであり、半導体装置と実装基板との熱膨張率の差で生じるストレス(応力)は応力緩和機能を有する外部接続用端子11で緩和され、半導体装置(CSP1)にクラックや断線が発生することを防止できる。応力緩和機能を有する外部接続用端子11の例としては、図8もしくは図9に示すように、外部に開放された中空部を有する保持体15の表面に導電性材料16を配設したものがあげられる。なお、図8は応力緩和機能を有する外部接続端子11の一例を側面から見た図(すなわち外部接続端子11を半導体装置に配設した際に半導体装置の側面より見た図)であり、図9は図2のA-A、線における断面を上方から見た(実装基板 40に実装した際に実装基板側から見た)図である。

【 O O 4 2】中空とした保持体15は柔構造のため、外部接続端子11と接続した実装基板が相当量の熱伸縮を繰り返しても、発生したストレス(応力)を吸収し応力を緩和することができる。これにより、絶縁層および封止樹脂と外部接続端子11との界面でのクラックの発生、および、クラックによる断線を防止できる。保持体15の材質は、耐熱性を有するエンジニアプラスチックが好ましい。ここでエンジニアプラスチックとは、耐熱性が100℃以上、強度が49MPa以上、曲げ弾性率50

が2.4Gpa以上のプラスチックのことをいうものである。上記条件を満たす材質として、ポリイミド、ポリアミドイミド、ポリエーテルイミド、熱可塑性ポリイミド、ポリアミド、ポリアセタール、ポリブチレンテレフタレート、ポリエチレンテレフタレート、ポリスチレン・ボリフェニレンサルファイド、ポリエーテルケトン、液晶ポリマー、ポリエーテルニトリル、フッ素樹脂、ポリカーボネート、変成ポリフェニレンエーテル、ポリサルフォン、ポリエーテルサルホン、およびポリアリレート等の樹脂が挙げられる。また、保持体15の材質は上記エンジニアプラスチックのポリマーアロイであっても構わない。

【0043】次いで、導電性材料16は、外部と固定を行い、かつ、電気的接続が可能でなければならず、このような条件を満たす導電性材料16としては、

②グラファイト、カーボンもしくは金属微粒子分散体、 ②金、銀、銅、アルミニウム、もしくはニッケルの単 体、または前記金属を二種類以上含む合金、

◎錫もしくは鉛を主成分とする低融点合金、が挙げられ、

上記①~②のうちから選択することが望ましい。

【0044】上記した低融点合金としては、水銀、ガリウム、またはインジウム等の金属を用いたものが挙げられるが、製造コスト等の観点から、錫もしくは鉛を主成分としたハンダ(半田)合金が好ましい。ハンダ合金としては、共晶ハンダや鉛の比率を高めた高融点ハンダが適用でき、また必要に応じてビスマス、カドミウム、アンチモン、亜鉛、マンガン、インジウム、錫、銀等を添加しても構わない。また、図8および図9の例に示すように、保持体15と導電性材料16との接着性を向上させるために導電性材料16の配設に先立ち、保持体15の表面に接着層27を形成しても構わない。

【0045】なお、保持体15の中空部を外部雰囲気に開放したものとし、外部雰囲気の空気(エアー)が自由に中空部に出入り可能な状態にしておけば、保持体15に含まれた水分が外部雰囲気に放出され樹脂の劣化が防止できる。また、保持体15の中空部が外部雰囲気に開放されていれば、実装時に加熱された際に、保持体15中の水分が蒸発した水蒸気や膨張した空気は外部雰囲気に放出され、保持体15に破裂が生じることを防止できる。さらに、実装後に半導体装置に熱が加わても、保持体15中の水分が外部雰囲気に放出されることになり、保持体15の破裂や劣化を防止できる。

【0046】また、半導体装置(CSP1)の使用される環境が熱変化の少ないものであり、半導体装置と実装 基板との間で生じる応力が小さいものであれば、保持体 15の形状は中空部を有しない円筒状であっても構わない。

[0047]

) 【実施例】以下に、本発明の実施例につき説明する。

〈実施例〉図2(a)は、従来公知の手段により得られた半導体素子2である。半導体素子2はシリコンウェハーを基材とし、アルミからなる電極3が形成されており、また、半導体素子2上には電極3を露出するようパッシベーション膜4が形成されている。また、図2(a)では説明の都合上、一枚のシリコンウェハー上に複数個面付けして形成されたうちの2箇所の半導体素子2を図示している。

【0048】次いで、シリコンウェハー上に感光性ポリイミド(旭化成工業(株)製、商品名「パイメル」)を 10 塗布した後、パターン露光、現像等を行う公知のフォトリソグラフィー法を用い、各半導体素子2上に電極3を露出する膜厚約10μmの第一の絶縁層5を形成した(図2(b))。次いで、第一の絶縁層5を形成した面側に、メタルバリア層6としてTiN層(膜厚200nm)を、次いで金属薄膜層17としてCu層(膜厚500nm)を、次いで金属薄膜層17としてCu層(膜厚500nm)を、各々スパッタ法を用い一括して積層形成した(図2(c))。

【0049】次いで、スピンコート法にて金属薄膜層17上に一括して膜厚20μmの感光性レジスト層を塗布、形成した後、公知のフォトリソグラフィ法を用い、メタルポストを形成する金属薄膜層17部位を露出したメッキマスクを形成した(図2(d))。次いで、電解メッキ法にてメッキマスクより露出した金属薄膜層17部位にCu(銅)からなるメタルポスト9を形成した後、メッキマスクを剥離した(図2(e))。なお、このとき金属薄膜層17をメッキ給電用の導体として用いた。

感光性レジスト層を形成した後、公知のフォトエッチング法を用いて金属薄膜層17にパターニングを行い、所 30 定のパターン形状とした配線層7を形成した(図2 (f))。次いで、図2(f)を得た後、配線層7を形成した面側に一括して感光性ポリイミド(旭化成工業(株)製、商品名「パイメル」)をスピンコート法にて塗布し、膜厚10μmの感光性ポリイミド層を形成した。次いで、公知のフォトリソグラフィー法にてメタルポスト9上の感光性ポリイミドを除去し第二の絶縁層8

【0050】次いで、スピンコート法にて膜厚1μmの

【0051】次いで、半導体素子2を形成した面とは反対面側であるシリコンウェハー裏面にシリコンウェハーと略同一サイズとした冷却用ヒートシンク材12を貼り付けた。なお、冷却用ヒートシンク材12の材質はCu(銅)を用いた。次いで、各半導体素子2の境界にダイシングを行い切れ目を入れ、半導体素子2を個片化した。なお、ダイシングによる切れ目はシリコンウェハーに入れ、冷却用ヒートシンク材12には入れていない(図3(b))。

【0052】次いで、スピンコート法にてダイシングで 形成された切れ目にも充填するよう感光性を有する封止 樹脂10をシリコンウェハー表面に塗布し樹脂封止を行 50

った後、公知のフォトリソグラフィー法にてメタルポス ト9先端上の封止樹脂10を除去した(図3(c))。 次いで、メタルポスト9上に外部接続端子11を載置し た(図3(d))。本実施例で用いた外部接続用端子1 1は応力緩和機能を持たせたもので、前述した図8およ び図9に示すように熱可塑性ポリイミドからなる中空の 保持体15の表面に導電性材料16として共晶ハンダを 形成しており、以下に記す工程で作成した。すなわちま ず、内径0.15mm、肉厚50μmの中空の熱可塑性 ポリイミドチューブを長尺状で購入した。次いで、チュ ーブ表面(外側面)に金属クロムと銅を順次積層成膜し た。金属クロムおよび銅は導電性材料を積層する際に接 着層27としての役目を持たせたもので、金属クロムの 膜厚を0.2μm、銅の膜厚を0.4μmとなるようス パッタリングにより成膜した。接着層17を形成した後、 導電性材料16として膜厚約20μmの共晶ハンダをメッ キ形成した。次いで、共晶ハンダの形成後、長尺状の熱 可塑性ポリイミドチューブを各々長さ約0.3mmにカ ッティングし、図8および図9に示す、本実施例で用い た外部接続用端子11とした。

【0053】次いで、図3(d)に示すように外部接続端子11を載置した後、半導体素子2の側面の封止樹脂を残すよう冷却用ヒートシンク材を含めたダイシングを行うことで最終的に個片化を行い、各々独立した半導体装置(CSP1)を得た(図3(e))。

【0054】上記実施例で得られた半導体装置(CSP1)をプリント基板に実装後、プリント基板に熱サイクル試験(-45℃~+125℃)を行ったが、1000回のサイクル試験後も半導体装置にはパッケージクラックや内部断線等の不具合は生じなかった。

【0055】以上、本発明の一実施例につき説明したが、本発明の実施の形態は上述した図面および記述に限定されるものではなく、本発明の趣旨に基づき種々の変形を行っても構わないことはいうまでもない。

【0056】例えば、使用する素材、形成する膜の膜厚等の製造条件は半導体装置の仕様に合わせ適宜設定して構わない。また、応力緩和機能を有する外部接続用端子として、Pbの含有率の多い高融点半田、または、Cu等の延性を有する金属を核とした多層構成の半田ボールを用いても構わない。

[0057]

【発明の効果】本発明の半導体装置の製造方法によれば、所定のパターン形状とした配線層を得る前に、ウェハー上全面に一様に形成された金属薄膜層をメッキ給電用の導体として利用するものである。これにより、従来の半導体装置の製造方法で必要とされた、最終的に不要となるメッキ給電用配線の形成および、メッキ給電用配線の除去を不要としたものである。また、樹脂封止の際に高価な金型の使用も不要としており、本発明の半導体装置の製造方法を用いることで、半導体装置の製造に要

を得た(図3(a))。

する費用を低減できる。また、従来の製造方法で生じていた、メッキ給電用配線の長さの相違によるメタルポストの高さのバラツキや、メタルポストの形成不良(メッキの不着)という電気的接続不良を防止できる。

【0058】また、メタルポスト上面を除いて封止樹脂が半導体素子の外周を保護できるため気密性、耐湿性に優れ、吸湿によるパッケージクラックが発生しにくくなる。さらに、外部接続用端子に応力緩和機能を持たせたことで、半導体装置と実装基板との熱膨張率の差で生じるストレス(応力)を応力緩和機能を有する外部接続用端子で緩和でき、半導体装置にクラックや断線等の不良が発生することを防止できる。また、半導体素子裏面に冷却用ヒートシンク材を設けたことで、放熱性にも優れた半導体装置とすることができる。

【0059】以上述べたように、本発明の半導体装置の 製造方法によれば、高信頼性の半導体装置(CSP)を 安価に製造することが可能となる。

[0060]

【図面の簡単な説明】

【図1】本発明の半導体装置の製造方法で得られ半導体 装置の一例を模式的に示す断面説明図。

【図2】(a)~(f)は本発明の半導体装置の製造方法の一実施例を工程順に示す断面説明図。

【図3】(a)~(e)は本発明の半導体装置の製造方法の一実施例を工程順に示す断面説明図。

【図4】(a)~(d)は従来の半導体装置の製造方法の一例を工程順に示す断面説明図。

【図5】(a)~(e)は従来の半導体装置の製造方法の一例を工程順に示す断面説明図。

1 4

【図6】(a)~(b)は従来の半導体装置の製造方法の一例を工程順に示す断面説明図。

【図7】従来の半導体装置の製造方法で得られた半導体 装置の一例を模式的に示す断面説明図。

【図8】本発明に係わる外部接続用端子の一例を示す側面説明図。

【図9】本発明に係わる外部接続用端子の一例を示す断面説明図。

【符号の説明】

1、70	CSP
2,72	半導体素子

3、73 電極

4、74 パッシベーション膜

5、75 第一の絶縁層6、76 バリア層

7、77 配線層

8、78 第二の絶縁層

9、79 メタルポスト

10、80 封止樹脂

11、81 外部接続用端子

12、82 ヒートシンク材

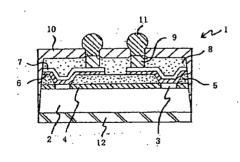
15 保持体

16 導電性材料

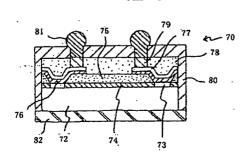
17、87 金属薄膜層

27 接着層

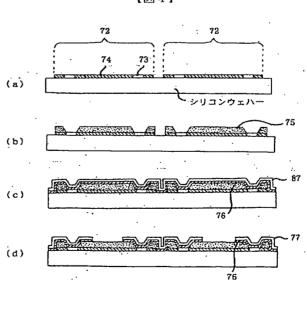
【図1】

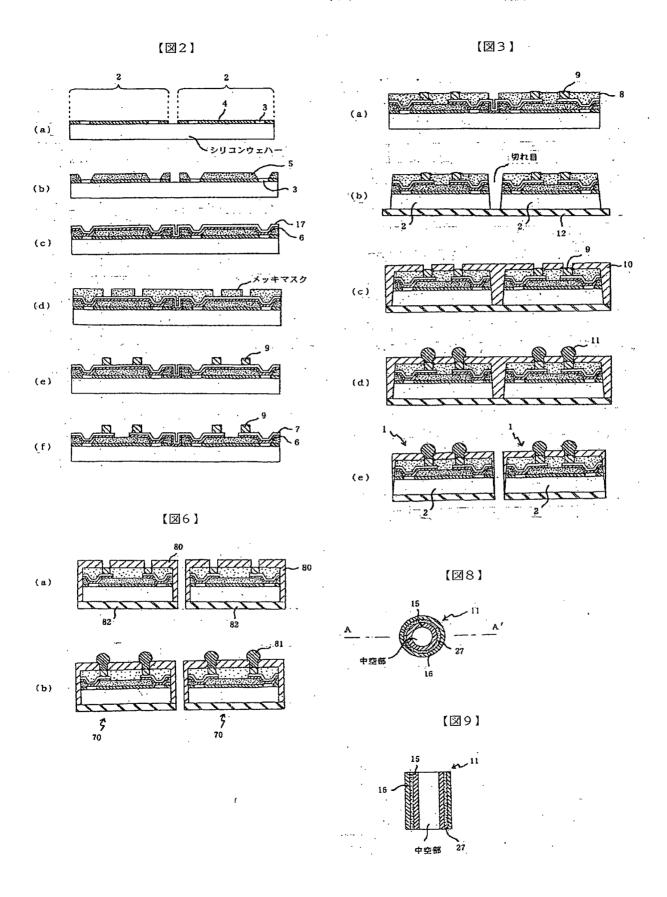


[図7]

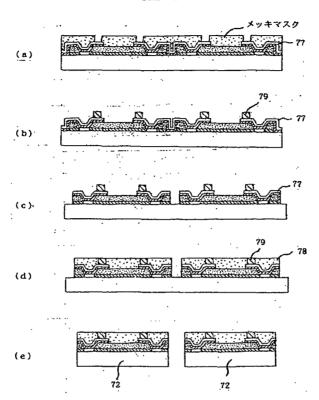


【図4】









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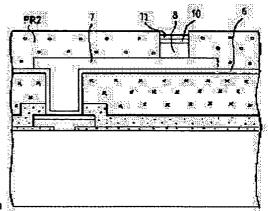
HARA SEIJI

TAKAO YUKIHIRO SHINOKI HIROYUKI

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57) Abstract:

PROBLEM TO BE SOLVED: To improve reliability by forming an Si3N4 film on an interface between a wiring whose main material is Cu and polyimide resin covering the wiring, preventing reaction of imide resin before curing with Cu, and covering a metal post and side surfaces of a thin film layer of Cu with Si3N4. SOLUTION: A photoresist PR2 is formed from which a wiring layer 7 corresponding to a region, on which a metal post is to be formed, is exposed, and a metal post 8 of Cu is formed on the exposed part by electrolytic plating. Since Cu 8, Ni 10 and Au 11 are continuously formed without leaving them for a long time, and oxidation of Cu and Ni can be prevented. After the photoresist PR2 is eliminated and a thin film layer 6 of Cu is eliminated by using the wiring layer 7 as a mask, an Si3N4 film SN is stuck on the whole surface containing the wiring layer 7 and the metal post 8 by a plasma CVD method. Since polyimide resin to be formed in a later process is active and reacts with Cu, the wiring layer 7 and the metal post 8 are wholly covered with the Si3N4 film.



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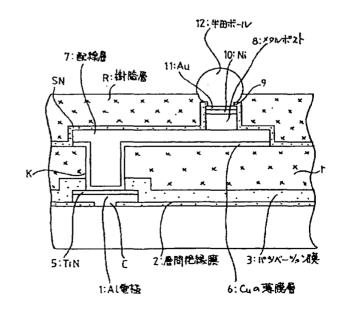
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(54) 【発明の名称】 半導体装置およびその製造方法

(57)【要約】

【課題】チップサイズパッケージの信頼性を向上させ

【解決手段】 Cuより成る配線層7、メタルポスト8 とポリイミド樹脂層Rとの界面にSi3N4膜SNを形成 し、熱硬化前のイミド樹脂とCuの反応を防止する。



]

【特許請求の範囲】

【請求項1】 金属材料から成る金属電極パッドに接続され、チップ表面に延在するCuを主材料とする配線層と、

この配線層を含むチップ表面を被覆する熱硬化型の樹脂から成る絶縁層と、前記配線層上の前記絶縁層に形成された開口部と、

この開口部に形成されたメタルポストと、

このメタルポストに固着された半田ボール (または半田 バンプ)とを具備する半導体装置に於いて、

前記半田ボール(または半田バンプ)が固着される前記 メタルポストの領域を除いて、前記絶縁層と前記配線層 の界面および前記絶縁層と前記メタルポストの界面には Si3N4膜が設けられる事を特徴とする半導体装置。

【請求項2】 金属材料から成る金属電極パッドに接続され、チップ表面に延在するCuを主材料とする配線層と、

この配線層を含むチップ表面を被覆する熱硬化型の樹脂から成る絶縁層と、前記配線層上の前記絶縁層に形成された開口部と.

この開口部に形成されたメタルポストと、

このメタルポストに固着された半田ボール (または半田 バンプ) とを具備する半導体装置に於いて、

前記半田ボールが固着される前記メタルポストの領域 は、前記絶縁層がドライエッチングされて形成される露 出領域が設けられ、この露出領域に半田ボールが固着さ れる事を特徴とする半導体装置。

【請求項3】 金属材料を被着し、パターニングすることにより金属電極パッドを形成し、

前記金属電極パッドの一部を露出する第1の開口部を有する第1の絶縁層を形成し、

前記第1の開口部から露出する前記金属電極パッド上 に、チップ表面に延在するCuより成る配線層を形成

前記配線層上にCuから成るメタルポストを形成し、 前記第1の絶縁層、前記配線層および前記メタルポスト を含むチップ表面にプラズマCVD法でSi3N4膜を被 覆し、

前記メタルポストの頭部を覆う様にチップ表面に、ポリイミド膜を被覆し、

前記メタルポストの頭部に対応する前記ポリイミド膜および前記Si3N4膜をエッチングして、半田ボールを固着する固着部を開口し、

前記半田ボールを固着する開口部を介して前記メタルポスト上に前記半田ボールを形成する事を特徴とする半導体装置の製造方法。

【請求項4】 前記半田ボールを固着する固着部は、ドライエッチングにより開口される請求項3に記職の半導体装置の製造方法。

【請求項5】 前記ポリイミド膜は、熱硬化性または感

光性である請求項3に記載の半導体装置の製造方法。

【請求項6】 前記半田ボールを固着する開口部は、研磨により露出される請求項3に記載の半導体装置の製造方法。

【発明の詳細な説明】

[0001]

【発明の属する技術分野】本発明は、半導体装置および その製造方法に関し、特にチップサイズパッケージとそ の製造方法に関する。チップサイズパッケージ(Chip S 10 ize Package) は、CSPとも呼ばれ、チップサイズと 同等か、わずかに大きいパッケージの総称であり、高密 度実装を目的としたパッケージである。本発明は、CS Pに採用されるボリイミド膜の劣化防止、メタルポスト 頭部の加工に関する。

[0002]

【従来の技術】従来、この分野では、一般にBGA(Ball Grid Array)と呼ばれ、面状に配列された複数のハンダボールを持つ構造、ファインピッチBGAと呼ばれ、BGAのボールピッチをさらに狭ピッチにして外形20がチップサイズに近くなった構造等が知られている。

【0003】また、最近では、「日経マイクロデバイス」1998年8月号 44頁~71頁に記載されたウエハーCSPがある。このウエハーCSPは、基本的には、チップのダイシング前に配線やアレイ状のパッドをウエハープロセス(前工程)で作り込むCSPである。この技術によって、ウエハープロセスとパッケージ・プロセス(後工程)が一体化され、パッケージ・コストが大幅に低減できるようになることが期待されている。

【0004】ウエーハCSPの種類には、封止樹脂型と 30 再配線型がある。封止樹脂型は、従来のパッケージと同様に表面を封止樹脂で覆った構造であり、チップ表面の配線層上にメタルポストを形成し、その周囲を封止樹脂で固める構造である。

【0005】一般にパッケージをプリント基板に搭載すると、プリント基板との熱膨張差によって発生した応力がメタルポストに集中すると言われているが、樹脂封止型では、メタルポストが長くなるため、応力が分散されると考えられている。

【0006】一方、再配線型は、図10に示すように、 40 封止樹脂を使わず、再配線を形成した構造である。つま りチップ51の表面にA1電極52、配線層53、絶縁 層54が積層され、配線層53上にはメタルポスト55 が形成され、その上に半田ボール56が形成されてい る。配線層53は、半田ボール56をチップ上に所定の アレイ状に配置するための再配線として用いられる。

【0007】封止樹脂型は、メタルポストを100μm程度と長くし、これを封止樹脂で補強することにより、高い信頼性が得られる。しかしながら、封止樹脂を形成するプロセスは、後工程において金型を用いて実施する 必要があり、プロセスが複雑になる。

3

【0008】一方、再配線型では、プロセスは比較的単 純であり、しかも殆どの工程をウエーハプロセスで実施 できる利点がある。しかし、なんらかの方法で応力を緩 和し信頼性を高めることが必要とされている。

[0009]

【発明が解決しようとする課題】しかし図10では、配 線層53はCuメッキで形成され、しかも絶縁層54 は、液状の硬化前のポリイミド樹脂を塗布し、これを温 度300~400°C程度でイミド化させて熱硬化させ ている。

【0010】しかしこのイミド化の時に、Cuがイミド 化前の樹脂と反応し、ポリイミド樹脂の膜質劣化を発生 させる問題があった。

【0011】従って、ポリイミド樹脂と配線層との間の 接着性、耐湿性が劣化する問題があった。

【0012】またメタルポスト55を完全に覆うように ポリイミド樹脂を塗布し、その上面を研磨して、前記メ タルポストの頭部を露出させていた。しかしこの研磨工 程は、その制御が非常に難しく、またメタルポストの露 出部が汚染され、半田ボール56の信頼性が低下する問 20 題もあった。

【0013】本発明は、前記問題点を解決するものであ る。

[0014]

【課題を解決するための手段】本発明は上記の課題に鑑 みてなされ、Cuを主材料とする配線とこの上をカバー するポリイミド樹脂との界面に、Si3N4膜を設けるこ とで解決するものである。

【0015】Si3N4膜は、SiO2膜よりもバリア材 として優れ、しかもプラズマCVD法は、ステップカバ レージも優れている。従ってCuから成る配線をSi3 N4膜でカバーすれば、イミド化時の高温反応でイミド 樹脂がCuと反応することがない。

【0016】特に、絶縁層をホトリソグラフィで開口し てメタルポストの頭部が露出されているので、半田ボー ル (または半田バンプ)が固着されるメタルポストの領 域を除いて、絶縁層と配線層の界面にSi3N4膜を設け れば、Cuから成るメタルポストとイミド樹脂の反応も 防止できる。

【0017】第2に、半田ボール(または半田バンプ) が固着されるメタルポストの領域に対応する絶縁層をド ライエッチングして露出領域が設けられると、メタルポ ストの頭部がクリーンな状態で形成でき、半田ボールの 固着性が改善される。

【0018】第3に、第1の絶縁層、前記配線層および 前記メタルポストを含むチップ表面にプラズマCVD法 でSi3N4膜を被覆し、前記メタルポストの頭部を覆う 様にチップ表面に、熱硬化型のポリイミド膜を被覆し、 前記メタルポストの頭部に対応する前記ポリイミド膜お よび前記Si3N4膜をエッチングして、半田ボールを固 50 がある。しかし、配線層の表面にはSi3N4膜SNが被

着する固着部を開口し、前記半田ボールを固着する開口 部を介して前記メタルポスト上に前記半田ボールを形成 すれば、前述したようにCuから成る配線層、Cuから 成るメタルポストとイミド層の反応を防止しつつ、Si 3N4膜で保護されたメタルポストを例えばエッチング等 で露出できるため、半田ボールとの接合面をクリーンに でき、半田ボールの信頼性を向上させることができる。 【0019】第4に、ドライエッチングにより開口され れば、スパッタ性も付加されるため、更にメタルポスト 10 の露出部をクリーンにできる。

[0020]

【発明の実施の形態】次に、本発明の実施形態について 説明する。

【0021】図9に於いて、図番1は、通常のワイヤボ ンディングタイプのICチップに於いて、最上層のメタ ル (ボンディングパッドとしても機能する部分)の部分 であり、このA1電極1のコンタクトホールCが形成さ れる層間絶縁膜を図番2で示す。

【0022】またこのコンタクトホールCの下層には、 メタルが複数層で形成され、例えばトランジスタ(MO S型のトランジスタまたはBIP型のトランジスタ)、 拡散領域、ポリSiゲートまたはポリSi等とコンタク トしている。

【0023】ここで、本実施例は、MOS型で説明して いるが、BIPでも良い事は言うまでもない。

【0024】また本構造は、一般には一層メタル、2層 メタル…と呼ばれる I Cである。

【0025】更には、パッシベーション膜を図番3で示 す。ここでパッシベーション膜3は、Si窒化膜、エポ キシ樹脂またはポリイミド等でなり、更にこの上には、 絶縁樹脂層ァが被覆されている。この絶縁樹脂層ァは、 後述するようにフラット性を実現し、半田ボールの高さ を一定にしている。

【0026】またA1電極1上には、窒化Ti膜5が形 成されている。

【0027】このパッシベーション膜3と絶縁樹脂層r は、窒化Ti膜5を露出する開口部Kが形成され、ここ には、配線層のメッキ電極 (シード層) としてCuの薄 膜層6が形成される。そしてこの上には、Cuメッキに よる配線層7が形成される。ここで、配線層7を含むチ ップ全面に本発明のポイントであるSi3N4膜SNが被 覆され、ポリイミド樹脂から成る樹脂層Rが形成され

【OO28】ポリイミド樹脂Rは、液状のイミド樹脂で 用意され、ウェハ全面にスピンオンされ、厚さ20~6 Oμm程度で形成される。その後、このイミド樹脂は、 熱硬化反応により重合される。温度は、300~400 C程度である。しかし熱硬化前のイミド樹脂は、非常 に活性でありCuと反応し、その界面を悪化させる問題 _

覆されているため、このCuとの反応を防止することができる。ここでSi3N4膜の膜厚は、1000~3000Å程度である。

【0029】また膜SNは、バリア性が優れた絶縁膜で良いが、Si02膜は、バリア性に劣る。しかしSi02 関を採用する場合は、Si3N4膜よりもその膜厚を厚くする必要があり。またSi3N4膜は、プラズマCVD法で形成できるので、そのステップカバレージも優れ、好ましい。

(*)【0030】更には、後述する製造方法から明らかとな 10 るが、メタルポスト8を形成した後、樹脂層Rを被覆するので、Cuから成る配線層7とイミド層の反応を防止するばかりでなく、Cuから成るメタルボスト8とイミド層の反応も防止できる。

【00031】続いて、配線層7の端部に開口部9が形成され、この開口部9には、メタルポスト8の頭部が顔を出し、メタルポスト8の頭部には、下層からNi10、Au11が形成されているため、実際はAuが開口部9から露出している。

【0032】Cuから成るメタルポスト8の上に直接半田ボールが形成されると、酸化されたCuが原因で半田ボールとの接続強度が劣化する。また酸化防止のためにAuを直接形成すると、Auが拡散されるため、間にNiが挿入されている。NiはCuの酸化防止をし、またAuはNiの酸化防止をしている。従って半田ボールの劣化および強度の劣化は抑制される。

【0033】ここでNi、Auは、電解メッキで形成されるが無電解メッキでも良い。またAuの代わりにPt,Pdが用いられても良い。

【0034】更には、Auの薄膜層11の上には、半田ボール12が形成される。

【0035】ここで半田ボールと半田バンプの違いについて説明する。半田ボールは、予めボール状の半田が別途用意され、メタルポスト8に固着されるものであり、半田バンプは、配線層7、メタルポスト8を介して電解メッキで形成されるものである。半田バンプは、最初は厚みを有した膜として形成され、後熱処理により球状に形成されるものである。

【0036】続いて図9の構造について図1より簡単にその製造方法について説明する。

【0037】まず、A1電極1を有するLSIが形成された半導体基板(ウエーハ)を準備する。ここでは、前述したように1層メタル、2層メタル・・のICで、例えばトランジスタのソース電極、ドレイン電極が一層目のメタルとして形成され、ドレイン電極とコンタクトしたA1電極1が2層目のメタルとして形成されている。

【0038】ここではドレイン電極が露出する層間絶縁膜2の開口部Cを形成した後、ウェハ全面にAlを主材料とする電極材料、窒化Ti膜5を形成し、ホトレジストをマスクとして、Al電極1と窒化Ti膜5を所定の50

形状にドライエッチングしている。

【0039】ここでは、パシベーション膜3を形成し、この後開口した開口部Cにバリアメタルを形成するのと違い、バリアメタルとしての窒化Ti膜も含めてホトレジストで一度に形成でき、工程数の簡略が可能となる。【0040】また窒化Ti膜5は、後に形成するCuの薄膜層6のバリアメタルとして機能させている。しかも窒化Ti膜は、反射防止膜として有効であることにも着目している。つまりパターニングの際に使用されるレジストのハレーション防止としても有効である。ハレーション防止として最低1200Å~1300Å程度必要であり、またこれにバリアメタルの機能を兼ね備えるためには、2000Å~3000Å程度が好ましい。これ以上厚く形成されると、今度は窒化Ti膜が原因で発生するストレスが発生する。

【0041】またA1電極1と窒化Ti膜5がパターニングされた後、全面にパッシベーション膜3が被覆される。パッシベーション膜として、ここではSi3N4膜が採用されているが、ポリイミド等も可能である。(以上図1参照)

続いて、パッシベーション膜3の表面に絶縁樹脂層 rが 被覆される。この絶縁樹脂層は、ここでは、ポジ型の感 光性ポリイミド膜が採用されている。

【0042】この感光性ポリイミド膜を採用することで、図2の開口部Kのパターニングに於いて、別途ホトレジストを形成して開口部Kを形成する必要が無くなり、工程の簡略化が実現できる。しかもこのポリイミド膜は、平坦化の目的でも採用されている。つまり半田ボールの高さが全ての領域において均一である為には、配線層7もフラットに精度良く形成される必要があり、その為にポリイミド樹脂を塗布してその表面をフラットにしている。

【0043】ここでA1電極1はLSIの外部接続用のパッドも兼ね、半田ボール(半田バンプ)から成るチップサイズパッケージとして形成しない時は、ワイヤボンディングパッドとして機能する部分である。(以上図2参照)

続いて全面にCuの薄膜層6を形成する。このCuの薄膜層6は、後に配線層7のメッキ電極となり、約100 0~2000 Å程度である。

【0044】続いて、全面に例えばホトレジスト層PR 1を塗布し、配線層7に対応するホトレジストPR1を 取り除く。(以上図3参照)

更に、このホトレジストPR1の開口部に露出するCuの薄膜層6をメッキ電極とし、配線層7を形成する。この配線層7は機械的強度を確保するために2~5μm程度に厚く形成する必要がある。ここでは、メッキ法を用いて形成したが、蒸着やスパッタリング等で形成しても

50 【0045】この後、ホトレジスト層PR2を除去す

る。(以上図4参照)

続いて、メタルポスト8が形成される領域に対応する配線層7を露出したホトレジストPR2が形成され、この露出部に電解メッキでCuのメタルポスト8が形成される。これもCuの薄膜層6がメッキ電極として活用される。このメタルポストは、30~40μm程度の高さに形成され、更にNi10が電解メッキで約1μm、Au11が電解メッキで約5000Åで形成される。

【0046】Cu8、Ni10、Au11が連続されて形成されるため、長時間放置されないので、Cuの酸化防止、Niの酸化防止が実現できる。(以上図5参照)続いて、ホトレジストPR2を除去し、配線層7をマスクとしてCuの薄膜層6を除去する。

【0047】次に示す工程は、本発明のポイントとなる 工程であり、配線層7、メタルポスト8も含めて全表面 にプラズマCVD法でSi3N4膜SNを被着する。

【0048】これは、後の工程で形成されるイミド樹脂が活性であり、Cuと反応する。従って配線層7、メタルポスト8は、全てこのSi3N4膜SNでカバーする必要がある。

【0049】ここでは、Ni10、Au11も含めたメタルポスト8を形成した後に、Si3N4膜SNを形成しているので、配線層7、メタルポスト8も含めてカバーすることができる。またパターニングされて露出している側面Mも一緒に保護する必要があるが、ここでは、両者をパターニングした後にSi3N4膜を被覆しているので、側面Mも一緒に保護される。

【0050】続いてSi3N4膜SNで保護された状態で、イミド樹脂Rを全面に塗布する。

【 0 0 5 1 】この樹脂も感光性樹脂で、熱硬化反応で硬化される。

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【0052】この感光性樹脂により、図8に示す工程の簡略化、表面のフラット性が実現できる。

【0053】また絶縁樹脂層R、rは、次のメリットもある。一般に粘性のある樹脂をディスペンサで塗布すると、脱泡してあっても中に気泡を取り込んでしまう問題がある。気泡を取り込んだまま焼結すると、これからの工程やユーザー側での高温雰囲気使用で気泡が破裂する問題がある。

【0054】本工程では、スピンオンで塗布し、一回のスピンで20~30μm程度の膜厚に形成できるように調整してある。この結果、この膜厚よりも大きな気泡は、膜の厚みが薄い故に弾けて消える。またこの膜厚よりも小さい気泡は、スピンオンの遠心力で外部へ飛ばされる樹脂と一緒に外に飛ばされ、気泡無しの膜が形成できる。

【0055】また絶縁樹脂層Rは、膜厚として50μm程度を必要とし、この場合、前述した原理を採用し、スピンオンで複数回に分けて塗布し、気泡を取り除きながら形成する。(以上図7参照)

続いて、例えばメタルマスクMSを採用し、メタルマスクの開口部がメタルポスト8の頭部に位置するように調整され、露光・現像により、メタルポスト頭部のポリイミド層Rに開口部20を形成する。開口部の開口径は、50μm程度がよい。図に示されるように、メタルマスクMSと絶縁樹脂層Rとの距離により、露光部の周辺は、その光がぼける。つまり周辺の光強度が主とする領域よりも弱くなり、その結果開口部20の側壁は、垂直に開口されず傾斜を有するようになる。

0 【0056】また、現像後は200℃~350°C程度の温度下でポリイミド層をベーキングするとよい。

【0057】更には、開口部20には、Si3N4膜SNが露出しているので、ポリイミド層Rの開口部20をマスクとしてSi3N4膜SNが取り除かれる。

【0058】ここで絶縁樹脂層Rの開口部は、等方的に エッチングされる。形状が球状になるので、半田ボール 12を載置する上で有利である。

【0059】またSi3N4膜は、ドライエッチングで開口されるので、半田ボール12との接合部は、スパッタ20性も有るためクリーンな状態となる。

【0060】ここでは、前記開口部の形成に於いて、エッチングの代わりに研磨法を用いても良い。(以上図8参照)

最後に、用意した半田ボール12を前記開口部20に搭載し、リフローする。そして、半導体基板をダイシング 工程により、スクライブラインに沿ってチップに分割 し、チップサイズ・パッケージとして完成する。

【0061】ここで半田を溶融するタイミングは、ダイシングの前である。図8で図示してあるように、開口部20を形成した後、ウェハ全面に保護シートを貼り付け、表面を保護しながらバックグラインドをする。

【0062】半田ボールを形成した後に保護シートを貼ると、半田ボールと保護シートとで形成される隙間にバックグラインド時に流れる水が入り保護シールが剥がれてしまう問題があった。また高温度雰囲気にさらされると、バックグラインド時の熱歪みが原因で、傷を介して割れる恐れがある。そのため、開口部20のドライエッチングで高熱になるため、このドライエッチング後に保護シートを貼り合わせてバックグラインドすれば、水の40 侵入もなく、更には熱歪みによるクラック等の防止も実現できる

【 0 0 6 3 】以上、本発明は、再配線型で説明してきたが、樹脂封止型でも実施できることは言うまでもない。 【 0 0 6 4 】

【発明の効果】本発明によれば、配線層とポリイミド樹脂層Rとの界面に、Si3N4膜が設けられてあるので、硬化前のイミド樹脂とCuとの反応を防止することができる。またメタルポスト、Cuの薄膜層の側面もSi3N4膜でカバーされ、前記反応を防止することができる。

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【0065】従って、Cuの配線層、Cuの薄膜層とポリイミド樹脂との界面は、反応もなく安定した状態で形成されるため、耐湿性、膨れ等を防止することができ、歩留まりの向上を実現できる。

【0066】また半田ボール(または半田バンプ)が固着されるメタルポストの領域に対応する絶縁層をドライエッチングして露出領域が設けられので、メタルポストの頭部がクリーンな状態で形成でき、半田ボールの固着性が改善される。

【0067】また、第1の絶縁層、前記配線層および前 10 記メタルポストを含むチップ表面にプラズマCVD法で Si3N4膜を被覆し、前記メタルポストの頭部を覆う様 にチップ表面に、熱硬化型のポリイミド膜を被覆し、前 記メタルポストの頭部に対応する前記ポリイミド膜および前記Si3N4膜をエッチングして、半田ボールを固着する間着部を開口し、前記半田ボールを固着する開口部を介して前記メタルポスト上に前記半田ボールを形成するので、前述したようにCuから成る配線層、Cuから成るメタルポストとイミド層の反応を防止しつつ、Si3N4膜で保護されたメタルポストを例えばエッチング等 20で露出できるため、半田ボールとの接合面をクリーンにでき、半田ボールの信頼性を向上させることができる。【0068】更に、ドライエッチングにより開口されれ

露出部をクリーンにできる。

【図面の簡単な説明】

【図1】 本発明の実施形態に係る半導体装置の製造方法を説明する図である。

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【図2】 本発明の実施形態に係る半導体装置の製造方法を説明する図である。

【図3】 本発明の実施形態に係る半導体装置の製造方法を説明する図である。

【図4】 本発明の実施形態に係る半導体装置の製造方 0 法を説明する図である。

【図5】 本発明の実施形態に係る半導体装置の製造方法を説明する図である。

【図6】 本発明の実施形態に係る半導体装置の製造方法を説明する図である。

【図7】 本発明の実施形態に係る半導体装置の製造方法を説明する図である。

【図8】 本発明の実施形態に係る半導体装置の製造方法を説明する図である。

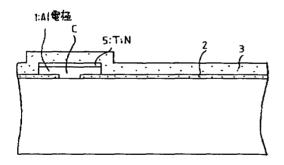
【図9】 本発明の実施形態に係る半導体装置の製造方 20 法を説明する図である。

【図10】 従来のチップサイズパッケージを説明する 図である。

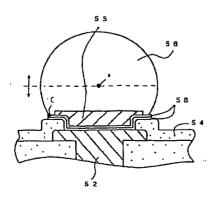
【図11】 従来のチップサイズパッケージを説明する 図である。

【図1】

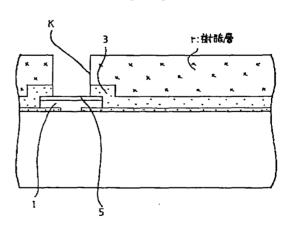
ば、スパッタ性も付加されるため、更にメタルポストの

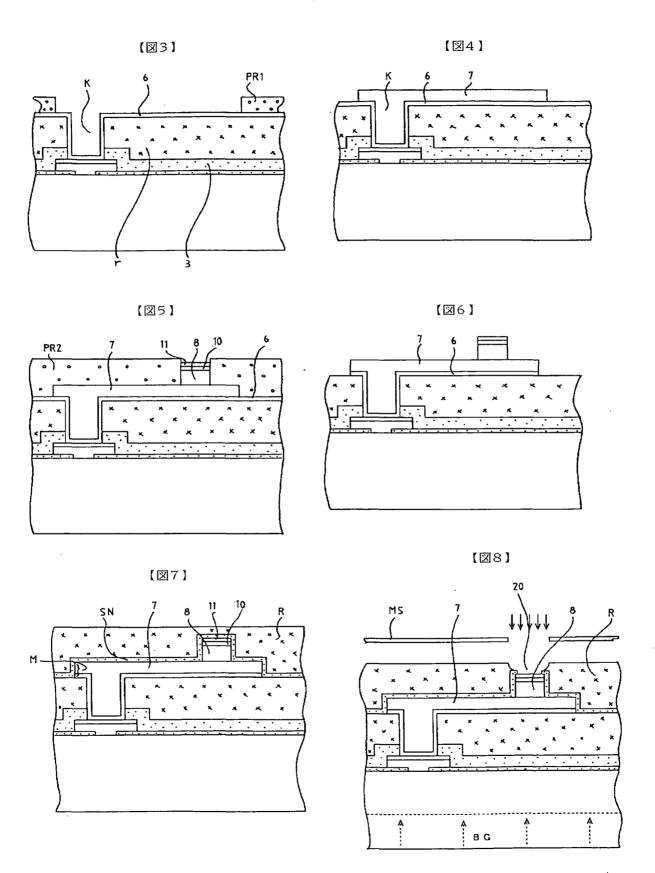


【図11】

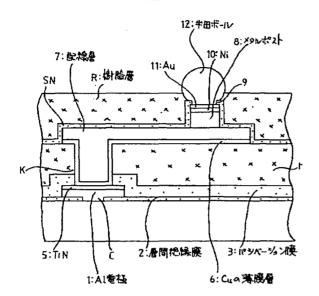


【図2】

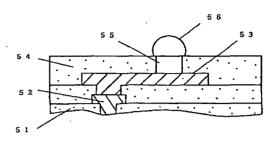




【図9】



【図10】



フロントページの続き

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Please check the appropriate assignee category or categories (will not be printed on the patent): 4a. The following fee(s) are enclosed:

The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _______ (enclose an extra copy of this form). 5. Change in Entity Status (from status indicated above) a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. □ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2). The Director of the USPTO is requested to apply the Usus Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

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Authorized Signature

Typed or printed name

06/22/2005 Date

Michael E Fogarty

36,139 Registration No.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/919,402 08/17/2004		Yoshifumi Nakamura	60188-932	6102	
20277 75	590 06/27/2005		EXAM	INER	
	T WILL & EMERY LL	HUYNH, ANDY			
600 13TH STREET, N.W. WASHINGTON, DC 20005-3096			ART UNIT	PAPER NUMBER	
			2818		
			DATE MAILED: 06/27/2009	5	

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES DEPARTMENT OF COMMERCE U.S. Patent and Trademark Office

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P.O. Box 1450

Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION		ATTORNEY DOCKET NO.
				EXAMINER
			ART UNIT	PAPER
				062005
			DATE MAILED) :

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The Information Disclosure Statement (IDS) filed May 04, 2005 has been entered and considered.

David Natms
Supervisory Patent Examiner
Technology Center 2500



SHEET 1 OF 1

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					APPLICANT Yoshifumi	NAKAMU	RA,	et al.	
		(PT	O-1449)		FILING DATE			OUP	
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^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Nakamura, et al. Docket No.: TA148-0017-US-02

Applicant(s): Tessera Advanced Art Unit: 2818

Technologies, Inc. Conf No.: 6102

Application No.: 10/919,402 Examiner: HUYNH, ANDY

Date Filed: 08-17-2004

Title: SEMICONDUCTOR DEVICE INCLUDING A DIFFUSION LAYER

COMMISSIONER FOR PATENTS PO Box 1450 Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION PTO'S ERROR

Dear Sir:

The Patentee submits herewith PTO Form PTO/SB/44 Certificate of Correction. This submission corrects an error by the U.S. Patent and Trademark Office (USPTO). Applicant's claim amendments filed on February 14, 2005 show the correct text on page 3, line 4. More particularly, the claim presented by the applicant recited "10 µm to 20 µm." Upon printing, the USPTO printer incorrectly omitted the second instance of "µ." Accordingly, the Applicant/Assignee requests a Certificate of Correction at the expense of the USPTO to correct this error. We believe that no fee is due. However, if a fee is required, please charge deposit account no 50-4701.

If any questions remain or anything additional is required to correct this patent copy, please contact the undersigned at (408) 321-6069.

Date: March 22, 2016 Respectfully submitted,

Customer Number 79220

By /Christopher Lattin/

Christopher Lattin Attorney, Reg. No. 56,064

Attorney for Applicant Tessera Advanced Technologies, Inc. Attorney phone: (408) 321-6069 3025 Orchard Parkway San Jose, California 95134 Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 6,954,001	Page1 of1
APPLICATION NO.: 10/919,402	
INVENTOR(S) : Yoshifumi NAKAMURA, et al.	
It is certified that an error appears or errors appear in the above-identified patent and to be the series is hereby corrected as shown below:	that said Letters Patent
In the Claims, In Claim 10, Line 16,	
Add μ immediately before "m." such that the claim recites "20 μ m."	
	ļ

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Tessera Advanced Technologies, Inc. 3025 Orchard Parkway San Jose, CA 95134

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Electronic Acknowledgement Receipt				
EFS ID:	25257843			
Application Number:	10919402			
International Application Number:				
Confirmation Number:	6102			
Title of Invention:	SEMICONDUCTOR DEVICE INCLUDING A DIFFUSION LAYER			
First Named Inventor/Applicant Name:	Yoshifumi Nakamura			
Customer Number:	20277			
Filer:	Christopher W. Lattin/Jennifer Kostic			
Filer Authorized By:	Christopher W. Lattin			
Attorney Docket Number:	60188-932			
Receipt Date:	22-MAR-2016			
Filing Date:	17-AUG-2004			
Time Stamp:	12:58:38			
Application Type:	Utility under 35 USC 111(a)			

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	PoA.pdf	60273	no	1
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Warnings:

Information: 192 of 199

SAMSUNG EXHIBIT 1004

2	Assignee showing of ownership per 37	TA148-0017-US-02_373- Statement.pdf	64740	no	2
2	CFR 3.73		1cde4fe651949490193c7311ab83f230a0c5 abff		
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3	Request for Certificate of Correction	TA148-0017-US-02_CoC.pdf	58891	no 2	2
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·	request or certificate or correction	US-02_CoCRequest.pdf	b80085f511bf9a8b0cdf0fad69f65bd8fa678 c33	0	
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		Total Files Size (in bytes)	27	75742	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby 37 CFR	revoke all previous powers of a 3.73(b).	attorney given in the	application identifi	ed in the attached state	ement under	
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√ Pra	ctitioners associated with the Customer	Number:	79220			
OR						
Pra	ctitioner(s) named below (if more than t	en patent practitioners a	re to be named, then a	customer number must be us	sed):	
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any and al	I patent applications assigned <u>only</u> to the other of this form in accordance with 37 CFR 3	ne undersigned accordin				
Please cha	ange the correspondence address for the	ne application identified i	n the attached statemen	nt under 37 CFR 3.73(b) to:		
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Assignee Name and Address:						
Tessera	Advanced Technologies, Inc.					
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San Jose	e, CA 95134					
A copy o	f this form, together with a state	ment under 37 CFR	3.73(b) (Form PTO/S	B/96 or equivalent) is re	quired to be	
filed in ea	ach application in which this forr	n is used. The state	ment under 37 CFR	3.73(b) may be complet	ed by one of	
	the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.					
		SIGNATURE of Assi				
	The individual whose signature			on behalf of the assignee		
Signature	1644	*		Date 1 3/3	de 15	
Name		aul Davis		Telephone		
Title	Senior Vice President and General Counsel					

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(c)
Applicant/Patent Owner: Tessera Advanced Technologies, Inc.
Application No./Patent No.: Patent No. 6954001 Filed/Issue Date: Issue Date 10/11/2005
Titled: SEMICONDUCTOR DEVICE INCLUDING A DIFFUSION LAYER
Tessera Advanced Technologies, Inc. , a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)
states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):
1. The assignee of the entire right, title, and interest.
2. An assignee of less than the entire right, title, and interest (check applicable box):
The extent (by percentage) of its ownership interest is
There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:
Additional Statement(s) by the owner(s) holding the balance of the interest <u>must be submitted</u> to account for the entire right, title, and interest.
3. The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:
Additional Statement(s) by the owner(s) holding the balance of the interest <u>must be submitted</u> to account for the entire right, title, and interest.
4. The recipient, via a court proceeding or the like (<i>e.g.</i> , bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.
The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):
A. An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel, Frame, or for which a copy thereof is attached.
B. A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:
1. From: Inventors: NAKAMURA, et al. To: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
The document was recorded in the United States Patent and Trademark Office at Reel 013540 , Frame 0756 , or for which a copy thereof is attached. 2. From: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. To: PANASONIC CORPORATION
The document was recorded in the United States Patent and Trademark Office at Reel $\frac{033777}{}$, Frame $\frac{0873}{}$, or for which a copy thereof is attached.

[Page 1 of 2]
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STATEMENT	T UNDER 37 CFR 3.73(c)
3. From: PANASONIC CORPORATION	To: PANNOVA SEMIC, LLC
Reel <u>036065</u> , Frame <u>0273</u>	ited States Patent and Trademark Office at, or for which a copy thereof is attached
The document was recorded in the Uni Reel <u>037581</u> , Frame <u>0466</u>	ited States Patent and Trademark Office at, or for which a copy thereof is attached.
	To:
The document was recorded in the Uni	ited States Patent and Trademark Office at
Reel, Frame	, or for which a copy thereof is attached.
6. From:	To:
The document was recorded in the Uni	ited States Patent and Trademark Office at
Reel, Frame	, or for which a copy thereof is attached.
Additional documents in the chain of title are lis	sted on a supplemental sheet(s).
As required by 37 CFR 3.73(c)(1)(i), the documer assignee was, or concurrently is being, submitted	ntary evidence of the chain of title from the original owner to the d for recordation pursuant to 37 CFR 3.11.
	original assignment document(s)) must be submitted to Assignment cord the assignment in the records of the USPTO. See MPEP 302.08]
The undersigned (whose title is supplied below) is author	rized to act on behalf of the assignee.
/Christopher Lattin/	March 21, 2016
Signature	Date
Christopher Lattin	56,064
Printed or Typed Name	Title or Registration Number

[Page 2 of 2]



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United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov UNITED STATES DEPARTMENT OF COMMERCE

APPLICATION NUMBER

Tessera Intellectual Properties Corp.

FILING OR 371(C) DATE

FIRST NAMED APPLICANT

ATTY. DOCKET NO./TITLE

10/919,402

c/o Christopher Lattin 3025 Orchard Parkway San Jose, CA 95134

08/17/2004

Yoshifumi Nakamura

CONFIRMATION NO. 6102 POA ACCEPTANCE LETTER



Date Mailed: 03/24/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/22/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

> Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/rmturner myles/



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United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov UNITED STATES DEPARTMENT OF COMMERCE

FILING OR 371(C) DATE FIRST NAMED APPLICANT APPLICATION NUMBER ATTY. DOCKET NO./TITLE

10/919,402 08/17/2004

Yoshifumi Nakamura

20277 MCDERMOTT WILL & EMERY LLP The McDermott Building 500 North Capitol Street, N.W. WASHINGTON, DC 20001



Date Mailed: 03/24/2016

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/22/2016.

 The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

> Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,954,001 B2

APPLICATION NO. : 10/919402 DATED : October 11, 2005

INVENTOR(S) : Yoshifumi Nakamura et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims, In Claim 10, Line 16,

Add -- μ -- immediately before "m." such that the claim recites "20 μ m."

Signed and Sealed this Third Day of May, 2016

Michelle K. Lee

Director of the United States Patent and Trademark Office

Michelle K. Lee