

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BROADCOM CORPORATION,
Petitioner,

v.

TESSERA ADVANCED TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01486
Patent 6,954,001 B2

Before BARBARA A. PARVIS, ROBERT J. WEINSCHENK, and
STACY B. MARGOLIES, *Administrative Patent Judges*.

MARGOLIES, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Broadcom Corporation (“Petitioner”) filed a Petition for *inter partes* review of claims 1–18 of U.S. Patent No. 6,954,001 B2 (Ex. 1001, “the ’001 patent”). Paper 1 (“Pet.”). Tessera Advanced Technologies, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.108. Upon consideration of the Petition and the Preliminary Response, we conclude that the information presented shows that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 1–18 of the ’001 patent.

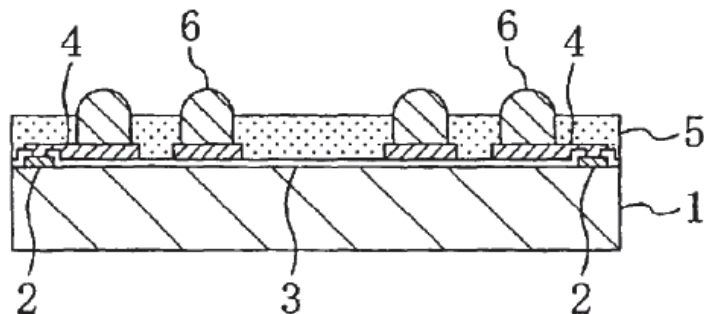
A. Related Matter

The parties identify the following matter in which the ’001 patent has been asserted: *Tessera, Inc. v. Broadcom Corporation*, Civil Action No. 1:16-cv-00380 (D. Del). Pet. 1; Paper 4, 1; *see* 37 C.F.R. § 42.8(b)(2).

B. The ’001 Patent

The ’001 patent, titled “Semiconductor Device Including a Diffusion Layer,” states that an object of the invention is to provide a semiconductor device “having improved junction reliability between the metal wiring and a ball electrode mounted on an external electrode portion of the metal wiring.” Ex. 1001, [54], 2:35–41. Figure 15, below, illustrates a cross section of a conventional semiconductor device:

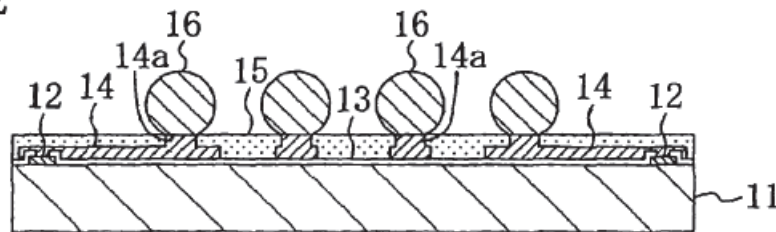
FIG. 15B
Prior Art



Id. at 1:43–46. As shown in Figure 15 above and as described in the '001 patent, in a conventional semiconductor device, wiring electrodes of a substrate on which the semiconductor device is mounted are connected to metal wirings 4 of copper (Cu) formed on the surface of semiconductor element 1 through ball electrodes 6 formed from solder. *Id.* at 2:4–9. According to the '001 patent, “tin (Sn) contained in solder of the ball electrode 6 diffuses into Cu of the metal wiring 4 to form a Sn–Cu alloy layer.” *Id.* at 2:15–18. The '001 patent states that, “[a]s a result, in the portion of the metal wiring 4 on which the ball electrode 6 is mounted (i.e., the external electrode portion) and the portion near the external electrode portion, the Sn–Cu alloy grows in the most part of the metal wiring.” *Id.* at 2:18–22. The patent states that “[t]he Sn–Cu alloy is weak and hard” and “is likely to be broken by the stresses” generated due to differences in the thermal expansion coefficients of the semiconductor element, the resin film (if included), and the substrate. *Id.* at 2:1–3, 2:22–31.

Figure 2 of the '001 patent, below, illustrates a cross-sectional view of “the semiconductor device of the first embodiment”:

FIG. 2



Id. at 8:11–12. As illustrated in Figure 2 above, electrodes 12 are formed on the surface of semiconductor element 11, and passivation film 13, also formed over the surface of semiconductor element 11, has an opening on

each electrode 12. *Id.* at 8:13–17. According to the '001 patent, metal wirings 14 containing copper are formed on passivation film 13, and “[e]ach metal wiring 14 is electrically connected to a corresponding one of the electrodes 12.” *Id.* at 8:18–21. The patent discloses that insulating film 15 is formed on metal wirings 14 and passivation film 13 and “has openings in order to expose a portion of each metal wiring 14 which functions as an external electrode (hereinafter, referred to as ‘external electrode portion 14a’).” *Id.* at 8:21–26. According to the '001 patent, “ball electrodes 16, which are formed from solder, are connected in a molten state to the openings of the insulating film 15, that is, the external electrode portions 14a of the metal wirings 14, respectively.” *Id.* at 8:27–35.

The '001 patent states that “[t]he present embodiment is characterized in that the thickness (e.g., 14 μ m) of the external electrode portion 14a of the metal wiring 14 is greater than that of the other portion of the metal wiring 14 (hereinafter, referred to as ‘non-electrode portion’).” *Id.* at 8:39–43. The patent states:

When the metal wirings 14 contain, e.g., Cu (which is a commonly used metal wiring material), Sn contained in solder of the ball electrode 16 diffuses into Cu contained in the metal wiring 14, whereby a Sn–Cu alloy layer having low strength grows in the thickness direction of the external electrode portion 14a. However, since the thickness of the external electrode portion 14a of the metal wiring 14 is greater than that of the non-electrode portion of the metal wiring 14, this Sn–Cu alloy layer can be prevented from growing through the entire thickness of the external electrode portion 14a.

Id. at 8:63–9:6. According to the '001 patent, “[s]ince a part of the external electrode portion 14a is left unchanged into the Sn–Cu alloy layer, the strength of the metal wiring 14 can be maintained even if Cu is used as a

metal wiring material.” *Id.* at 9:9–12. The patent adds that even if stresses due to a difference in thermal expansion coefficients are generated, “the . . . structure of the first embodiment can prevent the Sn–Cu alloy layer having low strength from being broken and thus can prevent disconnection of the metal wirings 14.” *Id.* at 9:20–24.

The ’001 patent states that “[i]n the first embodiment, the thickness of the external electrode portion 14a of the metal wiring 14 (e.g., the total thickness of the non-electrode portion of the metal wiring 14 and the metal-material embedded portion) is preferably in the range of 10 μm to 20 μm .” *Id.* at 9:36–40. The patent also states that “[i]n the first embodiment, the thickness of the non-electrode portion of the metal wiring 14 is preferably in the range of 0.01 μm to 8 μm , and more preferably in the range of 0.01 μm to 4 μm .” *Id.* at 9:25–28.

C. Illustrative Claims

Claims 1 and 10 are illustrative of the subject matter of the challenged claims and read as follows:

1. A semiconductor device, comprising:
 - a semiconductor element;
 - a first electrode portion* formed on the semiconductor element, said first electrode portion comprising a first metal component;
 - a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal component; and
 - a diffusion layer formed between said first electrode portion and said second electrode portion,wherein said diffusion layer comprises said first metal component and said second metal component.

10. A semiconductor device comprising:
- a semiconductor element;
 - a first electrode portion formed on the semiconductor element, said first electrode portion comprising a first metal component;
 - a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal component; and
 - a diffusion layer formed between said first electrode portion and said second electrode portion,
- wherein said diffusion layer comprises said first metal component and said second metal component, and
- said first electrode portion and said diffusion layer have a combined thickness in the range of 10 μm to 20 μm .*

Id. at 26:15–28, 26:61–27:9 (emphases added to disputed limitations),
Certificate of Correction (correcting claim 10).

D. Asserted Grounds of Unpatentability

Petitioner contends that claims 1–18 of the '001 patent are unpatentable based on the following specific grounds (Pet. 7–8, 15–64):

Reference(s)	Basis	Challenged Claims
Narizuka ¹	35 U.S.C. § 102(b) ²	1–18
Takizawa ³	35 U.S.C. § 102(b)	1–7, 9–16, and 18
Takizawa and Narizuka	35 U.S.C. § 103	8 and 17
Takizawa and Hashimoto ⁴	35 U.S.C. § 103	7 and 16

In its analysis, Petitioner relies on the declaration testimony of Dr. Jeffrey C. Suhling (Ex. 1002).

II. DISCUSSION

A. Claim Construction

In an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard). Consistent with the broadest reasonable construction, claim terms are presumed to have their ordinary and customary meaning as understood by a person of ordinary skill in the art in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir.

¹ PCT Published Application No. WO00/52755, published Sept. 8, 2000, and certified translation thereof (Ex. 1012, “Narizuka”).

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), revised 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the challenged patent was filed before March 16, 2013, we refer to the pre-AIA versions of §§ 102 and 103 in this Decision.

³ German Patent Publication No. DE 100 11 368, published December 7, 2000, and certified translation thereof (Ex. 1014, “Takizawa”).

⁴ PCT Published Application No. WO99/49511, published Sept. 30, 1999, and certified translation thereof (Ex. 1015, “Hashimoto”).

2007). In addition, the Board may not “construe claims during [an *inter partes* review] so broadly that its constructions are unreasonable under general claim construction principles.” *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) (emphasis omitted). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner proposes constructions for “electrode,” “electrode portion,” “metal component,” “diffusion layer formed between said first electrode portion and said second electrode portion,” “said first electrode portion and said diffusion layer have a combined thickness in the range of 10 μm to 20 μm ,” and “flush with or higher than a surface of the insulating film.” Pet. 12–15.

Patent Owner argues that Petitioner’s proposed constructions of “electrode” and “electrode portion” should be rejected and proposes constructions for the larger claim phrases “first electrode portion,” “second electrode portion,” and “third electrode portion.” Prelim. Resp. 24–29. Patent Owner also asserts that the other phrases identified by Petitioner do not require construction. *Id.* at 29–34.

We address Patent Owner’s proposed construction of “first electrode portion” below. We do not need to construe any other claim term or phrase to determine whether or not to institute *inter partes* review.

First electrode portion

Patent Owner asserts that “first electrode portion” “means ‘external electrode portion’ or, alternatively, ‘portion of metal wiring that serves as an

electrode, and that has a greater thickness than the non-electrode portion of the metal wiring.” Prelim. Resp. 26–28.

Patent Owner fails to identify any statements in the specification or prosecution history that define (implicitly or explicitly) or disavow subject matter such that the claimed “first electrode portion” is limited in the manner proposed by Patent Owner. Patent Owner merely cites to a statement in the prosecution history describing “one embodiment of the present invention.” *Id.* (citing Ex. 1004, 82). Patent Owner fails to explain sufficiently how this statement in the prosecution history limits the scope of the claims.

Based on the current record and for purposes of institution, we determine that “first electrode portion” is not limited to an “external electrode portion” or a “portion of metal wiring that serves as an electrode, and that has a greater thickness than the non-electrode portion of the metal wiring.”

B. Level of Ordinary Skill

Petitioner’s declarant, Dr. Suhling, opines that a person of ordinary skill in the art of the ’001 patent would have had:

i) a bachelor-level degree in mechanical engineering, materials science, electrical engineering, or a related field and at least 3–5 years of experience in the design/development of semiconductor packages; ii) a Master’s level degree in mechanical engineering, materials science, electrical engineering, or a related field and at least 1–3 years of experience in the design/development of semiconductor packages, or iii) a PhD-level degree in mechanical engineering, materials science, electrical engineering, or a related field and at least some experience in the area of semiconductor packaging.

Ex. 1002 ¶ 21.

Patent Owner does not propose an alternative definition for the level of ordinary skill in the art, or otherwise comment on Dr. Suhling's proposed definition. *See* Prelim. Resp. 23.

We determine on the current record that the level of ordinary skill proposed by Dr. Suhling, not including the qualifiers "at least," is consistent with the challenged patent and the asserted prior art and we therefore adopt that level for the purposes of this decision.

C. Asserted Anticipation by Narizuka

Petitioner contends that claims 1–18 of the '001 patent are unpatentable under 35 U.S.C. § 102(b) as anticipated by Narizuka. Pet. 2, 16–40. Relying in part on the testimony of Dr. Suhling, Petitioner explains how Narizuka purportedly discloses each limitation of the claims. *Id.* at 16–40.

1. Summary of Narizuka

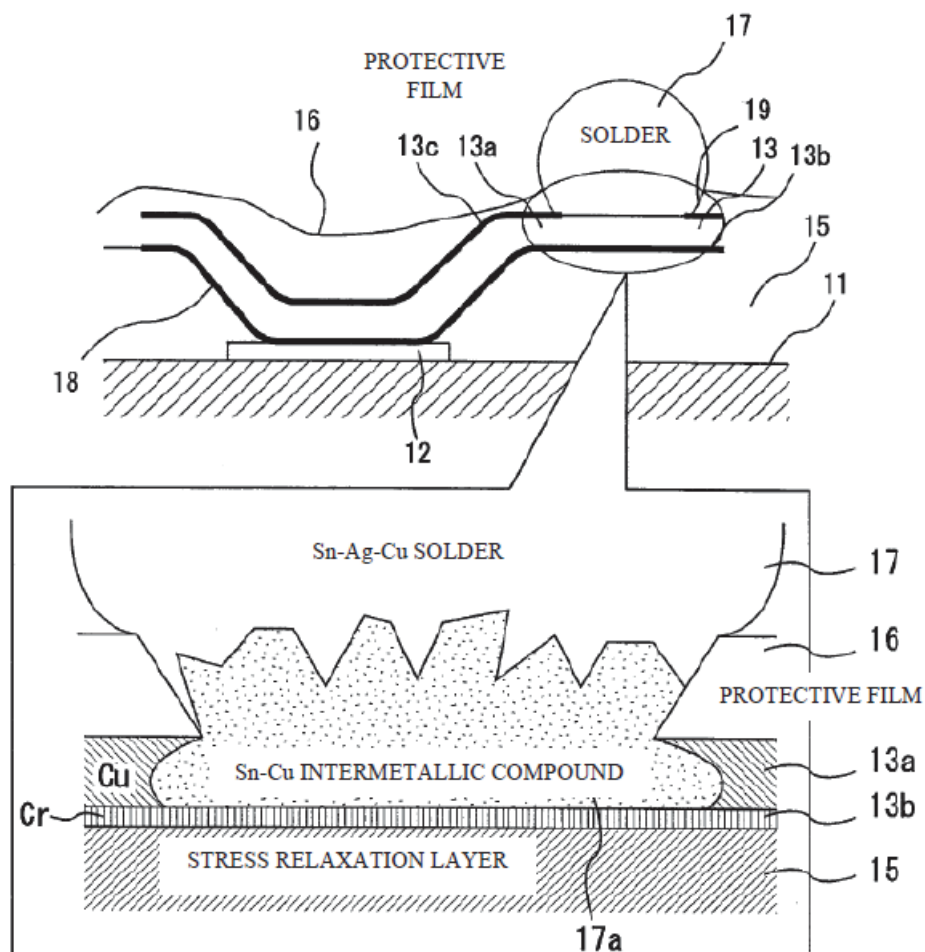
Narizuka is a PCT Application Publication that describes a wiring board and a semiconductor device "having high density and high connection reliability." Ex. 1012, [57].⁵ According to Narizuka, "when a wiring layer is directly connected to a solder in order to connect a wiring board to an external circuit, a phenomenon (solder damage) occurs, wherein element atoms constituting the solder and element atoms constituting the wiring layer diffuse mutually at the time of solder connection or by the subsequent changes over time, causing the wiring structure material to disappear." *Id.* at 1:17–20. Narizuka states that "[a]n alloy layer is produced from the

⁵ All citations to Narizuka are citations to the certified English translation at pages 1–33 of Exhibit 1012. Ex. 1012, 1–33, 67.

component of the solder and the wiring in connection with such a phenomenon, causing adverse effects such as the connecting part becoming brittle.” *Id.* at 1:20–2:1. Narizuka states that “[i]f the solder damage further advances, the solder will reach to the lower surface of a wiring material, causing loss of adhesiveness between the wiring material and the under layer, . . . resulting in a defective product.” *Id.* at 2:1–3.

Figure 1 of Narizuka, below, illustrates a wiring board and semiconductor device according to the invention disclosed therein:

FIG. 1



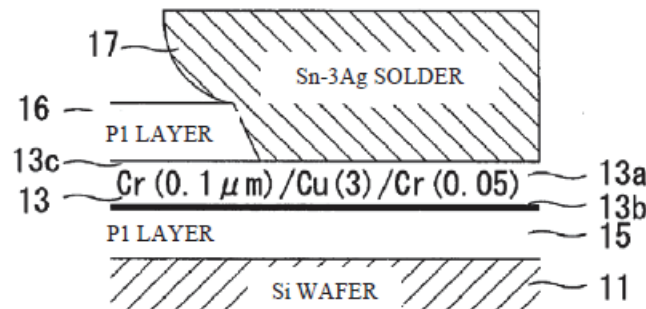
Id. at 8:5–11. As illustrated in Figure 1 above and according to Narizuka, electrode 12 is formed on substrate 11, wiring 13 is connected to electrode 12, insulation film 15 is provided between wiring 13 and substrate 11, protective film 16 is provided with a hole for the connection to solder 17 for protecting the surface of wiring 13, and solder 17 is provided on the portion opened in protective film 16 and is connected and mounted to the electrode of an external circuit, such as a package board. *Id.* Narizuka discloses that wiring 13 “is formed by laminating a Cu layer 13a with a thickness of about 0.1–10 μm . . . into the portion that connects to an external circuit.” *Id.* at 8:14–17. Narizuka also discloses that “Cu or Ti thin film layer 13b [has] a thickness of about 0.05–1.0 μm on the under layer 15 side” and that “Cr thin film layer 13c [has] a thickness of about 0.01–0.3 μm thick on the protective film side 16 side.” *Id.* at 8:14–17.

Narizuka states that “the connection between the solder 17 and the Cu layer of wiring . . . is a key feature of the present invention.” *Id.* at 10:21–22. Narizuka discloses that “the connection is basically achieved by the alloy of Sn and Cu” and that “the reaction of alloy formation of Cu and Sn influences the resistance against solder damage.” *Id.* at 11:3–4. Narizuka states that by setting particular reflow times depending on the thickness of the Cu layer 13a, “the connection can basically be achieved by the alloy 17a of Sn and Cu (Sn-Cu intermetallic compound), and the solder can reach the under layer 13b of Cr or Ti and the solder can connect to the under layer 13 of Cr or Ti, thereby the connection strength and reliability can be secured.” *Id.* at 11:16–12:2. According to Narizuka, “[a] shown by an enlarged drawing in FIG. 1, by a reflow, the main component Sn reacts with Cu to

form an alloy so as to diffuse and connect the Cr (Ti) layer 13b to establish a solder connection.” *Id.* at 12:3–5.

Figure 4 of Narizuka, below, illustrates “a connection structure between a wiring and a solder”:

FIG. 4



Id. at 12:6–7. As shown in Figure 4 above, wiring 13 “consists of three layers of Cr thin film layer 13b (about 0.1 μm in thickness), a Cu layer 13[a], and a Cr thin film layer 13c (about 0.05 μm).” *Id.* at 12:7–11.

2. Analysis

a. Claim 1

Petitioner cites to passages of Narizuka and identifies elements illustrated in Figures 1, 3(c), 4, and 8 of Narizuka that purportedly correspond to the limitations of claim 1. Pet. 18–26. Petitioner contends that Narizuka discloses “two different configurations” of a first electrode portion formed on a semiconductor element, as illustrated in Petitioner’s annotated versions of Figures 1 and 3(c) of Narizuka, below:

intermetallic compound) to the claimed diffusion layer formed between the first electrode portion and the second electrode portion. *Id.* at 24–26.

Patent Owner argues that Narizuka does not disclose “a first electrode portion formed on the semiconductor element, said first electrode portion comprising a first metal component.” Prelim. Resp. 34–39. Specifically, Patent Owner argues that the area identified by Petitioner for the first configuration “does not have a greater thickness than the non-electrode portion of the metal wiring.” *Id.* at 36. Patent Owner also argues that Petitioner’s modified Figure 3(c) “is not found in Narizuka and is not supported by its teachings.” *Id.* at 36–39.

Patent Owner further argues that Narizuka does not teach a diffusion layer “formed between” the first and second electrode portion because Narizuka teaches that the solder diffuses through the copper layer “to surely reach the under layer of Cr or Ti.” *Id.* at 40–42 (quoting Ex. 1012, 10:2–4). Patent Owner argues that, “consistent with” the teachings in Narizuka, “no copper remains between the Cr layer and the Sn-Cu alloy layer.” *Id.* at 41. Patent Owner also disagrees with Petitioner’s contention, supported by Petitioner’s declarant, that one of skill in the art “would have appreciated that at least some of the Cu of Narizuka’s ‘first electrode portion’ remains in non-intermetallic form.” *Id.* at 42 (quoting Pet. 26). Patent Owner contends that “one of skill in the art would understand that Narizuka teaches the alloy layer should ‘sufficiently reach’ the Cr or Ti under layer by consuming the entire thickness of the Cu layer.” *Id.* at 43.

Having reviewed the record, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that claim 1 is unpatentable as anticipated by Narizuka. For

example, Petitioner sufficiently shows that Narizuka discloses the claimed first electrode portion comprising a first metal component by disclosing wiring layers 13a and 13b, which include either copper and chromium or copper and titanium. Pet. 19–24 (citing, e.g., Ex. 1012, Figs. 1, 3(c), 3(d), 5:12–14, 8:14–17, 12:6–11; Ex. 1002 ¶¶ 69–71). Petitioner also sufficiently shows that Narizuka discloses the claimed second electrode portion comprising a second metal component by disclosing solder ball 17, which includes tin. *Id.* at 24–25 (citing Ex. 1012, Figs. 1, 3(c), 4:7–8, 10:21–11:2, 12:3–11; Ex. 1002 ¶¶ 74, 75). Petitioner also sufficiently shows that Narizuka discloses the claimed diffusion layer comprising the first and second metal components by disclosing the alloy 17a of tin and copper formed between the first electrode portion and the second electrode portion. *Id.* at 25–26 (citing Ex. 1012, Fig. 1, Abstract, 11:18–12:2; Ex. 1002 ¶ 76).

Patent Owner’s arguments are not persuasive at this preliminary stage and on the current record. For example, Patent Owner attempts to distinguish Narizuka based on a construction of “first electrode portion,” which we do not adopt on the current record as explained in Section II.A above. *See* Prelim. Resp. 36. Also, Patent Owner’s statements regarding the diffusion layer and the purported knowledge of one of ordinary skill in the art are unsupported attorney argument and insufficiently explained. *See id.* at 40–43.

b. Claims 2–9

Claim 2 depends from claim 1 and adds that “said first metal component includes copper and said second metal component includes tin.” Claim 3 depends from claim 1 and recites further limitations directed to a third electrode portion and a metal wiring. Claims 4–8 depend from claim 3

and add further limitations regarding the metal wiring, the third electrode portion, an insulating film, and/or an insulating resin layer. Claim 9 depends from claim 1 and adds a limitation directed to a wiring electrode. Petitioner asserts that Narizuka discloses the limitations recited in dependent claims 2–9. Pet. 26–40.

Patent Owner does not raise in its Preliminary Response any arguments specific to the limitations added in claims 2–9. *See* Prelim. Resp. 46–47.

Having reviewed the record, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that claims 2–9 are unpatentable as anticipated by Narizuka. For example, Petitioner sufficiently shows that Narizuka discloses a third electrode portion (electrode 12) on the surface of semiconductor element, which is connected to wiring 13. *See* Pet. 27–29 (citing, e.g., Ex. 1012, Figs. 1, 3(d), Abstract, 4:11–13, 5:8–14, 8:5–11). Petitioner also sufficiently shows that Narizuka discloses an insulating film 16 formed on metal wiring and an insulating resin layer 15 between the surface of the semiconductor element and metal wiring. *Id.* at 29–34 (citing, e.g., Ex. 1012, Figs. 1, 3(c), 3(d), 5:11–14, 5:16–17, 8:12–13, 10:18–20, 12:9–11).

c. Claim 10

Claim 10 has the same limitations as claim 1 but adds “said first electrode portion and said diffusion layer have a combined thickness in the range of 10 μm to 20 μm .” As explained above, Petitioner asserts that, in Narizuka, the first electrode portion is layers 13a and 13b and the diffusion layer is the alloy 17a. Petitioner asserts that Narizuka discloses that 13a has a thickness between 0.1 and 10 microns and that 13b has a thickness

between 0.05 microns and 1 micron. Pet. 37 (citing Ex. 1012, 8:14–15). Petitioner relies on testimony from Dr. Suhling regarding what the thickness of the diffusion layer “would be,” citing a different reference (Zakraysek). *Id.* at 37–38 (citing Ex. 1002 ¶¶ 99–101; Ex. 1010).

Patent Owner argues that Narizuka does not disclose “said first electrode portion and said diffusion layer have a combined thickness in the range of 10 μm to 20 μm .” Prelim. Resp. 43–46. Patent Owner argues that “Petitioner’s reliance on Zakraysek is fundamentally flawed” because Zakraysek describes solder diffusion at a different temperature and time, and, according to Patent Owner, “[o]ne of skill in the art would recognize that reflows at different temperatures and times can drastically change the thickness of solder diffusion.” *Id.* at 44. Patent Owner also argues that “the combined thickness of the first electrode portion and diffusion layer is not a sum of the individual thicknesses . . . since the diffusion layer grows into the first electrode portion.” *Id.* at 45.

Having reviewed the record, we determine that the information presented does not establish a reasonable likelihood that Petitioner would prevail in showing that claim 10 is unpatentable as anticipated by Narizuka. Petitioner fails to show that Narizuka expressly or inherently discloses the claimed combined thickness of the first electrode portion and the diffusion layer in the range of 10 μm to 20 μm . Although Petitioner points to a disclosure of the thickness of what Petitioner alleges constitutes the claimed first electrode portion, Petitioner fails to identify an express disclosure in Narizuka of the thickness of the claimed diffusion layer. *See* Pet. 36–38. Nor does Petitioner contend or sufficiently explain that Narizuka necessarily discloses a particular thickness of the diffusion layer. *Id.* Rather, Petitioner

relies on information from another reference and testimony of its expert, who opines what the thickness “would typically be.” *Id.* at 37–38 (citing Ex. 1010; Ex. 1002 ¶¶ 99–100).

Petitioner thus fails to make a sufficient showing that claim 10 and claims 11–16, which depend from claim 10 and for which Petitioner does not add any additional analysis regarding the claimed thickness range (*see* Pet. 38–40), are anticipated by Narizuka.

D. Asserted Anticipation by Takizawa

Petitioner contends that claims 1–7, 9–16, and 18 of the ’001 patent are unpatentable under 35 U.S.C. § 102(a) as anticipated by Takizawa. Pet. 2–3, 40–59. Relying in part on the testimony of Dr. Suhling, Petitioner explains how Takizawa allegedly discloses each claim limitation. *Id.* at 40–59. Petitioner also cites to Lau⁶ in connection with claims 5 and 14 and cites to Hashimoto in connection with claims 7 and 16. *See id.* at 51–52, 55, 59.

1. Summary of Takizawa

Takizawa is a published German patent application that describes “forming a copper-tin alloy layer between a solder ball and a wiring layer to thereby prevent occurrence of breakage and cracking at a connection between a solder ball and a wiring layer.” Ex. 1014, 3:36–38.⁷ Takizawa discloses a semiconductor device including (i) a semiconductor chip, (ii) a wiring making electrical connection with the semiconductor chip and containing copper (Cu), (iii) “a solder ball making contact with the wiring

⁶ Lau, John H., Chapter 10: Wafer-Level Packaging, *Low Cost Flip Chip Technologies* (The McGraw-Hill Companies, Inc. 2000) (Ex. 1007, “Lau”).

⁷ All citations to Takizawa are citations to the certified English translation at pages 1–18 of Exhibit 1014. Ex. 1014, 1–18, 37.

and containing tin (Sn),” and (iv) “a layer made of copper-tin (Cu-Sn) alloy, sandwiched between the wiring and the solder ball, and having a thickness equal to or greater than 1.87 micrometers.” *Id.* at 3:41–44. Takizawa states that “tin contained in the solder ball is diffused in liquid into the wiring layer containing copper, resulting in that a copper-tin alloy layer . . . formed between the solder ball and the wiring layer, having a thickness sufficient to prevent the solder ball from being separated from the wiring layer.” *Id.* at 4:1–3.

Figure 5A below is a cross-sectional view of Takizawa’s semiconductor device and Figure 5B below is an enlarged view of the connection between the wiring layer and the solder ball:

FIG. 5A

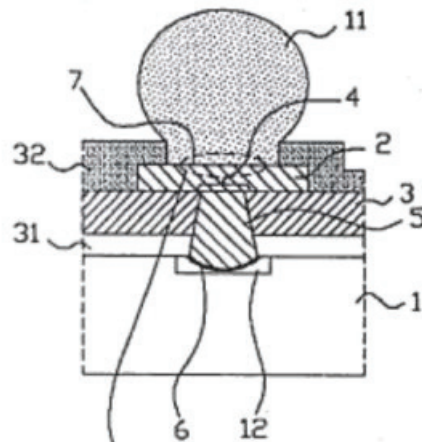
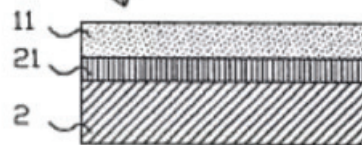


FIG. 5B



Id. at 4:21–23. As illustrated above, the semiconductor device includes “solder ball [11] mounted on the wiring layer 2 in the land 7,” a layer 21 (illustrated in Figure 5B) “made of copper-tin alloy and sandwiched between the solder ball [11] and the wiring layer 2,” metal 5 filled in “through-hole 4

formed through both the film substrate 3 and the polyimide adhesive layer 31,” and gold (Au) layer 6 covering metal 5. *Id.* at 4:38–44. According to Takizawa, wiring layer 2 contains copper and solder ball 11 contains tin. *Id.* at 4:45–46.

Takizawa states that “[t]he Cu-Sn alloy layer 21 makes it possible to prevent occurrence of breakage and cracking across the solder ball 11 and the wiring layer 2, preventing that the solder ball 11 is separated from the wiring layer 2 due to the breakage and/or cracking across the solder ball 11 and the wiring layer.” *Id.* at 4:62–5:2. According to Takizawa, “[t]he Cu-Sn alloy layer 21 has a thickness preferably of 1.87 micrometers or greater, more preferably of 2 micrometers or greater, and most preferably of 3 micrometers or greater.” *Id.* at 5:4–5.

2. Analysis

a. Claim 1

Petitioner cites to passages of Takizawa and identifies elements illustrated in Figures 5A, 5B, and 6B of Takizawa that purportedly correspond to the limitations of claim 1. Pet. 43–47.

Patent Owner argues that Takizawa does not disclose the claimed first electrode portion as defined under Patent Owner’s proposed construction because the portion of the metal wiring that serves as an electrode does not have a thickness greater than that of the non-electrode portion of the metal wiring. Prelim. Resp. 48–49. Patent Owner also argues that wiring layer 2 in Takizawa is not “formed on the semiconductor element,” as required by claim 1. *Id.* at 49–50. Rather, according to Patent Owner, “wiring layer 2 is formed ‘on an upper surface of a film substrate 3’ before the substrate 3 is

attached to the semiconductor chip 1.” *Id.* at 49 (quoting Ex. 1014, 2:31–47).

Having reviewed the record, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that claim 1 is unpatentable as anticipated by Takizawa. For example, Petitioner sufficiently shows that Takizawa discloses the claimed first electrode portion comprising a first metal component by disclosing a portion of wiring 2 below the solder ball, which includes copper. Pet. 44–45 (citing, e.g., Ex. 1014, Figs. 1A, 5A, 2:19, 4:45–46, 5:14). Petitioner also sufficiently shows that Takizawa discloses the claimed second electrode portion comprising a second metal component by disclosing solder ball 11, which includes tin. *Id.* at 45–46 (citing, e.g., Ex. 1014, Figs. 1A, 5A, 4:52–53). Petitioner also sufficiently shows that Takizawa discloses the claimed diffusion layer comprising the first and second metal components by disclosing the Sn-Cu alloy layer 21 formed between the first electrode portion and the second electrode portion. *Id.* at 46–47 (citing, e.g., Ex. 1014, Figs. 1B, 5B, 6B, 2:28–29, 4:61–5:3).

Patent Owner’s arguments are not persuasive at this preliminary stage and on the current record. For example, Patent Owner attempts to distinguish Takizawa based on a construction of “first electrode portion,” which we do not adopt on the current record as explained in Section II.A above. *See* Prelim. Resp. 48–49. Also, Patent Owner’s argument that Takizawa’s metal wiring is not “formed on” the substrate is not persuasive at this preliminary stage because claim 1 is directed to a semiconductor device, not a method of manufacturing such a device, and because Patent Owner fails to explain sufficiently or provide evidence supporting a construction

that “formed on” the semiconductor element means formed *directly* on the semiconductor element (i.e., with no other components or materials therebetween). *See id.* at 49–50.

b. Claim 10

Claim 10 has the same limitations as claim 1 but adds “said first electrode portion and said diffusion layer have a combined thickness in the range of 10 μm to 20 μm .” As explained above, Petitioner asserts that, in Takizawa, the first electrode portion is the portion of wiring 2 below the solder ball and the diffusion layer is the Cu-Sn alloy layer 21. Petitioner also asserts that Takizawa discloses that wiring 2 for the embodiment shown in Figure 5A is 18 microns thick and that the Cu-Sn alloy layer for the embodiments shown in Figures 5B and 6B is 1.87 microns thick. Pet. 57–58 (citing, e.g., Ex. 1014, 5:16, 6:32–33). Thus, Petitioner asserts that Takizawa discloses that the first electrode portion and the diffusion layer have a combined thickness of 19.87 microns. *Id.* at 58.

Patent Owner raises the same arguments for claim 10 that is raises for claim 1. Prelim. Resp. 48–51. For the reasons explained above in connection with claim 1, and because Petitioner sufficiently shows that Takizawa discloses that the first electrode portion and the diffusion layer have a combined thickness in the range of 10 μm to 20 μm , we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that claim 10 is unpatentable as anticipated by Takizawa.

c. Claims 2–7, 9, 11–16, and 18

Claim 2 depends from claim 1 and adds that “said first metal component includes copper and said second metal component includes tin.”

Claim 3 depends from claim 1 and recites further limitations directed to a third electrode portion and a metal wiring. Claims 4–7 depend from claim 3 and add further limitations regarding the metal wiring, the third electrode portion, an insulating film, and/or an insulating resin layer. Claim 9 depends from claim 1 and adds a limitation directed to a wiring electrode. Claims 11–16 and 18 add the same limitations added by claims 2–7 and 9, respectively, but depend from claim 10 rather than claim 1.

Petitioner asserts that Takizawa discloses the limitations recited in claims 2–7, 9, 11–16, and 18. Pet. 47–59. Patent Owner does not raise in its Preliminary Response any arguments specific to the limitations added in these dependent claims. *See* Prelim. Resp. 51–52.

Having reviewed the record, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that claims 2–7, 9, 11–16, and 18 are unpatentable as anticipated by Takizawa. For example, Petitioner sufficiently shows that Takizawa discloses a third electrode portion (electrode 12) on the surface of semiconductor element, which is connected to metal 5 and wiring 2. *See* Pet. 48–49 (citing, e.g., Ex. 1014, Figs. 1A, 5A, 2:17–18, 4:47–49). Petitioner also sufficiently shows that Narizuka discloses an insulating film (solder resist 32) formed on metal wiring and an insulating resin layer (e.g., film substrate 3 and adhesive layer 31) between the surface of the semiconductor element and metal wiring. *Id.* at 49–51 (citing, e.g., Ex. 1014, Figs. 1A, 5A, 2:14–15, 4:38–44), 53–55 (citing, e.g., Ex. 1014, Figs. 1A, 1B, 5A, 2:34–37, 4:38–44, 5:15–19).

E. Asserted Obviousness Over Takizawa and Narizuka

Claims 8 and 17 depend from claims 3 and 12, respectively, and add the limitation “wherein the metal wiring has a thickness in the range of 0.01 μm to 8 μm .” Petitioner contends that claims 8 and 17 of the ’001 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Takizawa and Narizuka. Pet. 3, 59–62.

Specifically, Petitioner asserts that even though Takizawa discloses that wiring 2 of Figure 5A is 18 microns thick, “that disclosure is only exemplary” and “selection of the metal wiring was simply a matter of design choice.” *Id.* at 59–60. Petitioner contends that “one of skill in the art would have known to create wiring within the claimed range using industry standard techniques and processes.” *Id.* at 60. Petitioner asserts that “[o]ne example of such wiring thicknesses is [in] Narizuka,” which according to Petitioner discloses that the thickness of the copper layer ranges from about 0.1 μm to about 10 μm . *Id.* at 60–61.

Patent Owner argues that Petitioner’s argument “is belied by the fact that the claims require the thickness of the metal wiring (specifically, the non-electrode portion) to be less than the thickness of the first electrode portion,” and that “neither Takizawa nor Narizuka suggests increasing the wiring thickness at the location of the solder ball electrode.” Prelim. Resp. 54. Patent Owner also argues that “Petitioner fails to specify *how* or *why* one of skill in the art would have decided to reduce the thickness of wiring of Takizawa from 18 μm to a thickness in the range of 0.1 μm to about 10 μm .” *Id.* at 55 (bold emphasis omitted).

Having reviewed the record, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in

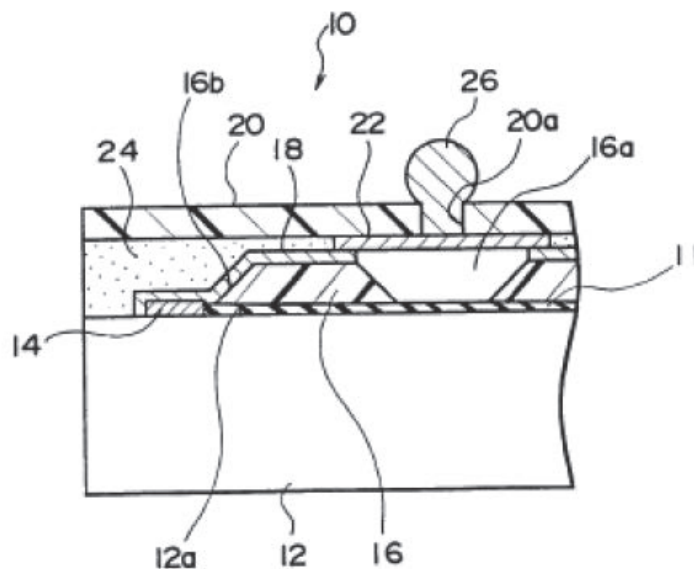
showing that claims 8 and 17 are unpatentable as obvious over Takizawa and Narizuka. For example, Petitioner sufficiently shows for purposes of institution that the combination of Takizawa and Narizuka teaches metal wiring having a thickness in the range of 0.01 μm to 8 μm and that one of skill in the art would have known to create wiring within the claimed range. Patent Owner's distinction regarding the thickness of the first electrode portion is based on a proposed claim construction which we do not adopt at this stage.

F. Asserted Obviousness Over Takizawa and Hashimoto

1. Summary of Hashimoto

Hashimoto is a PCT patent application publication that describes “[a] semiconductor device capable of effectively absorbing thermal stresses.”

Ex. 1015, [57].⁸ Figure 1 of Hashimoto is shown below:



⁸ All citations to Hashimoto are citations to the certified English translation at pages 1–45 of Exhibit 1015. Ex. 1015, 1–45, 91.

Figure 1 above shows a cross-sectional view of semiconductor device 10. *Id.* at 7:14–16. Hashimoto discloses that “intermediate layer 16 is made of an insulating resin, for example, a polyimide resin.” *Id.* at 8:9–13. According to Hashimoto, “when the semiconductor device 10 is mounted to a circuit board (not shown), this layer can relax the stress occurred due to the difference in the coefficient of thermal expansion between the semiconductor chip 12 and the mounted circuit board.” *Id.*

2. Analysis

Claims 7 and 16 depend from claims 3 and 12, respectively, and further require that the semiconductor device include “an insulating resin layer formed between the surface of the semiconductor element and the metal wiring, wherein the metal wiring is formed along a surface of the insulating resin layer.” Petitioner contends that the subject matter of claims 7 and 16 of the '001 patent would have been obvious over Takizawa and Hashimoto. Pet. 3, 62–63.

Specifically, Petitioner asserts that “it would have been obvious to use” the insulating resin material disclosed in Hashimoto, “and the benefits of using that material are expressly disclosed in Hashimoto itself.” *Id.* at 62. Petitioner argues, relying on the testimony of Dr. Suhling, that “one of skill in the art would use Hashimoto’s ‘insulating resin’ polyimide to construct Takizawa’s substrate 3 in both Fig. 5A and prior art Fig. 1A embodiments, where that substrate is already disclosed as being made of polyimide.” *Id.* at 62–63. According to Petitioner, “[i]n such a combination, expressly motivated by Hashimoto itself, the benefits of the material disclosed in Hashimoto would be imparted to Takizawa’s existing semiconductor device, without altering its overall existing structure.” *Id.* at 63.

Patent Owner argues that the film substrate in Takizawa is not “formed between” wiring layer 2 and the surface of the semiconductor chip 1. Prelim. Resp. 57. Rather, according to Patent Owner, “the film substrate 3 is formed between the wiring layer 2 and the adhesive layer 31 to complete the tape substrate 93,” and “[t]he semiconductor chip 1 is then mounted to the tape substrate 93.” *Id.* Patent Owner also argues that Petitioner fails to specify how or why one of skill in the art would have been motivated to substitute the polyimide resin layer of Hashimoto for the polyimide substrate layer of Takizawa. *Id.* at 57–58.

Having reviewed the record, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that claims 7 and 16 are unpatentable as obvious over Takizawa and Hashimoto. Patent Owner’s argument that Takizawa’s film substrate is not “formed between” the surface of the semiconductor element and the metal wiring is not persuasive at this preliminary stage because claims 7 and 16 are directed to semiconductor devices, not methods of manufacturing such devices. Petitioner also provides, for institution purposes, sufficient reason to combine the teachings of Takizawa and Hashimoto.

III. CONCLUSION

For the above reasons, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that (i) claims 1–9 are unpatentable as anticipated by Narizuka, (ii) claims 1–7, 9–16, and 18 are unpatentable as anticipated by Takizawa, (iii) claims 8 and 17 are unpatentable as obvious over Takizawa and Narizuka, and (iv) claims 7 and 16 are unpatentable as obvious over Takizawa and Hashimoto.

At this preliminary stage, the Board has not made a final determination with respect to the patentability of the challenged claims or any underlying factual and legal issues.

IV. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted as to (i) claims 1–9 on the ground of anticipation by Narizuka, (ii) claims 1–7, 9–16, and 18 on the ground of anticipation by Takizawa, (iii) claims 8 and 17 on the ground of obviousness over Takizawa and Narizuka, and (iv) claims 7 and 16 on the ground of obviousness over Takizawa and Hashimoto.

FURTHER ORDERED that no other ground set forth in the Petition is authorized for *inter partes* review; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this decision.

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