

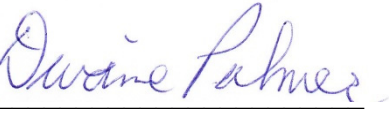
CERTIFICATE OF TRANSLATION ACCURACY

I, Dwaine Palmer, declare:

1. I am a professional translator specializing in translating Japanese to English.
2. I have over 18 years of experience translating thousands of technical documents and patents from Japanese to English.
3. I certify that the Japanese to English translation of the laid-open patent application publication document identified below is true and correct to the best of my knowledge and ability.

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I hereby certify under penalty of perjury that the foregoing is true and correct. Executed this 13th day of March, 2018 in the Utah County of the state of Utah.

By: 

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(54) Semiconductor Device and Method of Manufacturing Semiconductor Device

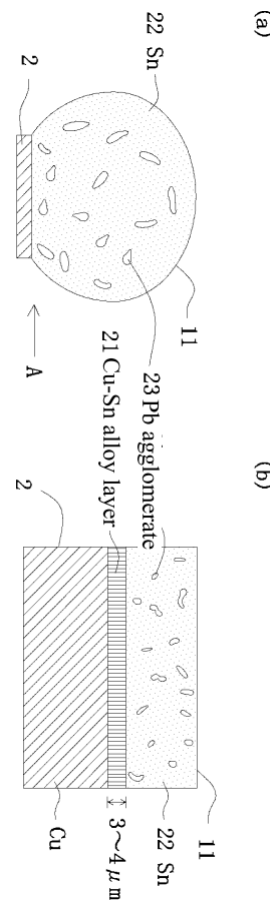
(57) ABSTRACT

[PROBLEM]

To provide a semiconductor device obtained as a device with favorable yield.

[RESOLUTION MEANS]

The semiconductor device of the present invention has a wiring part 2 containing copper connected to a semiconductor chip, and a solder ball 11 containing tin bonded to the wiring part 2, wherein a Cu-Sn alloy layer 21 with a thickness of approximately 1.87 μm or more is formed on the bonding part of the solder ball 11 and the wiring part 2. Thereby the aforementioned objective can be achieved.



What Is Claimed Is:

[Claim 1]

A semiconductor device, comprising: a wiring part containing copper connected to a semiconductor chip, and a solder ball containing tin bonded to the wiring part; wherein a Cu-Sn alloy layer with a thickness of approximately $1.87\text{ }\mu\text{m}$ or more is formed on the bonding part of the solder ball and the wiring part.

[Claim 2]

A semiconductor device, comprising: a wiring part containing copper connected to a semiconductor chip, a solder ball containing tin bonded to a main surface of the wiring part, and a film substrate that contacts the wiring part on an opposite side surface as the bonding surface between the wiring part and the solder ball, wherein a hole is provided that passes through the film substrate from the wiring part to the surface on the opposite side as the bonding surface to the wiring part of the film substrate, a metal is filled into the hole, a gold layer is formed on the metal surface of the opening part of the hole, a Cu-Sn alloy layer with a thickness of approximately $1.87\text{ }\mu\text{m}$ or more on the bonding part between the solder ball and the wiring part.

[Claim 3]

The semiconductor device according to claim 1 or claim 2, wherein a Pb agglomerate is formed in the solder ball, and the dispersion density per unit cross-sectional area of the Pb agglomerates is 20×10^4 particles/ mm^3 or higher.

[Claim 4]

The semiconductor device according to claim 1 or claim 2, wherein a Pb agglomerate is formed in the solder ball, and the average cross-sectional area of the Pb agglomerate is $10\text{ }\mu\text{m}^2$ or lower.

[Claim 5]

The semiconductor device according to claim 3 or claim 4, wherein the solder ball and a printed board are bonded, and a bonded part between the solder ball and the wiring part is strengthened by the Cu-Sn alloy layer.

[Claim 6]

A method of manufacturing a semiconductor device, comprising: disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn on a land provided on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[Claim 7]

A method of manufacturing a semiconductor device, comprising: disposing a wiring part containing copper on a main surface of a film substrate, protecting the surface of the wiring part using resist, providing a hole that passes through the film substrate from the film substrate to the wiring part, and then filling the hole with metal, forming a gold layer on the metal surface of the opening part of the hole; bonding the semiconductor chip and the formed surface of the gold layer of the film substrate, disposing a solder ball containing Sn on a land provided on the wiring part, and then maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[Claim 8]

The method of manufacturing a semiconductor device according to claim 6 or claim 7, wherein a thin film of Au is formed on the surface of the land, and then a solder ball is disposed.

[Claim 9]

A semiconductor device, wherein a Cu-Sn alloy layer with a thickness of $3\text{ }\mu\text{m}$ or more is formed on the bonded part between the solder ball and the wiring part, obtained by disposing a wiring part containing

copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[Claim 10]

A semiconductor device, wherein the dispersion density per unit cross-sectional area of Pb agglomerates formed in the solder ball is 20×10^4 particles/ mm^3 or less, obtained by disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn and Pb on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[Claim 11]

A semiconductor device, wherein the average cross-sectional area of the Pb agglomerates formed in the solder ball is $10\text{ }\mu\text{m}^2$ or less, obtained by disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn and Pb on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[Claim 12]

A semiconductor device, wherein the solder ball and the printed board are bonded together, and the bonded part between the solder ball and the wiring part is strengthened by a Cu-Sn alloy layer, obtained by disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn and Pb on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

DETAILED DESCRIPTION OF THE INVENTION

[0001]

TECHNICAL FIELD OF THE INVENTION

The present invention relates to a semiconductor device and to a method of manufacturing the semiconductor device. In particular, the present invention relates to a semiconductor device obtained as a device with favorable yield, and a method of manufacturing a semiconductor device with high productivity.

BACKGROUND TECHNOLOGY

[0002]

In recent years, new forms of semiconductor devices have been successively developed in order to respond to the demand for higher performance, smaller size, lighter weight, and higher-speed of electronic devices. For example, the aforementioned electronic devices are made smaller and lighter by miniaturizing and thinning a semiconductor device by high integration of a semiconductor chip.

[0003]

As illustrated in FIG. 7(a), a conventional semiconductor device, includes: a wiring part 2 containing copper connected to a semiconductor chip 1, a solder ball 101 containing tin bonded to a land 7 formed on a surface of the wiring part 2, and a film substrate 3 that contacts the wiring part 2 on an opposite side surface as the bonding surface between the wiring part 2 and the solder ball 101, wherein a

hole 4 is provided that passes through the film substrate 3 from the wiring part 2 to the surface on the opposite side as the bonding surface to the wiring part 2 of the film substrate 3, a metal 5 is filled into the hole 4, and a gold layer 6 is formed on the metal 5 surface of the opening part of the hole 4. Furthermore, the land 7 is a hole provided on the wiring part 2 by shaving a predetermined location of the resist 32 in order to dispose a solder ball 101, and a Au layer 8 is formed on the surface of the land 7. Note that the Au layer 8 is illustrated in FIG. 7, but this Au layer 8 is thought to diffuse into the solder ball 101 by heat treatment of temperature cycle testing or the like performed after manufacturing this device, and it is hypothesized that the Au layer is not disposed on the wiring part 8 [Translator's note: presumably wiring part 2] after heat treatment. FIG. 8 illustrates an expanded view of the on the part between the wiring part 2 and the solder ball 101 illustrated in FIG. 7(a). Note that FIG. 8 illustrates an example (schematic diagram) of a conventional semiconductor device where the solder ball 101 is formed from a Sn-Pb eutectic solder (Sn content: 63%, Pb content: 37%). With the conventional semiconductor device illustrated in FIG. 7(a), the solder ball 101 and the printed board 34 are bonded as illustrated in FIG. 7(c).

[0004]

Furthermore, the conventional semiconductor device illustrated in FIG. 7 is manufactured by the steps illustrated in FIG. 9 and FIG. 10. First, the first manufacturing step of forming a land 7 after attaching the wiring part 2 to the film substrate 3 is described while referring to FIG. 9. FIG. 9(a) through FIG. 9(h) are all cross-sectional diagrams of a portion where the solder ball 101 is disposed in a subsequent step on the film substrate 3. As illustrated in FIG. 9(a), a wiring part 2 containing Cu is disposed on a main surface of the film substrate 3. Furthermore, an adhesive 31 is applied to the surface on the opposite side as the surface where the wiring part 2 of the film substrate 3 is disposed. The film substrate 3 is made of a material that can withstand temperature conditions of 250°C or higher such as polyimide or the like, and the adhesive 31 is made of a polyimide system. Next, a wiring part 2 is patterned to a predetermined shape on the film substrate 3 illustrated in FIG. 9 (a) (refer to FIG. 9 (b)), and then a resist 32 is applied to the externally exposed surface of the wiring part 2 and the film substrate 3 (refer to FIG. 9(c)). Next, a hole 4 is formed passing through the film substrate 3 from the adhesive 31 to the wiring part 2 (refer to FIG. 9(d)). Formation of this hole 4 is formed using a tool such as laser or the like. Furthermore, a metal 5 such as Cu or Al or the like is filled into the hole 4 (refer to FIG. 9(e)), and then an Au layer 6 is formed on the surface of the metal 5 supposed at the opening part of the hole 4 (FIG. 9(f)). Furthermore, a land 7 for placing a solder ball in a subsequent step is disposed by providing a hole on the surface of the wiring part 2 (refer to FIG. 9(g)). Next, a thin film made of an Au layer 8 is formed on the surface of the land 7 (refer to FIG. 9(h)). The aforementioned steps provide a tape substrate 93 with a film substrate 3 on which the wiring part 2 is formed on a main surface. Note that FIG. 9 illustrates an

expanded view of one land 7 portion provided on the film substrate 3, where the film substrate 3 has a tape-like shape, and a plurality of lands 7 for providing the solder ball 101 in a subsequent step are formed on the film substrate 3.

[0005]

Next, a manufacturing step that provides a solder ball 101 on the land 7 after the semiconductor chip 1 is connected to the tape substrate 93 obtained by the steps illustrated in FIG. 9 is described while referring to FIG. 10. First, the tape substrate 93 obtained by the step illustrated in FIG. 9 is provided such that the side surface where the Au layer 6 is provided on the film substrate 3 is facing upward (refer to FIG. 10(a)), and then a stiffener 41 made of copper or stainless steel or the like is attached to both end parts of the tape substrate 93 (refer to FIG. 10(b)). The stiffener 41 is provided in order to secure the tape substrate 93 when the semiconductor chip 1 is provided on the tape substrate 93. Next, one semiconductor chip 1 is disposed between two stiffeners 41 on the tape substrate 93, and an electrode part 12 made of Al or the like provided on the semiconductor chip 1 is connected to the Au layer 6 on the aforementioned tape substrate 93 (refer to FIG. 10(c)). This connection is made by concomitantly using heat and ultrasonic waves using a bonding tool. Next, if necessary, a reinforcing resin 42 is injected and cured between the tape substrate 93 and the semiconductor chip 1, and thereby reinforcement is performed on the bonding part between the tape substrate 93 and the semiconductor chip 1 is performed (referred to FIG. 10(d)). The reinforcing resin 42 is a liquid resin such as epoxy resin or the like. Next, with the semiconductor chip 1, a lid part 43 made of Cu, Al, SiC, or the like is provided on the surface on the opposite side as the tape substrate 93 in order to protect the semiconductor chip 1, and then sealing below ambient pressure is performed (refer to FIG. 10 (e)). In this case, a conductive adhesive 44 such as a Ag paste or a Cu paste or the like is applied to the surface of the lid part 43 that connects with the semiconductor chip 1, the conductive adhesive 44 is heated and cured by sealing, and ambient pressure sealing is performed using a belt furnace or oven. Next, a solder ball 101 is attached while suctioning under reduced pressure onto each of the lands 7 on the wiring part 2 provided on the tape substrate 3 using a positioning tool 45 (refer to FIG. 10(f)), and then agglomerates (not illustrated in the drawings) is applied around the bonding part between the solder ball 101 and the land 7, and then the land 7 and the solder ball 101 are connected by re-flowing the solder ball 101. Next, if necessary, the flux used in the aforementioned step is washed off. Next, sorting and inspection or the like is performed after temperature cycle testing for determining the operating properties and the durability or the like towards physical damage, and then the device is mounted on the printed board 34 by bonding the printed board 34 and the solder ball 11 by reflowing the solder ball 11 to obtain the semiconductor device which is the final product (refer to FIG. 10(i)).

[0006]

PROBLEM TO BE RESOLVED BY THE INVENTION

However, the following problems exist with the conventional semiconductor device illustrated in FIG. 7. As described above, increased integration of semiconductor chips is proceeding in order to meet the demand for reducing the size and thinning of semiconductor devices in recent years. Increased integration of semiconductor chips creates a need for an increase in the number of pins per unit area of the semiconductor chip, and therefore the interval between the chips is smaller. In this case, the number of external terminals that are connected to a single semiconductor chip, or in other words the number of solder balls also increases, along with an increase in the number of pins disposed per unit area, and therefore the interval between the solder balls is smaller. Generally, as the interval between solder balls becomes smaller, the bonding area between the solder balls and wiring part per solder ball becomes smaller, so the bonding strength of the bonding part between the solder ball and the wiring part is weaker. In other words, with the conventional semiconductor device illustrated in FIG. 7, the bonding area of the wiring part 2 per solder ball 101 is smaller, so the bonding strength of the bonding part between the solder ball 101 and the wiring part 2 is weaker. Therefore, breaking and cracking can more easily occur near the bonding part between the solder ball 11 and the wiring part 2, and peeling of the solder ball 101 may occur due to these fractures and cracks. As a result, productivity of the semiconductor device is reduced, and there is a problem with poor yield.

[0007]

The present invention was achieved by focusing on the problems of the conventional technology. An object of the present invention is to provide a semiconductor device obtained as a device with favorable yield. Furthermore, another object of the present invention is to provide a manufacturing method for a semiconductor device that can improve productivity.

[0008]

In order to resolve the aforementioned problems, the present inventors performed extensive research related to improving the strength of the bonding part between the solder ball and the land. As a result, the present inventors were able to increase the strength of the bonding part by forming on a bonding part between the land and the solder ball a Cu-Sn alloy layer with sufficient thickness in order to prevent detachment of the solder ball, and conceived of the semiconductor device of the present invention based on the concept that a semiconductor device with favorable yield can be obtained by reducing fractures and cracks that occur around the bonding part. Furthermore, the present inventors conceived of a method of manufacturing the semiconductor device of the present invention based on a concept that a Cu-Sn alloy layer with sufficient thickness to prevent detachment of the solder ball can be formed on the bonding part by maintaining the semiconductor device with a solder ball provided on a land provided on the wiring part in an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[0009]

MEANS FOR SOLVING THE PROBLEMS

The first invention of the present application provided to resolve the

aforementioned problem is a semiconductor device, comprising: a wiring part 2 containing copper connected to a semiconductor chip, and a solder ball 11 containing tin bonded to the wiring part 2; wherein a Cu-Sn alloy layer 21 with a thickness of approximately 1.87 μm or more is formed on the bonding part of the solder ball 11 and the wiring part 2.

[0010]

Herein, if the Cu-Sn alloy layer formed on the bonding part of the wiring part of the solder ball has a thickness that is less than approximately 1.87 μm , the bonding part between the solder ball and the wiring part cannot have sufficient strength, there will be a possibility of breaking or cracking occurring to the bonding part during temperature cycle testing or the like, and preventing detachment of the solder ball will not be possible, so it is conceivable that the yield will drop. The semiconductor device of the first invention of the present application having the aforementioned configuration can reduce detachment of the solder ball caused by breaking or cracking in order to be able to reduce the occurrence of fractures and cracks near the bonding part by providing a wiring part containing copper connected to a semiconductor chip, and a solder ball containing tin bonded to the wiring part; wherein a Cu-Sn alloy layer with a thickness of approximately 1.87 μm or more is formed on the bonding part of the solder ball and the wiring part, and has a wiring part containing Cu connected to the semiconductor chip and a solder ball containing Sn bonded to the wiring part. Thereby, a semiconductor device can be obtained with favorable yield and that increases the reliability of the bonding part and increases the productivity of the semiconductor device.

[0011]

Furthermore, the second invention of the present application is a semiconductor device, comprising: a wiring part containing copper connected to a semiconductor chip, a solder ball containing tin bonded to a main surface of the wiring part, and a film substrate that contacts the wiring part on an opposite side surface as the bonding surface between the wiring part and the solder ball, wherein a hole is provided that passes through the film substrate from the wiring part to the surface on the opposite side as the bonding surface to the wiring part of the film substrate, a metal is filled into the hole, a gold layer is formed on the metal surface of the opening part of the hole, a Cu-Sn alloy layer with a thickness of approximately 1.87 μm or more on the bonding part between the solder ball and the wiring part.

[0012]

Herein, if a Cu-Sn alloy layer formed on the bonding part of the wiring part of the solder ball has a thickness that is less than approximately 1.87 μm , the bonding part between the solder ball and the wiring part cannot have sufficient strength, there will be a possibility of breaking or cracking occurring to the bonding part during temperature cycle testing or the like, and preventing detachment of the solder ball will not be possible, so it is conceivable that the yield will drop. However, the semiconductor device of the second invention of the present application having the aforementioned configuration can reduce detachment of the solder ball caused by breaking or cracking by reducing the occurrence of fractures and cracks near the bonding part, by forming a Cu-Sn alloy layer with a thickness of approximately 1.87 μm or more on the bonding part of the solder ball and the wiring part. Thereby, a

semiconductor device can be obtained with favorable yield and that increases the reliability of the bonding part and increases the productivity of the semiconductor device.

[0013]

Furthermore, the semiconductor device of the third invention of the present application is the semiconductor device of the first invention of the present application or the second invention of the present application, wherein a Pb agglomerate is formed in the solder ball, and the dispersion density per unit cross-sectional area of the Pb agglomerate is 20×10^4 particles/mm³ or higher.

[0014]

Herein, if the dispersion density per unit cross-sectional area of the Pb agglomerate that is formed is 20×10^4 particles/mm³ or less, distortion will easily occur in the solder ball due to the Pb agglomerates, there will be a possibility that breaking or cracking will occur in the bonding part during the temperature cycle testing or the like, and preventing detachment of the solder ball will not be possible, so it is conceivable that the yield will drop. The semiconductor device of the third invention of the present application having the aforementioned configuration can reduce detachment of the solder ball caused by breaking or cracking in order to be able to reduce the occurrence of fractures and cracks near the bonding part, wherein a Pb agglomerate is formed in the solder ball, and the dispersion density per unit cross-sectional area of the Pb agglomerate is 20×10^4 particles/mm³ or higher. Thereby, a semiconductor device can be obtained with favorable yield and that increases the reliability of the bonding part and increases the productivity of the semiconductor device.

[0015]

Furthermore, the semiconductor device of the fourth invention of the present application is the semiconductor device of the first invention of the present application or the second invention of the present application, wherein a Pb agglomerate is formed in the solder ball, and the average cross-sectional area of the Pb agglomerate is $10 \mu\text{m}^2$ or lower.

[0016]

Herein, if the average cross-sectional area of the Pb agglomerate is $10 \mu\text{m}^2$ or more, distortion will easily occur in the solder ball due to the Pb agglomerates, there is a possibility that breaking and cracking of the bonding part will occur in the temperature cycle testing or the like, and preventing detachment of the solder ball will not be possible, so it is conceivable that the yield will drop. However, with the semiconductor device of the fourth invention of the present application having the aforementioned configuration, wherein a Pb agglomerate is formed in the solder ball, and the average cross-sectional area of the Pb agglomerate is $10 \mu\text{m}^2$ or lower, and therefore the distortion occurring in the solder ball can be reduced, and therefore the occurrence of breaking and cracking can be reduced near the bonding part, and detachment of the solder ball caused by breaking or cracking can be reduced. Thereby, a semiconductor device can be obtained with favorable yield and that increases the reliability of the bonding part and increases the productivity of the semiconductor device.

[0017]

Furthermore, the semiconductor device of the fifth invention of the present application is the semiconductor device of the third invention of the present application or the fourth invention of the present application, wherein the solder ball and the printed board are bonded, and a bonded part between the solder ball and the wiring part is strengthened by the Cu-Sn alloy layer.

[0018]

Herein, if the bonding part between the solder ball and the wiring part is

not strengthened by the Cu-Sn alloy layer, there will be a possibility of breaking or cracking occurring to the bonding part during temperature cycle testing or the like, and preventing detachment of the solder ball will not be possible, so it is conceivable that the yield will drop.

However, the semiconductor device of the fifth invention of the present application having the aforementioned configuration has the solder ball and the print board bonded together, and can reduce detachment of the solder ball caused by breaking or cracking by reducing the occurrence of fractures and cracks near the bonding part between the wiring part and the solder ball that also bonds the print board, by strengthening the bonding part of the solder ball and the wiring part using a Cu-Sn alloy layer. Thereby, a semiconductor device can be obtained with favorable yield and that increases the reliability of the bonding part and increases the productivity of the semiconductor device.

[0019]

Furthermore, the sixth invention of the present application is a method of manufacturing a semiconductor device, including disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn on a land provided on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[0020]

Herein, the predetermined time refers to the time sufficient for increasing the strength of the bonding part between the solder ball and the wiring part. The method of manufacturing the semiconductor device the sixth invention of the present application with the aforementioned configuration can cause the Sn in the solder ball to liquid phase diffuse to the Cu in the wiring part and form a Cu-SN alloy layer with sufficient thickness to prevent detachment of the solder ball near the bonding part, and therefore can increase the strength of the bonding parts, and can reduce the occurrence rate of fractures and cracks near the bonding part by disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time. Thereby the occurrence of defects due to the occurrence of raking and cracking can be reduced so the productivity of the semiconductor device can be enhanced.

[0021]

Furthermore, the seventh invention of the present application is a method of manufacturing a semiconductor device, including: disposing a wiring part containing copper on a main surface of a film substrate, protecting the surface of the wiring part using resist, providing a hole that passes through the film substrate from the film substrate to the wiring part, and then filling the hole with metal, forming a gold layer on the metal surface of the opening part of the hole; bonding the semiconductor chip and the formed surface of the gold layer of the film substrate, disposing a solder ball containing Sn on a land provided on the wiring part, and then maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[0022]

Herein, the predetermined time refers to the time sufficient for

increasing the strength of the bonding part between the solder ball and the wiring part. The method of manufacturing the semiconductor device the seventh invention of the present application with the aforementioned configuration can cause the Sn in the solder ball to liquid phase diffuse to the Cu in the wiring part and form a Cu-Sn alloy layer with sufficient thickness to prevent detachment of the solder ball neared the bonding part, and therefore can increase the strength of the bonding parts, and can reduce the occurrence rate of fractures and cracks near the bonding part by disposing a solder ball containing Sn on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time. Thereby the occurrence of defects due to the occurrence of raking and cracking can be reduced so the productivity of the semiconductor device can be enhanced.

[0023]

Furthermore, the method of manufacturing the semiconductor device of the eighth invention of the present application is a method of manufacturing the semiconductor device of the sixth invention of the present application for the seventh invention of the present application, wherein a thin film of Au is formed on the surface of the land, and then a solder ball is disposed.

[0024]

The method of manufacturing the semiconductor device of the eighth embodiment of the present application having the aforementioned configuration can prevent oxidation of the wiring part by forming a thin film made of Au on the surface of the land and then providing the solder ball.

[0025]

Furthermore, the ninth invention of the present application is a semiconductor device, wherein a Cu-Sn alloy layer with a thickness of 3 μm or more is formed on the bonded part between the solder ball and the wiring part, obtained by disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[0026]

Herein, if the Cu-Sn alloy layer formed on the bonding part of the wiring part of the solder ball has a thickness that is less than approximately 1.87 μm , the bonding part between the solder ball and the wiring part cannot have sufficient strength, there will be a possibility of breaking or cracking occurring to the bonding part during temperature cycle testing or the like, and preventing detachment of the solder ball will not be possible, so it is conceivable that the yield will drop. However, the semiconductor device of the ninth invention of the present application having the aforementioned configuration can increase the strength of the bonded part and can reduce detachment of the solder ball caused by breaking or cracking by reducing the occurrence of fractures and cracks near the bonding part, wherein a Cu-Sn alloy layer with a thickness of approximately 3 μm or more is formed on the bonding part of the solder ball and the wiring part, and has a wiring part containing Cu connected to the semiconductor chip and a solder ball containing Sn bonded to the wiring part. Thereby, a semiconductor device can be obtained with favorable yield and that increases the reliability of the bonding part and increases the productivity of the semiconductor device.

[0027]

Furthermore, the 10th invention of the present application is a

semiconductor device, wherein the dispersion density per unit cross-sectional area of Pb agglomerates formed in the solder ball is 20×10^4 particles/ mm^3 or less, obtained by disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn and Pb on a land provided at a predetermined location on the wiring part; and maintaining an inert environment for a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[0028]

Herein, if the dispersion density per unit cross-sectional area of the Pb agglomerate that is formed is 20×10^4 particles/ mm^3 or less, distortion will easily occur in the solder ball due to the Pb agglomerates, there will be a possibility that breaking or cracking will occur in the bonding part during the temperature cycle testing or the like, and preventing detachment of the solder ball will not be possible, so it is conceivable that the yield will drop. However, the semiconductor device of the 10th invention of the present application having the aforementioned configuration can reduce distortion that occurs in the solder ball, and can reduce detachment of the solder ball caused by breaking or cracking in order to be able to reduce the occurrence of fractures and cracks near the bonding part, wherein the dispersion density per unit cross-sectional area of the Pb agglomerate is 20×10^4 particles/ mm^3 or higher. Thereby, a semiconductor device can be obtained with favorable yield and that increases the reliability of the bonding part and increases the productivity of the semiconductor device.

[0029]

Furthermore, the 11th invention of the present application is a semiconductor device, wherein the average cross-sectional area of Pb agglomerates formed in the solder ball is $10 \mu\text{m}^2$ or less, obtained by disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn and Pb on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[0030]

Herein, if the average cross-sectional area of the Pb agglomerate is $10 \mu\text{m}^2$ or more, distortion will easily occur in the solder ball due to the Pb agglomerates, there is a possibility that breaking and cracking of the bonding part will occur in the temperature cycle testing or the like, and preventing detachment of the solder ball will not be possible, so it is conceivable that the yield will drop. However, with the semiconductor device of the fourth invention of the present application having the aforementioned configuration, wherein the average cross-sectional area of the Pb agglomerate in the solder ball is $10 \mu\text{m}^2$ or lower, and therefore the distortion occurring in the solder ball can be reduced, and therefore the occurrence of breaking and cracking can be reduced near the bonding part, and detachment of the solder ball caused by breaking or cracking can be reduced. Thereby, a semiconductor device can be obtained with favorable yield and that increases the reliability of the bonding part and increases the productivity of the semiconductor device.

[0031]

The 12th invention of the present application is a semiconductor device,

wherein the solder ball and the printed board are bonded together, and the bonded part between the solder ball and the wiring part is strengthened by a Cu-Sn alloy layer, obtained by disposing a wiring part containing copper on a semiconductor chip via a film substrate, and then bonding the semiconductor chip and the film substrate; disposing a solder ball containing Sn and Pb on a land provided at a predetermined location on the wiring part; and maintaining an inert environment or a reducing environment at a temperature above the melting point of the solder ball for a predetermined period of time.

[0032]

Herein, if the bonding part between the solder ball and the wiring part is not strengthened by the Cu-Sn alloy layer, there will be a possibility of breaking or cracking occurring to the bonding part during temperature cycle testing or the like, and preventing detachment of the solder ball will not be possible, so it is conceivable that the yield will drop.

However, the semiconductor device of the 12th invention of the present application having the aforementioned configuration has the solder ball 11 and the printed board 34 bonded together, and can reduce detachment of the solder ball caused by breaking or cracking by reducing the occurrence of fractures and cracks near the bonding part between the wiring part 2 and the solder ball 11 that also bonds the print board, by strengthening the bonding part of the solder ball and the wiring part using a Cu-Sn alloy layer. Thereby, a semiconductor device can be obtained with favorable yield and that increases the reliability of the bonding part and increases the productivity of the semiconductor device.

[0033]

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The semiconductor device according to the embodiment of the present invention is described below while referring to the drawings, but the following embodiments are only an example of the semiconductor device of the present invention. FIG. 1 is a cross-sectional view showing the semiconductor device according to one embodiment of the present invention. In regards to the semiconductor device shown in FIG. 1, FIG. 2 is an enlarged cross-sectional view of a solder ball part 11 when using a solder ball made from an eutectic solder (Sn content ratio: 63%, Pb content ratio: 37%) as the solder ball 11. FIG. 3 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 4 is a figure showing one manufacturing process of the semiconductor device illustrated in FIG. 1. FIG. 5 is a figure showing measurement results of the shear strength for a bonding part between a wiring part 7 and the solder ball 11 after bonding a printed board and the solder ball according to a process illustrated in FIG. 4(i) after maintaining the device provided by the process illustrated in FIG. 3 and FIG. 4 (a) to (g) in an N₂ environment for a predetermined time at a temperature above the melting point of the solder ball according to a process illustrated in FIG. 4 (h) using the solder ball made from the Sn-Cu eutectic solder as the solder ball 11. FIG. 6 is a figure showing one example of the measurement method of the shear strength shown in FIG. 5.

[0034]

As illustrated in FIG. 1(a), the semiconductor device according to the present embodiment has the wiring part 2 containing Cu that is connected to a semiconductor chip 1 and the solder ball 11 containing Sn that is connected to the wiring part 2.

In other words, the semiconductor device according to the present embodiment has the wiring part 4 containing Cu that is connected to the semiconductor chip 1, the solder ball 11 containing Sn connected to a main surface of the wiring part 4, and a film substrate 3 that is connected to the wiring part 2 that is the opposite side surface of the bonding surface between the wiring part 2 and the solder ball 11, is provided with a hole 4 that passes through the film substrate 3 from the wiring part 2 to the opposite side surface of the bonding part between the film substrate 3 and the wiring part 2, a metal 5 is filled in the hole 4, and an Au layer 6 is formed on a surface of the metal 5 of an opening part of the hole 4.

Note, the hole 4 is placed directly above an electrode part 12 that is placed on the semiconductor chip 1 on the semiconductor device according to the present embodiment, and the solder ball 11 and the electrode part 12 are connected by the metal 5 filled in the hole 4, but the solder ball 11 does not have to be placed directly above the electrode part 12. Furthermore, as illustrated in FIG. 1(c), the solder ball 11 and the printed board 34 are connected in the semiconductor device according to the present embodiment illustrated in FIG. 1(a).

[0035]

Furthermore, Sn is a main component in the solder ball, and the solder ball is formed, for example, using Pb free solder or the like containing Ag, Cu, An, Bi, Ni, Cd, S, As, Zn, and the like with Sn-Pb alloy, Sn-Ag alloy, or Sn as a main constituent. Furthermore, in regards to FIG. 1(a), a figure in which the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 vicinity is illustrated enlarged in FIG. 1(b). As illustrated in FIG. 1(b), a strong Cu-Sn alloy layer is formed on the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 portion on which the solder ball 11 is placed on the wiring part 2. As described above, detachment of the solder ball 11 caused by fractures and cracks can be reduced by reducing the occurrence of fractures and cracks near the bonding part by providing the Cu-Sn alloy layer on the bonding part between the solder ball 11 and the wiring part 2. As a result, productivity of the semiconductor device can be improved, and yield can be further increased. The Cu-Sn alloy layer preferably has a thickness of 1.87 μ m or more, more preferably a thickness of 2 μ m or more, and even more preferably a thickness of 3 μ m or more, in order to reduce the occurrence of fractures and cracks in the vicinity of the bonding part.

[0036]

Furthermore, when the solder ball 11 contains a material other than Sn, the material is frequently present in the form of agglomerates. If the agglomerates are large, distortion in the solder ball 11 will easily occur, and fractures and cracks will readily occur, so the material is preferably dispersed into smaller agglomerates.

For example, when the solder ball 11 contains Pb in addition to Sn, agglomerates made from Pb will form in the solder ball 11 and dispersing the agglomerates into smaller agglomerates is preferable.

[0037]

Next, a manufacturing process of the semiconductor device illustrated in FIG. 1 is described while referring to FIG. 3 and FIG. 4. First, one

manufacturing process in which the wiring part 2 is placed on the film substrate 3 is described while referring to FIG. 3. As illustrated in FIG. 3(a), the wiring part 2 containing Cu is placed on one main surface of the film substrate. Furthermore, an adhesive is applied on the opposite side surface of the wiring part 2 of the film substrate 3. A material such as polyimide or the like that can withstand temperatures of 250°C or higher is used as the film substrate 3 and a polyimide is used for the adhesive agent 31. Next, the wiring part 2 on the film substrate 3 illustrated in FIG. 3(a) is patterned with a predetermined shape (refer to FIG. 3(b)), and a resist 32 is applied to a surface that is exposed on the outer part of the film substrate and the wiring part 2 (refer to FIG. 3(c)). The hole 4 that passes through the film substrate 3 is formed from the adhesive 31 to the wiring part 2. A tool such as a laser or the like is used to form the hole 4. A metal 5 such as Cu or Al is filled in the hole 4 (refer to FIG. 3(e)), and the Au layer 6 is formed on the surface of the metal 5 at the opening part of the hole 4 (refer to FIG. 3(f)). A tape substrate 33 having the film substrate 3 on which the wiring part 2 is formed on one main surface is provided by the aforementioned process. Note, FIG. 3 illustrates one enlarged land 7 provided on the film substrate 3, and a plurality of lands 7 for placing the solder ball 101 are provided on the film substrate 3 in a later process.

[0038]

Next, one manufacturing process for providing the solder ball 11 using the tape substrate 33 provided by the process illustrated in FIG. 3 is described while referring to FIG. 4. The tape substrate 33 provided by the process illustrated in FIG. 3 is provided on the surface where the Au layer 6 was provided (refer to FIG. 4(a)), and a stiffener 41 made from Cu, stainless steel, or the like is attached to both ends of the tape substrate 33 (refer to FIG. 4(b)). The semiconductor chip 1 is provided between the 2 stiffeners 41, and the Au layer 6 and the electrode part made from Al or the like placed on the semiconductor chip 1 are bonded (refer to FIG. 4(c)). The connection is performed by combining heat and ultrasound using a bonding tool. Next, as needed, reinforcement of the bonding part between the tape substrate 33 and the semiconductor chip 1 is performed (refer to FIG. 4(d)) by injecting reinforcement resin 42 between the tape substrate 33 and the semiconductor chip 1 in order to cure. Liquid resin such as epoxy resin or the like is used as the reinforcement resin 42. In regards to the semiconductor chip 1, a lid part 43 made from Cu, Al, Si, C, or the like is placed on a surface that is on the opposite side of the surface connected to the tape substrate 33, and sealing is performed under normal pressure (refer to FIG. 4(e)). When this occurs, a conductive adhesive 44 such as Ag paste, Cu paste, or the like is applied on the surface of the lid part 43 connected to the semiconductor chip 1, and sealing under normal pressure is performed using a belt furnace or an oven while heat curing the related conductive adhesive 44 by sealing. The land 7 (not illustrated in the figures) for placing the solder ball 11 is provided by forming a groove by performing etching or the like on a predetermined location of the resist 32 placed on the film substrate 3 of the tape substrate 33, the solder ball 11 is attached (refer to FIG. 4(f)) to

each land 7 which are on the wiring part 2 placed on the tape substrate 33 while performing decompression suctioning, a flux (not illustrated in the figures) is applied to the surrounding of the bonding part between the solder ball 11 and the land 7, and the land 7 and the solder ball 11 are connected by reflowing the solder ball 11. Next, if necessary, the flux used in the aforementioned process is washed off. The device provided by the aforementioned processes (refer to FIG. 4(g)) is maintained for a predetermined time at a temperature that is above the melting point of the solder ball 11 that is in an inert environment or a reducing environment (refer to FIG. 4(h)). Sorting, inspection, and the like are performed on the device provided by the process above after performing temperature cycle testing in order to determine operating characteristics and durability towards physical damage and the like, the device is mounted to the printed board 34 by bonding the printed board 34 and the solder ball 11 by reflowing the solder ball 11 (refer to FIG. 4(i)) in order to provide the semiconductor device which is the final product. As described above, Sn in the solder ball 11 and Cu in the land 7 are alloyed and Cu-Sn alloy is formed in the vicinity of the bonding part between the solder ball 11 and the land 7 by maintaining the device illustrated in FIG. 4(g) at a temperature that is above the melting point of the solder ball 11 in an inert environment or a reducing environment for a predetermined amount of time. Herein, inert environment refers to a gas that does not react with the solder ball 11 and the land part 7, such as, N₂, Ar, He, Ne, and the like, or a mixture of these, and a reducing environment refers to gas that has reducibility, such as CO, H₂, or the like. As described above, the occurrence rate of fractures and cracks in the vicinity of the bonding part between the solder ball 11 that is also connected to the printed board 34 and the wiring part 2 can be reduced since the solder ball 11 can improve strength of the bonding part between the solder ball 11 and the wiring part 2 in the process illustrated in FIG. 4(i) since Sn in the solder ball 11 is liquid phase diffused into a Cu matrix of the wiring part 2 and a Cu-Sn alloy layer that has a thickness sufficient to prevent detachment of the solder ball 11 in the vicinity of the bonding part by maintaining the device for a predetermined period of time at a temperature that is above the melting point of the solder ball 11 in an inert environment or a reducing environment. Thereby, productivity of the semiconductor device can be improved since the occurrence of defective parts due to the occurrence of fractures and cracks can be reduced.

[0039]

Note, FIG. 3(f) illustrates a case in which the solder ball 11 was provided on the land 7 without forming a thin film made from Au on the land 7 in the present embodiment. Similar to the manufacturing process of the conventional semiconductor device illustrated in FIG. 9, the solder ball 11 can be provided on the land 7 after forming the thin film made from Au on the land 7 even in the present embodiment since oxidation of the wiring part 2 can be prevented while promoting

alloying by placing the solder ball on the land 7 after forming the thin film made from Au on the land 7. Thereby, oxidation of the wiring part 2 can be prevented.

[0040]

[Example 1]

The semiconductor device of the present embodiment illustrated in FIG. 1 is an example using a solder ball made from Sn-Pb eutectic solder (Sn content ratio: 63%, Pb content ratio: 37%) as the solder ball 11. FIG. 2 illustrates an enlarged view of the solder ball 11 portion according to the present example. As shown in FIG. 2, a Cu-Sn alloy layer was formed in the vicinity of the bonding part between the solder ball 11 and the wiring part 2. In regards to the solder ball 11 provided on the semiconductor device of the present invention illustrated in FIG. 2, 1.87 to 4.0 μm of the Cu-Sn alloy layer was formed on each solder ball 11, and in particular, many solder balls were formed with 3.0 to 4.0 μm of the Cu-Sn alloy layer. On the other hand, 1.00 to 1.50 μm of the Cu-Sn alloy layer was formed on the solder ball 101 placed on the conventional semiconductor device illustrated in FIG. 8. Thereby, it was revealed that the semiconductor device of the present invention illustrated in FIG. 2 was formed with a strong Cu-Sn alloy layer that was thicker. Forming the Cu-Sn alloy layer with a thickness of at least 1.87 μm or more was preferable in order to prevent detachment of the solder ball 11. Thereby, the occurrence ratio of fractures and cracks in the vicinity of the bonding part could be reduced since strength of the bonding part between the solder ball 11 and the wiring part 2 was strengthened by forming the Cu-Sn alloy layer with sufficient thickness in the vicinity of the bonding part. Thereby, a device with favorable yield could be provided since the occurrence of defective parts caused by the occurrence of fractures and cracks could be reduced.

[0041]

As mentioned above, when the solder ball 11 contains material other than Sn, generally, the material is an agglomerate, and the Pb contained in the raw material of the solder ball 11 are agglomerates in the solder ball 11 illustrated in FIG. 2. The agglomerate formed from Pb will be referred to agglomerate below simply as a Pb agglomerate. Dispersing the Pb agglomerate to form smaller agglomerates is preferable since a larger Pb agglomerate means that distortion can more easily occur in the solder ball 11, and fractures or cracks can also occur. In the solder ball 11 illustrated in FIG. 2, the dispersion density per unit cross sectional area of the Pb agglomerate was $20 \times 10^4/\text{mm}^3$ or higher. On the other hand, the dispersion density per unit cross sectional area of the Pb agglomerate formed in the solder ball 101 provided on the conventional semiconductor device illustrated in FIG. 8 was $15 \times 10^4/\text{mm}^3$. In comparison, with the solder ball 101 provided on a conventional semiconductor device, the solder ball 11 provided on the semiconductor device of the present invention had Pb agglomerates that were more dispersed. Furthermore, in the solder ball 11 illustrated in FIG. 2, the cross sectional area of the Pb agglomerate was 1 to 10 μm^2 . On the other hand, the cross sectional area of the Pb agglomerate formed in the solder ball 101 provided on the conventional semiconductor device illustrated in FIG. 8 was 10 to 30 μm^2 . In comparison to the solder ball

101 provided on a conventional semiconductor device, the solder ball 11 provided on the semiconductor device of the present invention had Pb agglomerates that were more minute. Thereby, the semiconductor device of the present invention illustrated in FIG. 2 can reduce the occurrence of fractures and cracks in the bonding part between the solder ball 11 and the wiring part 2 as well as the occurrence of distortions in the solder ball 11 since Pb agglomerates in the solder ball 11 provided on the semiconductor device were more minute and formed by dispersing. Thereby, a device with favorable yield can be provided since the occurrence of defective parts caused by the occurrence of fractures and cracks could be reduced.

[0042]

[Example 2]

Similar to example 1, the device provided by the process illustrated in FIG. 3 and Fig. 4 (a) to (g) was maintained for a predetermined amount of time at a temperature above the melting point of the solder ball 11 in an N_2 environment using N_2 as the inert gas of FIG. 4(h) using the solder ball made from Sn-Cu eutectic solder as the solder ball 11, and the results of measuring the shear strength for the bonding part between the solder ball 11 and the wiring part 7 after bonding the printed board 34 and the solder ball 11 is illustrated in FIG. 4 (i). The relationship between the shear strength and the maintenance time for the bonding part is shown in FIG. 5. In FIG. 5, the horizontal axis is the time period the device was maintained in the N_2 environment (maintained time, units: time), the vertical axis is the shear strength (unit: gf), \circ is the shear strength for each time period when maintained at 240°C which is above the melting point of the solder ball 11 (melting point of the Sn-Cu eutectic solder is 183°C), and for comparison, \bullet is the shear strength for each time period when maintained at 150°C which is below the melting point of the solder ball 11. Furthermore, as shown in FIG. 6, the shear strength is the strength measured when the solder ball 11 was sheared using the measuring tool 61 in an approximately horizontal direction (arrow A direction) with the bonding surface between the solder ball 11 and the wiring part 2 for the bonding part between the solder ball 11 and the wiring part 2. The semiconductor device according to the present example was provided such that the diameter of the solder ball 11 was 0.5 mm, the pitch of the loaded solder ball 11 (distance between the center and adjacent solder ball 11) was 0.8 mm, and the diameter of the land 7 (bonding part between the solder ball 11 and the wiring part 2) was 0.4 mm. As shown in FIG. 5, in comparison to when the device was maintained below the melting point of the solder ball 11, the shear strength for the bonding part between the solder ball 11 and the wiring part 2 was improved more when the device was maintained above the melting point of the solder ball 11. The Sn in the solder ball 11 liquid phase diffused to the Cu of the wiring part by maintaining the device above the melting point of the solder ball 11, it was speculated that this was to form the Cu-Sn alloy layer in the

vicinity of the bonding part, and thereby, improve the strength of the bonding part between the solder ball 11 and the wiring part 2. In particular, when the device was maintained above the melting point of the solder ball 11, the shear strength was improved to 680 gf or higher by maintaining at 1 hour or more, and a strength sufficient to prevent detachment of the solder ball 11 in the vicinity of the bonding part between the solder ball 11 and the wiring part 2 could be provided for the device made by bonding the solder ball 11 and the printed board 34. [0043]

[Table 1]

Element or Alloy	Coefficient of thermal expansion (ppm)	Density (g/cm ³)
Cu	16.8	8.93
Pb	29	11.34
Sn	21	7.28
Cu-Sn alloy	17.1 to 17.8	---

Smaller Pb agglomerates are preferable in order to reduce distortion that occurs in the solder ball 11 due to the occurrence of deformations in the solder ball 11 and the occurrence of fractures and cracks occurring more frequently in the solder ball 11 as the size of the Pb agglomerate increases. On the other hand, as illustrated in FIG. 1, the coefficient of thermal expansion for Pb is larger than the coefficient of thermal expansion for Cu, Cu-Sn alloy, and Sn, and the density for Pb is larger than the density of Sn. Therefore, when temperature cycling testing or the like (heat processes at a temperature below the melting point of the solder ball 11) were performed on the provided semiconductor device, it was thought that many distortions occurred at the portion of the Pb agglomerate since the coefficient of the thermal expansion for Pb was larger than the other ingredients and the Pb agglomerate expanded more than the other portions of the solder ball 11. In other words, a larger Pb agglomerate contained in the solder ball 11 is more likely to cause larger distortions in the solder ball 11, and the more likely that fractures and cracks would occur in the solder ball. However, as illustrated in FIG. 2, the crystal structure of the element contained in the solder ball 11 changed by performing the heat process at a temperature above the melting point of the solder ball 11 in the present example, and the agglomerates formed from Pb (Pb agglomerates) were more minute and were formed by dispersing in comparison to the conventional semiconductor device (refer to FIG. 8) provided without performing the heat treatment processes. In this manner, distortion caused by the portion of the Pb agglomerates could be made smaller since the Pb agglomerates contained in the solder ball 11 were formed by miniaturization, and distortions caused from the portion of the Pb agglomerates could be dispersed since the Pb agglomerates were formed by dispersing in the semiconductor device according to the present example provided without performing the corresponding heat treatment processes. Thereby, the bonding strength for the bonding part between the solder ball 11 and the wiring part 2 could be increased. [0044]

Note, the material for the solder ball 11 in the present example was Sn-Pb eutectic solder, but the material for the solder ball 11 is not restricted to this, and can be any material as long as the material contains Sn, and can, for example, have Sn-Ag alloy or Sn as a main component, and Pb free solders or the like containing Ag, Cu, Zn, Cd, Ni, S, As, or Bi can be used.

Furthermore, the solder ball 11 contained Pb since the solder ball 11 used in the present example was formed from eutectic solder, and the solder ball 11 had a component distribution as shown in FIG. 2. As illustrated in FIG. 2, the Pb existed as agglomerates in the solder ball 11 (referred to below simply as Pb agglomerates). The coefficient of thermal expansion (units: ppm) and density (units: g/cm³) of the main component (Cu, Pb, Sn, Cu-Sn alloy) contained in the solder ball 11 are shown in table 1.

[Brief Description of the Drawings]

FIG. 1 is a cross sectional view illustrating the semiconductor device according to one embodiment of the present invention.

FIG. 2 is an enlarged cross sectional view of the solder ball portion when using a solder ball made from Sn-Pb eutectic solder (Sn content ratio: 63%, Pb content ratio: 37%) as the solder ball for the semiconductor device illustrated in FIG. 1.

FIG. 3 is a figure illustrating one manufacturing process of the semiconductor device shown in FIG. 1.

FIG. 4 is a figure illustrating one manufacturing process of the semiconductor device illustrated in FIG. 1.

FIG. 5 is a figure showing results of the shear strength for the bonding part between the solder ball and the wiring part measured after bonding the printed board and the solder ball after maintaining the device provided by the processes illustrated in FIG. 3 and FIG. 4 (a) to (g) in an N₂ environment for a predetermined time at a temperature above the melting point of the solder ball in FIG. 4 (h).

FIG. 6 is a figure illustrating one example of the measurement method of the shear strength shown in FIG. 5.

FIG. 7 is a figure illustrating a conventional semiconductor device.

FIG. 8 is an enlarged cross sectional view (schematic diagram) of the solder ball portion when using the solder ball made from Sn-Pb eutectic solder (Sn content ratio: 63%, Pb content ratio: 37%) as the solder ball for the conventional semiconductor device illustrated in FIG. 7.

FIG. 9 is a figure showing one manufacturing process of the conventional semiconductor device.

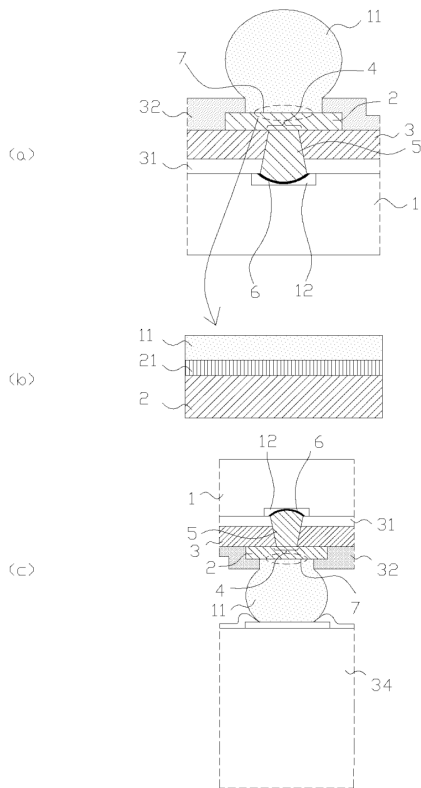
FIG. 10 is a figure showing one manufacturing process of the conventional semiconductor device.

[Description of the Symbols]

- 1 Semiconductor chip
- 2 Wiring part

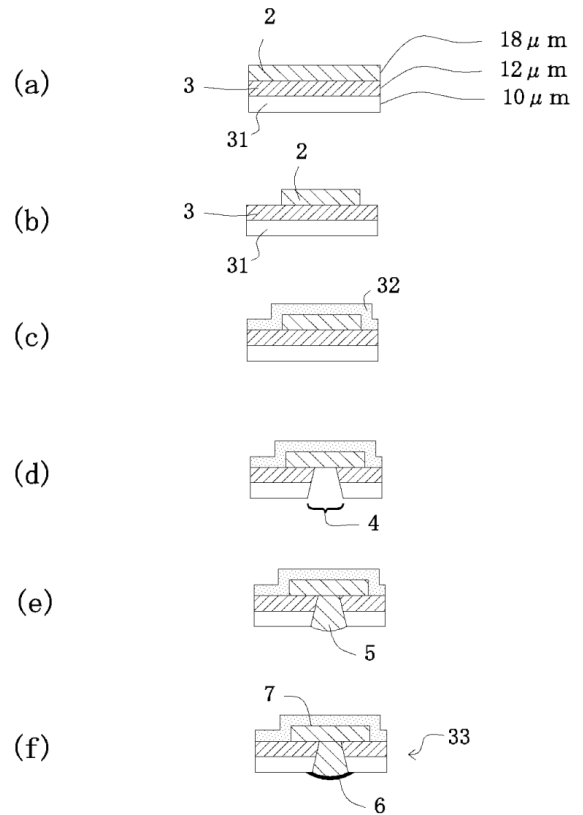
3 Film substrate
 4 Hole
 5 Metal
 6 Au layer
 7 Land
 8 Au layer
 11 Solder ball
 12 Electrode part
 21 Cu-Sn alloy layer
 22 Sn
 23 Pn agglomerate [Translator's note: probably Pb agglomerate]
 31 Adhesive agent
 32 Resist
 33 Tape substrate

[FIG. 1]

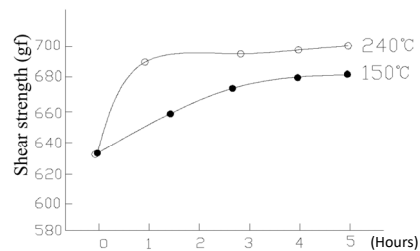


34 Printed board
 41 Stiffener
 42 Reinforced resin
 43 Lid part
 44 Conductive adhesive agent
 45 Position determining tool
 46 Epoxy resin or silicon resin
 61 Measuring tool
 81 Cu-Sn alloy layer
 82 Sn
 83 Pn agglomerate [Translator's note: probably Pb agglomerate]
 93 Tape substrate
 101 Solder ball

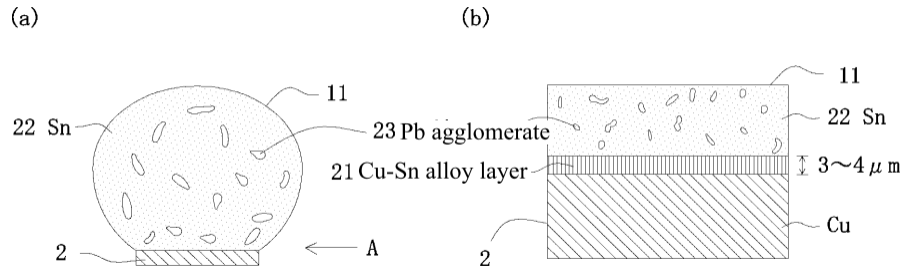
[FIG. 3]



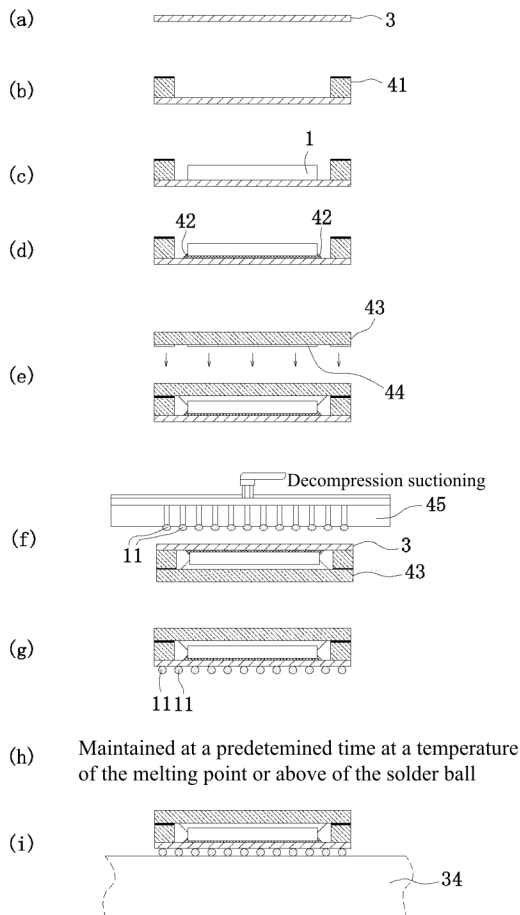
[FIG. 5]



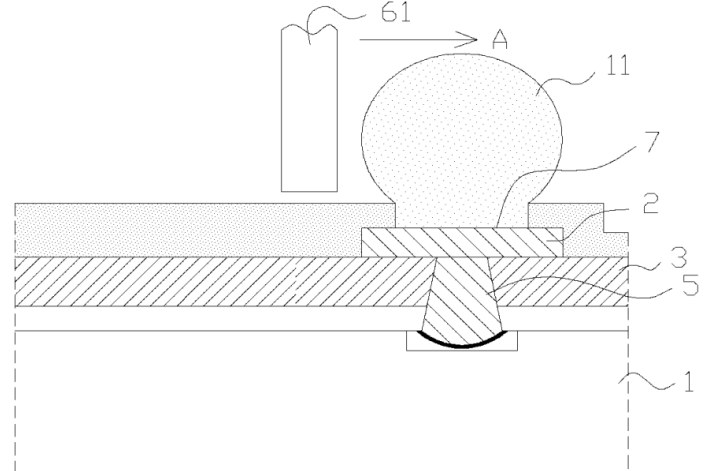
[FIG. 2]



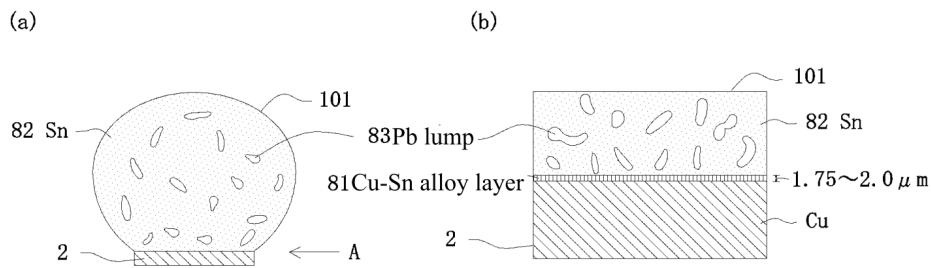
[FIG. 4]



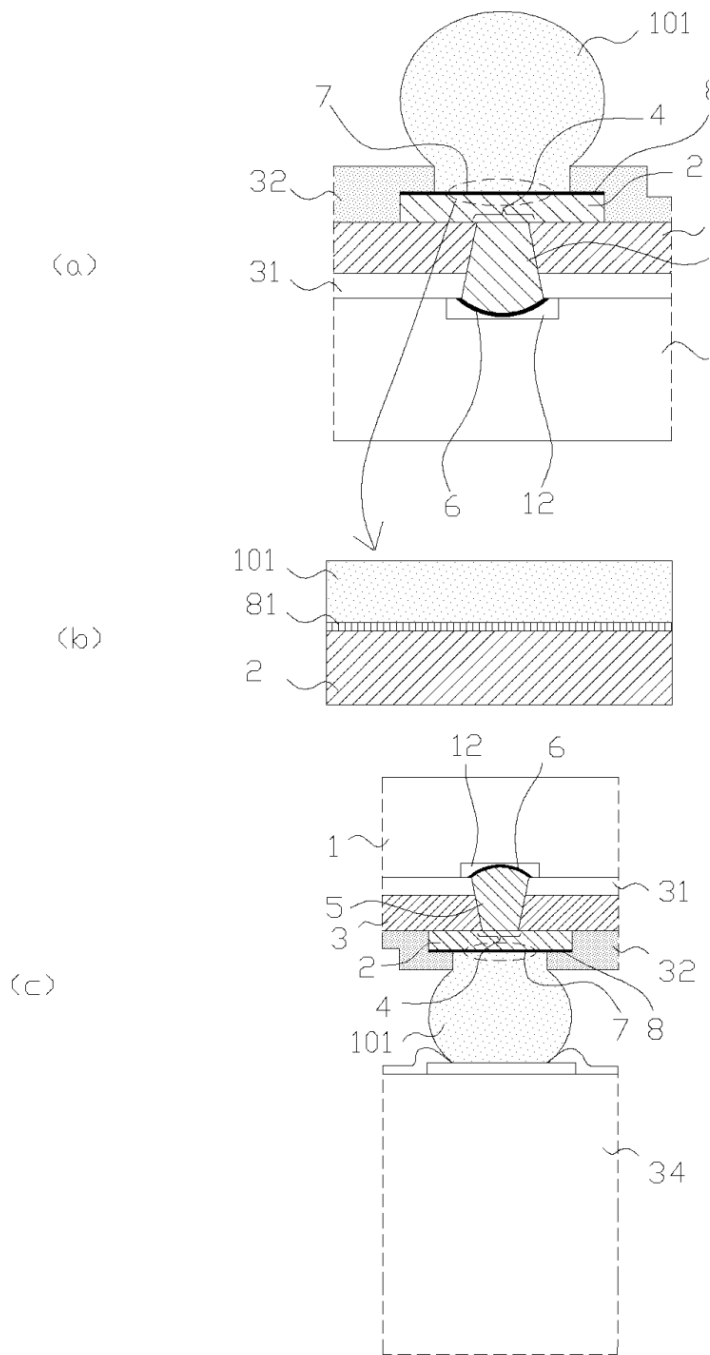
[FIG. 6]



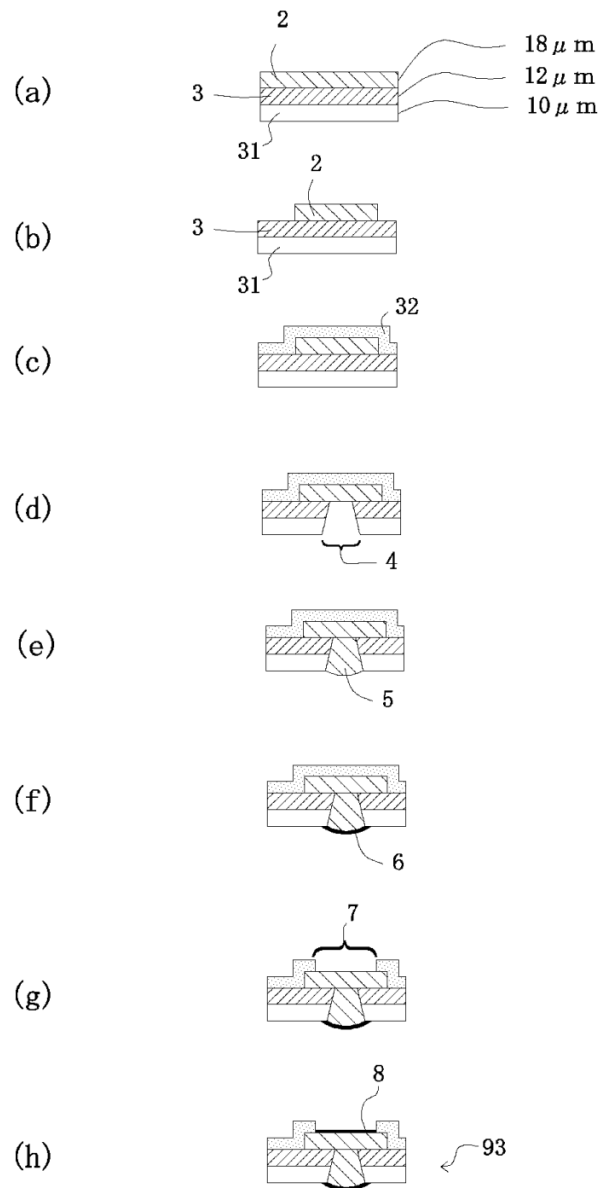
[FIG. 8]



[FIG. 7]



[FIG. 9]



[FIG. 10]

