

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA, INC.,
AND SAMSUNG SEMICONDUCTOR, INC.,¹
Petitioner,

v.

TESSERA ADVANCED TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2018-00798
Patent 6,954,001 B2

Before BARBARA A. PARVIS, ROBERT J. WEINSCHENK, and
SCOTT B. HOWARD, *Administrative Patent Judges*.

HOWARD, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

¹ The Notice of Filing Date Accorded inadvertently omitted “Samsung” from “Samsung Semiconductor, Inc.” in the caption. *See* Paper 5, 1. The parties are encouraged to use the heading on the first page of this Decision, and not the first page of the Notice of Filing Date Accorded (Paper 5), for all future filings in the proceeding.

I. INTRODUCTION

Samsung Electronics Co., Ltd, Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (collectively “Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–18 of U.S. Patent No. 6,954,001 B2 (Ex. 1001, “the ’001 patent”) pursuant to 35 U.S.C. §§ 311–319. Paper 1 (“Pet.”). Tessera Advanced Technologies, Inc. (“Patent Owner”) did not file a Patent Owner Preliminary Response.

We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). *Inter partes* review may be not instituted unless “the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). On April 24, 2018, the Supreme Court held that a decision to institute under 35 U.S.C. § 314 may not institute on less than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018). For the reasons set forth below, upon considering the Petition and evidence of record, we determine that the information presented in the Petition establishes a reasonable likelihood that Petitioner will prevail with respect to at least one of the challenged claims. Accordingly, we institute *inter partes* review on all of the challenged claims based on the all of the grounds identified in the Petition.

Our findings of fact and conclusions of law discussed below are based on the evidentiary record developed thus far and made for the sole purpose of determining whether the Petition meets the threshold for initiating review. This decision to institute trial is not a final decision as to the patentability of

any challenged claim or the construction of any claim limitation. Any final decision will be based on the full record developed during trial.

A. Real Party-In-Interest

Petitioner identifies itself—Samsung Electronics Co., Ltd, Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.—as the real parties-in-interest. Pet. 2.

B. Related Proceedings

The parties identify the following current patent litigation proceedings in which the '001 patent is asserted: (1) the Matter of *Certain Wafer-Level Packaging Semiconductor Devices And Products Containing Same (Including Cellular Phones, Tablets, Laptops, And Notebooks) And Components Thereof*, Inv. No. 337-TA-1080 (USITC); and (2) *Tessera Advanced Techs., Inc. v. Samsung Elecs. Am., Inc.*, Civ. No. 2:17-cv-07621 (D.N.J.). *Id.* at 2–3; Paper 7, 2. In addition, Petitioner identifies the following completed patent litigation proceeding in which the '001 patent was asserted: *Tessera, Inc. v. Broadcom Corp.*, Div. No. 1:16-cv-00380 (D. Del.). Pet. 2–3.

Additionally, the parties identify two pending *inter partes* review proceedings: (1) *Samsung Elecs. Co. v. Tessera Advanced Techs., Inc.*, Case IPR2018-00799 (involving the '001 patent); and (2) *Samsung Elecs. Co. v. Tessera Advanced Techs., Inc.*, Case IPR2018-00466 (involving a related patent, U.S. Patent No. 6,784,557). Pet. 3; Paper 7, 2. Petitioner also identifies *Broadcom Corp. v. Tessera Advanced Techs., Inc.*, Case IPR2017-01486, which was terminated pursuant to a settlement agreement after trial was instituted. *See* Pet. 3; *see also* *Broadcom Corp. v. Tessera Advanced*

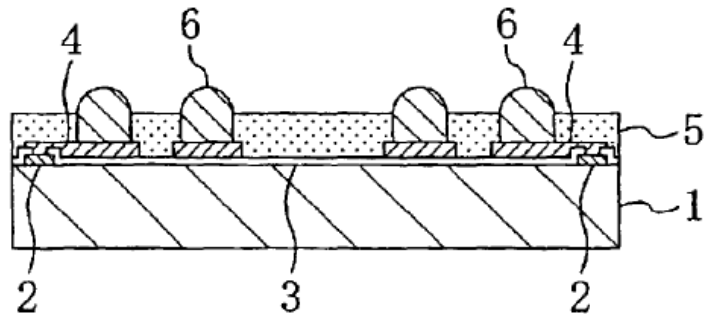
Techs., Inc., Case IPR2017-01486, slip op. at 2 (PTAB Jan. 2, 2018) (Paper 13).

C. The '001 Patent

The '001 patent, titled “Semiconductor Device Including a Diffusion Layer,” states that an object of the invention is to provide a semiconductor device “having improved junction reliability between the metal wiring and a ball electrode mounted on an external electrode portion of the metal wiring.” Ex. 1001, [54], 2:35–41.

Figure 15, reproduced below, illustrates a cross section of a conventional semiconductor device.

FIG. 15B
Prior Art



As shown in Figure 15 above and as described in the '001 patent, in a conventional semiconductor device, “the wiring electrodes of the substrate on which the semiconductor device is mounted are respectively connected to metal wirings 4 of [copper (Cu)] formed on the surface of semiconductor element 1 through ball electrodes 6 formed from the solder.” *Id.* at 2:4–9. According to the '001 patent, “tin (Sn) contained in solder of the ball electrode 6 diffuses into [copper (Cu)] of the metal wiring 4 to form a Sn–Cu alloy layer.” *Id.* at 2:15–18. The '001 patent states that, “[a]s a result, in the portion of the metal wiring 4 on which the ball electrode 6 is mounted (i.e., the external electrode portion) and the portion near the external

electrode portion, the Sn–Cu alloy grows in the most part of the metal wiring.” *Id.* at 2:18–22. The ’001 patent states that “[t]he Sn–Cu alloy is weak and hard” and “is likely to be broken by the stresses” generated due to differences in the thermal expansion coefficients of the semiconductor element, the resin film (if included), and the substrate. *Id.* at 2:1–3, 2:22–31.

Figure 2 of the ’001 patent is reproduced below.

FIG. 2

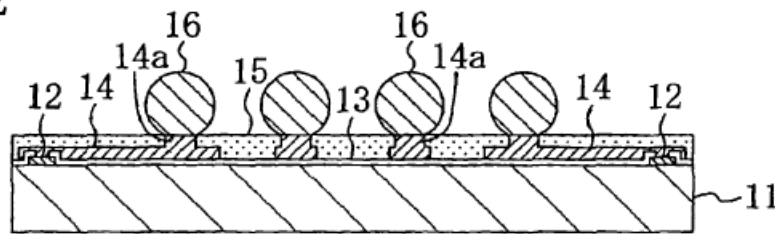


Figure 2 illustrates a cross-sectional view of “the semiconductor device of the first embodiment.” *Id.* at 8:11–12. As illustrated in Figure 2 above, electrodes 12 are formed on the surface of semiconductor element 11. *Id.* at 8:10–11. A passivation film 13, also formed over the surface of semiconductor element 11, has an opening on each electrode 12. *Id.* at 8:13–17. According to the ’001 patent, metal wirings 14 containing copper are formed on passivation film 13, and “[e]ach metal wiring 14 is electrically connected to a corresponding one of the electrodes 12.” *Id.* at 8:18–21. The ’001 patent discloses that insulating film 15 is formed on metal wirings 14 and passivation film 13 and “has openings in order to expose a portion of each metal wiring 14 which functions as an external electrode (hereinafter, referred to as ‘external electrode portion 14a’).” *Id.* at 8:21–26. According to the ’001 patent, “ball electrodes 16, which are formed from solder, are connected in a molten state to the openings of the insulating film 15, that is,

the external electrode portions 14a of the metal wirings 14, respectively.”
Id. at 8:27–35.

The '001 patent states that “[t]he present embodiment is characterized in that the thickness (e.g., 14 μm) of the external electrode portion 14a of the metal wiring 14 is greater than that of the other portion of the metal wiring 14 (hereinafter, referred to as ‘non-electrode portion’).” *Id.* at 8:39–43. The '001 patent further states:

When the metal wirings 14 contain, e.g., Cu (which is a commonly used metal wiring material), Sn contained in solder of the ball electrode 16 diffuses into Cu contained in the metal wiring 14, whereby a Sn–Cu alloy layer having low strength grows in the thickness direction of the external electrode portion 14a. However, since the thickness of the external electrode portion 14a of the metal wiring 14 is greater than that of the non-electrode portion of the metal wiring 14, this Sn–Cu alloy layer can be prevented from growing through the entire thickness of the external electrode portion 14a.

Id. at 8:63–9:6. According to the '001 patent, “[s]ince a part of the external electrode portion 14a is left unchanged into the Sn–Cu alloy layer, the strength of the metal wiring 14 can be maintained even if Cu is used as a metal wiring material.” *Id.* at 9:9–12. The '001 patent adds that even if stresses due to a difference in thermal expansion coefficients are generated, “the . . . structure of the first embodiment can prevent the Sn–Cu alloy layer having low strength from being broken and thus can prevent disconnection of the metal wirings 14.” *Id.* at 9:20–24.

The '001 patent further states that “[i]n the first embodiment, the thickness of the external electrode portion 14a of the metal wiring 14 (e.g., the total thickness of the non-electrode portion of the metal wiring 14 and the metal-material embedded portion) is preferably in the range of 10 μm to

20 μm .” *Id.* at 9:36–40. The patent also states that “in the first embodiment, the thickness of the non-electrode portion of the metal wiring 14 is preferably in the range of 0.01 μm to 8 μm , and more preferably in the range of 0.01 μm to 4 μm .” *Id.* at 9:25–28.

D. The Challenged Claims

Petitioner challenges claims 1–18 of the ’001 patent. Pet. 4. Claims 1 and 10 are independent claims. Claims 1 and 10 are illustrative of the subject matter of the challenged claims and read as follows:

1. A semiconductor device, comprising:

a semiconductor element;

a first electrode portion formed on the semiconductor element,
said first electrode portion comprising a first metal
component;

a second electrode portion formed on the semiconductor
element and electrically connected to said first electrode
portion, said second electrode portion comprising a
second metal component different from said first metal
component; and

a diffusion layer formed between said first electrode portion
and said second electrode portion,

wherein said diffusion layer comprises said first metal
component and said second metal component. . . .

10. A semiconductor device comprising:

a semiconductor element;

a first electrode portion formed on the semiconductor element,
said first electrode portion comprising a first metal
component;

a second electrode portion formed on the semiconductor
element and electrically connected to said first electrode
portion, said second electrode portion comprising a

second metal component different from said first metal component; and

a diffusion layer formed between said first electrode portion and said second electrode portion,

wherein said diffusion layer comprises said first metal component and said second metal component, and

said first electrode portion and said diffusion layer have a combined thickness in the range of 10 μm to 20 μm .

Id. at 26:15–28, 26:61–27:9, Certificate of Correction (correcting claim 10).

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

References	Basis ²	Challenged Claim(s)
Furuya ³ and Takizawa ⁴	§ 103(a)	1–4, 6–8, 10–13, and 15–17
Furuya, Takizawa, and Yaguchi ⁵	§ 103(a)	5 and 14
Furuya, Takizawa, and Nozawa ⁶	§ 103(a)	9 and 18

² The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. § 100 *et seq.* effective on March 16, 2013. Because the ’001 patent issued from an application filed before March 16, 2013, we apply the pre-AIA versions of the statutory bases for unpatentability.

³ Furuya et al., JP 2001-53184-A (published Feb. 23, 2001) (“Ex. 1005”). Petitioner provides the English language translation of Furuya which is being referenced. Ex. 1006. All references to foreign language documents in this Decision are made to the corresponding English translation.

⁴ Takizawa et al., JP 2000-260894 A (published Sept. 22, 2000) (“Ex. 1014”). Petitioner provides the English language translation of Takizawa which is being referenced. Ex. 1015.

⁵ Yaguchi, et al., WO 00/55910, (published Sept. 21, 2000) (“Ex. 1010”). Petitioner provides the English language translation of Yaguchi which is being referenced. Ex. 1011.

⁶ US 6,181,010 B1 (issued Jan. 30, 2001) (“Ex. 1012”).

Pet. 5. In its analysis, Petitioner relies on the declaration testimony of Miltiadis K. Hatalis, Ph.D (“Ex. 1002”).

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see also Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable construction standard).

“Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history.” *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016). In addition, the Board may not “construe claims during [an *inter partes* review] so broadly that its constructions are unreasonable under general claim construction principles.” *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) (emphasis omitted). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner contends, for purposes of this proceeding, that no terms need to be construed. Pet. 18.

Having considered the evidence presented, we conclude that no express claim construction is necessary for our determination of whether to institute review of the challenged claims. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need

be construed that are in controversy, and only to the extent necessary to resolve the controversy.”).

B. Legal Principles of Obviousness

An invention is not patentable as obvious “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and, (4) where in evidence, objective evidence of nonobviousness such as commercial success, long-felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). When evaluating a combination of teachings, we also must “determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441, F.3d 977, 988 (Fed. Cir. 2006)). We analyze the ground based on obviousness in accordance with the above-stated principles.

C. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citing *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955,

962 (Fed. Cir. 1986)). In a given case, “one or more factors may predominate.” *Id.*

Petitioner asserts that a person having ordinary skill in the art at the time of the invention

would have had (i) a bachelor-level degree in mechanical engineering, materials science, electrical engineering, or a related field and 3–5 years of experience in the design/development of semiconductor packages; (ii) a Master’s-level degree in mechanical engineering, materials science, electrical engineering, or a related field and 1–3 years of experience in the design/development of semiconductor packages; or (iii) a Ph.D.-level degree in mechanical engineering, materials science, electrical engineering, or a related field and some experience in the area of semiconductor packaging.

Pet. 18–19 (citing Ex. 1002 ¶¶ 21–23).

For purposes of this Decision, we apply Petitioner’s definition of the level of ordinary skill in the art.⁷

D. Obviousness over Furuya and Takizawa

Petitioner asserts that the subject matter of claims 1–4, 6–8, 10–13, and 15–17 would have been obvious to a person of ordinary skill in the art at the time of the invention in light of the teachings of Furuya and Takizawa. Based on the current record, we are persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted obviousness ground with respect to claims 1–4, 6–8, 10–13, and 15–17.

⁷ To the extent Patent Owner proposes a materially different level of ordinary skill in the art, that difference and its effect on the unpatentability analysis should be explicitly set forth in Patent Owner’s Response.

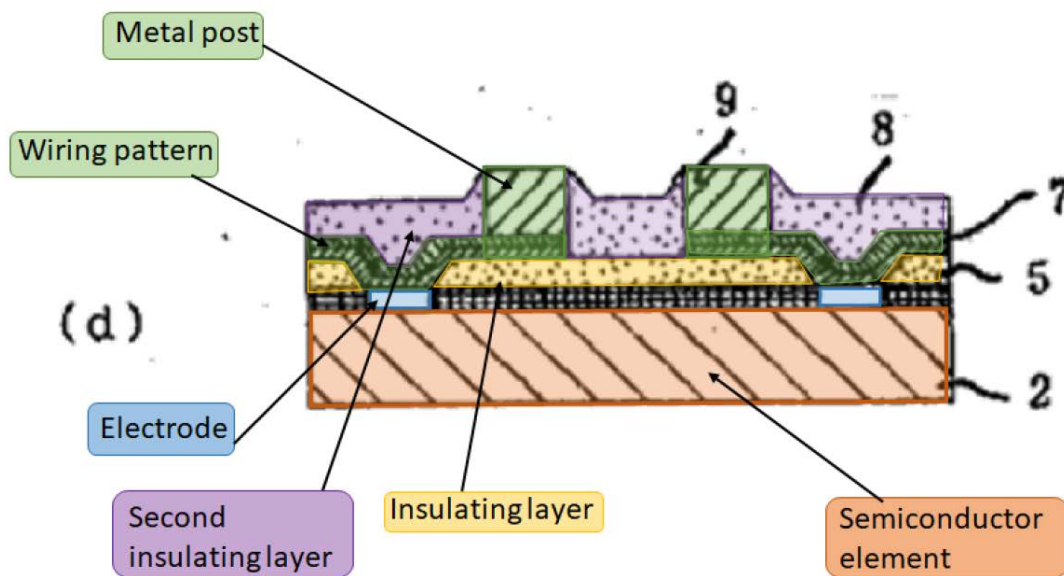
1. Summary of Furuya

Furuya is titled “Semiconductor Device and Method of Manufacturing Same” and relates “to . . . semiconductor devices, which are known as a chip size packages (CSPs), in which a wiring layer is formed on a semiconductor element, and to a method for manufacturing the same.” Ex. 1006, ¶ 1, [54].

Furuya discloses a semiconductor device that includes “an electrode which has been formed on a semiconductor element.” *Id.* ¶ 16. Furuya further discloses “a wiring pattern, which is connected with the electrode of the semiconductor element, [that] is formed on the first insulating layer [and] a metal post for external connection [that] is formed on the wiring pattern.” *Id.* Furuya also discloses an insulation layer “which is in close contact with the wiring pattern [and that] is formed in a manner so as to cover a side face of the metal post excluding a tip surface of the metal post.” *Id.*

Furuya “provid[es] a highly reliable chip-size package type semiconductor device in which the connection strength between the metal post and the wiring pattern is high and the reliability of the electrical connection with the outside is high [thus] improving the reliability of external connections.” *Id.* ¶ 15. Furuya accomplishes this objective by first forming “a first insulating layer 5, which has substantially the same shape as a passivation film 4, . . . on the passivation film 4, in a manner so as to expose electrodes 3, which have been formed on a semiconductor element 2.” *Id.* ¶ 27. Next, “a wiring pattern 7 (wiring layer) . . . is connected with the electrodes 3 . . . formed on the first insulating layer 5” and “metal posts 9 for external connection . . . are formed at predetermined positions on the wiring pattern 7.” *Id.* Then, “a second insulating layer 8 is formed . . . in

close contact with the wiring pattern 7 and the first insulating layer 5, and which covers the side face of the metal post 9 excluding the tip surface of the metal post 9.” *Id.* Finally, the “semiconductor element is resin-sealed with sealing resin 1 in a manner to expose the tip surface of the metal post 9, and an external connection terminal 14 is provided on the metal post 9.” *Id.* Furuya Figure 4(d), annotated by Petitioner and reproduced below, illustrates these features.



Pet. 21. Figure 4(d) is a sectional explanatory view “illustrating one example of a method of manufacturing a semiconductor device of the present invention in the order of the steps,” and has been annotated by Petitioner to identify various aspects of the semiconductor. Ex. 1006 ¶ 67.

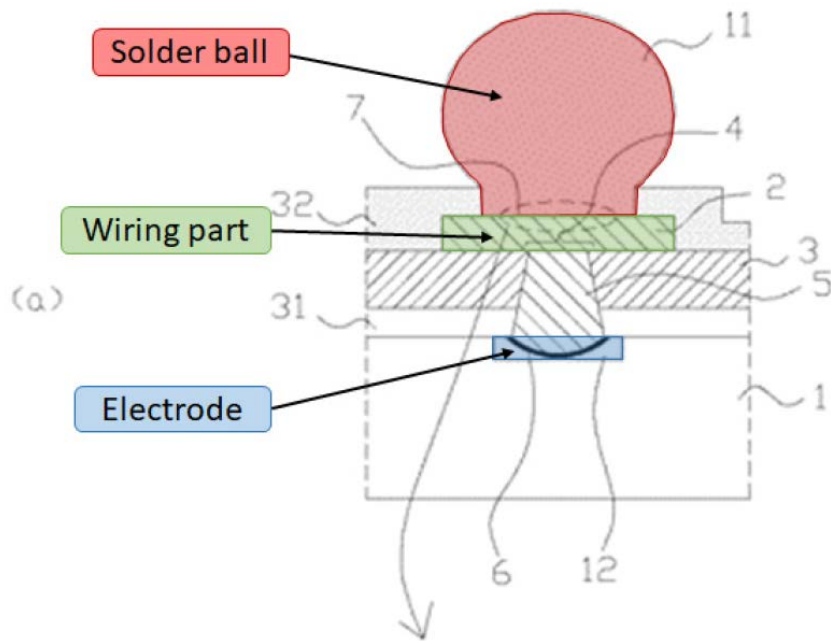
Furuya discloses that the wiring is desirably made from “a material with good conductivity” such as “copper, silver, aluminum, alloys thereof, other metals that are good conductors or the like.” *Id.* ¶ 35. Furuya further discloses that “[i]f copper, silver, or the like is used as the material for the wiring pattern 7” then then “it is preferable to form a metal barrier layer 6

made of a TiW alloy, TiN, TaN, W, Cr or the like as an undercoat layer, and then form the wiring pattern 7 on the metal barrier layer 6.” *Id.* Furuya also discloses that the “metal post[s] . . . formed on the wiring pattern” may also be made of copper. *Id.* ¶ 53.

2. *Summary of Takizawa*

Takizawa is titled “Semiconductor Device and Method of Manufacturing Semiconductor Device.” Ex. 1015, [54]. Takizawa discloses a “semiconductor device [that] has [a] wiring part 2 containing [copper] that is connected to a semiconductor chip 1.” *Id.* ¶ 34. Takizawa further states that “the solder ball 11 containing [tin] is connected to the wiring part 2.” *Id.* ¶ 34. Takizawa also discloses “an electrode part 12 that is placed on the semiconductor chip 1 on the semiconductor device according to the present embodiment, and the solder ball 11 and the electrode part 12 are connected by the metal 5.” *Id.* The Petition contains an annotated version for Takizawa Figure 1, reproduced below, that Petitioner contends shows those features.

[FIG. 1]



Pet. 26. Takizawa Figure 1 “is a cross sectional view illustrating the semiconductor device according to one embodiment of the present invention” and has been annotated by Petitioner to identify the solder ball, wiring part, and electrode. *Id.*; Ex. 1015, 10.

Takizawa also discloses that “a strong [copper-tin] alloy layer is formed on the bonding part between the solder ball 11 and the wiring part 2, or in other words, the land 7 portion on which the solder ball 11 is placed on the wiring part 2.” Ex. 1015 ¶ 35; *see also id.* ¶ 20 (discussing the benefit of having the tin from the solder ball diffuse to the copper to “form a Cu-SN alloy layer with sufficient thickness to prevent detachment of the solder ball near the bonding part, [which] can increase the strength of the bonding parts[] and . . . reduce the occurrence rate of fractures and cracks near the bonding part”). Takizawa further discloses that “[f]orming the [copper-tin]

alloy layer with a thickness of at least $1.87\text{ }\mu\text{m}$. . . was preferable in order to prevent detachment of the solder ball 11.” *Id.* ¶ 40.

3. Claim 1

Petitioner argues that the combination of Furuya and Takizawa teaches all of the limitations recited in claim 1 and that a person of ordinary skill in the art would have been motivated to combine the teachings of the two references. Pet. 34–45.

Petitioner contends Furuya teaches “[a] semiconductor device.” *See id.* at 34. Specifically, Petitioner argues Furuya’s title and preamble both state that Furuya is directed to a semiconductor device. *Id.* (citing Ex. 1006, [54], ¶ 1; Ex. 1002 ¶¶ 87–88).

Petitioner further contends Furuya teaches a “a semiconductor element.” *See id.* at 34–35. Specifically, Petitioner points to semiconductor element 2. *Id.* (citing Ex. 1006 ¶¶ 1, 16, 27, 37, 51, Fig. 1; Ex. 1002 ¶¶ 89–91).

Petitioner also argues Furuya teaches “a first electrode portion formed on the semiconductor element, said first electrode portion comprising a first metal component.” *See id.* at 36–38. Specifically, Petitioner argues “[t]he metal post, wiring pattern, and metal barrier layer collectively act as the first electrode portion and serve to create external electrical connections.” *Id.* at 36 (citing Ex. 1006 ¶¶ 52–53; Ex. 1002 ¶ 92); *see also id.* at 36–38 (citing Ex. 1006 ¶¶ 46, 52–53, Fig. 1; Ex. 1002 ¶¶ 92–95).

Petitioner further contends Furuya and Takizawa both teach “a second electrode portion formed on the semiconductor element and electrically connected to said first electrode portion, said second electrode portion comprising a second metal component different from said first metal

component.” *See id.* at 38–41. Specifically, Petitioner argues Furuya teaches “an external connection terminal (i.e., a second electrode portion) placed at the tip end of the metal post (i.e., the top of a first electrode portion), which external connection terminal is formed of a soldering metal component such as tin.” *Id.* at 38 (citing Ex. 1006 ¶ 36; Ex. 1002 ¶ 97); *see also id.* at 38–40 (citing Ex. 1006 ¶¶ 36, 43–44; Ex. 1002 ¶¶ 97–100). Petitioner further asserts that tin, used in the second electrode portion, “is different from the first metal component of the first electrode portion that includes copper.” *Id.* at 40 (citing Ex. 1002 ¶ 100).

With respect to Takizawa, Petitioner asserts Takizawa teaches a second electrode portion comprising a second metal component because it employs a solder ball (i.e., second electrode portion) that comprises tin and is mounted on a copper wiring layer (i.e., first electrode portion). *Id.* (citing Ex. 1015 ¶¶ 3, 9, 19–20, 33–35; Ex. 1002 ¶ 101).

Petitioner also argues Furuya and Takizawa both teach “a diffusion layer formed between said first electrode portion and said second electrode portion.” *Id.* at 41–43. More specifically, Petitioner contends Furuya teaches “that when a connection is made between the metal post (i.e., first electrode portion) and mounting board using solder (i.e., second electrode portion), that some of the metal post will ‘dissolve and dissipate’ into the solder, creating a diffusion layer” and that a person having ordinary skill in the art “would have understood that this dissolution of the metal post into the solder results in a diffusion layer.” *Id.* at 41–42 (citing Ex. 1006 ¶ 7, Ex. 1002 ¶¶ 103–104). Petitioner further contends that although the above teaching relates to the prior art, the person having ordinary skill in the art “would have understood that the same principle results in a diffusion layer

forming between the external electrical connection 14 and the metal post in Figure 1 as well, considering that similar materials and techniques are used to connect the metal post and mounting board.” *Id.* at 42 (citing Ex. 1002 ¶ 104; Ex. 1006, ¶¶ 55–56).

Additionally, Petitioner contends Takizawa teaches a diffusion layer, formed between its wiring and solder ball. *Id.* at 42–43 (citing Ex. 1015 ¶ 35, Fig. 2(b), Fig. 8(b); Ex. 1002 ¶¶ 105–106).

Petitioner also contends Furuya and Takizawa both teach “wherein said diffusion layer comprises said first metal component and said second metal component.” *Id.* at 43–45. Specifically, Petitioner avers “Furuya describes a soldering process in which a molted eutectic solder containing tin is in direct contact with a copper metal external electrode” and that a person having ordinary skill in the art would know that “when solder containing tin (Sn) is connected in a molten state to a copper electrode (Cu), the tin and copper form a Sn-Cu diffusion layer.” *Id.* at 43–44 (citing Ex. 1006 ¶¶ 55–56; Ex. 1002 ¶ 108; Ex. 1001, 2:12–29) (emphasis omitted).

Alternatively, Petitioner asserts “Takizawa discloses a diffusion layer that forms between the first and second electrode portions. Takizawa further discloses that the diffusion layer comprises the first metal component (from the first electrode portion) and the second metal component (from the second electrode portion).” *Id.* at 44 (citing Ex. 1015 ¶¶ 33–34; Ex. 1002 ¶ 110); *see also id.* at 44–45 (citing Ex. 1015 ¶¶ 3, 9, 19–20, 33–35, 42, 44, Figs. 2, 8; Ex. 1002 ¶¶ 110–113).

Finally, Petitioner argues a person having ordinary skill in the art would have been motivated to combine the relevant teachings of Furuya and Takizawa. *See id.* at 31–34. According to Petitioner, a person of ordinary

skill in the art would have “incorporate[ed] Takizawa’s teaching to improve the connection reliability between a solder ball and a metal wire by forming a copper- tin diffusion layer between the wiring and the solder ball in the optimum thickness range of 1.87 μm to 4 μm .” *Id.* at 31–32 (citing Ex. 1002 ¶ 82); *see also id.* at 33–34 (citing Ex. 1002 ¶¶ 35, 86; Ex. 1015 ¶ 40; Ex. 1020, 52–53). In further support of its argument, Petitioner asserts that the two references are in the same field of technology, were filed around the same time, and are directed to similar devices that operate in a similar manner and address a similar problem. *Id.* at 32–33 (citing Ex. 1002 ¶¶ 82–85; Ex. 1006, [57], ¶¶ 8, 15, Fig. 1; Ex. 1015, [57], ¶¶ 6–10, Fig. 1(a)). Petitioner further asserts that “combining the thicker alloy layer of Takizawa to the semiconductor of Fuyura . . . would have led a [person having ordinary skill in the art] to conclude that the combination would yield a predictable and successful result.” *Id.* at 34 (citing Ex. 1002 ¶ 86).

Having reviewed the record, we determine, for the reasons stated in the Petition and discussed above, that Petitioner has shown sufficiently for the purpose of institution that the combination of Furuya and Takizawa teaches each limitation of claim 1, and that a person of ordinary skill in the art would have had reason to combine the references’ teachings in the manner asserted with a reasonable expectation of success.

4. Claim 10

For most of the limitations recited in independent claim 10, Petitioner relies on arguments and evidence discussed above with respect to independent claim 1. *See id.* at 56–57.

In addition to the limitations recited in claim 1, claim 10 further recites: “wherein . . . said first electrode portion and said diffusion layer

have a combined thickness in the range of 10 μm to 20 μm .” Ex. 1001, 27:8–9, Certificate of Correction. Petitioner asserts Furuya in combination with Takizawa teaches this additional limitation. Pet. 58–62.

Specifically, Petitioner contends that Furuya teaches “that the metal post portion of the first electrode portion is 15 μm ” and that the wire portion is 0.7 μm thick, resulting in “the entire thickness of the first electrode portion in Furuya [being] 15.7 μm .” *Id.* at 58 (citing Ex. 1006 ¶ 52; Ex. 1002 ¶ 140).

Petitioner further contends that because Furuya is silent as to the size of the diffusion layer, a person of ordinary skill in the art would turn to Takizawa, which teaches the advantages of having a specific thickness to the diffusion layer. *Id.* at 58–60. Based on the ranges in Takizawa, Petitioner asserts that the combined thickness could range between 15.7 μm and 19.7 μm , which is within the range cited in claim 10. *Id.* at 58–61 (Ex. 1015 ¶¶ 9–12, 35, 40, Figs. 2, 8; Ex. 1002 ¶¶ 140–141).

Having reviewed the record, we determine, for the reasons stated in the Petition and discussed above, that Petitioner has shown sufficiently for the purpose of institution that the combination of Furuya and Takizawa teaches each limitation of claim 10, and that a person of ordinary skill in the art would have had reason to combine the references’ teachings in the manner asserted with a reasonable expectation of success.

5. Dependent Claims 2–4, 6–8, 11–13, and 15–17

Because Petitioner has demonstrated a reasonable likelihood of success in proving that at least one claim of the ’001 patent is unpatentable, we will institute on all grounds and all claims raised in the Petition. Given that we have found Petitioner has satisfied its burden to move forward as to

claims 1 and 10, it is not necessary for us to provide an assessment of every other ground raised by Petitioner, especially, whereas here, Patent Owner has elected not to file a Preliminary Patent Owner's Response.

Nevertheless, we note that Petitioner provides detailed explanations supported by the testimony of Dr. Hatalis and specific citations to Furuya and Takizawa indicating where in the references the limitations of claims 2–4, 6–8, 11–13, and 15–17 are taught. Pet. 46–56, 62–63. For purposes of this Decision, we agree with Petitioner's analyses of claims 2–4, 6–8, 11–13, and 15–17 and adopt them as our own.

E. Furuya, Takizawa, and Yaguchi

Petitioner asserts that the subject matter of claims 5 and 14 would have been obvious to a person of ordinary skill in the art at the time of the invention in light of the teachings of Furuya, Takizawa, and Yaguchi. Based on the current record, we are persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted obviousness ground with respect to claims 5 and 14.

1. Summary of Yaguchi

Yaguchi is titled “Semiconductor Device and Semiconductor Module” and is directed to “to a small semiconductor device having a semiconductor element with various functions manufactured using wafer processes and to a semiconductor module having a semiconductor device with external terminals mounted on a printed wiring board.” Ex. 1011, [54], 1:5–9.

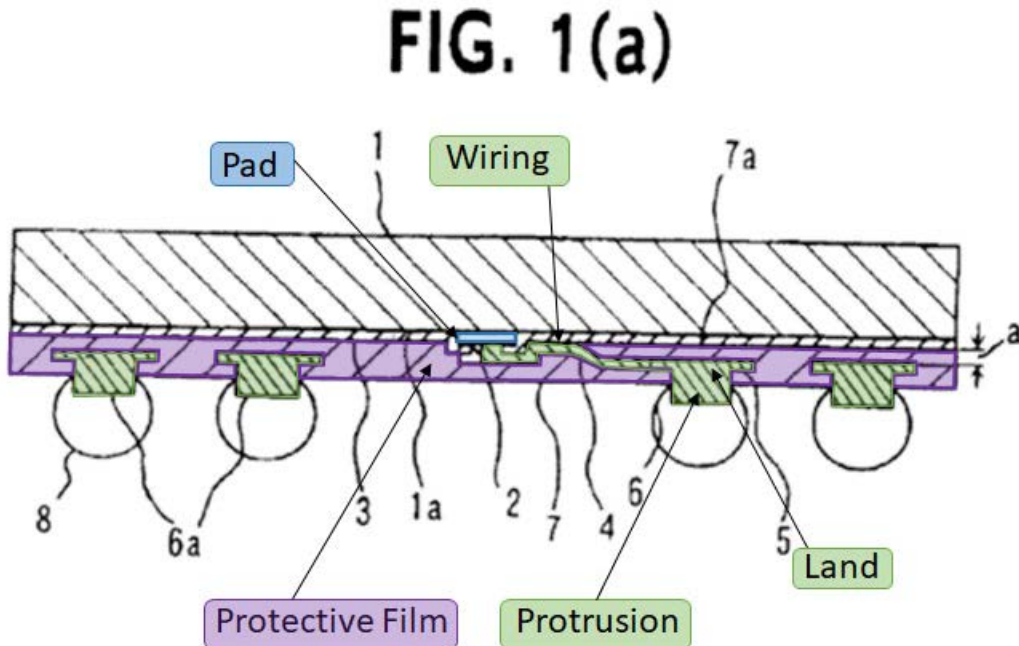
Yaguchi discloses a semiconductor including

a semiconductor element 1, a passivation film 3 formed so the surface of a pad 2 on the semiconductor device surface 1a is exposed, a conductive wire line 4 connected to the pad 2, a land

5 connected to the conductive wire line 4, a protective film 7, a protrusion 6 provided on the land 5, and an external terminal 8.

Id. at 9:5–10. Yaguchi further discloses that there are various passivation and insulation layers, including a protective film formed on the conductive wiring, land, and protrusions. *Id.* at 9:5–19. Yaguchi further teaches that “[a] part of the protrusion 6 protrudes through the protective film 7 and this protruding part 6a is bonded to the external terminal 8.” *Id.* at 9:16–17.

Yaguchi Figure 1(a), annotated by the Petitioner, is reproduced below.



Pet. 29. Figure 1(a) depicts “a cross-sectional view of a semiconductor device according to a first embodiment of the present invention and plan view with a portion of its protective film removed” and has been annotated by the Petitioner to identify the pad, wiring, protective film, protrusion, and land. Ex. 1011 7:30–31; Pet. 29.

2. *Claim 5 and 14*

Claims 4 and 14 indirectly depend from claim 1 and 10, respectively.

Claim 5 and 14 further recite:

an insulating film formed on said metal wiring,
wherein an opening of said insulating film exposes a surface of
the first electrode portion, and
wherein said surface of the first electrode portion is flush with
or higher than a surface of the insulating film.

Ex. 1001 26:42–46, 28:2–6.

Petitioner argues Furuya teaches “an insulating film formed on said metal wiring.” *See* Pet. 67. Specifically, Petitioner argues Furuya teaches a second insulating layer formed on top of the wiring pattern. *Id.* (citing Ex. 1006 ¶¶ 16, 27, 63, Fig. 1; Ex. 1002 ¶ 155).

Petitioner further argues Furuya teaches “an opening of said insulating film exposes a surface of the first electrode portion.” *Id.* at 68–69. Specifically, Petitioner contends Furuya teaches “forming an opening in insulating layer 8 to expose a surface of the first electrode portion.” *Id.* at 68 (citing Ex. 1002 ¶¶ 156–157; Ex. 1006 ¶¶ 24, 27, 46, 62, Fig. 1).

Petitioner also argues Furuya in combination with Yaguchi teaches “said surface of the first electrode portion is flush with or higher than a surface of the insulating film.” *See id.* at 69–73. Specifically, Petitioner contends Furuya teaches that

after the metal post 9 is formed, the second insulating layer 8 is formed, using the insulating resin that has been applied and formed, and at this time, this is formed so that the height of the second insulating layer 8, excluding the side face of the metal post 9, is such as to be a position that is lower than the height of the tip surface of the metal post 9.

Id. at 70 (quoting Ex. 1006 ¶ 47 (emphasis omitted)). Based on the above, Petitioner argues that a person having ordinary skill in the art film, “would have understood that the exposed top indicates that the insulating film is at most flush with (or approximately flush as the ’001 Patent uses the term), and generally lower than, the top surface of the metal post.” *Id.* at 70–71 (citing Ex. 1002 ¶¶ 159–162).

Alternatively, Petitioner contends Yaguchi explicitly teaches that “the first electrode portion is flush with or higher than the insulating film because it explains the first electrode portion is composed of a ‘land,’ . . . connected to the conductive wiring and a protrusion formed on the land.” *Id.* at 71 (citing Ex. 1011, 4:18–29; Ex. 1002 ¶ 163). That is, according to Petitioner, “Yaguchi explains that although some of the protrusion 6 is covered by the protective film, ‘[a] part of the protrusion 6 protrudes through the protective film 7 and this protruding part 6a is joined to the external terminal 8.’” *Id.* at 72 (quoting Ex. 1011, 9:16–17). Petitioner further asserts “because protruding part 6a extends beyond the protective film, or insulating layer, Yaguchi teaches that the first electrode portion is higher than the insulating film.” *Id.* at 72–73 (citing Ex. 1002 ¶ 164).

Petitioner also contends that a person of ordinary skill in the art “would have been motivated to improve the semiconductor device disclosed in Furuya by looking to the teachings of Yaguchi for improving the connection reliability for a semiconductor mounted on a printed wiring board (i.e., PCB).” *Id.* at 64 (citing Ex. 1002, ¶ 150). In support of its argument, Petitioner asserts that the two references are in the same field of technology, were filed around the same time, and are directed to similar devices that operate in a similar manner and address a similar problem. *Id.*

at 64–66 (citing Ex. 1002 ¶¶ 150–153; Ex. 1006, [57], ¶¶ 8, 15 Fig. 1; Ex. 1011, 2:7–3:26, 4:18–20, 9:6–10, 9:13–19, 24:5–8, Fig. 1(a)). Thus, according to Petitioner, a person of ordinary skill in the art “would have been motivated to add a protrusion that extended above the insulating film in Furuya to ensure a better connection, as taught by Yaguchi” and, “[b]ecause such a combination would be nothing more than applying known techniques to similar systems, . . . would have expected the combination to yield a predictable result and be successful.” *Id.* at 66 (citing Ex. 1002 ¶ 154; Ex. 1011, 4:18–29).

Having reviewed the record, we determine, for the reasons stated in the Petition and discussed above, that Petitioner has shown sufficiently for the purpose of institution that the combination of Furuya, Takizawa, and Yaguchi teaches each limitation of claims 5 and 14, and that a person of ordinary skill in the art would have had reason to combine the references’ teachings in the manner asserted with a reasonable expectation of success.

F. Obviousness over Furuya, Takizawa, and Nozawa

Petitioner asserts that the subject matter of claim 9 and 19 would have been obvious to a person of ordinary skill in the art at the time of the invention in light of the teachings of Furuya, Takizawa, and Nozawa (Ex. 1012). Based on the current record, we are persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted obviousness ground with respect to claims 9 and 18.

1. Summary of Nozawa

Nozawa “relates to a semiconductor device and method of manufacturing the same, a circuit board and an electronic instrument.” Ex. 1012, 1:6–8.

Nozawa discloses a “semiconductor chip 100 [upon which] a plurality of electrodes 104 are formed.” *Id.* at 4:34–36. Nozawa further discloses that “the electrodes 104 are connected [to] an interconnect layer 120 [which] extends into a region avoiding the electrodes 104.” *Id.* at 4:42–45. “In the position (part or region) of the interconnect layer 120 avoiding the electrodes 104 [is] provided a conducting layer 122,” upon which “an underlying metal layer 124” is placed. *Id.* at 4:46–5:11. Additionally, a resin layer 126 is formed on the interconnect layer 120 and a bump 200 is provided on the underlying metal layer 124. *Id.* at 5:12–20, 5:40–52. According to Nozawa, the claimed invention results in a device that allows for a reliable connection to be formed directly between the semiconductor device and the substrate resulting in electronic instruments that are more compact and lightweight. Ex. 1012, 1:41–48. Figure 1 of Nozawa, which shows these features, is reproduced below.

FIG. 1

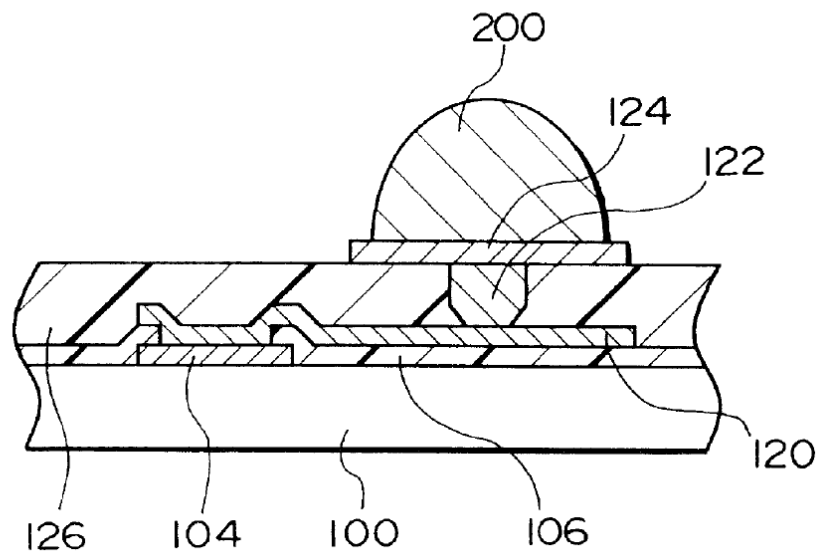


FIG. 1 shows a first embodiment of the semiconductor device of the present invention. The semiconductor device shown in

FIG. 1 comprises a semiconductor chip (semiconductor chip) 100 on which is provided a bump 200 with a stress relief function interposed. This configuration allows flip-chip having a stress relief function, and can also be classified as CSP (Chip Size/Scale Package).

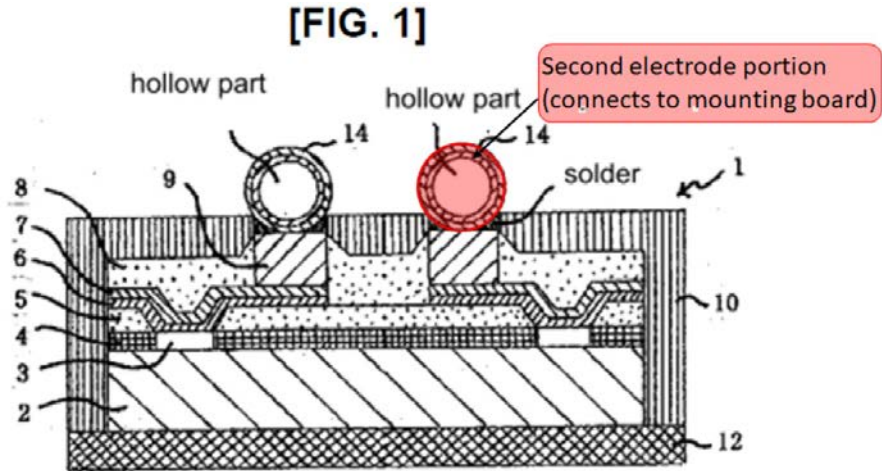
Ex. 1012, 4:26–32.

2. Claims 9 and 18

Claims 9 and 18 depend, respectively, from claims 1 and 10, and further require “a substrate having a wiring electrode, wherein said wiring electrode is electrically connected to said second electrode portion.” Ex. 1001, 26:57–60, 28, 17–20.

Petitioner argues “because the external connection terminal (i.e., second electrode portion) forms an external electrical connections with electrodes on a mounting board or PCB (i.e., wiring electrode),” Furuya teaches the additional limitations of claims 9 and 18. Pet. 77 (citing Ex. 1002 ¶ 174; Ex. 1006 ¶ 6; Ex. 1001, 1:23–35, 2:4–15).⁸ In support of its argument, Petitioner directs us to an annotated version of Furuya Figure 1, reproduced below, which identifies external connection terminal 14 as the second electrode portion

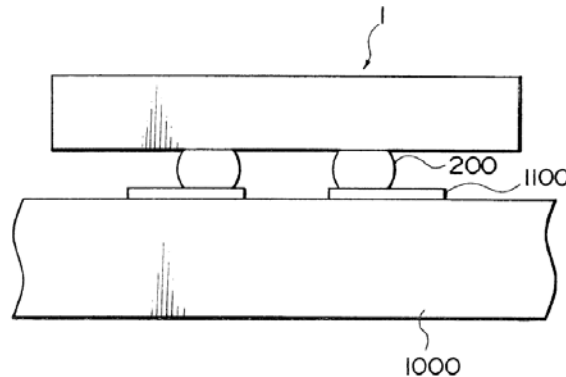
⁸ Petitioner relies on the same evidence for both claims 9 and 18. Pet. 81.



Pet. 78. Figure 1 “is a sectional explanatory view, schematically illustrating one embodiment of a semiconductor device” and has been annotated by Petitioner to identify the second electrode portion which connects to a mounting board. Ex. 1006 ¶ 67; Pet. 78.

Alternatively, Petitioner relies on Nozawa, which Petitioner argues “explicitly discloses a substrate having a wiring electrode that is electrically connected to the second electrode portion.” Pet. 79 (citing Ex. 1002 ¶ 179). More specifically, Petitioner relies on Figure 9 and the corresponding description, which Petitioner states “illustrates the connection between the semiconductor device and the circuit board.” *Id.* at 79–80 (citing Ex. 1012, 8:30–44, Fig. 9; Ex. 1002 ¶ 180). Nozawa Figure 9 is reproduced below.

FIG. 9



Ex. 1012, Fig. 9. Nozawa Figure 9 “shows a circuit board on which the semiconductor device of [Nozawa] is mounted.” *Id.* at 4:12–14.

Petitioner also contends that a person of ordinary skill in the art “would have known that applying the teaching of Nozawa to the device described in Furuya would provide benefits including integration with a wide variety of PCBs for a wide range of applications.” Pet. 74 (citing Ex. 1002 ¶ 169). In further support of its argument, Petitioner asserts that the two references are in the same field of technology, were filed around the same time, and are directed to similar devices that operate in a similar manner and address a similar problem. *Id.* at 75–76 (citing Ex. 1002 ¶ 172; Ex. 1006, [57], Fig. 1; Ex. 1012, 1:53–64, Fig. 1). Thus, according to Petitioner, it would have been “natural” to a person of ordinary skill in the art to apply “the teachings of Nozawa to the device in Furuya” and, “[b]ecause such a combination would be nothing more than applying known techniques to similar systems, a [person having ordinary skill in the art] would have expected the combination to yield a predictable, successful result.” *Id.* at 76 (citing Ex. 1002 ¶ 173).

Having reviewed the record, we determine, for the reasons stated in the Petition and discussed above, that Petitioner has shown sufficiently for the purpose of institution that the combination of Furuya, Takizawa, and Nozawa teaches each limitation of claims 9 and 18, and that a person of ordinary skill in the art would have had reason to combine the references' teachings in the manner asserted with a reasonable expectation of success.

III. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review of all challenged claims (claims 1–18) of the '001 patent is instituted with respect to all grounds set forth in the Petition (*see* Section I.E, *supra*); and;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '001 patent is hereby instituted commencing on the entry date of this Decision, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

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Patent 6,954,001 B2

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