IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Jentsung Lin	
U.S. Patent No.:	7,693,002	Attorney Docket No.: 39521-0054IP1
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Appl. Serial No.:	11/548,132	
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Title:	DYNAMIC WORD LINE DRIVERS AND DECODERS FOR	
	MEMORY ARRAYS	

DECLARATION OF Robert W. Horst, Ph.D.

I, Robert W. Horst, Ph.D., of San Jose, CA, declare that:

QUALIFICATIONS AND BACKGROUND INFORMATION

1. I am currently an Adjunct Research Professor in the Department of

Electrical and Computer Engineering the University of Illinois at Urbana-Champaign and am also an independent consultant at HT Consulting. I am an independent consultant with more than 30 years of expertise in the design and architecture of computer systems. I have testified as an expert witness and consultant in patent and intellectual property litigation as well as *inter partes* reviews and re-examination proceedings. My curriculum vitae is provided (as APPLE-1004).

2. I earned my M.S. (1978) in electrical engineering and Ph.D. (1991) in computer science from the University of Illinois at Urbana-Champaign after earning my B.S. (1975) in electrical engineering from Bradley University. During my master's program, I designed, constructed and debugged a shared memory

parallel microprocessor system. During my doctoral program, I designed and simulated a massively parallel, multi-threaded task flow computer.

3. After receiving my bachelor's degree and while pursuing my master's degree, I worked for Hewlett-Packard Co. While at Hewlett-Packard, I designed the micro-sequencer and cache of the HP3000 Series 64 processor. From 1980 to 1999, I worked at Tandem Computers, which was acquired by Compaq Computers in 1997. While at Tandem, I was a designer and architect of several generations of fault-tolerant computer systems and was the principal architect of the NonStop Cyclone superscalar processor. The system development work at Tandem also included development of the ServerNet System Area Network and applications of this network to fault tolerant systems and clusters of database servers.

4. Since leaving Compaq in 1999, I have worked with several technology companies, including 3Ware, Network Appliance, Tibion, and AlterG in the areas of network-attached storage and biomedical devices. From 2012 to 2015, I was Chief Technology Officer of Robotics at AlterG, Inc., where I worked on the design of anti-gravity treadmills and battery-powered orthotic devices to assist those with impaired mobility.

5. In 2001, I was elected an IEEE Fellow "for contributions to the architecture and design of fault tolerant systems and networks." I have authored

over 30 publications, have worked with patent attorneys on numerous patent applications, and I am a named inventor on 82 issued U.S. patents.

6. My patents include those directed to memory system design including U.S. Pat. No. 5,146,589 (Refresh control for dynamic memory in multiple processor system), U.S. Pat. No. 5,287,472 (Memory system using linear array wafer scale integration architecture), and U.S. Pat. No. 5,329,629 (Apparatus and method for reading, writing, and refreshing memory with direct virtual or physical access). My patents also include aspects of circuit design including U.S. Pat. No 5,034,964 (N:1 time-voltage matrix encoded I/O transmission system) and U.S. Pat. No. 9,893,604 (Circuit with low DC bias storage capacitors for high density power conversion).

7. In writing this Declaration, I have considered the following: my own knowledge and experience, including my work experience in the fields of memory systems and circuit design and my experience in working with others involved in those fields. In addition, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

• U.S. Patent No. 7,693,002 (APPLE-1001), and its accompanying prosecution history (APPLE-1002)

- U.S. Patent No. 4,951,259 ("Sato") (APPLE-1005)
- U.S. Patent Pub. No. 2006/0098520 ("Asano") (APPLE-1006)

- Kiyoo Itoh, VLSI Memory Chip Design, (Springer 2001) ("Itoh")
 (APPLE-1007)]
- Stephen Brown et al., Fundamentals of Digital Logic with Verilog Design, (McGraw Hill 2003) ("Brown") (APPLE-1009)
- U.S. Patent No. 6,483,771 to Tae-jeen Shin ("Shin") (APPLE-1011)

OVERVIEW OF CONCLUSIONS FORMED

8. This expert Declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions:

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-28 and 31-37 of the '002 patent are rendered obvious by Sato.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-17, 20-28, and 31-36 of the '002 patent are rendered obvious by Asano and Itoh.

BACKGROUND KNOWLEDGE ONE OF SKILL IN THE ART WOULD HAVE HAD PRIOR TO THE PRIORITY DATE OF THE '002 PATENT

9. The technology in the '002 patent at issue generally relates to a circuit device that includes a first and second logic to decode a memory address. The patent specification and figures include CMOS circuits and memory system block diagrams. Prior to the priority date of the '002 patent, there existed numerous

products, publications, and patents that implemented or described the functionality claimed in the '002 patent. Thus, the methodology of the '002 patent was well-known in the prior art. Further, to the extent there was any problem to be solved in the '002 patent, it had already been solved in the prior art systems before the priority date of the '002 patent.

10. Fig. 1 of the '002 patent is a block diagram showing the elements for driving wordlines in a memory array.



The wordline drivers are partitioned into "groups," with each group including four wordline drivers. The diagram shows the first and last group of the 16 total groups. A group is selected by decoding four bits of the address with the

4-to-16 decoder, which produces the 16 decoder output signals called the "Partially Decoded Address" in this figure. This signal is also called the "common address input," and after passing through an in inverter (shown in Fig. 3 below) is called the "shared address input," or "shared address line." Note that the signal after the inverter merely changes the AND decoder to a NAND decoder.

> the decoded output of the four-to-sixteen bit memory address decoder 108 may be utilized via a logical AND operation to selectively activate a wordline driver of the group of wordline drivers 104, for example.

'002 patent at 4:5-9.

In general, each group of wordline drivers, such as the group of wordline drivers 104 may share a common partially decoded address input, such as the partially decoded address line (0) 120 for the group of wordline drivers 104, reducing layout area usage and layout complexity.

'002 patent at 3:46-50.

12. The concept of decoding part of a memory address is well known in

the art. There are often multiple stages of decoding before the final selection that combines the first stage decoder outputs to select the final output.

13. Continuing with Fig. 1, the selected group of wordline drivers also

receives four clock lines from a "conditional clock generator" that receives a clock

input and four outputs from a decoder, which decodes two more bits of the

memory address. The "conditional clock generator" has no diagram to show the

structure, but is described as follows:

The two-to-four bit decoder112 may decode the first portion of the memory address and may provide the decoded portion to the conditional clock generator110. The conditional clock generator 110 receives a clock signal via the clock input 118 and selectively applies the clock signal to a selected one of the clock outputs 124, 126, 128 and 130. . . . In a particular embodiment, the conditional clock generator 110 may derive the clock outputs 124, 126, 128 and 130 from a single clock.

'002 patent at 3:26-36 (emphasis added).

14. Here, a POSITA would have understood the clock generator to

produce an output whose characteristics track those of an input clock signal. For example, a POSITA would have understood "selectively appl[ying] the clock signal" to a selected output and "deriv[ing] the clock output" to mean simply that the selected clock output generally tracks with the input clock signal. For example, the input clock could have been ANDed with the decoder outputs in such a way that the clock appears on one clock output while the other three are held low. This structure is also supported by the text that states that the other clocks are held at a ground voltage level.

In a particular illustrative embodiment, a conditional clock generator, such as the conditional clock generator110 in FIG. 1, applies the clock signal to a selected clock output, such as the clock output 126. The other clocks 124, 128 and 130 may be held at a ground voltage level.

'002 patent at 5:54-58 (emphasis added).

15. When a group of wordline drivers is selected by receiving the partially decoded address signal, only one of the clock lines will be active, with the active clock line determining which wordline to drive.

16. The '002 patent attributes particular significance to the way it drives only one of the four clocks at a time, and that the capacitance driven by these clocks is less than if a single clock were to drive all of the word lines. However, as is clear from the cited art that follows, the '002 patent was far from the first to realize the advantage of driving more clocks with fewer loads per clock. In particular, Sato, Asano and Itoh all have the same type of conditional clock generator reducing the capacitive load on each clock.

17. Fig. 2 of the '002 patent shows four static memory cells, each represented by latches formed form a pair of inverters. Each bit connects to a word line, a bit line and a complemented bit line. This particular arrangement of the memory cell is not part of the issued claims.

18. Fig. 3 shows the internal structure of the wordline drivers.



Each driver is formed with a P-channel and an N-channel transistor,
 followed by an inverter. The clock line connects to the gates of the P-channel and

N-channel transistors and the selection signal (inversion of the partially decoded address) connects to the N-channel transistor's source terminal.

20. As an example of operation, assume that the address input selects group 0 and that CLK<0> is enabled. In this case, the output of the inverter formed by Mp0 and Mn0 drives ddh0 with the inverted clock signal which is then inverted again as it passes through inverter XWL0 to drive WL<0>. Groups that are not selected cannot pull lines ddh0-3 low because their N-channel transistor source lines are not at ground potential.

21. During the low clock phase, when all four CLK signals are low, Mp0-Mp3 pull all the ddh lines high which pulls all of the wordlines WL<0>-WL<3> low. A wordline driver with a low clock (and its ddh line high) is said to be in the static precharge state, and the driver with an active clock is said to be in the evaluation state.

22. The particular arrangements of transistors in the 002 patent is not particular unique or noteworthy. For instance, Sato has a nearly identical structure that has a wordline driver with P and N transistors forming an inverter with input connected to a conditional clock, and with the N-channel source node connected to a NAND decoder.

23. Fig 4 of the '002 patent shows a physical layout of transistors that could implement the structures shown in the block diagrams. No particular layouts are part of the issued claims.

24. Fig. 5 is a flowchart describing the structure shown in the block diagrams. The described steps do not add new information and are largely redundant with the description of operation of the block diagrams.

25. In summary, the '002 patent is primarily disclosing a wordline decoder with part of the address decoded to select a group, and the selection within the group determined by a conditional clock based on decoding of other bits of the memory address. I find that this structure was not unique at that time and similar or identical wordline decoders were previously disclosed by others including Sato, Asano and Itoh.

26. A review of other relevant literature available at the time further shows that the idea of dynamic wordline drivers and decoders for memory arrays was well known in the technical community by 2006. In addition to the references I discuss below that render obvious the '002 patent, the following exemplary references demonstrate the prevalence of these ideas in the prior art:

- U.S. Patent No. 4,338,679 to James E. O'Toole;
- U.S. Patent No. 5,166,554 to Chitranjan N. Reddy, et al.;
- U.S. Patent No. 5,327,026 to Kim C. Hardee, et al.;

• U.S. Patent No. 6,914,849 to Tai Anh Cao, et al.

27. Thus, based on the foregoing and upon my experience in this area, a person of ordinary skill in the art in this field at the relevant time frame ("POSITA") would have had at least an undergraduate degree in electrical engineering, or a related field, and three years of experience in the design of memory systems and circuits. Alternatively, a person of ordinary skill with less than the amount of experience noted above could have had a correspondingly greater amount of educational training such a graduate degree in a related field.

28. Based on my experiences, I have a good understanding of the capabilities of a POSITA. Indeed, I have participated in organizations and worked closely with many such persons over the course of my career.

29. I am well qualified in the memory and circuit design technologies related to the '002 Patent and I was a person of at least ordinary skill in the art in the '002 timeframe.

STATE OF THE ART AND OVERVIEW OF TECHNOLOGY AT ISSUE Circuit design

30. The '002 patent and related prior art include circuits presented as diagrams at the gate level (AND, NAND, OR, NOR and inverters) as well as diagrams showing individual transistors. The gate-level diagrams use standard notation for gates and use bubbles to indicate signal inversion.

31. The circuit level diagrams use a variety of different conventions to draw transistors. For the art cited in this report, the transistors are primarily enhancement mode metal-oxide-semiconductor field-effect transistors (MOSFETs), sometimes just called field-effect transistors (FETs). Below I have shown some of the different ways of drawing these transistors:



32. For the purposes of analyzing the '002 patent, the P-channel and Nchannel transistors can be analyzed as if they are ideal switches, with the Pchannels conducting when the gate (G) is negative relative to the source (S), and the N-channels conducting when gate is positive relative to the source.

33. Note that the left two sets of transistor diagrams (as represented in the '002 patent, Bridges, Sato and Asano) have no indication to show which terminal is source (S) and which is drain (D). The orientation matters because the FETs have a "body diode" that always conducts current when the source is at a higher voltage than the drain, even if the gate voltage would otherwise cause it not to conduct. It is usually easy for a POSITA to understand which terminal should be

connected to the source because the source usually connects to a positive voltage rail for a P-channel and to ground for an N channel. However, in some circuits, more analysis may be needed to determine the transistor orientations. The right two representations for transistors do not have this ambiguity and clearly indicate which terminal is the source and which is the drain. The fact that the '002 patent uses the ambiguous notation indicates that a POSITA should be assumed to have sufficient skill in circuit design to understand how such transistors would normally be connected.

34. Most of the circuits in this report show a mix of N-channel and Pchannel transistors, often configured as standard CMOS circuits. For instance, a CMOS inverter has N-channel and P-channel transistors with gates connected together, the source terminals to ground and the positive voltage rail, and the drains connected together and to the output.

Clocked decoder circuits

35. Clocked decoder circuits are well known in the art. Patent 5,291,076 (the "Bridges" patent) gives several examples of clocked decoder circuits. Fig. 1 of Bridges, reproduced below, shows a simple clocked decoder.



Bridges '076, Fig 1

36. Bridges' Fig. 1 shows a CLOCK signal that, when low, causes Pchannel transistor Q4 to conduct to precharge node 12. When CLOCK transitions to high, the precharge is removed and if the A1-A3 are all high, N-channel MOSFETs Q1, Q2, Q3 and Q5 all conduct to cause 12 to be pulled low. Note that if any of the A1-A2 inputs is low, no current passes through Q1-Q4 to pull node 12 low or high and the node stays at the high level until leakage or other events cause the node to drift back down to the low logic level. *See e.g.*, Bridges, 3:1-4:24.

37. A full clocked decoder circuit would include eight copies of the NAND gate of Fig 1, each with the eight different combinations of true and complement inputs A1-A3. After the precharge, one of the eight decoder outputs is pulled low and the other seven remain high, causing a single output line to be selected. This type of decoder is called a NAND decoder because each output has

the same structure as a NAND gate. The function is the same as a NAND gate in which the output is low only when all inputs are high.

38. The clock input of a clocked decoder switches between two phases of operation that are often referred to as the precharge and evaluation phases.

39. Other examples of clocked decoder are shown in all three of Sato's embodiments, as shown in Sato Fig. 1, 2 and 3. These circuits employ clocked decoders controlled by the timing (clock) signal ϕ ce. When ϕ ce is low, these circuits precharge the inputs to the final inverters which then drive all of the word lines W0-W3 low. When ϕ ce is high, the circuits evaluate the address lines causing a single input to a final inverter to be pulled low, thus causing only that word line to be driven high while the others are driven low.

SRAM and DRAM

40. The common acronyms SRAM and DRAM stand for Static Random Access Memory and Dynamic Random Access Memory. In general, these terms refer to whether the memory cells are static and hold information indefinitely, or the cells are dynamic and need to be periodically refreshed to maintain their state. Other parts of memory chips can also be static or dynamic independently of whether the memory cells are static or dynamic.

41. The '002 patent is directed to "dynamic wordline drivers and decoders for memory arrays." '002 patent at 1:8-9. Dynamic (clocked) drivers and

decoders can be used in both SRAMs and DRAMs. As in the '002 patent, some of the cited prior art cited does not require any particular type of memory cell and those techniques could be applied to SRAM, DRAM or other types of memory.

INTERPRETATIONS OF THE '002 PATENT CLAIMS AT ISSUE

42. I understand that the best indicator of claim meaning is its usage in the context of the patent specification as understood by a POSITA. I further understand that the words of the claims should be given their plain meaning unless that meaning is inconsistent with the patent specification or the patent's history of examination before the Patent Office. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time of the invention was made (not today). Because I do not know at what date the invention as claimed was made, I have used the earliest priority date of U.S. Patent No. 7,693,002 as the point in time for claim interpretation purposes. That date was October 10, 2006. I have been asked to provide my interpretation of the following terms and phrases of the '002 patent set forth below.

Claim Constructions

"static precharge state"

43. Claims 18 and 37 recite: "wherein other wordline drivers of the group of wordline drivers are in a <u>static precharge state</u>." In my opinion, the plain meaning of the claim term "static precharge state" in view of the '002

patent specification would include a state in which a fixed voltage level is applied to a wordline driver. See my analysis at paragraphs 19-21 and the '002 patent at 3:52-57; 7:11-15.

44. Based upon my knowledge and experience in this field, I believe that a POSITA would have understood that this interpretation is consistent with the plain meaning of this term and is consistent with the '002 patent specification.

"conditional clock generator"

45. Claim 2 recites "**conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output**." Claims 3, 9, 13, 20-22, 27, 31, 32, and 37 recite similar language. In my opinion, the plain meaning of the claim term "<u>conditional clock generator</u>" in view of the '002 patent specification would include a circuit component that applies a clock signal to one of several output terminals. See my analysis at paragraphs 13-15 and the '002 patent at 3:26-31; 5: 54-58.

46. Based upon my knowledge and experience in this field, I believe that a POSITA would have understood that this interpretation is consistent with the plain meaning of this term and is consistent with the '002 patent specification.

"means for decoding a first portion of a memory address of a memory array"

47. Claim 11 recites: "means for decoding a first portion of a memory address of a memory array." In my opinion, the '002 patent specification describes a "decoder" as a structure for performing the function of "decoding a first portion of a memory address of a memory array." See my analysis at paragraphs 13-15; 35-39 and the '002 patent at 3:26-31; 5: 54-58.

48. Based upon my knowledge and experience in this field, I believe that a POSITA would have understood that this interpretation is consistent with the plain meaning of this term and is consistent with the '002 patent specification.

"means for selectively providing a clock signal to a selected group of wordline drivers based on the first portion of the memory address [of a memory array]"

49. Claims 11 and 27 recite: "means for selectively providing a clock signal to a selected group of wordline drivers based on the first portion of the memory address [of a memory array]." In my opinion, the '002 patent specification describes a "conditional clock generator" as a structure for performing the function of "selectively providing a clock signal to a selected group of wordline drivers based on the first portion of the memory address [of a memory array]." See my analysis at paragraphs 13-15 and the '002 patent at 3:26-31; 5: 54-58.

50. Based upon my knowledge and experience in this field, I believe that a POSITA would have understood that this interpretation is consistent with the plain meaning of this term and is consistent with the '002 patent specification.

"means for decoding a second portion of the memory address"

51. Claim 11 recites: "**means for decoding a second portion of the memory address**." In my opinion, the '002 patent specification describes a "decoder" as a structure for performing the function of "**decoding a second portion of the memory address**." See my analysis at paragraphs 11-12, 35-39 and the '002 patent at 3:46-50; 4:5-9.

52. Based upon my knowledge and experience in this field, I believe that a POSITA would have understood that this interpretation is consistent with the plain meaning of this term and is consistent with the '002 patent specification.

"means for activating a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address"

53. Claims 11 and 27 recite: "means for activating a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address." In my opinion, the '002 patent specification describes a "decoder" as a structure for performing the function of "activating a particular wordline driver of the selected group of wordline

drivers according to the second portion of the memory address." See my analysis at paragraphs 11-12, 18-22 and the '002 patent at 3:46-50; 4:5-9.

54. Based upon my knowledge and experience in this field, I believe that a POSITA would have understood that this interpretation is consistent with the plain meaning of this term and is consistent with the '002 patent specification.

"means for applying the second portion of the memory address to a shared address line"

55. Claim 14 recites: "means for applying the second portion of the memory address to a shared address line." In my opinion, the '002 patent specification describes a "decoder" as a structure for performing the function of "decoding a second portion of the memory address." See my analysis at paragraphs paragraphs 11-12, 18-22 and the '002 patent at 3:46-50; 4:5-9.

56. Based upon my knowledge and experience in this field, I believe that a POSITA would have understood that this interpretation is consistent with the plain meaning of this term and is consistent with the '002 patent specification.

ANALYSIS OF SATO

57. Sato discloses an X address decoder XCDR for either an SRAM or DRAM memory array. Sato's XCDR decodes a memory address (AX0-AXi) to drive selected wordlines (WD0-WDm) of a memory array as indicated by the address. The XCDR includes a pre-decoder PDCR and NAND decoder circuits

(NAG0-NAGk) which each decode a portion of the memory address to activate an appropriate wordline driver.

58. As I illustrated in the annotated Fig. 3 from Sato (below), Sato's X address decoder (XDCR) includes an address input (e.g., internal address input (ax0-axi)) as shown in Fig. 3 and Fig. 4. The PDCR has four clock outputs (ϕ x0- ϕ x3). Sato's Figure 3 shows wordline drivers (e.g., wordline drive circuits WD0-WD3 along with precharge transistors Q19~Q20 and reset transistors Q29~Q30)¹ coupled to respective wordlines (e.g., W0-W3) of memory array (e.g., M-ARY). Each of the wordline drivers (e.g., WD0-WD3) is coupled to part of the address input (bits ax2-axi) through the NAND gate decoding circuits, and to the rest of the address input (bits ax0-ax1) through the predecoder PDCR. Each wordline driver is also coupled to one of the clock outputs (ϕ x0- ϕ x3) as shown in Fig. 3.

¹ For simplicity Sato's wordline drivers are referred to by (WD0-WD3) throughout to avoid repeating the combination of Sato's wordline drive circuits WD0-WD3, precharge transistors Q19~Q20, and reset transistors Q29~Q30.



59. Annotated Fig.3 (below) of Sato shows Sato's X address decoder including structures meeting the limitations of the first and second logic of the '002 patent. Operations of Sato's first and second logic are described in detail below.



60. The annotations in Fig. 3 above show that the pre-decoder PDCR meets the limitation for the *first logic* because it receives both a timing (*clock*) signal and a portion of the memory address. PDCR decodes two bits of the memory address, ax0 and ax1. PDCR in Fig.3 receives timing signal ϕ ce while PDCR in Fig.1 does not, although the same decoding function is described for these embodiments:

The pre-decoder <u>PDCR decodes the lower 2-bit complementary</u> <u>internal address signals ax0 and ax1</u> supplied thereto from the X address buffer XADB and generates selection signals $\phi x0-\phi x3$. These selection signals $\phi x0-\phi x3$ are formed selectively in accordance with the complementary internal address signals ax0 and ax1. In other words, the selection signal $\phi x0$ is set to the high logic level when both the inversed internal address signals ax0 and ax1 are at the high logic level. Similarly, the selection signals $\phi x1$, $\phi x2$ and $\phi x3$ are set to the high logic level when both the non-inversed internal address signal ax0 and the inversed internal address signal ax1 are at the high logic level, when both the inversed internal address signal ax0 and non-inversed internal address signal ax1 are at the high logic level and when both the non-inversed internal address signal ax0 and non-inversed internal address signal ax1 are at the high logic level and when both the non-inversed internal address signals ax0 and ax1 are at the high logic level, respectively.

Sato at 5:25-42 (emphasis added).

61. The function of the timing signal input to PDCR in the third

embodiment is described as follows:

In FIG. 3, the X address decoder XDCR of the CMOS static RAM of this embodiment includes one pre-decoder <u>PDCR</u> and k+1 decoding NAND gate circuits NAG0-NAGk in the same way as in the foregoing embodiments. ...

In the X address decoder XDCR of this embodiment, the aforementioned <u>timing signal ϕce </u> (selection control signal) <u>is</u> <u>supplied to the pre-decoder PDCR</u>. Accordingly, the CMOS static RAM is brought into the selection state and the timing signal ϕce is set to the high logic level so that the output signal of the pre-decoder PDCR, that is, the selection signal $\phi x0-\phi x3$, is set selectively to the high logic level.

Sato at 9:44-59 (emphasis added).

62. Sato does not provide a diagram the internals of XDCR in Fig. 3, but

the text description above provides enough detail for a POSITA to understand that

it performs a function equivalent to four AND gates as I have drawn below. This

structure is also equivalent to how a POSITA would have understood the operation

of the '002 patent's conditional clock generator, as I described above in paragraphs 13-16.



63. Furthermore, Brown's digital logic textbook corroborates this

understanding. Brown describes the operation of a demultiplexer circuit that is the

same as my illustration above. See Brown, 314-315, Fig. 3.16. In reference to Fig.

3.16, which I have reproduced below, Brown describes:

The demultiplexer can be implemented using a decoder circuit. For example, the 2-to-4 decoder in Figure 6.16 can be used as a 1-to-4 demultiplexer. In this case the *En* input serves as the data input for the demultiplexer, and the *y*0 to *y*3 outputs are the data outputs. The valuation of w1w0 determines which of the outputs is set to the value of *En*. To see how the circuit works, consider the truth table in Figure 6.16*a*. When En = 0, all the outputs are set to 0, including the one selected by the valuation of w1w0. When En = 1, the valuation of w1w0 sets the appropriate output to 1.

Brown, 315 (emphasis added).

Brown's description also corresponds to the operations of Sato's PDCR. Like Brown's signals w0 and w1, the values of Sato's address signals (ax0 and ax1) select one of four outputs ($\phi x 0 - \phi x 3$) and force the non-selected outputs low. Like Brown's enable signal En, the value of timing signal ϕ ce is passed through to the selected output; when En (ϕ ce) is low, the selected output is low and when En (ϕ ce) is high, the selected output is high.



Clock signal

64 The operations of Sato's address decoder are coordinated by a timing signal. A POSITA would have viewed the function of the timing signal ϕ ce as similar to or equivalent to that of a clock signal because 1) "clock" is another name for a timing signal, 2) the Greek symbol phi (ϕ) is frequently used in the art to indicate clock signals, 3) this signal performs the same function as the clock signal in the '002 patent and 4) ϕ ce performs the same function as the clock signal in a clocked decoder such as that described by Bridges. See e.g., Sato, 1:10-11, 12:4-6; '002 patent, 3:28-62; Bridges, 3:1-4:24, Figure 1; Shin, 1:23-42 (referring to multiple clock signals with the Greek symbol phi (ϕ)). In addition, Sato states that his invention "can be applied widely to semiconductor memory devices having at least a clocked static type address decoder" and that "CMOS static RAMs including clocked static decoders are known in the art." Sato, 1:10-11, 12:4-6 (emphasis added). See background section at paragraph 35-39 for a discussion on the operation of clocked decoders.

65. A POSITA would have recognized that the function of Sato's timing signal ϕ ce and PDCR in the third embodiment of Sato as shown in Fig 3 closely matches the function of the Clock 118 signal and conditional clock generator 110 in the '002 patent figures and specification.

The conditional clock generator 110 receives a clock signal via the clock input 118 and selectively applies the clock signal to a

selected one of the clock outputs 124, 126, 128 and 130. In general, each clock output 124,126,128 and130 is coupled to each of the groups of wordline drivers 104 and 106 of the particular group of wordline drivers. In a particular embodiment, the conditional clock generator 110 may derive the clock outputs 124, 126, 128 and 130 from a single clock

'002 patent at 3:28-36.

Since only one of the four clock outputs 124, 126, 128 and 130 may be active at a time, only one of the four wordline drivers of the group of wordline drivers104 is in the dynamic <u>evaluation</u> <u>state</u> (e.g. a <u>clock signal is present</u>), while the other three remain in a static <u>precharge state</u> (such as a logic high state).

'002 patent at 3:57-62 (emphasis added).

66. In Sato, predecoder PDCR receives the ϕ ce clock signal. When ϕ ce is

low (the precharge state) all of the clock outputs $\phi x0-\phi x3$ are also forced low as is evident from the four AND gates in the internal structure of PDCR illustrated above. In the precharge state, each of the low $\phi x0-\phi x3$ clocks activates one of the reset P-channel MOSFETs Q29 ... Q30, causing all of the inverter inputs to be precharged up to Vcc (high) which in turn causes and all of the word lines W0-W3 to be pulled down to ground (low) by activating Qd2. When ϕ ce goes high (the evaluation state) one of the $\phi x0-\phi x3$ clocks is driven high to cause one of the capacitance cut N-channel MOSFETs Q19 ... Q20 to conduct, in turn allowing one of the precharged inverter inputs to be driven by the NAND decoder NAGO (which has also been activated during the evaluation phase by ϕ ce). Thus, a POSITA would have understood that the Sato ϕ ce timing signal is performing a similar function as Clock 118 in the '002 patent Figure 1, and that the Sato PDCR is performing a similar function of applying a clock signal to an output as conditional clock generator 110 in the '002 patent Figure 1.

67. Similarly, Sato's timing signal ϕ ce performs the same function as the clock in a clocked decoder (see Bridges Fig. 1) described above in paragraphs 36-39. In this case, the timing/clock signal precharges decoder output lines while low, then evaluates the decoder while high.

68. When used in a clocked decoder such as those described in the '002 patent, in Sato, and in Bridges, the timing/clock signal oscillates between the low and high state once to complete the selection process, requiring a clock cycle per access for each precharge plus evaluation cycle. A POSITA would have recognized that, when used for the row decoder of a memory circuit, if the clock line did not cycle each address change, multiple output word lines could be selected at once causing the circuit to malfunction. That is, if the timing signal ϕ ce did not oscillate during the wordline selection process the XDCR may enter a state in which two wordlines were activated simultaneously, which would cause errors in the data being read from or written to the memory array.

69. For instance, if a six bit memory address of 000000 were supplied to the XCDR at one time (with the last two bits 00 being the two bits ax0 and ax1) the PDCR would assert the ϕ x0 output when the timing signal goes high (*see* my

illustration in paragraphs 71 below). This would cause the transistor Q19 to turn on and permit a selection signal $\overline{S0}$ to be provided to wordline driver W0 to activate the wordline driver. If the timing signal does not cycle low before the next memory address is supplied, the input to wordline driver W0 will not be reset by transistor Q29 or transistor Qg1 if the bits ax0 and ax1 remain the same for the subsequent address. For example, if the subsequent address is 111100. In this case the output of PDCR would remain the same (e.g., $\phi x0$) because the bits ax0 and ax1 have not changed and the timing signal has not changed. Yet, a different decoding NAND gate circuit activates its selection signal (e.g., \overline{Sk} of NAND gate NAGk) in response to the change in address bits ax2-axi, resulting in two wordlines being active simultaneously.

Decoding a first portion of a memory address

70. The function of the Sato predecoder (PDCR) is to decode a first portion (ax0 and ax1) of the memory address. These two address bits are decoded into four outputs $\phi x0-\phi x3$, the well-known function of a 2:4 decoder. The four outputs are all low when timing signal ϕ ce is low, and when timing signal ϕ ce is high, a single output is high depending on which of the four combinations of the two address bits (00, 01, 10, 11) is present. Thus, when signal ϕ ce is high, one of the outputs $\phi x0 - \phi x3$ is high and the others are low. *See* paragraph 62-63 above for annotated diagrams of Sato's Fig. 3 and the internal structure of the PDCR.

<u>Applying a clock signal to a clock output/providing a clock signal to a</u> group of wordline drivers

71. Sato discloses a plurality of clock outputs which are the timing signals $\phi x0-\phi x3$ in the third embodiment. These are clock signals as indicated by their use of the Greek letter phi (ϕ) and the fact that each of the outputs $\phi x0-\phi x3$ follows the same low-to-high and high-to-low transitions as the input clock signal ϕ ce when that clock output is selected. The figure below shows an example in which ax0 and ax1 are both low.



72. The illustration shows that for the 00 case (ax0=ax1=0), ϕ x1- ϕ x3 are forced low because at least one input of those AND gates is low, and ϕ x0 will adopt the same state as input clock ϕ ce because the other two inputs of its AND gate are high. In other words, in the 00 case, output ϕ x0 is low when the input clock ϕ ce is low, and is high when input clock ϕ ce is high, and therefore ϕ ce is

applied to clock output $\phi x0$. Similarly, with the other three combinations of the two address lines, the input clock is applied to the corresponding output clock when that output is selected. Consequently, Sato's PDCR applies the timing signal ϕ ce to one of $\phi x0-\phi x3$ according to the logic levels of the address signals ax1 and ax1. Thus, the logic acts to *apply the clock signal to a selected clock output*. Further, because the input clock ϕ ce is applied to one of $\phi x0-\phi x3$ outputs, a POSITA would have also understood the outputs to be clock outputs.

Selected group of [a plurality of] wordline drivers

73. Note that the decoders of the '002 patent and Sato both have two separate selection operations – one to select the clock and another to select the group of wordline drivers. The *selected group of wordline drivers* may be different from the selection process used to determine the *selected clock output*.

74. Similarly, Sato shows groups of wordline drivers as shown in annotated Fig. 3 below.



75. Sato shows groups of wordline drivers, each group driving four wordlines, and each group receiving a shared address input from the partially decoded address bits ax2-axi. Exactly one of the NAND decoders NAG0-NAGk will match the address bits ax2-axi and drive the selected inverted S0...Sk output low. That group is the *selected group of a plurality of wordline drivers*.

[Clock outputs] associated with a selected group of wordline drivers

76. In annotated Sato Fig. 3 above, the selection of a single wordline within the group is done by the activation of one of the four clock outputs (ϕx 0- ϕx 3). In other words, those clock outputs are associated with a selected group of a plurality of wordline drivers.

Associated with the memory array

77. Sato's wordline drivers are connected to a memory array as indicated by the label "TO M-ARY" in Fig. 3.

Word line drive circuits WD=WDm are also disposed in such a manner as to correspond to the word lines W0-Wm of the <u>memory array</u> M-ARY, respectively.

Sato at 9:48-51 (emphasis added).

78. This quotation, in conjunction with Fig. 3, shows that the wordline

driver circuits are associated with the memory array.

Decoding a second portion of a memory address

79. As illustrated in annotated Fig. 3 of Sato above, NAND gates NAG0-

NAGk decode a second portion of a memory address. As is well known in the art,

a NAND gate receives inputs and generates a low output when all inputs are high

and outputs a high output if one or more of the inputs are low. For example,

NAG0 receives the complement of address lines ax2-axi, and when the

complemented addresses are all high (indicating that the non-complemented ax2-

axi are all low), group 0 wordline drivers are selected with active-low selection
signal S0. Each of the other NAND gates (not shown) is connected to a different combination of the true and complemented address lines ax2-axi, and selects the appropriate output for that combination. This collection of NAND gates implements the well-known function of a decoder. The notation in Sato (0 through k) allows for decoders of different sizes for memories with different numbers of address bits. For instance, with four address lines connected to NAG0-NAG15, the address inputs are ax2-ax5 and the sixteen NAND gates implement a 4-to-16 decoder. Address lines ax2-axi to this decoder are *a second portion of the memory address* (address line ax0-ax1).

Activating a particular wordline driver

80. The second logic in Sato acts to selectively activate a particular wordline as shown in the following annotated Fig. 3.



81. In this example, a *particular wordline* W3 is activated when NAG0 selects group0 because ax2-axi are all low (*according to the second portion of the memory address*) whenever clock driver ϕ x3 is selected (based on high values of ax0 and ax1). Other addresses similarly cause other particular wordlines to be activated.

82. Sato describes the details of the NAND decoder circuit in its description of Fig. 1. Sato states that "the output signal of the NAND gate circuit NAG0" is asserted "when all the inversed internal address signals $\overline{ax}2-\overline{ax}i$ are at the high logic level." Sato, 5:66-6:4. "In other words, the selection signal $\overline{S0}$ is at the low logic level when . . . any one of the word lines W0 through W3 is designated by the X address signal AX0-AXi²." Sato, 6:4-8. "The output signals of the NAND gate circuits NAG1-NAGk-1, that is, the inversed selection signals $\overline{S1}-\overline{Sk}-1$, which are not shown in the drawing, are generated by the same logic as described above." Sato, 6:17-21. Thus, together all of the k+1 decoding NAND gate circuits receive and decode a second portion of the memory address (ax2-axi).

83. As shown in the annotated comparison between Fig. 3 of Sato with Fig. 3 of the '002 patent below, even Sato's wordline driver activation circuitry is nearly identical to that of the '002 patent. In both circuits a common address input (Sato's selection signal $\overline{S0}$ and the '002 patent's shared address [input] line 304) is provided to a source of an N-channel transistor (compare transistors Q19 and Mn0). Both N-channel transistors (Q19/Mn0) receive a clock signal (ϕ x0 and CLK<0>) at their respective gates and provide an output signal through their

 $^{^{2}}$ Sato refers the external address lines in upper case (e.g. AX0) and the internal copies of the address lines in lower case (e.g. ax0). See Fig 4, showing both the internal and external addresses.

respective drains to the input of a wordline driver (WD0 and 322). The inputs of both wordline drivers (WD0 and 322) are connected to drain terminals of respective P-channel reset transistors (Q29 and Mp0). The sources of both reset transistors (Q29 and Mp0) are connected to a high voltage supply and the gates of both reset transistors are connected to the clock outputs (ϕ x0 and CLK<0>). Finally, both wordline drivers (WD0 and 322) are inverter circuits.



Conditional Clock Generator

84. The predecoder PDCR of Sato is a *conditional clock generator* because it conditionally generates a clock to one output (when that output is selected). See paragraphs 14, 62-63 and 71-72, annotated Fig. 3 and my PDCR diagrams. Furthermore, as described above in paragraphs 14, 60-63 and 71-72, the selected clock output is determined by address inputs to the PDCR, namely (ax0 and ax1).

Activating one clock output at a time

85. As described above in paragraphs 64-69, the four outputs of PDCR are *four conditional clock outputs* (ϕ x0- ϕ x3). Furthermore, as above in paragraphs 62-63 and 71-72, decoder PDCR makes only one of the *conditional clock outputs* (ϕ x0- ϕ x3) active at a time. Finally, Sato's PDCR applies the one selected clock output (one of ϕ x0- ϕ x3) as the selected clock output.

A common/shared address input for multiple wordline drivers

86. As discussed above in paragraphs 73-75, Sato discloses four wordline drivers per group (e.g. WD0-WD3) and each of the four wordlines is associated with a respective wordline of the memory array (e.g. W0-W3).

87. Claims 6, 24 and 35 include the term "common address input," claims 10 26 and 35 include the term "shared address input," and claims 14 and 28 include the term "shared address line."

the decoded output of the four-to-sixteen bit memory address decoder 108 may be utilized via a logical AND operation to

selectively activate a wordline driver of the group of wordline drivers 104, for example.

'002 at 4:5-9.

88. The term "common address input" is used in the '002 patent to

describe the partially decoded memory address lines 120 and 122 in Fig. 1 and Fig

3 and this line is generated by the 4-to-16 decoder 108.

the decoded output of the four-to-sixteen bit memory address decoder 108 may be utilized via a logical AND operation to selectively activate a wordline driver of the group of wordline drivers 104, for example.

'002 patent at 4:5-9.

In general, each group of wordline drivers, such as the group of wordline drivers 104 may share a <u>common</u> partially decoded <u>address input</u>, such as the partially decoded address line (0) 120 for the group of wordline drivers 104, reducing layout area usage and layout complexity.

'002 patent at 3:46-50.

89. In Fig. 3, address 120 (common address input) goes to inverter 302 to produce line 304, described in the specification as "shared address line 304," ('002 patent at 5:2) and "shared address input 304." '002 patent at 5:29-31.

90. The presence of inverter 302 has no particular significance in either the specification or the claims and merely produces an active low signal from an active high signal. I find that all three terms, "common address input," "shared address input" and "shared address line" have no patentable distinction and should be construed as "a signal indicating a match of a part of a memory address." 91. Annotated Fig 3 of Sato (below) shows that the wordline drivers (e.g. WD0-WD3) all share a common address input signal (selection signal $\overline{S0}$). "In other words, the selection signal $\overline{S0}$ is at the low logic level when . . . any one of the word lines W0 through W3 is designated by the X <u>address signal</u> AX0-AXi." Sato, 6:4-8 (emphasis added).



Means for decoding a first portion of a memory address

92. Sato discloses *means for decoding a first portion of a memory address of a memory array* as recited in claim 11.

93. As I explained above in paragraphs 60-63 and 70, Sato's PDCR decodes a first portion of a memory address for a memory array. Furthermore, it is my opinion that a POSITA would have considered Sato's PDCR to include the same or equivalent structure as the decoder described in the '002 patent for performing these functions.

Means for providing a clock signal

94. Sato discloses *selectively providing a clock signal to a selected group of wordline drivers based on the first portion of the [a] memory address* as recited in claims 11 and 27.

95. As I explained above in paragraphs 60-63 and 71-72, Sato's PDCR selectively provides a clock signal (ϕ ce) to different wordline drivers based on the first two bits (ax0 and ax1) of a memory address. Furthermore, it is my opinion that a POSITA would have considered Sato's PDCR to include the same or equivalent structure as the "conditional clock generator" described in the '002 patent for performing these functions.

96. Note that the PDCR of Sato performs both the decoding and conditional clock generation functions of the '002 patent. These functions could

be performed in a single stage as shown in my diagram (with 3-input AND gates). Alternatively, the decoding and conditional clock generation could be performed in separate stages of logic. The first stage, a two-to-four decoder would connect to the second stage comprising a set of AND gates (acting as the conditional clock generator) which would AND each of the decoder outputs with the clock. The single-stage and dual-stage structures are equivalent and either one meets the claim limitations.

Means for decoding a second portion of a memory address

97. Sato discloses *means for decoding a second portion of the memory address* as recited in claim 11.

98. As I explained above in paragraph 79, Sato's decoding NAND gate circuits decode a second portion (ax2-axi) of a memory address. Furthermore, it is my opinion that a POSITA would have considered Sato's decoding NAND gate circuits (NG0-NGk) to include the same or equivalent structure as the address decoder 108 described in the '002 patent for performing these functions.

Means for activating a particular wordline driver

99. Sato discloses means for activating a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address as recited in claims 11 and 27.

100. As I explained above in paragraphs 80-83, Sato's decoding NAND gate circuits activate a particular wordline driver in a group based on address signals ax2-axi by generating an appropriate output signal (\overline{SO} - \overline{Sk}) which is applied to the appropriate word line driver. Furthermore, it is my opinion that a POSITA would have considered Sato's decoding NAND gate circuits (NG0-NGk) to include the same or equivalent structure as the address decoder 108 described in the '002 patent for performing these functions.

<u>Means for applying the second portion of the memory address to a</u> <u>shared address line</u>

101. Sato discloses means for applying the second portion of the memory address to a shared address line as recited in claim 14.

102. As I explained above in paragraphs 86-91, Sato's decoding NAND gates apply a second portion of the memory address (e.g., selection signal \overline{SO}) to an address line that is shared by four wordline drivers. Furthermore, it is my opinion that a POSITA would have considered Sato's decoding NAND gate circuits (NG0-NGk) to include the same or equivalent structure as the address decoder 108" described in the '002 patent for performing these functions. A POSITA would further have recognized that the output of Sato's decoding NAND gate circuits apply the second portion of the memory address (e.g., selection signal \overline{SO}) to an address line that is shared by four wordline drivers.

Active evaluation and precharge states

103. The wordline drivers in Sato are in a static precharge state when timing signal ϕ ce is low and are in an active evaluation state when ϕ ce is high. The two annotated versions of Sato Fig. 3 below show the operation of these states.



104. When ϕ ce is low, predecoder PDCR drives all four outputs $\phi x0-\phi x3$ low. Each of these outputs activates one of the reset P-channel MOSFETs Q29...30, pulling all wordline driver inputs up to Vcc (logic 1) and the wordlines W0... Wm to ground (logic 0), These lines will remain in this *static precharge*

state until clock ϕ ce becomes high. The annotated diagram shows the inputs to wordline drivers WD0-WD3 precharged to a logic "1" level and the wordlines precharged to a logic "0" level.



105. Once the wordlines have been precharged, ϕ ce goes from low to high to perform the evaluation phase as shown in the annotated Fig. 3 above. At that time, exactly one wordline is selected by one of the capacitance cut MOSFETs Q19-Q20 which will have both a high gate signal from the selected clock, and a low source input from the NAND gate decoder NAGi. For example, the annotated figure shows W3 as the selected wordline and Q20 pulls the input to the WD3 inverter low because it is an N-channel FET with its gate high and source low, causing it to conduct and pull its drain low. All other wordlines remain at the precharged state because Q19, etc., do not have a high gate signals and therefore do not conduct to discharge their wordline inputs. During the evaluation phase, a single wordline input is pulled low and its wordline is driven high while all other wordline inputs remain precharged high with their wordlines driven low.

State of the Wordline Driver

106. As detailed in the previous section, the states of the wordline driver (static precharge or active evaluation) are determined by the particular clock signal (one of $\phi x 0 \cdot \phi x 3$) received by the driver. When the clock signal ϕ ce is low, all wordline drivers are precharged, and when ϕ ce is high, the clock is selectively applied to one of the clock signals $\phi x 0 \cdot \phi x 3$. The clock received by a wordline driver determines whether that driver, or another driver in the group, enters the evaluation state.

OVERVIEW OF ASANO

107. Fig. 2 of Asano is reproduced below:



108. While Fig. 2 of Asano shows key elements of the '002 patent, there is more information disclosed in the text of Asano. Below, I have redrawn Asano Fig. 2 with added details from the Asano specification. These redrawn figures will be used to identify the parts of the Asano disclosure that correspond to the claim elements of the '002 patent.



109. The redrawn Fig. 2 shows additional detail of the address lines, predecoder, final decoder and the replication of the groups of wordline drivers.

For each addition to the original diagram, I have identified where in the specification that additional detail is disclosed.

110. The six address lines shown in the redrawn Fig. 2 have been numbered [5:0] to facilitate discussion, but the actual bit numbers are not directly relevant to the '002 patent claims. Asano describes the fields from the decoders as follows:

Typically, the address is <u>6 bits long</u>, and from those 6 bits, the predecoder derives a wordline enable signal and two wordline select signals in step 304, an X wordline select signal and a Y wordline select signal. The <u>X wordline select signal is 8 bits long</u> and is output to the final decoder 204 through a second communication channel 218. The <u>Y wordline select signal</u> is output to the final decoder 204 through a third communication channel 220 and <u>is 4 bits long</u>.

Asano at [0016] (emphasis added).

111. From the description above, a POSITA would have understood that if the decoded X wordline select signal is 8 bits long, it would come from decoding three bits of the address field (e.g. bits 4:2) with a 3-to-8 decoder as shown in the predecoder of redrawn Fig. 2. Similarly, if the Y wordline select signal is 4 bits long, it would come from a 2-to-4 decoder connected to two address bits (e.g. bits 1:0) as shown in the diagram.

112. The final decoder receives the X and Y outputs of the predecoder and generates a single output when both an X and Y input are active. A POSITA

would have understood that an AND gate serves this purpose and the final decoder comprises one AND gate for each pair of X and Y outputs of the predecoder as shown in the redrawn diagram. Note that although the redrawn diagram shows AND gates, it is well known that an equivalent AND function can be implemented in other ways, such as with a NAND gate followed by an inverter. Asano also points out that other gate types could be used:

Also, AND gates can be replaced by NAND gates, NOR gates, or OR gates depending upon the circuit type which receives the wordlines.

Asano at [0018].

113. The LCBs in the redrawn diagram are shown as AND gates because they perform an AND function by passing the clock signal through (when the enable is high) and forcing the output low (when the enable is low). The redrawn diagram uses the AND symbol instead of the buffer symbol shown in the original Fig. 2 to make this function of the LCB more explicit.

114. The enable signals to the LCBs are shown in Fig. 2 as coming from the predecoder. Asano explains this function as follows:

The first AND gate 212 receives a clocking signal from the first LCB 208 through the fifth communication channel 228, while the second AND gate 236 receives a clocking signal from the second LCB 234 through the sixth communication channel 240. Depending on the most significant bit of the address signal that is input into the predecoder 202, either the first AND gate 212or the second AND gate 236 is selected. Asano at [0019] (emphasis added).

115. This "most significant bit" of the memory address is shown as bit 5 in the diagram and it selects one LCB when that bit is low and the other LCB when it is high. Driving one of two outputs high based on an input bit is the well-known function of a 1-to-2 decoder as shown in the redrawn Fig. 2. Thus, all six input bits have been accounted for, with bits [4:2] selecting the X output, bits [1:0] selecting the Y output, and the most significant bit [5] selecting only one of the LCBs. Asano shows that each LCB receives a selection signal (from the predecoder) and a CLK signal as input. Thus, the CLK signal will be propagated by only the LCB that receives an active selection signal from the predecoder.

116. The redrawn diagram also shows how groups of drivers are replicated to produce all 64 wordlines. Each group comprises two LCBs along with the latch of the final decoder output and 32 groups drive the 64 word lines.

117. The following diagram takes the redrawn Fig. 2 and further extends it by using two bits to select the LCB, an option described by Asano:

Additionally, for the purposes of illustration, 1 bit has been utilized for LCB selections. It is possible to have <u>2 or more LCB selections up to N bits</u>.

Asano at [0021] (emphasis added).



118. In this diagram, the Y decoder is now a 1-to-2 decoder instead of a 2to 4 decoder, freeing up a bit to be used for LCB selection. The LCB selection uses the two most significant bits [5:4] to select one of four LCBs. Note that the extra bit could have instead been taken from the X decoder, making all three decoders (X, Y and LCB) 2-to-4 decoders. The exact arrangement of the decoders inside the predecoder is not important because that structure is not part of the '002 claims and a POSITA would have understood how to make simple design choices to implement the predecoder in different ways.



119. As indicated in the figure above, Asano includes an address input, a plurality of clock outputs and a group of wordline drivers coupled to a wordline of a memory array. Furthermore, each wordline driver (AND gate output) of the group of wordline drivers (highlighted in blue) is coupled to the address input

(output of the final decoder) and coupled to a respective clock output of the plurality of clock outputs (to one of the LCB outputs). Although Asano appears to label two AND gates as a wordline driver, a POSITA would have understood that each wordline driver (AND gate output) drives only one wordline. Further, Asano explains that only one of the wordlines WL is driven at a time when "either the first AND gate 212 or the second AND gate 236 is selected, wherein the clocking signal is ANDed with the output of the latch 210 [which is the output of the final decoder]." Asano, [0019], Figure 2. The AND operation only produces a non-zero output when both inputs to the AND gate are asserted. Thus, because Asano's CLK signal is propagated by only the LCB that receives an active selection signal from the predecoder and the final decoder supplies only a single wordline enable signal to one set of AND gates, only one of the AND gates (e.g., wordline drivers) will produce a non-zero output. See supra ¶¶111-115; see also Asano, [0017]-[0019], claim 17, Figure 2. Thus, a POSITA would have understood that the output of each AND gate drives one wordline, and that only one wordline would be enabled at a time.

120. The following detailed analysis uses the redrawn diagram with four LCBs per group to clearly show how Asano discloses the elements of the '002 patent claims.

OVERVIEW OF ITOH

121. Itoh provides additional details about decoding circuits, predecoding circuits and wordline drivers. A POSITA designing a memory circuit according to Asano, would have naturally turned to a textbook such as Itoh's "VLSI Memory Chip Design," for details on memory design techniques for integrated circuits.

122. Itoh shows the circuit design of a specific predecoder circuit suitable for wordline address decoders in memory chips. A POSITA would have looked to such circuits to determine how the internal circuitry for Asano's predecoder and decoder would be built. Furthermore, Itoh's predecoder circuits corresponds to that shown in my redrawn versions of Asano's Fig. 2 above and represent well-known predecoder circuit designs.

123. Itoh shows the design of both a 2:4 bit predecoder (Fig. 3.46(b)) and a 3:8 bit predecoder (Fig. 3.46(c)). Itoh's predecoder design is a well-known design that uses NAND gates to generate a selection signal (e.g., a logic low) on one of 4 output lines (for the 2:4 predecoder) or on one of 8 output lines (for the 3:8 decoder) when a particular input address is received. Further, as I noted above (paragraph 112) NAND gate and AND gate decoders are interchangeable because an AND gate is simply a NAND gate plus an inverter. The predecoders include a series of NAND gates each of which is connected to a unique combination of address inputs or complements of the address inputs in a manner similar to the

diagram I presented in my explanation of Sato's predecoder above. Each combination of address signals and complementary address signals connected to a NAND gate represents a unique memory address. Only one of the NAND gates will provide a selection signal (logic low) for each combination of possible address bits while the other NAND gates in the predecoder remain un-selected (e.g., provide a logic high output).



124. I redrew Asano's Fig. 2 above using AND gates (for simplicity), however a NAND gate predecoder would operate identically to the redrawn circuit above by using a corresponding NAND final decoder (as shown below in the annotated figure showing Asano's predecoder 202 implemented using Itoh's predecoder circuitry as depicted in Itoh Figure 3.46).



125. While clocked decoder circuits were already well-known before the '002 critical date, Itoh shows the circuit design of a specific clocked decoder circuit suitable for word line decoders in memory chips. Such a circuit could be implemented in Asano to give it the known benefits of clocked decoders for reducing power consumption of the integrated circuit.



126. Itoh shows the design of the clock word line decoder in Fig. 3.48:

127. The Itoh clocked row decoder that functions as follows. In Fig. 3.48(a), lines Xj and Xk come from a predecoder, such as those illustrated in Fig. 3.46. Note that the predecoder outputs are called x/y in Asano and j/k in Itoh, but both serve the same function in indicating a match from decoding part of the memory address. Xj and Xk connect to N-channel MOSFETs connected as a NAND circuit, which pulls the output low when both Xj and Xk are high. Only one NAND circuit is shown, there would be one NAND gate for every group of four drivers, and this NAND serves the same function as the AND gates in the final decoder of Asano. An inverter follows the NAND to generate the complement of the decoded signal (equal to the AND of the inputs). The true and complement signals connect to a set of 8 transistors configured as 4 CMOS inverters driving word lines WL0-WL3.

128. The word lines are driven high when the predecoder outputs Xj and Xk are high, indicating an address match whenever the corresponding RX line is also high. The RX lines serve the same function as the conditional clock outputs from the LCBs of Asano. Itoh describes the predecoder and RX signals as follows:

Address signals <u>Xj</u> and <u>Xk</u> are inputted from <u>2-bit</u> <u>predecoders</u> to the decoder. Each of the four word drivers selected by the decoder is selectively driven by decoded <u>select lines RX (RX_0 - RX_3)</u>, enabling the corresponding word line to be driven

Itoh at p. 149 (emphasis added).

129. Fig. 3.48(b) shows how the RX lines are driven. The clock input, ϕ_B passes through the 3-input NAND gate for the RX driver with the right combination of the two a0-a1 address lines. The output of the NAND gate connects to an inverter and then goes through two inversion stages before driving the RX line. Thus, only one RX line is driven high while the others are driven low. Itoh describes this logic as follows:

When BL addresses have been valid after starting activation with RP: L, a <u>clock $\phi_{\rm B}$ generated by the RAS</u> buffer is applied, so that only one selected RX line driven at a high enough voltage, boosted by CB.

Itoh at p. 149 (emphasis added).

130. This structure of Itoh fits directly into the 4-LCB version of Asano and a POSITA could easily combine the teachings of Itoh with those of Asano and obtain predictable results. For instance, the use of standard predecoder, decoder, and wordline driver circuits as disclosed by Itoh to implement any of Asano's block diagram circuit components would have been well within the skill level of a POSITA. The resulting structure has the same predecoding and decoding structure as the '002 patent.

DETAILED ANALYSIS OF ASANO AND ITOH

131. As shown in the 4-LCB version of Fig. 2 below, Asano has a 2:4
decoder fed from memory address bits [5:4] (*a first portion of a memory address*).
The wordlines connect to the "64 WL ARRAY" (*memory array*). The outputs of

this decoder are connected to AND gates connected to the CLK signal (*to receive a clock signal*).



<u>Applying a clock signal to a clock output/providing a clock signal to a</u> group of wordline drivers

132. As indicated in the annotated figure above, a POSITA would have understood that the AND gates connected to the 2-to-4 decoder and CLK function to apply the CLK signal to one of the outputs of the AND gates as designated by address bits [5:4]. The diagram also shows a POSITA that each of the plurality of wordline drivers is associated with a wordline of the memory array (WL0-WL63).

Selected group of [a plurality of] wordline drivers

133. Note that the decoders of the '002 patent and Asano both have two separate selection operations – one to select the clock and another to select the group of wordline drivers. The selected group of wordline drivers may be different from the selection process used to determine the selected clock output. A POSITA would have considered the selected group of wordline drivers in Asano as the group selected by the final decoder.

Activating a particular wordline driver

134. A POSITA would have understood that the output of the Asano final decoder activates a particular wordline driver of the selected group of wordline drivers because each output is connected to a different group and only one of those outputs is high at a time (the standard function of a decoder). The active group receives four clock outputs but only one clock is active at a time. Only a single

particular wordline driver is activated because only one driver in the selected group also has an active clock.

Conditional Clock Generator

135. The annotated figure above identifies the conditional clock generator of Asano as the four LCBs (shown as four AND gates) that conditionally allow only one clock to pass through. That clock is the *selected clock output* of the *conditional clock generator*.

A common/shared address input for multiple wordline drivers

136. The annotated diagram below shows how a POSITA would have understood Asano's disclosure as presenting a shared address input to groups of wordline drivers.



137. The outputs of the final decoder each communicate the shared address to a group of wordline drivers. This drawing shows four wordlines per group

wherein the four wordline drivers share a common address input. Also, as is evident from the drawing, each of the four wordline drivers is associated with a respective wordline of the memory array.

Means for decoding a first portion of a memory address

138. Asano in view of Itoh discloses means for decoding a first portion of a memory address of a memory array as recited in claim 11.

139. As I explained above in paragraphs 108-118 and 131, the decoder connected to ADDRESS[5:4] decodes a first portion of a memory address for a memory array. Furthermore, it is my opinion a POSITA would have considered Asano's decoding logic (to enable the LCBs) to include the same or equivalent structure as the "decoder" described in the '002 patent for performing these functions.

140. Itoh's Fig. 3.48(b), with bits a0 and a1and their complements connected to a NAND decoder, also shows the same or equivalent structure as the "decoder" described in the '002 patent for performing these functions.

Means for providing a clock signal

141. Asano in view of Itoh discloses *selectively providing a clock signal to a selected group of wordline drivers based on the first portion of the [a] memory address* as recited in claims 11 and 27.

142. As I explained above in paragraphs 108-118 and 132, Asano's LCBs selectively provide a clock signal to different wordline drivers based on two bits ([5:4]) of a memory address. Furthermore, it is my opinion a POSITA would have considered Asano's LCBs to include the same or equivalent structure as the "conditional clock generator" described in the '002 patent for performing these functions.

143. Itoh's Fig. 3.48(b), with bits a0 and a1and their complements connected to a NAND decoder, selectively applies clock signal ϕ_B to RX0-RX3 which are provided to the groups of wordline drivers as shown in Fig. 3.48(a). Thus, Itoh also shows the same or equivalent structure as the "decoder" described in the '002 patent for performing these functions.

Means for decoding a second portion of a memory address

144. Asano in view of Itoh discloses *means for decoding a second portion of the memory address* as recited in claim 11.

145. As I explained above in paragraphs 108-120, Asano's predecoder plus final decoder decode a second portion ([3:0]) of a memory address. Furthermore, it is my opinion a POSITA would have considered Asano's decoders to include the same or equivalent structure as the "memory address decoder" described in the '002 patent for performing these functions.

146. Itoh's Fig. 3.48(a) also shows the outputs of 2-bit predecoders, Xj and Xk, connected to transistors configured as a NAND decoder. Thus, Itoh also shows the same or equivalent structure as the "address decoder108" described in the '002 patent for performing these functions.

Means for activating a particular wordline driver

147. Asano in view of Itoh discloses *means for activating a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address* as recited in claims 11 and 27.

148. As I explained above in paragraphs 108-120 and 134, Asano's final decoder activates a particular wordline driver in a group based on address signals [3:0] by generating an appropriate output signal, which is applied to the appropriate word line driver. Furthermore, it is my opinion a POSITA would have considered Asano's final decoder to include the same or equivalent structure as the "address decoder 108" described in the '002 patent for performing these functions.

149. Itoh's Fig. 3.48(a) also shows the outputs of 2-bit predecoders, Xj and Xk, connected to transistors configured as a NAND decoder. Thus, Itoh also shows the same or equivalent structure as the "address decoder 108" described in the '002 patent for performing these functions.

Means for applying the second portion of the memory address to a shared address line

150. Asano in view of Itoh discloses *means for applying the second portion of the memory address to a shared address line* as recited in claim 14.

151. As I explained above in paragraphs 108-120 and 136-137, Asano's final decoder applies a second portion of the memory address to an address line that is shared by four wordline drivers. Furthermore, it is my opinion a POSITA would have considered Asano's predecoder plus final decoder to include the same or equivalent structure as the "address decoder 108" described in the '002 patent for performing these functions.

152. Itoh's Fig. 3.48(a) also shows the outputs of 2-bit predecoders, Xj and Xk, connected to transistors configured as a NAND decoder. Thus, Itoh also shows the same or equivalent structure as the "address decoder108" described in the '002 patent for performing these functions

LEGAL PRINCIPLES

Anticipation

153. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed limitations, it anticipates.
154. I have been informed that a claim is invalid under 35 U.S.C. § 102(a) if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the applicant's invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(b) if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (critical date). And a claim is invalid, as I have been informed, under 35 U.S.C. § 102(e), if an invention described by that claim was described in a U.S. patent granted on an application for a patent by another that was filed in the U.S. before the date of invention for such a claim.

<u>Obviousness</u>

155. I have been informed that a patent claim is invalid as "obvious" under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a POSITA, taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called "secondary considerations" of nonobviousness, which include: (i) "long felt need" for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) "copying" of the claimed invention by others. For purposes of my analysis above and because I know of no indication from the

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patent owner or others to the contrary, I have applied a date of October 10, 2006, as the date of invention in my obviousness analyses, although in many cases the same analysis would hold true even at an earlier time than October 10, 2006.

156. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason to modify the single prior art reference, or combine two or more references, in order to achieve the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference or references themselves, the knowledge or "common sense" of one skilled in the art, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

ADDITIONAL REMARKS

157. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

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158. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Dated: 6/11/18 By: Much hit Robert W. Horst, PH.D.