

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Jentsung Lin
U.S. Patent No.: 7,693,002 Attorney Docket No.:
Issue Date: April 6, 2010
Appl. Serial No.: 11/548,132
Filing Date: October 10, 2006
Title: DYNAMIC WORD LINE DRIVERS AND DECODERS FOR
MEMORY ARRAYS

DECLARATION OF Robert W. Horst, Ph.D.

I, Robert W. Horst, Ph.D., of San Jose, CA, declare that:

I. Introduction.

1. I summarized my relevant knowledge and experience in my first Declaration (APPLE-1003). In writing this Second Declaration, I have considered the following: my own knowledge and experience, including my work experience in the fields of memory systems and circuit design and my experience in working with others involved in those fields. In addition, I have analyzed the following publications and materials, in addition to other materials I cite herein and in my first declaration: Patent Owner's Response to the IPR Petition

- Dr. Massoud Pedram's Declaration (Ex. 2001)
- The IEEE Dictionary (Ex. 2002 and APPLE-1014)
- Itoh (additional portions) (Ex. 2003)
- Horst Deposition Transcript (Ex. 2005)
- The Modern Dictionary of Electronics (APPLE-1015)

- U.S. Patent No. 4,922,461 (“Hayakawa”) (APPLE-1016)
- M. Pedram. “Design technologies for Low Power VLSI,” in *Encyclopedia of Computer Science and Technology*, Marcel Dekker, Editors: A Kent, J. G. Williams, and C. M. Hall, vol. 36, 1997, pages 73-95 (APPLE-1017)
- N. Mohyuddin, K. Patel, and M. Pedram. “Deterministic clock gating to eliminate wasteful activity in out-of-order superscalar processors due to wrong-path instructions,” *Proc. of Int’l Conf. on Computer De-sign*, Oct. 2009, pages 166-172 (APPLE-1018)
- Pedram Deposition Transcript (APPLE-1019).

II. A POSITA would not have limited the interpretation of “clock signal” to include only periodic clock signals

A. A broad plain and ordinary meaning for “clock signal” should be used

3. A POSITA would not have considered a periodic clock signal to be the broadest reasonable interpretation (BRI) of “clock signal” as used in the claims of the ’002 patent. There is no indication in the ’002 patent itself that would have led a POSITA to adopt such a restrictive interpretation because there is no explicit definition, waveform, or circuit in the ’002 Patent defining or suggesting such a narrow definition.

4. Instead of using the BRI for “clock signal,” Dr. Pedram adopts a restrictive definition inconsistent with the way “clock signal” is used in many systems, patents and textbooks. He defines “clock signal” as follows:

The term “clock signal,” as recited in each of the independent claims of the '002 patent, should be interpreted to mean “a **periodic signal** used for synchronization.” This interpretation is consistent with the plain and ordinary meaning of the term as understood by the POSA.

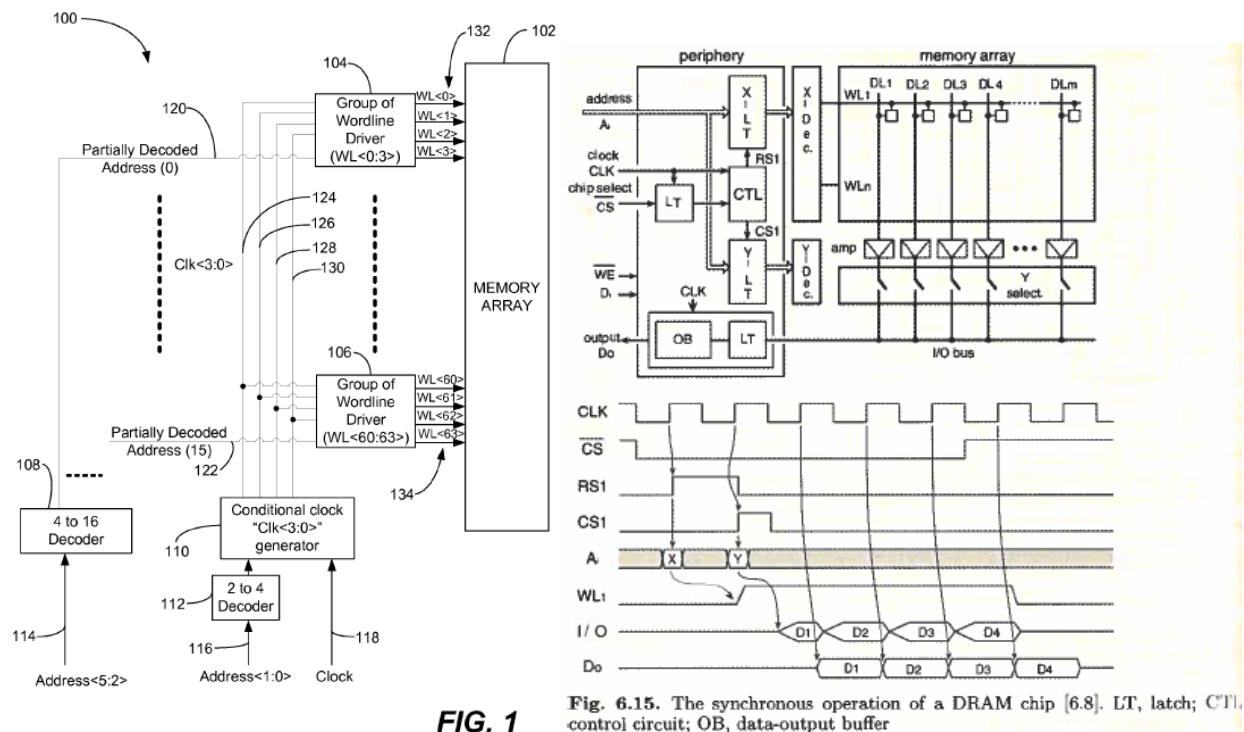
Pedram Decl. at ¶53, emphasis added.

it is my opinion that a POSA looking at this patent would understand the clock to be a **periodic signal** of fixed frequency used for synchronization purposes in the context of this memory system

Pedram Depo., p. 78, emphasis added.

5. Dr. Pedram’s definition appears to be based on his assumption that the '002 Patent is directed only to synchronous memory systems. I disagree because I find no such restriction in the specification or drawings of the '002 Patent. Dr. Pedram’s opinion is based on an absence in the depicted embodiments of the '002 patent of any timing circuitry he states would be required in an asynchronous system. However, Dr. Pedram acknowledged during his deposition that the figures in the '002 patent omit many necessary components of any memory system, such as column decoders (44:17-48:1), synchronous memory control logic (54:8-60:7), and clock drivers (40:10-20). Dr. Pedram’s exemplary synchronous memory

system, as depicted in Itoh, shows many circuit components that are not depicted in the figures of the '002 patent. The figures in the '002 patent depict only a specific portion of a memory system (e.g., a row address decoder), and the absence of any one circuit component from the figures does not indicate to a POSITA that the circuit component must be absent from the entire memory system. As seen below by the side-by-side comparison of '002 patent's Fig. 1 with Itoh's Fig. 6.15, the '002 patent does not show any control logic or other circuitry associated with either synchronous or asynchronous memory systems, but only that necessary to explain the operation of its row address decoder.



6. In the embodiment in Fig. 1 of the '002 patent, the clock input could be supplied with any type of clock signal—e.g., a periodic clock signal, a non-

periodic gated clock signal, a non-periodic clock signal derived from a periodic clock (e.g., RS1 as shown in Itoh's synchronous clock system), or another type of non-periodic clock signal—without adversely affecting its row decoding functionality. Similarly, the clock signal supplied to the Sato and Asano prior art combinations could be periodic or non-periodic while implementing the same row decoding functionality as the '002 Patent.

7. Dr. Pedram states that his definition is the broadest reasonable interpretation based on the definition of “clock signal” from an IEEE dictionary. Ex. 2002 and APPLE-1014. The portion of the IEEE dictionary cited in Dr. Pedram's declaration defines “clock signal” as “[a] periodic signal used for synchronizing events,” but this partial quotation omits the part of the definition that says “*Synonyms*: clock pulse; timing pulse.” Many systems and devices have clock pulses and other timing signals that are not periodic.

8. Also, Dr. Pedram's declaration omits alternate definitions for “clock” in the same IEEE dictionary. One of the alternate definitions of “clock” is as follows:

(2) A signal, the transitions of which (between the low and high logic level [or vice versa]) are used to indicate when a stored-state device, such as a flip-flop or latch, may perform an operation.

APPLE-1014 at 4.

9. As would be well-known to a POSITA and detailed in references below, many devices include flip-flops and latches are clocked by non-periodic clock signals. Thus, this IEEE definition of “clock” is broader than the narrow definition of “clock signal” given by Dr. Pedram.

10. The Modern Dictionary of Electronics also includes two broad definitions of “clock”:

1. A pulse generator or **signal waveform used to achieve synchronization of the timing of switching circuits** and the memory in a digital computer system”
...
4. **A strobe signal** that activates a certain **sequence of operations.**”

APPLE-1015, 3-4.

11. These definitions similarly are not restricted to periodic signals and are broader than Dr. Pedram’s proposed definitions. If anything, a commonality of these definitions is synchronization, not periodicity.

B. The ’002 Patent uses “clock” for gated clocks that are not periodic

12. The ’002 patent itself uses “clock” and “clock signal” to refer to signals that are not periodic. In particular, the outputs of the conditional clock generator are referred to as clocks:

The conditional clock generator may receive a clock input, such as the clock input 118 in FIG.1, and may selectively **apply the clock signal to a selected clock**, such as one of the **clocks 124, 126, 128 and 130** in FIGS.1 and 3. The

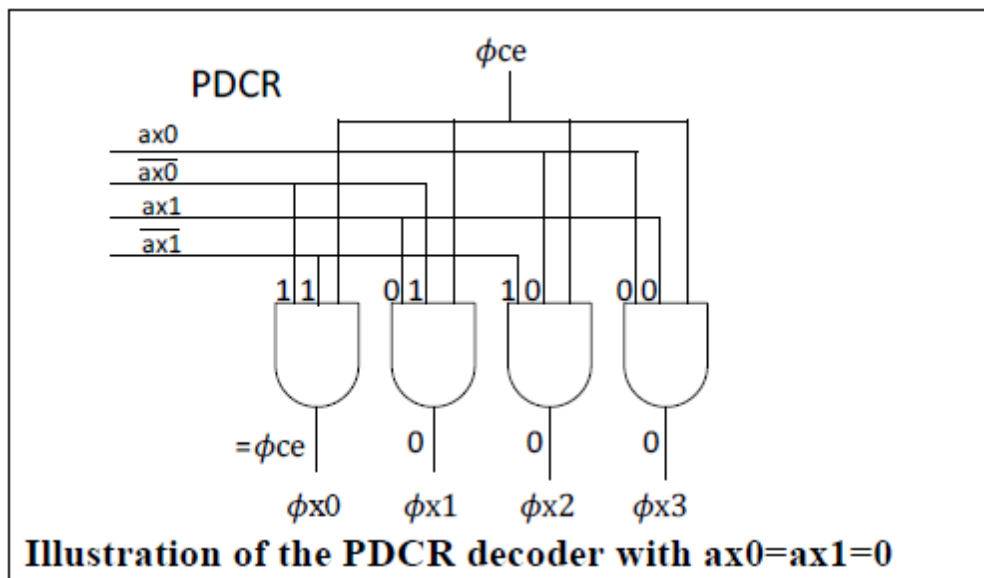
conditional clock generator may apply a zero voltage, a logic low, or ground voltage signal to the non-selected **clocks**.

'002 Patent at 9:53-58, emphasis added.

13. This usage of “clock” and “clock signal” in the '002 Patent for gated clock signals is inconsistent with a construction that requires clocks to be periodic. Non-selected clocks can be low for long, unpredictable, periods of time when the corresponding memory locations are not being accessed, hence these clocks are not periodic. Dr. Pedram apparently agrees that the gated clock signals at the outputs 124, 126, 128, and 130 of the conditional clock generator would not be “clock signals” under his narrow construction of the term as being periodic. Pedram Depo., 83:9-13, 83:19-84:6-7.

14. Furthermore, the outputs of Sato's PDCR would have been considered to be “clock outputs” as used in the claims of the '002 Patent. A POSITA would have understood the PDCR to be performing a similar gating operation with Sato's timing signal as the '002 Patent's clock generator or first logic do with the '002 Patent's clock signal. As I explained in my first declaration (¶¶60-63, 65-66, and 70-71), a POSITA would have understood that Sato's PDCR functions similar to a demultiplexer by effectively switching the timing signal between each of the four PDCR outputs $\phi x0$ - $\phi x3$ according to the values of the two internal address bits $ax0$ and $ax1$ and their complements. I even provided an illustration (reproduced below)

of how a POSITA would have understood the PDCR to operate in view of Sato's explanation. Dr. Pedram did not dispute the accuracy of this opinion. The clock gating demultiplexer that I have illustrated switches one input (ϕ_{ce}) between multiple outputs ϕ_{x0} - ϕ_{x3} according to one or more control signals (e.g., internal address bits). Thus, functionally, Sato's PDCR operates the same as the conditional clock generator and the "first logic" of the '002 patent. Essentially, Sato's PDCR operates similarly to Dr. Pedram's description of clock gating with the added functionality of selecting a particular output ϕ_{x0} - ϕ_{x3} for the gated timing signal ϕ_{ce} based on the memory address inputs ($ax0$ and $ax1$) and their compliments. The functional operation of Sato's PDCR is undisputed. APPLE-1019, 31:6-11.



C. Many references use "clock" or "clock signal" to refer to non-periodic signals

15. In asynchronous dynamic RAMs, the row and column strobe signals ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$) are sometimes described as clocks, even though they are not periodic or fixed-frequency. An example of this usage is in the Itoh reference:

$\overline{\text{RP}}$: H) and all address signals and thus all RX lines are fixed at 0 V. When the addresses have been valid after starting activation with $\overline{\text{RP}}$: L, a clock ϕ_B generated by the $\overline{\text{RAS}}$ buffer is applied, so that only one selected RX line is driven at a high enough voltage, boosted by C_B .

Itoh VLSI, p. 149.

16. Static RAMs also may include non-periodic timing signals referred to as clocks. For instance:

The clock signal generator 14 receives the address transition detect signal SATD from the address transition detector 13, and produces a **clock signal ϕS** that is effective in level for a fixed period. The clock signal ϕS is applied through a clock signal line 23 to the sense amplifier 10 and the data output circuit 11, so that those circuits are rendered active during the fixed period.

Hayakawa, 3:50-57, emphasis added.

17. The clock described in Hayakawa is generated in response to an address change detected by the address transition detector. This clock depends on the particular address pattern and is not periodic. Thus, this static RAM clock requires a definition broader than the definition of “clock signal” offered by Dr. Pedram.

D. Dr. Pedram used the term “clock” for non-periodic signals in his own published papers

18. In addition to the previously cited references, some of Dr. Pedram's own papers use the term "clock" to refer to non-periodic timing signals. Dr. Pedram lists both of these papers in his CV. See Ex. 2001, CV citations [BC18], [C217]. The following quote is from a chapter entitled "Design Technologies for Low Power VLSI" which Dr. Pedram contributed for the book *Encyclopedia of Computer Science and Technology*. *Encyclopedia of Computer Science and Technology*. In this chapter, which was published before the '002 Patent priority date, Dr. Pedram writes:

Moreover in many cases the switching of the clock causes a lot of additional unnecessary gate activity. For that reason, circuits are being developed with controllable clocks. This means that from the master clock other **clocks are derived that can be slowed down or stopped completely** with respect to the master clock, based on certain conditions. The circuit itself is partitioned in different blocks and each block is clocked with its own (derived) clock. The power savings that can be achieved this way are very application dependent, but can be significant.

APPLE-1017, page 90, emphasis added.

19. The bolded text describes "clocks" derived from a master clock, but these clocks are slowed down or stopped and hence would not meet Dr. Pedram's narrow definition for clock signal because these clocks, when stopped, are not periodic.

20. A conference paper that Dr. Pedram's co-authored was published shortly after the '002 Patent priority date in *Proc. of Int'l Conf. on Computer Design*. In the paper, titled "Deterministic clock gating to eliminate wasteful activity in out-of-order superscalar processors due to wrong-path instructions," Dr. Pedram writes:

Clock gating is a well-known technique used to reduce power dissipation in clock associated circuitry. The idea of clock gating is to **shut down the clock of any component** whenever it is not being used (accessed). It involves inserting combinational logic along the clock path to prevent the unnecessary switching of sequential elements. The conditions under which the transition of a register may be safely blocked should automatically be detected. This problem is the target of our paper.

APPLE-1018, p. 1, emphasis added.

21. The clock of a component that is shut down is not periodic. Hence this paper is also describing non-periodic signals as clocks. Again, this usage of "clock" fails to fall under Dr. Pedram's definition for clock signal.

E. A BRI of "Clock Signal"

22. The previous sections give several reasons that the plain meaning of clock should not include a requirement that the signal is periodic. If a construction of the term "clock signal" is required, it is my opinion that a person of ordinary skill in the art would have understood "clock signal" as used in the '002 patent to mean: "a signal used for synchronization." This proposed construction is identical

to Dr. Pedram's construction, except that it removes his unwarranted requirement that the clock signal be "periodic." This proposed construction encompasses the broad usage of the term in '002 patent to refer to signals that are not periodic, the broader scope of the dictionary definitions that include non-periodic clock signals, and the usage of "clock" and "clock signal" in prior art references. In particular, this construction correctly allows for gated clocks including the conditional clock outputs in the '002 patent.

III. There is no race condition related to Sato's clock signal

23. The Pedram declaration has several paragraphs addressing a potential race condition that could occur if Sato's clock signal, ϕ_{ce} , was disconnected from decoders NAG0-NAGk. Pedram Decl. at ¶¶110-113. In my opinion, this is purely a strawman argument because Sato's Fig. 3 and text clearly show that timing signal ϕ_{ce} is connected to those decoders, and none of the '002 Patent claims would preclude this connection from a clock to the decoder. The 4:16 decoder (second logic) of '002 Patent claims do not specify whether this decoder is dynamic or static, and the Sato decoder as shown (including the connections to ϕ_{ce}) satisfies this claim element. The operation of the decoder without the clock is irrelevant. In the actual operation of Sato as described below, there are no race conditions.

IV. Sato discloses a timing signal that synchronizes operations of its row decoder in the same way the '002 clock signal synchronizes operation of its row decoder

24. Pedram is incorrect when he states:

The above-described function performed by the selection control signal ϕ_{ce} of Sato—ensuring that the memory system does not enter into an unstable race condition—is **entirely different than any function performed by the clock signal** of the '002 patent claims. The clock signal of the '002 patent claims does not prevent an unstable race condition from occurring.

Pedram Decl. at ¶113, emphasis added.

25. In fact, as shown below, ϕ_{ce} performs the same function required by the clock recited in '002 Patent claims and as described in the '002 Patent specification – determining when a selected word line is driven low or high.

26. Dr. Pedram may be arguing that the “same function” must mean that the clock signal is not allowed to be used for other functions as well, but no such restriction is part of the '002 Patent claims.

27. Both the '002 Patent and Sato drive the inputs to the final inverting wordline driver in a similar manner. A particular wordline driver is held in a static precharge state with a high input when a different group is selected or a different clock is selected. The clock selection is done by the conditional clock generator (called the predecoder PCDR in Sato). Clock ϕ_{ce} of Sato performs the same function as CLOCK in the '002 Patent claims. It transitions the wordline driver to

the active evaluation state by driving the word line driver input low when the clock is high and the corresponding address is selected.

28. Table 1 compares four operational states for wordline driver XWL0 of the '002 Patent and wordline driver WD0 of Sato in reference to the annotated figure below (described in the petition at pages 30-32 and in my first declaration at ¶83). The four operational states represented in Table 1 are based on 1) whether the wordline driver group of driver XWL0 or WD0 is selected or not and 2) whether the clock generator output/PDCR output (e.g., CLK<1> or $\phi x0$) associated with the wordline driver (XWL0 or WD0) is high or low. In all four cases, the '002 Patent's row address decoder (as shown in the embodiment of Figs. 1 and 3) performs the same operation as Sato's row address decoder (as shown in Fig. 3). In each case, transistors force the input to the word line driver high or low. The input is driven low ("activating" the wordline by driving it high) only when the group is selected (by the 4:16 decoder), the clock is selected (by the 2:4 predecoder), and the clock is high.

#	Selection Status	'002 Word Line Driver Input (ddh0)	Sato Word Line Driver Input (input to WD0)
0	Nonselected group (Address Line 304/ $\overline{S0}$ = HIGH) Nonselected or LOW clock (CLK<0>/ $\phi x0$ = LOW)	Pulled HIGH by LOW CLK<0> turning Mp0 ON and by wordline via 320 (Mn0 is OFF blocking Address Line 304 signal) Wordline WL<0> is LOW	Pulled HIGH by $\phi x0$ turning Q29 ON (Q19 is OFF blocking NAND decoder output $\overline{S0}$ signal) Wordline W0 is LOW
1	Nonselected group (Address Line 304/ $\overline{S0}$ = HIGH) Selected HIGH clock (CLK<0>/ $\phi x0$)	Unselected HIGH address line 304 maintains ddh0 at a HIGH level through Mn0. Wordline WL<0> is LOW	Unselected HIGH NAND decoder output $\overline{S0}$ maintains the wordline driver input at a HIGH level through Q19. Wordline W0 is LOW
2	Selected group (Address Line 304/ $\overline{S0}$ = LOW) Nonselected or LOW clock (CLK<0>/ $\phi x0$ = LOW)	Pulled HIGH by LOW CLK<0> turning Mp0 ON and by wordline via 320 (Mn0 is OFF blocking LOW Address Line 304 group select signal) Wordline WL<0> is LOW	Pulled HIGH by $\phi x0$ turning Q29 ON (Q19 is OFF blocking LOW NAND decoder output $\overline{S0}$ group select signal) Wordline W0 is LOW
3	Selected group (Address Line 304/ $\overline{S0}$ = LOW) Selected HIGH clock (CLK<0>/ $\phi x0$)	Pulled LOW by LOW (selected) address line 304 signal through Mn0 being turned on by HIGH CLK<0> Wordline WL<0> is HIGH	Pulled LOW by LOW (selected) NAND decoder output $\overline{S0}$ signal through Q19 being turned on by HIGH $\phi x0$ Wordline W0 is HIGH

TABLE 1

V. The row address circuit of Sato could be applied in synchronous memory systems

30. Dr. Pedram states that:

Sato's selection control signal ϕ_{ce} does not meet the "clock signal" limitation because it is not a periodic signal used for synchronization but rather one of multiple non-periodic timing signals (ϕ_{ce} , ϕ_{we} , ϕ_{sa} , ϕ_{oe}) used in an asynchronous system.

Pedram Decl. at ¶114.

31. As my previous analysis shows, the "clock signal" limitation should not be restricted to periodic signals. However, even if such a limited construction were adopted, the timing signal ϕ_{ce} of Sato would still satisfy the limitation for "clock signal" because the Sato row decoder circuit would still function with periodic external signals. In other words, there is nothing in Sato suggesting to a POSITA that the periodicity of the timing signal would adversely affect the operation of Sato's row address decoder.

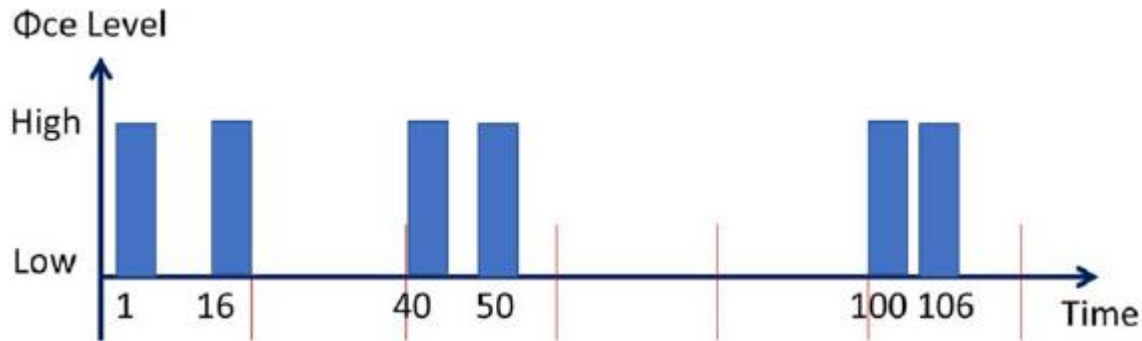
32. Sato shows the ϕ_{ce} signal generated from the TC block in Fig.4 in response to an unspecified function of external signals $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$. No logic or timing diagrams are included in Sato to give the details of how ϕ_{ce} is generated. Dr. Pedram seems to assume that ϕ_{ce} has the same or similar waveform to $\overline{CE}$, but then incorrectly assumes that the external signal must not be periodic.

33. Dr. Pedram and I agree that Sato's timing signal must be an oscillatory signal for Sato's row address decoder to function properly. Compare

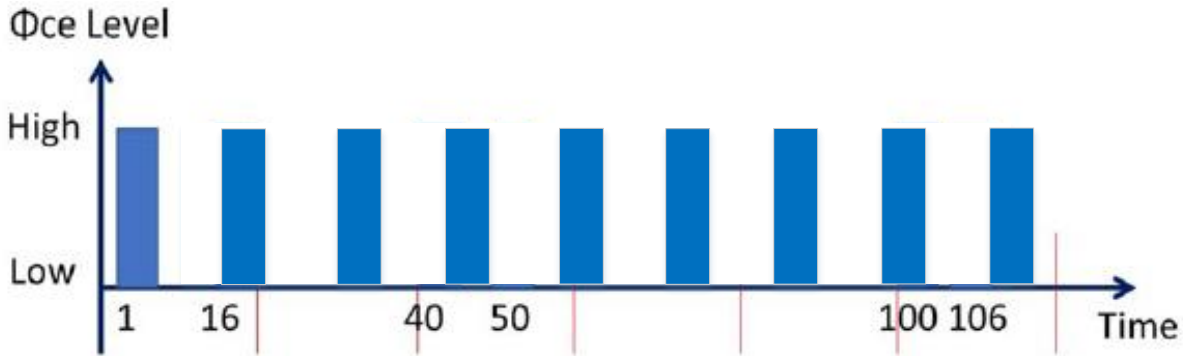
my first declaration at ¶¶68-69 with Dr. Pedram's declaration at ¶¶120-122. In his declaration, Dr. Pedram confirms that, while Sato does include an obscure statement that the timing signal is "kept at a high level" when the RAM is in a selection state (Sato, 3:59-65), the timing signal " ϕ_{ce} cannot stay in a selected state while the row address is changing." Pedram Decl. at ¶120. Dr. Pedram further confirms the analysis I presented in my first declaration:

The petition also argues that "[a]lthough Sato includes an obscure statement suggesting that the timing signal could be kept at a high level, in contrast, a POSITA would not have read this statement as one embodiment, distinct of other aspects described within the Sato disclosure," and that "POSITA would have understood that the Sato system would perform poorly or malfunction if the timing signal in Sato were kept at a high level throughout operation." Petition at 16-17, citing Horst declaration ¶¶68-69. **Dr. Horst's example** of how Sato's address decoder XDCR would fail if it was supplied with two consecutive addresses 000000 and 111100 (the rightmost two bits correspond to ax_0 and ax_1 , respectively) without the timing signal ϕ_{ce} changing state from a selected state to a non-selected state to a selected state (high to low to high) simply **confirms the fact that ϕ_{ce} cannot stay in a selected state while the row address is changing.** In fact, there is a return to non-selected state requirement after a row address is correctly decoded and before a new row address comes in, and **the dynamic NAND gates NAG0- NAGk would fail if one was to evaluate them multiple times without precharging them in between evaluations.** **These facts were well known to a POSA.**

34. Our primary disagreement is merely over the timing of the oscillations or pulses in Sato's timing signal ϕ_{ce} . Dr. Pedram suggests that Sato's memory would only be accessed at random intervals giving rise to only non-periodic timing signals such as that shown in Dr. Pedram's timing diagram reproduced below.



However, as I noted above, this is not my experience. In my experience, it is common to use asynchronous memories in systems that have a synchronous global clock, and in such systems, one would expect memory selection signals to be synchronous to the global clock. Depending on the number of memory banks, such selection may not always be periodic, but in systems with a single memory bank, one would expect the selection signal to be periodic. In such a system, Sato's timing signal would be periodic (as shown by the modifications to Dr. Pedram's diagram below), at least during memory access operations. This application of the Sato circuit would meet the claim limitations under Dr. Pedram's restrictive definition of "clock signal."



35. Even in synchronous systems, such as those illustrated by Itoh, memory control signals (e.g., RS1 and CS1) are not periodic indefinitely. See Itoh's Figure 6.15. These signals are often gated (e.g., turned off) when the memory is not being accessed (e.g., the chip select signal is in a deselected state). In fact, Sato's row address decoder would function fundamentally the same whether the timing signal was periodic or not. The only difference would be regularity at which Sato's predecoder performed its operations, which are the same as the operations recited in the claims of the '002 patent.

36. Furthermore, Sato states that his address decoder could be modified (if necessary) for use in clocked synchronous systems. Modifications, such as adding a global clock input to the TC block would, in my opinion, be well within the capabilities of a POSITA. Indeed, I agree with Dr. Pedram's deposition testimony that a POSITA would have been able to build a clock generator from well-known components in order to accomplish Sato's clear suggestion that his

address decoder could be used in clocked synchronous systems. Pedram Depo., 48:2-21.

VI. Combination of Asano and Itoh

37. I agree with Dr. Pedram's explanation of how one would have built separate address decoders for partitioned groups of address bits. Pedram Depo., 18:7-25:12. I also agree with Dr. Pedram's explanation that the use of a programmable logic array (or "PLA") to implement separate decoders was well-known prior to the priority date of the '002 Patent. Pedram Depo., 23:16-25:12. Even in a single PLA, however, separate and distinct logic paths within the PLA would generate each decoder output.

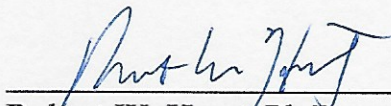
ADDITIONAL REMARKS

38. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

39. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code and that such

willful false statements may jeopardize the validity of the application or any patents issued thereon.

Dated: July 13, 2019

By: 
Robert W. Horst, Ph.D.