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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____))	
APPLE INC.,)	
Petitioner,)	
v.)	Case IPR2018-01249
))	Patent 7,693,002
QUALCOMM INCORPORATED,)	
Patent Owner.)	
_____))	

DEPOSITION OF MASSOUD PEDRAM, PH.D.
LOS ANGELES, CALIFORNIA
THURSDAY, JUNE 6, 2019

DORIEN SAITO, CSR 12568, CLR

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

3
4 APPLE INC.,

5 Petitioner,

6 v.

7 QUALCOMM INCORPORATED,

8 Patent Owner.
9

)
)
)
) Case IPR2018-01249
) Patent 7,693,002
)
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12 DEPOSITION OF MASSOUD PEDRAM, taken
13 on behalf of PETITIONER, at 555
14 South Flower Street, 50th Floor,
15 Los Angeles, California 90071,
16 commencing at 10:01 a.m., Thursday,
17 June 6, 2019, before DORIEN SAITO,
18 CSR 12568, CLR.
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23
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25

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1 I N D E X

2 W I T N E S S :

3 MASSOUD PEDRAM PAGE

4 EXAMINATION BY MS. REICHEL 6

5 AFTERNOON SESSION:

6 EXAMINATION BY MS. REICHEL 80

7
8 INFORMATION REQUESTED:

9 (NONE)

10 QUESTIONS INSTRUCTED NOT TO ANSWER:

11 (NONE)

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1	E X H I B I T S : (Previously marked.)		
2			
3	NUMBER	DESCRIPTION	PAGE
4	Apple 1001	U. S. Patent No. : 7, 693, 002 B2	39
5			
6	Apple 1005	U. S. Patent No. : 4, 951, 259	85
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8	Apple 1006	U. S. Patent Application	85
9		Publication	
10		No. : US 2006/0098520 A1	
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12	Apple 1007	Excerpt from VLSI Memory	85
13		Chip Design Book by Kiyoo Itoh	
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19	Qualcomm 2001	Declaration of Dr. Massoud	9
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25			

1 LOS ANGELES, CALIFORNIA; THURSDAY, JUNE 6, 2019

2 10:01 A.M.

3 -0o0-

4 ***

5 MASSOUD PEDRAM,

6 having been duly administered an oath

7 in accordance with CCP 2094, was

8 examined and testified as follows:

9 ***

10 EXAMINATION

11 BY MS. REICHEL:

12 Q. Good morning, Dr. Pedram.

13 A. Good morning.

14 Q. Can you please state your full name for the
15 record.

16 A. Massoud Pedram.

17 Q. Where are you employed?

18 A. University of Southern California.

19 Q. What is your home address?

20 A. 155 North Willaman Drive, Beverly Hills,
21 California 90211.

22 Q. Do you understand that you're under oath
23 here today, Dr. Pedram?

24 A. Yes, I do.

25 Q. Is there any reason that you cannot give

1 truthful and accurate testimony here today?

2 A. No.

3 Q. Do you understand that you here to discuss
4 your declaration in IPR case No. 2018-01249 relating
5 to U.S. Patent No. 7,693,002?

6 A. Yes, I do.

7 Q. If I refer to the '002 patent, will you
8 understand that I'm referring to Patent No.
9 7,693,002?

10 A. Yes, ma'am.

11 Q. Dr. Pedram, on how many occasions have you
12 provided an expert declaration in an IPR proceeding?

13 A. As I mentioned, three or four times.

14 Q. On how many occasions have you provided an
15 expert declaration in an IPR on behalf of the patent
16 owner?

17 A. At least three out of these four times, but
18 I don't remember the -- the last case, as I
19 mentioned before also. I can check it and let you
20 know.

21 Q. Dr. Pedram, on how many instances have you
22 provided a declaration in an IPR on behalf of
23 Qualcomm?

24 A. This is the only case, the one that we are
25 talking about here. And I -- I don't -- no.

1 There's '674 also. '674, '002 case -- or cases.

2 These are the only times I've provided any kind of
3 declaration in support of the patent owner where the
4 patent owner is Qualcomm.

5 Q. To clarify, you've provided declarations in
6 three different IPR proceedings on behalf of
7 Qualcomm. Two relating to a patent you refer to as
8 the '674 patent and one relating to the '002 patent
9 we're here discussing today?

10 A. That's what I mean. I consider the whole
11 thing to be one case. But you are correct, yes.

12 Q. Dr. Pedram, what did you do to prepare for
13 today's deposition?

14 A. I had a meeting with the counsel here,
15 Joe Sauer, and Josh Nightingale the day before
16 yesterday, from about 10:00 a.m. to 3:30 p.m.,
17 4:00 p.m.

18 I also read through my own declaration. I
19 looked at some of the prior art references. And
20 generally checked the filings that I see and are
21 relevant to this case.

22 I have the list of material that I
23 considered in paragraph 3 of my declaration. Those
24 are generally the ones that I did take a quick look
25 at before coming to this particular session.

1 MS. REICHEL: Can we go off the record for
2 a moment, please.

3 (A discussion was held off the record.)

4 BY MS. REICHEL:

5 Q. Dr. Pedram, regarding the meeting you had
6 on June 4th, how much of that meeting related to the
7 '002 patent in your preparation to today's
8 deposition?

9 A. Probably half of it.

10 Q. Was anyone else present for any of that
11 time, other than the two people you mentioned?

12 A. Joe was physically present. Josh called
13 in. Nobody else was present.

14 Q. Did you speak with anyone else regarding
15 today's deposition?

16 A. No.

17 MS. REICHEL: You should have in front of
18 you what's been marked Qualcomm Exhibit 2001 which
19 is entitled "Declaration of Dr. Massoud Pedram."

20 (The aforementioned document was
21 previously marked Exhibit 2001 for
22 identification by the reporter.)

23 BY MS. REICHEL:

24 Q. Do you see that?

25 A. Yes.

1 Q. Is this a copy of the declaration that you
2 submitted in the -1249 case?

3 A. Yes.

4 Q. You can turn, please, to page 67.

5 A. Yes.

6 Q. Is that your signature on page 67?

7 A. That's correct, yes.

8 Q. Are there any corrections to your
9 declaration that you'd like to make here today?

10 A. No.

11 Q. Did you draft your declaration, Dr. Pedram?

12 A. Yes. All the ideas here are mine. Exactly
13 how the document is put together is not something
14 that I did in terms of the final formatting and then
15 submission and so on. But everything here is my own
16 statements and my own views on different subject
17 matters.

18 Q. Who prepared the various figures in your
19 declaration, Exhibit 2001?

20 A. Prepared actually the artwork, I didn't do
21 it. I think the counsel, maybe they got some
22 graphics person to do it or they cut and paste. You
23 can see most of the figures here are cut and paste
24 so you can clip it and include it. But there are
25 some that are color-coded. I believe somebody, a

1 graphic design or someone did it. I didn't do it.

2 Q. You didn't participate in the creation of
3 those graphics?

4 A. Again, it was done under my suggestion and
5 advice. I wanted certain parts to be highlighted
6 and so on, so forth. But I didn't do it physically.

7 Q. How much time did you spend preparing the
8 declaration that you submitted regarding the '002
9 patent?

10 A. I don't know the exact number of hours I
11 spent. Generally, so far, excluding this particular
12 deposition and preparation for it, I believe I would
13 spend something in the order of 80 to a hundred
14 hours on both '674 and '002.

15 That includes all the reviews I've done and
16 all the discussions I have had with the counsel, and
17 all the readings of various related materials and
18 the preparation of the declaration itself.

19 Out of these 80 to a hundred hours, I would
20 say half of it is spent on the '002 and half spent
21 on the '674.

22 Q. What's your understanding of what your
23 assignment was in this case regarding the '002
24 patent?

25 A. Basically, to understand and evaluate the

1 obviousness combinations that have been presented by
2 Apple to the IPR. And opine on whether these
3 combinations are -- would have been obvious to a
4 person of ordinary skill in the art. And whether
5 the combinations actually meet the limitations of
6 the claims in question.

7 Q. How did you go about your analysis?

8 A. Of course, it's important to -- I sort of
9 assign a -- a broadest reason or interpretation to
10 the claims themselves in view and consistent with
11 the specification.

12 So with that understanding and
13 understanding of the -- some of the legal matters
14 related to obviousness and anticipation and prior
15 art, priority date, and so on, so forth, I looked at
16 the patent itself, which I was quite familiar with.

17 I looked at the particular combinations. I
18 read the report that was submitted by Apple experts.
19 I spent time analyzing that report, looking at the
20 prior art combinations, comparing it to the
21 specification and the claim. And then opining as
22 I've done here.

23 Q. Anything else?

24 A. Generally, no. I mean, not that I recall.

25 Q. What is the priority date that you used for

1 your analysis for the '002 patent?

2 A. I used the priority date, which was the
3 filing date of the '002 patent, which is October 10,
4 2006.

5 Q. Dr. Pedram, do you adopt all the statements
6 in Qualcomm Exhibit 2001, your declaration, as your
7 own?

8 A. Yes, I do.

9 Q. Does paragraph 3 of your declaration
10 comprise a complete list of materials that you
11 reviewed in performing your analysis in this case?

12 A. Yes, it does.

13 Q. You have a paragraph labeled 3(I) that
14 states, "Any other materials referenced herein." Do
15 you see that?

16 A. Yes.

17 Q. Is it fair to say that you would have
18 included any other materials not on this list that
19 you reviewed in some way, in your declaration?

20 A. Yes.

21 Q. Under subheading I, you have a section
22 labeled Professional Background.

23 A. Yes.

24 Q. And spans paragraphs 4 to 19?

25 A. Yes.

1 Q. And does that discussion, combined with
2 your CV, capture all of your relevant experience
3 relating to the '002 patent?

4 A. No. There is a lot of other expertise that
5 I have both in terms of the teaching of the
6 undergraduate and graduate course work, as well as
7 the research projects that I have conducted for
8 various government entities or companies that have,
9 in fact, significant relevance to the memory design
10 and synchronous systems and so on, so forth.

11 The issues related to the '002 patent that
12 probably could not be easily read out or seen in the
13 combination of these paragraphs and my CV.

14 My CV includes the complete list of my
15 publications. So somebody looking at that would see
16 I have many papers on memory-related topics and
17 synchronous systems and clocking and so on, so
18 forth.

19 But my CV does not include the list of
20 projects I have done. For example, I've had 15 NSF
21 funded projects so far. The National Science
22 Foundation. I've had at least four, five big, large
23 amount of funding. Many people involved.

24 DARPA funding. I have had IARPA funding.
25 I have had SRC funding. And I do different projects

1 as part of these projects. Myself and my Ph.D.
2 students over the years have performed a lot of
3 different tasks that are not captured in the
4 combination of these paragraphs and my CV.

5 Q. Is appendix A to your declaration an
6 accurate copy of your CV?

7 A. Yes, ma'am.

8 Q. Prior to October 10, 2006, have you -- have
9 you designed or supervised the design of any memory
10 decoding scheme?

11 A. Sure. Yes, of course.

12 Q. How many?

13 A. I worked both on decoding for SRAM as well
14 as DRAM. I have papers on various kinds of coding
15 schemes that would minimize switching activity or
16 power dissipation of address buses or data buses
17 feeding into these memory type devices.

18 I teach SRAM design and DRAM design as part
19 of my -- I shouldn't say my -- but our VLSI design
20 course series at University of Southern California,
21 EE department. We have an undergraduate course
22 called 477L. We have two graduate courses, 577A and
23 577B.

24 As part of 477L, we teach basic knowledge
25 of SRAM and DRAM cells and small arrays. 577A

1 focuses on big arrays and more complicated topics,
2 such as all kinds of things about sensing and
3 address decoding and pre-decoding this and that, and
4 various other optimizations you could perform to
5 maximize performance or minimize power dissipation.

6 Then 577B, which is the more advanced
7 course, actually, the final projects that's
8 typically given to students is the design of a DDR-3
9 DRAM controller. So we actually do the full -- look
10 at the specification. We ask the students to write
11 the DDR-3 controller according to the specs. We do
12 the VLSI design of the DDR-3 controller. We verify
13 post sort of layouts to make sure it meets the
14 timing spec and so on, so forth.

15 So I've had significant, I must say,
16 expertise in this area that goes well beyond what a
17 person of ordinary skill in the arts know -- would
18 have known at 2006 time frame.

19 Q. Dr. Pedram, if I can ask you to please slow
20 down a bit. I think it's a bit difficult for the
21 court reporter to keep up with you.

22 A. I appreciate that. That's good -- good
23 comment, yes.

24 Q. Dr. Pedram, do you understand that my prior
25 question was limited to your experience prior to

1 October 10, 2006?

2 A. Yes, I do.

3 Q. The classes that you just described, you
4 taught those class prior to October 10, 2006?

5 A. Yes.

6 Q. You mentioned that you taught your students
7 about pre-decoding prior to October 10, 2006. What
8 were you referring to?

9 A. So basically, if you are implementing a
10 decoding of a set of address bits, you could do it
11 in one shot or you could do it in two stages.

12 And the idea of pre-decoding that I taught
13 my students was that you can take a group of bits,
14 partition them into two subgroups and do the
15 decoding of these two parts separately and combine
16 the results.

17 And that tends to create tradeoffs in terms
18 of area, performance, power dissipation that's of
19 interest to us, generally. And we had discussed it
20 and -- and I teach those things in any classes even
21 then, yes.

22 Q. Prior to October 10, 2006, how did you
23 teach your students to partition an address into two
24 subgroups?

25 A. At that point, it was more of a general

1 exercise. If I have six bits less partition into
2 group -- two groups of three bits, and then decode
3 this group of three bits, decode this other group of
4 three bits. And then, of course, you have to
5 combine them to get the final decoding. And that's
6 how it would start.

7 Q. When you say you would teach your students
8 to partition the bits, what do you mean by
9 "partition"?

10 A. Create two different group -- grouping of
11 bits. Like if you have groups 0 to 5 as the
12 complete address bit, you would do 0, 1, 2 as one
13 group and then 3, 4, 5 bits as a second group.

14 That's the partition. Partition always
15 refers to sort of creating these parts which are
16 disjoined from each other. And then when combined
17 together, they create original set.

18 Q. When you say that you taught your students
19 to create groups that were disjoined from each
20 other, what makes a group disjoined from each other?

21 A. If you look at the group of bits as two
22 sets of elements, the intersection of the two sets
23 is null.

24 Q. Sorry. What was the last word you said?

25 A. Null, n-u-l-l. It's a null set. I mean,

1 it's well-known in Venn diagram and so on.

2 Q. Prior to October 10, 2006, did you teach
3 your students to create different logic elements to
4 decode the different address bits that you had
5 taught them to partition?

6 A. Yeah. Of course. I mean, when you want to
7 decode logic depending on various performance power
8 dissipation or area constraints, you have different
9 options.

10 And one simple method is to just take every
11 bit, create two -- itself -- use itself and its
12 complement, and then run the various combinations of
13 the bit and the complements into AND gates that
14 would fire only when the right combination of the
15 input values of the complements is applied.

16 And because of the way you do it exactly,
17 one of these AND gates would fire and then you take
18 that and gate as the output and -- and use it to
19 drive whatever you need to drive.

20 And this kind of decoding really has very
21 little to do with memory design as such. I mean,
22 you could do it for all kinds of other applications.
23 Any time you want to decode address bits, you
24 typically use AND gates. Sometimes you would use OR
25 gates if it's -- the sense of the signals are active

1 low, for example, compared to active high.

2 But it's well-known that you can do these
3 things, and the logic elements of such are known
4 also.

5 Q. Would you refer to the system you just
6 described as a one-hot decoder?

7 A. Yes. So the implementation I suggested to
8 use an and gate and so on is a one-hot decoder. It
9 could have been also a 0-hot decoder. And 0-hot
10 decoder -- so one-hot decoder means you have a
11 series of output bits, exactly one of them is one.
12 The rest are 0.

13 0-hot decoder means you have same group of
14 bits, all of them are one with the exception of one,
15 which is 0. So what I described to you was
16 implementation of either one-hot decoder or 0 hot
17 decoder.

18 Q. Prior to October 10, 2006, did you teach
19 your students about both types of decoding, the
20 one-hot and the 0-hot decoder?

21 A. Normally we do talk about it, yes. Because
22 it's -- again, always it's interesting when you
23 present one extreme, because one-hot decoder is one
24 extreme, 0-hot decoding is the other extreme. And
25 then you have all these other coding schemes in

1 between. Balance codes and weighted codes and gray
2 codes and so on, so forth, that sometimes you teach
3 to students also.

4 So -- because they're -- those are the
5 extremes that, as I see it, one-hot versus 0-hot, I
6 definitely mention those. And in between, sometimes
7 we mention that there's ways of coding also, if
8 relevant.

9 Q. Prior to October 10, 2006, when you taught
10 your students about splitting an address into two
11 different portions, did you teach them that distinct
12 logic elements could be used to decode each portion
13 of the address?

14 A. I'm not sure what that means exactly, the
15 question means distinct. So obviously you would use
16 distinct gates. So you have different gates. So
17 one logic gate is distinct from another logic gate.

18 So normally, I would consider this even, if
19 you're doing one -- one shot decoding or multistage
20 decoding, the overall module is just your decoder.
21 You have one module doing decoding. Internal to
22 that module, you see two different implementations
23 with different number of logic gates. And these
24 logic gates, of course, are separate from each
25 other. They are different logic gates. Right?

1 But that's it. I mean, the module that
2 does decoding is the same module. It's just the
3 internal implementation is one shot decoding or
4 multi stage, multiple step decoding.

5 Q. If you were teaching your students prior to
6 October 10, 2006, to take a 6-bit address and
7 partition it into 1-bit, 3 bits and 2 bits, would
8 each of those groups of bits have its own logic
9 gates?

10 A. So first of all, I want to make sure that
11 I -- I -- when I teach my students about this, I
12 don't say this is the preferred way of doing it
13 versus the other way. I'm just telling them you
14 could do it one shot, you could do it multiple step,
15 and these are the tradeoffs that exist. Right? And
16 then stop there.

17 So there is no preference stated for one or
18 the other. People might use one or the other. So
19 having said that, if somehow the partitioning was
20 1-bit, 2 bits and 3 bits as you described of the
21 group of 6 bits, then these will all be implemented
22 inside the decoding module.

23 And then in that decoding module, of
24 course, there's going to be some sharing of the
25 signals. Because, as you know, with -- when I

1 implement, for example, the 3-bit decoder, a
2 particular variable or its complement will be used
3 as input to multiple different AND gates because it
4 has to go to all the different AND gates to create
5 the combinations of all possible 01 assignments of
6 the bits. Right? So that you can decode all
7 different combinations simultaneously.

8 So there's a sharing definitely there and
9 then of the signal or the inverter that did the
10 inversion of the original signal, going to all these
11 different AND gates. So that's there.

12 But obviously, the AND gate that's used in
13 one part to deal with one combination is different
14 than the AND gate that is used in a different part
15 to deal with a different combination of AND gates.

16 Q. Are you saying you would use one set of AND
17 gates for the 1-bit, another set for the 2 bits and
18 another set for the 3 bits?

19 A. So one implementation would be precisely
20 what you said. Of course, for the 1-bit, you won't
21 use any AND gates. But yeah, for the 2 and 3 bits,
22 the AND gates that would do the decoding of the
23 2-bit group will be different from the AND gates
24 that are used for the decoding of the 3 bits.

25 But mind you, there is another

1 implementation that I also teach to my students,
2 which is, for example, using a PLA. If you use a
3 PLA to do this kind of decoding, a PLA has rows and
4 columns. And the number of rows are fixed, the
5 number of columns are fixed. These are programmable
6 logic arrays with fixed capacity. And then you
7 would program the rows and the columns so that you
8 produce the right result.

9 In that case, you have a single PLA that's
10 implementing the 3-bit decoder and the 2-bit decoder
11 and the 1-bit decoder all in one fabric. And that's
12 another implementation that we do teach our students
13 because it's not necessary to implement these 1-bit
14 decoder, 2-bit decoder, 3-bit decoder as having
15 separate disjoint gate sets. You could actually use
16 the same joint fabric, common fabric, which is a
17 programmer logic array, to implement all three of
18 them using that one fabric. And that, I do teach to
19 my students also.

20 Q. When you say "PLA," are you referring to
21 programmable logic array?

22 A. Yes, ma'am.

23 Q. So prior to October 10, 2006, your students
24 would have been familiar with using both a PLA as
25 well as using distinct logic elements for each

1 portion of the memory address; correct?

2 A. If they were tasked to separate the bits of
3 address into different groups, if they have decided
4 this is the thing they want to do and there was a
5 tradeoff. So they have to decide if that's the
6 right thing to do for the decoding task at hand or
7 no. But if they decide they want to partition it
8 into two disjointed group and decode them separately
9 and combine them -- as I said, you have to combine
10 the results -- then, sure. They know how to do it
11 using logical gates and they know how to do it using
12 PLAs, yeah.

13 Q. Are there any other approaches you would
14 have taught your students prior to October 10, 2006,
15 to decode an address that they had already decided
16 should be partitioned?

17 A. I guess the point I'd like to make here
18 are two, which is relevant. One is sometimes,
19 especially in my advanced VLSI design course, 577A,
20 we talk about other coding schemes. Right? That --
21 some of which I have developed personally in my
22 research group. Right? But also some of which are
23 also well-known.

24 And so we teach people how to implement,
25 create decoders for those types of codes; black

1 codes or gray codes or T1 codes, so on, so forth.
2 And so -- and some of these coding schemes, then,
3 are not separable in the way that you have in mind.
4 One.

5 Secondly, there is a -- I think there's
6 a -- I realize from the line of questioning now
7 there is a point that needs to be clarified. When
8 we talked -- when I taught my students to do a 6-bit
9 de- -- for example, decoding, the idea still was to
10 come up with the two to the six possible different
11 outputs. Right?

12 So if I break it in two groups of three
13 bits, so when I decode the first group I get eight
14 outputs. I decode the second group, I get eight
15 outputs. I still have to combine these eight and
16 eight. 8 times 8 is 64. Right?

17 So there's going to be AND gates that will
18 take the output of these things and combine them
19 together to finally create the 64 outputs that I
20 want to come.

21 It's not like I'm doing a 1-bit decoder, I
22 don't care about the rest. I just do the 1-bit
23 decoding or 2-bit decoding. I never taught them
24 that.

25 I taught them that they can do the decoding

1 of a 6-bit address producing two to the six
2 different outputs, which are 64 outputs, in a single
3 stage or in multiple stages.

4 That's what I mean by partitioning and in
5 different implementation. I did not mean -- and I
6 did not then, a few minutes ago. And I did not
7 teach my students that while maybe there are
8 applications in which the 6-bit decoder really
9 doesn't have to be fully decoded and you take maybe
10 2 bits of it and use it to do something, and then
11 another 4 bits and do something else with it.

12 No, that's not what I taught. I just want
13 to clarify what I taught and what I did not.

14 Q. In the example we discussed earlier where
15 you would teach your students to take a 6-bit
16 address, for example, and partition it into 1-bit, 3
17 bits and 2 bits, what type of logic would you use to
18 decode the 1-bit?

19 A. Actually, I never taught the students to do
20 1-bit. I mean, that didn't make any sense to me. I
21 mean, so if you talk to people normally that do
22 multi stage decoding, I've never seen -- and this is
23 without any exaggeration -- I mean, really, I've
24 never seen anybody create a partition of 1-bit and
25 5-bit.

1 If anything, you would know, from the law
2 of minimizing your effort and cost, that the best
3 partition is typically half. Half of the elements
4 go into one group, half go into the other group.
5 Right? That's usually how it's done.

6 So 3 and 3. Normally, you don't do 3 and 2
7 and 1. Maybe you do 4 and 2 sometimes because of
8 some performance preservation. But you never -- I
9 mean, I've seen 3, 2, 1. So I've never taught my
10 students. And in fact, I would discourage them now,
11 as a student, and I would even discourage them here,
12 then and now, that this is not a good idea.

13 If -- because when you do 1-bit decoding,
14 what are you doing? You're just doing nothing,
15 actually. You're just passing two wires ahead. The
16 signal and its complement are being pushed forward.
17 You are delaying the work that needs to be done to a
18 later stage, the final stage in which you combine
19 things. That's not a good idea.

20 Just do it as soon as you can and then
21 combine them. Don't delegate things to the future
22 and then potentially create more problems for
23 yourself. So that's not the preferred thing I would
24 have ever taught my students. But, please, go
25 ahead.

1 Q. Prior to October 10, 2006, would your
2 students have been able to decode an address bit
3 that -- or an address that was only 1-bit?

4 A. I don't know even what that means. Address
5 that's -- what is a 1-bit address? I mean, as you
6 say 1-bit address means what? So it's a
7 selection -- selection signal.

8 So if I'm using a selection signal, I would
9 normally -- and, again, a POSA would understand that
10 to be a selection signal you use for a multiplexer
11 or to steer logic flow, signal flow in some
12 implementation and so on.

13 So a 1-bit address -- so 1 bit of an
14 address, I understand. But a 1-bit address, as
15 such, I -- I guess you -- you could have that, but
16 it's not something I would have taught my students.

17 Q. How would a person of skill in the art
18 prior to October 10, 2006, have used 1 bit as a
19 selection signal to steer signal flow?

20 A. So again, multiplexers. I mean, normally,
21 if you have a multiplexer, there is a select signal.
22 And the multiplexers need both a select and a select
23 bar. And then, depending on what the value of the
24 select is, either you let the pass starting from
25 input A to go through or the pass starting from

1 input B to go through.

2 So you steer logic from A to output or from
3 B to output based on the selection signal S. That's
4 how we normally use selectors. Yeah.

5 Q. And when you say you would let the signal
6 go through or not go through, how would a person of
7 skill in the art have done that in the October 10,
8 2006, and earlier time frame?

9 A. Again, multiplexers are well-known and
10 people would have been taught to use multiplexers.
11 2 to 1. There is 2 to 1 multiplexer, for example,
12 that takes two inputs and passes only to the output
13 based on the selection signal.

14 Q. Any other methods that would have been
15 known prior to October 10, 2006?

16 A. I don't know. I haven't considered this.
17 Off the top of my head, I can sort of think of and
18 see what else one could have done. I know there are
19 many different implementations of the selectors.

20 I mean, you could have pass transistor
21 based implementation. You could have transmission
22 gate based implementation. You could have fully
23 static logic implementation. You could have dynamic
24 logic implementation. You could probably do it in
25 digital domain. You could do it in analog domain.

1 I mean -- yeah, and maybe more. Just can't
2 be comprehensive here and now.

3 Q. Dr. Pedram, prior to October 10, 2006, were
4 you familiar with a concept called clock gating?

5 A. Yes.

6 Q. What is clock gating?

7 A. It's the gating of the clock signal such
8 that you allow the clock signal to propagate to the
9 rest of the circuit under one condition -- or set of
10 conditions, and then stop it from propagating
11 through under a complimentary set of conditions.

12 Q. When you say "gating of the clock signal,"
13 are you referring to the process of either allowing
14 the clock signal to pass through or preventing the
15 clock signal from passing through?

16 A. That's generally what clock gating means,
17 yes. Yes, I would say.

18 Q. Were persons of ordinary skill in the art
19 familiar with clock gating prior to October 10,
20 2006?

21 A. I'm trying to remind myself what the skill
22 set of the person of ordinary skill in the art is
23 relevant to this. I think it's a bachelor's degree,
24 but I want to look at -- can you point me, to speed
25 up, to the appropriate section?

1 Q. Sure. Take a look at paragraph 48 of your
2 declaration.

3 A. Thank you.

4 Q. Using the definition of the person of
5 ordinary skill in the art in paragraph 48 of your
6 declaration, was that person familiar with the
7 concept of clock gating in October 10, 2006, in your
8 opinion.

9 A. I can't be sure, but likely. Yes.

10 Q. Did you teach your students the concept of
11 clock gating prior to October 10, 2006?

12 A. As part of my undergraduate course in that
13 timeframe, I don't believe I did that. No. As part
14 of my graduate course work, definitely we did.

15 So 577A, I had modules and lectures on
16 clock gating. 477, because the students come from a
17 background which is general EE, electrical
18 engineering 101, 201, 301, that kind of thing.

19 Clock gating would be considered an
20 advanced topic for them, so we don't talk about
21 clock gating in that course to the undergraduate
22 students. But the graduate students, yes.

23 Q. Prior to October 10, 2006, how did you
24 teach your graduate students to implement a clock
25 gating scheme?

1 A. Simple ways are to use AND gates or OR
2 gates depending on, again, if the conditions you are
3 interested in are sort of active high conditions or
4 active low conditions, you'd use OR gates.

5 And then you would also look at the sense
6 of the clock, whether the triggering edge of the
7 clock is positive as triggered or negative as
8 triggered. And there are tradeoffs in terms of how
9 you do the clock gating.

10 And so -- and then that's normally what we
11 teach them, that be careful what kind of clock
12 gating element you use, AND gates versus OR gate for
13 what kind of clock signal and what kind of
14 conditions, clock gating conditions at that level,
15 to the graduate students only.

16 I -- I can say that for sure. This is
17 definitely not a topic I would have covered for my
18 undergraduate students.

19 Q. Did you provide your graduate students
20 prior to October 10, 2006, with any reason they may
21 want to do clock gating in systems?

22 A. Yes, of course. Clock gating helps
23 minimize the effort of, basically, when you do clock
24 gating when the clock signal is not needed for the
25 computations. You could, of course, let it go

1 through. It doesn't do any harm, typically, it just
2 goes when you do some computations. But then you
3 ignore the result of those computations because you
4 didn't need the computation to be performed under
5 those conditions.

6 So in that case, you are being wasteful in
7 terms of the resource usage. And so we teach the
8 students not to be wasteful. And so one idea would
9 be, therefore, if you can, use clock gating.

10 And I've been working low power design
11 maybe since 1992 and three. So one of the big --
12 and back then, people didn't care about power
13 dissipation and efficiency and energy efficiency and
14 so on.

15 So we would go around, myself and a
16 colleague of mine from UC Berkeley, Jan Rabaey,
17 would give these tutorials -- and this is 1998 time
18 frame -- that would say, yeah, try to do clock
19 gating because it will help you reduce power
20 consumption.

21 Q. Do you agree that, starting in the 1998
22 timeframe, persons with ordinary skill in the art
23 would have understood that clock gating was an
24 option they could look at to implement their designs
25 in VLSI?

1 A. Again, not because of the particular
2 training as an undergraduate graduating in
3 electrical engineering. But perhaps because of the
4 three years of experience that this person would
5 have, I -- I would expect a -- a POSA, as I said,
6 would be familiar with some concepts related to
7 clock gating and why clock gating is useful.

8 Q. I don't think I asked you this question, so
9 I'm going to ask it now.

10 Is the definition set forth in paragraph 48
11 of your declaration of the person of ordinary skill
12 in the art, the definition that you use in arriving
13 at your opinions in this case?

14 Actually, let me ask that again, because it
15 was not a very good question.

16 Dr. Pedram, is the -- does the discussion
17 at paragraphs 48 to 51 of your declaration
18 accurately reflect the level of skill in the art
19 that you applied in arriving at your opinions in
20 this case?

21 A. Yes, they do.

22 Q. Can you please turn to pages 7 to 9 of your
23 declaration, Exhibit 2001.

24 A. Yes.

25 Q. Who drafted paragraphs 20 to 26 of your

1 declaration at pages 7 to 9?

2 A. This was mostly provided to me by the
3 counsel. I reviewed it, I understood it, and I
4 included it as relevant legal standards in this
5 matter.

6 Q. Do paragraphs 22 to 26 of your declaration
7 accurately reflect the legal standards that you
8 applied in arriving at your opinions in this case?

9 MR. SAUER: Objection; form.

10 THE WITNESS: This is a good summary of the
11 relevant law. Without trying to be comprehensive of
12 all the applicable legal standards, this is a
13 summary of the high level points that was provided
14 to me, and I understood and agreed to it and applied
15 it.

16 BY MS. REICHEL:

17 Q. Is there anything in paragraphs 22 to 26 of
18 your declaration that you did not agree with and did
19 not apply in your analysis in this indication?

20 A. No.

21 Q. Dr. Pedram, did you perform any analysis in
22 this case specific to any dependent claims?

23 A. I know I looked at number of different
24 independent claims. 1, 7, 11, 17, so on, so forth.
25 Yes. Some of them, yes.

1 Q. Which ones?

2 A. I guess what I'm saying is that I find that
3 the claims at issue include dependent claims also.
4 Of course, I focused primarily on independent claims
5 saying that they are valid. And my understanding is
6 that if an independent claim is valid in view of the
7 prior art, all the dependent claims are also valid.
8 And so I didn't focus on any of the dependent
9 claims, as such. My focus was on independent
10 claims.

11 Q. There's no analysis in your declaration
12 that is specific to a limitation that was added by
13 any dependent claim of the '002 patent; correct?

14 A. That is correct.

15 Q. Is it also correct that you did not perform
16 any analysis specific to the means plus function
17 aspects of any of the claims of the '002 patent?

18 MR. SAUER: Objection; form.

19 THE WITNESS: I -- I -- I believe so.

20 BY MS. REICHEL:

21 Q. Please turn to the section Roman numeral
22 III of your declaration that begins at page 9.

23 A. Yes.

24 Q. You have here a technology background and
25 overview of the '002 patent; is that right?

1 A. Yes, ma'am.

2 Q. Is there a reason that your technology
3 background and overview of the '002 patent does not
4 include any figures in the '002 patent?

5 A. No, no particular reason.

6 Q. You, instead, have two other figures that
7 are not present in the '002 patent; is that right?

8 A. Yeah. They are sort of a redrawing of
9 the -- some of the concepts which are also taught in
10 '674 as prior art. Right?

11 So I like colors and colorful drawings, and
12 I remember the first time I gave a talk in Japan.
13 This was 2000-- 1996. The talk went well.
14 Everybody liked it. I came down, and then the host
15 came to me, said, Excellent talk. Great job,
16 Dr. Pedram. But you know, in Japan, we don't like
17 so many colors. Because my slides were full of
18 color. Black and white, gray, shades of gray are
19 better. So fine. So --

20 Q. Dr. Pedram, I appreciate your stories, but
21 I'm concerned that we'll be here all day if we have
22 to put them all on the record. So I'm going to ask
23 my question again, which is specific to these two
24 figures.

25 MR. SAUER: For the record, Dr. Pedram

1 referred to the '674 patent and I think he meant to
2 refer to the '002 patent.

3 THE WITNESS: That's correct, yes.

4 BY MS. REICHEL:

5 Q. Well, I'll ask the question again, anyway.

6 Dr. Pedram, you agree that the figures on
7 pages 10 and 12 of your declaration are not present
8 in the '002 patent, as drawn here; correct?

9 A. That's correct, yes.

10 Q. Were the figures on pages 10 and 12 of your
11 declaration created by you?

12 A. Not the graphics itself. But the hand
13 drawing of this, what we want to do, definitely is
14 mine.

15 Q. Is it your understanding that the drawings
16 shown on pages 10 and 12 of your declaration depict
17 what was prior art to the '002 patent?

18 A. Yes.

19 Q. Can you turn to page 12 of your
20 declaration, please.

21 (The aforementioned document was previously
22 marked Exhibit 1001 for identification by
23 the reporter.)

24 THE WITNESS: Yes.

25 ///

1 BY MS. REICHEL:

2 Q. In the figure in page 12 of your
3 declaration there is a triangle labeled Clock
4 Driver. Do you see that?

5 A. Yes.

6 Q. Does the clock driver that you've depicted
7 on page 12 of your declaration correspond to any
8 element shown in any image of the '002, which is
9 Apple Exhibit 1001?

10 A. There is a clock signal in various figures
11 of the '002, as well as in the description, the
12 specification itself. There is no clock driver
13 block, that I can see, in any of these figures.

14 Although, it's intrinsic. Inherent, I must
15 say, that if you have a clock, there should be a
16 clock driver for it.

17 So I included this because I don't know of
18 anything, and I believe this is inherently true,
19 that there should be a clock driver to produce the
20 clock signal.

21 Q. Are you saying that the clock signal in the
22 '002 patent which is labeled 118 in Figure 1, would
23 be output of the top of clock driver that you have
24 shown on page 12 of your declaration?

25 A. Yes.

1 Q. What were some types of clock drivers known
2 to persons of skill in the art prior to October 10,
3 2006?

4 A. So typically, a clock driver would take the
5 output of a clock generator and drive it to where it
6 has to go. And that could be a series of big
7 inverter circuits. Right? That just provide the
8 strength that you need to distribute the clock
9 signal to where it has to go.

10 So I would say at least one easy way of
11 doing a clock driver would be an appropriately sized
12 inverter that -- that -- or a pair of inverters that
13 would pass the signal through at the right strength.

14 Of course, there's a clock generator also,
15 and there are PLA circuitry called phase lock loops
16 that take the output of a crystal chip and then
17 multiply it appropriately to create the operating
18 frequency for the circuitry on the chip.

19 The clock frequency of the crystal
20 oscillator could be maybe 10s of megahertz and you
21 multiply it out to get it to gigahertz range, or
22 whatever you need, and using phase lock loops. And
23 then you distribute it to the rest of the circuit.

24 You could also internally use delay lock
25 loops to create further synchronization wherever you

1 need it, and so on, so forth. But that's beyond the
2 scope. For the purpose of clock driver, think of it
3 as a pair of inverters.

4 Q. You used a few terms. I want to back up
5 and make sure we clarify those terms. When you
6 refer to a crystal, is that the circuit component
7 that actually generates the clock?

8 A. It -- it generates a steady stream of
9 pulses. Typically, very precise fixed frequency
10 periodic pulse stream. And that -- that is at low
11 frequency for the chips that we run today. Maybe in
12 5, 10, 15 gigahertz range -- I'm sorry -- megahertz
13 range. Megahertz range.

14 And then you take that and you multiply it
15 out so that you get high frequency of maybe 800
16 gig -- megahertz or 1 gigahertz or 2 gigahertz,
17 whatever you need to have.

18 That's well-known in the art. Of course,
19 you could do clock generation itself using a loop
20 of -- with odd number of inverters in it,
21 appropriately sized and so on. Because when you do
22 that, if you analyze it, it will generate the pulse
23 stream of fixed frequency.

24 And the cycle time of that pulse stream
25 would be twice the loop delay. But -- but those --

1 those are not very well compensated against process
2 manufacturing valuations and temperature effects,
3 and so on.

4 So for chips that need to rely on a steady
5 periodic stream of pulses for orchestration of their
6 activities and synchronization, typically using a
7 loop of inverters, odd number of inverters is not
8 advisable. It's not stable enough.

9 So people use the other method, which I
10 said. Crystal frequency is very precise temperature
11 compensated, typically. And then you increase the
12 frequency by whatever factor you need to get to the
13 frequency range of features using phase lock loops
14 and -- or multipliers.

15 Q. Let me try and clarify some of what you
16 just said. In the type of system that we see in the
17 '002 patent, it would have been typical, prior to
18 October 10, 2006, to have some sort of clock
19 generation circuit, like a crystal, that could
20 generate fixed frequency periodic pulses that would
21 then be used by other circuitry, such as a phased
22 lock loop, to generate the frequency of pulses
23 needed for the system; is that right?

24 MR. SAUER: Objection; form.

25 THE WITNESS: And frequency multipliers.

1 So frequency multiplication could be integrated into
2 the phase lock loop itself or could be done
3 separately, but generally correct.

4 I mean, you have phase lock loop and
5 frequency multipliers. You take the output
6 frequency -- a crystal oscillator, very precise
7 frequency output at relatively low frequency and get
8 whatever you want at the output.

9 So that would be your frequency generation,
10 clock generation step. And then you have to
11 distribute it. And the distribution was clock
12 drivers and so on.

13 So when I used the term "clock driver," I
14 meant, yeah, somebody gave me the clock signal. I'm
15 just driving it to where it has to go.

16 BY MS. REICHEL:

17 Q. The figure that you have on page 12 of your
18 declaration, as well as what we see in Figure 1 of
19 the '002 patent, both relate to the decoding of a
20 row address; is that right?

21 A. Yes.

22 Q. Would the system that we see in Figure 1 of
23 the '674 patent also have a mechanism for decoding a
24 column address?

25 A. Not that's shown in Figure 1.

1 I mean, one would generally understand if
2 you have a memory array you have rows that you need
3 to decode, you have columns that you need to decode.
4 But this particular invention relates to the row
5 decoding, as is says it, and doesn't discuss the
6 column decoding.

7 And there are issues one has to be aware of
8 with respect to column decoding. The state of the
9 art memory devices do burst access, which means you
10 don't have to do full column decoding because a lot
11 of axis are inversed, like 8 and 16, and so on, so
12 forth.

13 So the issues aren't the same. You have to
14 be aware of those issues. But again, that's not
15 been the focus of Lin's patent, '002 patent?

16 Q. There's no mechanism for decoding column
17 addresses shown in Figure 1, or anywhere else in the
18 '002; correct?

19 A. Not that I recall, no.

20 Q. In practice, however, a person of ordinary
21 skill in the art would have added a mechanism for
22 decoding column addresses to use in combination with
23 the decoding mechanism that is described in the '002
24 patent; correct?

25 MR. SAUER: Objection; form.

1 THE WITNESS: It -- again, there are
2 differences between column decoder and -- and row
3 decoder. There are different performance
4 constraints. One is driving board lines. One is
5 drawing columns. Board lines are, typically, highly
6 resistive. Columns are very low resistance.

7 So in terms of performance issues, there
8 are different observations. Columns that are
9 accessed in burst typically maybe burst length of 8
10 or burst chop mode 4, what have you. But generally,
11 you need to do decoding of some bits of the column
12 address also. And one would have known to decode --
13 how to decode corresponding bits of the column
14 address, yes.

15 BY MS. REICHEL:

16 Q. Just to be clear, the memory array that's
17 depicted in the '002 patent would require both the
18 row decoding scheme and the column decoding scheme;
19 correct?

20 A. It doesn't say it. Again, it depends,
21 really, on the size of the array. So imagine I'm
22 trying to address 16 bits of data as I do this, and
23 I have only 16 columns in the array. Then I don't
24 need to do any column decoding because the whole row
25 is 16 column bits and I need to read out 16 bits

1 anyway. Why should I decode? I don't decode the
2 columns. I just read it out.

3 In fact, many places, if you look at the
4 hierarchy of the memory organization, they bake
5 these big memory arrays into banks and quarter banks
6 and sections and subsections, and when they read,
7 finally, a subsection, they will probably read the
8 whole subsection.

9 There's no column decoding there. I mean,
10 they're just reading the whole thing. The whole
11 thing is being read out. But that's a matter of
12 implementation.

13 I'm not disagreeing with you saying that no
14 column decoding is needed. But I'm saying, from
15 this specification, it's not clear to me because the
16 memory array size is not given and the width of the
17 word that I'm reading out is not clear, whether a
18 column decoding would have been necessary. Maybe
19 not.

20 Q. If the memory array in Figure 1 of the '002
21 patent were large enough that a column decoding
22 mechanism were necessary, a person of skill in the
23 art would have been able to implement such a column
24 decoding mechanism; correct?

25 A. I would think so, yes. Column decoders,

1 row decoders are well-known in that time frame, yes.

2 Q. Would the person of ordinary skill in the
3 art prior to October 10, 2006, have known how to
4 create the clock 118 signal that we see in Figure 1
5 from the clock generation circuitry that you
6 discussed before?

7 A. So if I understand the question correctly,
8 the person skilled in the arts would know that there
9 are these components that you could have purchased,
10 acquire, integrate, that would allow you to
11 establish a clock generator circuitry that would
12 produce the clock signal. You have to have drivers
13 to get the signal where it has to go.

14 That would have been known to a POSA. But
15 a POSA would have a lot of difficulty, for example,
16 trying to design a PLL himself or design -- I mean,
17 those are very complicated analog tasks that's far
18 beyond, I think, the normal person's expertise.

19 But -- but yeah, using known components,
20 putting them together, you could generate the clock
21 signal. He would have known that yes, or she.

22 MS. REICHEL: Why don't we take a break.

23 (A recess was taken.)

24 BY MS. REICHEL:

25 Q. Welcome back, Dr. Pedram.

1 A. Thank you.

2 Q. Did you discuss your testimony with counsel
3 at all --

4 A. No, I did not.

5 Q. -- over the break?

6 Dr. Pedram, if you could turn to Figure 1
7 of the '002 patent. Do you see there's an element
8 labeled 110 conditional clock CLK 3 to 0 generator.

9 A. Yes.

10 Q. Does that component relate to the clock
11 generator that you were describing earlier?

12 A. No.

13 Q. What does the '002 patent mean by the label
14 conditional clock generator for element 110 in
15 Figure 1?

16 A. This conditional clock generator takes, as
17 one of its inputs, the clock signal as its other
18 inputs, the four lines coming out of the 2 to 4
19 decoder, 112.

20 Depending on the setting of the signal
21 values on these four lines coming out of the 224
22 decoder, it will selectively apply the clock signal
23 118 to one of the outputs of the conditional clock
24 generator, which is -- which are 124, 126, 128 and
25 130.

1 Q. Is the conditional clock generator doing
2 anything to generate the clock signal?

3 A. No, it's not generating the clock signal.

4 Q. Would a person of ordinary skill in the art
5 have understood that the 2 to 4 decoder labeled 112
6 and the conditional clock generator labeled 110 were
7 separate and distinct circuits in the '002 patent?

8 A. I think a POSA looking at a figure like
9 this would have understood that this is drawn to
10 serve as a functional block diagram describing the
11 major blocks that are needed, functionally, to
12 produce the final wordline driving function into the
13 memory array.

14 I don't think a POSA, and I don't believe a
15 POSA would look at this functional block diagram and
16 conclude that, therefore, the 2 to 4 decoder and the
17 conditional clock generator block have to be
18 implemented as two separate blocks, as such.

19 I mean, maybe in final implementation they
20 would combine them together in some form. But this
21 is, again, serving as a -- a functional block
22 diagram.

23 I mean, my understanding is that,
24 especially for independent claims which is not
25 means-plus-function, this is just telling you what

1 the functionality is, and that's it. There is no
2 structural limitation that you would sort of draw
3 from this particular embodiment that limits the
4 scope of the claim.

5 Q. The person of ordinary skill in the art
6 would not interpret a functional block diagram like
7 what we see in Figure 1 to dictate the actual
8 physical implementation of the circuits, is that
9 what you're saying?

10 A. Yes. But physical implementation, I'm just
11 trying to making sure we be -- again, the term.
12 Physical implementation, I -- I mean the -- the
13 implementation of the logic gates in terms of
14 grouping them into one block or in two different
15 blocks or placing them near each other or apart from
16 each other.

17 So I'm referring to physical layout,
18 placement of components. That's what I meant when I
19 said physical implementation. I agreed with you.

20 So for example, a POSA could take this 2 to
21 4 decoder and sort of put it near the conditional
22 clock generator or far from it. Put it near the 4
23 to 16 decoder or far from it. That -- that's the
24 physical implementation I'm talking of.

25 Q. Could a person of skill in the art have

1 taken the 4 to 16 decoder and the 2 to 4 decoder and
2 implemented them in the same circuit?

3 A. Of course. Everything here is in the same
4 circuit. So the memory array, the group of wordline
5 drivers, the conditional clock generator, all the
6 decoders all are in the same circuit. So I don't
7 understand the question.

8 Q. Dr. Pedram, it's your opinion that the '002
9 patent is limited to applications that you refer to
10 as synchronous clock systems; is that right?

11 A. I think I said synchronous systems, but
12 maybe -- synchronous clock systems. Can you refer
13 me to a part that I use the term "synchronous clock
14 systems"?

15 Q. I'll re-ask the question.

16 Dr. Pedram, it's your opinion that the '002
17 patent is limited to applications you would
18 characterize as synchronous memory systems; correct?

19 A. So again, I'm not here to opine on the
20 scope of the claim. This is a different inquiry.
21 I'm here to render my opinion with respect to
22 certain prior art combinations, whether they render
23 obvious any of the claims of the '002.

24 So I -- I do state clearly that all the
25 embodiments that I see here refer to synchronous

1 systems. There is a clock signal which is a
2 synchronizing signal of fixed periodicity being
3 applied to these systems.

4 So the embodiments are definitely that.
5 And -- but what the scope of the claim is, I mean,
6 it's a different inquiry that I really haven't
7 considered. I mean --

8 Q. You're saying you haven't considered
9 whether the claims of the '002 patent are limited to
10 synchronous memory systems, but only whether the
11 embodiments of the '002 patent depict synchronous
12 memory systems?

13 MR. SAUER: Objection; form.

14 THE WITNESS: Again, this is really not a
15 question I have considered, to define the exact
16 scope of any of the claims with respect to the
17 systems that it covers or it does not cover.

18 And I -- I have construed, in my view, and
19 describe my understanding of what the clock signal
20 is in this context, for example. But I haven't
21 opined on what systems are covered by these claims
22 or not. Just, I haven't done it. That's all I'm
23 saying.

24 MS. REICHEL: Can you please turn to
25 page 62 -- I'm sorry, strike that.

1 Can you please turn to paragraph 62 of your
2 declaration.

3 (The aforementioned document was previously
4 marked Exhibit 2003 for identification by
5 the reporter.)

6 THE WITNESS: Yes.

7 BY MS. REICHEL:

8 Q. On page 26, paragraph 62, of your
9 declaration, you have an image of what you have
10 called a synchronous memory system; is that right?

11 A. And I believe this is from a Ito reference,
12 Exhibit 2003. I don't call it that. I mean, the
13 description here, Figure 6.15 of that reference, it
14 does clearly state that this is a depiction of the
15 synchronous operation of a DRAM chip.

16 Q. You've captioned paragraph 62 by stating
17 that the following diagram illustrates aspects of
18 synchronous memory systems; correct?

19 A. Yes.

20 Q. You believe that this is the same type of
21 memory system that's depicted in Figure 1 of the
22 '002 patent; correct?

23 A. Yes. Conceptually, yes. They are both
24 synchronous memory systems. As I say here, this
25 Figure 6.15 is capturing certain aspects of these

1 memory systems.

2 And then my understanding of Figure 1 of
3 the '002 is that it relates to synchronous memory
4 system with a clock signal that's construed as I
5 have construed it.

6 Q. In Ito Figure 6.15, which you have on
7 page 26 of your declaration, there is a signal
8 labeled Clock CLK --

9 A. Yes.

10 Q. -- that goes into a block labeled CTL. Do
11 you see that?

12 A. Yes.

13 Q. What is CTL?

14 A. I believe it's some kind of clock tree
15 logic. I can't be sure. I -- I have to look at Ito
16 reference. If you -- can I have Ito reference and
17 then --

18 Q. You should have Ito in front of you.

19 A. Yeah.

20 Q. Are you looking at the version of Ito
21 that's labeled Exhibit 2003?

22 Dr. Pedram?

23 A. Yes.

24 Q. I just want to clarify. There are two
25 versions of Ito on the record.

1 A. CTL is control circuit. It's called a
2 control circuit.

3 Q. The control circuit of Figure 6.15 of Ito
4 2003 generates two signals. One is RS1 and one is
5 CS1; is that right?

6 A. Yes.

7 Q. The RS1 signal in Ito Figure 6.15 goes to a
8 circuit labeled XILT; is that right?

9 A. Yes.

10 Q. Is that the row decoding circuit—
11 actually, strike that.

12 What is the XILT block that the RS1 [sic]
13 signal in Ito Figure 6.15 Exhibit 2003 goes to?

14 A. I do not find in the pages of Uita -- Ito
15 reference a clear description of what XILT or YILT
16 is. From the context and the choice of the terms
17 that are used for RS1 and CS1 and where the signals
18 were driven, and those other blocks being called,
19 for example, XI dec, which I would assume is XI
20 decoder and then YI dec, which is some kind of YI
21 decoder, I mean, one -- one would expect that this
22 is something -- that these blocks are something
23 having to do with the processing of the row
24 addresses for the case of XILT and processing of the
25 column addresses for YILT.

1 So the description in Ito is supposed to
2 sort of highlight the differences between
3 synchronous systems of Figure 6.15 and a synchronous
4 systems of Figure 18.

5 So without going into a lot of details with
6 regard to what each of these blocks are at the time
7 of diagram and sort of in a high level conceptual
8 manner, it describes the key differences between the
9 two systems. The description here is not as
10 detailed as one would have liked it to be, but
11 sufficient for our understanding.

12 Q. Ito describes the RS1 signal in Figure 6.15
13 as a row address for a signal; correct?

14 A. That's correct, yes.

15 Q. Ito describes the CS1 signal in Figure 6.15
16 as a column address strobe signal; correct?

17 A. Yes. The signals RS1 and CS1, as you say,
18 power synchronous with the clock signal, as you can
19 see.

20 Q. Which signal in Figure 6.15 would
21 correspond to the clock 118 signal of Figure 1 of
22 the '002 patent?

23 MR. SAUER: Objection; form.

24 THE WITNESS: I haven't really tried to
25 create a correspondence between various elements of

1 this conceptual drawing of the synchronous operation
2 of a DRAM chip diagram with that of the '002.

3 Obviously there are different signals here
4 being used. There is different architecture which
5 is not entirely clear to me even as we speak now.

6 So I -- I can speculate. If you want me, I
7 will speculate, but it's just a speculation because
8 I haven't done the analysis. And the only thing I
9 could say is that what I see here, there is a clock
10 signal, CLK, is synchronous signal coming in of --
11 of a fixed period and frequency as shown here.

12 And therefore, this clock signal would be
13 similar to functioning the same -- perform the same
14 function as the clock signal that I see in '002.

15 BY MS. REICHEL:

16 Q. Are you saying that in implementing the
17 '002 patent, the person of ordinary skill in the art
18 would not have been able to use Ito's control block
19 generating the RS1 clock signal?

20 MR. SAUER: Objection; form.

21 THE WITNESS: I don't know. Hypothetical.
22 How would I know? I mean, I'm not sure what you're
23 asking me. I mean, so are you saying somebody
24 looking at '002 patent saying well, I like some of
25 the ideas here, but let me try to apply them to

1 Ito's systems; or he puts Ito's system in front of
2 himself and says how do I take some of the ideas
3 that they are uniquely described and provide all
4 these great advantages, now to the Ito system and do
5 a reengineering of the Ito system? Can a POSA do it
6 with the description that we talked about in terms
7 of his qualifications? Maybe. I don't know.
8 Maybe. Depends how good the person is.

9 BY MS. REICHEL:

10 Q. Would it be possible for the person of
11 ordinary skill in the art to practice the claims of
12 the '002 patent using Ito's RS1 signal as the clock
13 signal 118?

14 MR. SAUER: Objection; form.

15 THE WITNESS: Again, this is really not
16 something that I've considered. I need time to even
17 think about if it's possible, in what way and what
18 the meaning is. These are architecturally different
19 in terms of implementation of the synchronous
20 operation. Different things.

21 I mean, you even have different blocks. I
22 mean, where do you see a control logic in -- for
23 example, '002 patent, where do you see a separation
24 of so-called XILT and an XI decoder block. It's
25 different.

1 I'm not saying this means that the system
2 that Ito describes is not synchronous DRAM. It is.
3 As it is for the '002, is synchronous design of the
4 memory in that figure. But the combination you're
5 asking me, I don't know. I really don't want to
6 speculate. It's hard question you're asking. I
7 don't know.

8 BY MS. REICHEL:

9 Q. Would a person of ordinary skill in the art
10 have been able to implement an embodiment of the
11 '002 patent that included a clock gating feature?

12 A. What is a clock gating feature? Meaning
13 that -- where? I guess I want you to be more
14 explicit. So I'm looking at -- I think -- set aside
15 general -- general hypotheticals.

16 Q. So let me --

17 A. So I'm looking at Figure 1. I'm sorry.
18 Figure 1 of '002. What are you precisely suggesting
19 whether a POSA can or cannot do?

20 Q. Let me back up because you asked for a
21 better question.

22 A. Yes.

23 Q. Do you see that Ito's Figure 6.15 includes
24 a chip select signal?

25 A. Yes.

1 Q. What is that chip select signal?

2 A. So typically, if the DRAM device, this
3 memory array is not selected, you don't want to sort
4 of activate the circuitry, you would show that the
5 DRAM device is not being selected, used, and,
6 therefore, do whatever you like to do. You're
7 telling the memory device do whatever you like to
8 do.

9 And typically, in these cases, memory
10 devices go into some kind of standby or lazy power
11 down state to reduce leakage power consumption.

12 Q. Can the chip select signal in 6.15 of Ito
13 be used to implement a clock gating functionality?

14 MR. SAUER: Objection; form.

15 THE WITNESS: In what way? Certainly, Ito
16 himself has no description of any kind of clock
17 gating being used here. Clock gating is a complex
18 process when it's applied to a DRAM chip because, as
19 you know, it's very important for DRAM chips to be
20 able to respond quickly to a memory request.

21 If you do clock gating without a lot of
22 care, a lot of problems could arise in terms of
23 performance. If you don't do clock gating
24 carefully, you might even disable the refresh cycles
25 of a DRAM chip, lose the contents of the data which

1 is stored in DRAM, which is a destructive process
2 that should be totally avoided.

3 So it can be done, but Ito has no teachings
4 of that nature. And generally, applying clock
5 gating to a DRAM device is -- is a very complex
6 task.

7 BY MS. REICHEL:

8 Q. Do you agree that when the chip select
9 signal in Figure 6.15 of Ito is high, the RS1 and
10 CS1 signals are both shown to be low?

11 A. Yes. When CS bar signal is high in the
12 drawing of Figure 6.15, both RS1 and CS1 are low.

13 Q. Is it possible to practice the claims of
14 the '002 patent using a chip select enable signal,
15 like what we see in Ito?

16 MR. SAUER: Objection; form.

17 THE WITNESS: I've not considered that
18 question.

19 BY MS. REICHEL:

20 Q. You haven't considered whether it's
21 possible to practice the claims of the '002 patent
22 using Ito's RS signal as the clock signal of the
23 '002 patent?

24 MR. SAUER: Objection; form.

25 THE WITNESS: Of course not. I was not

1 asked to do it. The -- the Apple expert never
2 presented anything like this as a potential
3 obviousness combination.

4 I just did what I was asked to do, which is
5 look at the obviousness combinations that I've been
6 presented to -- to me, in view of the claims, the
7 specifications and appropriate claim constructions
8 and opine. And that's what I did. I did not do
9 anything beyond that.

10 BY MS. REICHEL:

11 Q. Do you have an opinion as to whether it is
12 possible to practice the claims of the '002 patent
13 with a DRAM memory?

14 MR. SAUER: Objection; form.

15 THE WITNESS: Again, I'm not here to opine
16 on the scope of the claim, and I really haven't
17 considered it for the purpose of this particular
18 inquiry.

19 Whether the claims of '002 are limited to
20 SRAM, static RAM devices, or do they also cover
21 dynamic RAM devices, I just haven't considered it.
22 I don't see anything in the claims that excludes any
23 of this, but I haven't considered that question.

24 BY MS. REICHEL:

25 Q. Is it possible to practice the claims of

1 the '002 patent using a synchronous memory system?

2 MR. SAUER: Objection; form.

3 THE WITNESS: I believe you asked the
4 question before, and it's not a question I have
5 considered.

6 BY MS. REICHEL:

7 Q. Are the claims of the '002 patent limited
8 to any particular voltage levels?

9 A. I don't believe so, no.

10 Q. How would the person of ordinary skill in
11 the art determine what voltage levels should be used
12 in practicing the '002 patent claims?

13 MR. SAUER: Objection; form.

14 THE WITNESS: First of all, what voltage
15 levels are we talking about?

16 BY MS. REICHEL:

17 Q. How would the person of ordinary skill in
18 the art determine what voltage levels should be used
19 in practicing the '002 patent?

20 A. I really don't know what that --

21 MR. SAUER: Objection; form.

22 THE WITNESS: Again, please give me better
23 questions.

24 So I'm looking at Figure 1. I see in
25 Figure 1 multiple blocks and a memory array. What

1 are these voltage levels you're talking about? Are
2 you talking about the voltage levels -- supply
3 voltage levels of the decoders? Are you talking
4 about the supply voltage levels of the group of
5 wordline drivers? Are you talking about the supply
6 voltage level that the memory array itself uses?

7 I mean, it's not clear. And none of this
8 has been specified, I agree with you, in the '002,
9 because it was -- the patent owner's inventors felt
10 it was not necessary for them to limit their
11 invention to any particular set of voltages for the
12 memory array or for the wordline drivers or for the
13 decoders, and so on, so forth.

14 But when you ask me this question, what are
15 you asking me precisely? All of the voltage levels?
16 Some of them? One of them?

17 BY MS. REICHEL:

18 Q. Would the person of ordinary skill in the
19 art be able to determine what voltage level should
20 be used for the decoders and the wordline driver and
21 all the other components --

22 MR. SAUER: Objection; form.

23 BY MS. REICHEL:

24 Q. -- in the '002 patent?

25 A. I guess a person of ordinary skill in the

1 art would come across, from having read the '002
2 invention, as teaching a particular way of reducing
3 the load on a clock signal to achieve power savings,
4 to be able to do all decoding in a -- in an
5 efficient way as a result.

6 And I don't think he or she would have come
7 across -- come away from reading this as a way of
8 deciding about the specific voltage levels that a
9 memory array, for example, should use. These are
10 complicated, truly complicated tasks, problems to
11 address because it has to do with the technology of
12 the memory device.

13 For example, if it's a DRAM: What kind of
14 capacitor technology you use; what kind of
15 transistors you have; what kind of technology mode
16 you are operating at; what's the maximum baked on
17 voltage of your devices; what's the leakage through
18 your turned off transistors; what's the duration of
19 the refresh cycle you would like to have; what kind
20 of dynamic power consumption versus leakage power
21 consumption straight off you want to create; what
22 kind of access speed you want to have.

23 Many, many, many, many factors. And then
24 as a result, by doing a simulation or study or using
25 legacy knowledge that exists in the company,

1 consulting with senior colleagues and designers,
2 come up with something for these voltages. It's
3 not, in any way, a -- a straightforward trivial
4 task. And it's not something that's taught in '002.

5 Q. Are there any IEEE standards that define
6 the type of voltage levels that should be used in
7 the system that is shown in Figure 1 of the '002
8 patent?

9 MR. SAUER: Objection; form.

10 THE WITNESS: I'm not aware of any. And
11 there shouldn't be any, but --

12 BY MS. REICHEL:

13 Q. Do you agree that the '002 patent does not
14 teach any particular circuitry to implement the 4 to
15 16 decoder labeled 108 in Figure 1?

16 A. Yes.

17 Q. Would a person of ordinary skill in the
18 art, as of October 10, 2006, have known different
19 ways that the 4 to 16 decoder shown as element 108
20 could be implemented?

21 A. I think so, yes.

22 Q. Do you agree that the '002 patent does not
23 teach any particular circuitry to implement the 2 to
24 4 decoder labeled 112 in Figure 1?

25 A. Yes.

1 Q. Would a person of ordinary skill in the
2 art, as of October 10, 2006, have known different
3 ways that the 2 to 4 decoder 112 could be
4 implemented?

5 A. Yes.

6 Q. How would the person of ordinary skill in
7 the art understand how those two decoders should be
8 implemented?

9 A. I'm not sure how to answer the "how" part
10 of your question. Please re-ask the question in a
11 different way.

12 Q. Sure. Sorry.

13 What is your basis for your opinion that a
14 person of ordinary skill in the art would have
15 understood how to implement the decoder in the '002
16 patent?

17 A. A decoder such as 4 to 16 decoder has a
18 very well-defined behavior once you know what the
19 code is that you're using. For example, if you
20 decide the code you want to use is one-hot code,
21 then the Boolean function that describes the mapping
22 from input to outputs would be known.

23 Having known the Boolean function mapping
24 from inputs to outputs, then it's a matter of
25 putting together the logic gates, AND gate, OR

1 gates, inverters or what have you, to create a
2 realization of the multi-input, multi-output Boolean
3 logic.

4 And that's something a POSA would know at
5 that time, subject to the coding scheme, as I said
6 before.

7 Q. Can you please turn to Apple Exhibit 1007,
8 which is another excerpt from the Ito textbook.

9 A. Yes.

10 Q. And please turn to what is page 147 of the
11 textbook, and page 115 of the exhibit itself.

12 A. Yes.

13 Q. Does Figure 3.46 on page 147 of the Ito
14 textbook depict some of the standard and known
15 decoding mechanisms?

16 A. I'm sorry. I missed the page number, the
17 last page number and Figure number.

18 Q. Can you please turn to what is the textbook
19 page 147, labeled at the top of the page, but is
20 page 15 --

21 A. Yes.

22 Q. -- labeled on the bottom of the page of
23 Apple Exhibit 1007.

24 A. Yes.

25 Q. Do you see that in Figure 3.46, Ito sets

1 forth various decoding mechanisms?

2 A. Yes.

3 Q. Does --

4 A. I see that, yeah.

5 Q. Does Figure 3.46 depict decoding mechanisms
6 that the person of ordinary skill in the art would
7 have understood could be used in the decoders of the
8 '002 patent?

9 A. I believe so. Yes. So these are some of
10 the methods as described here, but as I've indicated
11 before, there are other ways of doing it also.
12 Yeah, sure.

13 Q. The methods shown in Figure 2.46 of Ito
14 were known to persons of ordinary skill in the art
15 prior to October 10, 2006; correct?

16 A. So how to do decoding is known. The fact
17 that you do decoding in one step or in multiple
18 steps is also known. Exactly how to do it to
19 achieve particular tradeoff, I don't know if a POSA
20 would know how to do that part. Perhaps not.

21 But certainly, the actual decoding process
22 itself and the fact that the decoding could be done
23 in a single shot, as I say it, or multiple steps,
24 would be known, yes.

25 Q. Do you agree that the Ito textbook is prior

1 art to the '002 patent?

2 A. Yes, I do.

3 Q. Do you have an opinion about whether the
4 claims of the '002 patent are limited to a specific
5 type of memory cell, for example, a 6T or a 4T SRAM
6 cell?

7 MR. SAUER: Objection.

8 THE WITNESS: There's no such description
9 in the '002, either in of the embodiments that I
10 see, or in any of the claims. There is no
11 limitation about the type of the memory element
12 itself. Whether it's a one transistor DRAM cell or
13 if it's 6 transistor SRAM cell or four transistor
14 cell. There's no such limitation, whatsoever, and
15 there're no such disclosure one way or the other in
16 '002.

17 BY MS. REICHEL:

18 Q. Do you agree that it would be necessary to
19 refresh the output of the 4 to 16 decoder in
20 Figure 1 of the '002 patent?

21 A. Refresh? What's the meaning of refresh?

22 Q. You don't have an understanding of what
23 that word means?

24 A. No, in this context. I never heard the
25 term "refresh" used in the context of a decoding

1 context. Refresh is used in the context of the
2 memory array itself. You refresh the memory, if
3 it's DRAM, type to not lose the content, the data.
4 But refresh in the context of a decoder, never heard
5 of it. No.

6 Q. Would the memory system in Figure 1 of the
7 '002 patent function if the output of the 4 to 16
8 decoder never changed?

9 A. Yes, it would function. Why would it not
10 function? It just doesn't produce any new results
11 for you, but it functions. You could have a
12 perfectly operational chip set in there and the
13 value of the address, it don't ever change or change
14 infrequently. Still functions perfectly well, it's
15 just not being used.

16 Q. In order to use the memory system in
17 Figure 1 of the '002 patent, is it necessary to
18 change the output of the 4 to 16 decoder?

19 A. Use it in the sense to access different
20 data values stored in the memory array, yes.
21 Because, again, imagine a case in which you're going
22 to the memory always asking for the same value.
23 You're not going to change the address. It's always
24 the same. But assuming that -- I'm trying to be
25 helpful -- assuming that you want to go to different

1 memory locations, yes.

2 Q. How would a person of ordinary skill in the
3 art have known how to change the output of the 4 to
4 16 decoder in Figure 1 of the '002 patent?

5 A. When different memory addresses come in --
6 for example, in Figure 1, if I'm going from one
7 memory location with a specific combination of 01
8 values for bits 5 to 2, to a different memory
9 location where the -- this portion of the memory
10 address 5 to 2 changed, then obviously the output of
11 the 4 to 16 decoder would change.

12 Q. How would the output of the 4 to 16 decoder
13 change?

14 A. The bit pattern, which is a 16 entry bit
15 factor, would change. I mean, again, 0 and 1
16 positions would change.

17 Q. A person of ordinary skill in the art would
18 have understood how to build a decoder where the
19 output will change when the input address bits
20 change?

21 A. Yes.

22 Q. Is it possible to practice the claims of
23 the '002 patent with a system where the clock signal
24 is also provided to the 4 to 16 decoder in Figure 1
25 of the '002 patent?

1 MR. SAUER: Objection; form.

2 THE WITNESS: I haven't considered that
3 question because it's not something that I was asked
4 to do.

5 BY MS. REICHEL:

6 Q. Which claim element, in your opinion, does
7 the 4 to 16 decoder of Figure 1 correspond to in
8 claim 1 of the '002 patent?

9 MR. SAUER: Objection; form.

10 THE WITNESS: There are many claims, so I
11 guess let's focus on one of the claims. Right? So
12 claim 1.

13 BY MS. REICHEL:

14 Q. I specified said claim 1.

15 A. Yeah, yeah. I missed that.

16 It would be the limitation that starts with
17 second logic to decode a second portion of the
18 memory address. The second logic to selectively
19 activate a particular wordline driver of the
20 selected group of wordline drivers according to the
21 second portion of the memory address.

22 Q. Is there anything in claim 1 of the '002
23 patent that precludes the clock signal from being
24 provided to the second logic?

25 A. The claim -- there is no such limitation in

1 the -- in claim 1.

2 Q. Are you aware of any limitation in any of
3 the claims in the '002 patent that precludes the
4 provision of a clock signal to the second logic?

5 A. Not that I remember, no.

6 Q. Which claim element of claim 1 corresponds
7 to the 2 to 4 decoder in Figure 1 of the '002
8 patent?

9 A. So I understand the term "corresponds to"
10 to mean that when I try to identify elements in
11 the -- one of the preferred embodiments of this
12 patent, which is this Figure 1, then what -- which
13 of the blocks in Figure 1 meet this particular
14 limitation of the claim 1.

15 So having said that, the 4 to -- I'm
16 sorry -- the 2 to 4 decoder would be sort of part of
17 the revealed functional block diagram in Figure 1.
18 That would read, "The first logic to receive a clock
19 signal and a first portion of a memory address of a
20 memory array, the first logic to decode the first
21 portion of the memory address and to apply the clock
22 signal to a selected clock output of a plurality of
23 clock outputs associated with a selected group of a
24 plurality of wordline drivers that are associated
25 with the memory array; and second logic to decode a

1 second portion of the memory address, the second
2 logic to selectively activate a particular wordline
3 driver of the selected group of wordline drivers
4 according to the second portion of the memory
5 address."

6 It's a part of the set of blocks that read
7 on this particular limitation.

8 Q. Which claim element of claim 1 corresponds
9 to the conditional clock generator in Figure 1 of
10 the '002 patent?

11 MR. SAUER: Objection; form.

12 THE WITNESS: So claim 1, which is a
13 general claim that goes beyond any specific
14 embodiment such as Figure 1, does mention that as
15 part of this limitation, the first logic receives a
16 clock signal and a first portion of a memory
17 address, and that decodes the first portion of the
18 memory address and then applies the clock signal to
19 a selected clock outputs.

20 And so the conditional clock generator that
21 you're mentioning here is affecting the process of
22 applying the clock signal to a selected clock output
23 in combination, of course, with the decoding of the
24 first portion of the memory address.

25 ///

1 BY MS. REICHEL:

2 Q. Is the conditional clock generator in
3 Figure 1 of the '002 patent part of the first logic
4 in claim 1 of the '002 patent?

5 A. Yeah. If I'm trying to, again, identify
6 the blocks in this embodiment of Figure 1 that
7 performed the required functions of that particular
8 limitation, obviously the conditional clock
9 generator that we have is the element that's
10 assisting, effecting, in fact, the application of
11 the clock signal to a selected clock output as
12 required in this limitation.

13 Q. Is the conditional clock generator in
14 Figure 1 of the '002 patent part of the first logic
15 in claim 1 of the '002 patent?

16 MR. SAUER: Objection; form.

17 THE WITNESS: Yes. I think the conditional
18 power generator, if I were to map it back to the
19 language of the claim, would probably be mapped --
20 not probably, will be mapped to something that falls
21 under first logic.

22 BY MS. REICHEL:

23 Q. In your opinion, does the claim term "clock
24 signal" in the '002 patent have a particularized
25 meaning set forth in a specification of the '002

1 patent, or is that term to be understood according
2 to its plain and ordinary meaning to an person of
3 ordinary skill in the art?

4 A. So having looked at the specification, the
5 embodiments, the claim language, it is my opinion
6 that a POSA looking at this patent would understand
7 the clock to be a periodic signal of fixed frequency
8 used for synchronization purposes in the context of
9 this memory system.

10 Q. Is it your opinion that the '002 patent set
11 forth a specialized definition of clock signal that
12 corresponds to the definition you just gave, or is
13 your definition intended to capture the plain and
14 ordinary meaning of the plain term "clock signal"?

15 MR. SAUER: Objection; form.

16 THE WITNESS: I'm applying the broadest
17 reasonable interpretation here, in my view, with
18 the -- when you look at the totality of this claim,
19 the specification of this patent, the claim language
20 and all the embodiments, a POSA looking at this
21 would have concluded that this clock is a periodic
22 pulse stream coming in to provide synchronization
23 within this memory system.

24 That's also consistent with the standard
25 definition of a clock signal. And that's what a

1 POSA would have concluded having looked at the
2 specification.

3 BY MS. REICHEL:

4 Q. Is there any place in the specification of
5 the '002 patent where you believe the inventors have
6 set forth a particular definition of the term "clock
7 signal"?

8 A. I have not seen in the '002 patent a
9 precise definition of the clock. And the reason, as
10 I explained also in my report at length, is because
11 the patent owners, the inventors, felt like a person
12 of ordinary skill in the art would understand what a
13 clock signal is in the context of memory systems.

14 A clock signal is a periodic pulse stream
15 used for synchronization purposes. So they didn't
16 feel they have to redefine what should be known and
17 is known of the person skilled in the arts.

18 MS. REICHEL: Why don't we take a break for
19 lunch.

20 (At the hour of 12:15 p.m., a
21 luncheon recess was taken, the
22 deposition to be resumed at 12:51
23 p.m.)

24 ///

25 ///

1 LOS ANGELES, CALIFORNIA; FRIDAY, JUNE 6, 2019

2 12:51 P.M.

3 -000-

4 ***

5 MASSOUD PEDRAM,

6 having been previously administered an

7 oath in accordance with CCP 2094, was

8 examined and testified as follows:

9 ***

10 EXAMINATION (Resumed)

11 BY MS. REICHEL:

12 Q. Welcome back, Dr. Pedram.

13 A. Thank you. It's good to be back.

14 Q. Did you discuss any of your testimony with
15 Counsel over the break?

16 A. No, I did not.

17 MS. REICHEL: Can you please pull up Apple
18 Exhibit 1012, the Sugio patent?

19 (The aforementioned document was
20 previously marked Exhibit 1012 for
21 identification by the reporter.)

22 THE WITNESS: Yes, I have it.

23 BY MS. REICHEL:

24 Q. Please turn to Figure 2.

25 A. Yes.

1 Q. Do you see, in Figure 2 of the Sugio
2 patent, there's a block labeled 1 that is called a
3 timing control circuit?

4 A. Yes, I see it.

5 Q. Do you see that the output of the timing
6 control circuits in Sugio are labeled S1?

7 A. Okay. Yes.

8 Q. Are the S1 signals in Sugio clock signals?

9 A. No. As I -- the clock signal, I think, is
10 CK signal, no?

11 Q. (No audible response.)

12 A. Let me -- please allow me time to read the
13 specs again, remind myself.

14 I -- I confirm my previous answer. CK is
15 the clock signal here, and S1s are the outputs of
16 the timing control circuit.

17 Q. It's your opinion that the S1 signals do
18 not meet your definition of clock signal; correct?

19 A. I -- I haven't analyzed the S1 signals. To
20 answer the question, I have to go back and remind
21 myself. But just looking at this timing diagram and
22 the description that Sugio has, he calls CK to be
23 the clock signal, and this is also being a DRAM.
24 This is the external clock signal, probably being
25 provided to the DRAM array.

1 These S1 signals are the outputs of the
2 timing control circuit, as I see it. And I don't
3 know their characteristics and -- and so on, because
4 I have a definition for clock signal, right. So my
5 definition of clock signal, construction of the
6 clock signal, the periodic signal with fixed
7 frequency, and used for synchronization purposes.

8 So I have to answer your question in view
9 of that construction. And again, off the top of my
10 head, I cannot answer the question whether any of
11 these S1 signals -- or S1 signals meets that
12 construction or not.

13 My -- my -- my, I guess, definition of a
14 clock is not based on the fact that a signal is
15 called CK or called S1 or this or that. It's just
16 whether it meets my limitation -- I should say, my
17 construction of the definition for the clock signal.

18 Q. Sitting here today, you don't know one way
19 or the other whether the S1 signals in Sugio meet
20 your definition of clock signal?

21 A. I have not done the analysis. I can do it
22 if you want to -- if you want me to do it. I'm not
23 hesitant to do it. I'll just read through this more
24 carefully, look at the -- any timing diagrams or any
25 description of the S1 signals, and then I would

1 know.

2 Q. You haven't done that prior to today's
3 deposition?

4 A. I haven't considered that question. It was
5 not presented to me. Nobody brought it up in that
6 way to me, so I haven't answered that question.

7 Q. Can you turn back to the '002 patent.

8 A. Yes.

9 Q. In Figure 1 of the '002 patent, there are
10 four signals labeled 124, 126, 128 and 130.

11 These are outputs of the conditional clock
12 generator 110; correct?

13 A. Yes.

14 Q. Are signals 124, 126, 128 and 130 clock
15 signals?

16 A. They are what the patent says. They are
17 conditional clock signals. These are outputs of
18 this generator. So that's the description.

19 Q. In your opinion, are signals 124, 126, 128
20 and 130 clock signals as you have defined that term?

21 A. In general, no, because a clock signal, in
22 my definition, would have fixed periodicity. You
23 see a fixed stream, constant stream of zero and ones
24 coming in with fixed interval in between, always
25 running, continuously running, and used for

1 synchronization purposes.

2 I don't believe, in general, any of these
3 signals which are called conditional clock signals,
4 I guess. We could call them that way because they
5 are the outputs of the conditional clock generator.
6 None of these signals, 124, 126, 128, 130 meet that
7 definition.

8 Q. Dr. Pedram, can you please pull out your
9 declaration, Exhibit 2001.

10 A. Yes.

11 Q. Can you please turn to Page 50,
12 paragraph 110.

13 A. Yes.

14 Q. In paragraph 110 of your declaration, you
15 have a discussion about a reference called the Sato
16 reference; correct?

17 A. Yes.

18 Q. In this paragraph, you describe something
19 called a race condition.

20 Do you see that?

21 A. Yeah, I see the phrase "race condition,"
22 but I have to read through the paragraph to remind
23 myself the context. I would also like to look at
24 the Sato's reference. I believe it's in front of
25 me, but I need to take a look, the reference as well

1 as this paragraph.

2 MS. REICHEL: While you do that, I'll note
3 for the record that the Sato reference, which is in
4 front of you, is Exhibit Apple 1005.

5 (The aforementioned documents were
6 previously marked Exhibits 1005,
7 1006, 1007 and 1008 for
8 identification by the reporter.)

9 BY MS. REICHEL:

10 Q. Please let me know when you have refreshed
11 yourself and I will re-ask my question.

12 A. Yes, thank you.

13 Okay. I'm ready.

14 Q. In the paragraph 110 of your declaration
15 you refer to something called a race condition.

16 Do you see that?

17 A. Yes.

18 Q. What do you mean by race condition?

19 A. So basically, generally, when I speak of
20 race conditions, it means that, depending on the
21 precise timing of different elements on -- on paths
22 that converge to the same node, you might have
23 observed different behavior. Sometimes one path
24 will be faster than the other path, and therefore
25 you see an outcome and then -- even if it's a

1 transient outcome. It could be a temporary outcome.

2 But because of the -- having different
3 delays that are different across different paths
4 that converge together, you could see either
5 non-deterministic behavior, or if it is
6 deterministic behavior, you see some kind of hazard
7 activity on the line. Some hazard shows up.

8 A hazard means if your correct value is
9 zero, you go to 1 first and then come back to zero.
10 That's unwanted activity, because the correct value
11 was zero. If you're at zero, you should stay at
12 zero, because that's the correct next value. But
13 you make this unwanted transition to 1 and come back
14 down to zero.

15 And sometimes this is just an error you
16 could ignore. But many times, especially for memory
17 for driving things, trying to read them, this could
18 be a significant error.

19 Q. Is it your opinion that Sato teaches a
20 circuit that can result in a race condition?

21 A. No, ma'am, that's not what I've said. I
22 mean, the point I'm making in this paragraph is that
23 if I take Sato's design and remove the clock from
24 NAGO to NAGK, and instead of implementing them using
25 the pre-charge evaluate logic style, as Sato has

1 suggested, replace them with static logic NAND gates
2 that do not receive or require a clock -- a timing
3 signal, PHI-CE timing signal, then this circuit with
4 the change that I just discussed would have a
5 problem, a serious problem.

6 Q. Which claim element in the '002 patent do
7 you believe requires static NAND gates?

8 MR. SAUER: Objection; form.

9 THE WITNESS: This is not -- no claims that
10 I know requires static NAND gates. No limitation of
11 any claims requires a static NAND gates to be used
12 as part of any first logic or second logic.

13 The point I'm making here, and maybe that's
14 the source of the confusion and the -- some of the
15 questions I'm getting, is that there a statement
16 that the PHI-CE signal performs the same function as
17 the clock signal in the '002 patent. And I'm
18 disagreeing with that, saying, well, when I look at
19 the preferred embodiment of the '002 patent, for
20 example, Figure 1, or when you go into details of
21 the wordline drivers and so all the other figures,
22 you will see that -- that the clock signal in those
23 embodiments functions differently than the -- this
24 timing control signal PHI-CE.

25 And I have multiple grounds for this

1 statement, but one of them is the fact that, well,
2 the clock signal that I see in '002 does not go to
3 the 4-to-16 decoder. And so -- implication being
4 that the 4-to-16 decoder is going to be implemented
5 as static logic independent of any clock signal,
6 whereas what the petitioner has identified as second
7 logic block in Figure 1 or 3 of the Sato reference,
8 which refers to this NAGO, NAGK, I can clearly see
9 that there's a timing control signal PHI-CE going to
10 those things.

11 And this timing critical signal is actually
12 critical to the performance. If you take out this
13 PHI-CE and use any PHI-CE independent realization,
14 no pre-charge evaluate the static logic, Sato's
15 design would have failed.

16 So PHI-CE of Sato is absolutely required
17 for the correct functionality of his so-called -- I
18 don't know -- his NAG decoders, NAGO through NAGK,
19 which have been identified as a part of the second
20 logic, whereas I don't see anything like this
21 required, performed, implied by the preferred
22 embodiment of Figure 1 of the '002. That's the
23 point I'm making.

24 BY MS. REICHEL:

25 Q. Just to make sure I understand, your

1 discussion beginning at paragraph 110 of your
2 declaration compared Sato's Figure 3 to an
3 embodiment of the '002 patent, and not to the full
4 claims scope of the '002 patent; right?

5 MR. SAUER: Objection; form.

6 THE WITNESS: So again, I -- I'm not here
7 to opine on the scope of the claims, right. The --
8 obviously, every one of the embodiments of the '002
9 reads on the claims, right, and is consistent with
10 those claims.

11 So I'm simply answering the -- or
12 responding to the statement by the petitioner that
13 somehow the Sato's selection control signal PHI-CE
14 performs the same function as the clock signal in
15 the '002 patent.

16 And I'm -- you know, I have multiple
17 grounds for rejecting this statement. This is one
18 of the grounds on which I'm disagreeing. And the
19 ground here is, when I look at the -- the preferred
20 embodiment of Figure 1 of the '002 and compare it to
21 Figure 1, 3, in combination, of Sato, clearly the
22 function performed by the control signal PHI-CE is
23 different than the function that's performed by the
24 clock signal, even if I set aside different set with
25 respect to periodicity or synchronization or this

1 and that, and just focus on where these -- this
2 PHI-CE signal goes, what components it drives, how
3 essential it is to the functionality of those
4 components, so on, so forth. That's all I'm saying.

5 Q. Okay. Again, you're comparing Sato
6 Figure 3 to the embodiments of the '002 patent --

7 MR. SAUER: Objection; asked and answered.

8 BY MS. REICHEL:

9 Q. -- correct?

10 A. I'm -- in -- so this -- the -- that's not
11 been my intention to only compare it to that
12 embodiment. I'm just saying the statement that it
13 performs the same function of -- as the clock
14 signal, I have to add a context in which I want to
15 answer the question, whether this statement is
16 accurate or not.

17 As the context, I chose the preferred
18 embodiment of Figure 1 of '002. And I see clear
19 differences with respect to where the clock signal
20 goes, what it does with respect to the first logic
21 or the second logic of the -- this embodiment that
22 I've focused on versus what happens with respect to
23 Sato Figure 1, 3 and his control signal PHI-CE.

24 Q. You state in paragraph 110 of your
25 declaration (reading):

1 "A race condition leading to a
2 complete breakdown of circuit
3 functionality can result if the
4 NAND gate circuits NAGO to NAGK do
5 not receive the selection control
6 signal PHI-CE. "

7 A. Yes.

8 Q. Have you performed any simulations or other
9 analysis to confirm whether or not a race condition
10 actually would result from that circumstance?

11 A. No, I've done analysis only.

12 Q. You don't have any simulations relating to
13 the '002 patent or any of the prior art references
14 in your declaration; correct?

15 A. No, I do not.

16 Q. In paragraph 112 of your declaration, you
17 refer to an unwanted hazard activity that can
18 subsequently result in creating a voltage
19 differential between a selected bit line.

20 Do you see that?

21 A. Yeah.

22 Q. Have you done any analysis to determine
23 whether or how frequently that result would occur?

24 A. Yes, I've done the analysis to answer the
25 question of whether it happens or not. Clearly,

1 definitely, it can happen. That analysis, I'm
2 confident of.

3 The question of how frequently it can
4 happen, no, I have not particularly done that. But,
5 again, these circuits drawn at very high
6 frequencies, even if this kind of event happens once
7 every billion times, a billion times' access to this
8 is probably just one second. So if the circuit will
9 fail once every second, imagine your cell phone
10 would reboot every one second, right, a cell phone
11 that's using this kind of memory device.

12 So generally, if you have any kind of
13 potential problem like this, you find it -- design
14 around it, do something about it. You change it.
15 You don't adopt that solution, you switch to a
16 different solution.

17 Q. A person of ordinary skill in the art would
18 have been able to design around this problem to
19 arrive at a different solution?

20 A. Not according to our definition of POSA. I
21 mean, this is a complicated problem. If you present
22 these kind of race conditions, these are some of the
23 most difficult problems to deal with, seriously. I
24 mean, to identify them, to track them down, to fix
25 them. That's why people who --

1 Sometimes these race conditions, with
2 respect to certain elements, are called hold -- hold
3 violations. So if you get these kind of race
4 conditions or hold violations, there's no fix. The
5 chip has to be thrown away.

6 So people who do the design, they do so
7 called six-sigma margin around it, whereas with
8 respect to setup time, failures, long path, delay
9 constraint, violations, you only do three-sigma
10 margin around it.

11 So the significance of six sigma is,
12 according to a normal distribution, when you're sure
13 that mean plus minus six sigma, you're okay. The
14 population size that shows up outside that is, I
15 believe, less than 300ths of 1 percent or 3,000ths
16 of 1 percent, something like this. Very, very, very
17 small population of chips would be bad and you throw
18 them away. But you would throw them away.

19 Q. You haven't simulated how frequently,
20 thought, this type of condition might occur?

21 A. No, I have not.

22 Q. Dr. Pedram, have you discussed with your
23 counsel any potential redirect testimony for today's
24 deposition?

25 A. Oh, no.

1 Q. Have you testified truthfully and
2 accurately here today?

3 A. Yes.

4 MS. REICHEL: I have no further questions.

5 MR. SAUER: No questions for me.

6 THE WITNESS: Thank you.

7 (The deposition proceedings were
8 concluded at 1:17 p.m.)

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CERTIFICATE OF DEPONENT

I hereby certify that I have read the foregoing pages of my deposition testimony in this proceeding, and with the exception of changes and/or corrections, if any, find them to be a true and correct transcription thereof.

Deponent

Date

NOTARY PUBLIC

Subscribed and sworn to before me this

_____ day of _____, 20____.

Notary Republic

My Commission Expires:_____

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2

3 Please read your deposition over carefully
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6 space on the errata sheet for any corrections
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9 After doing so, please sign the errata
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21 transcript may be deemed to be accurate
22 and may be used in court.

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1 CERTIFICATE OF REPORTER

2 I, DORIEN SAITO, CSR 12568, CLR, a certified
3 Shorthand reporter in and for the State of
4 California, County of Los Angeles, do hereby
5 certify;

6 That MASSOUD PEDRAM, PH.D., the witness
7 named in the foregoing deposition, was, before the
8 commencement of the deposition, duly administered an
9 oath in accordance with CCP 2094;

10 That said deposition was taken down in
11 stenograph writing by me and thereafter transcribed
12 into typewriting under my direction.

13 That before completion of the deposition,
14 review of the transcript [] was [X] was not
15 requested. If requested any changes made by the
16 deponent (and provided to the reporter) during the
17 period allowed are appended hereto.

18 I further certify that I am neither counsel
19 for nor related to any party to said action, nor in
20 any way interested in the outcome thereof.

21 Dated this 19th day of June, 2019.

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25 IN AND FOR THE COUNTY OF LOS ANGELES, STATE OF CALIFORNIA