

Apple, Inc. (Petitioner)
v.
Qualcomm Incorporated (Patent Owner)
Petitioner Demonstratives

Case No. IPR2018-01249
U.S. Patent No. 7,693,002

Before Hon. Trevor M. Jefferson, Daniel J. Galligan, and Scott B. Howard
Administrative Patent Judges

FISH.

Issues

- Challenged '002 Patent
- Issue 1: Whether Asano/Itoh Combination Teaches distinct “first” and “second logic”
- Issue 2: Whether Patent Owner’s Construction of “Clock Signal” is Improper
- Issue 3: Whether Sato Renders the '002 Patent Claims Obvious

Challenged '002 Patent

'002 Overview

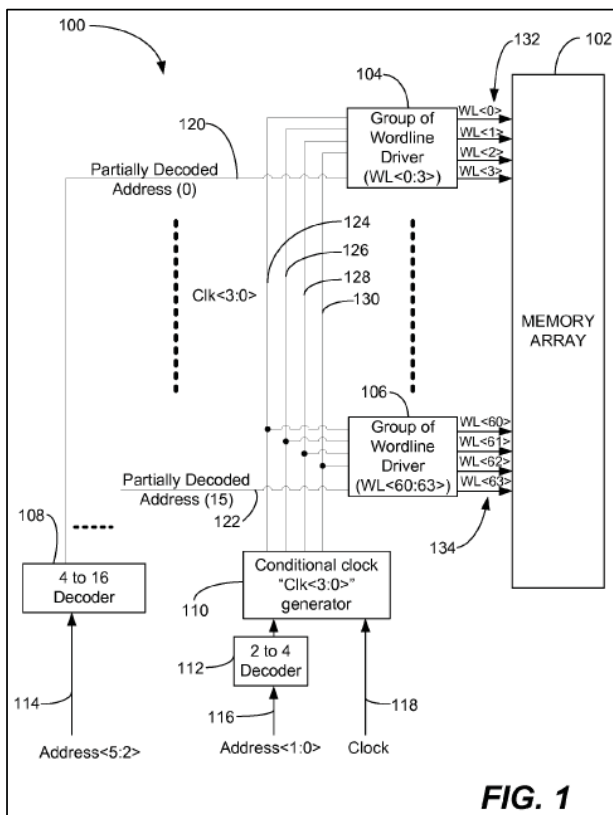


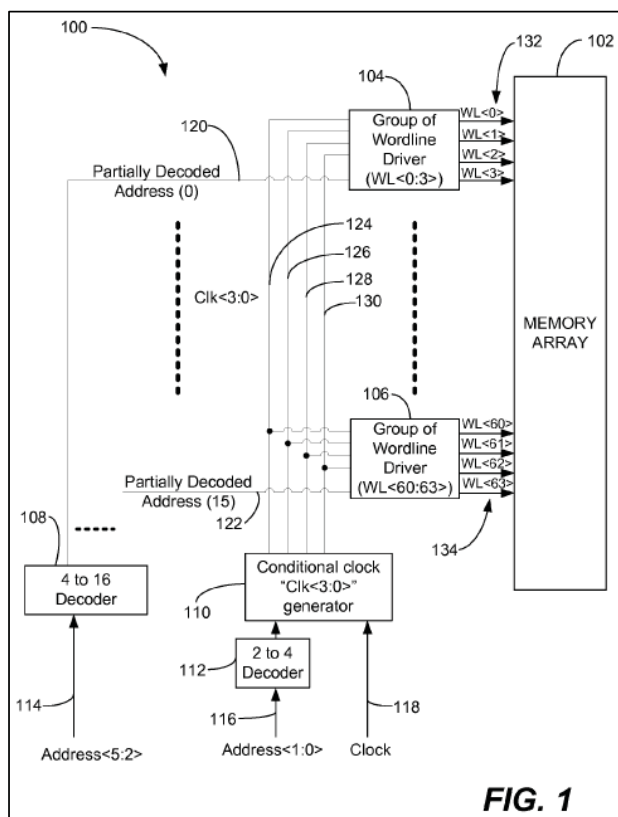
FIG. 1

'002 Patent (APPLE-1001), FIG. 1.

- U.S. Patent No. 7,693,002 (“the ’002 patent”) includes 38 claims, of which claims 1, 7, 11, 17, 21, 23, 24, 25, 26, 27, and 29 are independent.
- The ’002 Patent’s claims are directed toward, e.g., “dynamic wordline drivers and decoders for memory arrays” and “[a] method of selecting a particular wordline of a memory array.”
- IPR2018-01249 challenges claims 1-28 and 31-37 of the ’002 patent under 35 U.S.C. § 103 in two independent grounds.

'002 Patent (APPLE-1001), 1:8-9, 10:65-16:9; Petition, 1-2, 7-8.

'002 Patent Fig. 1




Q. Would a person of ordinary skill in the art have understood that the 2 to 4 decoder labeled 112 and the conditional clock generator labeled 110 were separate and distinct circuits in the '002 patent?

A. I think a POSA looking at a figure like this would have understood that this is drawn to serve as a functional block diagram describing the major blocks that are needed, functionally, to produce the final wordline driving function into the memory array.

I don't think a POSA, and I don't believe a POSA would look at this functional block diagram and conclude that, therefore, the 2 to 4 decoder and the conditional clock generator block have to be implemented as two separate blocks, as such.

Pedram Depo. (APPLE-1019), 50:4-18; Pet. Reply, 22.



Issue 1: Whether Asano/Itoh Combination Teaches distinct “first” and “second logic”

'002 Patent: Claim 1

'002 Patent

1. A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

APPLE-1001, 10:65-11:10.

Issue 1: Asano/Itoh Teach “first logic” and “second logic”

Asano's Wordline Address Decoder and Driver

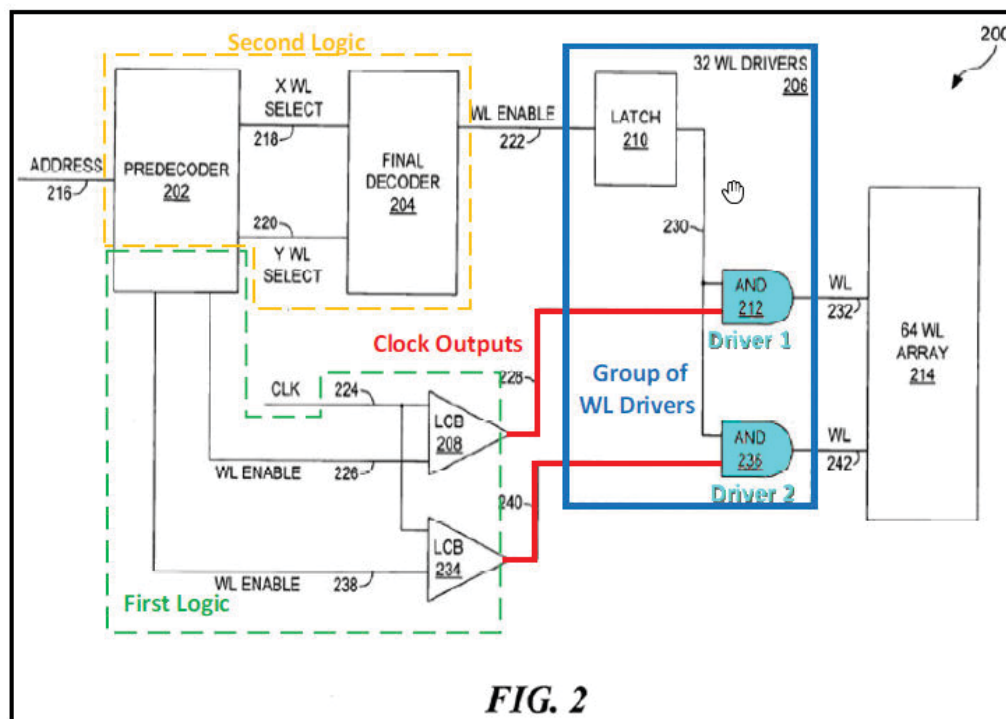
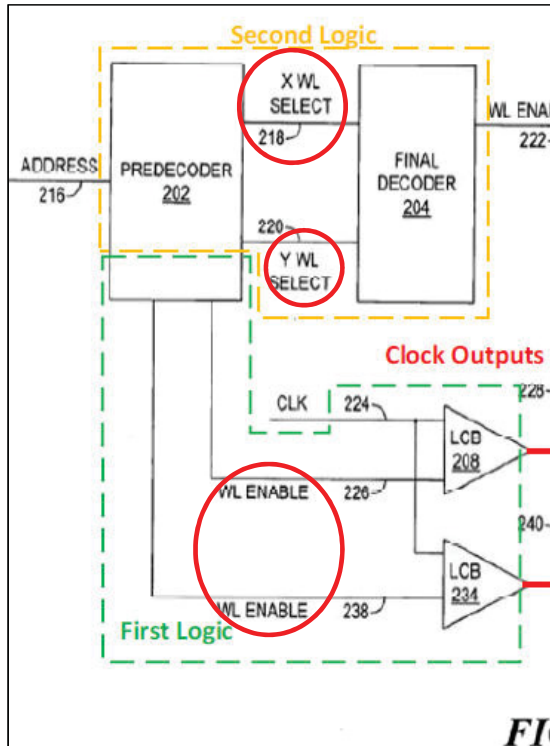


FIG. 2

Asano, FIG. 2 (annotated); Petition, 33-35.

Issue 1: Asano/Itoh Teach “first logic” and “second logic”

Asano discloses a predecoder 202 that decodes three separate portions of a 6-bit address 216 to derive three distinct output signals:



- a wordline enable signal (WL enable)
- an X wordline select signal, and
- a Y wordline select signal.

Petition, 33, 36-41; Dr. Horst (APPLE-1003), para. 111, 115; Asano, [0016], [0019].

[0016] To begin the access cycle for the memory 200, an address is first received in step 302 at the predecoder 202 through a first communication channel 216. Typically, the address is 6 bits long, and from those 6 bits, the predecoder derives a wordline enable signal and two wordline select signals in step 304, an X wordline select signal and a Y wordline select signal. The X wordline select signal is 8 bits long and is output to the final decoder 204 through a second communication channel 218. The Y wordline select signal is output to the final decoder 204 through a third communication channel 220 and is 4 bits long.

Asano, [0016]; Petition, 33, 36.

Asano Decodes 5-bits to produce wordline select signals

Dr. Horst Explains

Petition, 33, 36-39.

“From the description [below], a POSITA would have understood that ... the **X wordline select signal** ... would come from decoding three bits of the address field (e.g., bits 4:2) with a **3-to-8 decoder**” and “the **Y wordline select signal** ... would come from a **2-to-4 decoder** connected to two address bits (e.g., bits 1:0) ...”

Dr. Horst (APPLE-1003), para. 111; Petition, 36, 39-40.

[0016] To begin the access cycle for the memory 200, an address is first received in step 302 at the predecoder 202 through a first communication channel 216. Typically, the address is 6 bits long, and from those 6 bits, the predecoder derives a wordline enable signal and two wordline select signals in step 304, an X wordline select signal and a Y wordline select signal. The X wordline select signal is 8 bits long and is output to the final decoder 204 through a second communication channel 218. The Y wordline select signal is output to the final decoder 204 through a third communication channel 220 and is 4 bits long.

Asano, [0016]; Petition, 33, 36.

Asano's Decodes 1-bit to produce two LCB selection signals

Dr. Horst Explains

Petition, 33, 36-39.

“This ‘most significant bit’ of the memory address . . . selects one LCB when the bit is low and the other LCB when it is high. Driving one of two outputs high based on an input but is the well-known function of a 1-to-2 decoder ...”

Dr. Horst (APPLE-1003), para. 115; Petition, 36, 39.

[0016] To begin the access cycle for the memory 200, an address is first received in step 302 at the predecoder 202 through a first communication channel 216. Typically, the address is 6 bits long, and from those 6 bits, the predecoder derives a wordline enable signal and two wordline select signals in step 304, an X wordline select signal and a Y wordline select signal. The X wordline select signal is 8 bits long and is output to the final decoder 204 through a second communication channel 218. The Y wordline select signal is output to the final decoder 204 through a third communication channel 220 and is 4 bits long.

Asano, [0016]; Petition 33, 36.

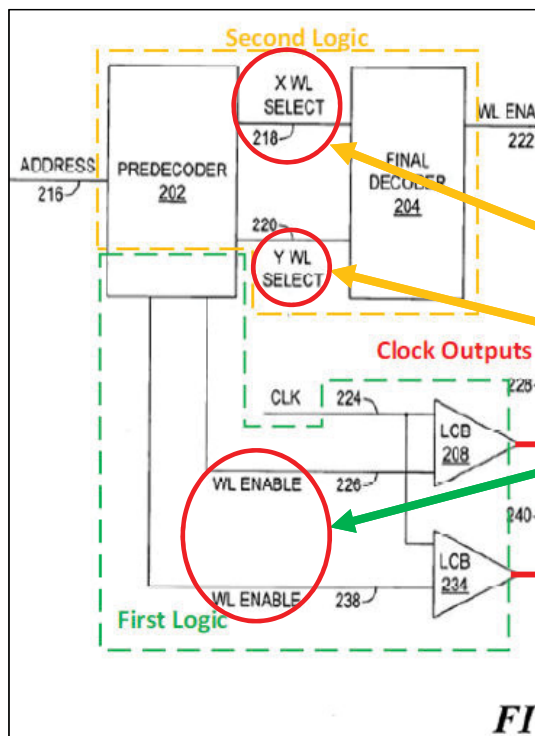
The first AND gate 212 receives a clocking signal from the first LCB 208 through the fifth communication channel 228, while the second AND gate 236 receives a clocking signal from the second LCB 234 through the sixth communication channel 240. Depending on the most significant bit of the address signal that is input into the predecoder 202, either the first AND gate 212 or the second AND gate 236 is selected.

Asano, [0019]; Petition, 33, 36.

“Thus, all six input bits have been accounted for, with bits [4:2] selecting the X output, bits [1:0] selecting the Y output, and the most significant bit [5] selecting only one of the LCBs.”

Dr. Horst (APPLE-1003), para. 115; Petition, 36, 39.

Review: Separate Outputs of Asano's Predecoder 202



6 Input Address Bits

3-address bits → 8-bit X WL Select

2-address bits → 4-bit Y WL Select

1-address bit → 2-bit WL Enable

Petition, 33-39.

Asano, FIG. 2 (annotated); Petition, 33-39.

Decoding 6 Input Address Bits

Dr. Pedram

Q. Are you saying you would use one set of AND gates for the 1-bit, another set for the 2 bits and another set for the 3 bits?

A. So one implementation would be precisely what you said. Of course, for the 1-bit, you won't use any AND gates. But yeah, for the 2 and 3 bits, the AND gates that would do the decoding of the 2-bit group will be different from the AND gates that are used for the decoding of the 3 bits.

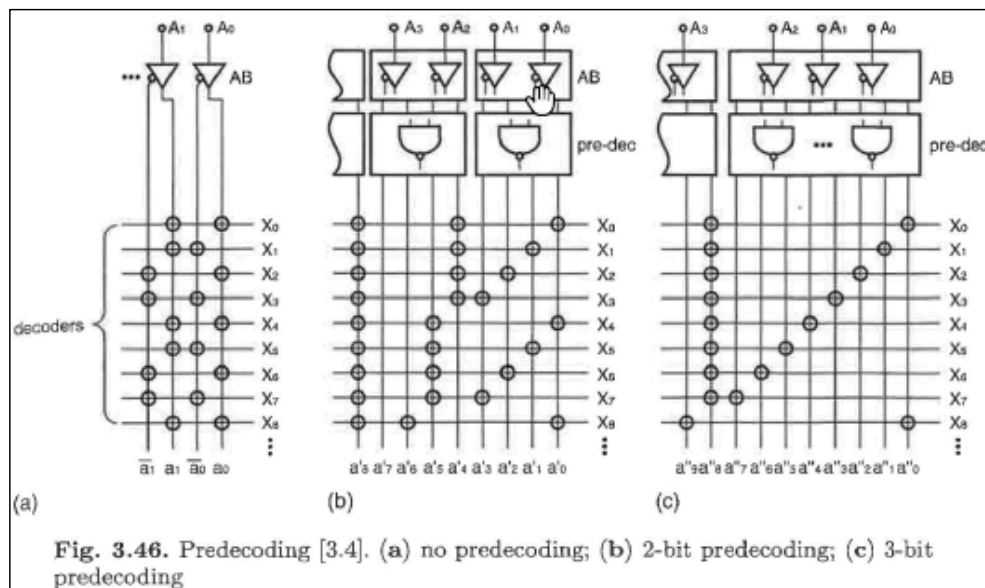
Pedram Depo. (APPLE-1019), 23:16-24; Pet. Reply, 23.

Itoh discloses textbook decoder circuits that a POSITA would have used to implement Asano's predecoder.

Petition, 33, 36-41; Dr. Horst (APPLE-1003), para. 111, 115.

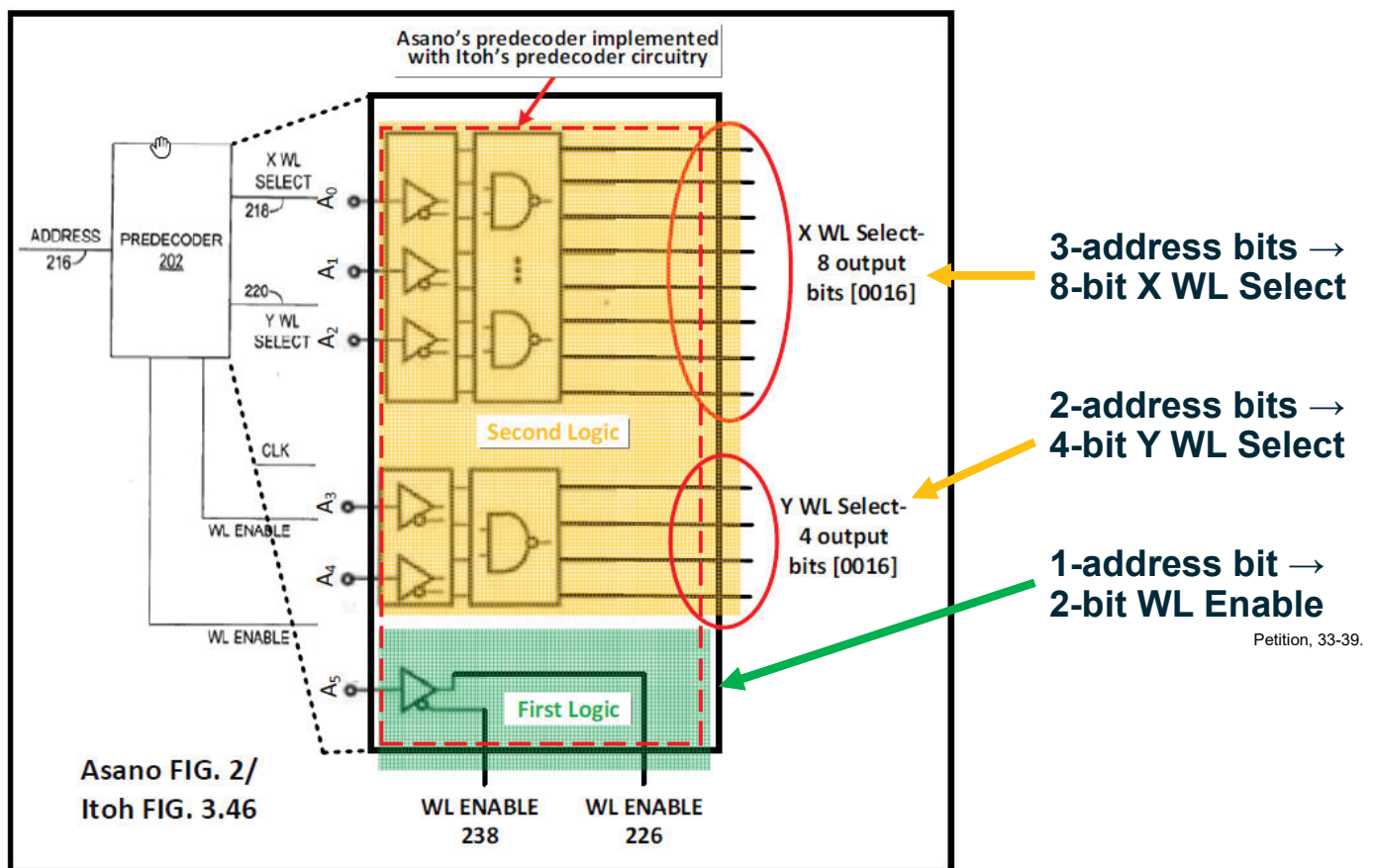
"A POSITA designing a memory circuit according to Asano, *would have naturally turned to a textbook such as Itoh's "VLSI Memory Chip Design," for details on memory design techniques for integrated circuits.*"

Dr. Horst (APPLE-1003), para. 121; Petition 35.



Petition, 35-41; Dr. Horst (APPLE-1003), para. 121-124; Itoh, Fig. 3.46.

Asano's block 202 Implemented with Textbook Decoder Circuits



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Asano FIG. 2 and Itoh FIG. 3.46 (annotated); Petition, 38.

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Motivation to combine Asano and Itoh

“An artisan endeavoring to practice Asano’s invention would have looked to known circuit designs when seeking to implement the Asano predecoder since Asano describes it at only a functional level...”

Petition, 41.

“For over a half century, the Court has held that a patent for a combination which only unites old elements with no change in their respective functions . . . obviously withdraws what already is known into the field of its monopoly and diminishes the resources available to skillful men. This is a principal reason for declining to allow patents for what is obvious. The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”

KSR Int’l Co. v. Teleflex Inc., 550 U.S. 398, 415-16, (2007);
cited at Pet. Reply, 24; *see also* Petition, 35, 41 (citing Dr. Horst (APPLE-1003), para. 121-124.



Issue 2: Whether Patent Owner's Construction of "Clock Signal" is Improper

'002: Exemplary Claim 1

1. A circuit device comprising:
first logic to receive a **clock signal** and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the **clock signal** to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and
second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

APPLE-1001, 10:65-11:10.

Proposed Constructions: “Clock Signal”

Petitioner: Plain Meaning

- but if necessary to construe then:

“a signal used for synchronization”

Pet. Reply, 1, 11.

Patent Owner: “a periodic signal used for synchronization”

POR, 11.

Examples of “Clock Signals” that do not meet Patent Owner’s Narrow Construction

“Conditional” Clock Signals

Q: In Figure 1 of the '002 patent, there are four signals labeled 124, 126, 128 and 130. These are outputs of the conditional clock generator 110; correct?

A: Yes.

...

Q: In your opinion, are signals 124, 126, 128 and 130 clock signals as you have defined that term?

A: In general, no, because a clock signal, in my definition, would have fixed periodicity. You see a fixed stream, constant stream of zero and ones coming in with fixed interval in between. always running, continuously running, and used for synchronization purposes. I don't believe, in general, any of these signals which are called conditional clock signals, I guess. We could call them that way because they are the outputs of the conditional clock generator. None of these signals, 124, 126, 128, 130 meet that definition.

Pedram Depo. (APPLE-1019), 83:9-13, 83:19-84:7;
Pet. Reply, 4.

5. The circuit device of claim 1, wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output.

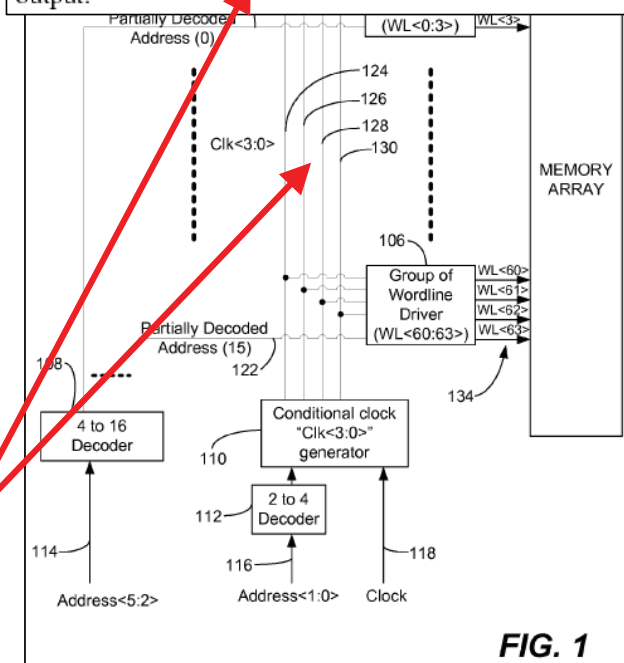


FIG. 1

'002 Patent (APPLE-1001), FIG. 1, Claim 5.

Examples of “Clock Signals” that do not meet Patent Owner’s Narrow Construction

“Gated” Clock Signals

Clock gating is a well known technique used to reduce power dissipation in clock associated circuitry. The idea of clock gating is to shut down the clock of any component whenever it is not being used (accessed).

Dr. Pedram (APPLE-1018), 1; Pet. Reply, 10.

For that reason, circuits are being developed with controllable clocks. This means that from the master clock, other clocks are derived that can be slowed down or stopped completely with respect to the master clock, based on certain conditions.

Dr. Pedram (APPLE-1017), 20; Pet. Reply, 10.

As Dr. Pedram testified at deposition, a “gated clock signal” is different than the claimed “clock signal” and can be turned on and off to propagate the clock signal or not. Ex. 1019 at 31:7-11.

Sur-Reply, 9 (citing Pedram Depo. (APPLE-1019), 31:7-11).

“Clock Signal” Synonymous with “Timing Pulse”

IEEE Dictionary:

clock signal A periodic signal used for synchronizing events.
Synonyms: clock pulse; timing pulse. (C) 610.10-1994

Ex. 2002, 9; Pet. Reply, 13.

Patent Owner:

The IEEE Dictionary is a reliable, unbiased authority

POR, 12.

Non-periodic Clocks in the Prior Art

Pet. Reply 8-9.

Itoh refers to non-periodic control signals as “clocks”

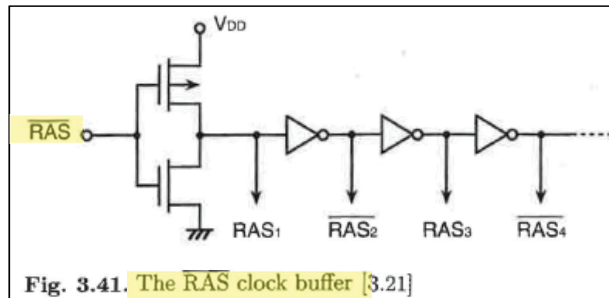


Fig. 3.41. The RAS clock buffer [3.21]

Figure 3.41 shows a typical $\overline{\text{RAS}}$ -clock buffer [3.21] to control the row address buffers. To discriminate between the TTL logic levels of over 2.4 V or

Itoh (APPLE-1007), 142; Pet. Reply, 8-9.

A Basic Word Driver. Figure 3.48 shows the basic unit of conventional word drivers [3.13, 3.21, 3.23]. Each word line is divided into two, to reduce word-line delay (see Fig. 3.40), and the resulting divided word line has its own word driver, Q_W . Since a CMOS NAND decoder cannot be placed at a tight word-line pitch, it is shared with two sets (left and right) of four word drivers, although only the right section is shown in the figure. Address signals X_j and X_k are inputted from 2-bit predecoders to the decoder. Each of the four word drivers selected by the decoder is selectively driven by decoded row select lines RX (RX_0 – RX_3), enabling the corresponding word line to be driven. The RX drivers in Fig. 3.48b provide a boost word voltage to one of RX s as a result of two-address bit (a_0, a_1) decoding, as follows. At first, node WDL is precharged almost to V_{DD} during the precharge period (i.e. $\overline{RP} : H$) and all address signals and thus all RX lines are fixed at 0 V. When the addresses have been valid after starting activation with $\overline{RP} : L$, a clock Φ_B generated by the $\overline{\text{RAS}}$ buffer is applied, so that only one selected RX line is driven at a high enough voltage, boosted by C_B .

Itoh (APPLE-1007), 149; Pet. Reply, 8-9.

Dr. Pedram States:

Finally, the RAS# and CAS#

timing signals are not referred to as clock signals, as seen above.

60. The POSA would understand that asynchronous systems do not use a periodic clock signal – rather, they use multiple, non-periodic timing signals, such as the RAS# and CAS# strobe signals shown above.

Dr. Pedram (Ex. 2001), para. 59-60; Pet. Reply 8-9.

Non-periodic Clocks in the Prior Art

United States Patent [19] Hayakawa et al.

Pet. Reply 10.

[54] STATIC RANDOM ACCESS MEMORY WITH ADDRESS TRANSITION DETECTOR

16. Static RAMs also may include non-periodic timing signals referred to as clocks. For instance:

□□

The clock signal generator 14 receives the address transition detect signal SATD from the address transition detector 13, and produces a clock signal ϕS that is effective in level for a fixed period. The clock signal ϕS is applied through a clock signal line 23 to the sense amplifier 10 and the data output circuit 11, so that those circuits are rendered active during the fixed period.

Hayakawa, 3:50-57, emphasis added.

17. The clock described in Hayakawa is generated in response to an address change detected by the address transition detector. This clock depends on the particular address pattern and is not periodic. Thus, this static RAM clock requires a definition broader than the definition of “clock signal” offered by Dr. Pedram.

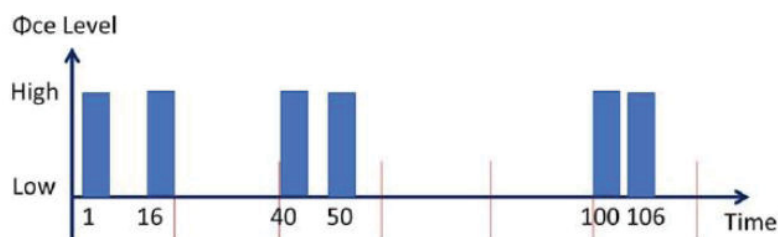
Dr. Horst (APPLE-1013),
para. 17; Pet. Reply, 10.

Dr. Pedram's Testimony on Static Ram Access Patterns

“The access pattern to a static RAM is determined by the access needs of the component or device using the RAM as memory . . .”

“The resulting access pattern is highly irregular . . .”

Dr. Pedram (Ex. 2001), para 97, 99.



Dr. Pedram (Ex. 2001), para. 121.

“PO provides no credible evidence” of “intrinsic evidence . . . support[ing] the interpretation of the claim term ‘clock signal’ as ‘a periodic signal . . . ”

Pet. Reply, 5.

Q. Is there any place in the specification of the '002 patent where you believe the inventors have set forth a particular definition of the term "clock signal"?

A. I have not seen in the '002 patent a precise definition of the clock.

Pedram Depo. (APPLE-1019), 79:4-9; Pet. Reply, 5.

“PO provides no credible evidence” of “intrinsic evidence . . . support[ing] the interpretation of the claim term ‘clock signal’ as ‘a periodic signal’ . . . ”

Pet. Reply, 5.

Patent Owner Reply

Support for this interpretation is also found in the '002 patent itself. Specifically, the POSA would understand that the '002 patent describes a synchronous memory system that uses a periodic clock signal. *Id.* at ¶54. The '002 patent *does not* describe an asynchronous memory system that uses multiple, non-periodic timing signals. *Id.*

POR, 12.

Dr. Pedram (Ex. 2001, para. 54)

54. Support for this interpretation is also found in the '002 patent itself. Specifically, the POSA would understand that the '002 patent describes a synchronous memory system that uses a periodic clock signal. It does not describe an asynchronous memory system that uses multiple, non-periodic timing signals.

Asynchronous Timing Signals Perform “the same functions” as “internally generated clock-synchronous signals”

Pet. Reply, 7-9.

Itoh

synchronous operation can eliminate the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ functions that are familiar in asynchronous operation, since the same functions are carried out by the internal signals RS1 and CS1.

Itoh (Ex. 2003), 19; Pet. Reply, 8-10.

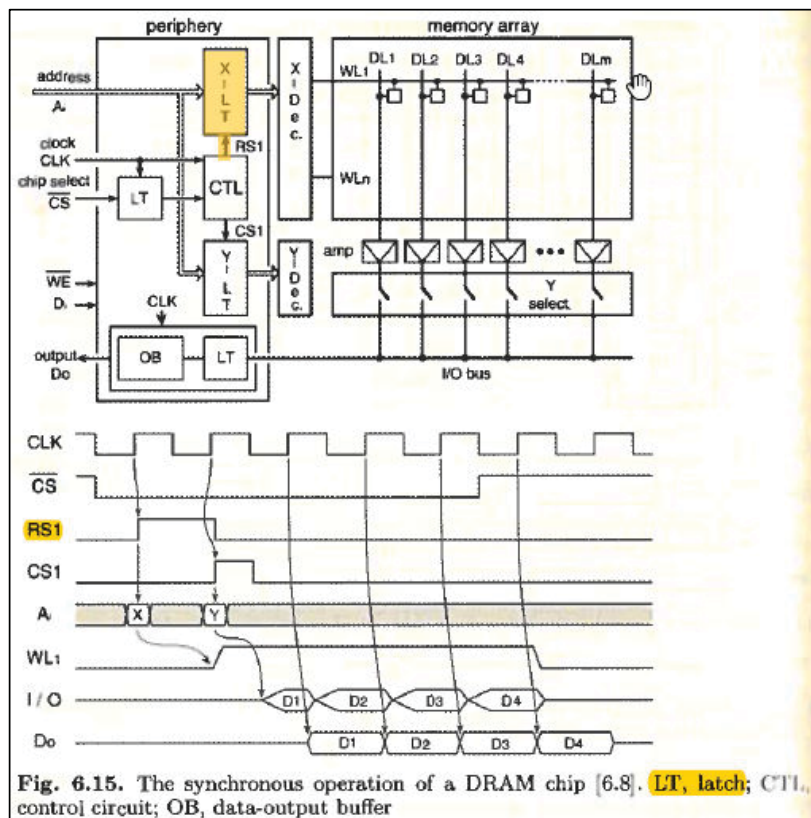
Dr. Pedram

Notice that, as Itoh also points out, synchronous operation can even eliminate the roles of RAS# and CAS# which are used in asynchronous operation, since the same functions are carried out by the internally generated clock-synchronous signals RS1 and CS1.

Dr. Pedram (Ex. 2001), para. 62; Pet. Reply, 8-10.

Even in synchronous memory systems, the periodic system clock is not passed to an address decoder.

Pet. Reply, 10.



“PO’s reliance on Dr. Pedram’s expert opinion is misplaced given Dr. Pedram admitted he failed to consider the full scope of the claims.”

Pet. Reply, 2-3.

Q: Dr. Pedram, it’s your opinion that the ’002 patent is limited to applications you would characterize as synchronous memory systems; correct?

A: So again, I’m not here to opine on the scope of the claims. This is a different inquiry... So, the embodiments are definitely that. And—but what the scope of the claim is, I mean, it’s a different inquiry that I really haven’t considered.

Q: You’re saying you haven’t considered whether the claims of the ’002 patent are limited to synchronous memory systems, but only whether the embodiments of the ’002 patent depict synchronous memory systems?

MR. SAUER: Objection; form.

WITNESS: Again, this is really not a question I have considered, to define the exact scope of any of the claims with respect to the systems that it covers or does not cover. And I—I have construed, in my view, and describe my understanding of what the clock signal is in this context.

Pet. Reply, 2-3 (quoting Pedram Depo. (APPLE-1019), 52:15-53:23.

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Issue 3: Whether Sato Renders the '002 Patent Claims Obvious

'002 Patent Claim 1

1. A circuit device comprising:
first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and
second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

APPLE-1001, 10:65-11:10.

**Patent
Owner**

"Sato is Fundamentally different than the synchronous memory system of the '002 patent." POR, 3.

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Petition, 14.

Petition, 10.

Petition, 8.

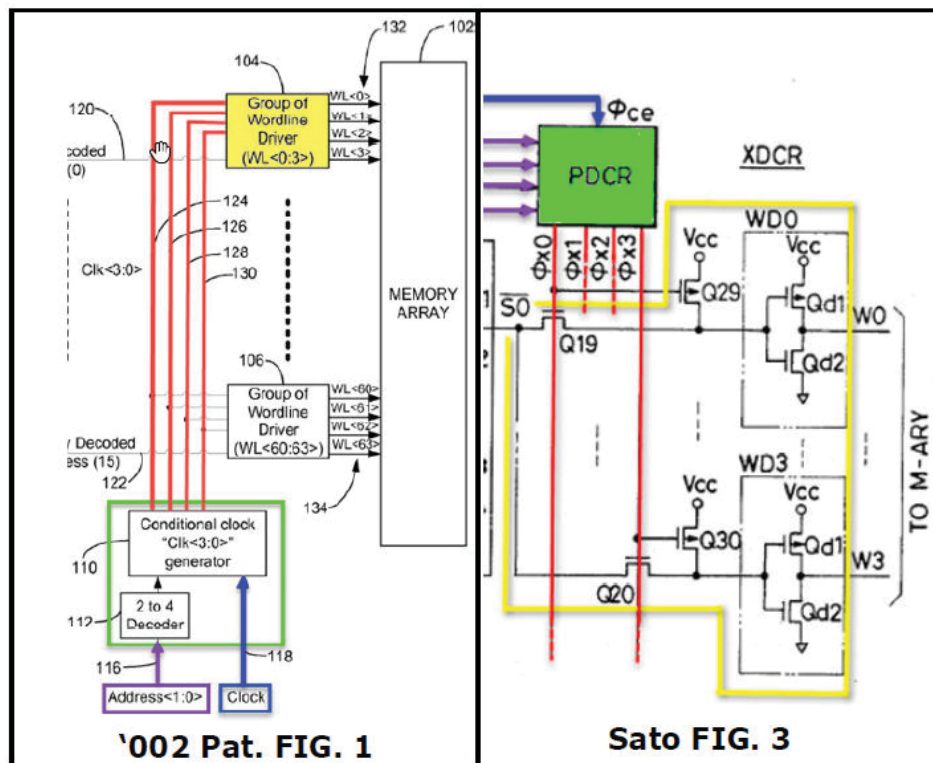


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Circuits of Sato and the '002 Patent Function the Same

Petition, 14-15, 20; Pet. Reply, 13-18.

Rebuttal "Sato is Fundamentally different than the synchronous memory system of the '002 patent." POR, 3.
to:



FISH.

Petition, 20; Pet. Reply, 13-18.

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'002 Patent Claim 1

1. A circuit device comprising:
first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and
second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

APPLE-1001, 10:65-11:10.

**Patent
Owner**

"Sato is Fundamentally different than the synchronous memory system of the '002 patent." POR, 3.

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Dr. Horst's Analysis

Rebuttal
to:

"Dr. Horst . . . parrots the reply without providing any reasoning or explanation." Sur-Reply, 17.

#	Selection Status	'002 Word Line Driver Input (ddh0)	Sato Word Line Driver Input (input to WD0)
0	<p>Nonselected group (Address Line 304/$\overline{S0}$ = HIGH)</p> <p>Nonselected or LOW clock (CLK<0>/$\phi x0$ = LOW)</p>	<p>Pulled HIGH by LOW CLK<0> turning Mp0 ON and by wordline via 320</p> <p>(Mn0 is OFF blocking Address Line 304 signal)</p> <p>Wordline WL<0> is LOW</p>	<p>Pulled HIGH by $\phi x0$ turning Q29 ON</p> <p>(Q19 is OFF blocking NAND decoder output $\overline{S0}$ signal)</p> <p>Wordline W0 is LOW</p>
1	<p>Nonselected group (Address Line 304/$\overline{S0}$ = HIGH)</p> <p>Selected HIGH clock (CLK<0>/$\phi x0$)</p>	<p>Unselected HIGH address line 304 maintains ddh0 at a HIGH level through Mn0.</p> <p>Wordline WL<0> is LOW</p>	<p>Unselected HIGH NAND decoder output $\overline{S0}$ maintains the wordline driver input at a HIGH level through Q19.</p> <p>Wordline W0 is LOW</p>
2	<p>Selected group (Address Line 304/$\overline{S0}$ = LOW)</p> <p>Nonselected or LOW clock (CLK<0>/$\phi x0$ = LOW)</p>	<p>Pulled HIGH by LOW CLK<0> turning Mp0 ON and by wordline via 320</p> <p>(Mn0 is OFF blocking LOW Address Line 304 group select signal)</p> <p>Wordline WL<0> is LOW</p>	<p>Pulled HIGH by $\phi x0$ turning Q29 ON</p> <p>(Q19 is OFF blocking LOW NAND decoder output $\overline{S0}$ group select signal)</p> <p>Wordline W0 is LOW</p>
3	<p>Selected group (Address Line 304/$\overline{S0}$ = LOW)</p> <p>Selected HIGH clock (CLK<0>/$\phi x0$)</p>	<p>Pulled LOW by LOW (selected) address line 304 signal through Mn0 being turned on by HIGH CLK<0></p> <p>Wordline WL<0> is HIGH</p>	<p>Pulled LOW by LOW (selected) NAND decoder output $\overline{S0}$ signal through Q19 being turned on by HIGH $\phi x0$</p> <p>Wordline W0 is HIGH</p>

TABLE 1

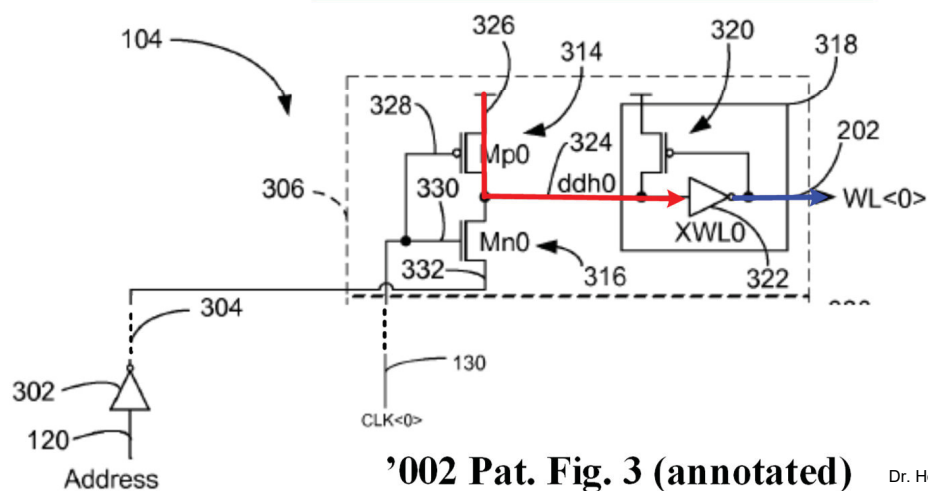
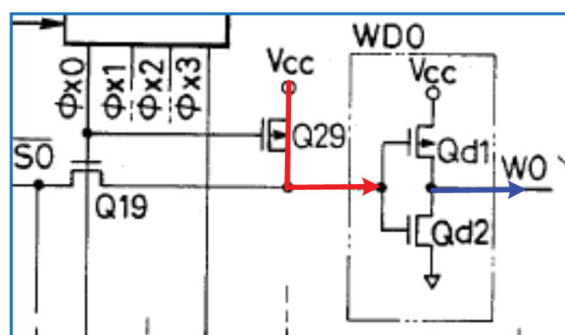
Dr. Horst (APPLE-1013), para. 28;
Pet. Reply, 15-16.

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Identical Wordline Activation

Petition, 32; Dr. Horst (APPLE-1013), para. 28.

Sato Fig. 3
(annotated)



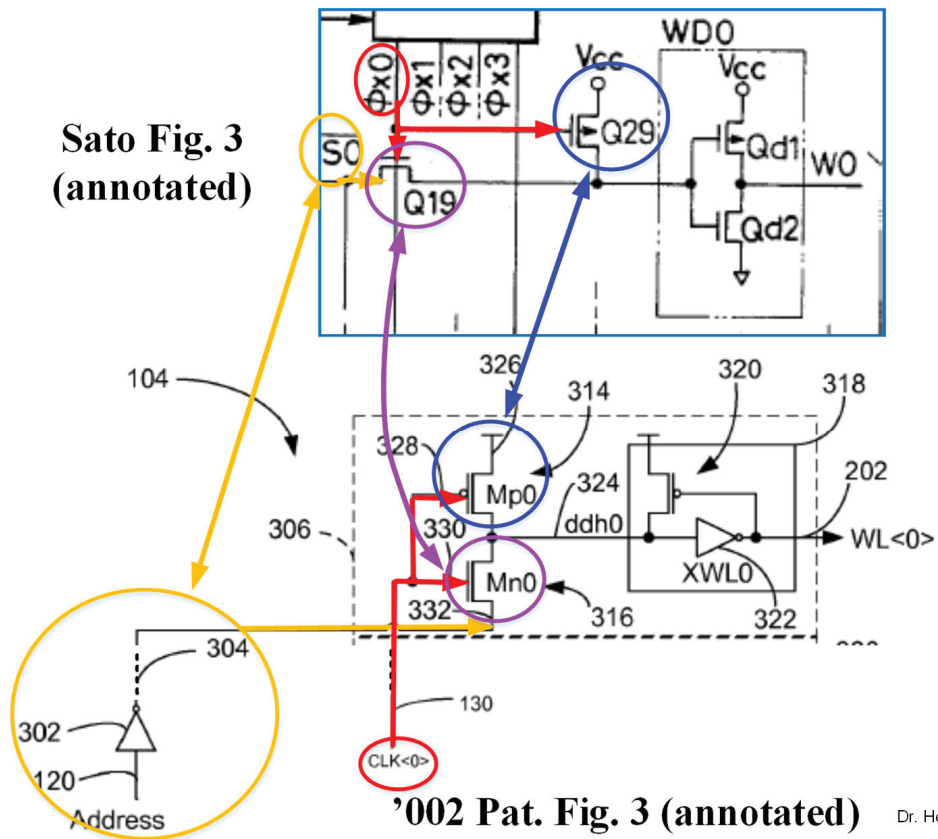
'002 Pat. Fig. 3 (annotated)

Dr. Horst (APPLE-1013), para. 28;
Pet. Reply, 15-16.

Identical Wordline Activation

Petition, 32; Dr. Horst (APPLE-1013), para. 28.

Sato Fig. 3
(annotated)

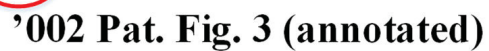


'002 Pat. Fig. 3 (annotated)

Dr. Horst (APPLE-1013), para. 28;
Pet. Reply, 15-16.

Petition, 32; Dr. Horst (APPLE-1013), para. 28.

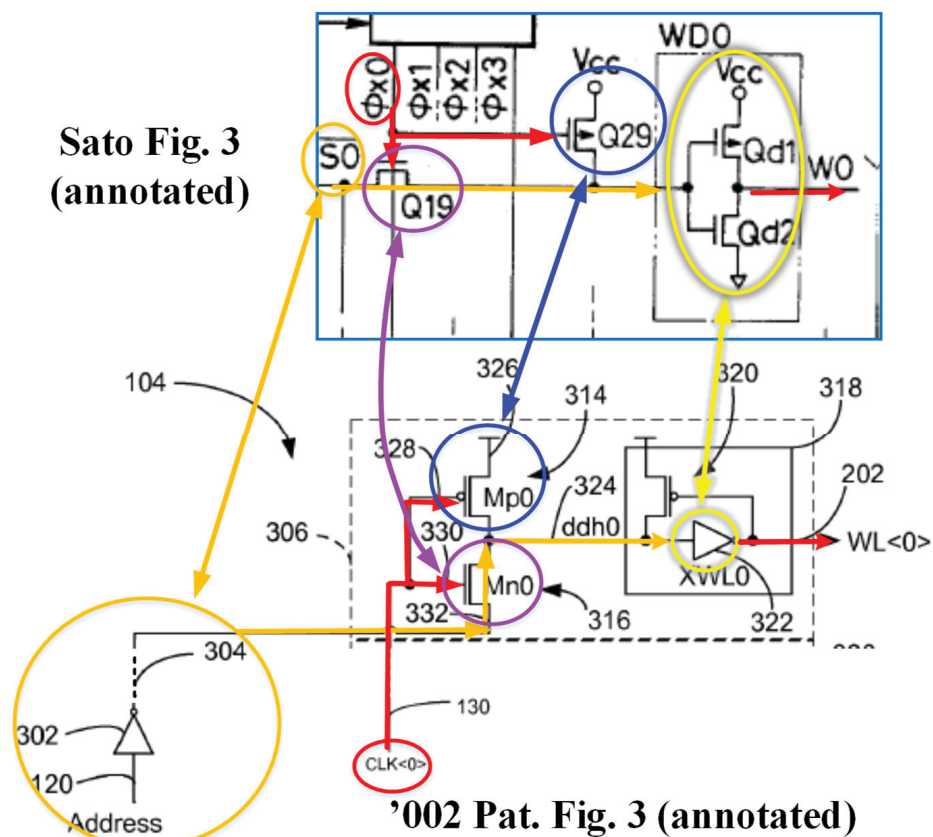
The diagram shows the internal circuit of the first stage of a 4-to-1 multiplexer. It consists of a 2-to-1 MUX block and a 4-to-1 MUX block. The 2-to-1 MUX has inputs S0 and S1, and its output is W0. The 4-to-1 MUX has inputs W0, W1, W2, and W3, and its output is W0. The circuit includes transistors Q29, Qd1, and Qd2, and a Vcc supply. The output of the first stage is W0.



Dr. Horst (APPLE-1013), para. 28;
Pet. Reply, 15-16.

Circuits of Sato and the '002 Patent Apply the PDCR/Clock Generator Output Identically

Petition, 32; Dr. Horst
(APPLE-1013), para. 28.



'002 Patent Claim 1

1. A circuit device comprising:
first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and
second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

APPLE-1001, 10:65-11:10.

“Sato expressly teach[es] [his] address decoder is modifiable to use in clocked synchronous systems . . .”

Pet. Reply, 17-18; Petition 15.

BACKGROUND OF THE INVENTION

This invention relates to semiconductor memory devices and to a technique which will be effective when applied, for example, to CMOS (Complementary MOS) static RAMs (Random Access Memories).

CMOS static RAMs including clocked static decoders are known in the art.

Sato, col. 1:6-11; Petition, 15.

Although the description given above deals primarily with the application of the invention to a static RAM as the background and field of utilization of the present invention, the invention is not particularly limited to such an application but can be applied to dynamic RAMs or other semiconductor memory devices as well. The present invention can be applied widely to semiconductor memory devices having at least a clocked static type address decoder and semiconductor devices with built-in semiconductor memory devices of the type described above.

Sato, col. 11:66-12:8; Petition, 15; Pet. Reply, 17.

Ortho-McNeil Pharm., Inc. v. Mylan Labs., Inc., 520 F.3d 1358, 1364 (Fed. Cir. 2008) (“a flexible TSM test remains the primary guarantor against a non-statutory hindsight analysis such as occurred in this case.”).

Cited at Pet. Reply, 17.

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... and “a POSITA would have been able to build a clock generator . . . to accomplish Sato’s clear suggestion”

Dr. Horst (APPLE-1013) para. 36; Pet Reply 17-18.

Dr. Horst

36. Furthermore, Sato states that his address decoder could be modified (if necessary) for use in clocked synchronous systems. Modifications, such as adding a global clock input to the TC block would, in my opinion, be well within the capabilities of a POSITA. Indeed, I agree with Dr. Pedram’s deposition testimony that a POSITA would have been able to build a clock generator from well-known components in order to accomplish Sato’s clear suggestion that his address decoder could be used in clocked synchronous systems. Pedram Depo., 48:2-21.

Dr. Horst (APPLE-1013), para. 36;
Pet. Reply 17-18.

Dr. Pedram

Q. Would the person of ordinary skill in the art prior to October 10, 2006, have known how to create the clock 118 signal that we see in Figure 1 from the clock generation circuitry that you discussed before?

A. So if I understand the question correctly, the person skilled in the arts would know that there are these components that you could have purchased, acquire, integrate, that would allow you to establish a clock generator circuitry that would produce the clock signal. You have to have drivers to get the signal where it has to go.

That would have been known to a POSA. . . .

But -- but yeah, using known components, putting them together, you could generate the clock signal. He would have known that yes, or she.

Pedram Depo. (APPLE-1019), 48:2-14, 19-21;
Pet. Reply 17-18.

Sato Applies the Timing Signal to its PDCR Outputs

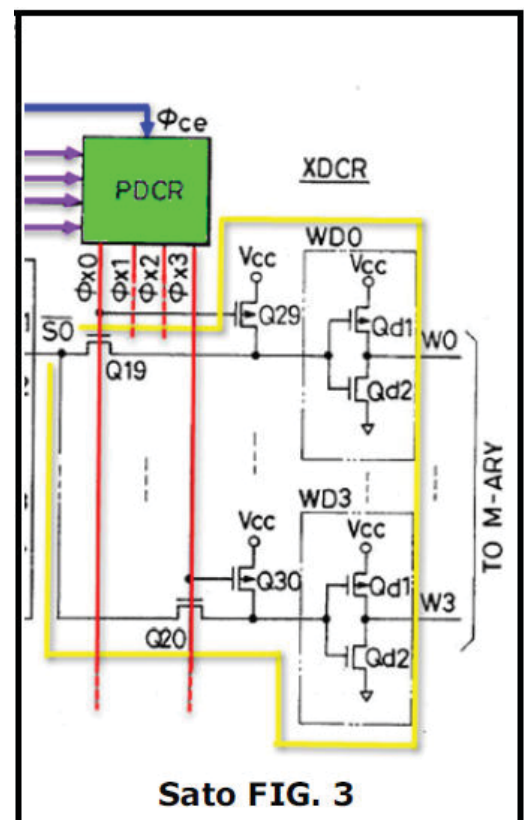
Petition, 19-23.

- Dr. Horst developed a detailed (nine paragraph) analysis of the operation of Sato's PDCR as a POSITA would have understood it based on Sato's own Description.

Dr. Horst (APPLE-1003), para. 60-65, 71-72; Petition, 19-23.

- Dr. Horst's analysis was corroborated by Brown's digital logic textbook (APPLE-1009)

Cited at Petition, 22.



Petition, 20.

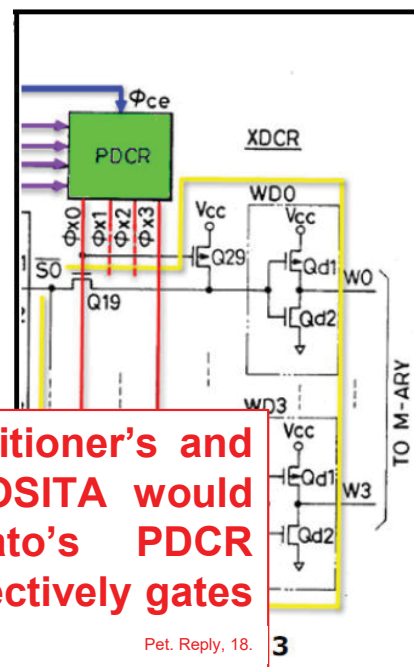
Sato Applies the Timing Signal to its PDCR Outputs

Petition, 19-23.

- Dr. Horst developed a detailed (nine paragraph) analysis of the operation of Sato's PDCR as a POSITA would have understood it based on Sato's own Description.

Dr. Horst (APPLE-1003), para. 60-65, 71-72; Petition, 19-23.

- Dr. Horst's analysis was corroborated by Brown's digital logic textbook (APPLE-1009)



“[Patent Owner] does not contest Petitioner's and Dr. Horst's explanation of how a POSITA would understand the operation of Sato's PDCR functioning as a demultiplexer that selectively gates the timing signal.”

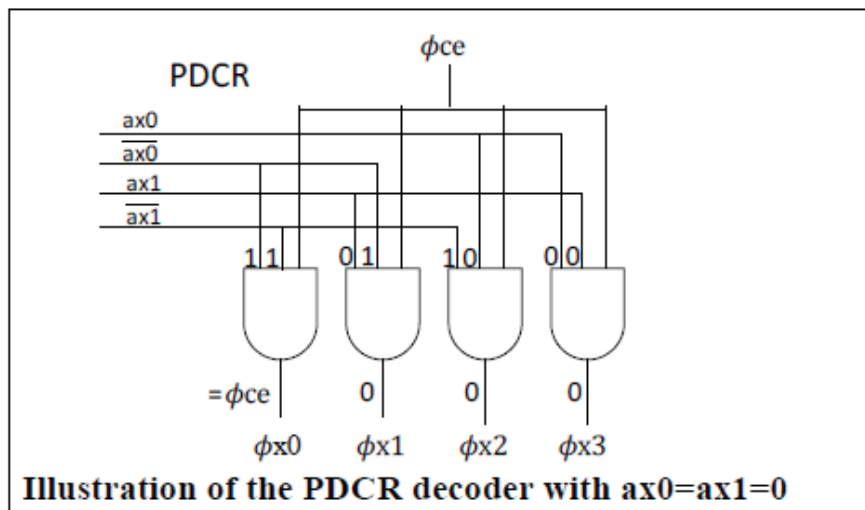
Pet. Reply, 18.

Petition, 20.

Dr. Horst Explained Sato's Clock Outputs in Detail

“Sato does not provide a diagram of the internals of XDCR in FIG. 3, but the text description [Sato, 9:44-59] provides enough detail for a POSITA to understand that it performs a function equivalent to four AND gates as I have drawn below. This structure is also equivalent to how a POSITA would have understood the operation of the ‘002 patent’s conditional clock generator . . .”

Dr. Horst (APPLE-1003), para. 62; Sato (APPLE 1001), 9:52-59, 10:36-39; Petition, 19-23.



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Dr. Horst Explained Sato's Clock Outputs in Detail

Petition, 19-23.

63. Furthermore, Brown's digital logic textbook corroborates this understanding. Brown describes the operation of a demultiplexer circuit that is the same as my illustration above. See Brown, 314-315, Fig. 3.16.

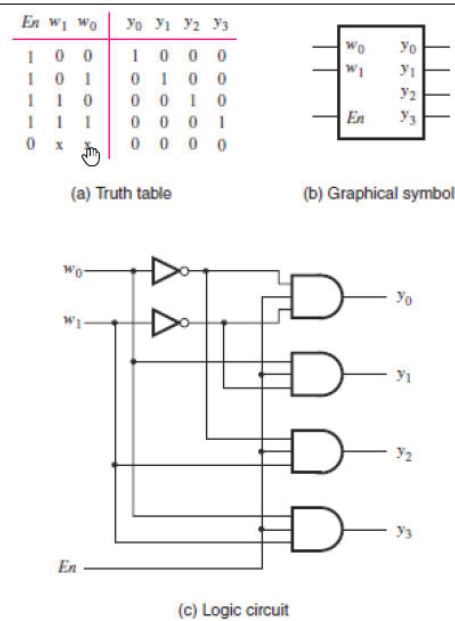


Figure 6.16 A 2-to-4 decoder.

Dr. Horst (APPLE-1003), para. 63; Petition, 19-23.

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Appendix Slides

“Clock Signal” Synonymous with “Timing Pulse”

IEEE Dictionary: clock signal A periodic signal used for synchronizing events.
Synonyms: clock pulse; timing pulse. (C) 610.10-1994

Ex. 2002, 9.

Patent Owner: The IEEE Dictionary is a reliable, unbiased authority

POR, 12.

Petitioner’s Argument

PO asserts that the “words ‘clock signal’ and ‘timing signal’ are not interchangeable, nor would the POSA have understood them as such.” *Id.*, 35-36.

Yet, PO’s own dictionary definition of “clock signal” states “timing pulse” is its synonym. Ex. 2002, 9. The same dictionary’s indication that “clock pulse” is also synonymous would suggest to a POSITA that any quibbles over the use of “timing pulse” rather than “timing signal” are irrelevant.

Pet. Reply, 13.

Patent Owner

In its reply, Petitioner points to the IEEE

Dictionary’s definition of “clock signal” indicating that this term is synonymous with “clock pulse” (Ex. 1014 at 5), and argues that the terms “clock signal” and “timing signal” should therefore have the same meaning. Paper 15 at 13. But the dictionary nowhere equates the term “clock signal” with either of the specific terms recited in Sato, *i.e.*, “timing signal” and “selection control signal.” See Ex. 1014 at 4-5. The cited definition of “clock signal” instead only refers to the different term “clock pulse” (*id.* at 5), and Qualcomm does not dispute that a periodic clock signal may be understood as including a plurality of regularly spaced, uniform clock pulses.

Sur-Reply, 12-13.

Circuits of Sato and the '002 Patent Function the Same

Petition, 14-15, 20; Pet. Reply, 13-18.

Rebuttal to: "Petitioner fails to provide any evidence or analysis to show that Sato would work with a periodic clock signal." Sur-Reply, 15.
"Dr. Horst . . . parrots the reply without providing any reasoning or explanation." Sur-Reply, 17.

Dr. Horst Testified that:

Q. You didn't simulate Sato's circuit using a periodic timing signal, correct?

A. No, I didn't simulate the circuit.

Q. **So how did you know it would work?**

A. On page 15 of my report, I developed this table of all the different states that the circuit can be in, and **I showed that the circuit functions correctly in all these different states.**

And **whether it sequences through these states periodically or not periodically doesn't affect its operation.** So it would work correctly in either case.

Horst Depo. (Ex. 2006), 87:2-13.

Sato's Timing Signal Represents or Renders Obvious the Clock Signal

Periodicity vs Pulse Spacing

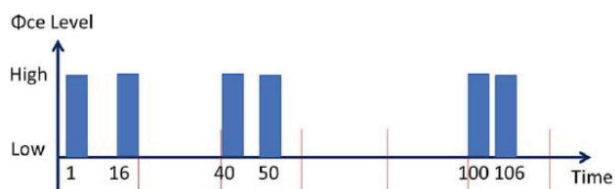
Pet. Reply, 16-17.

THE WITNESS: If the transistors weren't fast enough and you gave it a clock that was too fast, it wouldn't function.

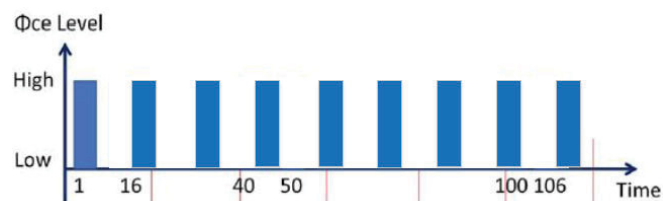
And also if you gave it a nonperiodic clock that was too fast, it wouldn't function.

So in both cases, you have to make sure that the circuit is fast enough for the clock pulses that it's given.

Horst Depo. (Ex. 2006), 88:3-10; cited in Sur-Reply, 18-19.



Pedram (Ex. 2001), para. 121; Pet. Reply, 16-17.



Dr. Horst (APPLE-1013), para. 24-35; Pet. Reply, 16-17.

***Graham* Factors**

A. The petition addresses all the *Graham* factors

PO argues the petition fails to address the second *Graham* factor to identify a difference between the claimed subject matter of the '002 patent and Sato. Response, 28-29. PO is incorrect. Specifically, in arguing Sato's "timing signal ϕ_{ce} represents or renders obvious a clock signal," the petition acknowledges that Sato does not use the words "clock signal," and explains a POSITA would immediately appreciate the timing signal as a type of clock signal, or, under a narrower definition of "clock signal," that it would have been obvious to use a clock signal as the ϕ_{ce} signal based on Sato's explicit teaching that his invention "can be applied widely to semiconductor memory devices having at least a clocked static type address decoder." Pet. 14-15 (citing APPLE-1005, 12:4-6).

Pet. Reply, 12-13 (citing Petition, 14-15).

Dictionary Definitions

IEEE Dictionary (APPLE-1014)

clock signal A periodic signal used for synchronizing events.
Synonyms: clock pulse; timing pulse. (C) 610.10-1994

clock (1) (A) A device that generates periodic signals used for synchronization. (B) A device that measures and indicates time. *See also:* master clock; real-time clock; time-of-day clock; timer; wall clock. (C) A register whose content changes at regular intervals in such a way as to measure time. (C) [20]

(2) A signal, the transitions of which (between the low and high logic level [or vice versa]) are used to indicate when a stored-state device, such as a flip-flop or latch, may perform an operation. (C/TT) 1149.1-1990, 1149.5-1995

(3) An object that measures the passage of time. The current value of the time measured by a clock can be queried and, possibly, set to a value within the legal range of the clock. (C/PA) 1003.5b-1995, 9945-1-1996

(4) (A) A device that generates periodic, accurately spaced signals used for such purposes as timing, regulation of the operations of a processor, or generation of interrupts.

(B) To trigger a circuit to perform an operation, such as to accept data into a register. (C) 610.10-1994

(5) *See also:* dynamometer.

(PE/T&D) 516-1987s, 524-1992

Modern Dictionary of Electronics (APPLE-1015)

clock—1. A pulse generator or signal waveform used to achieve synchronization of the timing of switching circuits and the memory in a digital computer system. It determines the speed of the CPU. 2. A timing device in a system: usually it provides a continuous series of timing pulses. 3. An electronic circuit that generates timing pulses to synchronize the operation of a computer as well as keep time. 4. A strobe signal that activates a certain sequence of operations. 5. An electronic circuit or device for producing precisely timed, repetitive pulses of fixed frequency and amplitude.

Sato - Clock Outputs

**Rebuttal
to:**

“... Sato’s predecoder PDCR is a black box, and the Petitioner’s arguments about what a POSA ‘would understand’ are based purely on speculation.” Sur-Reply, 20.

In the X address decoder XDCR of this embodiment, the afore-mentioned timing signal ϕ_{ce} (selection control signal) is supplied to the pre-decoder PDCR. Accordingly, the CMOS static RAM is brought into the selection state and the timing signal ϕ_{ce} is set to the high logic level so that the output signal of the pre-decoder PDCR, that is, the selection signal $\phi_{x0} \sim \phi_{x3}$, is set selectively to the high logic level.

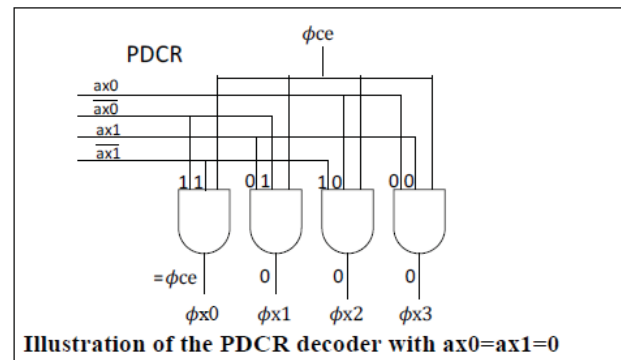
Sato (APPLE-1005), 9:52-59; Petition, 19-23.

The timing signal ϕ_{ce} described above is supplied to the pre-decoder PDCR and its output signal, that is, the selection signal $\phi_{x0} \sim \phi_{x3}$, is generated in accordance with this timing signal ϕ_{ce} .

Sato (APPLE-1005), 10:36-39; Petition, 19-23.

62. Sato does not provide a diagram the internals of XDCR in Fig. 3, but the text description above provides enough detail for a POSITA to understand that it performs a function equivalent to four AND gates as I have drawn below. This structure is also equivalent to how a POSITA would have understood the operation of the '002 patent's conditional clock generator, as I described above in paragraphs 13-16.

Dr. Horst (APPLE-1003), para. 62 (explaining Sato, 9:52-59, 10:36-39);
Petition, 19-23.



Petition, 22.

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Ex. 2004

Specifically, in another IPR proceeding not directed to the '002 patent, but addressing the meaning of the claim term “clock,” Dr. Alpert told the Board that the term “clock” should be interpreted as “a periodic signal used for synchronization.” Ex. 2004 at 3-4. Dr. Alpert stated that the “definition [‘a periodic signal used for synchronization’] is consistent with the broadest reasonable interpretation of the term [‘clock’].” *Id.* Dr. Alpert’s statement provides further support for Qualcomm’s proposed construction.

POR, 14-15 (citing Ex. 2004 at 3-4).

Ex. 2004

I. Claim Construction for “clock”

6. In Ex. 2002 at Section VII.A, Dr. Hayes documents his opinion that the broadest reasonable interpretation of the term “clock” for the ‘122 patent is a “periodic signal used for synchronization in a digital system.” [Ex. 2002 par. 42]

Ex. 2004 at 3; POR, 14-15.

“U.S. Patent 6,356,122 has at least ten references to periodic characteristics of a clock (e.g., frequency) whereas the ‘002 patent has no such references.”

Pet. Reply, 11.