

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc.
Petitioner

v.

Qualcomm Incorporated
Patent Owner

Case IPR2018-01249
Patent 7,693,002

**PATENT OWNER RESPONSE TO PETITION FOR *INTER PARTES*
REVIEW PURSUANT TO 37 C.F.R. § 42.220**

TABLE OF CONTENTS

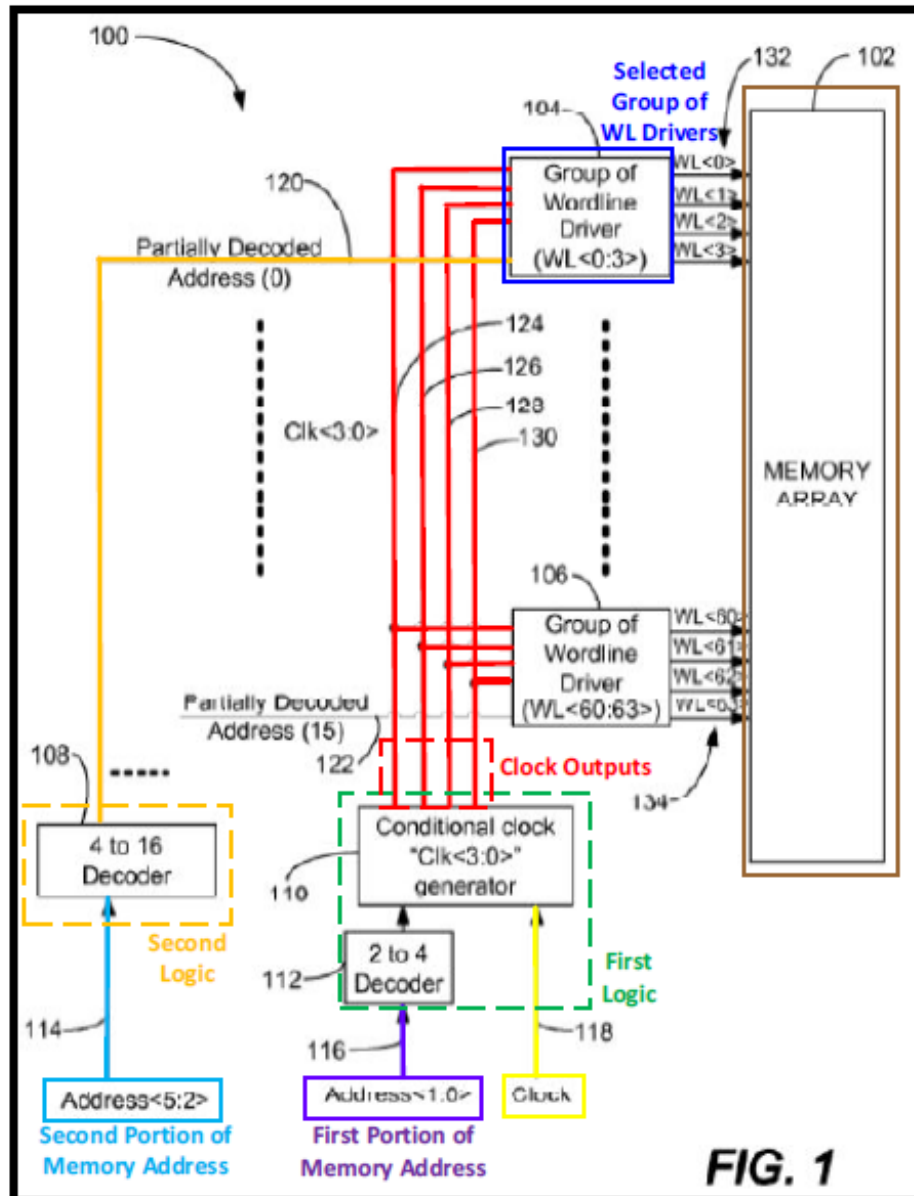
I.	INTRODUCTION	1
II.	THE ALLEGED GROUNDS OF UNPATENTABILITY	6
III.	OVERVIEW OF THE '002 PATENT	7
IV.	CLAIM CONSTRUCTION	11
V.	LEVEL OF ORDINARY SKILL IN THE ART	15
VI.	OVERVIEW OF THE CITED REFERENCES	16
	A. Overview of Sato.....	16
	B. Overview of Asano.....	23
	C. Overview of Itoh	26
VII.	SATO DOES NOT RENDER CLAIMS 1-28 AND 31-37 OBVIOUS (GROUND 1).....	27
	A. The Petition Fails to Establish a <i>Prima Facie</i> Case of Obviousness over Sato.....	28
	B. Sato Does Not Teach or Suggest the “Clock Signal” Required by the Claims.....	30
	1. Sato’s Selection Control Signal ϕ_{ce} is Not a “Periodic Signal Used for Synchronization,” As Required Under the Proper Construction of the Term “Clock Signal.”.....	30
	2. Sato Discloses an Asynchronous Memory System That Does Not Use a Periodic Clock Signal.	33
	3. Petitioner’s Assertion That Sato’s Selection Control Signal “Represents or Renders Obvious a Clock Signal” Is Erroneous.	35
	C. Sato Does Not Teach or Suggest the “Clock Output” Required by the Claims.....	45

VIII.	ASANO AND ITOH DO NOT RENDER CLAIMS 1-17, 20-28, AND 31-36 OBVIOUS (GROUND 2)	47
A.	Asano Does Not Disclose or Suggest a Circuit Device Including Distinct “First Logic” and “Second Logic.”	48
B.	The Petition Does Not Sufficiently Articulate Why a POSA Would Allegedly Have Been Motivated to Combine Asano and Itoh.....	53
IX.	CONCLUSION.....	58

Pursuant to the Board’s Decision – Institution of *Inter Partes* Review (Paper 6), entered January 15, 2019 – Patent Owner Qualcomm, Inc. (“Qualcomm” or “Patent Owner”) submits this response in opposition to the petition for *inter partes* review of U.S. Patent No. 7,693,002 (the “’002 patent”) filed by Apple Inc. (“Apple” or “Petitioner”).

I. INTRODUCTION

The ’002 patent describes and claims an improved wordline driver system. In that system, a received memory address specifying a particular wordline of a memory array is split into first and second portions. Ex. 1001 at 3:18-25. A first logic receives and decodes the first portion of the memory address, and a second logic receives and decodes the second portion. *Id.* at 3:26-28, 3:37-40. The first logic also receives a clock signal and applies the clock signal to a selected clock output based on the first portion of the memory address. *Id.* at 3:28-36, 9:35-40. The second logic, by contrast, selectively activates a particular wordline driver based on the second portion of the memory address. *Id.* at 3:9-4:8. With this arrangement, the clock loading for the synchronous memory circuit is significantly reduced. Ex. 2001 at ¶¶34-35, 67. The first and second logics of the ’002 patent are shown in the annotated illustration below.



Paper 2 at 8.

The first and second logics operate independently of each other and apply their respective outputs directly to wordline drivers in parallel, thus reducing a timing delay in providing the clock signal to a particular wordline driver. Ex. 2001

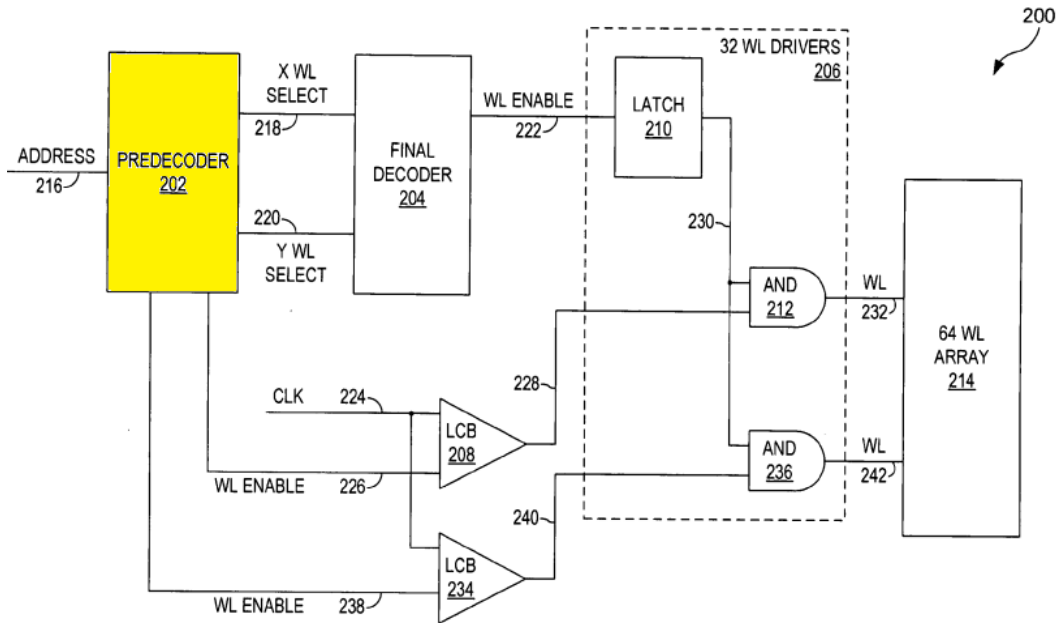
at ¶¶35, 67. These and other benefits are described in the patent’s specification. *See, e.g.,* Ex. 1001 at 1:61-2:19.

In this IPR, Petitioner submits references that are far afield from the invention of the ’002 patent and do not provide any of its benefits. Petitioner’s Ground 1 asserts that claims 1-28 and 31-37 of the ’002 patent are obvious over a single reference, Sato (Ex. 1005). Petitioner’s presentation of Sato as an obviousness ground—rather than anticipation—shows that Sato *does not* disclose all limitations of the challenged claims, and the deficiencies of Sato are readily apparent. First, Sato does not disclose or suggest a “clock signal,” as claimed. The reference is directed to an asynchronous memory system that uses multiple, non-periodic timing signals, and the person of ordinary skill in the art (POSA) would not consider any of these signals to be a clock signal.

The asynchronous memory system of Sato is fundamentally different than the synchronous memory system of the ’002 patent. As explained below, synchronous memory systems use a periodic clock signal to time all memory operations. By contrast, asynchronous memory systems, like those of Sato, are configured to receive asynchronous inputs and generate multiple, non-periodic timing signals to control the movement of data in the memory system. Accordingly, the POSA would not be motivated to modify Sato to use a periodic clock signal because the use of such a signal would be contrary to how asynchronous systems operate.

Second, even if Sato could be understood to disclose a clock signal, the reference does not disclose the claimed “clock outputs.” Petitioner argues that Sato’s predecoder PDCR generates signals $\phi x0$, $\phi x1$, $\phi x2$, and $\phi x3$ that are clock outputs. Paper 2 at 18-23. But Sato never refers to the signals $\phi x0\sim\phi x3$ as “timing signals,” much less “clocks” or “clock outputs.” Rather, Sato refers to the signals $\phi x0\sim\phi x3$ exclusively as “selection signals.” *See, e.g.*, Ex. 1005 at 5:25-28. Further, the predecoder PDCR is a black box—Sato provides no disclosure on its internal circuitry that would suggest the signals $\phi x0\sim\phi x3$ are clock outputs.

Petitioner’s Ground 2 fares even worse. This ground asserts that claims 1-17, 20-28, and 31-36 are obvious over the combination of Asano (Ex. 1006) and Itoh (Ex. 1007). Petitioner relies on Asano as the “base reference” of Ground 2 (Paper 2 at 33), but this reference fails to disclose fundamental aspects of the ’002 patent invention: The reference *does not* disclose splitting a memory address into a “first portion” and “second portion,” nor does it disclose sending the first and second portions to distinct first and second decoding logics, respectively. In Asano, the entire memory address is received and decoded by a single predecoder 202:



Ex. 1007 at Fig. 2 (highlighting added).

Petitioner attempts to remedy the deficiencies of Asano with Itoh, arguing that Asano's predecoder 202 could be implemented with a specific implementation of separate decoders disclosed by Itoh arranged in a specific way. Paper 2 at 35. But Petitioner has not sufficiently articulated why the POSA allegedly would have been motivated to combine Asano and Itoh in the way suggested by Petitioner. Petitioner and its declarant, Dr. Robert Horst, acknowledge that there are a variety of different ways to implement Asano's predecoder 202. *See, e.g.*, Ex. 1003 (Horst Decl.) at ¶118, Ex. 2005 (Horst Depo. Transcript) at 50:7-52:18. Despite this, Petitioner fails to provide *any reason* why the POSA allegedly would have selected the decoders of Itoh, specifically, from among the many different ways of implementing the predecoder 202. Petitioner's obviousness ground is therefore deficient.

Additionally, Dr. Horst's declaration (Ex. 1003) provides nothing more than a vague prior-art analysis without addressing the full language of a single claim of the '002 patent. In fact, Dr. Horst readily admits that his declaration fails to provide analysis of any of the claims as a whole. Ex. 2005 at 54:19-57:11. Petitioner relies on Dr. Horst's vague and non-specific declaration testimony in support of its obviousness grounds, but an allegation of obviousness cannot be supported without reference to the specific language of the claims, read in the context of the claim as a whole. *See Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537 (Fed. Cir. 1983). Having admittedly failed to address any of the claims as a whole in his declaration, Dr. Horst's testimony cannot properly support a conclusion of obviousness and should therefore be given little to no weight.

For at least these reasons and those detailed below, challenged claims 1-28 and 31-37 of the '002 patent should be confirmed.

II. THE ALLEGED GROUNDS OF UNPATENTABILITY

Pursuant to the Board's institution decision (Paper 6 at 18), the alleged grounds of unpatentability for this trial are:

- Ground 1 – Claims 1-28 and 31-37 are unpatentable under 35 U.S.C. § 103 over Sato; and
- Ground 2 – Claims 1-17, 20-28, and 31-36 are unpatentable under 35 U.S.C. § 103 over Asano in view of Itoh.

(Paper 2 at 2.)

III. OVERVIEW OF THE '002 PATENT

The '002 patent, titled “Dynamic Word Line Drivers and Decoders for Memory Arrays,” was filed on October 10, 2006, and issued on April 6, 2010. The patent describes wordline driver systems and methods for selectively activating a wordline driver of a group of wordline drivers. Fig. 1 of the '002 patent illustrates a wordline driver system 100 including groups of wordline drivers 104, 106 that are associated with a memory array 102 (*id.* at 2:53-56):

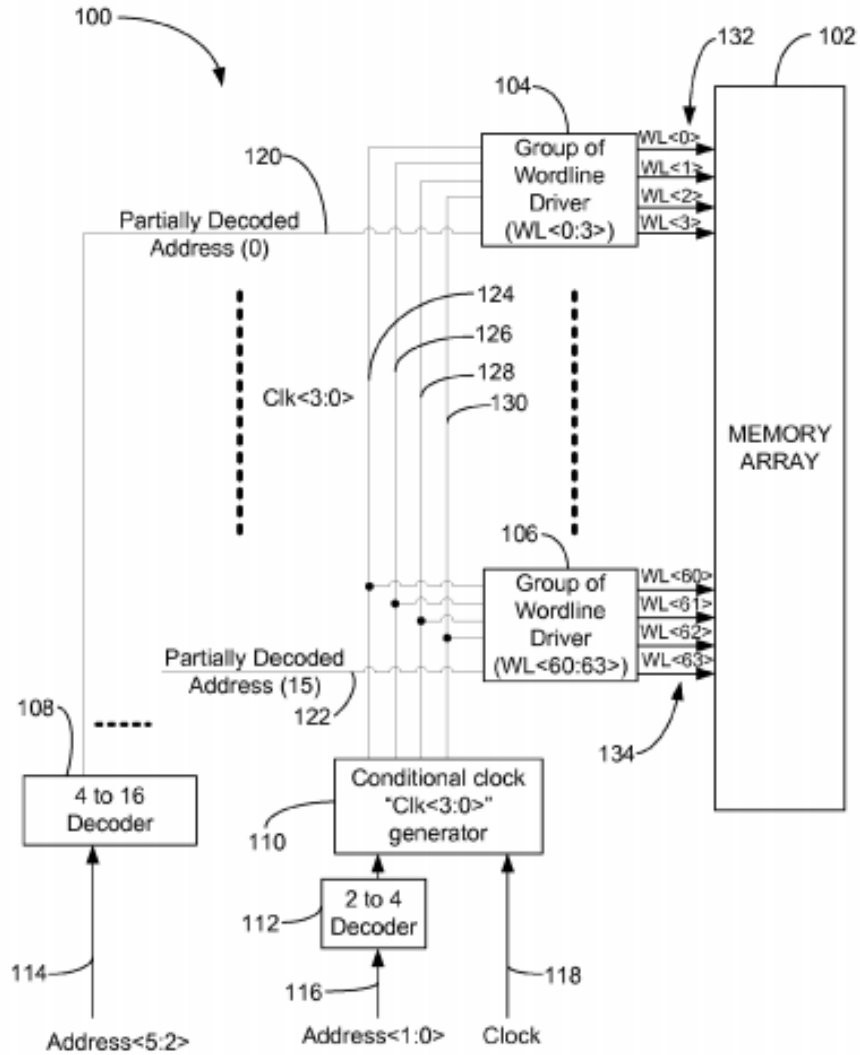
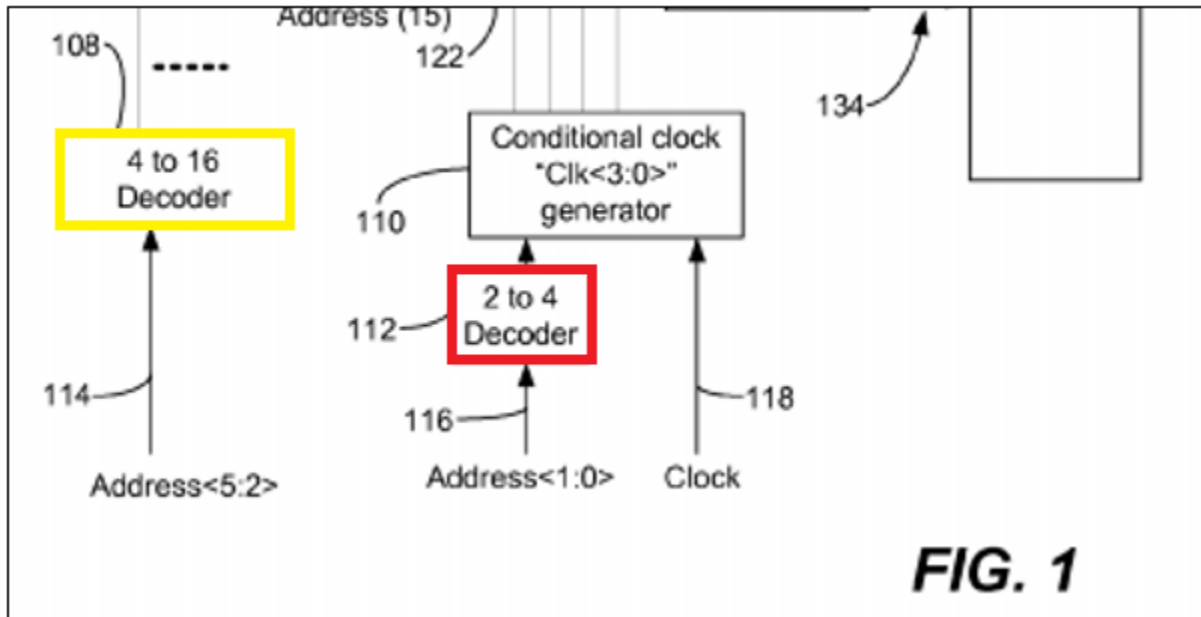


FIG. 1

Id. at Fig. 1.

In the example of Fig. 1, a six-bit memory address specifying one of sixty-four wordlines in the memory array 102 is received. *Id.* at 3:18-20. The six-bit memory address is divided into first and second portions, and a two-to-four bit memory address decoder 112 receives the first portion (*e.g.*, bits zero and one), and

a four-to-sixteen bit memory address decoder 108 receives the second portion (e.g., bits two to five) (*id.* at 3:20-25):



Id. at Fig. 1 (highlighting added).

The two-to-four bit memory address decoder 112 decodes the first portion of the memory address and provides the decoded portion to a conditional clock generator 110. *Id.* at 3:26-28. The conditional clock generator 110 receives the decoded portion and further "receives a clock signal via ... clock input 118." *Id.* at 3:28-31. The conditional clock generator 110 selectively applies the clock signal to a selected one of clock outputs 124, 126, 128, 130 based on the first portion of the memory address. *Id.* at 3:28-31, 9:35-40. The non-selected clock outputs are held at a fixed voltage level. *Id.* at 3:52-62.

Each of the clock outputs 124, 126, 128, 130 is coupled to a particular wordline driver of each of the groups of wordline drivers. *Id.* at 3:31-34. For example, in Fig. 1, the clock output 124 may be coupled to the wordline driver having the lowest number in each group (e.g., WL<0> in group 104, WL<60> in group 106, and so on). *See id.* at 3:67-4:3. In a group of wordline drivers, the driver that receives the clock signal is in a dynamic evaluation state, whereas the other three drivers of the group that do not receive the clock signal are in a static precharge state. *Id.* at 3:52-62.

The four-to-sixteen bit memory address decoder 108 decodes the second portion of the memory address and “applies a partial address input to the wordlines that are related to the decoded memory address.” *Id.* at 3:37-40. The outputs of the conditional clock generator 110 and the four-to-sixteen bit memory address decoder 108 are used together to activate a particular wordline driver. *Id.* at 3:62-4:8. More specifically, “the decoded output of the two-to-four decoder 112 with clock generator 110 and the decoded output of the four-to-sixteen bit memory address decoder 108 may be utilized via a logical AND operation” to selectively activate a wordline driver. *Id.* at 4:3-8.

The invention of the '002 patent provides numerous advantages. *Id.* at 1:61-2:19. These advantages include, among others, reduced loading on the clock signal, increased capacitive noise-coupling immunity between wordline driver outputs,

lower timing delay from a clock to a particular wordline, and reduced power consumption. *See id.*; *see also* Ex. 2001 at ¶¶34-35.

Claim 1 of the '002 patent illustrates the claimed invention:

1. A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

Id. at 10:65-11:10.

IV. CLAIM CONSTRUCTION

37 C.F.R. § 42.100(b) states that claims must be given their broadest reasonable interpretation in light of the specification (“BRI”).

“Clock Signal”

The term “clock signal,” as recited in each of the independent claims of the '002 patent, should be interpreted to mean “a periodic signal used for synchronization.” This interpretation is consistent with the plain and ordinary

meaning of the term as understood by the POSA. Ex. 2001 at ¶53. The POSA's understanding of the term is reflected, for example, by the IEEE Dictionary, which defines the term "clock signal" as "[a] periodic signal used for synchronizing events." Ex. 2002 at 9. The IEEE Dictionary is a reliable, unbiased authority that sets forth the definition of clock signal that would be understood by the POSA as of the filing date of the '002 patent. Ex. 2001 at ¶53.

Support for this interpretation is also found in the '002 patent itself. Specifically, the POSA would understand that the '002 patent describes a synchronous memory system that uses a periodic clock signal. *Id.* at ¶54. The '002 patent *does not* describe an asynchronous memory system that uses multiple, non-periodic timing signals. *Id.* This is explained below and in further detail in the attached declaration of Dr. Massoud Pedram. *Id.* at ¶¶54-69.

As explained by Dr. Pedram, certain memory systems are controlled *asynchronously*, which means that externally provided inputs to the memory system can arrive at any time, for example, driven by a memory read or write event. *Id.* at ¶¶55-60. The timing of such inputs is not synchronized with rising or falling edges of a periodic clock signal. *Id.* Thus, asynchronous memory systems are event-driven and must include control circuitry for receiving the asynchronous inputs and generating appropriately timed sequences of internal timing signals to control the movement of data in the memory. *Id.* Neither the asynchronous inputs nor the

internal timing signals are periodic, and none of them are commonly referred to as “clocks” or “clock signals.” *Id.* The duration and precise timing of the internal timing signals is key to the correct operation of the asynchronous memory system, and multiple timing constraints among external control signals and address/data signals must be satisfied. *Id.*

By contrast, in a memory system that is controlled *synchronously*, a single, periodic, synchronizing clock is used to time all memory operations. *Id.* at ¶¶61-64. In synchronous memory systems, this synchronizing clock is expressly referred to as a “clock,” “clock signal,” or an abbreviation such as “CLK” or “CK.” *Id.* Externally provided control signals and address/data signals are all synchronized with respect to the periodic clock, and the internal circuitry of the memory system operates in synchrony with the clock signal. *Id.* The timing constraints of synchronous memory systems are fundamentally different than those of asynchronous memory systems, and all such constraints are described with reference to edges of the single, periodic clock signal. *Id.*

The POSA would understand that the ’002 patent discloses a synchronous memory system that uses a periodic clock signal, rather than an asynchronous memory system. *Id.* at ¶¶65-69. The invention of the ’002 patent does not use multiple, internal timing signals for controlling the movement of data within the memory system, nor does the patent describe control logic circuitry for generating

such signals. *Id.* at ¶65. As described above, such timing signals are *necessary* for correct operation of asynchronous memory systems, but they are generally not employed in synchronous memory systems that use a periodic clock signal. *Id.* Further, as confirmed by Petitioner’s declarant Dr. Horst (Ex. 2005 at 14:16-22), the memory system of the ’002 patent uses a *single clock signal*, rather than multiple timing signals, which is consistent with synchronous systems’ use of a single, periodic clock signal. Ex. 2001 at ¶66.

Additionally, the ’002 patent does not describe any timing constraints among external control signals and address/data signals. *Id.* These timing constraints, as described above, are important considerations in asynchronous memory systems, but no such timing constraints exist in synchronous memory systems. *Id.* The ’002 patent’s lack of any description of these important aspects of asynchronous memory systems evidences that the invention is not directed to an asynchronous system but rather a synchronous system that uses a periodic clock signal. The intrinsic evidence thus supports the interpretation of the claim term “clock signal” as “a periodic signal used for synchronization.” *Id.* at ¶¶65-69.

Petitioner did not propose a construction for the term “clock signal” in its petition. *See* Paper 2 at 3-7. However, Petitioner’s expert in the related ITC proceeding involving the ’002 patent, Dr. Donald Alpert, previously provided relevant testimony. Specifically, in another IPR proceeding not directed to

the '002 patent, but addressing the meaning of the claim term “clock,” Dr. Alpert told the Board that the term “clock” should be interpreted as “a periodic signal used for synchronization.” Ex. 2004 at 3-4. Dr. Alpert stated that the “definition [‘a periodic signal used for synchronization’] is consistent with the broadest reasonable interpretation of the term [‘clock’].” *Id.* Dr. Alpert’s statement provides further support for Qualcomm’s proposed construction.

For at least these reasons, the term “clock signal” should be interpreted to mean “a periodic signal used for synchronization.”

V. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of the trial in this proceeding, Qualcomm accepts Petitioner’s proposed education and experience level of one of ordinary skill in the art, as modified by the Board’s institution decision. *See* Paper 2 at 2; Paper 6 at 6. Thus, for purposes of the trial in this proceeding, the POSA for the '002 patent would have had an undergraduate degree in electrical engineering, or a related field, and three years of experience in the design of memory systems and circuits. Alternatively, a person of ordinary skill with less than the amount of experience noted above would have had a correspondingly greater amount of educational training such a graduate degree in a related field. *See id.*

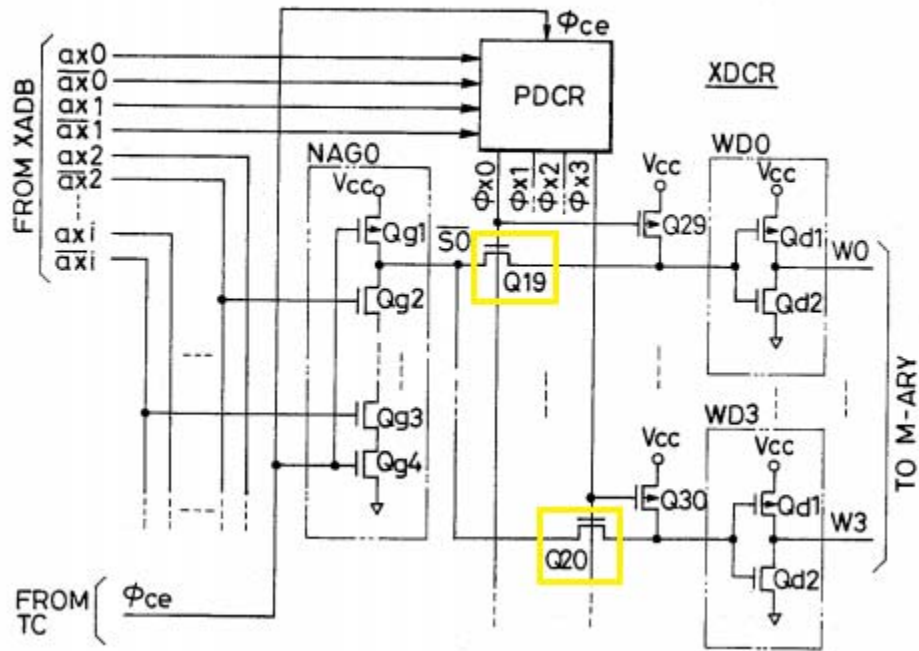
VI. OVERVIEW OF THE CITED REFERENCES

A. Overview of Sato

U.S. Patent No. 4,951,259 (“Sato”), titled “Semiconductor Memory Device with First and Second Word Line Drivers,” relates generally to semiconductor memory devices. Ex. 1005 at 1:6-9. Sato was filed on February 18, 1988, and issued on August 21, 1990.

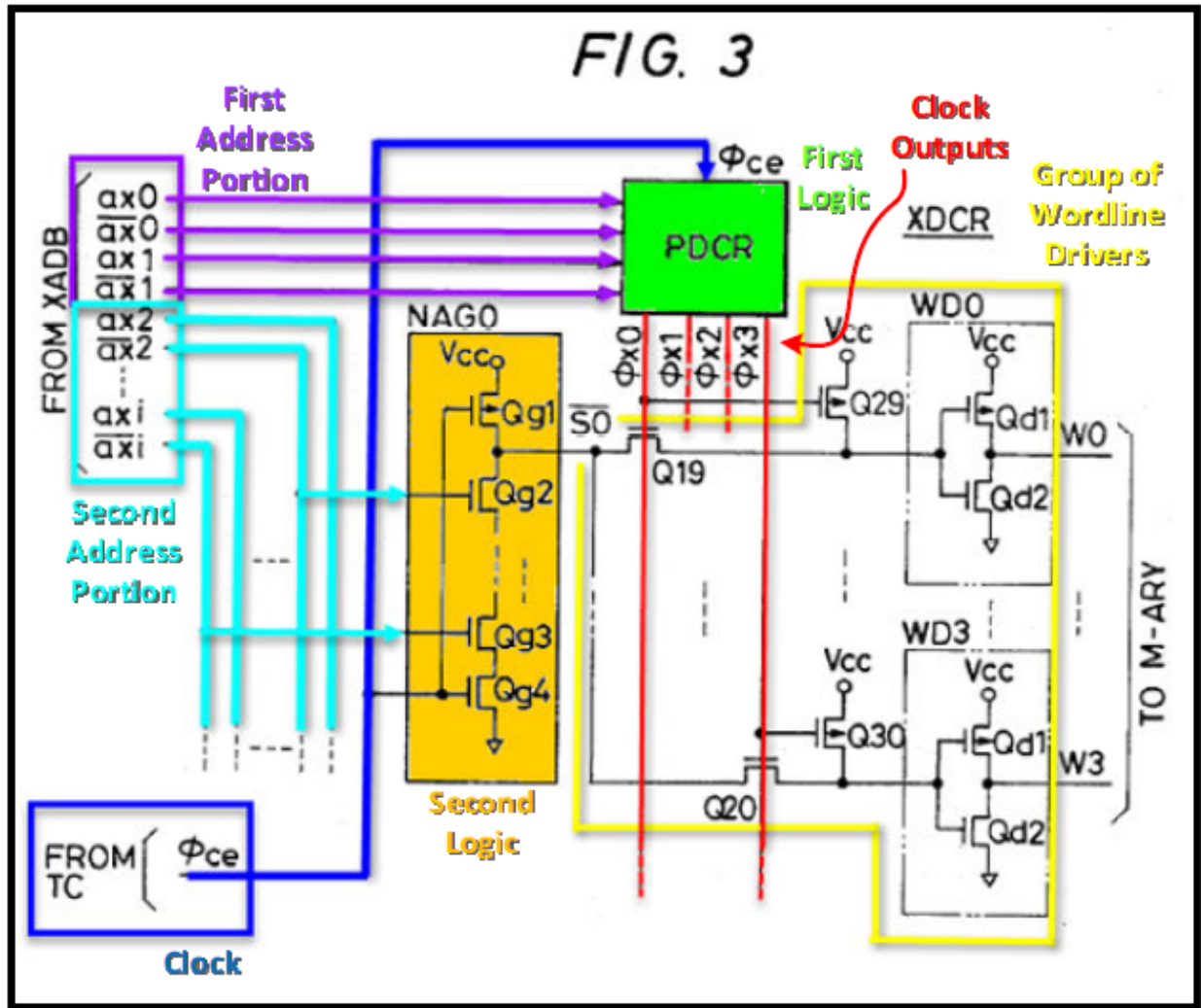
Sato explains that “[i]n large memory arrays, the word line driver circuits can place large capacitive loads on the output of the logic decoding circuit because the word line driver transistors must be relatively large. This large load on the logic decoding circuitry adversely effects the operating speed of the memory.” *Id.* at Abstract. To reduce this load, Sato describes a “switching arrangement [that] is provided between the output of the logic decoding circuitry and the word line drivers.” *Id.* In Fig. 3 of Sato, the switching arrangement comprises capacitance cut MOSFETs Q19 and Q20 disposed between output terminals of decoding NAND gate circuit NAG0 and the input terminals of wordline drivers WD0-WD3 (*id.* at 9:60-65):

FIG. 3



Id. at Fig. 3 (highlighting added). Through the use of the capacitance cut MOSFETs Q19 and Q20, the decoding NAND gate circuit NAG0 is isolated from the wordline drivers WD0-WD3, and the capacitive load on the output terminals of the decoding NAND gate circuit NAG0 is thereby reduced. *Id.* at 2:21-35, 10:60-66. The capacitance cut MOSFETs are controlled by selection signals ϕ_{x0} , ϕ_{x1} , ϕ_{x2} , and ϕ_{x3} generated by predecoder PDCR. *Id.* at 9:68-10:4.

The petition cites to Fig. 3 of Sato as allegedly meeting claim limitations of the '002 patent. *See, e.g.*, Paper 2 at 9-32. Petitioner provides an annotated Fig. 3 showing the alleged disclosure of certain claim limitations:



Id. at 10. Fig. 3 of Sato depicts “a circuit a diagram showing [an] X address decoder of [a] static RAM.” Ex. 1005 at 2:57-39.

The X address decoder of Fig. 3 includes a predecoder PDCR that “decodes the lower 2-bit complementary internal address signals ax0 and ax1 supplied thereto ... and generates selection signals $\phi_{x0} \sim \phi_{x3}$.” *Id.* at 5:25-28. The “selection signals $\phi_{x0} \sim \phi_{x3}$ are formed selectively in accordance with the complementary internal address signals ax0 and ax1.” *Id.* at 5:28-31. Further, “[t]he timing signal

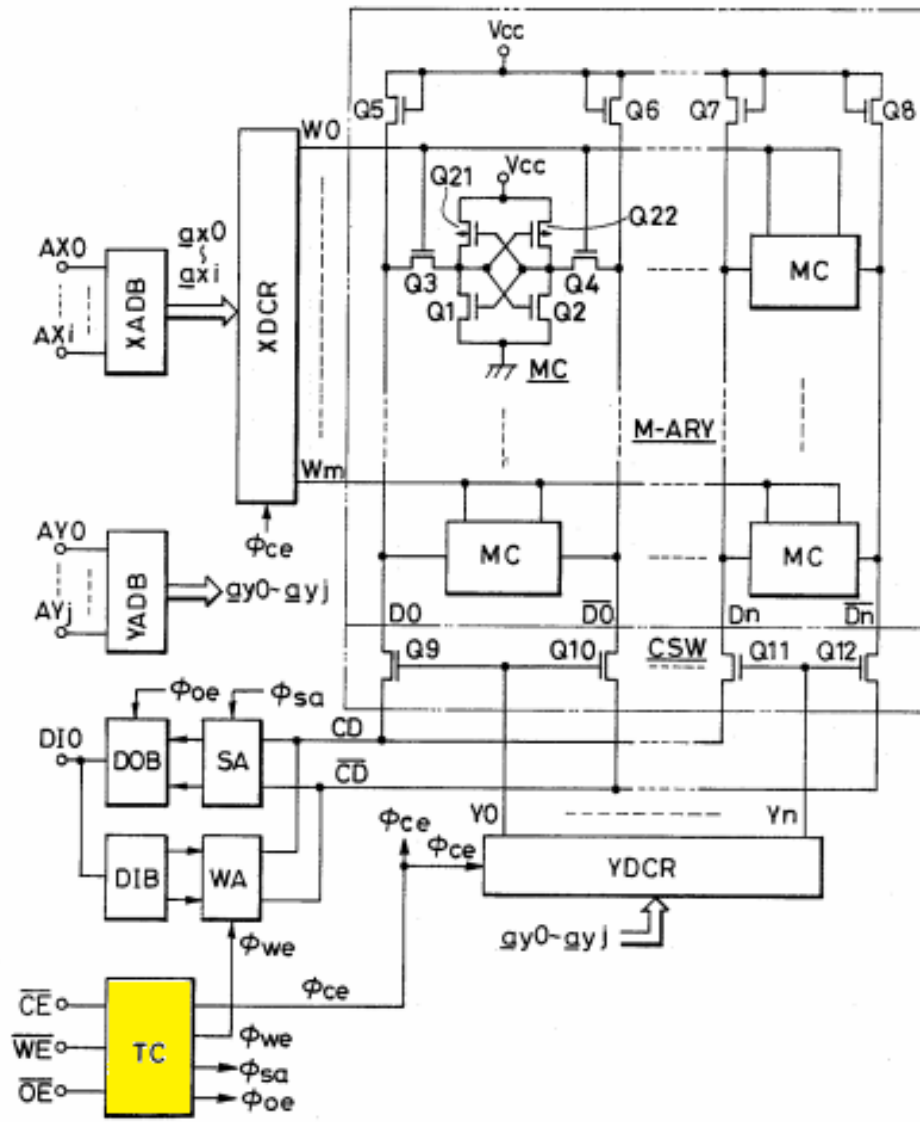
ϕ_{ce} ... is supplied to the pre-decoder PDCR,” and the PDCR’s “output signal, that is, the selection signal $\phi_{x0}\sim\phi_{x3}$, is generated in accordance with this timing signal ϕ_{ce} .” *Id.* at 10:36-39.

As seen in the annotated Fig. 3 above, Petitioner argues that the predecoder PDCR meets the claimed “first logic,” and that the signals $\phi_{x0}\sim\phi_{x3}$ disclose the claimed “plurality of clock outputs” of the first logic. But Sato never refers to the signals $\phi_{x0}\sim\phi_{x3}$ as “timing signals,” much less “clocks” or “clock outputs.” Rather, Sato refers to the signals $\phi_{x0}\sim\phi_{x3}$ exclusively as “selection signals” to reflect the function and purpose of those signals, which is to selectively turn on one of the capacitance cut MOSFETs. *See, e.g., id.* at 5:25-28. In contrast, the first logic output of the ’002 patent claims is a clock signal provided to wordline drivers for synchronization. Sato also provides no details on the internal circuitry of the predecoder PDCR that would suggest the signals $\phi_{x0}\sim\phi_{x3}$ are clock outputs. Likewise, Petitioner argues that the signal ϕ_{ce} discloses the claimed “clock signal,” but Sato only refers to the signal ϕ_{ce} as a “timing signal” or “selection control signal.” *See, e.g., id.* at 3:59-61.

The X address decoder of Fig. 3 further includes NAND gate circuits NAG0-NAGk, though the illustration “shows only the NAND gate circuit NAG0.” *Id.* at 9:34-35. As seen in Figs. 1 and 3 of Sato, the NAND gate circuits NAG0-NAGk receive (i) complementary internal address signals $ax2\sim axi$, and (ii) the selection

control signal ϕ_{ce} . The NAND gate circuits NAG0-NAG k use these received signals in generating selection signals $\overline{S0} \sim \overline{Sk}$. *See, e.g., id.* at 5:66-6:4 (“ $\overline{S0}$... is set to the low logic level in synchronism with the timing signal ϕ_{ce} when all the inversed internal address signals $ax2 \sim axi$ are at the high logic level”).

The timing signal ϕ_{ce} and additional timing signals ϕ_{we} , ϕ_{sa} , and ϕ_{oe} are generated by a timing control circuit TC shown in Fig. 4 of Sato:



Id. at Fig. 4 (highlighting added). The timing control circuit TC generates the ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} timing signals “on the basis of a chip enable signal $\overline{CE}$, a write enable signal $\overline{WE}$ and an output enable signal $\overline{OE}$ supplied as control signals from outside.” *Id.* at 5:7-12. No clock signal is used in the generation of the ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} timing signals. Ex. 2001 at ¶90.

The ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} signals are internal timing signals that control different portions of Sato’s memory system. *Id.* at ¶¶90-95. The ϕ_{ce} signal, as described above, is a “selection control signal” that is provided to both the predecoder PDCR and NAND gate circuits NAG0-NAGk and subsequently provided to a selected output of these respective circuits. *Id.* at 3:59-61, 5:43-6:59, 10:36-39. The ϕ_{we} signal is a timing signal that controls a write amplifier WA (*id.* at 4:63-5:6), the ϕ_{sa} signal is a timing signal that controls a sense amplifier SA (*id.* at 4:40-46), and the ϕ_{oe} signal is a timing signal that controls a data output buffer DOB (*id.* at 4:47-57).

In contrast to the ’002 patent, Sato is directed to asynchronous memory systems and does not disclose a synchronous memory system that uses a periodic clock signal. Ex. 2001 at ¶100-04. As explained in Section IV above, asynchronous memory systems include control circuitry for receiving external inputs and generating appropriately timed sequences of internal timing signals for controlling movement of data in the memory. Sato’s timing control circuit TC is an example of

such “control circuitry”: It receives external input signals $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ and generates multiple internal timing signals ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} based on the inputs for different components and operations. *Id.* at ¶102. Thus, in Sato, there is no single, periodic clock signal to which all memory operations are synchronized, but rather multiple internal timing signals ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} for controlling different components of the memory. Moreover, Sato *does not* suggest that any of the inputs $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ or outputs ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} of the timing control circuit TC are periodic. *Id.* at ¶103. Rather, the only relevant disclosure in Sato indicates that the signal ϕ_{ce} is *not periodic*, stating that the signal ϕ_{ce} is “kept at a high level” based on a value of the chip enable signal $\overline{CE}$. Ex. 1005 at 3:59-65; Ex. 2001 at ¶96.

Additionally, the alleged “first logic” and “second logic” of Sato operate in a serial manner that differs from the parallel arrangement described in the ’002 patent. Specifically, in the ’002 patent, the first and second logics operate independently of each other and apply their respective outputs directly to wordline drivers in parallel, thus reducing a timing delay in providing the clock signal to a particular wordline driver. *See, e.g.*, Ex. 1001 at Fig. 1. By contrast, in Sato, outputs of the NAND gate circuits (*i.e.*, the alleged “second logic”) are not applied to the wordline drivers until selected by outputs of the predecoder PDCR (*i.e.*, the alleged “first logic”), which are received by the capacitance cut MOSFETs (*e.g.*, Q19, Q20, etc.). Ex. 1005

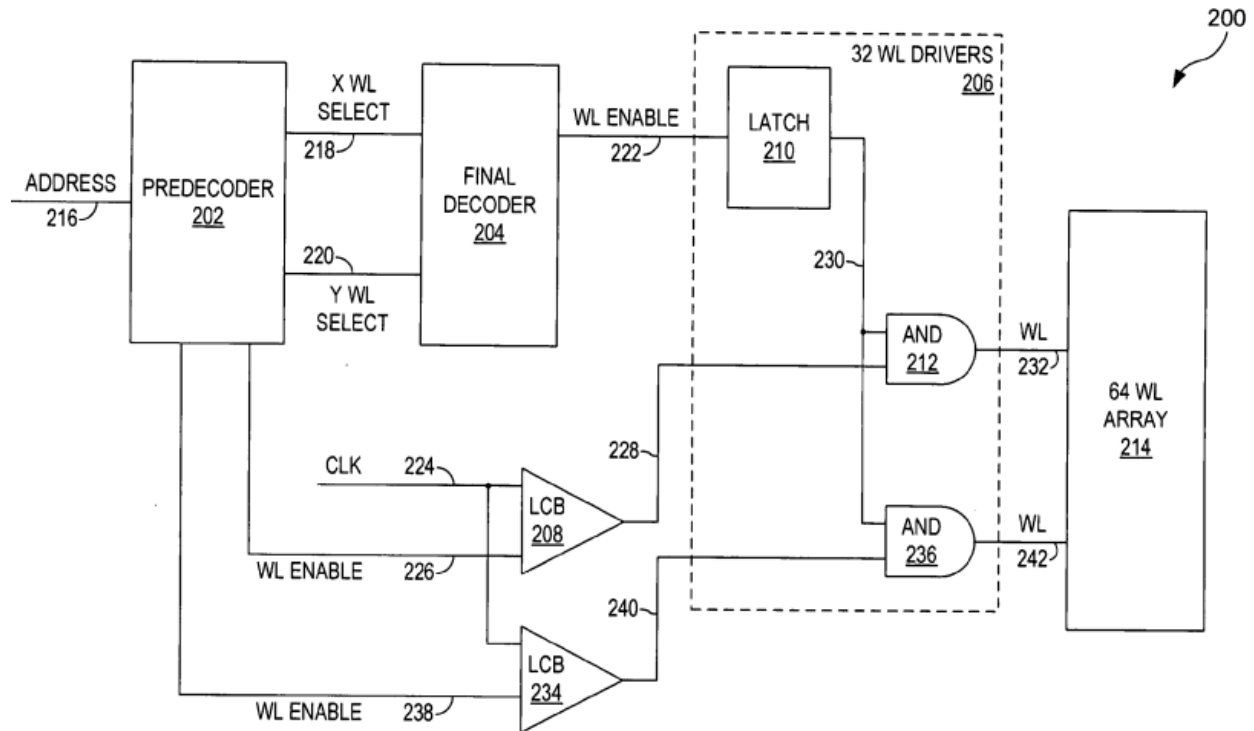
at 9:68-10:4. With this slower serial operation, Sato thus fails to achieve the advantage of reduced timing delay described in the '002 patent.

B. Overview of Asano

U.S. Patent Publication No. 2006/0098520 (“Asano”), titled “Apparatus and Method of Word Line Decoding for Deep Pipelined Memory,” relates generally to memory arrays, and more particularly to wordline decoding for memory arrays. Ex. 1006 at ¶[0001]. Asano was filed on November 5, 2004, and published on May 11, 2006.

The purpose of Asano is to reduce the number of latches in a deep pipeline wordline decoder. *Id.* at Abstract. Asano explains that conventional systems used a single local clock buffer (LCB) to provide a driving signal to wordline drivers, and that these conventional systems required “a large number of latches.” *Id.*; *see also id.* at Fig. 1 (prior-art system with single LCB 108 driving wordline drivers 106). “To reduce this latch usage,” Asano provides a system in which multiple “LCBs are employed, such that one latch can enable an increased number of [wordlines].” *Id.* at Abstract. This reduces the area occupied by the latches and results in less power consumption. *Id.*

Petitioner cites to Fig. 2 of Asano as allegedly meeting limitations of the '002 patent. *See, e.g.*, Paper 2 at 33-50. This figure is a block diagram of a memory 200 (Ex. 1006 at ¶[0015]):



Id. at Fig. 2.

“To begin the access cycle for the memory 200,” a 6-bit memory address is received at a predecoder 202. *Id.* at ¶[0016]. In contrast to what is described in the ’002 patent, the 6-bit memory address is *not* split into first and second portions that are sent to respective first and second logics. Rather, in Asano, all six bits are received by the single predecoder 202. *See id.* Further, Asano’s two-page description provides no details on the internal circuitry of the predecoder 202, and there is nothing in the reference suggesting that the predecoder 202 would include distinct first and second logics. Ex. 2001 at ¶¶127-29.

Using the received 6-bit memory address, the predecoder 202 generates an 8-bit X wordline select signal and a 4-bit Y wordline select signal that are provided to

a final decoder 204. Ex. 1006 at ¶[0016]. Using the received X wordline select signal and Y wordline select signal, the final decoder 204 “determines which of ... 32 wordline drivers 206 are to be enabled.” *Id.* at ¶[0017]. Each of the 32 wordline drivers 206 drives two wordlines, and each wordline driver includes a latch and two AND gates. *Id.* at ¶[0019]. “For the sake of illustration, a single latch 210, first AND gate 212, and a second AND gate 236 are depicted [in Fig. 2].” *Id.* “[T]he latch 210 receives a wordline enable signal [from the final decoder 204] through the fourth communication channel 222, where the signal is latched in step 310 and 312.” *Id.*

The predecoder 202 also generates selection signals based “on the most significant bit” of the received 6-bit memory address. *Id.* at ¶[0019]. The selection signals are provided to LCBs 208, 234, and each of the LCBs 208, 234 further “receive[s] a clocking signal through a seventh communication channel 224.” *Id.* at ¶[0018]. The LCBs 208, 234 “provide clocking signals to the wordline drivers 206” based on the received selection signals and clocking signal. *Id.* at ¶¶[0017]-[0018]. More specifically, Asano indicates that one of the LCBs 208, 234 is enabled by the received selection signal, whereas the other LCB is not enabled. *Id.* at claims 7, 11.

The enabled LCB propagates the clocking signal to the AND gate 212 or 236 to which it is connected, thus selecting one of the two AND gates 212, 236. *Id.*

at ¶[0019]. The non-enabled LCB does not propagate the clocking signal. *See id.* A wordline driver is enabled and a wordline signal is “output ... to a wordline within the 64 wordline array” when the clocking signal from the enabled LCB is ANDed with an enable signal from the final decoder 204. *See id.*

C. Overview of Itoh

Ex. 1007 (“Itoh”) is a portion of a book entitled “VLSI Memory Chip Design.” Itoh discusses an address decoder for DRAM circuits and states that “[a] predecoding scheme achieves a faster decoding and area reduction of [the] decoder,” as compared to other decoding schemes. *Id.* at 14. Itoh provides a Figure 3.46 that “compares predecoding schemes” (*id.*):

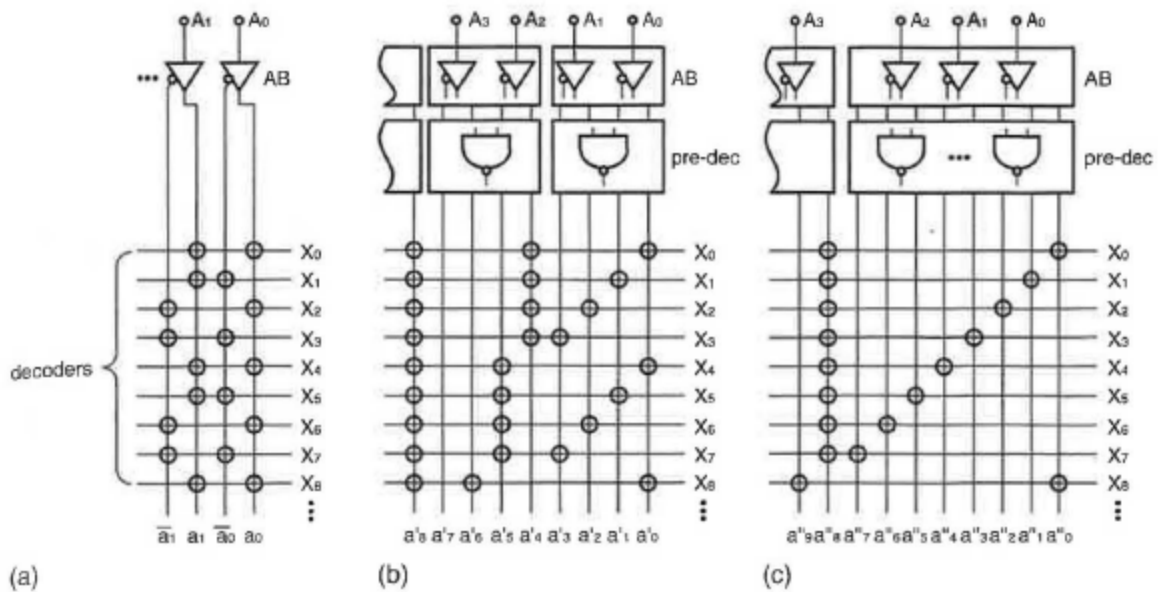


Fig. 3.46. Predecoding [3.4]. (a) no predecoding; (b) 2-bit predecoding; (c) 3-bit predecoding

Id. at 15.

“Direct decoding, 2 bit predecoding, and 3 bit predecoding are shown in Figs. 3.46a-c, respectively.” *Id.* at 14. The direct decoding shown in Fig. 3.46a shows circuit components that each receive a single input (*e.g.*, A_1) and generate two outputs (*e.g.*, $\overline{a_1}$ and a_1). *Id.* at 15. With reference to Figs. 3.46b-c, Itoh states that “[e]ach 2 bit predecoder can select one of four address input lines coming to the decoders ...[,] while each 3 bit decoder can select one of eight address input lines.” *Id.* Petitioner asserts that Figs. 3.46a-c of Itoh disclose a 1-to-2 bit decoder, 2-to-4 bit decoder, and 3-to-8 bit decoder, respectively. *See, e.g.*, Paper 2 at 38-39.

VII. SATO DOES NOT RENDER CLAIMS 1-28 AND 31-37 OBVIOUS (GROUND 1)

Petitioner asserts in Ground 1 that claims 1-28 and 31-37 are unpatentable under § 103 as obvious over Sato. Petitioner’s presentation of Sato as an obviousness ground, rather than anticipation, shows that the reference does not disclose all limitations of the claims. Despite this, however, Petitioner ignores the proper obviousness inquiry mandated by *Graham v. John Deere Co.*, 383 U.S. 1 (1966), and fails to provide *any explanation* of the differences between the claims and the disclosure of Sato. Ground 1 is deficient for at least this reason.

In any event, the deficiencies of Sato are readily apparent. Sato is directed to an asynchronous memory system—in contrast to the synchronous memory system of the ’002 patent—and fails to disclose the clock signal and clock output limitations of the claims. Further, Petitioner *does not* argue that Sato could allegedly be

modified to meet the missing limitations, nor does Petitioner provide any reasons why the POSA would allegedly be motivated to make such modifications. For these reasons and those explained below, the patentability of challenged claims 1-28 and 31-37 should be confirmed over Sato.

A. The Petition Fails to Establish a *Prima Facie* Case of Obviousness over Sato.

Ground 1 of the petition alleges that claims 1-28 and 31-37 are obvious over Sato. Paper 2 at 1-2. Because the petition ignores the *Graham* factors and fails to provide any explanation of the differences between the claimed subject matter and the prior art, claims 1-28 and 31-37 should be upheld over Sato.

The Board has recognized that the question of obviousness is resolved on the basis of the four *Graham* factors:

- (1) the scope and content of the prior art;
- (2) *the differences between the claimed subject matter and the prior art*;
- (3) the level of ordinary skill in the art; and
- (4) objective evidence of nonobviousness.

See, e.g., Zetec, Inc. v. Westinghouse Elec. Co., LLC, IPR2014-00384, Paper 10 at 11-12 (P.T.A.B. July 23, 2014) (citing *Graham*, 383 U.S. at 17-18) (emphasis added). The identification of the differences between the claimed subject matter and the prior art is central to an obviousness analysis. Put simply, the obviousness or

nonobviousness of a claimed invention cannot be determined without first understanding how the claimed invention differs from the prior art.

Here, Petitioner has not identified any differences between the claimed subject matter of the '002 patent and Sato. *See* Paper 2 at 9-32, 51-81. Petitioner instead argues that Sato discloses each and every limitation of the challenged claims. *See id.*; *see also* Ex. 2005 (Horst Depo. Transcript) at 47:8-13 (“I believe [the claims of the '002 patent] are anticipated [by Sato], yes.”). This is erroneous—Sato fails to disclose multiple limitations, as explained below—and it shows that Petitioner has not identified any differences between the claims and Sato. Although Petitioner uses some ambiguous language with respect to the “clock signal” limitation (“[t]iming signal ϕ_{ce} represents or renders obvious a clock signal,” *see* Paper 2 at 14), Petitioner elsewhere argues that the signal ϕ_{ce} expressly discloses this limitation. *See, e.g., id.* at 17, 19, 21, 22 (referring to the signal ϕ_{ce} as a “clock signal”). Having identified no differences between the claimed subject matter of the '002 patent and Sato, Petitioner failed to comply with *Graham* and has not established a *prima facie* case of obviousness.

Further, Petitioner’s obviousness argument relies on the declaration of Dr. Horst (Ex. 1003) for support, but the declaration never addresses the full language of a single claim of the '002 patent. An allegation of obviousness cannot be supported without reference to the specific language of the claims, read in the

context of the claim as a whole, *see Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537 (Fed. Cir. 1983), and Dr. Horst’s testimony therefore does not support a conclusion of obviousness over Sato and should be given little to no weight.

Claims 1-28 and 31-37 should be upheld over Sato for at least these reasons.

B. Sato Does Not Teach or Suggest the “Clock Signal” Required by the Claims.

Independent claims 1, 7, 11, 17, 21, and 23-27 recite the term “clock signal.” Petitioner argues that Sato’s signal ϕ_{ce} meets this limitation (Paper 2 at 14-17), but this is erroneous. Ex. 2001 at ¶¶87-123. Sato never refers to the signal ϕ_{ce} as a “clock signal” and instead consistently refers to it as a “selection control signal” or a “timing signal.” *See, e.g.*, Ex. 1005 at 3:59-61. Moreover, Sato’s signal ϕ_{ce} is not a periodic signal used for synchronization, as required under the proper construction of the term “clock signal.” Sato states that the signal ϕ_{ce} is “kept at a high level” based on a chip enable signal $\overline{CE}$, thus indicating that it is not periodic. *Id.* at 3:62-65. And as explained below, Sato’s disclosure of an asynchronous memory system with multiple internal timing signals further indicates that the signal ϕ_{ce} is not periodic.

1. Sato’s Selection Control Signal ϕ_{ce} is Not a “Periodic Signal Used for Synchronization,” As Required Under the Proper Construction of the Term “Clock Signal.”

As explained in Section IV above, the claim term “clock signal” should be interpreted to mean “a periodic signal used for synchronization.” Sato’s selection

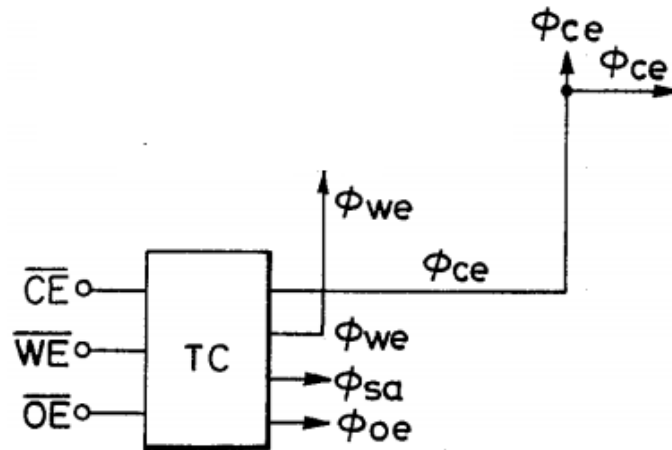
control signal ϕ_{ce} is not periodic and is therefore not a clock signal. Ex. 2001 at ¶¶88-99.

Sato provides no indication that the selection control signal ϕ_{ce} is periodic. *See generally* Ex. 1005. The reference never refers to the signal ϕ_{ce} as being regular or periodic and includes no signal timing diagrams illustrating the shape of the signal over time. *See id.* Although the signal ϕ_{ce} is mentioned throughout Sato, only one portion of the reference provides an indication of the values that the signal takes on over time. That portion states that the signal ϕ_{ce} is “kept at a high level” under the control of a chip enable signal $\overline{CE}$:

A timing signal ϕ_{ce} (a selection control signal) is supplied, too, from a later-discussed timing control circuit TC to the X address decoder XDCR. *This timing signal ϕ_{ce} is generated in accordance with a chip enable signal $\overline{CE}$ supplied as a control signal from outside and is kept at a high level* under the selection state of this CMOS static RAM.

Id. at 3:59-65 (emphasis added). As explained by Dr. Pedram, this means that the signal ϕ_{ce} takes on a value opposite that of the chip enable signal $\overline{CE}$, such that when the signal $\overline{CE}$ is low, the signal ϕ_{ce} is “kept at a high level.” Ex. 2001 at ¶96. Sato’s disclosure of keeping the selection control signal ϕ_{ce} at a certain level based on a value of the chip enable signal $\overline{CE}$ does not suggest that the signal ϕ_{ce} is periodic.

Moreover, Sato also provides no indication that the chip enable signal $\overline{CE}$ is periodic. The chip enable signal $\overline{CE}$ is one of multiple inputs to a timing control circuit TC. Ex. 1005 at 5:7-12. Specifically, the timing control circuit receives an externally provided chip enable signal $\overline{CE}$ and other inputs (write enable signal $\overline{WE}$, output enable signal $\overline{OE}$) and uses these inputs to generate multiple internal timing signals ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} (*id.*):



Id. at Fig. 4. Sato does not disclose or suggest that the chip enable signal $\overline{CE}$ or any of the other inputs to the timing control circuit TC are periodic.

In fact, as explained by Dr. Pedram, the POSA would understand that the chip enable signal $\overline{CE}$ is *not periodic*. Ex. 2001 at ¶¶97-98. The chip enable signal $\overline{CE}$ is generally kept at a high value, and it assumes a low value only when the memory of Sato is accessed for read or write operations. *Id.* Because the signal ϕ_{ce} is controlled by the chip enable signal $\overline{CE}$ and takes on a value opposite of the signal $\overline{CE}$, it follows that the signal ϕ_{ce} is generally low and takes on a high value only

when the memory is accessed for reading or writing. *Id.* Access patterns to a static RAM, such as that disclosed by Sato, are determined by the access needs of the component or device using the static RAM as memory. *Id.* These access patterns are generally highly irregular, and Sato does not suggest that its static RAM would be accessed in a regular manner. *Id.* Given these irregular access patterns, the POSA would understand that the chip enable signal $\overline{CE}$ and the selection control signal ϕ_{ce} of Sato are not periodic. *Id.*

In sum, Sato's selection control signal ϕ_{ce} is not a periodic signal used for synchronization, and the reference therefore does not meet the "clock signal" limitation of the challenged claims. For these additional reasons, claims 1-28 and 31-37 are not obvious over Sato.

2. Sato Discloses an Asynchronous Memory System That Does Not Use a Periodic Clock Signal.

Sato discloses an asynchronous memory system. Ex. 2001 at ¶¶100-05. The POSA would understand that Sato's asynchronous memory system does not use a periodic clock signal for synchronization, as required by the '002 patent claims. Further, asynchronous systems are not configured to use a periodic clock signal, and the POSA therefore would not be motivated to modify Sato to use such a signal.

As explained by Dr. Pedram, asynchronous memory systems require control logic circuitry for receiving asynchronous inputs to the memory system. Ex. 2001 at ¶101. These inputs can arrive at any time and are not synchronized with edges of

a periodic clock signal. *Id.* Based on these inputs, the control logic circuitry generates appropriately timed sequences of internal timing signals to control the movement of data in memory. *Id.* The internal timing signals are not periodic and are instead generally pulses or strobes without a periodic component. *Id.* Thus, asynchronous systems do not use a periodic clock signal and instead use multiple, non-periodic internal timing signals. *Id.*

While Sato does not expressly refer to its memory system as being asynchronous, the POSA would understand it as such because it is an exact match of the asynchronous systems described above. *Id.* at ¶102. In Sato, the timing control circuit TC is the control logic circuitry required by asynchronous memory systems. *Id.* The timing control circuit TC receives external input signals $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ and generates multiple internal timing signals ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} based on the inputs. Ex. 1005 at Fig. 4, 5:7-12. Thus, in Sato, there is no single, periodic clock signal to which memory operations are synchronized, but rather multiple internal timing signals ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} for controlling different components of the memory system. Ex. 2001 at ¶102. Moreover, Sato *does not* suggest that any of the signals ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} are periodic, which is consistent with asynchronous systems' use of multiple, non-periodic internal timing signals. *Id.* at ¶103.

The asynchronous memory system of Sato is fundamentally different than the synchronous memory system of the '002 patent. *Id.* at ¶104. As explained above in Section IV, synchronous memory systems use a periodic clock signal to time all memory operations. By contrast, asynchronous memory systems, like those of Sato, are not configured to use a periodic clock signal—instead, they use non-periodic timing signals generated based on asynchronous, external inputs. Accordingly, the POSA would not be motivated to modify Sato to use a periodic clock signal because the use of such a signal would be contrary to how asynchronous systems operate. *Id.*

Sato does not meet the “clock signal” limitation of the challenged claims for these additional reasons, and claims 1-28 and 31-37 are therefore not obvious over Sato.

3. Petitioner’s Assertion That Sato’s Selection Control Signal “Represents or Renders Obvious a Clock Signal” Is Erroneous.

The petition asserts that Sato’s selection control signal ϕ_{ce} “represents or renders obvious a clock signal” and provides a number of arguments in support of its assertion. Paper 2 at 14-17. But all of these arguments are erroneous.

The petition argues that “clock” is another name for a timing signal. Paper 2 at 15, citing Ex. 1003 (Horst Decl.) at ¶64. Neither Petitioner nor Dr. Horst provide any evidence or reasoning to support their argument, and it is wrong: The words “clock signal” and “timing signal” are not interchangeable, nor would the POSA

have understood them as such. Ex. 2001 at ¶108. In fact, Petitioner’s own reference, Itoh, reinforces the fact that clock signals and timing signals are different. Specifically, Itoh provides signal timing diagrams for an asynchronous memory system in Figure 6.14 and does not refer to any of its signals as being a “clock signal”:

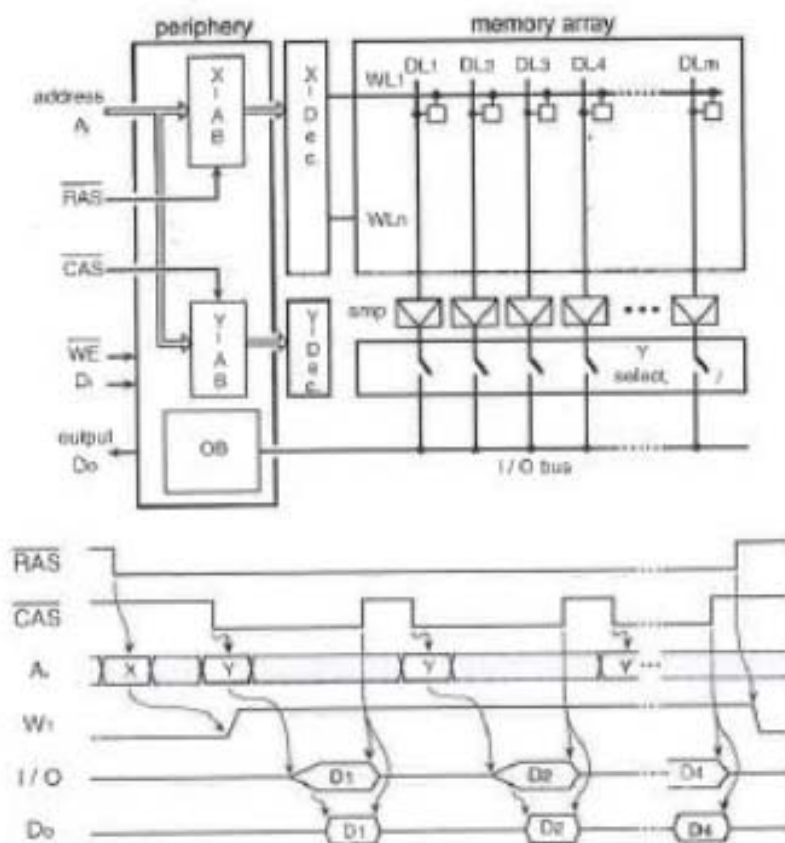
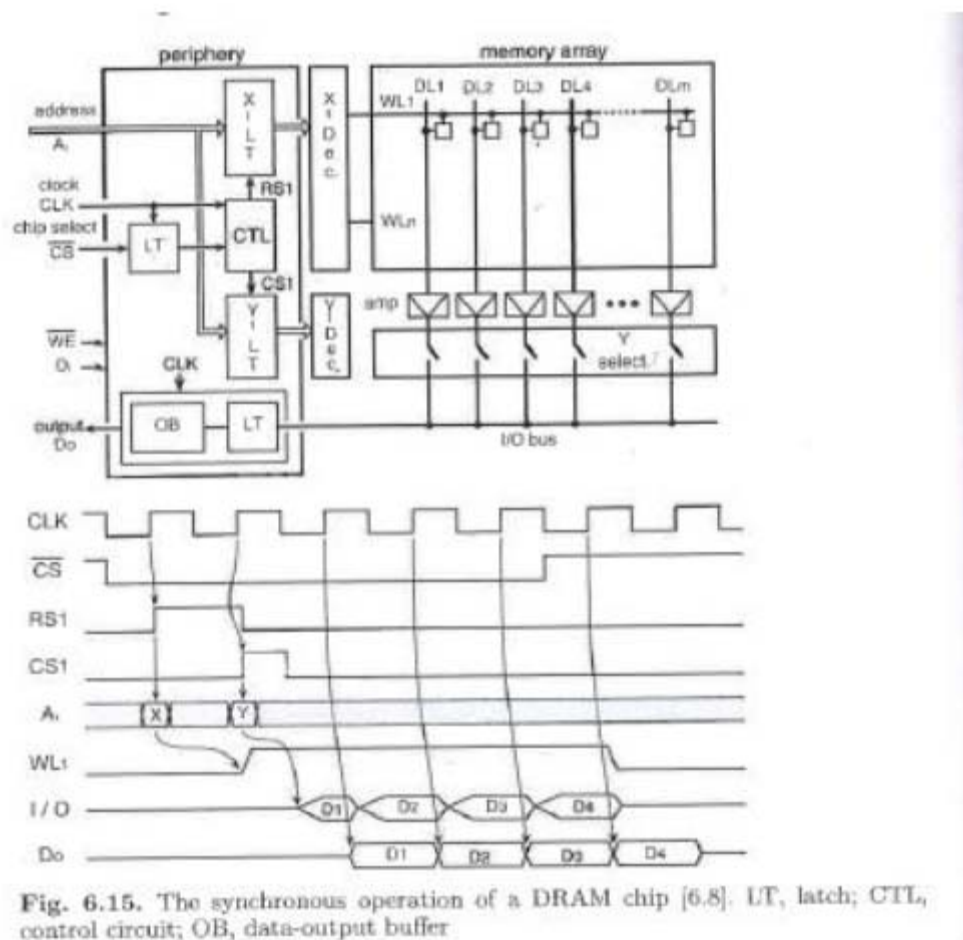


Fig. 6.14. The asynchronous operation of a DRAM chip [6.8]. AB, address buffers; OB, data-output buffer; X, row; Y, column.

Ex. 2003 at 18. The figure shows signal timing diagrams for asynchronous input signals $\overline{RAS}$ and $\overline{CAS}$. Ex. 2001 at ¶¶59, 108. Internal activities of the memory (e.g., activation of a selected wordline $W1$, the appearance of data on an I/O bus, etc.) are initiated by asynchronous transitions on the signals $\overline{RAS}$ and $\overline{CAS}$. *Id.*

Notably, Itoh does not refer to the signals $\overline{RAS}$ and $\overline{CAS}$ —or any other signals of the asynchronous memory system—as being “clock signals.” *Id.* at ¶¶59-60, 108. If anything, the non-periodic $\overline{RAS}$ and $\overline{CAS}$ signals may be understood by the POSA as being “timing signals.” *Id.*

By contrast, Figure 6.15 of Itoh provides signal timing diagrams for a synchronous memory system having a periodic clock signal that is specifically referred to as “CLK”:



Ex. 2003 at 19. In the synchronous memory system depicted above, all events occur in synchrony with the periodic clock signal CLK. Ex. 2001 at ¶¶62, 108. The fact that Itoh refers to the periodic signal in the synchronous memory system as a “CLK” signal and does not refer to any of the non-periodic signals in the asynchronous memory system as such reinforces the proposition that asynchronous timing signals are different than periodic clock signals. *Id.* at ¶108.

Petitioner also argues that “the Greek symbol phi (ϕ) is frequently used in the art to indicate clock signals” (Paper 2 at 15, citing Ex. 1003 at ¶64) but this, too, is wrong. As explained by Dr. Pedram, the POSA would understand that the symbol ϕ is used in the art to denote a phase signal, not a clock signal. Ex. 2001 at ¶109. In Sato, the ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} signals are phase signals, with positive (*i.e.*, high) and negative (*i.e.*, low) phase levels that determine the signals’ precise effects on the memory system. *Id.* Petitioner and Dr. Horst provide no evidence or explanation to support their assertion that the symbol ϕ is indicative of a clock signal, and it is wrong.

Petitioner further argues that Sato’s selection control signal ϕ_{ce} “performs the same function as the clock signal in the ’002 patent.” Paper 2 at 15, citing Ex. 1003 at ¶64. But a synchronous circuit design, as used in the ’002 patent, is fundamentally different than the asynchronous design of Sato, such that the selection control signal ϕ_{ce} does not perform the same function as the claimed clock signal. Ex. 2001

at ¶104. For example, in a synchronous circuit design, each function is timed with the clock signal's rising or falling edge. *Id.* at ¶¶62-64. Accordingly, to ensure the system's proper functioning, each function needs to finish its operation within a clock period with some margin. If Sato's selection control signal ϕ_{ce} is replaced with a clock signal, the circuit will not work unless each function block is redesigned to meet the timing requirement for synchronous circuits. *See id.* at ¶104. The signal ϕ_{ce} does not perform the same function as the claimed clock signal for at least these reasons.

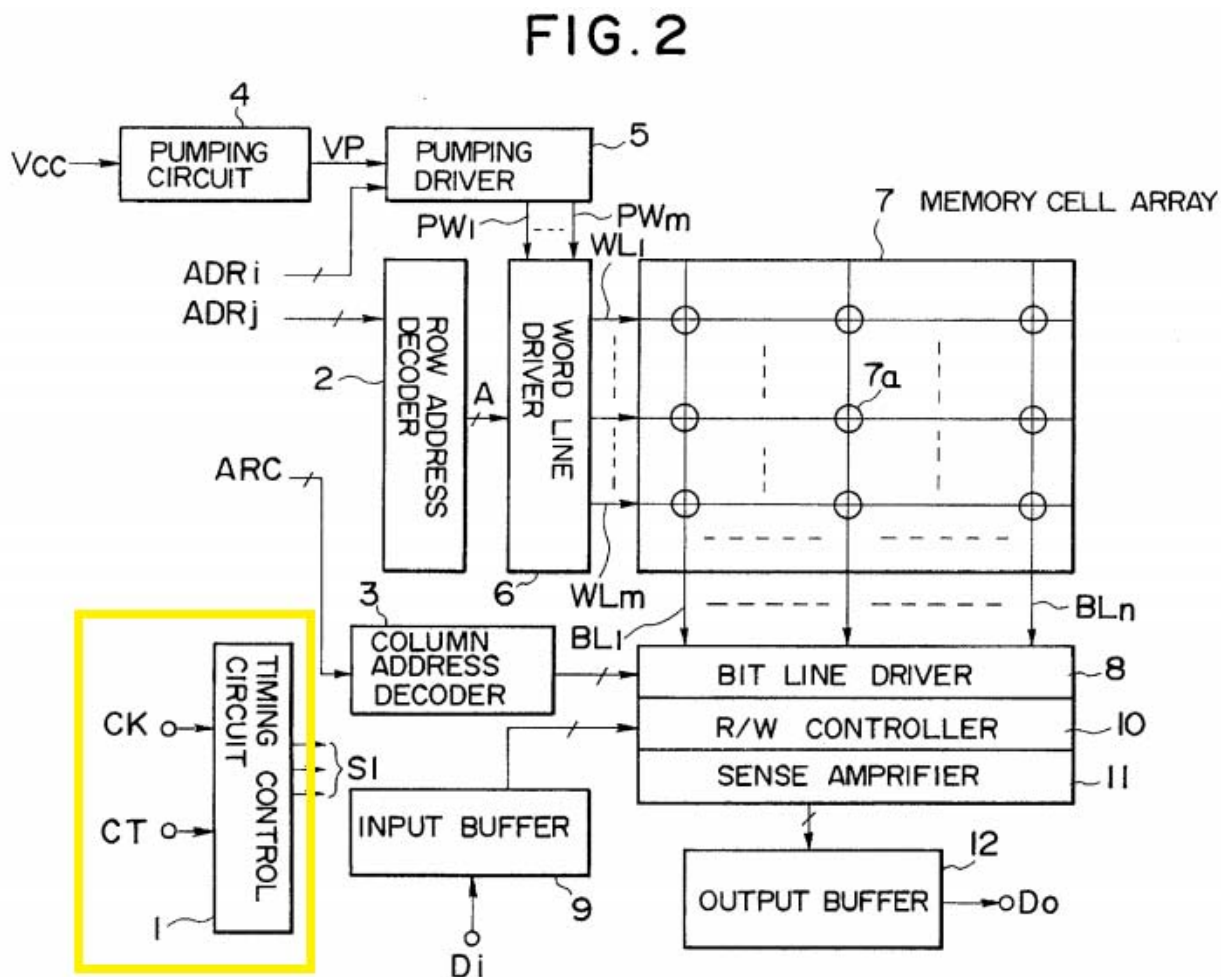
Additionally, as explained by Dr. Pedram, a race condition leading to a complete breakdown of circuit functionality can result if the NAND gate circuits NAG0-NAGk do not receive the selection control signal ϕ_{ce} . *Id.* at ¶¶110-13. This function performed by Sato's selection control signal ϕ_{ce} —ensuring that the memory system does not enter into an unstable race condition—is entirely different than any function performed by the clock signal of the '002 patent claims. *Id.* Petitioner's assertion that Sato's selection control signal ϕ_{ce} “performs the same function as the clock signal in the '002 patent” is wrong. *Id.*

Petitioner also asserts that Sato's selection signal ϕ_{ce} “performs the same function as the clock signal in a clocked decoder such as that described by Bridges.” Paper 2 at 15-16, citing Ex. 1003 at ¶¶67-68. Even if true, however, it does not follow that Sato discloses the “clock signal” claimed in the '002 patent. Ex. 2001

at ¶114. With this argument, Petitioner is *not* comparing the disclosure of Sato to the claims or description of the '002 patent. Rather, Petitioner is comparing Sato to an unrelated prior-art reference, Bridges, and this comparison is irrelevant to whether Sato discloses the clock signal claimed in the '002 patent. Unlike Bridges, Sato does not disclose a clocked decoder because none of its decoders operate based on a periodic, synchronizing clock signal. *Id.* at ¶114. And as explained in Sections VII.B.1-2 above, Sato's selection control signal ϕ_{ce} does not meet the "clock signal" limitation because it is not a periodic signal used for synchronization but rather one of multiple non-periodic timing signals (ϕ_{ce} , ϕ_{we} , ϕ_{sa} , ϕ_{oe}) used in an asynchronous system. *Id.* Any similarity between the uses of Sato's selection control signal ϕ_{ce} and the clock signal of Bridges cannot somehow transform the signal ϕ_{ce} into a periodic clock signal.

The petition also argues that "even the examiner and Patent Owner recognized a timing signal as being equivalent to a clock signal during prosecution of the '002 patent." Paper 2 at 15. The petition cites to the November 19, 2007 Office Action, where the Office rejected originally filed claims 17 and 18 as allegedly being anticipated by U.S. Patent No. 5,602,796 ("Sugio"). *Id.* Petitioner argues that the Office "equat[ed] the claimed clock outputs with timing control signal outputs of Sugio's timing control circuit 1." *Id.* But Petitioner's argument fails because Sugio is entirely different from Sato and expressly discloses a clock signal. Ex. 2001

at ¶¶115-16. As shown below, Sugio discloses a timing control circuit 1 that receives a clock signal CK:



Ex. 1012 at Fig. 2 (annotations added). “[T]he timing control circuit 1 outputs the control signals S_1 ... based on the control signal CT and the clock CK .” *Id.* at 3:58-61. The control signals S_1 are “for controlling timings provided for respective components.” *Id.* at 2:10-14.

Sugio does not disclose whether the control signals S_1 are periodic clock signals, but it is possible that they are periodic because they are generated based on

the clock signal CK. Ex. 2001 at ¶115. In Sato, by contrast, the selection control signal ϕ_{ce} is *not* generated based on a clock signal, but is instead generated based on the non-periodic chip enable signal $\overline{CE}$. *Id.* at ¶116. The disclosures of Sugio and Sato are not the same at all. Thus, to the extent that the Office previously found that Sugio’s control signals S_1 are clock signals, this is irrelevant to whether Sato’s selection control signal ϕ_{ce} is a clock signal because the disclosures of the two references are completely different.

The petition also highlights the statement in the Background section of Sato that “CMOS static RAMs including clocked static decoders are known in the art.” Paper 2 at 15 (citing Ex. 1005 at 1:10-11). This general statement is not related to the selection control signal ϕ_{ce} , and it thus provides no support for Petitioner’s position that the signal ϕ_{ce} is a clock signal. Ex. 2001 at ¶117. If anything, as explained by Dr. Pedram, this statement from Sato’s Background section tends to show that the selection control signal ϕ_{ce} is *not* a clock signal. *Id.* The statement shows that Sato was aware of the term “clock” and used it to describe the state of the art. *Id.* But when Sato described his own invention, he never referred to any clocks or clock signals. *Id.* This further evidences that no such clock signal is disclosed by Sato.

The petition further argues that “Sato states that his invention ‘can be applied widely to semiconductor memory devices having at least a clocked static type

address decoder[,]' ... which further corroborates Dr. Horst's opinion." Paper 2 at 15 (quoting Ex. 1005 at 12:4-6). As explained by Dr. Pedram, however, none of the X address decoders disclosed in Figs. 1-5 of Sato are clocked because they do not use a periodic, synchronizing clock signal, and Sato never equates any of its X address decoders with clocked decoders. Ex. 2001 at ¶118. The portion of Sato cited by Petitioner merely provides Sato's unexplained, unsupported opinion that his invention can be applied to devices having a clocked static type address decoder in the same way that Sato opines that his invention can also be applied to dynamic RAMs and other semiconductor memory devices. *Id.* at ¶118; *see, e.g.*, Ex. 1005 at 11:66-12:3.

Significantly, Sato provides no disclosure on *how* its invention could be applied to devices having a clocked static type address decoder, nor whether any modifications would be required to use the invention in this manner. Ex. 2001 at ¶119. Sato also does not suggest that the non-periodic selection control signal ϕ_{ce} would be replaced with a periodic clock signal when its invention is applied to a device having a clocked static type address decoder. *Id.* Petitioner likewise provides no explanation or evidence on how Sato's invention could be applied to such a device nor how Sato's statement, if true, is relevant to the question of whether Sato discloses a clock signal. *Id.* Sato's vague statement about potential uses for its

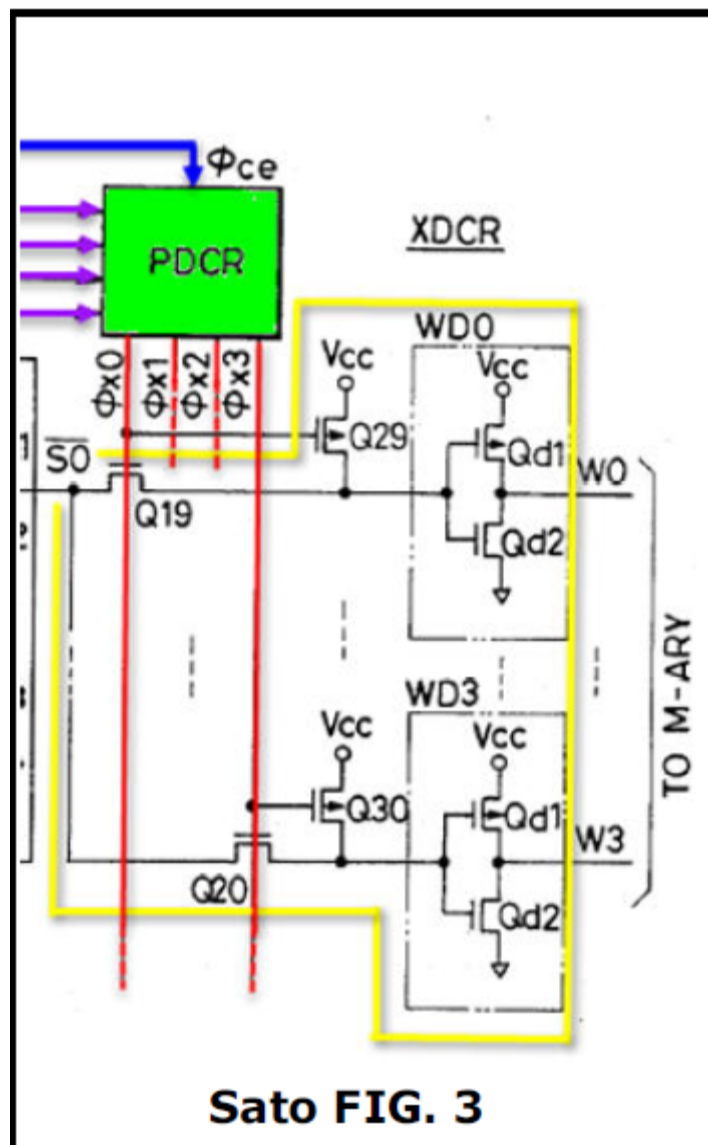
invention does not transform the reference's non-periodic timing signal ϕ_{ce} into a periodic clock signal.

The petition also argues that the “POSITA would have understood that the Sato system would perform poorly or malfunction if the timing signal in Sato were kept at a high level throughout operation.” Paper 2 at 16-17. In support of these assertions, Dr. Horst argues that Sato's address decoder would fail if it was supplied with two consecutive addresses 000000 and 111100 without the signal ϕ_{ce} changing from high to low to high. Ex. 1003 at ¶¶68-69. But even if true, this merely confirms that the signal ϕ_{ce} should not stay in a selected state while the row address is changing, and it provides *no indication* that the signal ϕ_{ce} is periodic. Ex. 2001 at ¶¶120-22. As described in Section VI.A above, Sato's signal ϕ_{ce} varies based on the highly irregular access patterns for reading and writing to the memory. *Id.* at ¶¶97-98. Thus, to the extent that the signal ϕ_{ce} must change from high to low to high, as Dr. Horst opines, it does so in an irregular, non-periodic manner and not at a fixed frequency, as would be found in a periodic signal. *Id.* at ¶122. Thus, Dr. Horst's argument does not show that the selection control signal ϕ_{ce} is a periodic clock signal.

Sato does not meet the “clock signal” limitation of the challenged claims for these additional reasons.

C. Sato Does Not Teach or Suggest the “Clock Output” Required by the Claims.

Independent claims 1, 17, 21, and 23-25 require the first logic to “apply the clock signal to a selected clock output” of a plurality of clock outputs associated with a selected group of wordline drivers. Independent claims 7, 11, 26, and 27 similarly require “providing a clock signal” to a selected group of wordline drivers. Petitioner argues that Sato’s “PDCR (green) applies the clock signal (blue) to one of four outputs (red)” (Paper 2 at 19):



Id. at 20. Petitioner thus argues that the signal ϕ_{ce} is a clock signal, and that the selection signals ϕ_{x0} , ϕ_{x1} , ϕ_{x2} , and ϕ_{x3} generated by the predecoder PDCR are clock outputs that apply the alleged clock signal to a group of wordline drivers. *Id.* at 18-23. But this is erroneous.

Even if Sato's signal ϕ_{ce} is considered to be a clock signal, Sato provides no indication that the selection signals ϕ_{x0} - ϕ_{x3} are also clock signals. Sato refers to

the signal ϕ_{ce} as a “timing signal” or a “selection control signal.” *See, e.g.*, Ex. 1005 at 3:59-61. By contrast, Sato refers exclusively to the signals ϕ_{x0} , ϕ_{x1} , ϕ_{x2} , and ϕ_{x3} as “selection signals.” *See, e.g., id.* at 1:23-54, 5:25-42, 7:31-48, 8:12-20, 8:55-68, 9:8-25, 9:54-10:39, 11:48-61. Petitioner’s declarant Dr. Horst confirmed this at deposition. Ex. 2005 at 30:18-32:12. Sato’s use of different terminology in referring to the input (“timing signal” or “selection control signal”) and outputs (“selection signals”) of the predecoder PDCR indicates that the outputs are not the same as the input, and thus that the outputs are not clock signals.

Further, the predecoder PDCR is a black box—Sato provides no disclosure on its internal circuitry. Ex. 2001 at ¶76; *see generally* Ex. 1005. For this additional reason, even if the input signal ϕ_{ce} to the predecoder PDCR is considered a clock signal, the outputs of the predecoder PDCR are not necessarily clock signals.

Sato thus fails to disclose the claimed “clock outputs” and “providing a clock signal” limitations of independent claims 1, 7, 11, 17, 21, and 23-27. For these additional reasons, claims 1-28 and 31-37 are not obvious over Sato.

VIII. ASANO AND ITOH DO NOT RENDER CLAIMS 1-17, 20-28, AND 31-36 OBVIOUS (GROUND 2)

The Board instituted trial on the ground that claims 1-17, 20-28, and 31-36 are obvious over Asano and Itoh. In this ground, Petitioner argues that Asano “represents the predecoder 202 simply using a block element in a block diagram,” and Itoh “illustrate[s] a possible implementation of the internal structure for the

predecoder 202.” Paper 2 at 35. But as explained below, Petitioner has not sufficiently articulated why the POSA allegedly would have been motivated to combine Asano and Itoh, and claims 1-17, 20-28, and 31-36 are therefore not obvious over these references.

A. Asano Does Not Disclose or Suggest a Circuit Device Including Distinct “First Logic” and “Second Logic.”

As explained above in Section III, the ’002 patent claims require distinct first and second logics that decode respective first and second portions of a memory address. The splitting of the memory address into multiple portions and the decoding of the two portions at separate first and second logics are fundamental features of the ’002 patent invention. *See, e.g.*, Ex. 1001 at 3:18-25; *see also* Ex. 2005 (Horst Depo. Transcript) at 16:10-14 (“[Figure 1 of the ’002 patent] shows separate decoders doing those decoding functions.”).

Petitioner states that “Asano forms ... the base reference of Ground-2 of [the] Petition,” but this reference does not disclose splitting a memory address into first and second portions, nor does it disclose decoding the first and second portions using distinct first and second logics, respectively. Ex. 2001 at ¶127. Rather, in Asano, the *entire memory address* is received and decoded by *a single predecoder 202 (id.)*:

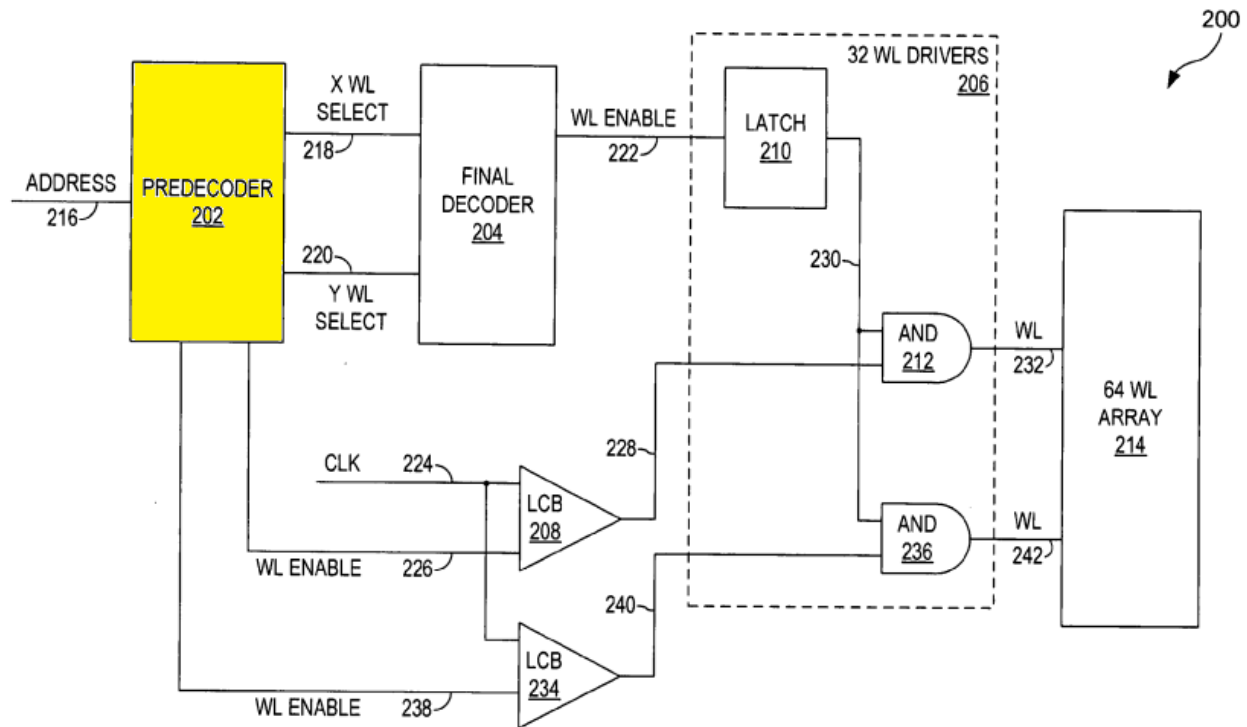
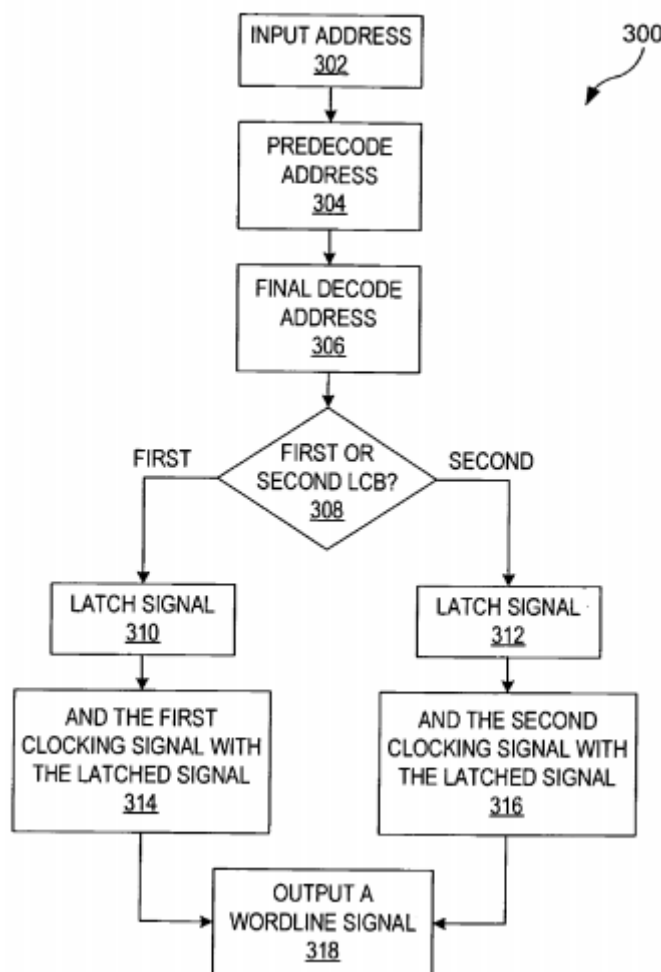


FIG. 2

Ex. 1006 at Fig. 2 (highlighting added).

The flowchart depicted in Fig. 3 of Asano likewise shows that the reference does not disclose splitting a memory address into two portions or decoding the two portions at respective first and second logics. As seen below, at step 302 of the flowchart, the entire memory address is “received ... at the predecoder 202 through a first communication channel 216,” and at step 304, the predecoder 202 predecodes the entire received memory address (*id.* at ¶[0016]):



Id. at Fig. 3. If portions the memory address were decoded in separate logics, Asano would include some description or illustration of this. It does not. All bits of the memory address are received and decoded by the single predecoder 202.

Petitioner cites to the predecoder 202 of Asano as allegedly meeting the “first logic” and “second logic” limitations of the claims (*see* Paper 2 at 36), but the predecoder 202 is a single predecoder, not separate first and second decoding logics. Petitioner’s attempt to read the single predecoder 202 on both the “first logic” and “second logic” limitations is improper. *See, e.g., Becton, Dickinson & Co. v. Tyco*

Healthcare Group, LP, 616 F.3d 1249, 1257 (Fed. Cir. 2010) (“Where a claim lists elements separately, the clear implication of the claim language is that those elements are distinct components of the patented invention.... There is nothing in the asserted claims to suggest that the hinged arm and the spring means can be the same structure.”) (internal quotations omitted); *Lantech Inc. v. Keip Machine Co.*, 32 F.3d 542, 547 (Fed. Cir. 1994) (“When a claim requires two separate elements, one element construed as having two separate functions will not suffice to meet the terms of the claim.”).

Moreover, Asano contains no teaching or suggestion that the predecoder can or should be split into multiple, different decoding logics. Ex. 2001 at ¶127. In fact, Asano contains no disclosure at all on the internal circuitry of the predecoder 202 (*id.*), and Petitioner concedes this, stating that “Asano represents the predecoder 202 simply using a block element in a block diagram.” Paper 2 at 35. Accordingly, Asano does not disclose or suggest the “first logic” and “second logic” required by the claims. *Id.* at ¶127.

Petitioner nevertheless argues that Asano’s predecoder 202 generates (i) an X wordline select signal that is 8 bits long, (ii) a Y wordline select signal that is 4 bits long, and (iii) two WL ENABLE signals. Paper 2 at 38-39. Petitioner further argues that “Asano’s predecoder uses three address bits to produce the X wordline select signal and two address bits to produce the Y,” and “[t]ogether, the three-bit

and two-bit predecoders represent the ‘second logic’ portion of the predecoder.” *Id.* at 39. Petitioner also argues that “a POSITA would have found it obvious to implement the ‘first logic’ portion of Asano’s predecoder ... using a 1 to 2 decoder.” *Id.*

But there Asano does not disclose the existence of any “‘first logic’ portion” or “‘second logic’ portion” of its predecoder—that is a construction of Petitioner. That is, as explained by Dr. Pedram, Petitioner is attempting to read disclosure into Asano that does not exist and would not have been obvious to the POSA. Ex. 2001 at ¶¶128-30. Specifically, Petitioner is relying on predecoder 202 of Asano as allegedly performing both the first logic decoding and the second logic decoding, but there is nothing in Asano to suggest that predecoder 202 can or should be implemented using multiple predecoders or multiple decoding logics, as opposed to a single predecoder, as the reference expressly teaches. *Id.* at ¶129. If Asano intended its predecoder 202 to include multiple predecoders or multiple logic circuits, it would have specified this, just as the reference specifies the use of two separate LCBs (208 and 234) and two separate AND gates (212 and 236). *Id.*; Ex. 1006 at Fig. 2, ¶¶[0018]-[0019].

For at least these reasons, Asano does not disclose or suggest the claimed “first logic” and “second logic.”

B. The Petition Does Not Sufficiently Articulate Why a POSA Would Allegedly Have Been Motivated to Combine Asano and Itoh.

Recognizing that Asano includes no teaching or suggestion of separate and distinct “first logic” and “second logic,” Petitioner argues

[b]ecause Asano represents the predecoder 202 simply using a block element in a block diagram, a POSITA would have looked to Itoh’s textbook circuits in determining how the internal structure of the predecoder 202 would be built as separate logic sections for decoding different portions of the 6-bit memory address.

Paper 2 at 35. Petitioner specifically argues that the POSA would be motivated to implement (i) a “first logic” in Asano’s predecoder 202 using a 1-to-2 decoder disclosed by Itoh, and (ii) a “second logic” in the predecoder 202 using 2-to-4 and 3-to-8 decoders disclosed by Itoh. *Id.* at 36-41. Petitioner also argues that Asano and Itoh can be combined in other ways, such as that illustrated at pages 40 and 44 of the petition.¹

But Petitioner has not adequately explained why the POSA would allegedly be motivated to combine Asano and Itoh. Ex. 2001 at ¶¶131-38. As seen above, Petitioner argues that “[b]ecause Asano represents the predecoder 202 simply using a block element in a block diagram, a POSITA would have looked to Itoh’s textbook

¹ In some places in the petition, it is not clear which combination of Asano and Itoh is being discussed. For instance, the combination described in page 39 of the petition does not match the “redrawn figure” shown at page 40.

circuits” in determining how to implement the predecoder 202. Paper 2 at 35. This argument is conclusory, and Petitioner has provided no reasons *why* the POSA allegedly would have looked specifically to Itoh. Ex. 2001 at ¶133. This is especially problematic because Petitioner admits that Itoh discusses just one of multiple different ways that Asano’s predecoder 202 could possibly be implemented:

Itoh discloses well-known circuits that illustrate *a possible implementation of the internal structure for the predecoder 202.*

Id. (emphasis added).

This statement and others from Petitioner (*see id.* at 37 (“POSITA *could have* implemented Asano’s predecoder using ... circuits disclosed by Itoh”)) acknowledge that Asano’s predecoder 202 can be implemented in multiple different ways, and that the specific combination of three of Itoh’s circuits arranged as proposed by Petitioner are just one “possible implementation of the [predecoder’s] internal structure.” Ex. 2001 at ¶133; *see also* Ex. 1003 (Horst Decl.) at ¶118, Ex. 2005 (Horst Depo. Transcript) at 47:3-49:7. Given this, Petitioner must provide reasons *why* the POSA allegedly would have selected the specific arrangement of three circuits from Itoh instead of the other possible implementations. Petitioner has not done so, and its obviousness ground is therefore deficient. In fact, the Board routinely rejects obviousness arguments where, as here, a petitioner fails to provide a sufficient factual basis for its assertions. *See, e.g., Heart Failure Techs., LLC v.*

Cardiokinetix, Inc., IPR2013-00183, Paper 12 at 9 (PTAB July 31, 2013) (“Petitioner must show some *reason* why a person of ordinary skill in the art would have thought to combine *particular* available elements of knowledge, as evidenced by the prior art, to reason the claimed invention.”) (emphasis in original).

Further, the Board has recognized that the legal test for obviousness considers whether the POSITA “would have” combined the prior art, not whether the art “could have” been combined. *See, e.g., TRW Automotive US LLC v. Magna Elecs., Inc.*, IPR2014-01355, Paper 21 at 15 (PTAB Nov. 19, 2015) (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)). Petitioner repeatedly argues that “[a] POSITA *could have* implemented Asano’s predecoder using a combination of the predecoder circuits disclosed by Itoh” (Paper 2 at 37 (emphasis added)) but such assertions, even if true, are insufficient for a proper obviousness analysis. *See also id.* at 42 (“‘first logic’ portion of Asano’s predecoder *could be* implemented using ... [circuitry] disclosed by Itoh”). Petitioner has provided no reasoning why the POSA *would have* been motivated to implement Asano’s predecoder using the circuits disclosed by Itoh.

Petitioner also argues that “[a] POSITA designing Asano’s memory circuit would have naturally turned to a textbook such as Itoh’s for details on memory design techniques for a predecoder.” Paper 2 at 35. Similarly, Petitioner asserts that “[a]n artisan endeavoring to practice Asano’s invention would have looked to known

circuit designs.” *Id.* at 41. But the petition provides no reasoning or explanation for these conclusory assertions—*why* would the POSITA have turned to “textbook[s]” and “known circuit designs” to implement the predecoder 202? Petitioner does not say. *See id.* But even assuming these assertions to be true, Petitioner has provided no explanation or evidence as to why the POSA would have looked to *Itoh’s decoding circuits*, specifically, instead of other circuits described in various other textbooks and sources. Petitioner’s obviousness ground is deficient for this additional reason.

The thrust of Petitioner’s argument appears to be that Asano’s predecoder 202 outputs an 8-bit X wordline select signal and a 4-bit Y wordline select signal, and “[a]s such, it would have been obvious for a POSITA to implement Asano’s predecoder using Itoh’s three-bit predecoder to generate the 8 bits of the X wordline select signal and Itoh’s two-bit predecoder to generate the 4 bits of the Y wordline select signal.” Paper 2 at 39. Likewise, Petitioner argues, because Asano’s predecoder 202 outputs two WL enable signals, it would have been obvious for the POSA to implement Asano’s predecoder using Itoh’s 1-to-2 decoder to generate the two WL enable signals. *Id.*

But here again, Petitioner provides no reasons why the POSA would be motivated to use the particular one-, two-, and three-bit decoders disclosed in Itoh. Ex. 2001 at ¶¶135-36. As explained by Dr. Pedram, Itoh discloses a specific type of

decoder—known as a “one-hot decoder”—but there are many other ways to implement the decoding functions of Asano’s predecoder 202. *Id.* at ¶136. For example, zero-hot decoders, balanced decoders, and constant-weight decoders are alternative ways of implementing Asano’s predecoder 202. *Id.* Because there are multiple different ways to perform the decoding of Asano’s predecoder 202, Petitioner must provide reasons *why* the POSA allegedly would have selected Itoh’s one-hot decoder implementation instead of another possible implementation. Petitioner has not done so, and its obviousness ground is therefore deficient.

In the end, Petitioner’s argument appears to be based on nothing more than impermissible hindsight reconstruction. Petitioner recognizes that Asano does not disclose the separate first and second decoding logics required by the claims, and Petitioner seeks to remedy this deficiency using different decoders disclosed in Itoh. But Petitioner has presented no legitimate reasons why the POSA allegedly would have been motivated to combine Asano with Itoh, and this evidences the hindsight reconstruction employed by Petitioner.

For at least these reasons, Petitioner has not sufficiently articulated why the POSA would allegedly be motivated to combine Asano and Itoh. Petitioner has not shown that claims 1-17, 20-28, and 31-36 are obvious over these references.

IX. CONCLUSION

The Board should hold that claims 1-28 and 31-37 are not unpatentable in the Final Written Decision.

Respectfully submitted,

Date:

By: /David B. Cochran/

Joseph M. Sauer, Reg. No. 47,919
David B. Cochran, Reg. No. 39,142
David M. Maiorana, Reg. No. 41,449
JONES DAY
North Point, 901 Lakeside Avenue
Cleveland, OH 44114
(216) 586-3939

Matthew W. Johnson, Reg. No. 59,108
Joshua R. Nightingale, Reg. No. 67,865
JONES DAY
500 Grant Street, Suite 4500
Pittsburgh, PA 15219

CERTIFICATE OF COMPLIANCE

I, the undersigned, certify that the above Patent Owner Response complies with the applicable type-volume limitations of 37 C.F.R. § 42.24 (b)(1). This Patent Owner Response contains 11,194 words, as counted by the word count function of Microsoft Word. This is less than the limit of 14,000 words as specified by 37 C.F.R. § 42.24(b)(2).

Date: April 15, 2019

/ Joshua R. Nightingale /
Joshua R. Nightingale, Reg. No. 67,865
JONES DAY
500 Grant Street, Suite 4500
Pittsburgh, PA 15219

Counsel for Patent Owner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing Patent Owner Response was served on April 15, 2019 by email, as follows:

W. Karl Renner
IPR39521-0054IP1@fr.com
axf-ptab@fr.com

Thomas A. Rozylowicz
PTABInbound@fr.com
rozylowicz@fr.com
tar@fr.com

Timothy W. Riffe
PTABInbound@fr.com
riffe@fr.com

Kenneth J. Hoover
hoover@fr.com

Whitney A. Reichel
wreichel@fr.com

Date: April 15, 2019

/ Joshua R. Nightingale /
Joshua R. Nightingale, Reg. No. 67,865
JONES DAY
500 Grant Street, Suite 4500
Pittsburgh, PA 15219

Counsel for Patent Owner

Exhibit List

EX	Description
2001	Declaration of Massoud Pedram, Ph.D.
2002	IEEE Dictionary
2003	Itoh (additional portions)
2004	IPR2015-00148, Declaration of Don Alpert
2005	Horst Deposition Transcript