

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE, INC.,
Petitioner

v.

QUALCOMM INCORPORATED.,
Patent Owner

Case IPR2018-01249
Patent 7,693,002

**PETITIONER APPLE, INC.'S
REPLY TO PATENT OWNER'S RESPONSE**

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APPLE-1001	U.S. Patent No. 7,693,002 to Jentsung Lin (“the ’002 patent”)
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APPLE-1003	Declaration of Dr. Robert Horst, Ph.D
APPLE-1004	Curriculum Vitae of Dr. Horst
APPLE-1005	U.S. Patent No. 4,951,259 to Yoichi Sato (“Sato”)
APPLE-1006	U.S. Patent Pub. No. 2006/0098520 to Toru Asano et al. (“Asano”)
APPLE-1007	Kiyoo Itoh, <i>VLSI Memory Chip Design</i> , (Springer 2001) (“Itoh”)
APPLE-1008	U.S. Patent No. 5,291,076 to Jeffrey T. Bridges (“Bridges”)
APPLE-1009	Stephen Brown et al., <i>Fundamentals of Digital Logic with Verilog Design</i> , (McGraw Hill 2003) (“Brown”)
APPLE-1010	Declaration of Edward G. Faeth (Authentication of APPLE-1007 and APPLE-1009)
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APPLE-1013	Second Declaration of Dr. Robert Horst, Ph.D
APPLE-1014	IEEE Dictionary (with additional page)
APPLE-1015	Modern Dictionary of Electronics
APPLE-1016	U.S. Patent No. 4,922,461 (“Hayakawa”)

- APPLE-1017 M. Pedram. "Design technologies for Low Power VLSI," in *Encyclopedia of Computer Science and Technology*, Marcel Dekker, Editors: A Kent, J. G. Williams, and C. M. Hall, vol. 36, 1997, pages 73-95
- APPLE-1018 N. Mohyuddin, K. Patel, and M. Pedram. "Deterministic clock gating to eliminate wasteful activity in out-of-order superscalar processors due to wrong-path instructions," *Proc. of Int'l Conf. on Computer Design*, Oct. 2009, pages 166-172
- APPLE-1019 Pedram Deposition Transcript

I. INTRODUCTION

Pursuant to 37 C.F.R. § 42.107(a), Petitioner Apple, Inc. (“Petitioner”) submits this Reply to Patent Owner’s Response (“Response”) to the Petition for Inter Partes Review (“IPR”) of U.S. Patent No. 7,693,002 (“the ’002 Patent”) filed by Patent Owner Qualcomm Inc. (“PO”).

II. CLAIM CONSTRUCTION

In accordance with 37 C.F.R. § 42.100(b), claims in this proceeding shall be given their broadest reasonable interpretation (“BRI”) as understood by a POSITA in view of the specification. In its Response, PO proposes that under a BRI construction the term “clock signal” should be interpreted as “a **periodic** signal used for synchronization.” Response, 11-15.¹ Petitioner submits this proposed construction is excessively narrow in view of the ’002 patent claims, specification, and objective extrinsic evidence. Petitioner proposes “clock signal” be given its plain meaning, or, if the Board views it necessary to construe the term, “clock signal” should be interpreted as “a signal used for synchronization.”

¹ All emphases added unless otherwise noted.

**A. Dr. Pedram failed to consider the full scope of the claims
when opining on the term “clock signal”**

PO’s reliance on Dr. Pedram’s expert opinion is misplaced given Dr. Pedram admitted he failed to consider the full scope of the claims.

The ’002 patent states its “**disclosure** is not intended to be limited to the embodiments shown herein but **is to be accorded the widest scope consistent with the principles and novel features as defined by the following claims.**” APPLE-1001, 10:59-63. Yet, Dr. Pedram considered only the disclosed embodiments, and testified the scope of the claims is “**a different inquiry that [he] really [hasn’t] considered.**” APPLE-1019, 53:6-7.

Q: Dr. Pedram, it’s your opinion that the ’002 patent is limited to applications you would characterize as synchronous memory systems; correct?

A: So again, **I’m not here to opine on the scope of the claims.** This is a different inquiry... So, **the embodiments** are definitely that. And—**but what the scope of the claim is, I mean, it’s a different inquiry that I really haven’t considered.**

Q: You’re saying you haven’t considered whether the claims of the ’002 patent are limited to synchronous memory systems, but only whether the embodiments of the ’002 patent depict synchronous memory systems?

MR. SAUER: Objection; form.

WITNESS: Again, **this is really not a question I have considered**, to define the exact scope of any of the claims with respect to the systems that it covers or does not cover. And I—**I have construed, in my view, and describe my understanding of what the clock signal is in this context.**

APPLE-1019, 52:15-53:23. Accordingly, Dr. Pedram’s opinion on the BRI of the term “clock signal,” and PO’s reliance on Dr. Pedram’s opinion, should be accorded little weight.

B. PO’s proposed construction of “clock signal” is narrower than the ’002 patent claims themselves

PO’s proposed construction is unduly narrow because it is inconsistent with claims of the ’002 patent. The claims repeatedly refer to the outputs of the first logic and conditional clock generator as “clock outputs.” See APPLE-1001, claims 1-3, 5, 8, 9, 13, 17, 21-25, 27-34, and 38. Claims 7, 11, 26, and 27 also state the “clock signal” is provided to “a selected group of wordline drivers” (e.g., output lines 124-130 of FIG. 1). Thus, a POSITA would understand the claimed “clock outputs” carry the claimed “clock signal” to the selected group of wordline drivers. APPLE-1013, ¶¶12-13. Yet, as Dr. Pedram confirms, the signals carried by these “clock outputs” are not periodic and would therefore not meet PO’s proposed construction of “clock signal”:

Q: In Figure 1 of the '002 patent, there are four signals labeled 124, 126, 128 and 130. These are outputs of the conditional clock generator 110; correct?

A: Yes.

...

Q: In your opinion, are signals 124, 126, 128 and 130 clock signals as you have defined that term?

A: In general, no, because a clock signal, in my definition, would have fixed periodicity. You see a fixed stream, constant stream of zero and ones coming in with fixed interval in between, always running, continuously running, and used for synchronization purposes. I don't believe, in general, any of these signals which are called conditional clock signals, I guess. We could call them that way because they are the outputs of the conditional clock generator. None of these signals, 124, 126, 128, 130 meet that definition.

APPLE-1019, 83:9-13, 83:19-84:6-7. Consequently, the PO's BRI interpretation of the term "clock signal" is too narrow to even encompass the clock signals carried by "clock outputs" of the '002 patent claims.

**C. PO's proposed construction of "clock signal" is
unsupported by the specification of the '002 patent**

Although PO argues the "intrinsic evidence ... supports the interpretation of the claim term 'clock signal' as 'a periodic signal used for synchronization,'" PO provides no credible evidence of this alleged fact. Response, 14. The '002 patent provides no definition for either "clock" or "clock signal." APPLE-1019, 79:8-9 (Dr. Pedram testifying "I have not seen in the '002 patent a precise definition of the clock.>"). And, neither PO nor Dr. Pedram provide a single citation to the '002 patent referring to the "clock signal" as periodic. See Response, 11-15; Ex. 2001, ¶¶52-70.

Instead, PO's "intrinsic evidence" is limited to a lengthy explanation by Dr. Pedram of how embodiments of the '002 patent only describe synchronous memory systems. Response, 11-15 (citing Ex. 2001, ¶¶52-70). Yet, Dr. Pedram does not cite to a single instance in the '002 patent referring to a synchronous memory system. Ex. 2001, ¶¶52-70. He instead argues from an absence of evidence. APPLE-1013, ¶5. Dr. Pedram reasons "a POSA would understand that the '002 patent discloses a synchronous memory system that uses a periodic clock signal" because "the patent does not describe a timing generator circuit to generate various internal timing signals [related to asynchronous systems]." Ex. 2001, ¶65. Yet, during deposition Dr. Pedram acknowledged the '002 patent is silent in regard to many aspects of

computer memory systems such as clock drivers (40:10-20), column address decoders (44:17-48:1), synchronous memory control logic (54:80-60:7), and operating voltages (64:7-67:4). Furthermore, the '002 patent explicitly states its memory address decoder “**generally relates to memory arrays.**” '002 patent, 1:7. In view of this statement and the complete lack of any reference to a synchronous system, a POSITA would not have concluded that the '002 patent's wordline driver system was limited to synchronous memory. APPLE-1013, ¶¶5-6. Consequently, even if all synchronous systems used periodic clocks to drive memory address row decoders (which Petitioner contests below), the claims of the '002 patent are not so limited.

D. PO's proposed construction of “clock signal” as necessarily being periodic is contradicted by objective evidence

The extrinsic evidence confirms a POSITA would not consider “clock signal” as limited to periodic signals. The IEEE Dictionary submitted by PO provides additional definitions for a clock signal that do not require periodicity. Response, 12. Specifically, consistent with Apple's expert Dr. Horst's opinion that “‘clock’ is another name for a timing signal” (which Dr. Pedram characterized as “a false statement”), the IEEE Dictionary states “clock signal,” “clock pulse,” and “timing pulse” are synonyms of each other. Pet., 15; Ex. 2001, ¶108.

clock signal A periodic signal used for synchronizing events.
Synonyms: clock pulse; timing pulse. (C) 610.10-1994

Ex. 2002, 9. In further support of Dr. Horst's opinion, a previously uncited page of the IEEE dictionary defines "clock" as "[a] signal, the transitions of which (between the low and high logic level [or vice versa]) are used to indicate when a stored-state device, such as a flip-flop or latch, may perform an operation."

APPLE-1014, 4. The Modern Dictionary of Electronics provides additional definitions indicating that a POSITA would understand that a "clock" or "clock signal" is not necessarily periodic. APPLE-1013, ¶¶3-4, 7-10. A "clock" is defined as "1. A pulse generator or signal waveform used to achieve synchronization of the timing of switching circuits and the memory in a digital computer system" and "4. A strobe signal that activates a certain sequence of operations." APPLE-1015, 3-4. "Clock pulse," a synonym of clock signal, is defined as "The synchronization signal produced by a clock." *Id.*, 4.

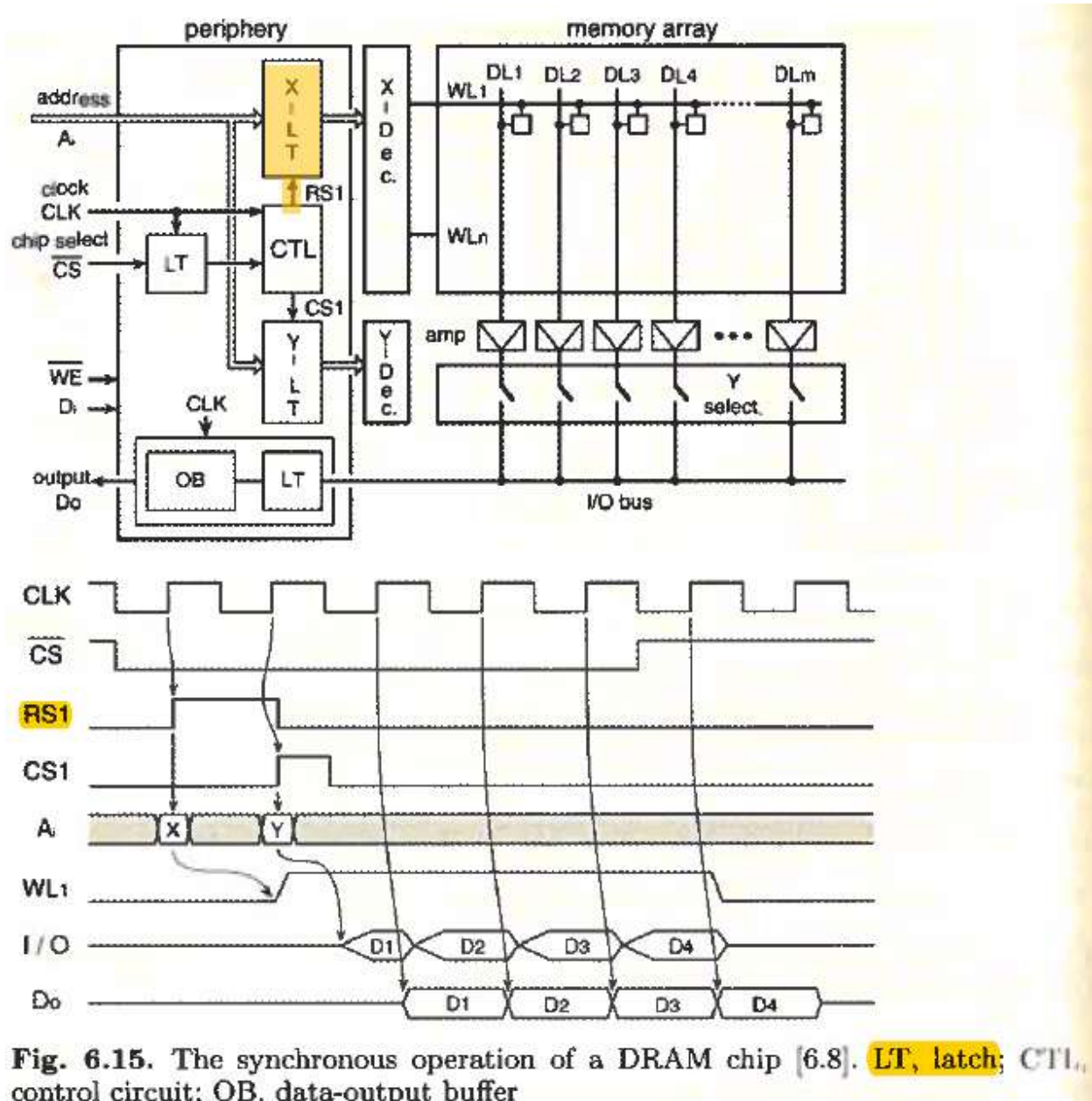
Synchronization and timing of operations is a clear commonality among these definitions, whereas periodicity is not. APPLE-1013, ¶11.

Second, PO's construction relies on the faulty assumption that a POSITA would not have viewed timing signals in asynchronous systems as clock signals. Response, 12-13 (citing Ex. 2001, ¶¶55-64). In particular, PO and Dr. Pedram refer to the row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$) described in Itoh as examples of such asynchronous memory timing signals. Response, 35-37;

Ex. 2001, ¶¶59-60. PO even asserts that “Itoh does not refer to the signals $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ —or any other signals of the asynchronous memory system—as being ‘clock signals.’” Response, 37 (citing Ex. 2001, ¶¶59-60, 108). “If anything, the non-periodic $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals may be understood by the POSA as being ‘timing signals.’” *Id.* However, Itoh uses the term “clock” in reference to this “non-periodic” $\overline{\text{RAS}}$ signal at least three times; twice on page 142 when describing a $\overline{\text{RAS}}$ buffer circuit as a “ $\overline{\text{RAS}}$ clock buffer” and once on page 149 stating “a clock Φ_B generated by the $\overline{\text{RAS}}$ buffer” being applied to a row select line RX. APPLE-1007. PO’s assumption is demonstrably false.

Third, Itoh’s synchronous memory system does not support PO’s assertion that in synchronous systems “a single, periodic, synchronizing clock is used to time all memory operations.” Response, 13 (citing Ex. 2001, ¶¶55-60). Dr. Pedram relies on FIG. 6.15 as an exemplary synchronous memory system similar to that allegedly disclosed by FIG. 1 of the ’002 patent. Ex. 2001, ¶¶55-60. However, Itoh illustrates and explains that in “synchronous operation, a row address strobe signal RS1,” not the periodic system clock CLK, is supplied to an X-LT (X address latch) “so that the row addresses are strobed and the corresponding wordline ... is activated.” Ex. 2003, 18-19, FIG. 6.15 (reproduced and highlighted below). Dr. Pedram agrees with Itoh that the RS1 signal carries out the “same function” as the non-periodic $\overline{\text{RAS}}$ signal. *Compare* Ex. 2003, 19

with Ex. 2001, ¶62 (“Itoh also points out, synchronous operation can even eliminate the roles of RAS# and CAS# which are used in asynchronous operation, since the same



functions are carried out by the internally generated clock-synchronous signals RS1 and CS1”). Yet, RS1 is not periodic because “[w]hen CS bar signal is high in

the drawing of Figure 6.15, both RS1 and CS1 are low.” APPLE-1019, 62:11-12; APPLE-1013, ¶35 (Dr. Horst agreeing). Thus, even in synchronous memory systems, the periodic system clock is not necessarily passed to an address decoder—the focus of the claims of the ’002 patent. PO’s narrow interpretation would thus exclude Dr. Pedram’s own example of a typical synchronous memory system.

Fourth, other prior art references, including some of Dr. Pedram’s own papers, likewise refer to non-periodic signals as clock signals. APPLE-1013, ¶¶15-21. As noted above, Itoh refers to a signal Φ_B generated from a non-periodic $\overline{RAS}$ signal as a clock. U.S. Patent No. 4,922,461 (“Hayakawa”) refers to a signal (ϕS) generated from an address transition detector as a clock signal. APPLE-1016, 3:50-57. Yet, this ϕS signal is only “effective in level for a fixed period of time.” *Id.* And, at least two of Dr. Pedram’s own papers refer to non-periodic signals (e.g., gated clocks) as clock signals. APPLE-1017; APPLE-1018; Ex. 2001, CV citations [BC18], [C217]; APPLE-1013, ¶¶18-21.

Consequently, the weight of the objective evidence shows a POSITA would not have considered the ’002 patent’s “clock signal” as necessarily periodic.

E. PO’s reliance on the Alpert Declaration is misplaced

PO’s reliance on the Alpert Declaration (Ex. 2004) in support of its claim construction is misplaced. First, Ex. 2004 is a declaration by Dr. Alpert submitted

on behalf of a different party (not Apple), in a different IPR, and in reference to a different patent. The opinion expressed by Dr. Alpert in Ex. 2004 is specific to U.S. Patent 6,356,122 at issue in IPR2015-00148 (where periodicity was uncontested), hence, Dr. Alpert does not therein offer any expert opinion relevant to the meaning of a term in the '002 patent. Third, U.S. Patent 6,356,122 has at least ten references to periodic characteristics of a clock (e.g., frequency) whereas the '002 patent has no such references.

F. If the Board considers it necessary to construe the term “clock signal,” Petitioner proposes “a signal used for synchronization”

For the reasons discussed above, a POSITA would not have limited the term “clock signal” to only periodic signals. APPLE-1013, ¶¶3-21. If the Board considers it necessary to construe the term “clock signal” an interpretation as “a signal used for synchronization” is sufficiently broad to give meaning to all the uses of the term “clock signal” and “clock outputs” recited in the claims. APPLE-1013, ¶22. Petitioner’s proposed interpretation, additionally, captures the fundamental commonality expressed by both the '002 patent and the industry definitions discussed above; namely, providing proper synchronization or timing for memory operations.

III. SATO RENDERS CLAIMS 1-28 AND 31-37 OBVIOUS (GROUND 1)

The petition set forth a complete and proper *prima facie* analysis showing that Sato renders claims 1-28 and 31-37 obvious.² Pet. 9-32, 51-81. Moreover, Sato would render claims 1-28 and 31-37 obvious even under the PO's restrictively narrow interpretation of the term "clock signal." PO's primary counter-argument to Petitioner's Sato Ground challenges only whether the electrical input signal to the address decoder meets the "periodic" requirement found only in PO's proposed construction. PO does not challenge the similarities in the overall function or structure of Sato's address decoder with that recited in the claims. Further, the '002 patent itself provides no indication to a POSITA that the claimed address decoder would function any differently whether the clock signal was periodic or not. APPLE-1013, ¶¶5-6.

A. The petition addresses all the *Graham* factors

PO argues the petition fails to address the second *Graham* factor to identify a difference between the claimed subject matter of the '002 patent and Sato. Response, 28-29. PO is incorrect. Specifically, in arguing Sato's "timing signal ϕ ce represents or renders obvious a clock signal," the petition acknowledges that

² Petitioner's application of Sato to the dependent claims remains uncontested. See Response; APPLE-1019, 37:11-14.

Sato does not use the words “clock signal,” and explains a POSITA would immediately appreciate the timing signal as a type of clock signal, or, under a narrower definition of “clock signal,” that it would have been obvious to use a clock signal as the ϕ ce signal based on Sato’s explicit teaching that his invention “can be applied widely to semiconductor memory devices having at least a clocked static type address decoder.” Pet. 14-15 (citing APPLE-1005, 12:4-6).

B. Sato does render the “clock signal” recited in the claims as obvious

The petition sets forth several reasons supported by evidence to explain why a POSITA would have understood Sato’s timing signal to represent or render obvious the clock signal recited in the ’002 patent claims. Pet., 14-17 (citing APPLE-1003, ¶¶64-69; APPLE-1005, 1:10-11, 12:4-6; APPLE-1001, 3:28-62; APPLE-1008, 3:1-4:24, Figure 1; APPLE-1011, 1:23-42). PO contests these rationales. Response, 35-39.

First, PO asserts that the “words ‘clock signal’ and ‘timing signal’ are not interchangeable, nor would the POSA have understood them as such.” *Id.*, 35-36. Yet, PO’s own dictionary definition of “clock signal” states “timing pulse” is its **synonym**. Ex. 2002, 9. The same dictionary’s indication that “clock pulse” is also synonymous would suggest to a POSITA that any quibbles over the use of “timing pulse” rather than “timing signal” are irrelevant.

Next, PO asserts that according to Dr. Pedram “the POSA would understand that the symbol ϕ is used in the art to denote a phase signal, not a clock signal.” Response, 38 (citing Ex. 2001, ¶109). However, Dr. Pedram did not review the Shin patent (APPLE-1011) which the petition and Dr. Horst cited to as evidence to the contrary. Ex. 2001, ¶3; APPLE-1019, 13:8-20; Pet., 15; APPLE-1003, ¶64. Shin refers to “**clock signals ϕ_1 and ϕ_2** ” using the symbol ϕ ; as do Itoh and Hayakawa. APPLE-1011, 1:23-42; APPLE-1007, 149 (“a clock Φ_B ”); APPLE-1016, 3:50-57.

PO argues Sato’s timing signal does not perform the same function as the ’002 patent’s clock signal because in addition to being provided to the PDCR (“first logic”) it also prevents Sato’s NAND gate circuits (“second logic”) from causing an “unstable race condition.” Response, 39. Dr. Horst explains that this is a “strawman argument” because PO must first deconstruct Sato by removing the timing signal from Sato’s NAND decoders. APPLE-1013, ¶23.

PO also argues Sato’s timing signal is not a “periodic” clock signal because “Sato states that the signal ϕ_{ce} is ‘kept at a high level.’” Response, 30-32. However, Petitioner and Dr. Horst explained that a “POSA would have understood that the Sato system would perform poorly or malfunction if the timing signal in Sato were kept at a high level throughout operation” as this statement suggests. Pet, 16-17 (citing APPLE-1003, ¶¶68-69). In fact, both experts agree

that Sato's timing signal "must be an oscillatory signal for Sato's row address decoder to function properly." APPLE-1013, ¶¶32-34; Ex. 2001, ¶¶120-122. Any disagreement is merely over the timing of pulses in Sato's timing signal. *Id.*

Tellingly, PO does not contest the similarity between the function performed by Sato's timing signal to synchronize the operation of Sato's wordline drivers in a manner similar to that of the '002 patent's clock signal. Pet., 14-22, 31-32 (citing APPLE-1003, ¶¶60-63, 65-66, 70-71); APPLE-1013, ¶¶14, 24-29. It is undisputed that Sato's timing signal is an input to the PDCR in a similar manner in which the clock in the '002 patent is an input to the conditional clock generator. Pet., 14-17. It is also undisputed that Sato's PDCR functions similar to the '002 patent's conditional clock generator to apply the timing signal to the outputs of the PDCR.³ *Id.*, 18-23. Likewise, it also remains undisputed that the outputs of Sato's PDCR are used to synchronize operations of transistors that control Sato's wordline drivers in a nearly identical manner to how the '002 patent's conditional clock generator outputs control its wordline drivers. Pet., 31-32; APPLE-1013, ¶¶14, 27-29; *see also* APPLE-1005, 5:66-6:2, 10:36-48, 11:48-56 (explaining how the

³ PO argues Sato does not teach a "clock output," however, as discussed in §III.D below this is a pure semantic argument and Dr. Horst's explanation of how Sato applies the timing signal to the PDCR outputs is undisputed.

timing signal sets logic levels of the NAND gates, capacitance cut MOSFETs and reset MOSFETs “in synchronism with the timing signal ϕ_{ce} ”). Dr. Horst provides a table illustrating the similarity between how Sato and the ’002 patent use their respective timing/clock signals to synchronize the operations of their wordline drivers in four possible operational states. APPLE-1013, ¶¶27-29. Dr. Horst’s table is presented to summarize the arguments made in the petition at 18-22, 31-32. Hence, both Sato’s timing signal and the ’002 patent’s clock signal are applied in a similar fashion to synchronize the operations of wordline drivers. APPLE-1013, ¶¶14, 29.

**C. Even under PO’s narrow construction, Sato renders the
“clock signal” obvious**

PO characterizes synchronous memory as “fundamentally” different from asynchronous memory in an attempt to over-complicate the fact that the primary point of dispute is over unclaimed characteristics of an input signal to an address decoder; not the substantive operational and structural similarity between Sato’s address decoder and that claimed by the ’002 patent. In fact, a POSITA would have understood that Sato’s address decoder would function fundamentally the same regardless of whether the timing signal was periodic or not. APPLE-1013, ¶¶30-35. The only difference would be the regularity at which Sato’s address decoder performed its operations. *Id.*, ¶¶34-35. Indeed, in Dr. Horst’s experience “it is common to use asynchronous memories in systems that have a synchronous

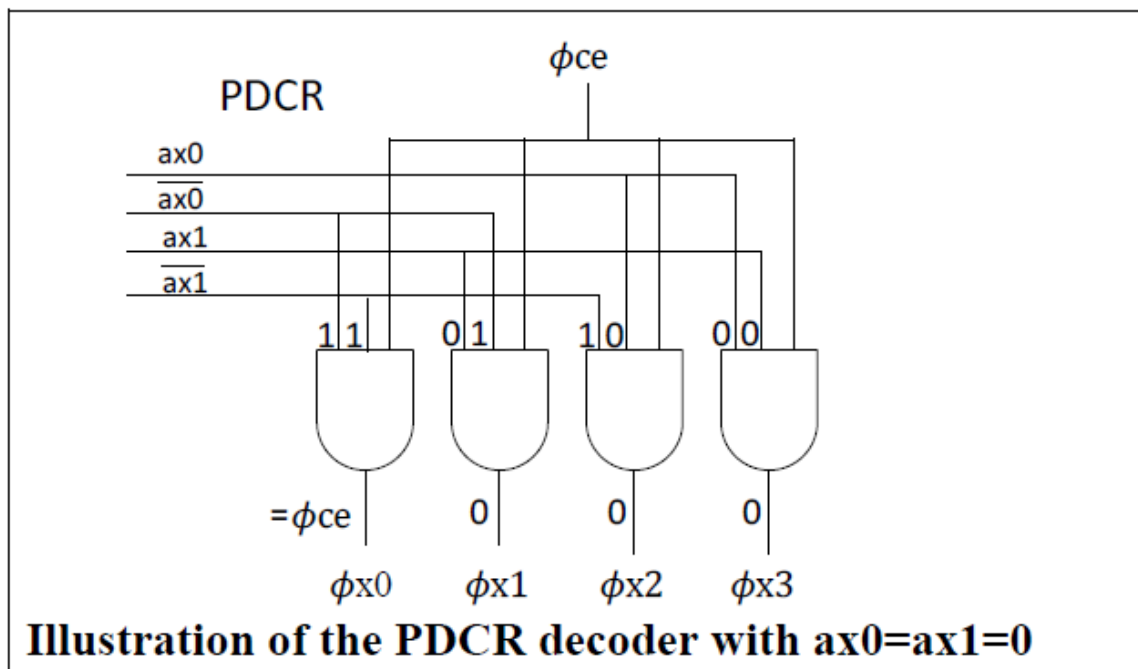
global clock, and in such systems, one would expect memory selection signals to be synchronous to the global clock.” *Id.*, ¶34. And, under such conditions Sato’s “circuit would meet the claim limitations under Dr. Pedram’s restrictive definition of ‘clock signal.’” *Id.*

Further, Sato teaches that the invention “can be applied widely to semiconductor memory devices having at least a clocked static type address decoder.” Pet. 14, 15 (citing APPLE-1005, 12:4-6). Thus, even if Sato’s timing signal ϕ_{ce} is not considered to be periodic, Sato provides an express teaching that its address decoder can be modified for operation with a clock signal. *Ortho-McNeil Pharm., Inc. v. Mylan Labs., Inc.*, 520 F.3d 1358, 1364 (Fed. Cir. 2008) (“a flexible TSM test remains the primary guarantor against a non-statutory hindsight analysis such as occurred in this case.”). While PO dismisses this statement as “Sato’s unexplained, unsupported opinion,” it is in-fact an express teaching in the reference itself that the address decoder described therein can be applied to clocked or synchronous memory systems. APPLE-1013, ¶36. Furthermore, Dr. Pedram confirmed that prior to the filing date of the ’002 patent, a POSITA would have been capable of purchasing known components and “putting them together” to form “clock generation circuitry that would produce the clock signal” recited in the ’002 patent claims. APPLE-1019, 48:2-21. Thus, not only does Sato expressly teach its address decoder is modifiable for use in clocked synchronous systems

(according to the TSM test), but doing so would merely have been the result of combining known prior art components according to known methods to achieve predictable results. APPLE-1013, ¶36; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416, (2007).

D. Sato does disclose a “clock output” as recited in the claims

PO does not contest Petitioner’s and Dr. Horst’s explanation of how a POSITA would understand the operation of Sato’s PDCR functioning as a demultiplexer that selectively gates the timing signal. Pet., 18-22; APPLE-1003, ¶¶60-63, 65-66, 70-71; APPLE-1013, ¶¶12-14. Dr. Pedram explains clock gating is a process that “allow[s] the clock signal to propagate to the rest of the circuit under one condition—or set of conditions, and then stop[s] it from propagating through under [other] conditions.” APPLE-1019, 31:6-11. Accordingly, in view of both Dr. Horst and Dr. Pedram’s explanations, a POSITA would have understood that Sato’s PDCR would function by selectively allowing the input timing signal ϕ_{ce} to propagate or not propagate along one of the PDCR output lines ϕ_{x0} – ϕ_{x3} according to the state of the address signals ($ax0$ and $ax1$) and their compliments. Pet., 18-22; APPLE-1003, ¶¶60-63, 65-66, 70-71; APPLE-1005, 5:25-42, 9:44-59; APPLE-1013, ¶14.



Pet., 22.

Instead, PO provides a purely semantic counter argument claiming that the outputs of SATO's PDCR would not be considered clock outputs "[e]ven if Sato's signal ϕce is considered to be a clock signal" because "Sato refers exclusively to signals $\phi x0$, $\phi x1$, $\phi x2$, and $\phi x3$ as 'selection signals'" not timing signals.

Response, 46-47. But, as Dr. Horst explained at his deposition, Sato uses the terms "timing signal" and "selection control signal" interchangeably. Ex. 2005, 38:9-13. Yet, the functional similarity between Sato's PDCR and the '002 patent's "second logic" and conditional clock generator is undisputed. APPLE-1013, ¶14.

For these reasons, PO's semantic argument as to why Sato does not disclose clock outputs fails.

**IV. ASANO AND ITOH RENDER CLAIMS 1-17, 20-28, AND 31-36
OBVIOUS (GROUND 2)**

Petitioner set forth a complete and proper *prima facie* analysis in the petition showing that Asano and Itoh render claims 1-17, 20-28, and 31-36 obvious.⁴ Pet. 33-81. Here, PO's arguments rely primarily on a mischaracterization of Petitioner's application of Asano and Itoh to the claims. Petitioner does not argue Asano's isolated block representation of a predecoder 202 represents both the first and the second logic recited in the claims. Rather, Petitioner explains that, when implemented using the decoder circuits disclosed by Itoh, the internal structure of the predecoder 202 "would be built as separate logic sections for decoding different portions of [Asano's] 6-bit memory address." Pet., 35-41.

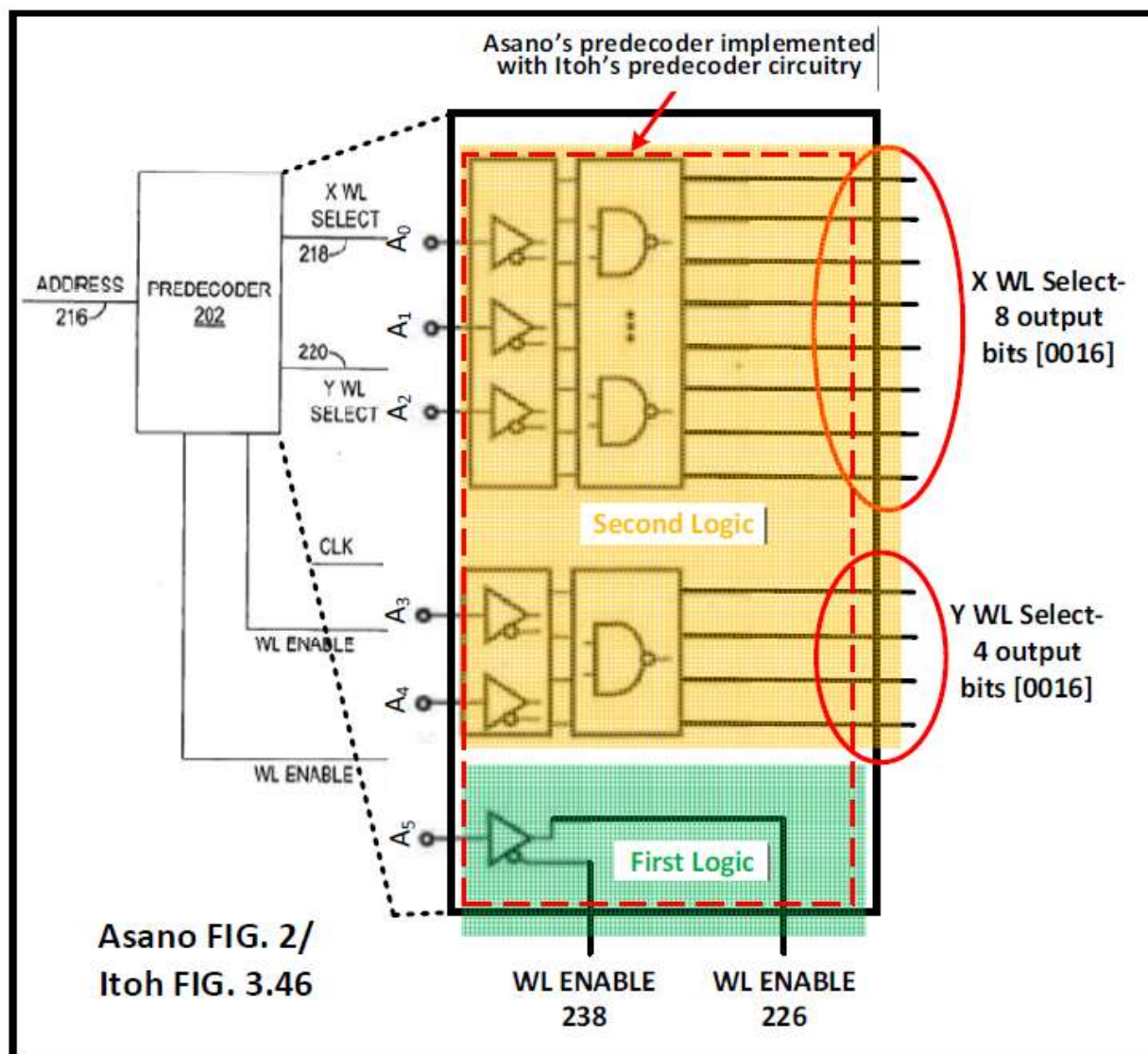
**A. The combination of Asano and Itoh renders a circuit device
with distinct "first logic" and "second logic" obvious**

First, PO argues Asano "does not disclose splitting a memory address into first and second portions." Response, 48. Yet, this argument ignores Petitioner and Dr. Horst's explanation of how Asano's predecoder partitions the six input address bits into individual sets of 1, 2, and 3 separately decoded address bits to "derive[] a wordline enable signal and two wordline select signals." Pet., 36

⁴ Petitioner's application of Asano and Itoh to the dependent claims remains uncontested. See Response; APPLE-1019, 37:11-14.

(quoting APPLE-1006, [0016]), 37-38; APPLE-1003¶¶121-124. Even Dr. Pedram explains that partitioning address bits is not necessarily a physical partition, but a logical partition into different “group[s] of bits as ... sets of elements, [where] the intersection of the two sets is [a] null [set].” APPLE-1019, 18:21-23, *see also* 18:7-19:1.

PO further argues Asano’s predecoder cannot represent separate and distinct first and second logics because “the predecoder 202 is a single predecoder.” Response, 50. However, this misconstrues Petitioner’s argument; which is that when implemented using the decoder circuits disclosed by Itoh, **the internal structure of the predecoder 202** “would be built as separate logic sections for decoding different portions of [Asano’s] 6-bit memory address.” Pet., 35-41. And, the petition clearly illustrates this distinction in an annotated figure combining Itoh’s internal predecoder logic circuits with Asano’s block diagram.



Pet., 38.

Dr. Pedram also acknowledged the distinction between a functional block diagram and physical implementation of block components thereof as distinct logical components. APPLE-1019, 50:4-51:24. Dr. Pedram described that in teaching his students to partition a 6-bit address into 1-bit, 3-bits, and 2-bits (similar to Asano), he would have taught them to use separate and distinct

combinations of logic circuitry to decode each set of bits. APPLE-1019, 22:5-23:24, 23:12-15 (“But obviously, the AND gates that’s used in one part to deal with one combination [of address bits] is different than the AND gate that is used in a different part to deal with a different combination ...”). Similar to Petitioner’s annotated drawing above, Dr. Pedram explained during deposition how, prior to October 10, 2006, his students would decode address bits partitioned in the manner disclosed in Asano using separate and distinct logic for each group of bits, as shown in Itoh:

Q. Are you saying you would use one set of AND gates for the 1-bit, another set for the 2 bits and another set for the 3 bits?

A. So one implementation would be precisely what you said. Of course, for the 1-bit, you won't use any AND gates. But yeah, for the 2 and 3 bits, the AND gates that would do the decoding of the 2-bit group will be different from the AND gates that are used for the decoding of the 3 bits.

APPLE-1019, 23:16-24; APPLE-1013, ¶37 (Dr. Horst agreeing). As Dr. Horst previously explained “it is well known that an equivalent AND function can be implemented in other ways, such as with a NAND gate followed by an inverter.” APPLE-1003, ¶112.

B. The petition articulates a clear motivation for combining Asano and Itoh

The petition explains that Itoh discloses fundamental textbook “decoding circuits” and “prerecording circuits,” “which a POSITA would have readily applied [to Asano’s block diagram] if seeking to implement Asano’s predecoder 202.” Pet., 35. Furthermore, “[b]ecause Asano represents the predecoder 202 simply using a block element ... a POSITA would have looked to Itoh’s textbook circuits [to determine] how the internal structure of the predecoder would be built” to separately “derive[] a wordline enable signal and two wordline select signals” from Asano’s six address bits. *Id.*, 35, 36 (quoting APPLE-1006, [0016]). The petition continues, a “POSITA designing Asano’s memory circuit would have naturally turned to a textbook ... for the details on memory design techniques for [building] a predecoder.” *Id.*, 35 (citing APPLE-1003, ¶121). The petition concludes, “[t]he POSITA would have understood that Itoh’s individual predecoder circuits would merely perform their intended functions when implemented in Asano’s predecoder 202.” *Id.*, (citing APPLE-1003, ¶¶121-123). Thus, the petition sets forth the judicially recognized motivation for combining the teaching of two references by combining known prior art elements according to known methods to achieve predictable results. *KSR*, 550 U.S. at 416.

PO argues Petitioner’s rationale is insufficient because the petition describes Itoh’s circuits as “*a possible implementation of the internal structure for the*

predecoder.” Response, 54 (quoting Pet., 35) (emphasis in original). PO argues this statement is problematic because “Petitioner admits that Itoh discusses just one of multiple different ways that Asano’s predecoder 202 could be implemented.” *Id.* While PO may be correct that there are many other references which would render the ’002 patent claims obvious, it does not negate the fact that the Asano/Itoh combination is one specific example that does so. The *KSR* decision, for example, does not require Petitioner to evaluate and compare every reference that would render a claim obvious, but only to provide a rational motivation for why a POSITA would combine the teachings of the references chosen. Here, the motivation set forth in the present petition meets at least one judicially recognized motivation for combining the teaching of Asano and Itoh. *KSR*, 550 U.S. at 416. The law requires no more.

PO also argues Petitioner’s obviousness rationale is insufficient for “repeatedly argu[ing] that ‘[a] POSITA *could have* implemented Asano’s predecoder using a combination of the predecoder circuits disclosed by Itoh.”” Response, 55 (quoting Pet., 37) (emphasis in original). PO also states “Petitioner has provided no reasoning why the POSA *would have* been motivated to implement Asano’s predecoder using circuits disclosed by Itoh.” *Id.* The excerpts from page 35 of the petition quoted above with extra emphasis added to each usage of “would have” demonstrates the baselessness of this argument.

V. THE OPINIONS OF DR. HORST ARE ENTITLED TO CONSIDERABLY MORE WEIGHT THAN THOSE OF DR. PEDRAM

Dr. Horst's testimony meets the Board's requirements for expert testimony. *Trial Practice Guide Update*, 2-4, (August 2018). Dr. Horst is a technical expert, not a legal one, and his testimony is accordingly directed to specific teachings of the prior art to assist the Board's understanding of the evidence. Contrary to PO's arguments, an expert's declaration is not required to present a *prima facie* invalidity analysis. See Response, 6, 29-30. That is the role of the Petition, not the expert declaration. See *e.g.*, 35 USC §312(a)(3); 37 CFR §§ 42.22(a)(2), 42.104(b)(4), (5); *Zetec, Inc. v. Westinghouse Elec. Co.*, Paper 10 at 6.

A. Dr. Pedram's testimony is tainted by his failure to consider the scope of the '002 patent claims

Dr. Pedram's opinions, on the other hand, are not relevant or reliable, because he failed to consider the proper scope of the '002 patent claims, instead limiting his opinion only to specific embodiments. APPLE-1019, 53:6-7, 52:15-53:23, 63:11-23, 88:25-90:23 (repeatedly stating he did not consider the scope of the claims in his opinions but only the context of "the preferred embodiment of Figure 1 of '002"). Therefore, by his own admission, Dr. Pedram's opinion is based on an improper interpretation of the claims that effectively limits the claim scope to particular embodiments. *Superguide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) ("a particular embodiment appearing in the

written description may not be read into a claim when the claim language is broader than the embodiment.”).

B. Dr. Pedram’s testimony is tainted by his failure to consider objective evidence contrary to his opinions

As noted above in sections II.D and III.B, several of Dr. Pedram’s opinions are demonstrably incorrect for failing to consider the totality of evidence readily available to him in this proceeding. Dr. Pedram asserts the “words ‘clock signal’ and ‘timing signal’ are not interchangeable” when the dictionary definition he presents for “clock signal” lists “clock pulse” and “timing pulse” as synonyms of “clock signal.” Dr. Pedram also asserts “the Greek symbol phi would not be understood by the POSA to refer to a clock signal.” Yet, two references presented with the petition, Itoh and Shin, explicitly contradict his opinion. APPLE-1007, 149; APPLE-1011, 1:23-42.

C. Dr. Pedram’s testimony is based on an inaccurate understanding of the law of obviousness

Dr. Pedram based his opinion on an inaccurate understanding of the law. Referring to the law of obviousness, Dr. Pedram’s declaration states: “This ‘as a whole’ assessment requires showing that one of ordinary skilled the art at the time of invention, confronted by the same problems as the inventor ... would have selected the elements from the prior art and combined them in the claimed manner.” Ex. 2001, ¶25; APPLE-1019, 36:6-20. However, this statement of the

“as a whole” inquiry requiring a consideration of the “**same problems as the inventor**” is contrary to the Supreme Court Opinion stated in *KSR*; and is precisely one of the errors that the Court corrected. *KSR*, 550 U.S. at 420 (“[t]he first error...in this case was...holding that courts and patent examiners should look only to the problem the patentee was trying to solve.”). Consequently, Dr. Pedram’s testimony is also tainted by a misunderstanding of the law of obviousness.

VI. CONCLUSION

As is evident from the discussion above and in the Petition, no claim of the ’002 patent challenged here represents patentable subject matter.

Respectfully submitted,

Date: July 15, 2019

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CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petitioner's Reply to Patent Owner's Response totals 5,526, which is less than the 5,600 allowed under 37 CFR § 42.24.

Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR § 42.8(b), the undersigned certifies that on July 15, 2019, a complete and entire copy of this Petitioner's Reply to Patent Owner's Response and all supporting exhibits were provided via email to the Patent Owner by serving the correspondence email addresses of record as follows:

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