

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple, Inc.,
Petitioner,

v.

Qualcomm Incorporated,
Patent Owner

Case IPR2018-01249
U.S. Patent No. 7,693,002

PATENT OWNER SUR-REPLY

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I. Introduction

Petitioner's reply introduces unpersuasive and belated arguments and evidence that cannot salvage the petition. Sato does not meet the "clock signal" limitation of the claims, as properly construed, and Petitioner failed to present an adequate motivation to combine Asano and Itoh. The Board should confirm the patentability of claims 1-28 and 31-37.

II. Claim Construction – "Clock Signal"

A. Petitioner's Criticism Of Dr. Pedram's Testimony Is Misplaced

In his expert declaration supporting Qualcomm's response, Dr. Pedram provided extensive testimony showing that the term "clock signal" should be interpreted as "a periodic signal used for synchronization." Ex. 2001 at 53-70. The reply argues that "Dr. Pedram's opinion on the BRI of the term 'clock signal' ... should be accorded little weight" because he has not provided testimony on the full scope of the claims. Paper 15 at 2-3.

Petitioner's criticism is misplaced. The reply cites no legal authority for the proposition that an expert must consider and testify as to the full scope of claims in order to opine on the meaning of certain claim terms. In preparing his expert declaration, Dr. Pedram considered and testified as to a number of discrete issues: (i) the meaning of the term "clock signal," and (ii) whether Petitioner's unpatentability grounds render obvious the challenged claims. *See generally*

Ex. 2001. None of these issues required consideration of the “exact scope of the claims.”¹

B. Qualcomm’s Construction Is Not Inconsistent With The Conditional Clock Outputs Of The ’002 Patent

The reply argues that because the challenged claims require a first logic and/or conditional clock generator that applies a clock signal to a selected one of multiple clock outputs, Qualcomm’s “interpretation of the term ‘clock signal’ is too narrow to even encompass the clock signals carried by ‘clock outputs’ of the ’002 patent claims.” Paper 15 at 3-4.

Petitioner’s argument is based on the unfounded assumption that in the ’002 patent, *all of the clock outputs* of the conditional clock generator *are always carrying a clock signal*. But they are not. In fact, the specification repeatedly makes clear that “[t]he conditional clock generator 110 receives a clock signal via the clock input 118 and selectively applies the clock signal to a *selected one* of the clock outputs 124, 126, 128 and 130” (Ex. 1001 at 3:28-31), and that

¹ The reply also criticizes Dr. Pedram as lacking understanding of the law of obviousness, citing a statement in his declaration that is allegedly contrary to the Supreme Court’s decision in *KSR*. Paper 15 at 27-28. Qualcomm disputes this criticism. As Dr. Pedram made clear at deposition, his understanding of obviousness is not limited to the legal standards recited in his declaration. *See* Ex. 1019 at 36:6-15. Thus, even assuming that the declaration contains a misstatement regarding the law of obviousness, this does not show that Dr. Pedram lacks a sufficient understanding of the law.

“[s]ince only one of the four clock outputs 124, 126, 128 and 130 may be active at a time,” the non-selected clock outputs are held at a fixed voltage level (*id.* at 3:52-62). Dr. Horst confirmed this at deposition. Ex. 2006 at 94:23-24, 98:23-25. Thus, in the ’002 patent, the selected clock output carries the clock signal, but the fixed voltage level on the non-selected clock outputs is not a clock signal.

The POSA would thus understand that in the ’002 patent, all of the clock outputs are not carrying a clock signal at all times. Accordingly, the fact that Qualcomm’s construction of “clock signal” does not encompass the fixed voltage levels of the non-selected clock outputs is consistent with the intrinsic evidence.

C. The Reply Does Not Rebut Qualcomm’s Showing That Its Construction Is Supported By The Intrinsic Evidence

The response showed that the intrinsic evidence supports Qualcomm’s proposed construction of “clock signal.” Paper 11 at 11-15. In fact, the invention of the ’002 patent is specifically intended to address problems that arise from the use of a periodic clock signal. Such a clock signal periodically switches between logic-level high and low states, thus resulting in high power consumption, and because the periodic clock signal is distributed to many different components of the memory system to synchronize them, a heavy load is placed on the clock signal. *See* Ex. 1001 at 1:11-25. The invention of the ’002 patent is intended to address the problems of

power consumption and loading that result from the use of a periodic, synchronizing clock signal. *See id.*

The reply does not rebut any of Qualcomm's showings. Paper 15 at 5-6. Instead, Petitioner argues that the '002 patent does not include explicit description of certain aspects of computer memory systems, and that therefore, no conclusion can be drawn from the patent's complete lack of any suggestion of an asynchronous system. *Id.* Petitioner's argument misses the point. Patents need not disclose what is well known in the art. *Lindemann Maschinenfabrik GMBH v. Am. Hoist and Derrick Co.*, 730 F.2d 1452, 1463 (Fed. Cir. 1984). Thus, the '002 patent's alleged lack of description of conventional components like "clock drivers" and "column address decoders" (Paper 15 at 5-6) is of no consequence.

But Petitioner's assertion that the claims should read on asynchronous memory systems when none are described in the patent, and the patent consistently describes features and functionality found only in synchronous systems, is not credible. If the inventors intended the claims to read on asynchronous memory systems that lacked a periodic clock signal—even though a primary motivation of the invention is to reduce the heavy load and large power consumption of the clock signal of a synchronous system—the specification would include some description or suggestion of asynchronous systems. It does not. The patent provides no basis for interpreting the claims as broadly as Petitioner proposes.

D. Extrinsic Evidence Shows That Petitioner’s Construction Of “Clock Signal” Is Overly Broad

Qualcomm showed in its response that unbiased and reliable extrinsic evidence supports its construction of “clock signal” as “a periodic signal used for synchronization.” Paper 11 at 11-12. Specifically, the response cited the IEEE Dictionary’s definition of the term “clock signal” as “[a] periodic signal used for synchronizing events.” Ex. 2002 at 9.

Petitioner does not dispute that the IEEE Dictionary’s definition of “clock signal” is nearly identical to Qualcomm’s proposed construction of the same term. Paper 15 at 6-7. Instead, Petitioner cites the IEEE Dictionary’s definition of “clock” and argues that this definition shows that the claimed “clock signal” need not be periodic. *Id.* (citing Ex. 1014 at 4). As an initial matter, the claim term at issue is “clock signal”—not “clock”—and Petitioner provides no explanation as to why the IEEE Dictionary’s definition of “clock” is allegedly more relevant than the dictionary’s definition of “clock signal.” *See* Paper 15 at 6-7. It is not. The IEEE Dictionary has *seven entries* for the term clock, as Dr. Horst acknowledged at deposition (Ex. 2006 at 71:21-72:3), but only *one entry* for the term “clock signal,” thus demonstrating that the term “clock” is broader than the term “clock signal” and not its equivalent. *See* Ex. 1014 at 4.

In any event, Petitioner’s cited definition of “clock” from the IEEE Dictionary is completely silent as to whether the signal needs to be periodic. Ex. 1014 at 4. But when read in conjunction with the dictionary’s definition of “clock signal”—“[a] *periodic signal* used for synchronizing events”—it is clear that the signal is, in fact, periodic. *Id.* at 5 (emphasis added).

Petitioner’s argument based on the Modern Dictionary of Electronics (Paper 15 at 7) fails for similar reasons. The reply cites the Modern Dictionary’s definitions of “clock”—*not* “*clock signal*”—but the cited definitions provide no indication as to whether a clock signal is periodic or not. Dr. Horst conceded this at deposition. Ex. 2006 at 79:8-12.

When read in conjunction with other portions of the Modern Dictionary of Electronics, however, it is clear that the signal is periodic. For example, the dictionary defines “clock frequency” as follows: “In digital computers, the master frequency of periodic pulses that are used to schedule the operation of the computer.” Ex. 1015 at 4. This definition references the “digital computer” system mentioned in the definition of “clock” (*id.* at 3-4) and shows that synchronization in such a system is performed using a periodic signal.

**E. Itoh Does Not Show That The Claimed “Clock Signal”
Encompasses Non-Periodic Signals**

Qualcomm showed in its response that the POSA would not have viewed timing signals in asynchronous systems as clock signals. Paper 11 at 12-14. Qualcomm showed, among other things, that Itoh’s row address strobe \overline{RAS} and column address strobe \overline{CAS} are asynchronous memory “timing signals” or “control signals” (Ex. 2001 at ¶¶59-62), and that Itoh never refers to these signals as being “clock signals” (*id.*). In fact, page 361 of Itoh explicitly refers to the row address strobe \overline{RAS} and column address strobe \overline{CAS} as “control signal[s],” rather than “clock signals,” as claimed. Ex. 2003 at 361.

In an attempt to rebut this showing, Petitioner cherry picks excerpts from a completely different portion of Itoh—pages 142 and 149, more than 200 pages before Qualcomm’s cited portions at page 361—mentioning an “ \overline{RAS} clock buffer” and “a clock Φ_B generated by the \overline{RAS} buffer.” Paper 15 at 7-8. But Petitioner has not established the relevance of the earlier portion of Itoh at pages 142 and 149 to the later portion at page 361 cited by Qualcomm. *See id.* The later portion of Itoh shows \overline{RAS} to be a non-periodic “control signal”—in contrast to the periodic clock signal CLK—and includes no description or illustration of an “ \overline{RAS} clock buffer” or “a clock Φ_B .” Ex. 1007 at 142, 149. Thus, there is no indication that the earlier-described “ \overline{RAS} clock buffer” and “clock Φ_B ” are somehow relevant to the later-

described \overline{RAS} signal, much less any indication that the non-periodic \overline{RAS} signal should be considered a clock signal.

The reply also argues that in the synchronous system of Itoh Figure 6.15, the non-periodic address strobe signal RS1 is used in activating a wordline, and that this disproves Qualcomm's contention that a periodic clock signal synchronizes all memory operations in synchronous systems. *See* Paper 15 at 8-9. But Qualcomm does not dispute that timing signals other than the periodic clock signal may be used to time operations in synchronous systems. *See, e.g.*, Ex. 2001 at ¶¶62. In synchronous systems, all events and all timing signals—such as the RS1 signal in Figure 6.15 of Itoh—are synchronized to the single, periodic clock signal, whereas no such single synchronizing signal exists in asynchronous systems. *Id.* at ¶¶60-62. Figure 6.15 of Itoh clearly shows that both RS1 and CS1 are triggered by the clock signal's rising edge and are thus synchronized by the periodic clock signal. Ex. 2003 at 19.

Petitioner also argues that in the synchronous system of Itoh Figure 6.15, the CLK clock signal “is not necessarily passed to an address decoder.” Paper 15 at 9-10. But even if true, this proves nothing. Qualcomm never argued that the system of Itoh Figure 6.15 is the same as the memory system of the '002 patent. Ex. 2001 at ¶¶61-69. Petitioner's argument that the two systems are not identical is a red herring and does not rebut Qualcomm's showing.

F. Petitioner's New References Do Not Support Its Construction

In a last-ditch effort, Petitioner cites new references that allegedly “refer to non-periodic signals as clock signals.” Paper 15 at 10. But none of these references supports the overly broad construction of “clock signal” advanced in the reply.

Petitioner cites U.S. Patent No. 4,922,461 to Hayakawa (Ex. 1016) and argues that this reference refers to a clock signal (ϕS) that “is only ‘effective in level for a fixed period of time.’” Paper 15 at 10 (citing Ex. 1016 at 3:50-57). But the cursory argument of the reply does not show that the signal ϕS of Hayakawa is non-periodic. The phrase “effective in level for a fixed period of time” is ambiguous and does not indicate whether the signal ϕS is periodic or not. Moreover, other portions of Hayakawa indicate that signal ϕS transitions between logic-level low and high states at regular, periodic intervals. Ex. 1016 at 6:3-22, 6:65-7:3.

The reply also cites two papers published by Qualcomm’s expert Dr. Pedram (Exs. 1017, 1018) as allegedly disclosing non-periodic clock signals. Paper 15 at 10. But Petitioner’s citation to these papers merely evidences its misunderstanding of a *gated clock signal* in relation to the claimed “clock signal.” As Dr. Pedram testified at deposition, a “gated clock signal” is different than the claimed “clock signal” and can be turned on and off to propagate the clock signal or not. Ex. 1019 at 31:7-11. Whenever the clock signal is being propagated, it is a periodic signal for the reasons

explained in Qualcomm's response. Paper 11 at 11-15. Petitioner's cursory argument (Paper 15 at 10) does not disprove this.

G. Dr. Alpert's Previous Testimony On The Meaning Of "Clock" Is Relevant To The Construction Of "Clock Signal"

Qualcomm's response showed that Apple's ITC expert, Dr. Alpert, previously told the Board that the term "clock" should be interpreted as "a periodic signal used for synchronization." Paper 11 at 14-15 (citing Ex. 2004 at 3-4). The reply argues that Dr. Alpert's previous testimony was "on behalf of a different party (not Apple), in a different IPR, and in reference to a different patent" (Paper 15 at 10-11), and is therefore irrelevant.

But Petitioner is wrong. As Qualcomm showed, Dr. Alpert testified that the "definition ['a periodic signal used for synchronization'] is consistent with the broadest reasonable interpretation of the term ['clock']." Ex. 2004 at 3-4. In so testifying, Dr. Alpert relied on the very same IEEE Dictionary definition that Qualcomm now cites. *See id.* Moreover, Dr. Alpert did not qualify his opinion on the meaning of "clock" or indicate that it was specific to that previous proceeding or the patent involved therein. *See* Ex. 2004 at 3-4. The fact that Dr. Alpert was testifying on behalf of a different party in the previous proceeding is of no consequence.

H. Petitioner’s Proposed Construction Is Wrong For The Reasons Stated In Qualcomm’s Patent Owner Response

The reply argues that the term “clock signal” should be construed as “a signal used for synchronization.” Paper 15 at 11. This construction is overly broad because it encompasses non-periodic timing and control signals. The POA would not consider any of these signals to be clock signals for the reasons stated in Qualcomm’s response. Paper 11 at 11-15. The Board should apply the proper construction of clock signal proposed by Qualcomm, *i.e.*, “a periodic signal used for synchronization,” for the reasons stated above and in Qualcomm’s response.

III. Sato Does Not Render Obvious Claims 1-28 And 31-37 (Ground 1)

A. The Petition Failed To Address All Of The *Graham* Factors

Qualcomm’s response showed that the petition failed to establish a *prima facie* case of obviousness over Sato because it did not identify any differences between the reference and the claims. Paper 11 at 28-30.

In its reply (Paper 15 at 12-13), Petitioner cites the petition’s statement that Sato’s selection control signal ϕ_{ce} allegedly “represents or renders obvious a clock signal” (Paper 2 at 14), and argues that this is a sufficient identification of a difference between the claims and Sato. But this statement only highlights the gamesmanship employed by Petitioner. Specifically, this statement and others (*id.* at 14-17) show that Petitioner knew when its petition was filed that the key dispute for Sato would be whether it discloses a clock signal. Despite this, Petitioner failed

to provide any construction for the term until its reply. And rather than explain any differences between Sato's selection control signal ϕ_{ce} and the claimed clock signal, Petitioner instead presented Sato as if it was anticipatory, asserting multiple times that the signal ϕ_{ce} is a clock signal. *See, e.g.*, Paper 2 at 10 ("Sato selectively applies a clock signal (ϕ_{ce}) to wordline drivers....").

If Petitioner believed that Sato's selection control signal ϕ_{ce} is a clock signal, then the petition should have presented Sato as an anticipation ground. It did not. Instead, the petition hedged on the meaning of clock signal and further hedged on whether Sato allegedly anticipates the claims or renders them obvious. This is contrary to "the expedited nature of IPRs," which "bring[s] with it an obligation for petitioners to make their case in their petition to institute." *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016).

B. Sato Does Not Disclose The Claimed "Clock Signal" Because Its Selection Control Signal ϕ_{ce} Is Not Periodic

Sato's signal ϕ_{ce} does not teach or suggest the claimed clock signal because it is not periodic. Paper 11 at 30-33. In its reply, Petitioner points to the IEEE Dictionary's definition of "clock signal" indicating that this term is synonymous with "clock pulse" (Ex. 1014 at 5), and argues that the terms "clock signal" and "timing signal" should therefore have the same meaning. Paper 15 at 13. But the dictionary nowhere equates the term "clock signal" with either of the specific terms

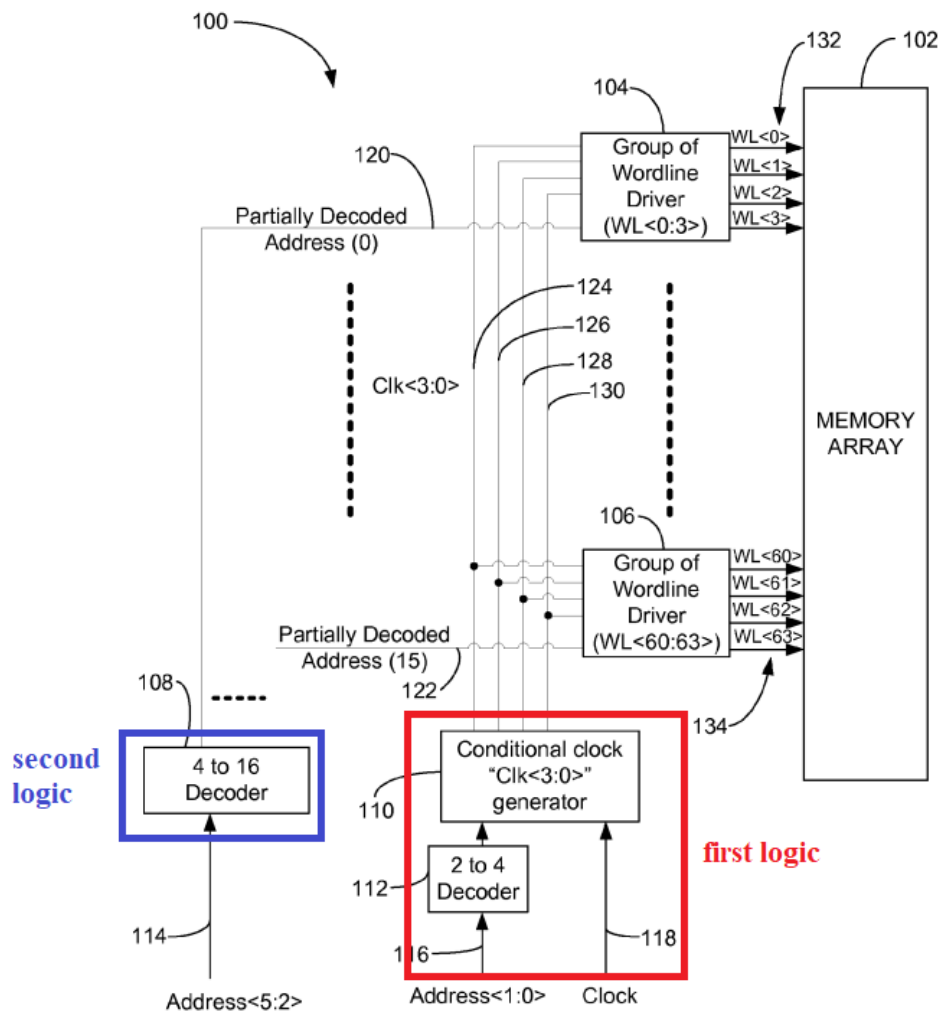
recited in Sato, *i.e.*, “timing signal” and “selection control signal.” *See* Ex. 1014 at 4-5. The cited definition of “clock signal” instead only refers to the different term “clock pulse” (*id.* at 5), and Qualcomm does not dispute that a periodic clock signal may be understood as including a plurality of regularly spaced, uniform clock pulses. This is not proof, however, that the terms “clock signal” and “timing signal” are interchangeable. Moreover, the IEEE Dictionary definition of “clock pulse” merely states “*See*: clock signal.” Ex. 2002 at 9.

The reply also disputes Dr. Pedram’s testimony (Ex. 2001 at ¶109) that the symbol ϕ is used in the art to denote a phase signal, not a clock signal. Paper 15 at 14. Petitioner cherry picks references that use the symbol ϕ to refer to a clock signal, but the existence of one or more isolated references that use the symbol ϕ in this non-conventional manner does not rebut Dr. Pedram’s testimony of how this symbol is most commonly used in the art. Dr. Pedram has over 30 years of experience in the field of computers and memory systems, and his testimony on the common usage of the symbol ϕ is informed by this extensive experience. *See* Ex. 2001 at ¶¶4-19.

Petitioner tries to minimize the gulf between Sato and the ’002 patent, stating that “[a]ny disagreement is merely over the timing of pulses in Sato’s timing signal.” Paper 15 at 15. But as Qualcomm explained (Paper 11 at 33-35), the asynchronous memory system of Sato—which uses multiple, non-periodic timing signals—is

fundamentally different than the synchronous memory system of the '002 patent, which uses the single, periodic clock signal. *Id.* at 12-15 (explaining that asynchronous memory systems are event-driven and must include control circuitry for receiving the asynchronous inputs and generating appropriately timed sequences of internal timing signals, whereas in synchronous memory systems, a single, periodic, synchronizing clock is used to time all memory operations). Accordingly, Sato's failure to disclose one of the distinguishing factors between synchronous and asynchronous systems, *i.e.*, a periodic clock signal, is not a minor difference, as Petitioner suggests.

Moreover, Sato's failure to disclose the periodic clock signal is not the only difference between Sato and the '002 patent. *See, e.g.*, Paper 11 at 22-23 (explaining difference between parallel arrangement of '002 patent and serial operation of Sato, where the parallel arrangement reduces a timing delay in providing the clock signal to a particular wordline driver). For example, Sato fails to achieve reduced loading on a clock signal, in contrast to the design of the '002 patent. The Background section of the '002 patent describes that one of the problems of conventional memory systems was the heavy load placed on the clock signal. Ex. 1001 at 1:11-25. To address this issue and others of the prior art, the '002 patent describes an improved wordline driver system having separate first and second logics:



Id. at Fig. 1 (annotations added).

The '002 patent describes that the first logic decodes a first portion of the memory address and applies a clock signal to a selected clock output. *Id.* at 3:26-31. The second logic, by contrast, decodes a second portion of the memory address and selectively activates a particular wordline driver, operating independently of the clock signal. *Id.* at 3:36-45. Accordingly, in the '002 patent, the first portion of the memory address is clocked, while the second portion is not, and there is a decoupling

of the clocking functionality of the circuit device from its decoding functionality. This design provides the benefit of reduced loading on the clock signal, thus addressing the problem described in the Background section of the patent. Ex. 1001 at 1:11-25.

In Sato, by contrast, both of the circuits that Petitioner identifies as the “first logic” and “second logic” are controlled by the alleged clock signal ϕ_{ce} , and the alleged second logic of Sato *does not* activate a particular wordline driver independently of the clock signal. Specifically, in Sato, the PDCR (*i.e.*, the alleged “first logic”) receives and processes the selection control signal ϕ_{ce} in generating its output. Paper 11 at 16-23. Further, Sato makes clear that the operation of the NAND gate circuits NAG0-NAGk (*i.e.*, the alleged “second logic”) is controlled by the selection control signal ϕ_{ce} . Ex. 1005 at 5:66-6:21. Petitioner’s declarant Dr. Horst confirmed this at deposition. Ex. 2005 at 34:10-16. Thus, both the alleged first and second logics of Sato operate based on the alleged clock signal ϕ_{ce} , and this is in contrast to the design of the ’002 patent.

C. Sato Does Not Render Obvious The Periodic “Clock Signal” Required By The Claims

Perhaps recognizing that Sato includes no disclosure or suggestion of a periodic clock signal, Petitioner advances the backup argument that Sato somehow renders this limitation obvious. Paper 15 at 16-18. Petitioner specifically argues

that “a POSITA would have understood that Sato’s address decoder would function fundamentally the same regardless of whether the timing signal was periodic or not.”

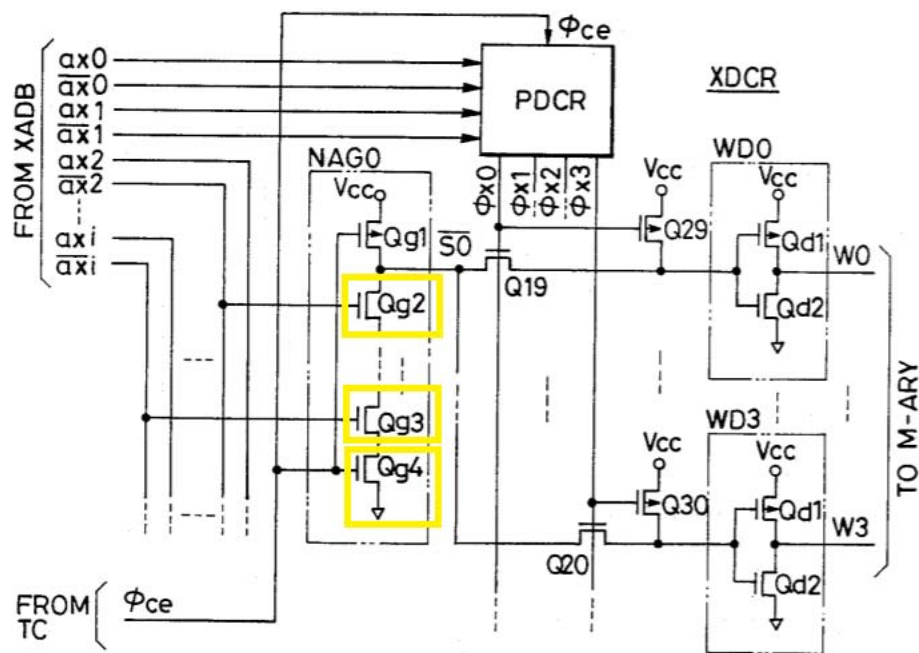
Id. at 16.

Petitioner fails to provide any evidence or analysis to show that Sato would work with a periodic clock signal. *See* Paper 15 at 16. Petitioner cites the supplemental declaration of Dr. Horst, but the declaration parrots the reply without providing any reasoning or explanation. *See* Ex. 1013 at ¶35. And Dr. Horst conceded at deposition that he performed no simulations or tests to determine whether Sato would actually work with a periodic signal. Ex. 2006 at 87:2-4.

In any event, there are many reasons why the POSA would not have been motivated to modify Sato as proposed. As Qualcomm explained in its response (Paper 11 at 38-39), synchronous systems that use a periodic clock signal are fundamentally different than the asynchronous system of Sato, such that using a periodic clock signal in Sato would require significant modifications that Petitioner has not explained. In a synchronous system, each function is timed with the clock signal’s rising or falling edge. *Id.* Accordingly, to ensure the system’s proper functioning, each function needs to finish its operation within a clock period with some margin. If Sato’s selection control signal ϕ_{ce} is replaced with a periodic clock signal, the circuit will not necessarily be fast enough to handle the clock signal.

For instance, Sato's circuit includes NAND gates NAG0-NAG k that operate in two states—an evaluation state and a precharge state. Ex. 2001 at ¶77; Ex. 2006 at 90:16-22. When the selection control signal ϕ_{ce} is high, the NAND gates are in the evaluation state, and the signal ϕ_{ce} discharges the output of one selected NAND gate to a low level. Ex. 2001 at ¶112; Ex. 2006 at 91:3-13. Discharging the output of the selected NAND gate takes an amount of time that is dictated by characteristics of the three NMOS transistors Qg2, Qg3, and Qg4 of the NAND gate (Ex. 2006 at 91:14-21):

FIG. 3



Ex. 1005 at Fig. 3 (annotations added). In replacing Sato's selection control signal ϕ_{ce} with a periodic clock signal, if the clock signal transitions from high to

low too quickly, the output of the selected NAND gate cannot discharge completely, thus causing the circuit to malfunction. Dr. Horst acknowledged this at deposition. Ex. 2006 at 88:3-5.

Accordingly, if Sato's selection control signal ϕ_{ce} is replaced with a periodic clock signal, in many instances the circuit will not work unless it is specifically redesigned to operate at the frequency of the clock signal.

D. Sato Does Not Meet The “Clock Signal” Limitation Even Under Petitioner's Proposed Construction

Petitioner proposed for the first time in its reply that the term “clock signal” should be construed as “a signal used for synchronization.” Paper 15 at 11. This construction is erroneous, but even if the Board accepts Petitioner's construction, Sato still fails to meet this limitation because the selection control signal ϕ_{ce} is not used for synchronization.

In Sato, the selection control signal ϕ_{ce} is provided to the predecoder PDCR (*i.e.*, the alleged “first logic”) and the NAND gate circuits (*i.e.*, the alleged “second logic”) in such a way that the predecoder gates the outputs of the NAND gate circuits in a serial fashion. Specifically, outputs of the NAND gate circuits are not applied to the wordline drivers until selected by outputs of the predecoder PDCR, which are received by the capacitance cut MOSFETs (*e.g.*, Q19, Q20, etc.). Ex. 1005 at 9:68-10:4. The alleged first and second logics of Sato are not synchronized—

i.e., operating at the same time—because the predecoder PDCR is controlling the output of the NAND gate circuits. In other words, these circuits operate in a serial, asynchronous manner, and not in a synchronous manner. Thus, the selection control signal ϕ_{ce} is not “used for synchronization,” as required by Petitioner’s proposed construction of clock signal.

E. Even If Sato’s Selection Control Signal ϕ_{ce} Is Considered A Clock Signal, The Reference Still Fails To Disclose The Claimed “Clock Outputs”

The petition argues that the outputs of Sato’s predecoder PDCR disclose the claimed “clock outputs” because the POSA would allegedly “understand” that Sato’s PDCR acts as a demultiplexer that applies the signal ϕ_{ce} to its outputs. Paper 2 at 18-23. Qualcomm rebutted this argument in its response, showing that Sato’s predecoder PDCR is a black box, and that Petitioner’s arguments about what the POSA “would understand” are based purely on speculation. Paper 11 at 45-47.

The reply does not dispute that Sato’s predecoder PDCR is a black box. Paper 15 at 18-19. Instead, the reply cites testimony from Dr. Pedram stating that clock gating is a process that “allow[s] the clock signal to propagate to the rest of the circuit under one condition—or set of conditions, and then stop[s] it from propagating through under [other] conditions.” *Id.* at 18 (citing Ex. 1019 at 31:6-11). Qualcomm does not dispute Dr. Pedram’s understanding of clock gating, and in any event, it is irrelevant to whether Sato’s PDCR meets the claimed “clock

outputs.” Sato never suggests that the PDCR performs a “gating” function—much less “clock gating”—and so Dr. Pedram’s testimony does nothing to advance Petitioner’s argument.

For these reasons and those in the response (Paper 11 at 45-47), even if Sato’s signal ϕ_{ce} is considered to be a clock signal, the reference still fails to disclose the claimed “clock outputs.”

IV. Asano And Itoh Do Not Render Obvious Claims 1-17, 20-28, And 31-36 (Ground 2)

A. Petitioner’s Proposed Combination Is Based On Impermissible Hindsight

The splitting of a memory address into multiple portions and the decoding of the two portions at separate first and second logics are fundamental features of the ’002 patent invention. Paper 11 at 47-48. But Asano—“the base reference of Ground-2 of [the] Petition,” *see* Paper 2 at 33—does not disclose or suggest either of these features. Paper 11 at 48-52.

The reply argues that Qualcomm “misconstrues Petitioner’s argument” because the petition proposes implementing Asano’s single predecoder 202 with separate first and second circuits disclosed in Itoh. Paper 15 at 21. But the point is that Asano includes *no disclosure* suggesting that its predecoder 202 should be implemented using multiple decoding logics, as opposed to the single predecoder that the reference expressly teaches. And Petitioner presented no legitimate reasons

why the POSA allegedly would have been motivated to combine Asano with Itoh as proposed, so Petitioner's obviousness argument appears to be based on nothing more than impermissible hindsight reconstruction.

In an attempt to avoid the appearance of hindsight, Petitioner mischaracterizes deposition testimony of Dr. Pedram. Paper 15 at 22-23. The reply argues that "Dr. Pedram explained ... how, prior to October 10, 2006, his students would decode address bits partitioned in the manner disclosed in Asano using separate and distinct logic for each group of bits, as shown in Itoh." *Id.* But this is contrary to Dr. Pedram's actual testimony. At deposition, Dr. Pedram reiterated multiple times that in decoding six address bits, as in Asano, a single decoder module would be used. Ex. 1019 at 21:9-21 ("[T]he overall module is just your decoder. You have one module doing decoding."); *see also id.* at 22:1-2, 22:5-22, 23:25-24:19.

The testimony cited by Petitioner (Ex. 1019 at 23:16-24) does not stand for the proposition that Dr. Pedram taught his students to "decode address bits partitioned in the manner disclosed in Asano using separate and distinct logic for each group of bits" (Paper 15 at 23), as the reply suggests. Rather, in the cited testimony, Dr. Pedram was merely explaining that in decoding six address bits, multiple logic gates would be used:

So obviously you would use distinct gates. So you have different gates. So one logic gate is distinct from another logic gate.

Ex. 1019 at 21:15-17; *see also* 21:21-25, 23:12-16.

Dr. Pedram thus explained that in decoding six bits, the decoding would not all be performed by a single logic gate. Dr. Pedram did not endorse the hindsight-based combination proposed by Petitioner.

B. The Petition’s Motivation To Combine Argument Is Inadequate

Qualcomm showed in its response that the petition does not adequately explain why the POSA would allegedly be motivated to combine Asano and Itoh. Paper 11 at 53-57. The response showed, for instance, that the petition repeatedly argues that “a POSITA *could have* implemented Asano’s predecoder using a combination of the predecoder circuits disclosed by Itoh” (Paper 2 at 37 (emphasis added)) but that such assertions, even if true, are insufficient for a proper obviousness analysis. Paper 11 at 54-55.

The reply highlights four instances from the petition where Petitioner allegedly argued that the POSA “would have” been motivated to combine Asano and Itoh. But each of the four assertions cited in the reply (Paper 15 at 24) is nothing more than a conclusory statement lacking any kind of articulated reasoning with rational underpinning:

[1] Itoh illustrates the circuit design of several predecoder circuits ... which a POSITA would have readily applied if seeking to implement Asano’s predecoder 202.

Paper 2 (Petition) at 35. Neither the petition (*id.*) nor the reply (Paper 15 at 24) provides any reasoning or support for this statement.

[2] Because Asano represents the predecoder 202 simply using a block element in a block diagram, a POSITA would have looked to Itoh's textbook circuits in determining how the internal structure of the predecoder 202

Paper 2 at 35. Here again, the petition provides no reasoning or explanation for this conclusory assertion—*why* would the POSITA have turned to “Itoh's textbook circuits” to implement the predecoder 202? Neither the petition nor the reply say.

The reply argues that *KSR* “does not require Petitioner to evaluate and compare every” possible implementation of Asano's predecoder 202. Paper 15 at 25. Even assuming that to be true, Petitioner must nevertheless “show some *reason* why a person of ordinary skill in the art would have thought to combine [the] *particular* available elements of knowledge [of Itoh] ... to reach the claimed invention.” *Heart Failure Techs., LLC v. Cardiokinetix, Inc.*, IPR2013-00183, Paper 12 at 9 (PTAB July 31, 2013) (emphasis in original). Petitioner has not done this.

[3] A POSITA designing Asano's memory circuit would have naturally turned to a textbook such as Itoh's for details on memory design techniques for a predecoder.

Paper 2 at 35. This statement is unsupported for the same reasons as the previous statement.

[4] The POSITA would have understood that Itoh's individual predecoder circuits would merely perform their intended functions when implemented in Asano's predecoder 202.

Paper 2 at 35. Neither the petition nor the reply provide any explanation or reasoning to support this bald assertion. *See* Paper 2 at 35. The petition cites paragraphs 121-123 of Dr. Horst's initial declaration (Ex. 1003), but the declaration likewise provides no analysis or evidence to demonstrate that it is true.

Petitioner has presented no legitimate reasons why the POSA allegedly would have been motivated to combine Asano with Itoh and therefore has not shown that claims 1-17, 20-28, and 31-36 are obvious over these references.

V. Conclusion

Qualcomm respectfully requests that the Board hold that the challenged claims are not unpatentable.

Respectfully submitted,

Date: August 15, 2019

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CERTIFICATE OF COMPLIANCE

The undersigned hereby certifies that the foregoing Patent Owner Sur-Reply complies with the type-volume limitations of 37 C.F.R. § 42.24(b). Excluding the items listed in 37 C.F.R. § 42.24(a) as not included in the word count, and using the word count of the word-processing system used to prepare the paper (Microsoft Word), the Patent Owner Sur-Reply contains 5,520 words.

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Exhibit List

EX	Description
2001	Declaration of Massoud Pedram, Ph.D.
2002	IEEE Dictionary
2003	Itoh (additional portions)
2004	IPR2015-00148, Declaration of Don Alpert
2005	Horst Deposition Transcript
2006	Horst Second Deposition Transcript