

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Jentsung Lin

U.S. Patent No.: 7,693,002

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Title: DYNAMIC WORD LINE DRIVERS AND DECODERS FOR
MEMORY ARRAYS

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 7,693,002 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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EXHIBITS

APPLE-1001	U.S. Patent No. 7,693,002 to Jentsung Lin (“the ’002 patent”)
APPLE-1002	Prosecution History of the ’002 patent (“the Prosecution History”)
APPLE-1003	Declaration of Dr. Robert Horst, Ph.D
APPLE-1004	Curriculum Vitae of Dr. Horst
APPLE-1005	U.S. Patent No. 4,951,259 to Yoichi Sato (“Sato”)
APPLE-1006	U.S. Patent Pub. No. 2006/0098520 to Toru Asano et al. (“Asano”)
APPLE-1007	Kiyoo Itoh, <i>VLSI Memory Chip Design</i> , (Springer 2001) (“Itoh”)
APPLE-1008	U.S. Patent No. 5,291,076 to Jeffrey T. Bridges (“Bridges”)
APPLE-1009	Stephen Brown et al., <i>Fundamentals of Digital Logic with Verilog Design</i> , (McGraw Hill 2003) (“Brown”)
APPLE-1010	Declaration of Edward G. Faeth (Authentication of APPLE-1007 and APPLE-1009)
APPLE-1011	U.S. Patent No. 6,483,771 to Tae-jeen Shin (“Shin”)
APPLE-1012	U.S. Patent No. 5,602,796 to Kenichiro Sugio (“Sugio”)

Apple Inc., (“Petitioner” or “Apple”) petitions for Inter Partes Review (“IPR”) under 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42 of claims 1-28 and 31-37 (“the Challenged Claims”) of U.S. Patent No. 7,693,002 (“the ’002 patent”). As explained in this petition, there exists a reasonable likelihood that Apple will prevail with respect to at least one of the Challenged Claims.

The Challenged Claims are unpatentable based on teachings set forth in at least the references presented in this petition. Apple respectfully submits that an IPR should be instituted, and that the Challenged Claims should be canceled as unpatentable.

I. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Apple certifies that the ’002 Patent is available for IPR. The present petition is being filed within one year of service of a complaint against Apple in ITC investigation Mobile Electronic Devices and Radio Frequency and Processing Components (ITC-337-TA-1093); and Qualcomm Inc. v. Apple Inc., 3:17-CV-02398 (S.D. Cal.).

Apple is not barred or estopped from requesting this review challenging the Challenged Claims on the below-identified grounds.

B. Challenge Under 37 C.F.R. § 42.104(b) and Relief Requested

Petitioner requests IPR on the grounds in the table below, as explained herein

and in APPLE-1003, the Declaration of Dr. Robert Horst.

Ground	'002 Patent Claims	Basis for Rejection
Ground 1	1-28, 31-37	§103: Sato
Ground 2	1-17, 20-28, 31-36	§103: Asano in view of Itoh

Each reference qualifies as prior art to the 10/10/06 (“Critical date”).

Reference	Date	Section
Sato	8/21/1990 (issued)	§102(b)
Asano	11/5/2004 (filed)	§102(e)
Itoh	2001 (published)	§102(b)

C. LEVEL OF ORDINARY SKILL

The '002 patent is directed to decoding circuits for semiconductor memories. The patent specification and figures include CMOS circuits and memory system block diagrams. A person of ordinary skill in the art (“POSITA”) as of October 10, 2006 would have had at least an undergraduate degree in electrical engineering, or a related field, and three years of experience in the design of memory systems and circuits. APPLE-1003, ¶¶27-29. Alternatively, a person of ordinary skill with less than the amount of experience noted above would have had a correspondingly greater amount of educational training such a graduate degree in a related field. *See id.*

D. CLAIM CONSTRUCTION

Unless otherwise noted below, Petitioner submits that all terms should be given their plain meaning, but reserves the right to respond to any constructions that may later be offered by the Patent Owner or adopted by the Board. Petitioner is not waiving any arguments concerning indefiniteness or claim scope that may be raised in litigation.

1. “static precharge state”

Claims 18 and 37 recite: “**wherein other wordline drivers of the group of wordline drivers are in a static precharge state.**” The evidence most relevant to construction—*e.g.*, recitations in the specification and expert testimony concerning plain meaning—leads to a construction of the claim term “static precharge state” that includes a state in which a fixed voltage level is applied to a wordline driver. Specifically, when differentiating a “dynamic evaluation state” from a “static precharge state,” the ’002 patent specification states: “in a static precharge state (*e.g.*, a fixed voltage level, such [as] a voltage high signal, is applied).” APPLE-1001, 3:55-57;¹ *see also* 3:52-62; APPLE-1003, ¶¶43-44.

2. “conditional clock generator”

Claim 2 recites “**conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output.**” Claims

¹ All emphases added unless otherwise noted.

3, 9, 13, 20-22, 27, 31, 32, and 37 recite similar language. The evidence most relevant to construction—*e.g.*, recitations in the specification and expert testimony concerning plain meaning—leads to a construction of the claim term “conditional clock generator” that includes a circuit component that applies a clock signal to one of several output terminals, selectively. Specifically, the ’002 patent specification explains that a “conditional clock generator 110 receives a clock signal via the clock input 118 and selectively applies the clock signal to a selected one of the clock outputs 124, 126, 128 and 130.” APPLE-1001, 3:28-31. In some cases, a “conditional clock generator 110 may derive the clock outputs 124, 126, 128 and 130 from a single clock.” APPLE-1001, 3:34-36. Based on this description in the ’002 patent, a POSITA would have understood the conditional clock generator to operate by either directly applying an input clock signal to one of the outputs of the conditional clock generator, or by deriving an output clock signal based on an input clock signal and applying the derived output clock signal to one of the outputs of the conditional clock generator. APPLE-1001, 3:28-36, 5:31-34; APPLE-1003, ¶¶45-46. In other words, the output of the conditional clock generator could be a near exact reproduction of the input clock or simply derived based on the input clock. *Id.* The proposed construction of a “conditional clock generator” as a circuit component that applies a clock signal to one of several output terminals reasonably incorporates both of the ’002 patent’s descriptions of

the term. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (“claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art.”).

3. “means for decoding a first portion of a memory address of a memory array” (claim 11)

This term includes the phrase “means for,” which creates a presumption that the term is governed by §112 ¶6. *Williamson v. CitrixOnline, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015) (en banc).

The corresponding structure for “decoding a first portion of a memory address of a memory array” is described in the ’002 patent as a “decoder.” APPLE-1001, 3:9-28, 3:37-45, 3:62-4:8, 6:12-19, 9:45-52, 9:64-10:27, 11:19-21, 13:2-10; APPLE-1003, ¶¶47-48. Thus, the corresponding structure is a “decoder.” *Id.*

4. “means for selectively providing a clock signal to a selected group of wordline drivers based on the first portion of the memory address [of a memory array]” (claims 11 and 27)²

This term includes the phrase “means for,” which creates a presumption that the term is governed by §112 ¶6. *Williamson*, 792 F.3d at 1348.

The corresponding structure for “selectively providing a clock signal to a selected group of wordline drivers based on the first portion of the memory address

² Claim 27 includes “of a memory array.”

[of a memory array]” is described in the ’002 patent as a “conditional clock generator.” APPLE-1001, 3:9-36, 4:3-8, 5:31-34, 5:54-57, 6:8-19, 9:48-58, 10:27-32, 11:11-18, 12:4-10, 12:48-67; APPLE-1003, ¶¶49-50. Thus, the corresponding structure is a “conditional clock generator.” *Id.*

5. “means for decoding a second portion of the memory address” (claims 11 and 14)

This term is the same as the term “means for decoding a first portion of a memory address of a memory array,” except that the term replaces “first” with “second” and omits “of a memory array.” Thus, for reasons discussed above, the term is governed by §112 ¶6 and the corresponding structure is a “decoder.” APPLE-1003, ¶¶51-52.

6. “means for activating a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address” (claims 11 and 27)

This term includes the phrase “means for,” which creates a presumption that the term is governed by §112 ¶6. *Williamson*, 792 F.3d at 1348.

The corresponding structure for “activating a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address” is described in the ’002 patent as the four-to-sixteen decoder. APPLE-1001, 1:35-38, 3:18-25, 3:37-49, 3:62-4:8, 5:65-6:7, 9:40-44; APPLE-1003, ¶¶53-54. Thus, the corresponding structure is a “decoder.” *Id.*

7. “means for applying the second portion of the memory address to a shared address line” (claim 14)

This term includes the phrase “means for,” which creates a presumption that the term is governed by §112 ¶6. *Williamson*, 792 F.3d at 1348.

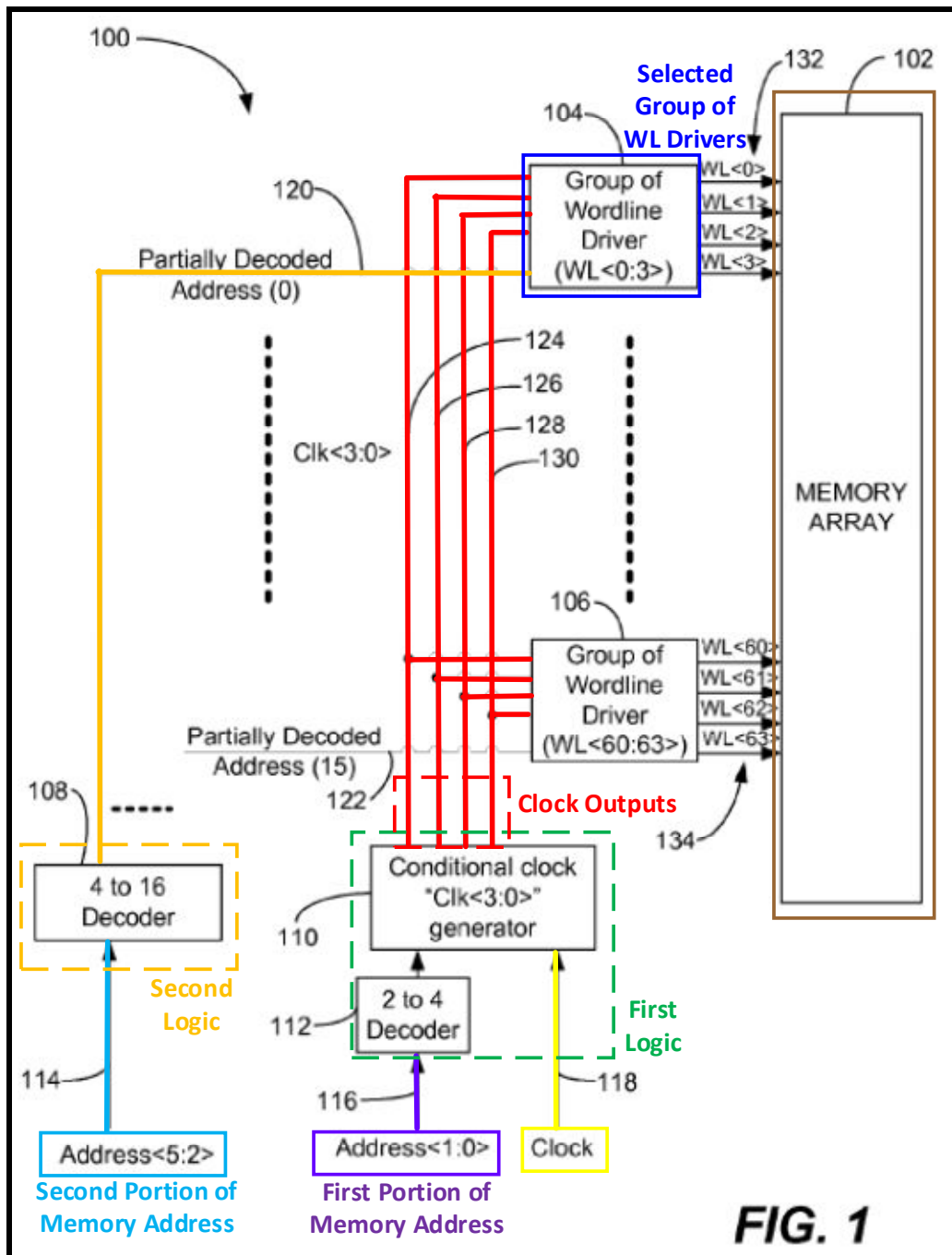
The corresponding structure for “applying the second portion of the memory address to a shared address line” is described in the ’002 patent as the four-to-sixteen decoder. APPLE-1001, 3:37-49, 3:62-67, 4:40-43, 10:32-37, 14:13-16; APPLE-1003, ¶¶55-56. Thus, the corresponding structure is a “decoder.” *Id.*

II. BACKGROUND

A. ’002 patent

The ’002 patent describes a “wordline driver system” for a “memory array.” APPLE-1001, 2:53-56, Figure 1 (below). The system separately decodes a “first portion” and a “second portion” of a memory address. APPLE-1001, 1:29-38. The “first logic” decodes the “first portion” of the memory address (e.g., the 2-to-4 decoder 112) and selectively provides a clock signal “to a selected group of wordline drivers based on a first portion of the memory address of the memory array” (e.g., conditional clock generator 110). APPLE-1001, 9:35-38; *see also* 1:29-35. This selective application of the clock signal is said to reduce “the clock driver’s capacitance loading” and “reduces power consumption.” APPLE-1001, 1:66-2:5. The “second logic” (e.g., 4-to-16 decoder 108) decodes the “second portion” of the memory address and “selectively activates a particular wordline

driver of the selected group of wordline drivers.” APPLE-1001, 1:35-37.



The '002 patent includes 38 claims, of which claim 1, 7, 11, 17, 21, 23-27 and 29 are independent.

B. Prosecution History

The '002 patent issued on April 6, 2010 from U.S. Patent Application No. 11/548,132 (“the '132 application”), which was filed on October 10, 2006 with 27 claims. *See* Ex. 1002. This application does not include a priority claim.

III. APPLICATION OF PRIOR ART TO CHALLENGED CLAIMS

Petitioner will prevail on the Challenged Claims.

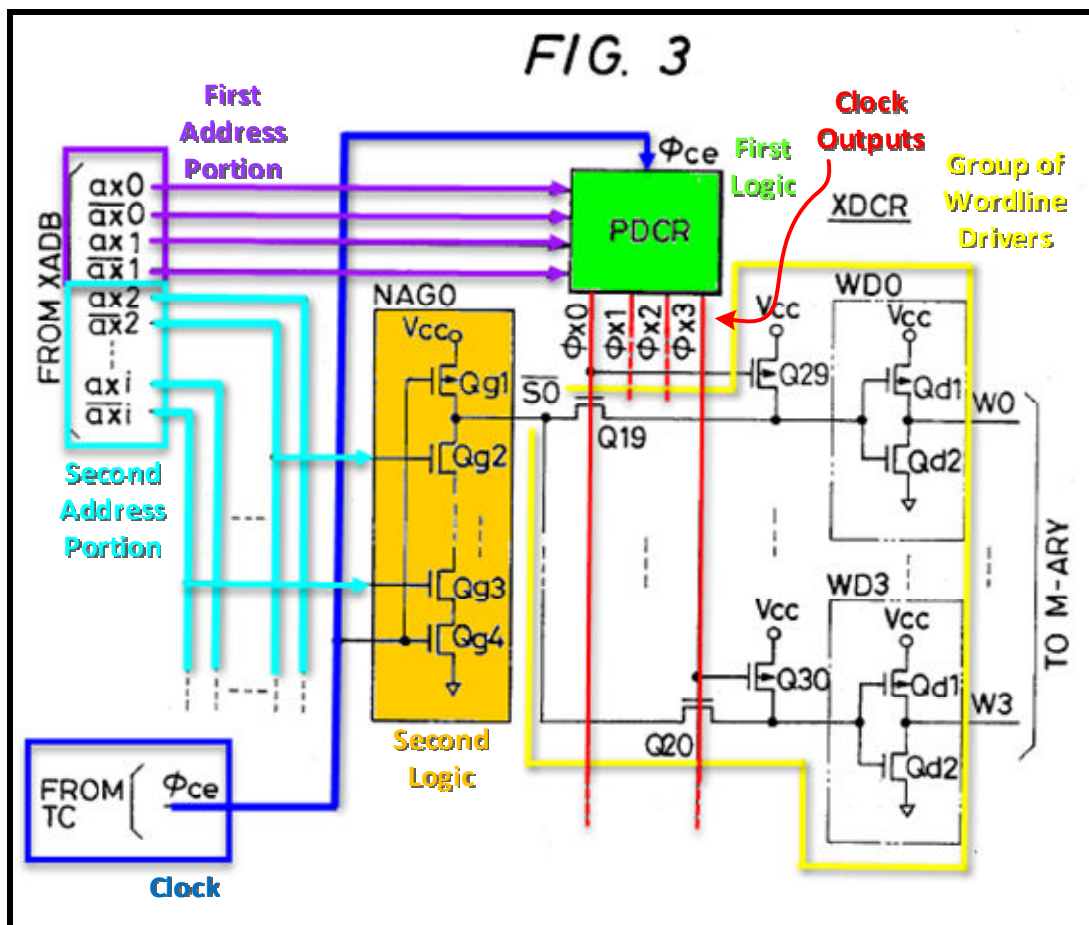
A. Claim 1 is Obvious Over Sato [GROUND-1]

A claim may be rendered unpatentable by a single reference if a POSITA would have been motivated to modify that reference in an obvious way. *SIBIA Neurosciences, Inc. v. Cadus Pharm. Corp.*, 225 F.3d 1349, 1356 (Fed. Cir. 2000). Notably, motivations to modify may be found implicitly in the prior art based on what the teachings of the art, a POSITA’s knowledge, and the nature of the problem to be solved would have suggested to a POSITA. *See In re Kahn*, 441 F.3d 977, 987-88 (Fed. Cir. 2006); *see also Cross Medical Prods., Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1322 (Fed. Cir. 2005) (motivation “equally can be found in the knowledge generally available to” a POSITA). The law credits a POSITA with ordinary creativity, and recognizes that the POSITA can draw upon both their knowledge and common sense to find motivation to make an obvious modification in view of disclosures in the art. *See also KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 420-21 (2007) (“Common sense teaches, however, that familiar items may have obvious uses beyond their primary purposes ... A

person of ordinary skill is also a person of ordinary creativity, not an automaton.”).

Overview of Sato³

Sato forms the basis of the Ground-1 in this Petition. As shown in Figure 3 below, Sato selectively applies a clock signal (ϕ_{ce}) to wordline drivers in a group of wordline drivers using a wordline decoder circuit (X address decoder XDCR) and separate logic circuitry (predecoder (PDCR)).



³ Petitioner hereby expressly incorporates the entirety of this Sato discussion into the element-by-element analysis of Ground 1, *infra*.

Sato, Figure 3 (annotated)

Similar to the conditional clock generator of the '002 patent, Sato's "PDCR decodes the lower 2-bit complementary internal address signals ax_0 and ax_1 . . . and generates selection signals $\phi_{x0}-\phi_{x3}$." APPLE-1005, 5:25-26. Sato explains in detail how "[t]hese selection signals $\phi_{x0}-\phi_{x3}$ are formed selectively in accordance with the complementary internal address signals ax_0 and ax_1 ." APPLE-1005, 5:28-31; *see also* 5:31-42. Furthermore, the timing signal ϕ_{ce} is also "supplied to the pre-decoder PDCR." APPLE-1005, 10:36-39. The PDCR "output signal, that is, the selection signal $\phi_{x0}-\phi_{x3}$, is generated in accordance with this timing signal ϕ_{ce} ." *Id.*

Furthermore, Sato's decoding NAND gate circuits are supplied with the remaining "complementary internal address signals ax_2-ax_i " similar to the '002 patent's four-to-sixteen decoder. APPLE-1005, 5:20-22. The decoding NAND gate circuits decode these remaining address signals to produce a selection signal (e.g., selection signal $\overline{S_0}$), which, along with one of the PDCR outputs, is used to activate one of the wordline drivers in each group of four drivers. APPLE-1005, 5:43-6:59; APPLE-1003, ¶57.

Claim 1–[1.0]: A circuit device comprising: first logic . . . and second logic . . .

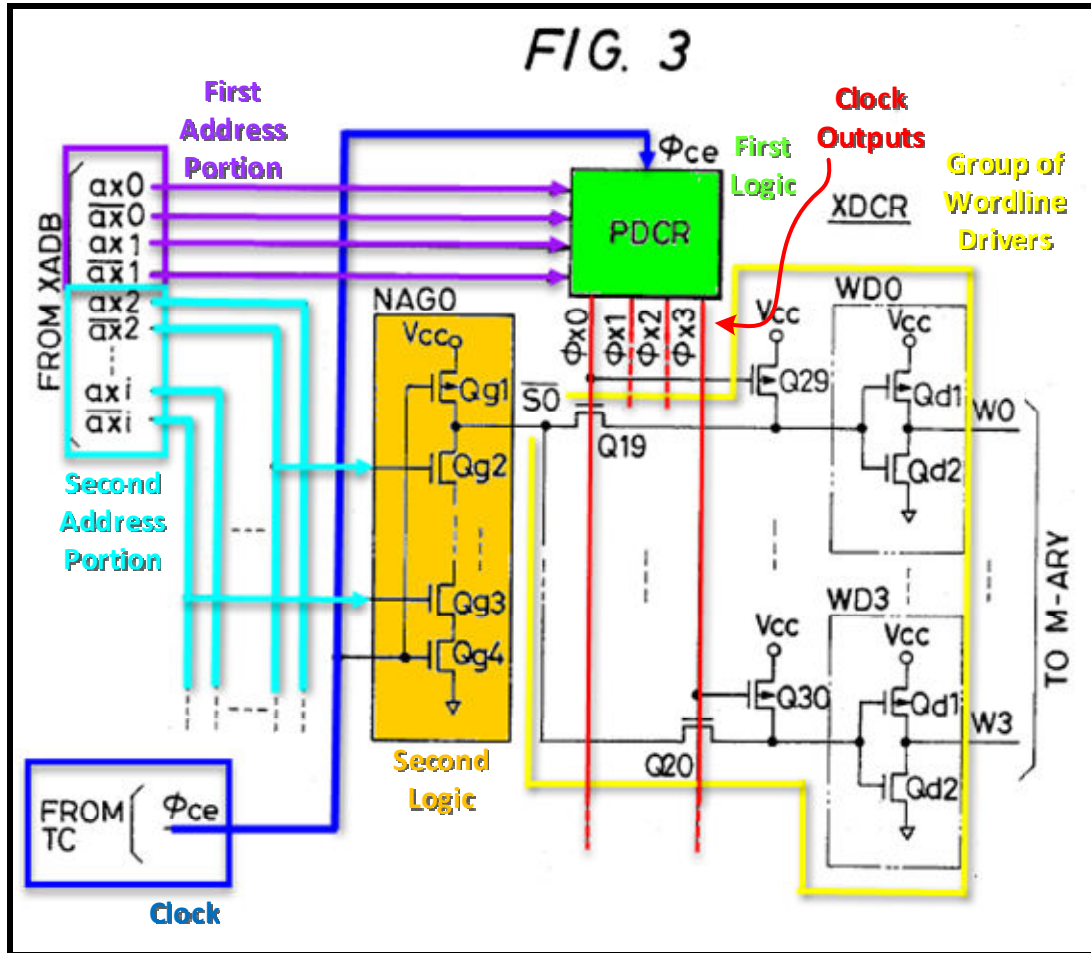
Sato discloses a "circuit device comprising: first logic . . . and second logic . . ." *See* APPLE-1005, Figure 3, 9:44-10:59, Claim 1. Specifically, Sato

discloses the details of an “X address decoder XCDR of [a] CMOS static RAM,” the circuit elements of which are “formed on one semiconductor substrate.”

APPLE-1005, 3:3-5, 9:31-32. Sato’s Figure 3 is “a circuit diagram” showing one embodiment of Sato’s “X address decoder of the static RAM.” APPLE-1005, 2:57-59. As recited in Sato’s first claim, the XCDR includes a “first logic decoding means coupled to receive a first group of address signals,” and “second logic decoding means coupled to receive another group of address signals.”

APPLE-1005, 12:49-50, 12:39-40. For example, in Figure 3 (below) “the X address decoder XDCR of the CMOS static RAM includes the pre-decoder PDCR [green-below] which receives the lower 2-bit complementary internal address signals ax0 and ax1[,] and k+1 decoding NAND gate circuits NAG0-NAGk [e.g., NAG0 depicted in orange below] to which the complementary internal address signals ax2-axi other than the lower two bits in respective combinations are supplied.” APPLE-1005, 5:16-22; *see also* 9:44-48. Accordingly, Sato’s PDCR and NAND gate circuits represent first and second logic of a circuit device.⁴

⁴ Sato’s reference to “first logic” and “second logic” in the claims is opposite to that of the ’002 patent solely on a labeling basis. Sato’s “second logic” performs functions equivalent to those performed by the ’002 patent’s “first logic” and



Sato's "first logic" performs functions equivalent to those performed by the '002 patent's "second logic."

[1.1]: [the first logic] to receive a clock signal and a first portion of a memory address of a memory array,

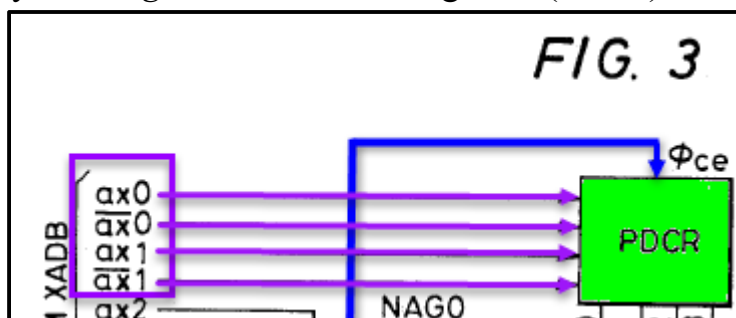
Sato discloses “first logic to receive a clock signal and a first portion of a memory address of a memory array” *See e.g.*, APPLE-1005, Figure 3 (below),

5:16-24, 9:44-54. Sato’s pre-

decoder PDCR (green)

represents the “first logic” as

recited in the ’002 patent’s



claims. The PDCR receives a timing signal ϕ_{ce} (blue line) and address signals $ax0$ and $ax1$ along with their complements (purple).

More specifically, the PDCR “receives the lower 2-bit complementary internal address signals $ax0$ and $ax1$,” i.e., signals $ax0$, $\overline{ax0}$, $ax1$, and $\overline{ax1}$. APPLE-1005, 5:16-19. The internal address signals represent externally supplied memory address signals, along with the complement of each address signal, for addressing memory cells in a memory array (M-ARY). *See* APPLE-1005, 3:9-15, 3:50-59. Sato explains, “[t]he X address buffer XADB receives the X address signals $AX0$ - AX_i supplied through external terminals $AX0$ - AX_i and generates the complementary internal address signals $\overline{ax0}$ - $\overline{ax_i}$ on the basis of these signals $AX0$ - AX_i and supplies them to the X address decoder XDCR.” APPLE-1005, 4:6-11.

Timing signal ϕ_{ce} represents or renders obvious a clock signal. APPLE-1003, ¶¶64-69. A POSITA would have “viewed the function of the timing signal

ϕ ce as similar to or equivalent to that of a clock signal because 1) “clock” is another name for a timing signal, 2) the Greek symbol phi (ϕ) is frequently used in the art to indicate clock signals, 3) this signal performs the same function as the clock signal in the '002 patent and 4) ϕ ce performs the same function as the clock signal in a clocked decoder such as that described by Bridges.” *Id.*, ¶64; APPLE-1005, 1:10-11, 12:4-6; APPLE-1001, 3:28-62; APPLE-1008, 3:1-4:24, Figure 1; APPLE-1011, 1:23-42. Indeed, even the examiner and Patent Owner recognized a timing signal as being equivalent to a clock signal during prosecution of the '002 patent. *See* APPLE-1002, 231 (9/11/2007 Office Action rejecting claims as anticipated by U.S. Patent 5,602,796 (“Sugio”) [APPLE-1012] and equating the claimed clock outputs with timing control signal outputs of Sugio’s timing control circuit 1.), *see also* 216-217 (Patent Owner’s response admitting that a “clock signal (CK) is used to drive all the wordline drivers” in Sugio through the timing control circuit 1.)(emphasis in original). Furthermore, Sato states that his invention “can be applied widely to semiconductor memory devices having at least a **clocked static type address decoder**” and that “CMOS static RAMs including **clocked static decoders** are known in the art,” which further corroborates Dr. Horst’s opinion. APPLE-1005, 1:10-11, 12:4-6; APPLE-1003, ¶64. In addition, Dr. Horst explains it would have been obvious to a POSITA that in order for Sato’s memory to operate properly, the timing signal must oscillate between subsequent

memory operations; otherwise, a selected wordline may not be properly reset.

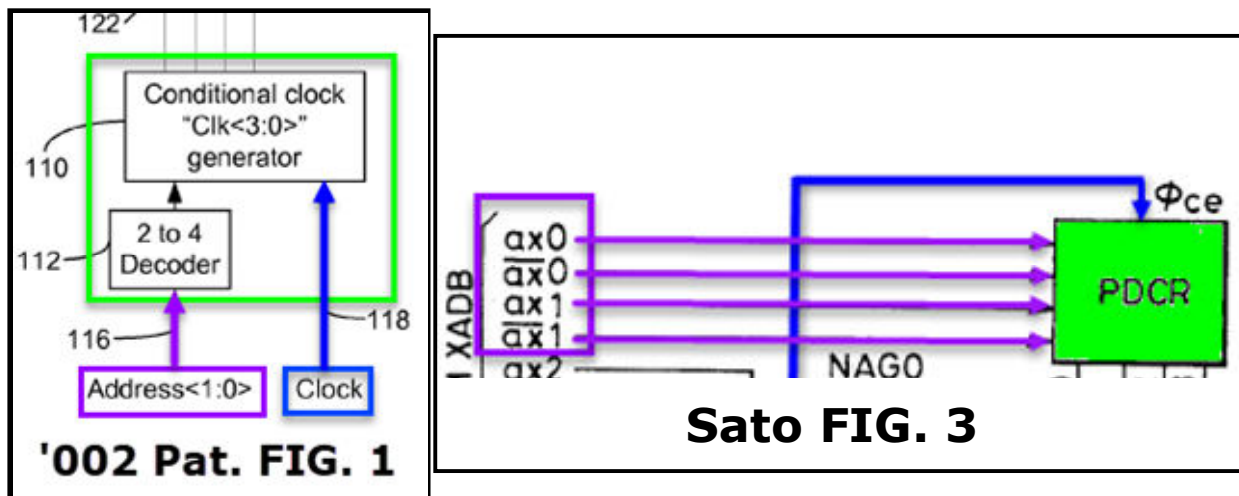
APPLE-1003, ¶¶68-69.

The function of the timing signal in Sato's PDCR as described in reference to Figure 3, is also similar to that of a prior art clocked decoder as disclosed in a patent to Bridges (APPLE-1008). APPLE-1003, ¶¶67-68; APPLE-1008, 3:1-4:24, Figure 1. Indeed, Dr. Horst demonstrates that a POSITA would have recognized the operational similarity between Bridge's clocked decoder and Sato's PDCR. *Id.* In view of the apparent similarity, Horst explains that a POSITA would have concluded that Sato's timing signal provides a comparable function for the PDCR as a clock signal does for a clocking clocked decoder. *Id.* Dr. Horst also notes that Sato's timing signal provides a comparable function as the clock 118 signal of the '002 patent. *Id.*, ¶¶65-66. Consequently, the POSITA would have reasonably viewed Sato's timing signal as disclosing or rendering obvious a clock signal.

In addition, various portions of Sato's disclosure describe ϕ_{ce} as a timing signal. APPLE-1005, 1:10-11, 3:59-4:2, 4:22-32, 5:7-12, 5:43-6:21, 6:60-7:30, 9:44-10:55, 12:4-6. Although Sato includes an obscure statement suggesting that the timing signal could be kept at a high level, in contrast, a POSTIA would not have read this statement as one embodiment, distinct of other aspects described within the Sato disclosure. *See* APPLE-1005, 3:59-65. As Dr. Horst explains, a POSITA would have understood that the Sato system would perform poorly or

malfunction if the timing signal in Sato were kept at a high level throughout operation. APPLE-1003, ¶¶68-69. Thus, in the context of Sato's disclosure, a POSITA would reasonably have understood that ϕ_{ce} would be kept high at most for only a portion of a memory operation.

In addition, Sato's PDCR corresponds to the '002 patent's conditional clock generator 110 and 2 to 4 decoder 112 of the '002 patent. *Id.*, ¶84. For example, compare Figure 1 of the '002 patent with Figure 3 of Sato (both reproduced below). Like the first logic in the '002 patent (conditional clock generator 110 and decoder 112-green outline) Sato's PDCR (green) receives both a clock signal (blue) and a first portion of a memory address (purple). APPLE-1001, Figure 1, 3:18-36; APPLE-1003, ¶¶65-66.



Thus, Sato discloses this limitation or at least renders it obvious.

**[1.2]: the first logic to decode the first portion of the memory address
and**

Sato discloses “the first logic to decode the first portion of the memory address.” *See* APPLE-1005, Figure 3, 5:25-31, 9:44-48, 11:54-56, Claim 1.

Drawing on this disclosure, Sato’s claim 1 recites, and thus, further discloses “logic decoding means coupled to receive a . . . group of address signals.”

APPLE-1005, Claim 1. Second, Sato describes, in reference to Figure 1, that the “PDCR decodes the lower 2-bit complementary internal address signals.” APPLE-1005, 5:25-26. The PDCR operates similarly in the embodiment shown in Figure 3. *See* APPLE-1005, 9:30-48 (“In FIG. 3, the X address decoder XDCR . . . of this embodiment includes one pre-decoder PDCR and k+1 decoding NAND gate circuits NAG0~NAGk in the same way as in the foregoing embodiments.”). Thus, Sato’s first logic (PDCR) decodes the first portion of the memory address.

APPLE-1003, ¶70.

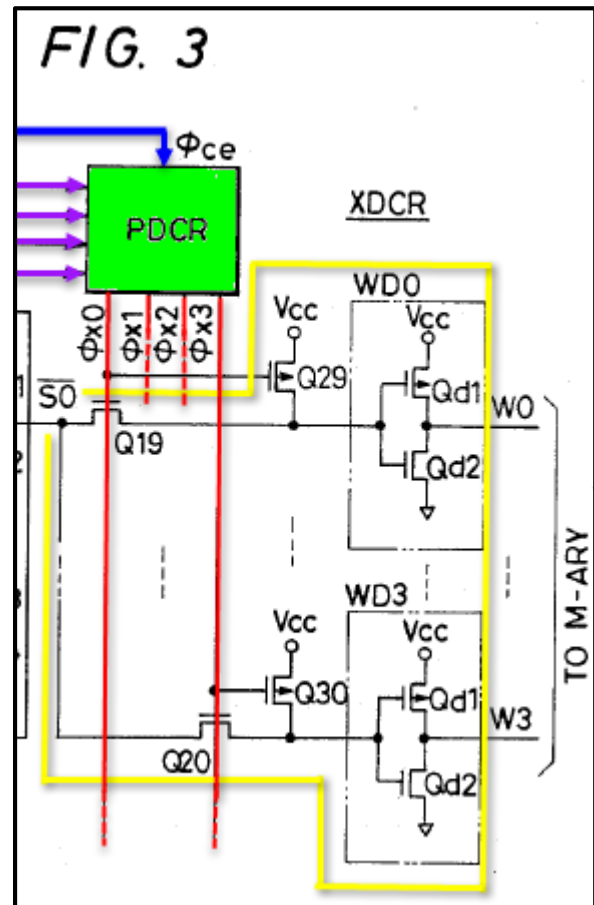
[1.3]: [the first logic . . .] to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array;

Sato renders obvious that the PDCR “appl[ies] the clock signal to a selected clock output of a plurality of clock out-puts associated with a selected group of a plurality of wordline drivers that are associated with the memory array.” *See* APPLE-1005, Figure 3 (below), 5:25-31, 6:40-55, 9:30-51, 9:52-65, 10:36-39, Claim 1.

First, Sato mimics disclosure within the '002 patent and, as such, provides disclosure that would have rendered obvious to a POSITA what is claimed by the '002 patent with respect to the application of a timing signal by the first logic to its output. APPLE-1003, ¶¶14, 65-72. For instance, the PDCR applies a clock signal to one of a plurality of outputs similar to the conditional clock generator 110 of the '002 patent. *Id.* For example, compare the Figure 1 of the '002 patent with Figure 3 of Sato (both reproduced below). Like the conditional clock generator 110 (green outline) in the '002 patent, the PDCR (green) applies the clock signal (blue) to one of four outputs (red) according to the first portion of the memory address (purple). *Compare* APPLE-1001, 3:26-36 *with* APPLE-1005, 5:25-31, 10:36-39; *see also* APPLE-1003, ¶¶14, 65-72.

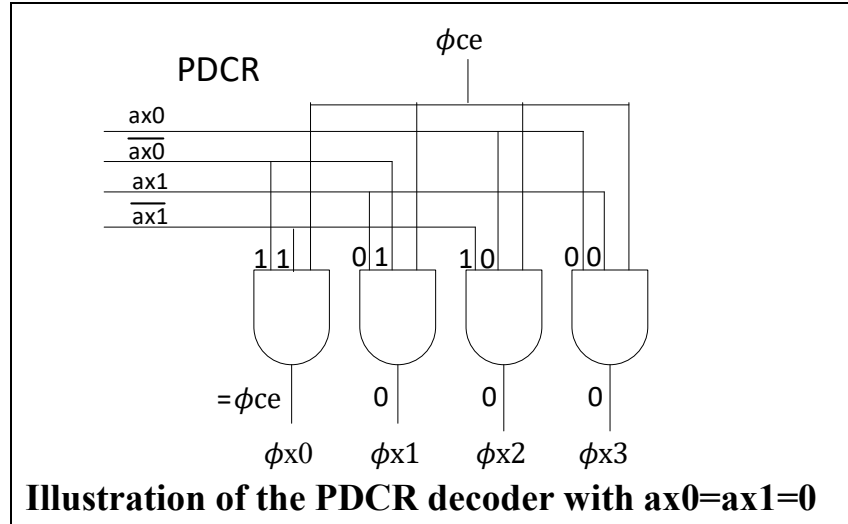


Next, Sato discloses or renders obvious to a POSITA that the PDCR (green) applies ϕ_{ce} to one of the four outputs (red lines) associated with selection signals ϕ_{x0} - ϕ_{x3} . For instance, with reference to the third embodiment, in describing the PDCR's output signal, Sato states, "the selection signal ϕ_{x0} - ϕ_{x3} , is generated in accordance with [the] timing signal ϕ_{ce} ." APPLE-1005, 10:36-39. The PDCR selects a particular one of the outputs "in accordance with the complementary internal address signals $ax0$ and $ax1$." APPLE-1005, 5:29-31; *see also* 5:31-42. The PDCR then *applies* the timing signal ϕ_{ce} to the selected output by generating the selection signal "in accordance with this timing signal ϕ_{ce} ." APPLE-1005, 10:39. In the third embodiment, when the "timing signal ϕ_{ce} is set to the high logic level . . . the output signal of the pre-decoder PDCR, that is, the selection signal ϕ_{x0} - ϕ_{x3} , is set selectively to the high logic level." APPLE-1005, 9:56-59.



Furthermore, Dr. Horst explains that a POSITA would have understood Sato's PDCR as applying the input clock signal (ϕ_{ce}) to one of the four clock

outputs based on the values of address bits ax0 and ax1. APPLE-1003, ¶¶14, 60-63, 71-72. Dr. Horst demonstrates by reference to an illustration of what a POSITA would have understood to be an accurate depiction of the internal logic of Sato's PDCR (right), such that the "outputs $\phi x0$ - $\phi x3$ follow[] the same low-to-high and high-to-low transitions as the input clock signal ϕce ." APPLE-1003,



¶71; *see also* APPLE-1009, 314-315, Figure 6.16. Dr. Horst continues:

Th[is] illustration shows that [when the input address is 00], $\phi x1$ - $\phi x3$ are forced low because at least one input of those AND gates is low, and $\phi x0$ will adopt the same state as input clock ϕce because the other two inputs of it's AND gate are high. In other words, in the 00 case, output $\phi x0$ will be low when the input clock ϕce is low, and will be high when input clock ϕce is high. Similarly, with the other three combinations of the two address lines, the input clock is *applied* to the corresponding output clock when that output is selected. . . . Thus, the logic acts to *apply the clock signal to a selected clock output*.

APPLE-1003, ¶72. Thus, it would have been obvious to a POSITA that Sato's PDCR could reasonably be considered to apply an input clock signal

(timing signal ϕ_{ce}) to one of the selection signal ϕ_{x0} - ϕ_{x3} outputs in accordance with the lower 2-bits of a memory address. *See Cross Medical*, 424. F.3d at 1322.

Second, as illustrated in Sato's Figure 3 (above), the selection signal ϕ_{x0} - ϕ_{x3} outputs (red) are associated with a group (yellow outline) of four wordline drivers (e.g., wordline drive circuits WD0-WD3 along with precharge transistors Q19~Q20 and reset transistors Q29~Q30). *See APPLE-1005*, 6:40-55, 7:32-36. Each wordline driver has a "capacitance cut MOSFET" (Q19-Q20) that is controlled by a corresponding one of the selection signals ϕ_{x0} - ϕ_{x3} from the PDCR. *APPLE-1005*, 9:60-62. Each wordline driver (WD0-WD3)⁵ is itself associated with a corresponding wordline (W0-W3) of the memory array M-ARY. *APPLE-1003*, ¶¶58, 76-78.

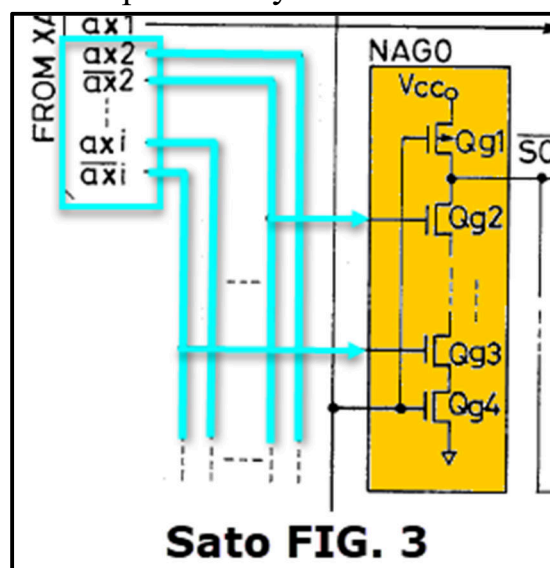
Thus, a POSITA would have found this limitation obvious in view of Sato's disclosure.

⁵ For simplicity Sato's wordline drivers are referred to by (WD0-WD3) throughout to avoid repeating the combination of Sato's wordline drive circuits WD0-WD3, precharge transistors Q19~Q20, and reset transistors Q29~Q30.

[1.4]: [the second logic] to decode a second portion of the memory address,

Sato discloses “second logic to decode a second portion of the memory address.” *See e.g.*, APPLE-1005, Figure 1, Figure 3 (below), 5:16-24, 5:43-6:21, 9:44-54, Claim 1. Sato’s claim 1 recites and therefore explicitly discloses “logic decoding means coupled to receive a . . . group of address signals, and including means for providing an output signal at an output terminal in accordance with said . . . group of address signals.” APPLE-1005, Claim 1.

Sato’s corresponding decoding NAND gate circuit (orange) renders obvious the “second logic” recited in the ’002 patent claims, as they decode the second portion of the memory address (light blue). The XDCR includes “k+1 decoding NAND gate circuits NAG0-NAGk to which the complementary internal address signals ax2-axi other than the lower two bits . . . are supplied.” APPLE-1005, 5:19-22; *see also* 9:44-48 (explaining that the “k+1 decoding NAND gate circuits NAG0-NAGk” in the third embodiment operate “in the same way as in the foregoing embodiments.”).



Sato further explains that “the inversed internal address signals $\overline{ax2}$ - $\overline{ax1}$ are all applied to . . . the NAND gate circuit NAG0 and the non-inversed internal

address signals ax_2 - ax_i are all supplied to . . . the NAND gate circuit NAG_k .”

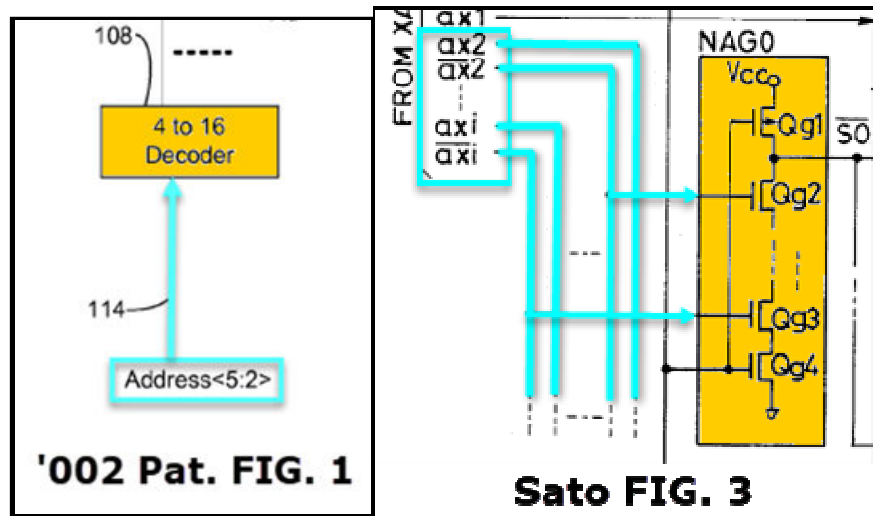
APPLE-1005, 5:53-58, Figure 1. The decoding NAND gate circuits generate an output selection signal (e.g., signals $\overline{S_0}$ - $\overline{S_k}$) according to the complementary address signals ax_2 - ax_i , which is a second portion of the memory address.

APPLE-1005, 5:66-6:21; APPLE-1003, ¶79. For example, Sato describes that “the output signal of the NAND gate circuit NAG_0 ” is asserted “when all the inversed internal address signals $\overline{ax_2}$ - $\overline{ax_i}$ are at the high logic level.” APPLE-1005, 5:66-6:4. “In other words, the selection signal $\overline{S_0}$ is at the low logic level when . . . any one of the word lines W_0 through W_3 is designated by the X address signal AX_0 - AX_i .”⁶ APPLE-1005, 6:4-8. Sato continues its description, stating “The output signals of the NAND gate circuits NAG_1 - NAG_{k-1} , that is, the inversed selection signals $\overline{S_1}$ - $\overline{S_k} - 1$, which are not shown in the drawing, are generated by the same logic as described above.” APPLE-1005, 6:17-21. Thus, together all of the $k+1$ decoding NAND gate circuits receive and decode a second portion of the memory address (ax_2 - ax_i). APPLE-1003, ¶79.

⁶ Petitioner notes that Sato uses capital letters to refer to the address signals AX_0 - AX_i as received from an external circuit and lowercase letter to refer to the same signals as used internally within Sato’s memory decoder. *See e.g.*, APPLE-1005, 3:65-4:11.

Moreover, the decoding NAND gate circuits decode a second portion of the memory address similar to the four-to-sixteen decoder 108 of the '002 patent. For example, compare the Figure 1 of the '002 patent with Figure 3 of Sato (both reproduced below). Like the four-to-sixteen decoder 108 (orange) in the '002 patent, each of the decoding NAND gate circuit (orange) decodes a combination of the input signals (the

second portion of the memory address-light blue). Compare APPLE-1001, 3:62-67 with APPLE-1005, 5:66-6:21; see also



APPLE-1003, ¶79. Specifically, the '002 patent states that if “the four-to-sixteen memory address decoder 108 decodes a portion (e.g. bits two to five) of the memory address to determine a set of wordlines from zero to three (WL<0>, WL<1>, WL<2> and WL<3> in FIG. 1), the four-to-sixteen bit memory address decoder 108 applies a signal to the address line 120.” APPLE-1001, 3:62-67. Sato’s decoding NAND gate circuits operate similarly. APPLE-1003, ¶79. For example, in the case where Sato uses a six-bit address, two address signals are used by the PDCR to select the clock signal output line and a different combination of

the remaining four signals (e.g., address bits ax2-ax5) are connected to one of the sixteen NAND gate circuits, thus, implementing a four-to-sixteen decoder comparable to the decoder 108 in the '002 patent's Figure 1. APPLE-1003, ¶79; APPLE-1005, 5:66-6:21. Sato's decoding NAND gate circuits apply "the selection signal $\overline{S0}$ " when "any one of the word lines W0 through W3 is designated by the X address signal AX0-AXi." APPLE-1005, 6:4-8.

Thus, Sato discloses or renders this limitation obvious.

[1.5]: the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

Sato discloses "second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address." *See e.g.*, APPLE-1005, Figure 3, 5:66-6:21, 6:40-44, 8:27-32, 9:60-10:13, 10:36-39, Claim 1. Sato's claim 1 recites and therefore explicitly discloses "[second] logic decoding means coupled to receive a first group of address signals, and including means for providing an output signal at an output terminal in accordance with said first group of address signals" and "selectively connect[ing] the output terminal of said [second] logic decoding means to one of

the input terminals of said first word line driver and said second word line driver.”

APPLE-1005, Claim 1.⁷

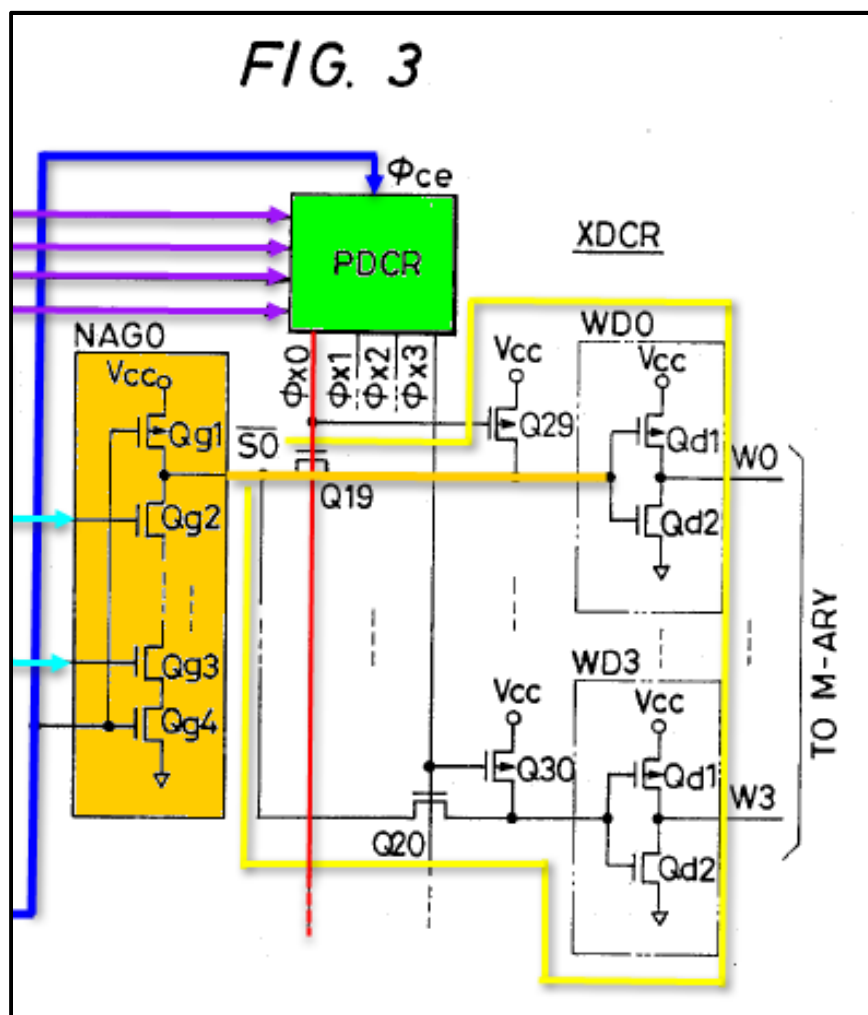
Sato further describes that “[t]he pre-decoder PDCR [first logic], the decoding NAND gate circuit NAG0 [second logic], the word line drive circuits WD0~WD3 and the capacitance cut MOSFETs [Q19-Q18 in Figure 3] perform the same selection operation as that of the first embodiment and bring one word line designated by the X address signal AX0-AXi to the high level selection state.”

APPLE-1005, 8:27-32, 9:31-51. In more detail and as shown in Sato’s Figure 3 (below), the selection signal $\overline{S0}$ generated by the decoding NAND gate circuit NAG0 (orange) is “supplied to the corresponding four sets of word line drive circuits WD0-WD3” through “corresponding capacitance cut MOSFETs” Q19-Q20. APPLE-1005, 6:40-44, 9:60. The decoding NAND gate circuit generates the selection signal $\overline{S0}$ according to the second portion of the memory address.

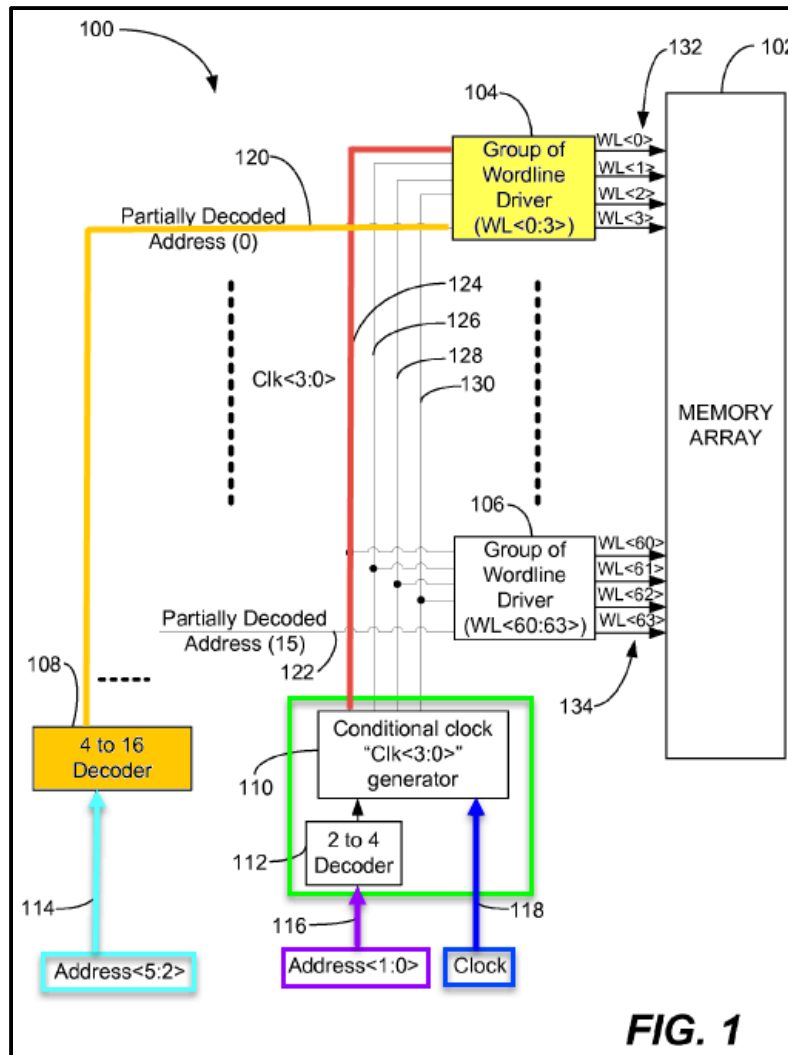
APPLE-1005, 5:66-6:21, APPLE-1003, ¶¶81-82. When an X address signal Ax0-Axi corresponding to a particular wordline (e.g., wordline WO) is supplied, PDCR (green) supplies the timing signal ϕ_{ce} to selection signal ϕ_{x0} (red line) turning capacitance cut MOSFET Q19 on, while the other capacitance cut MOSFETs

⁷ See FN-1 regarding Sato’s use of “first” and “second” logic in comparison to the ’002 patent claims.

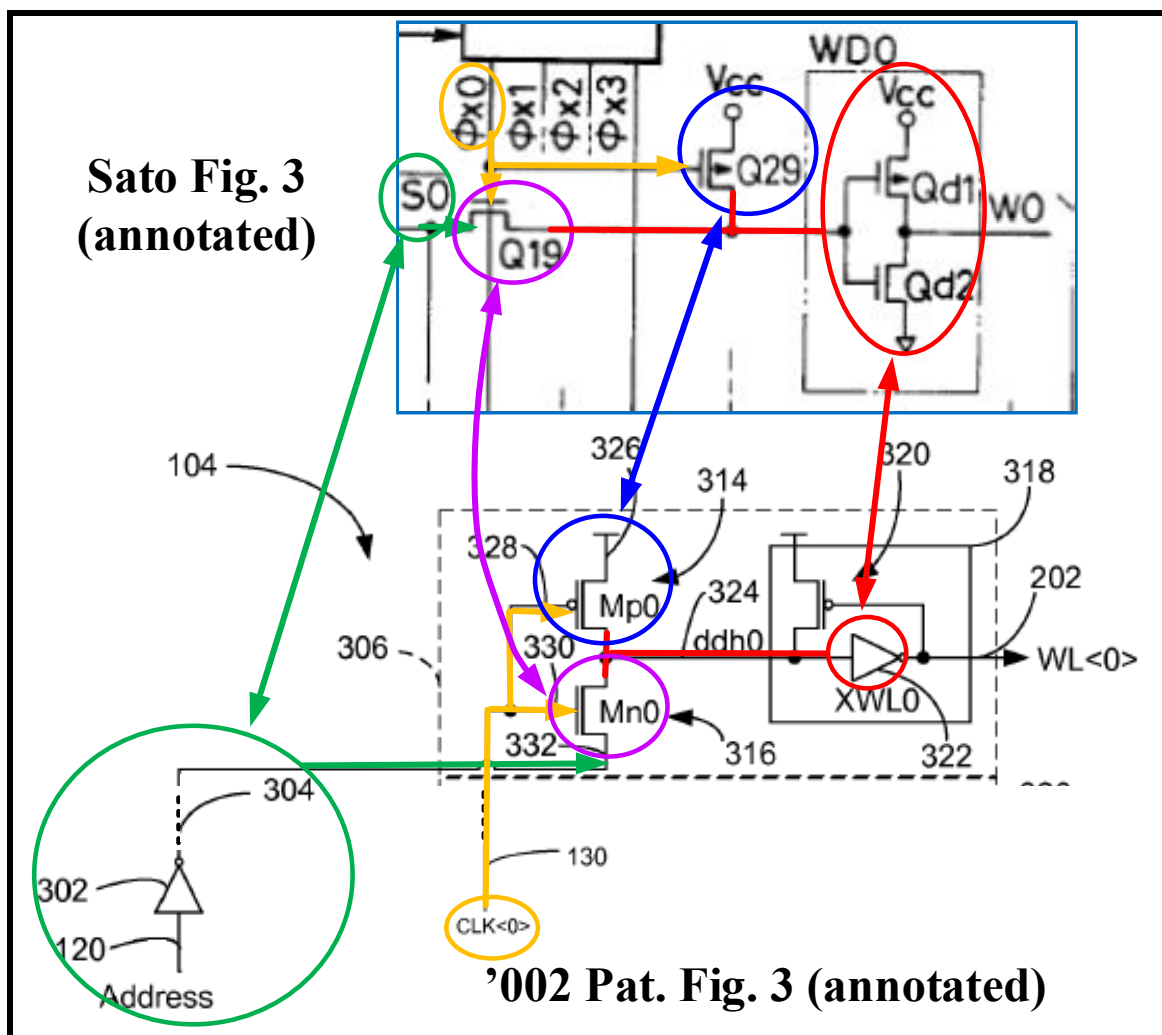
remain off. APPLE-1003, ¶105; *see also* APPLE-1005, 6:40-59, 9:60-10:13, 10:36-39. Consequently, the selection signal $\overline{S0}$ (orange line) of NAND gate circuit NAG0 (e.g., the second logic) “is transmitted to only the wordline drive circuit corresponding to one word line that is designated by the X address signal A_{x0} - A_{xi} ,” e.g., wordline drive circuit WD0 of the group of wordline drivers indicated by the yellow outline. APPLE-1005, 6:55-59; APPLE-1003, ¶¶82-83, 105.



As Dr. Horst explains, Sato's operations resemble and render obvious those of the '002 patent in view of the wordline driver activation operations described by the '002 patent itself. APPLE-1003, ¶¶11-12, 19-21, 81-83. For example, in reference to Figure 1 (below), the '002 patent explains that "the four-to-sixteen bit memory address decoder 108 [orange] decodes the remainder of the six-bit memory address (e.g. bits two to five) and applies a partial address input to the wordlines that are related to the decoded memory address. For example, the decoded four bits of the partially decoded address may be applied to the partially decoded address line (0) 120 [orange line] to enable the group of wordline drivers 104 [yellow] to enable one of the four wordlines (WL<0:3>) 132 to access data stored in the memory array 102." '002 patent, 3:37-45; APPLE-1003, ¶11. The '002 patent continues: "If the four-to-sixteen memory address decoder 108 decodes a portion (e.g. bits two to five) of the memory address to determine a set of wordlines from zero to three (WL<0>, WL<1>, WL<2> and WL<3> in FIG. 1), the four-to-sixteen bit memory address decoder 108 applies a signal to the address line 120." APPLE-1001, 3:62-67. Dr. Horst even demonstrates by comparing Sato's Figure 3 with the Figure 3 from the '002 patent



that “even Sato’s wordline driver activation circuitry is nearly identical to that of the ’002 patent.” APPLE-1003, ¶83. For example, Dr. Horst demonstrates that the transistor configuration of Sato’s wordline driver circuitry is a rearranged version of the wordline driver transistors shown in Figure 3 of the ’002 patent (see Dr. Horst’s annotated figure reproduced below). *Id.*



Thus, Sato discloses this limitation.

B. Claim 1 is Obvious Over Asano in view of Itoh [GROUND-2]

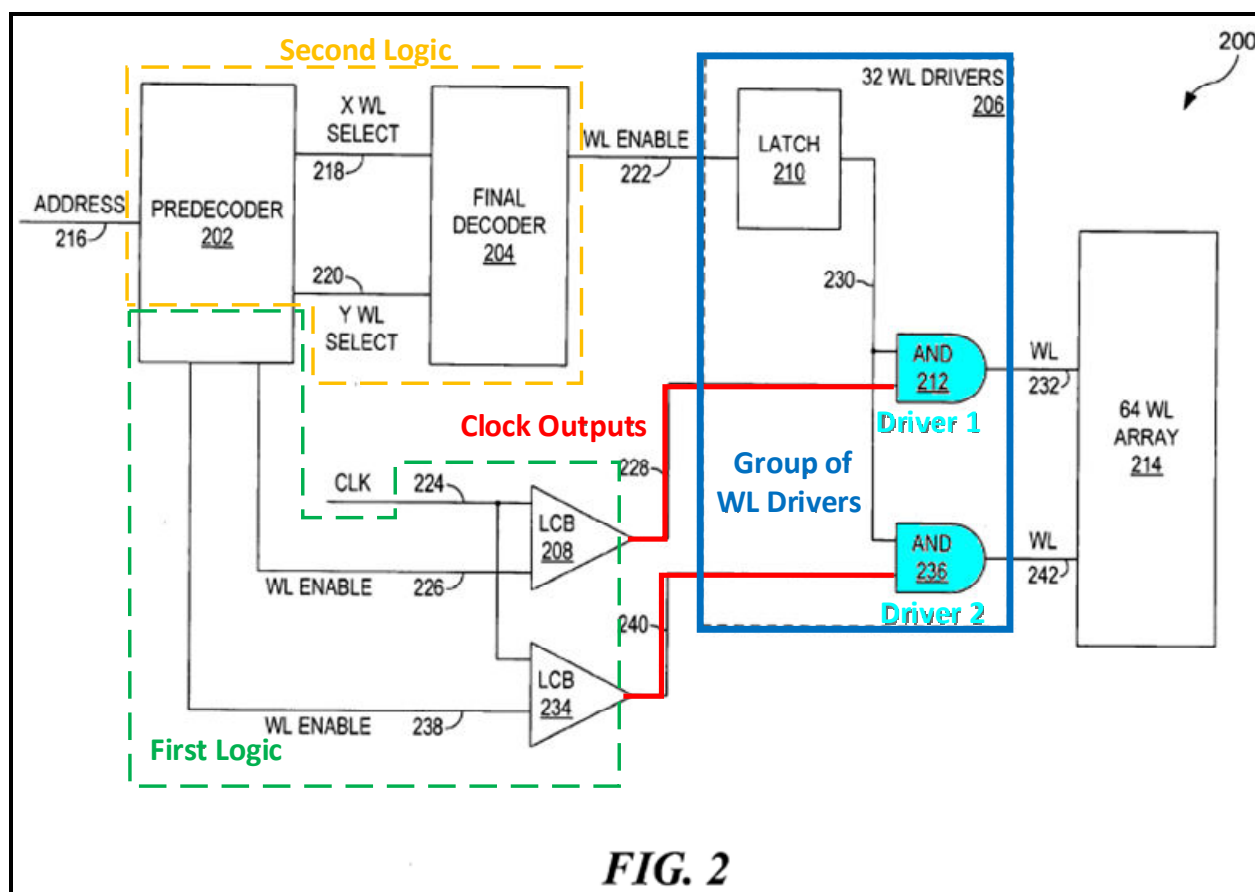
Overview of Asano⁸

Asano forms is the base reference of Ground-2 of this Petition. As shown below, Asano describes a “wordline driver method [and] apparatus” that selectively applies a clock signal to wordline drivers in a group of wordline drivers of a memory array. APPLE-1006, [0008]. Asano’s predecoder 202 and final decoder 204 decode 5 out of 6 address bits to generate “wordline enable signals.” APPLE-1006, [0016]-[0017]. “The wordline enable signals are communicated to the wordline drivers 206 through a fourth communication channel 222” to enable one of the wordline drivers. APPLE-1006, [0017].

Asano’s predecoder 202 also decodes “the most significant address bit of the address signal” to generate selection signals for the LCBs 208 and 234. APPLE-1006, [0018], [0019]. Asano explains that a “selection signal for the first LCB 208 and for the second LCB 234 are provided by the predecoder 202 through an eighth communication channel 226 and a ninth communication channel 238, respectively.” Further, the “first LCB 208 and the second LCB 234 also provide clocking signals to the wordline drivers 206” “based on two inputs, a clock input

⁸ Petitioner hereby expressly incorporates the entirety of this Asano discussion into the element-by-element analysis of Ground 2, *infra*.

and [the] select[ion] signal” from the predecoder 202. APPLE-1006, [0017]-[0018]. The LCBs effectively select an output to which to direct the clock signal. APPLE-1006, Claim 7 (“each LCB of the plurality of . . . LCBs is at least configured to propagate clocking signals if enabled”), *see also* claim 11. Asano describes that a wordline driver is enabled and a “wordline signal” is output “to a wordline within the 64 wordline array” when “the clocking signal [from the enabled LCB] is ANDed with” an enable signal from the final decoder (WL ENABLE line 222).” APPLE-1006, [0019]; APPLE-1003, ¶¶11, 119.



Asano, Figure 2 (annotated)

Overview of Itoh and its Integration with Asano

Itoh combines with Asano to provide the internal circuitry for Asano's predecoder. Itoh is a memory chip design textbook that provides details about decoding circuits, predecoding circuits and wordline drivers. Itoh illustrates the circuit design of several predecoder circuits, e.g., 3:8 predecoder and 2:4 predecoder circuits, which a POSITA would have readily applied if seeking to implement Asano's predecoder 202. APPLE-1007, 144-147; APPLE-1003, ¶122.

Specifically, Itoh discloses well-known circuits that illustrate a possible implementation of the internal structure for the predecoder 202. APPLE-1003, ¶¶121-122. Because Asano represents the predecoder 202 simply using a block element in a block diagram, a POSITA would have looked to Itoh's textbook circuits in determining how the internal structure of the predecoder 202 would be built as separate logic sections for decoding different portions of the 6-bit memory address. A POSITA designing Asano's memory circuit would have naturally turned to a textbook such as Itoh's for details on memory design techniques for a predecoder. APPLE-1003, ¶121. The POSITA would have understood that Itoh's individual predecoder circuits would merely perform their intended functions when implemented in Asano's predecoder 202. APPLE-1003, ¶¶121-123.

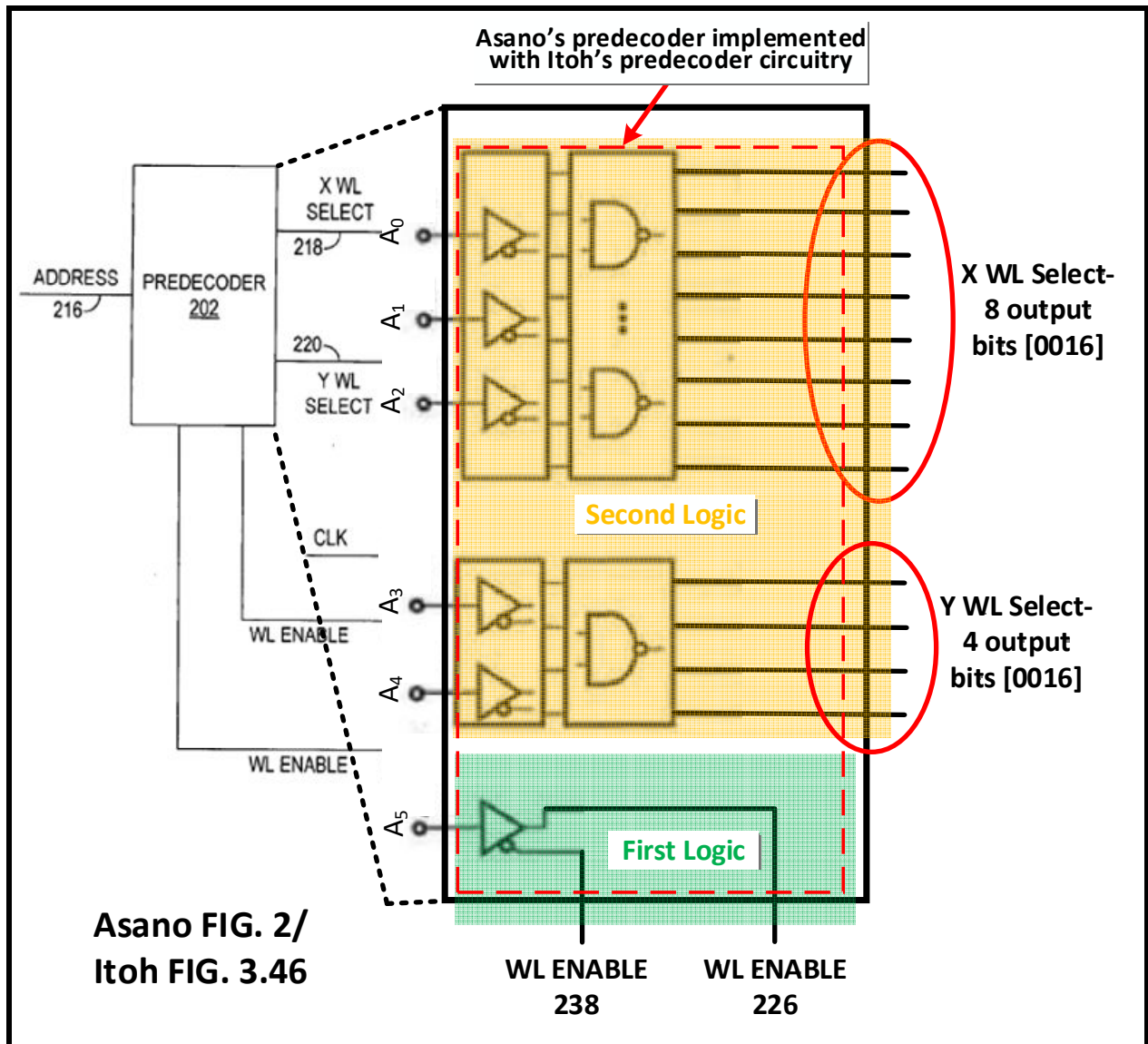
Claim 1–[1.0]: A circuit device comprising: first logic . . . and second logic . . .

Asano discloses a “circuit device comprising: first logic . . . and second logic . . .” *See* APPLE-1006, Figure 2, Abstract, [0001], [0008], [0014], [0016], [0019]-[0021]; APPLE-1003, ¶¶107-119, 131; *see also* overview of Asano, *supra*. Asano discloses a “wordline (WL) driver method, apparatus, and computer program for reducing required latches in a WL decode path” that can be implemented with “integrated circuits.” APPLE-1006, [0008], [0014]. Asano’s memory 200, illustrated in Figure 2 (below), includes a predecoder 202, a final decoder 204, and a set of local clock buffers (LCBs 208/234) that decode a memory address to select a wordline (WL) of the wordline array 214 for a computer memory. APPLE-1006, [0015]-[0019].

Asano’s predecoder and LCBs together represent the “first logic” (outlined in green) and the predecoder together with the final decoder represent the “second logic” (outlined in yellow). Asano explains that the predecoder receives a six-bit memory address. From “those 6 bits, the predecoder derives a wordline enable signal and two wordline select signals.” APPLE-1006, [0016]. Of those six bits, the predecoder uses one bit (the most significant bit) to generate LCB selection signals (WL ENABLE 226/238) “for LCB selections” and the remaining five bits to generate X WL SELECT and Y WL SELECT signals. APPLE-1006, [0016], [0019], [0021]; APPLE-1003, ¶¶110-111, 115. As explained in more detail below,

it would have been obvious to a POSITA that Asano's predecoder should include circuitry to decode the most significant address bit to produce the LCB selection signals and circuitry to separately decode the remaining five address bits to produce the X and Y WL SELECT signals. APPLE-1003, ¶¶108-116.

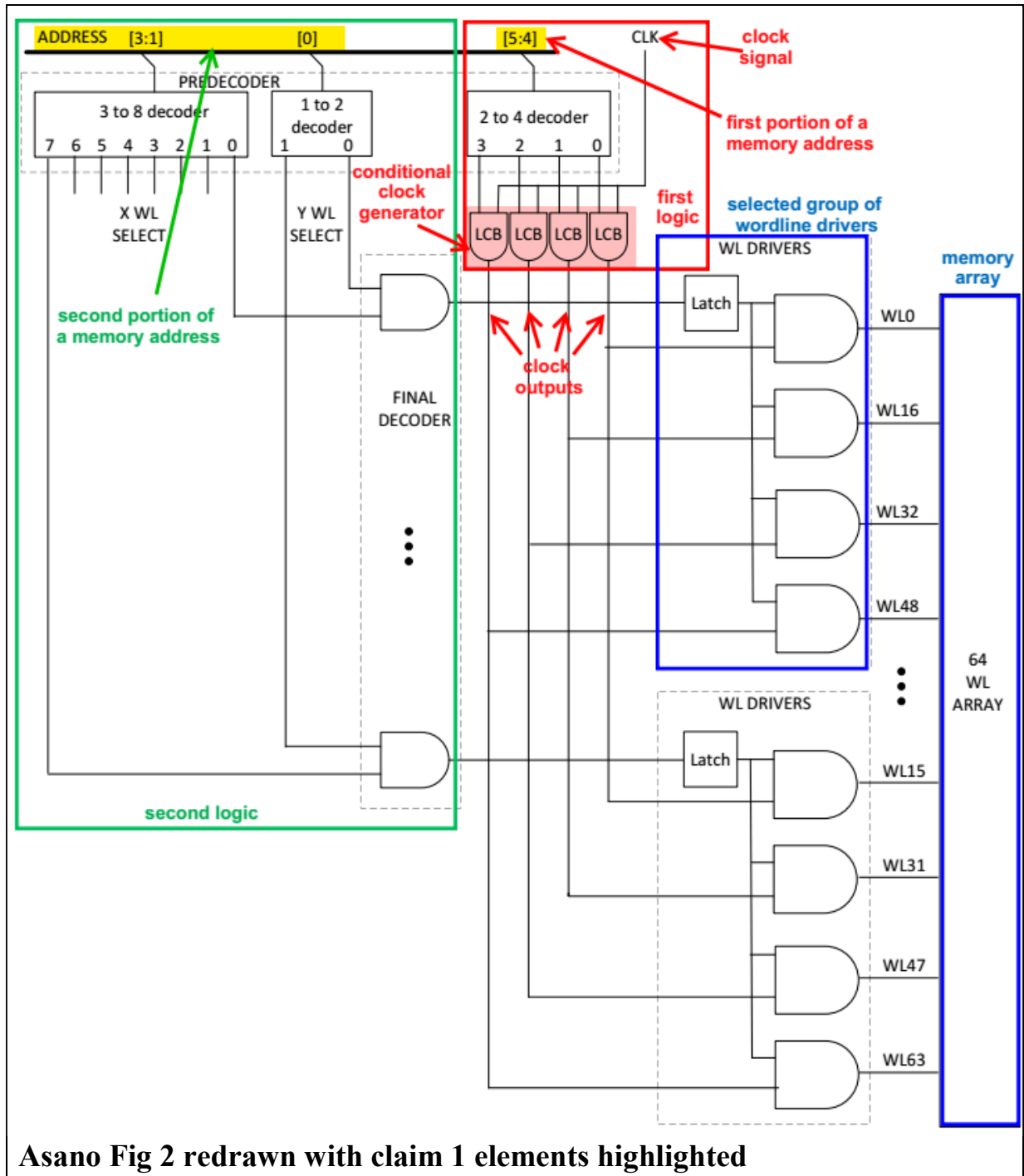
Memory address predecoding circuits which could be used to implement Asano's predecoder were well known before the '002 patent. APPLE-1007, 144-147; APPLE-1003, ¶¶121-124. Itoh provides several exemplary predecoder circuits in Figure 3.46. As an example, a POSITA could have implemented Asano's predecoder using a combination of the predecoder circuits disclosed by Itoh as shown in the annotated version of Asano's Figure 2 below.



Specifically, Asano explains that the “X wordline select signal” produced by the predecoder “is predecoder is 8 bits long,” and that the “Y wordline select signal” produced by the predecoder “is 4 bits long.” APPLE-1006, [0016]. As Dr. Horst explains, a predecoder generates intermediate signals that represent partially decoded addresses. APPLE-1003, ¶¶121-124. For example, Itoh’s two-bit predecoder (Figure 3.46(b)) generates four output signals that each represent one

of four possible combinations of two address bits (e.g., 00, 01, 10, and 11).

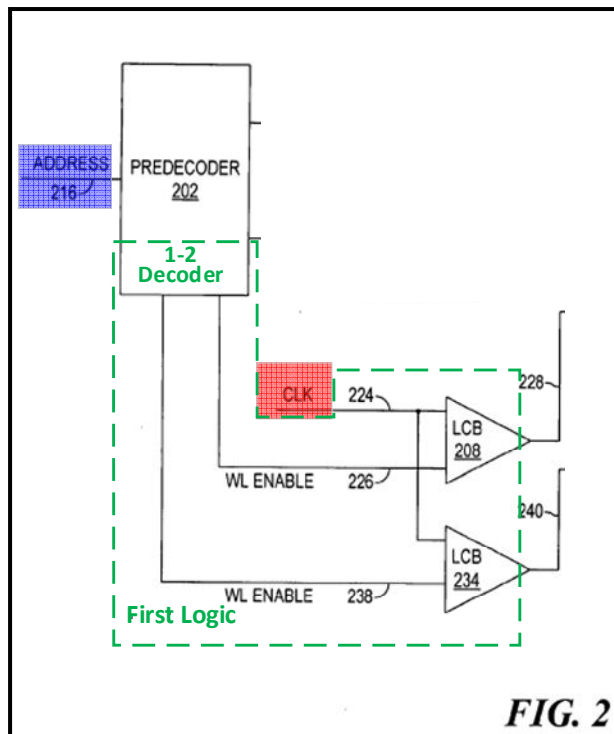
APPLE-1003, ¶¶111, 123. Similarly, Itoh's three-bit predecoder (Figure 3.46(c)) generates eight output signals that each represent one of eight possible combinations of two address bits (e.g., 000, 001, 010, 011, 100, 101, 110, and 111). APPLE-1003, ¶¶111, 123. Therefore, Asano's predecoder uses three address bits to produce the X wordline select signal and two address bits to produce the Y wordline select signal. As such, it would have been obvious for a POSITA to implement Asano's predecoder using Itoh's three-bit predecoder to generate the 8 bits of the X wordline select signal and Itoh's two-bit predecoder to generate the 4 bits of the Y wordline select signal. Together, the three-bit and two-bit predecoders represent the "second logic" portion of the predecoder (yellow). Finally, as Dr. Horst explains, a POSITA would have found it obvious to implement the "first logic" portion of Asano's predecoder (green) using a 1 to 2 decoder such as Itoh's address buffer circuit (Itoh Figure 3.46(a)) which provides the address bit and its complement as the two WL ENABLE signals (e.g., A_5 and $\overline{A_5}$). APPLE-1003, ¶¶108, 114-115. Moreover, Asano's Figure 1 can be redrawn to illustrate clearly what a POSITA would have understood the internal structure of the predecoder to look like from Asano's description. APPLE-1003, ¶¶108-115, 131. Dr. Horst's redrawn figure is reproduced below with annotations to indicate the elements of claim 1.



Finally, the above-described use of standard predecoder logic circuits disclosed by Itoh to implement Asano's predecoder would have been well within the skill level of a POSITA, because the exemplary implementation merely applies

known circuit designs to provide the functionality described by Asano. An artisan endeavoring to practice Asano's invention would have looked to known circuit designs when seeking to implement the Asano predecoder since Asano describes it at only a functional level, and since a POSITA would have known that the circuit level construction of such components was well known in the art. APPLE-1003, ¶¶121-124.

[1.1]: [the first logic] to receive a clock signal and a first portion of a memory address of a memory array,

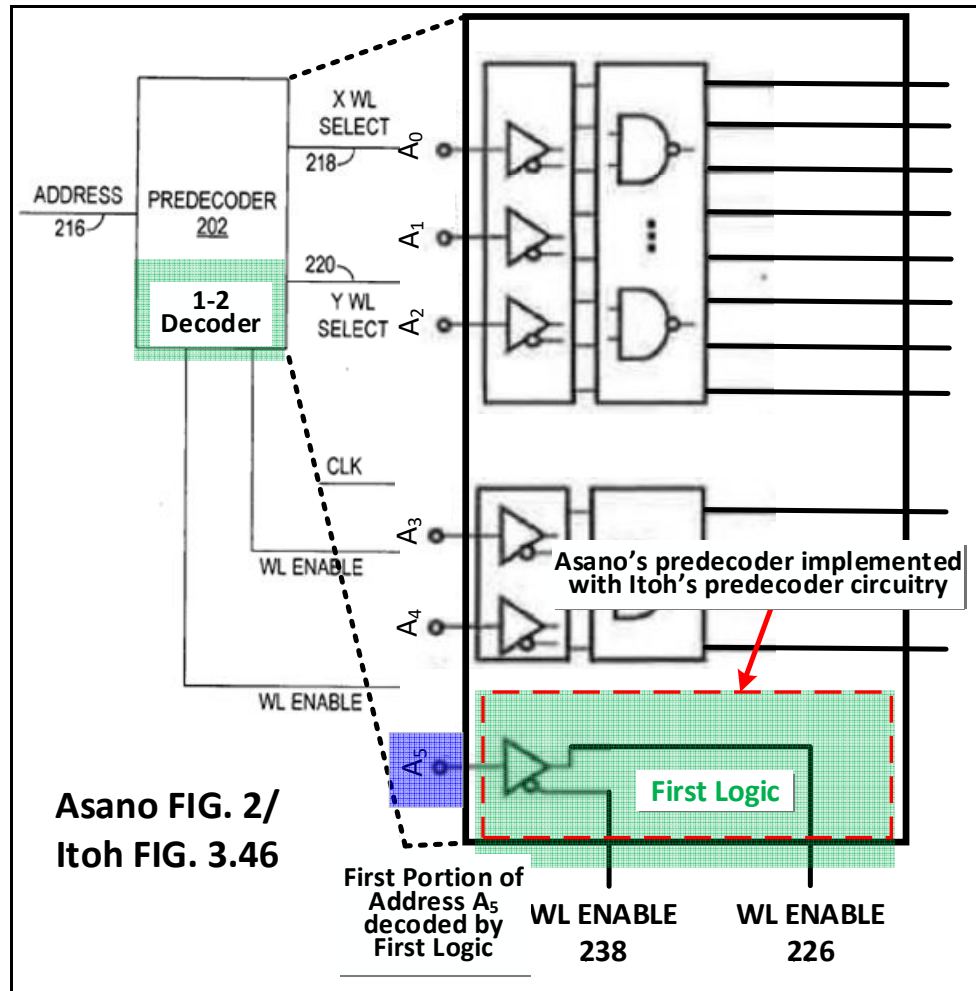


Asano discloses “first logic to receive a clock signal and a first portion of a memory address of a memory array” *See e.g.*, APPLE-1006, Figure 2 (below), [0016], [0019], [0021]; APPLE-1003, ¶¶117-120, 131. Asano’s “first logic” (green), as described above in view of Itoh, receives a clock signal (CLK-red) and the “most significant bit

of the address signal that is input into the predecoder” (purple). APPLE-1006, [0019]; APPLE-1003, ¶¶117-120, 131.

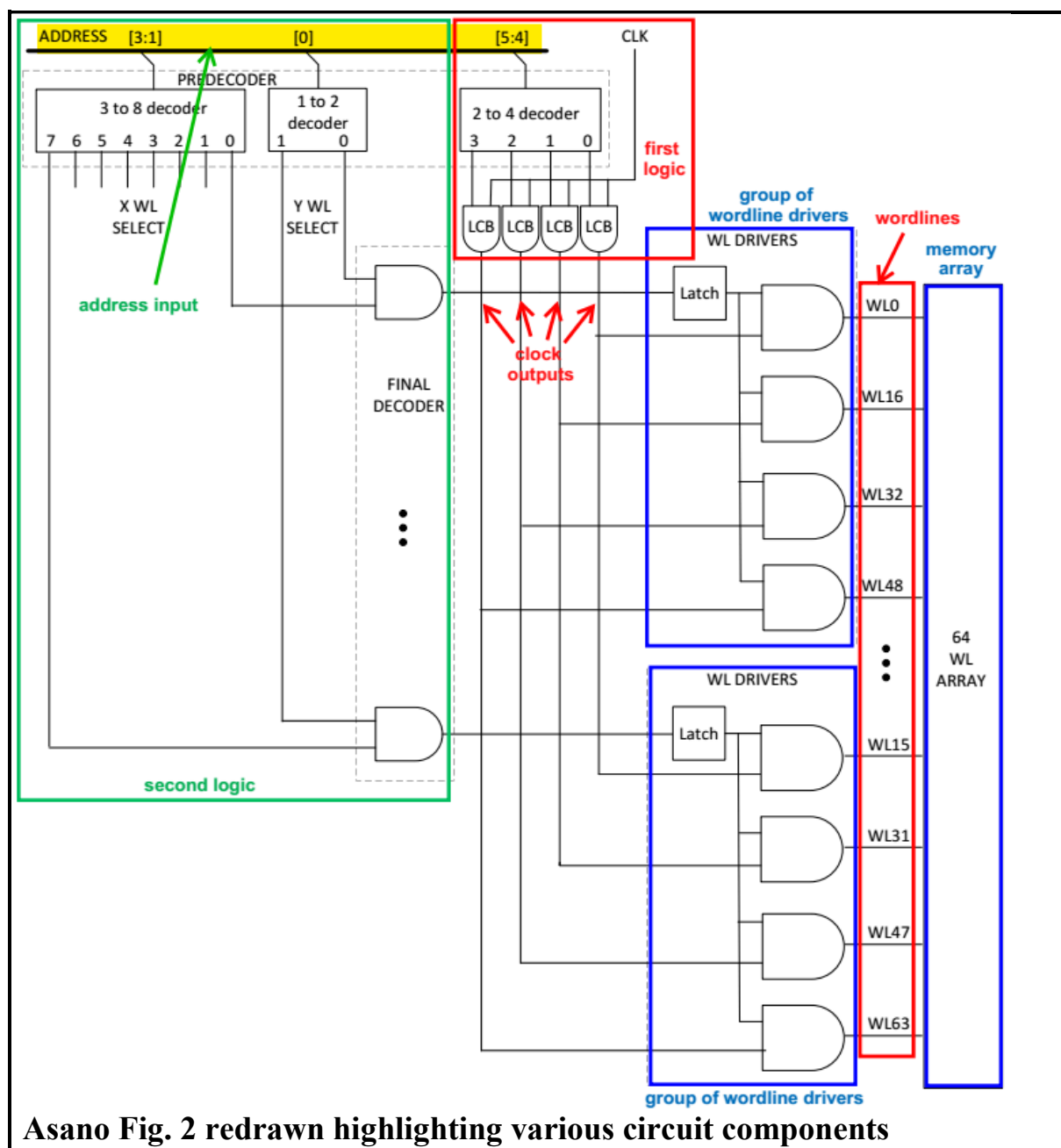
**[1.2]: the first logic to decode the first portion of the memory address
and**

Asano renders obvious “the first logic to decode the first portion of the memory address.” *See* APPLE-1006, Figure 2, [0016], [0018]-[0021]; APPLE-1003, ¶¶117-120. Asano’s predecoder 202 decodes a first portion of a memory address (e.g., the most significant bit) to generate the WL enable signals 226/238, which the predecoder provides to LCBs 208/234. APPLE-1006, [0018]-[0019]. As discussed above, a POSITA would have understood that the “first logic” portion of Asano’s predecoder could be implemented using known logic circuitry such as that disclosed by Itoh. Such circuitry would have been a 1:2 decoder that can “decode” one address bit by outputting the address bit along with its complement (see Asano’s Figure 2 as annotated below to include Itoh’s Figure 3.46) such as complementary address. APPLE-1003, ¶¶115, 123.



Asano also notes that more than one address bit may be used for LCB selection. Asano states, "for the purposes of illustration, 1 bit has been utilized for LCB selections." APPLE-1006, [0021]. But, "[i]t is possible to have 2 or more LCB selections up to N bits." *Id.* In each case, 2^N LCBs would each have a "reduced load of 2^{-N} ." *Id.* In such a situation, it would have been reasonable for a POSITA to implement the "first logic" portion of Asano's predecoder using Itoh's two-bit predecoder circuit to provide four (2^2) LCB selection signals. APPLE-1003, ¶¶117-120. For example, Dr. Horst provides a redrawn version of Asano's

Figure 2 (reproduced below) that illustrates how a POSITA would have expanded Asano's address decoder to utilize two address bits for LCB selection. *Id.*, ¶¶117-118.



Thus, Asano in view of Itoh renders this limitation obvious.

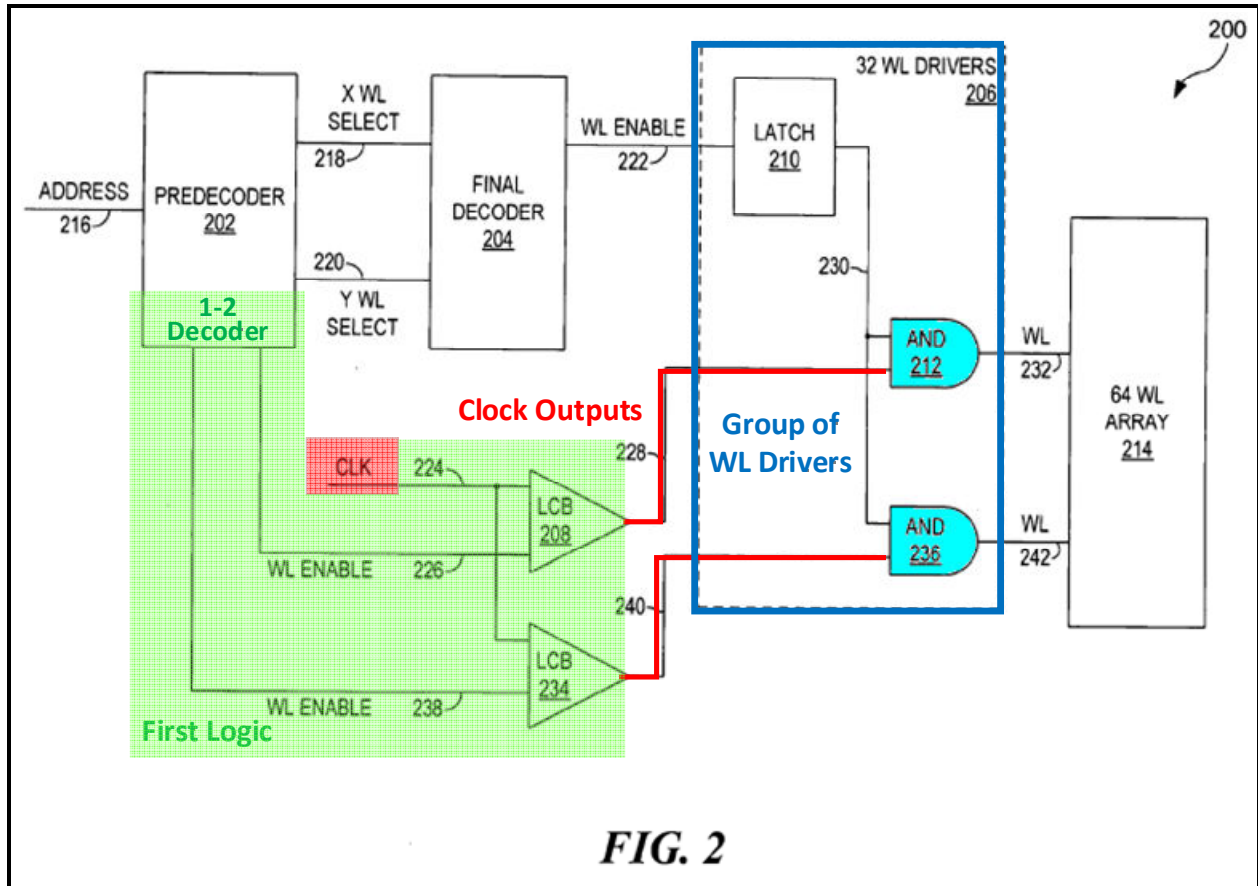
[1.3]: [the first logic . . .] to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array;

Asano in view of Itoh renders obvious that the LCBs “apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array.”

See APPLE-1006, Figure 2 (below), [0016]-[0021]; APPLE-1003, ¶¶14, 113-118, 132-133.

First, Asano discloses that the “first logic” (green), and more specifically the LCBs 208/234, apply the clock signal (light red) to one of the clock outputs (communication channels 228/240). APPLE-1006, [0017]-[0018]; APPLE-1003, ¶¶118-119, 131. Asano explains that the “first LCB 208 and the second LCB 234 . . . provide clocking signals to the wordline drivers 206 through a fifth communication channel 228 and a sixth communication 240.” APPLE-1006, [0017]. Furthermore, the “clocking signal from each of the LCBs 208 and 234 are based on two inputs, a clock input and a select signal.” APPLE-1006, [0018]. “Each of the LCBs 208 and 234 receive a clocking signal through a seventh communication channel 224, and the predecoder 202 generates additional selection signals for the LCBs 208 and 234” based on the “most significant bit of the address signal.” APPLE-1006, [0018]-[0019]; *see also* [0021]. Finally, each LCB is “configured to propagate [the] clocking signal if [it] is enabled” by a selection

signal. APPLE-1006, Claim 7. A POSITA would have understood from this explanation in view of Figure 2 that the output for the clock is selected between channels 228 and 240 based on the most significant address bit. APPLE-1003, ¶115.



Second, Asano's Figure 2 illustrates that the clock outputs (224/240) are associated with a selected group of a plurality of wordline drivers (e.g., WL DRIVERS 206-outlined in blue) which are themselves associated with the memory array 214. In Asano's illustrated embodiment, there are 32 groups of wordline drivers with two drivers (light blue) per group. APPLE-1006, [0019]. Wordline

drivers (e.g., AND gates 212/236) drive wordlines (e.g., WL 232/242) of the wordline array 214 and therefore are associated with the memory array. APPLE-1006, [0019].

Notably, Asano identifies 206 as WL DRIVERS (plural), consistent with how a POSITA would have understood that structure, based on their understanding of the term wordline driver as used in the art. APPLE-1003, ¶¶119, 126-128; *see also* APPLE-1007, 149 (each “word line has its own word driver”), Figure 3.48.

For example, typically each wordline driver drives a corresponding wordline. *Id.*

For instance, Itoh’s description of the “Basic Word Driver” states that “[e]ach

word line . . . has its own word

driver.” APPLE-1007, 149. Itoh

further illustrates a group of four

basic wordline drivers in which each

driver drives only one wordline.

APPLE-1007, Figure 3.48(a) (right).

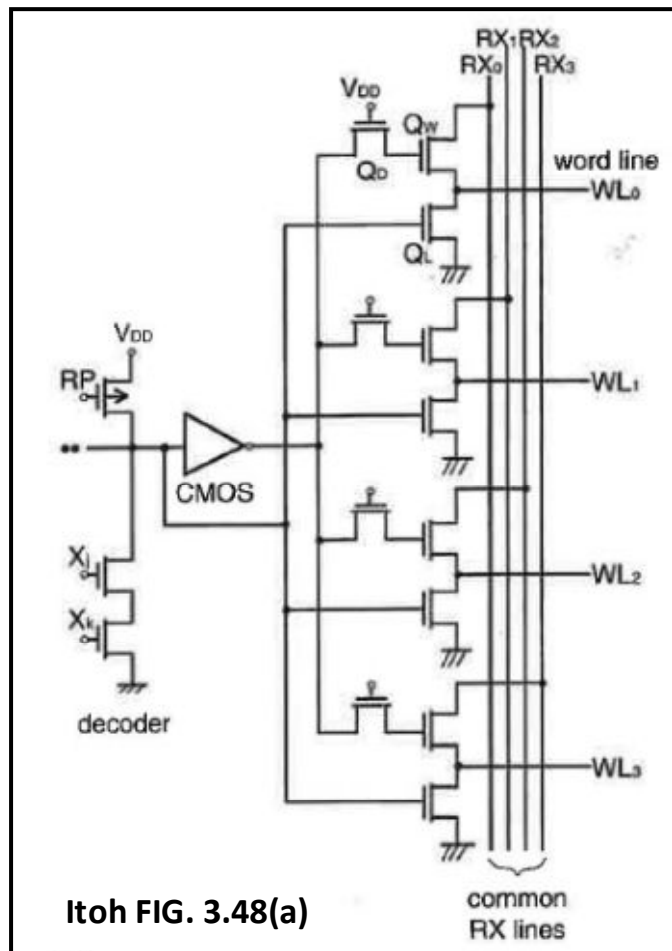
Sato also corroborates this

interpretation of a wordline driver.

APPLE-1005, 6:22-31. Thus, each

of Asano’s AND gates 212/236

would have been understood by a

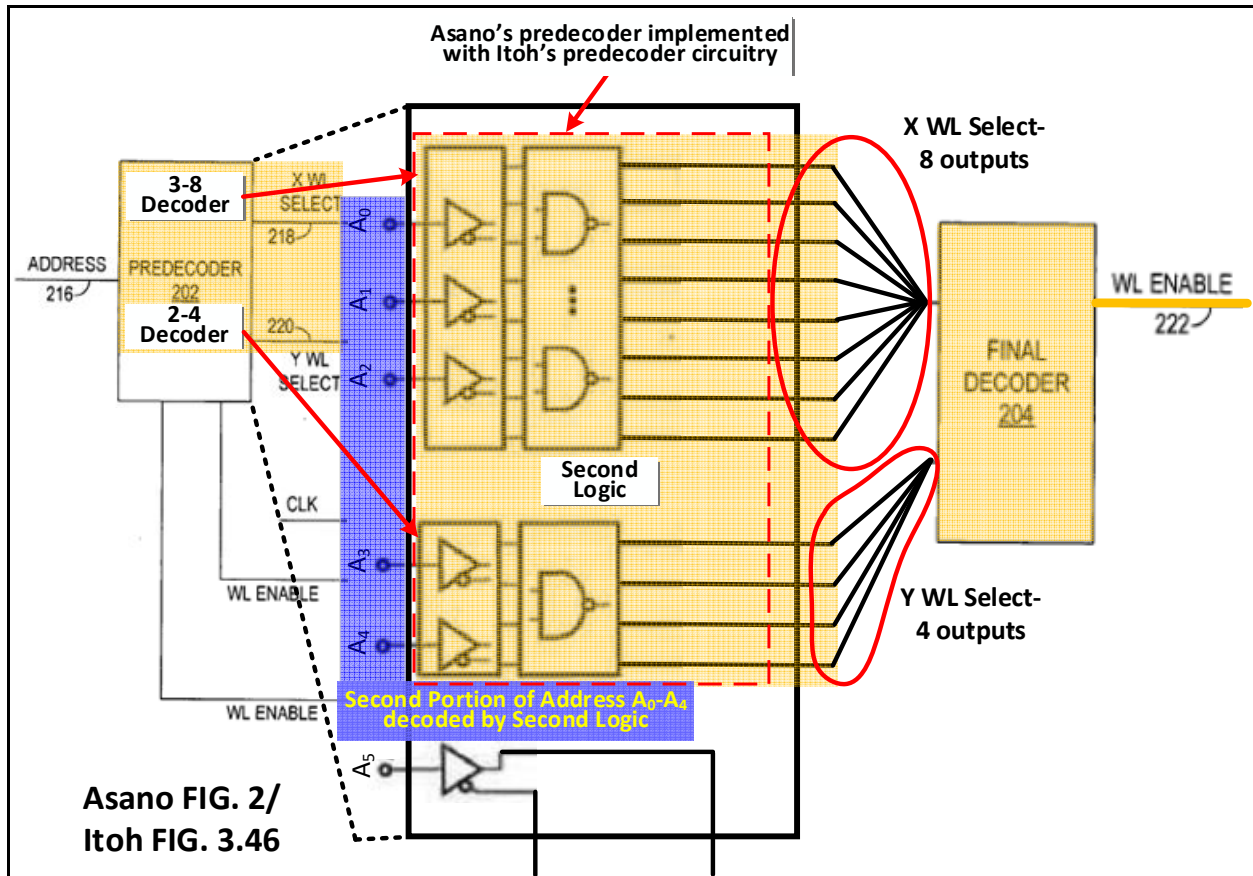


POSITA to represent an individual wordline driver in conformance with the common understanding of a wordline driver as used within the art.

Accordingly, Asano in view of Itoh renders this limitation obvious.

[1.4]: [the second logic] to decode a second portion of the memory address,

Asano and Itoh render obvious second logic to decode a second portion of the memory address. *See* APPLE-1006, Figure 2, [0016]-[0017]; APPLE-1003, ¶¶110-111, 118, 122-123. Asano's predecoder 202 and final decoder 204 decode five of six address bits (e.g., the second portion) of memory address 216. APPLE-1006, [0016]; APPLE-1003, ¶¶110-111, 118. Asano states that "from those 6 [address] bits, the predecoder derives . . . an [8-bit] X wordline select signal and a [4-bit] Y wordline select signal." APPLE-1006, [0016]. As discussed in Ground-2 [1.0] above, it would have been an obvious design choice for a POSITA to implement Asano's predecoder using Itoh's three-bit and two-bit predecoders to generate the X and Y wordline select signals as shown in the annotated figure below. APPLE-1003, ¶¶110-111, 118, 122-123. As demonstrated in the figure below, the three-bit predecoder decodes the three bits of the second portion of the address signal (purple) to produce the 8-bit X WL select signal and the two-bit predecoder decodes two bits of the second portion of the address signal to produce the Y WL select signal. APPLE-1003, ¶¶110-111, 118, 122-124.



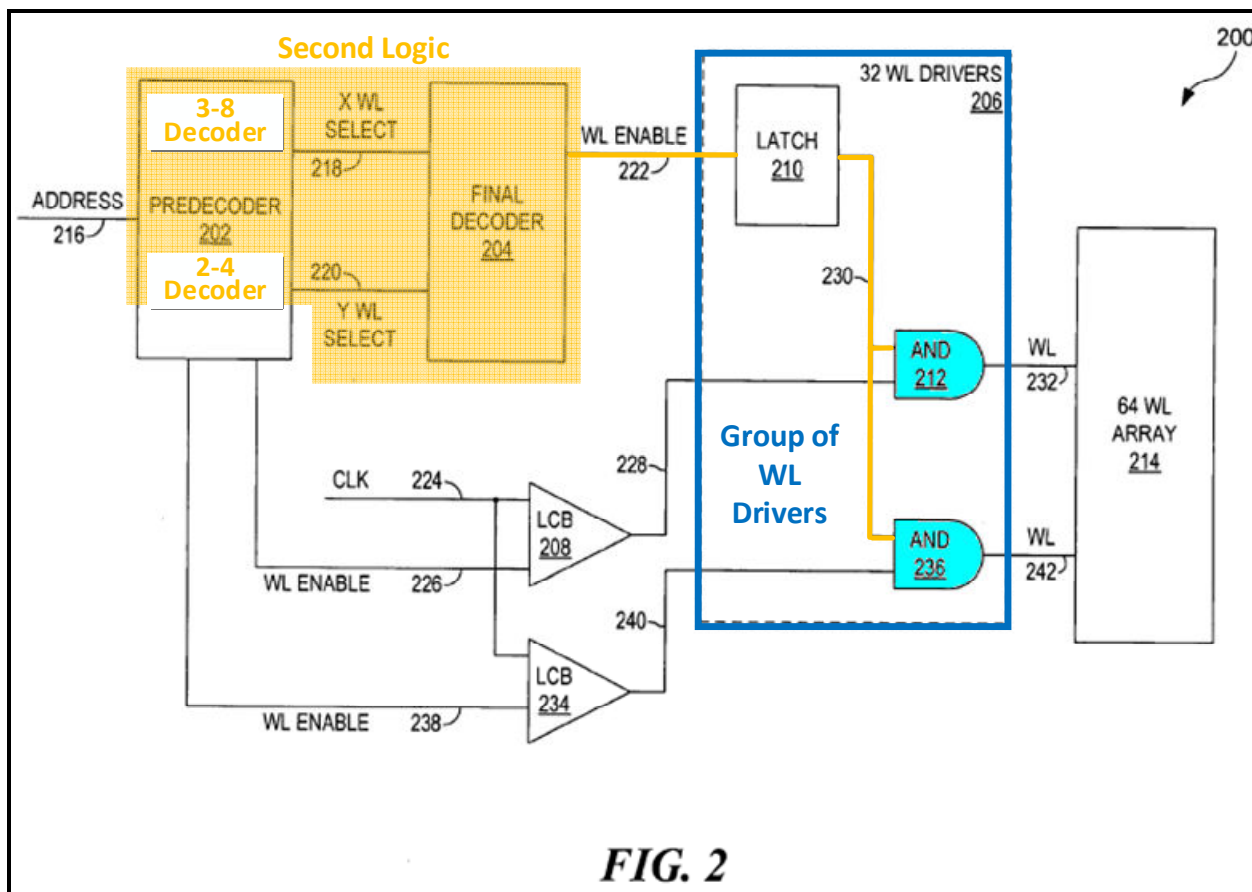
The final decoder decodes the X and Y wordline select signals to determine which of the 32 wordline groups to enable. APPLE-1003, ¶112. Specifically, “[o]nce the X wordline select signal and the Y wordline select signal have been transmitted to the final decoder 204, the final decoder 204 . . . determines which of the 32 wordline drivers 206 are to be enabled.” APPLE-1006, [0017]. The final decoder passes respective WL ENABLE signals (orange line) to the wordline drivers. APPLE-1006, [0017].

Accordingly, Asano in view of Itoh renders obvious this limitation.

[1.5]: the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

Asano and Itoh render obvious second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address. *See* APPLE-1006, Figure 2 (below), [0016]-[0017], [0019]; APPLE-1003, ¶134. Asano discloses that the final decoder (part of the second logic—orange below) “determines which of the 32 wordline drivers 206 are to be enabled” and communicates the WL enable signal (orange line) to the appropriate group of wordline drivers (blue outline). APPLE-1006, [0017]; APPLE-1003, ¶¶119, 134. The WL enable signal is latched and output to both AND gate wordline drivers (light blue) in the group. APPLE-1006, [0019]. “Either the first AND gate 212 or the second AND gate 236” wordline driver “is selected [when] the clocking signal is ANDed with the output of the latch.” APPLE-1006, [0019]. The output of the latch is the WL enable signal. Finally, the selected AND gate wordline driver can then “output a wordline signal in step 318 to a wordline within the 64 wordline array.” APPLE-1006, [0019].

Accordingly, Asano in view of Itoh renders this limitation obvious.



C. Claims 2-28 and 31-37 Are Obvious Over Sato [GROUND-1]; Claims 2-17, 20-28, and 31-36 Are Obvious Over Asano in view of Itoh [GROUND-2]

Claim 2-[2.0]: The circuit device of claim 1, wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output.

Ground-1

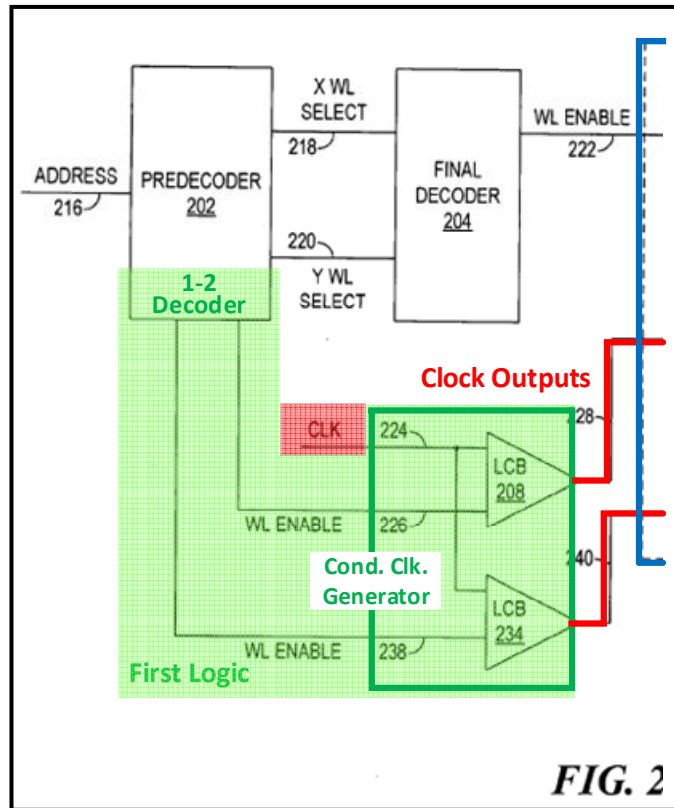
Sato's PDCR operates comparably to the conditional clock generator 110 described in the '002 patent. *See* Ground-1, [1.1], [1.3]; APPLE-1003, ¶84. The '002 patent states that the conditional clock generator 110 "receives a clock signal

via the clock input 118 and selectively applies the clock signal to a selected one of the clock outputs 124, 126, 128 and 130 [or] [i]n a particular embodiment, the conditional clock generator 110 may derive the clock outputs 124, 126, 128 and 130 from a single clock.” APPLE-1001, 3:28-36. In a similar manner, the PDCR receives the timing signal ϕ_{ce} and generates a selection signal $\phi_{x0}-\phi_{x3}$ “in accordance with the complementary internal address signals ax_0 and ax_1 ” and “in accordance with [the] timing signal ϕ_{ce} , thereby, selectively applying the timing signal to a selected one of the selection signal outputs. APPLE-1005, 5:28-31, 9:52-59, 10:36-39; APPLE-1003, ¶¶14, 65-69, 71-73, 84. Thus, Sato’s PDCR performs comparable functions to that of the ’002 patent’s conditional clock generator and a POSITA would have correctly interpreted Sato’s PDCR as a conditional clock generator. Therefore, Sato discloses or renders the features of claim 2 obvious.

Ground-2

Asano’s LCBs work to together to generate a conditional clock, and thus represent a conditional clock generator like conditional clock generator 110 described in the ’002 patent. *See* APPLE-1006, Figure 2 (below), [0018]-[0020], Claims 7, 11; Ground-2, [1.1], [1.3]; APPLE-1003, ¶¶131, 135. The ’002 patent states that the conditional clock generator 110 “receives a clock signal via the clock input 118 and selectively applies the clock signal to a selected one of the

clock outputs 124, 126, 128 and 130.” APPLE-1001, 3:28-31. In a similar manner, the LCBs receive the clock signal (CLK) and selectively apply clock signal to one of the outputs (red). APPLE-1006, [0018]-[0019]; APPLE-1003, ¶¶113-115. In particular, Asano’s claims state that the LCBs are “configured to propagate clocking signals if



enabled” and “only one LCB of the plurality of LCBs are enabled at one time.” APPLE-1006, Claims 7, 11. As in the ’002 patent, Asano’s LCBs are controlled based on the decoded first portion of the memory address (WL enable selection signals). Compare APPLE-1006, Figure 2, [0018], [0021] with APPLE-1001, Figure 1, 10:26-32 (Asano’s LCBs are controlled by decoded address signals (WL enable) like the clock generator is controlled by the output of the 2-4 decoder). Specifically, Asano states, “for the purposes of illustration, 1 bit has been utilized for LCB selections.” APPLE-1006, [0021].

In other words, like the conditional clock generator described in the ’002 patent, Asano’s LCBs receive a clock signal (CLK) and decoded address signals

(e.g., WL enable selection signals) from a first portion of the input address (e.g., (the most significant bit of the address signal”). APPLE-1006, [0019]. The LCBs then selectively apply the clock signal to one of a plurality of outputs (e.g., lines 228 or 240) based on the state of the decoded address signals (e.g., WL enable). Thus, a POSITA would have found a conditional clock generator obvious in view of Asano’s LCBs, which operate similar to the ’002 patent’s conditional clock generator. APPLE-1003, ¶¶131, 135. Accordingly, the combination of Asano and Itoh renders the features of claim 2 obvious.

Claim 3-[3.0]: The circuit device of claim 2, wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.

Ground-1

Sato’s PDCR applies the clock signal to the selected clock output according to the first portion of the memory address. *See* Ground-1, [1.1], [1.3]; APPLE-1003, ¶84. In particular, Sato’s PDCR receives timing signal ϕ_{ce} and generates a selection signal $\phi_{x0}-\phi_{x3}$ “in accordance with the complementary internal address signals ax_0 and ax_1 ” (the first portion of the memory address) and “in accordance with [the] timing signal ϕ_{ce} , thereby, selectively applying the timing signal to a selected one of the selection signal outputs. APPLE-1005, 5:28-31, 9:52-59, 10:36-39; APPLE-1003, ¶84. Thus, Sato discloses or renders the features of claim 3 obvious.

Ground-2

See Ground-2, [2.0]; APPLE-1006, [0021], Claim 7 (“for the purposes of illustration, 1 bit has been utilized for LCB selections” and LCBs are “configured to propagate clocking signals if enabled”).

Claim 4-[4.0]: The circuit device of claim 1, wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address.

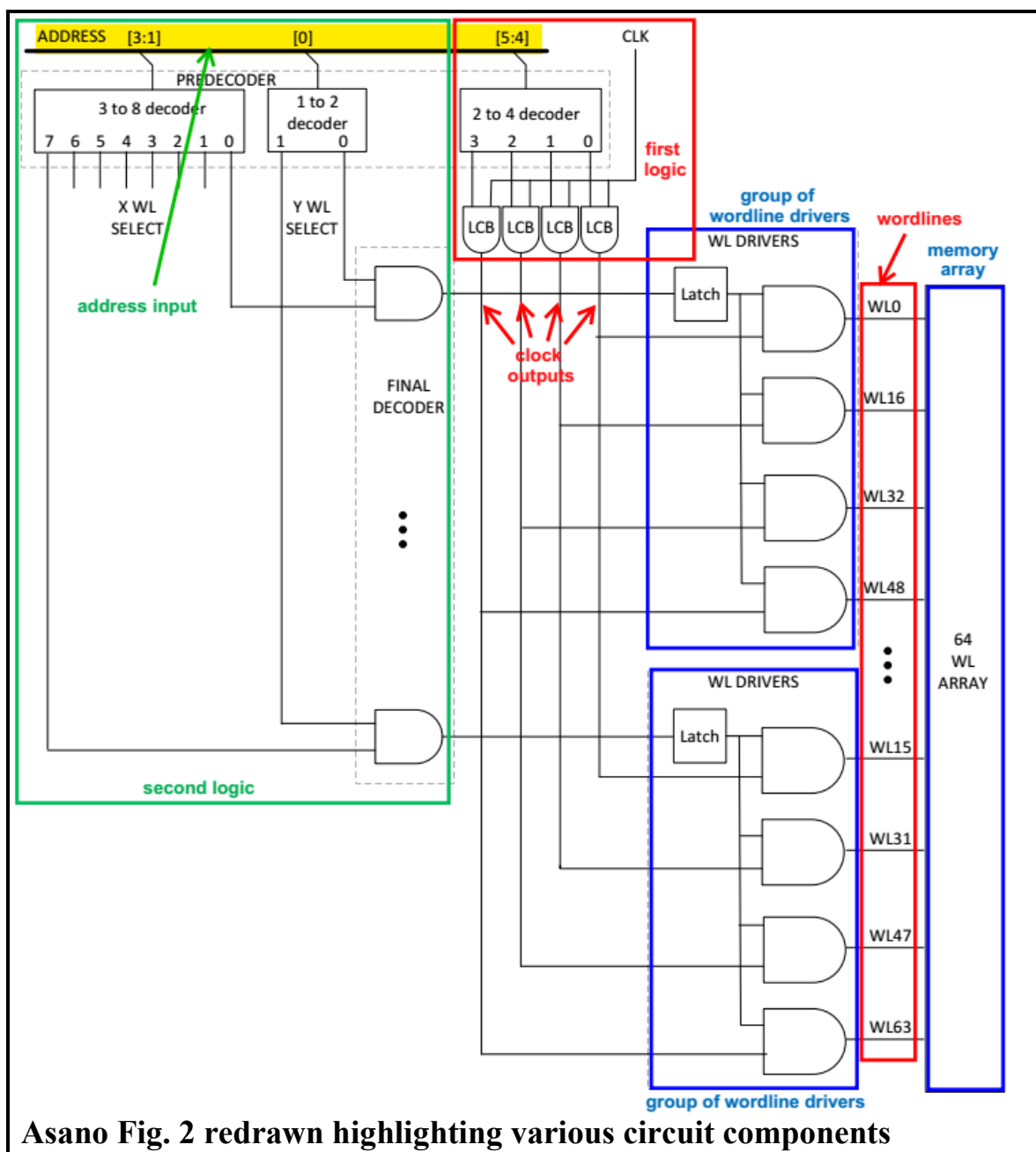
Ground-1

Sato’s PDCR “decodes the lower 2-bit complementary internal address signals ax0 and ax1 supplied thereto from the X address buffer XADB.” APPLE-1005, 5:25-27. Alternately, “[t]he pre decoder PDCR may be of such a type which decodes the address signal of at least three lower bits.” APPLE-1005, 11:54-56. Thus, Sato discloses or renders the features of claim 4 obvious.

Ground-2

Asano acknowledges that additional bits (e.g., two) can be used for LCB selection. APPLE-1006, [0021] (“for the purposes of illustration, 1 bit has been utilized for LCB selections,” but “[i]t is possible to have 2 or more LCB selections up to N bits. In each case, there will be 2^N LCBs”). Thus, it would have been obvious to a POSITA to implement Asano’s predecoder to use Itoh’s two-bit predecoder to generate four LCB selection signals based on two bits of the input address. APPLE-1003, ¶¶117-119. In view of the fact that Asano explicitly

suggests expanding the number of bits used for LCB selection, a POSITA would have recognized that the particular number of address bits decoded by the first logic as the “first portion of the memory address” would merely have been an obvious design choice selected from five possible options (e.g., 1-5 of Asano’s six address bits). APPLE-1003, ¶¶117-119. Moreover, the uses of more LCBs would serve to reduce the number of latches and allow “the area of the final decoder [to] be reduced by 2^{-N} .” APPLE-1006, [0021]. For example, Dr. Horst provides a redrawn and expanded version of Asano’s Figure 2 (below) that illustrates how a POSITA would have the structure shown in Asano’s Figure 2 to use 2-bits the first portion of the memory address. *See* APPLE-1003, ¶¶117-119, 124, 131.



Claim 5-[5.0]: The circuit device of claim 1, wherein the first logic generates four conditional clock outputs,

Ground-1

Sato's PDCR generates four conditional clock outputs; selection signals ϕ_{x0} , ϕ_{x1} , ϕ_{x2} , and ϕ_{x3} . *See* Ground-1, [1.3]; APPLE-1005, Figure 3, 5:25-42, 9:52-95. Thus, Sato discloses or renders this limitation obvious.

Ground-2

See Ground-2, [4.0]. In view of the explicit suggestion by Asano to use additional bits for LCB selection, it would have been obvious to a POSITA to implement Asano's predecoder using Itoh's two-bit predecoder to generate four LCB selection signals based on two bits of the input address (e.g., $2^2=4$). APPLE-1003, ¶¶117-119. Such a modification would have resulted in four clock outputs, one for each LCB. *Id.*

[5.1]: wherein one of the four conditional clock outputs is active at a time,

Ground-1

Sato discloses activating only one of the four selection signals ϕ_{x0} - ϕ_{x3} at a time. APPLE-1003, ¶85. Sato describes how each of the signals ϕ_{x0} - ϕ_{x3} are selected based on a different combination of the lower two address bits (ax_0 , ax_1) of an input address so that "only the word line drive circuit corresponding to one word line that is designated by the X address signal Ax_0 - Ax_i ." . APPLE-1005,

5:25-42, 6:57-59; *see also* 6:40-59; 9:31-51, Claim 1; APPLE-1003, ¶85.

Consequently, a POSITA would have understood that only one of the selection signals $\phi x0$ - $\phi x3$ can be active at a time for a given memory address. APPLE-1003, ¶85. Thus, Sato discloses or renders the limitation obvious.

Ground-2

Asano states, “only one LCB of the plurality of LCBs are enabled at one time.” APPLE-1006, Claim 11. Therefore, only one clock output would be active at a time. APPLE-1003, ¶135. Thus, the combination of Asano and Itoh renders this limitation obvious.

[5.2]: the first logic to apply the one conditional clock output as the selected clock output.

Ground-1

See Ground-1, [1.3] (describing how the PDCR applies the selected clock output (selection signal $\phi x0$ - $\phi x3$) as an output).

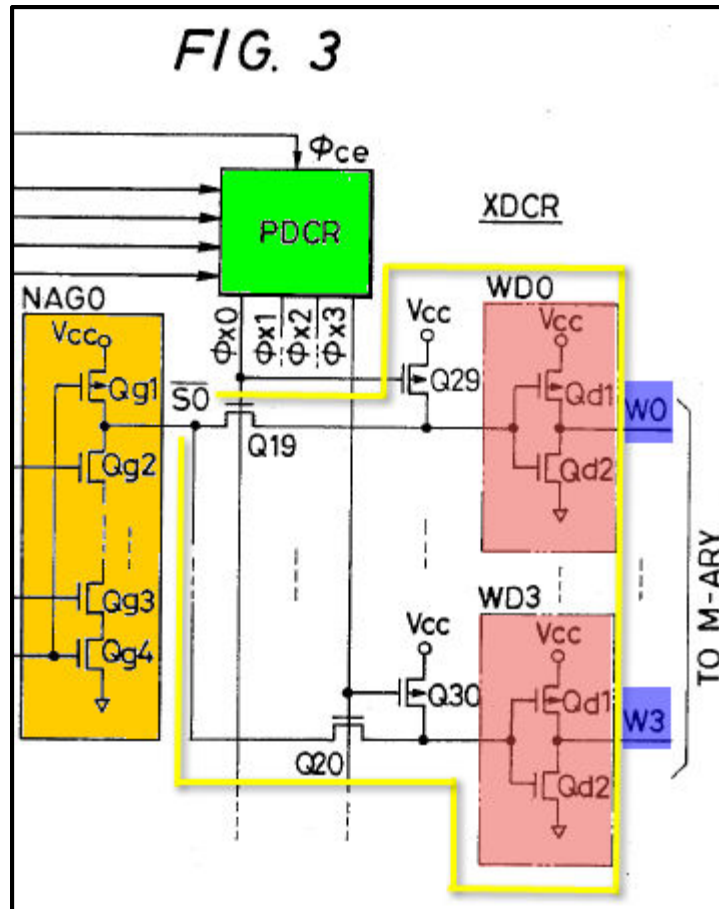
Ground-2

See Ground-2, [1.3], [5.1]; APPLE-1006, Claim 7 (the LCB is “configured **to propagate** clocking signals **if enabled**”).

Claim 6-[6.0]: The circuit device of claim 1, wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array,

Ground-1

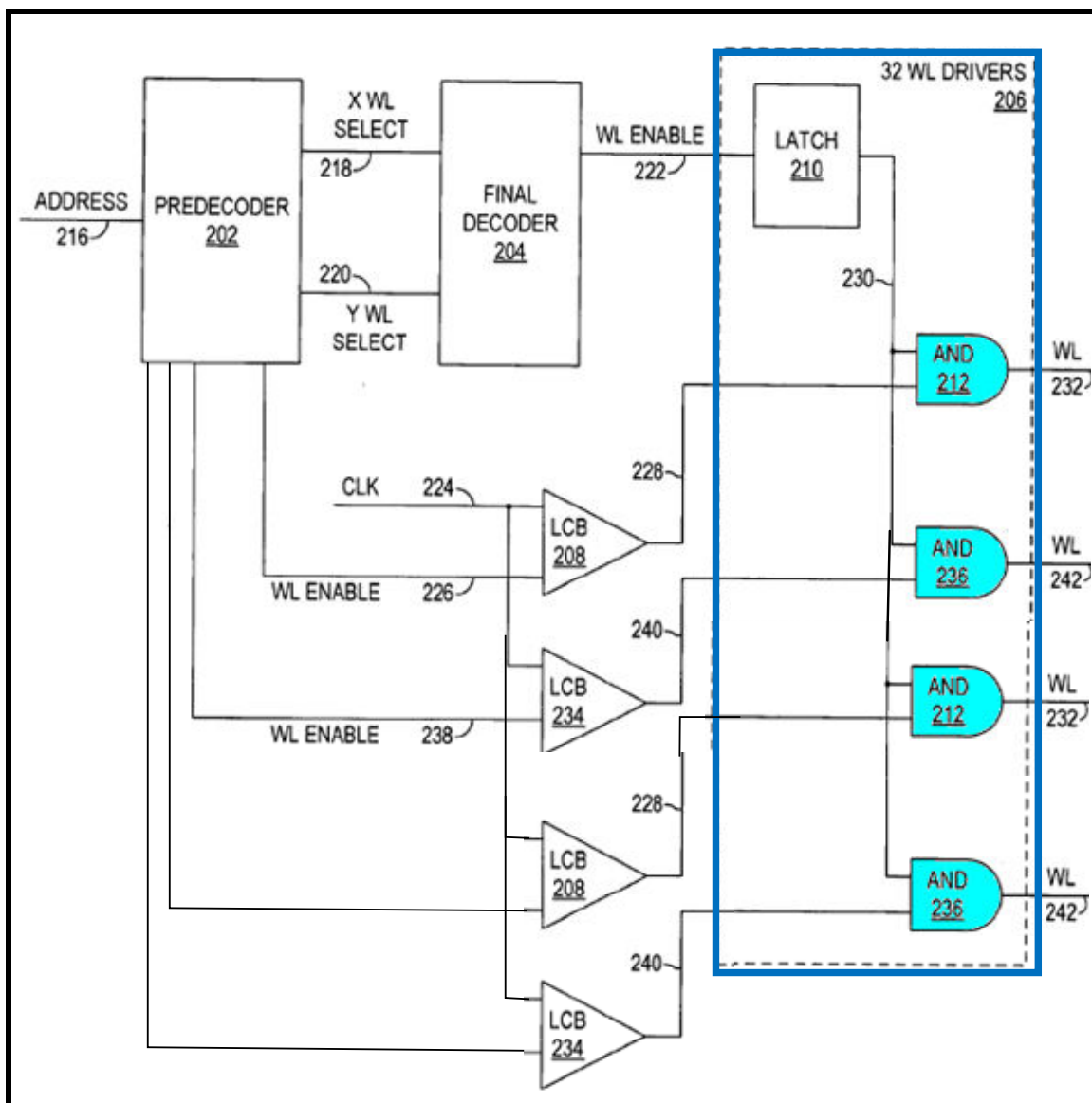
Sato describes and illustrates groups of wordline drivers that each include four wordline drivers each associated with a wordline of the memory array. Each of Sato's figures (1-3) illustrate groups of four wordline drivers, e.g., WD0 through WD3 and W_m-3 W_m (Figure 1). Sato explains that each group of wordline drivers (yellow) in Figure 3 (below) includes "capacitance cut MOSFETs Q19-Q20 for receiving the corresponding selection signals ϕ_{x0} - ϕ_{x3} from the pre-decoder PDCR [green] at their gates are disposed between the decoding NAND gate circuit NAG0 [orange] and the corresponding **four** sets of word line drive circuits WD0-WD3 [red]." APPLE-1005, 9:60-64. Furthermore, each wordline driver is associated with one wordline (W0-W3) (blue) of memory array M-ARY. APPLE-1005, 6:22-39; 9:44-51; APPLE-1003, ¶58.



Ground-2

See Ground-2 [4.0], [5.0]. It would have been obvious to a POSITA to include four AND gate wordline drivers (light blue in Asano's Figure 2 annotated and redrawn below) in each group of wordline drivers (blue outline) if one were to use two address bits for "LCB selections." APPLE-1003, ¶¶117-119. Asano states that "[i]t is possible to have 2 or more LCB selections up to N bits. In each case, there will be 2^N LCBs" (e.g., $2^2=4$ LCBs). Asano also states that using more bits would reduce the number of latches. APPLE-1006, [0021]. In view of Asano's

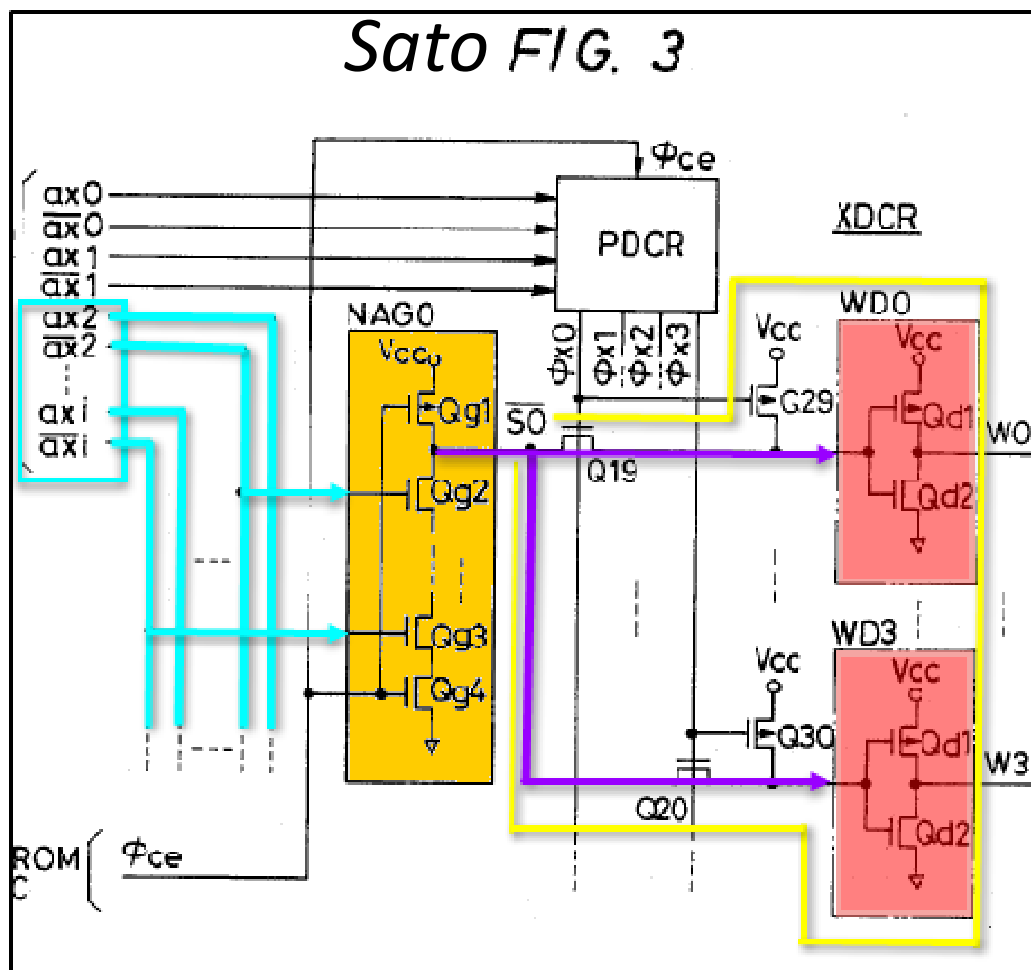
design in Figure 2, it would have been obvious to a POSITA that in order for the use of more address bits for LCB selection to result in less latches, the number of AND gate drivers per latch must be correspondingly increased. APPLE-1003, ¶¶117-119. Thus, if a POSITA chose to use two address bits to produce four clock outputs (*see* Ground-2 [5.0]), the resulting circuit would have included four AND gate wordline drivers per group. *Id.*



[6.1]: wherein the four wordline drivers share a common address input.

Ground-1

Sato discloses a common address input for each of the four wordline drivers (e.g., WD0-WD3). The '002 patent equates a shared (or common) address input with the partially decoded address lines 120/122 of Figures 1 and 3. *See* APPLE-1001, 10:32-37. By comparison with Figure 3 of the '002 patent, Sato's Figure 3 (below) discloses a common address line (purple) that provides the selection signal $\overline{S0}$ from the decoding NAND gate circuit NAG0 (orange) to each of the four wordline drivers WD0-WD3 (red) of the depicted group of drivers (yellow). *See* APPLE-1005, 5:43-21; APPLE-1003, ¶¶83, 86-91. For example, each of the wordline drivers WD0-WD3 of the depicted group of drivers share the same input address $\overline{ax2}-\overline{axi}$ (blue) provided to the decoding NAND gate circuit NAG0. APPLE-1003, ¶91. Sato explains that the output of a respective decoding NAND gate circuit (e.g., $\overline{S0}$) is asserted (e.g., set to a low logic level) when any one of the wordlines associated with its wordline drivers is designated by the X address signal AX0-AXi and (as shown) is applied through the common address line each of the wordline drivers depending on the state of the respective capacitance cut MOSFET (Q19-Q20). *See* APPLE-1005, 5:43-6:21; APPLE-1003, ¶75, 83. Thus, Sato discloses that each group of wordline drivers shares a common address input.

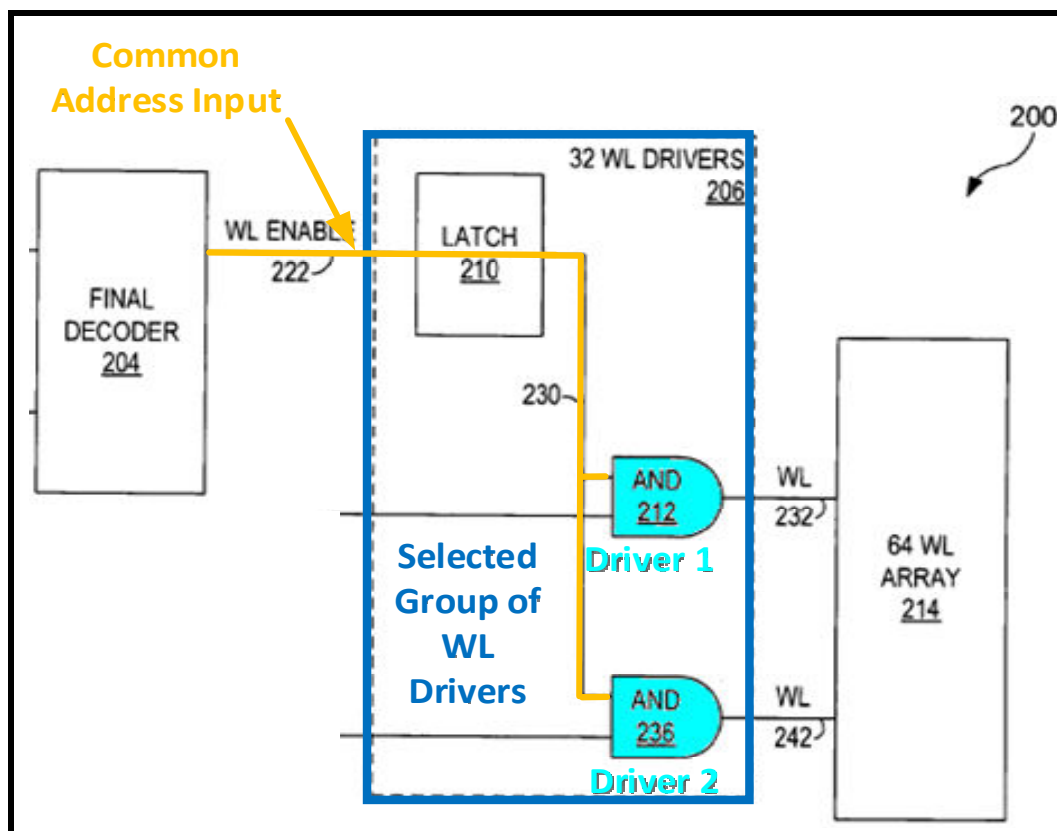


Ground-2

Asano discloses a shared common address input for a group of wordline drivers. APPLE-1006, Figure 2 (below), [0019]. APPLE-1003, ¶¶136-137. The output of Asano's final decoder 204, which represents the decoded second portion of a memory address (*see* Ground-2 [1.4]), is a common address input to all of the AND wordline drivers in a given group. *Id.* For each group of wordline drivers, the "latch 210 receives a wordline enable signal through the fourth communication channel 222 [from the final decoder], where the signal is latched" and then output

“to the first AND gate 212 and the second AND gate 236.” APPLE-1006, [0019].

According to the modification discussed in [6.0] all four AND gate wordline drivers would share a common address input at least because they would share a latch that receives and latches the common address input. *Id.* Therefore, it would have been obvious to a POSITA that the modified design of [6.0] would include a shared common address input between four AND gate wordline drivers.



Claim 7-[7.0]: A method of selecting a particular wordline of a memory array, the method comprising:

Ground-1

Sato describes a method of selecting a particular wordline of a memory array because it describes the operation of its X address decoder, which selects “one of

the wordlines designated by the X address signal AX0-AXi.” APPLE-1005, 3:65-4:2; Ground-1, [1.0].

Ground-2

Asano describes a method of selecting a particular wordline of a memory. APPLE-1006, Abstract, Figure 3, [0008] (“The present invention provides a wordline (WL) driver method”); Ground-2, [1.0].

[7.1] decoding a first portion of a memory address of the memory array;

See Ground-1 and Ground-2, [1.2].

[7.2]: selectively providing a clock signal to a selected group of a plurality of wordline drivers based on the first portion of the memory address, wherein each of the plurality of wordline drivers is associated with a wordline of the memory array;

See Ground-1 and Ground-2, [1.3], [6.0] (explaining that each of four wordline drivers of Sato (Ground-1) and Asano (Ground-2) are associated with a respective wordline of a memory array).

[7.3]: decoding a second portion of the memory address; and

See Ground-1 and Ground-2, [1.4].

[7.4]: activating a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

See Ground-1 and Ground-2, [1.5].

Claim 8-[8.0]: 8. The method of claim 7, further comprising: receiving the clock signal;

See Ground-1 and Ground-2, [1.1].

[8.1]: selectively applying the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

See Ground-1, [1.3].

Claim 9-[9.0]: 9. The method of claim 7, further comprising: determining a clock output according to the first portion of the memory address using a conditional clock generator.

See Ground-1, [2.0], [3.0]; APPLE-1003, ¶84 (e.g., Sato's PDCR).

See Ground-2, [2.0],[3.0]; APPLE-1003, ¶¶113-115, 131, 135 (e.g., Asano's predecoders in combination with the LCBs determine a clock output according to the most significant address bit (e.g., first portion of the address)).

Claim 10-[10.0]: The method of claim 7, wherein each wordline driver in the selected group of wordline drivers has a shared address input to receive the second portion of the memory address.

See Ground-1, [6.1].

See Ground-2, [6.1]. Asano discloses that the final decoder applies the decoded second portion of the memory address (WL enable signal) the communication path 222 which is shared by each AND gate wordline driver in a group of wordline drivers. Ground-2, [6.1]; APPLE-1006, Figure 2, [0019]; APPLE-1003, ¶¶136-137.

Claim 11-[11.0]: A circuit device comprising: means for decoding a first portion of a memory address of a memory array;

See Ground-1, [1.2]; APPLE-1005, Figure 3, 5:25-31, 9:44-48, 11:54-56, Claim 1; APPLE-1003, ¶¶60-63, 71, 92-93. Sato's PDCR decodes a first portion of a memory address of a memory array. Ground-1, [1.2]; APPLE-1005, Figure 3,

5:25-31, 9:44-48, 11:54-56, Claim 1; APPLE-1003, ¶¶60-63, 71, 92-93. Sato's PDCR is an address decoder, which includes the same or equivalent structure as the "decoder" described in the '002 patent as set forth in Section I.D. *Id.*

See Ground-2, [1.2], APPLE-1006, Figure 2, [0016], [0018]-[0021]; APPLE-1003, ¶¶117-120, 138-140. Asano discloses a predecoder that decodes the most significant bit of an address to produce LCB selection signals. Ground-2, [1.2], APPLE-1006, Figure 2, [0016], [0018]-[0021]; APPLE-1003, ¶¶117-120, 138-140. Itoh discloses individual predecoder circuits which would have been obvious for a POSTIA to use in implementing Asano's predecoder. *Id.* A POSITA would have found it obvious to use, in the combination of Asano and Itoh, the same or equivalent structure as the "decoder" described in the '002 patent as set forth in Section I.D. *Id.*

[11.1]: means for selectively providing a clock signal to a selected group of wordline drivers based on the first portion of the memory address;

See Ground-1, [1.3], [2.0], [3.0]; APPLE-1005, 5:28-31, 10:36-39; APPLE-1003, ¶¶60-63, 71-72, 94-96. Sato discloses that the PDCR selectively provides a clock signal (ϕ_{ce}) to a selected group of wordline drivers based on the first portion (ax0-ax1) of a memory address. Ground-1, [1.3], [2.0], [3.0]; APPLE-1005, 5:28-31, 10:36-39; APPLE-1003, ¶¶60-63, 71-72, 94-96. Sato's PDCR is an address decoder, which includes the same or equivalent structure as the "conditional clock generator" described in the '002 patent as set forth in Section I.D. *Id.*

See Ground-2, [1.3], [2.0], [3.0]; APPLE-1006, Figure 2, [0016]-[0021]; APPLE-1003, ¶¶113-118, 132-133, 141-143. Asano discloses LCBs that together selectively provide a clock signal to a selected group of wordline drivers. Ground-2, [1.3], [2.0], [3.0]; APPLE-1006, Figure 2, [0016]-[0021]; APPLE-1003, ¶¶113-118, 132-133, 141-143. Asano's LCBs include the same or equivalent structure as the "conditional clock generator" described in the '002 patent as set forth in Section I.D. *Id.*

[11.2]: means for decoding a second portion of the memory address; and

See Ground-1, [1.4]; APPLE-1005, 5:16-24; APPLE-1003, ¶¶79, 97-98. Sato discloses that the decoding NAND gate circuits decode a second portion (ax2-axi) of a memory address. Ground-1, [1.4]; APPLE-1005, 5:16-24; APPLE-1003, ¶¶79, 97-98. Sato's decoding NAND gate circuit is an address decoder, which includes the same or equivalent structure as the "decoder" described in the '002 patent as set forth in Section I.D. *Id.*

See Ground-2, [1.4]; APPLE-1006, Figure 2, [0016]-[0017]; APPLE-1003, ¶¶110-111, 118, 122-123. Asano discloses that the predecoder decodes five of six address bits. Ground-2, [1.4]; APPLE-1006, Figure 2, [0016]-[0017]; APPLE-1003, ¶¶110-111, 118, 122-123. Itoh discloses individual predecoder circuits, which would have been obvious for a POSTIA to use in implementing Asano's predecoder. *Id.* A POSITA would have found it obvious to use, in the

combination of Asano and Itoh, the same or equivalent structure as the “decoder” described in the ’002 patent as set forth in Section I.D. *Id.*

[11.3]: means for activating a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

See Ground-1, [1.5]; APPLE-1005, 5:16-24, 5:66-6:44, 6:55-59; APPLE-1003, ¶¶82-83, 99-100, 105. Sato discloses that decoding NAND gate circuit provides an output (\overline{SO}) to a selected one of the wordline drivers in order to activate the wordline driver according to address signals ax2-axi. Ground-1, [1.5]; APPLE-1005, 5:66-6:44, 6:55-59; APPLE-1003, ¶¶82-83, 99-100, 105. Sato’s decoding NAND gate circuit is an address decoder, which includes the same or equivalent structure as the “decoder” described in the ’002 patent as set forth in Section I.D. *Id.*

See Ground-2, [1.5]; APPLE-1006, Figure 2, [0016]-[0017], [0019]; APPLE-1003, ¶¶119, 134, 147-149. Asano discloses that the final decoder determines which of the wordline drivers is to be enabled and generates a WL enable signal to activate the selected wordline driver. Ground-2, [1.5]; APPLE-1006, Figure 2, [0016]-[0017], [0019]; APPLE-1003, ¶¶119, 134, 147-149. Asano’s final decoder includes the same or equivalent structure as the “decoder” described in the ’002 patent as set forth in Section I.D. *Id.*

Claim 12-[12.0]: The circuit device of claim 11, wherein each of the wordline drivers is associated with a wordline of the memory array.

See Ground-1, [1.3], [6.0], [7.2] and Ground-2, [1.3], [6.0], [7.2].

Claim 13-[13.0]: The circuit device of claim 12, further comprising: a conditional clock generator including an address input to receive the first portion of the memory address and a clock input to receive a clock signal,

See Ground-1, [1.1], [2.0]. Sato's PDCR includes an input to receive the complementary internal address signals ax0-ax1. *See* APPLE-1005, 5:28-31, 9:52-59, 10:36-39, Figure 3; APPLE-1003, ¶¶65-66, 84. Thus, Sato discloses or renders this limitation obvious.

See Ground-2, [1.1], [2.0]. Like the '002 patent's conditional clock generator 110, Asano's LCBs include inputs to receive decoded address signals from a first portion of a memory address. *See* APPLE-1006, Figure 2, [0018], [0019], [0021]; APPLE-1003, ¶¶113-115. Thus, the combination of Asano and Itoh renders this limitation obvious.

[13.1]: the conditional clock generator to selectively apply the clock signal to one of a plurality of clock outputs according to the first portion of the memory address.

See Ground-1 and Ground-2, [1.3], [2.0]-[3.0].

Claim 14-[14.0]: The circuit device of claim 12, wherein the means for decoding a second portion of the memory address further comprises means for applying the second portion of the memory address to a shared address line.

See Ground-1, [1.4], [1.5], [6.1]; APPLE-1005, 5:43-21; APPLE-1003, ¶¶83, 86-91, 101-102. Sato discloses decoding NAND gate circuit applies a

second portion of the memory address (e.g., selection signal $\overline{S0}$) to an address line that is shared by four wordline drivers. Ground-1, [1.4], [1.5], [6.1]; APPLE-1005, 6:40-44; APPLE-1003, ¶¶83, 86-91, 101-102. Sato's decoding NAND gate circuit is an address decoder, which includes the same or equivalent structure as the "decoder" described in the '002 patent as set forth in Section I.D. *Id.* Thus, a POSITA would have recognized that the Sato decoding NAND gate circuits each include an output that applies the selection signal $\overline{S0}$ (e.g., second portion of the memory address) to an address line that is shared the wordline drivers (e.g., purple line in the annotated Sato Figure 3 shown in Ground-1 [6.1]). *Id.*

See Ground-2, [1.4], [6.1], [10.0]; APPLE-1006, Figure 2; APPLE-1003, ¶¶150-152. Asano discloses that the final decoder applies the decoded second portion of the memory address (WL enable signal) to the communication path 222 which is shared by each AND gate wordline driver in a group of wordline drivers. Ground-2, [1.4], [6.1], [10.0]; APPLE-1006, Figure 2; APPLE-1003, ¶¶150-152. Asano's final decoder includes the same or equivalent structure as the "decoder" described in the '002 patent as set forth in Section I.D. *Id.*

Claim 15-[15.0]: The circuit device of claim 12, wherein the circuit device comprises an integrated circuit.

Ground-1

Sato discloses that the entire RAM circuit of Figure 4, which includes the X address decoder and memory array, is "formed on one semiconductor substrate

such as single crystal silicon by known fabrication technique of CMOS integrated circuits.” APPLE-1005, 3:1-6.

Ground-2

Asano states that “all functions described herein may be performed in either hardware or software” including by “integrated circuits.” APPLE-1006, [0014].

Claim 16-[16.0]: The circuit device of claim 15, wherein the integrated circuit includes the memory array.

See Ground-1, [15.0].

See Ground-2, [15.0]; APPLE-1006, [0015] (Asano states that the “memory 200 comprises a predecoder 202, a final decoder 204, 32 wordline drivers 206 a first LCB 208, a second LCB 234, and a 64 wordline array 214.”). .

Claim 17-[17.0]: A circuit device comprising: an address input;

Ground-1

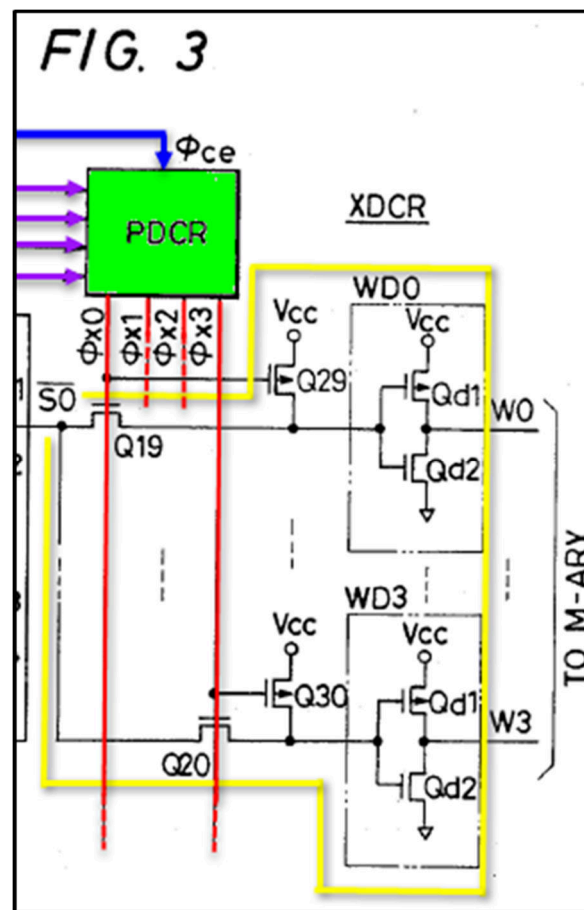
Sato discloses a circuit comprising an address input. *See e.g.*, Sato Figures 3 and 4 (internal address input (ax0-axi) to XDCCR); *see also* 3:50-4:11.

Ground-2

Asano discloses a memory with a six-bit address input. APPLE-1006, [0016] (“To begin the access cycle for the memory 200, an address is first received.”); *see also* Asano Figure 2; Ground-2, [1.0], [1.1], [1.4].

[17.1]: a plurality of clock outputs;

See Ground-1, [1.3] (describing outputs $\phi x0$ - $\phi x3$ (red-below) from Sato's PDCR as following the input timing (e.g., clock) signal ϕce); APPLE-1005, 5:25-31, 10:36-39; see also APPLE-1003, ¶65-72 ("because the input clock ϕce is applied to one of $\phi x0$ - $\phi x3$ outputs, a POSITA would have also understood the outputs to be clock outputs").



See Ground-2, [1.3] (explaining that the outputs of the LCBs are clock outputs); see also APPLE-1006, Claim 7 (reciting a wordline decoder with "a

plurality of local clock buffers (LCBs), wherein **each LCB** of the plurality . . . of LCBs is at least **configured to propagate clocking signals if enabled.**”).

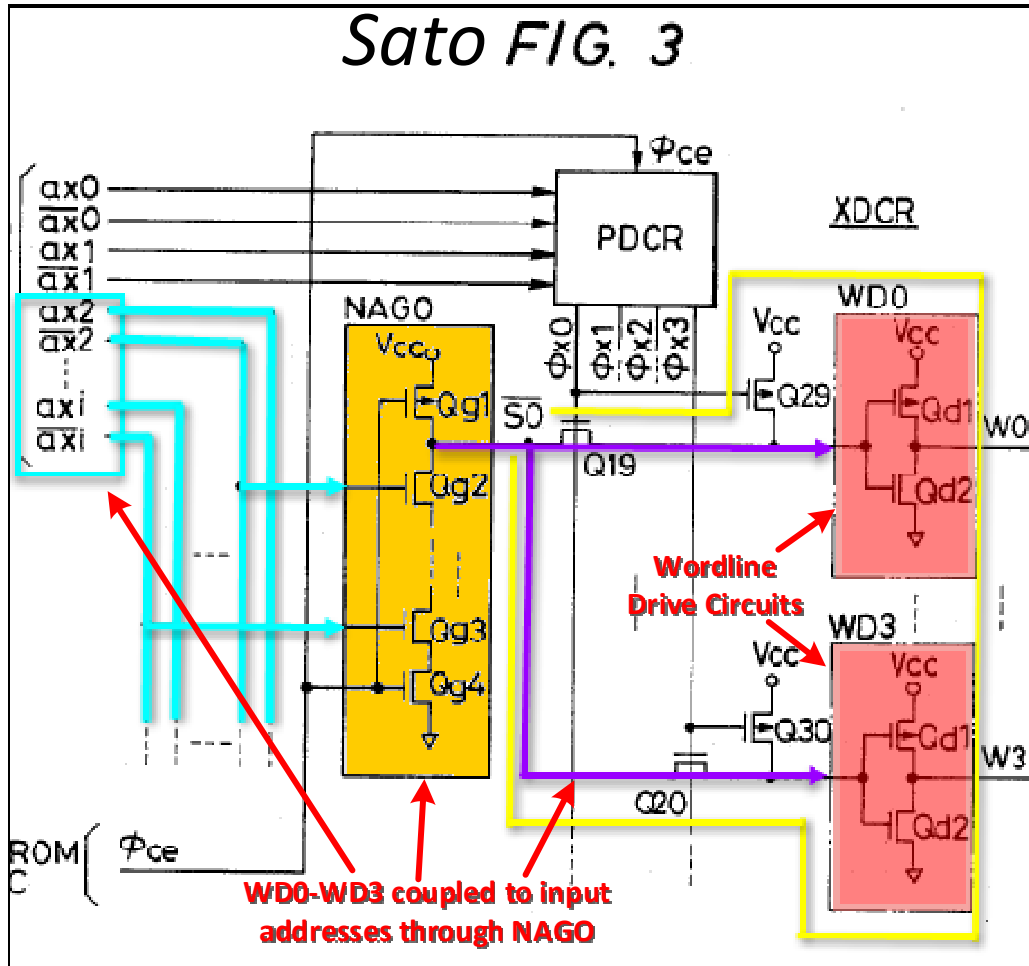
[17.2]: a group of wordline drivers coupled to a wordline of a memory array,

See Ground-1, [1.3]; APPLE-1005, Figure 3 (Each of Sato’s wordline drivers WD0-WD3 is coupled to a wordline W0-W3 of memory array M-ARY).

See Ground-2, [1.3]; Asano Figure 2 (each AND gate wordline driver is coupled to a respective wordline of the memory array).

[17.3]: each wordline driver of the group of wordline drivers coupled to the address input

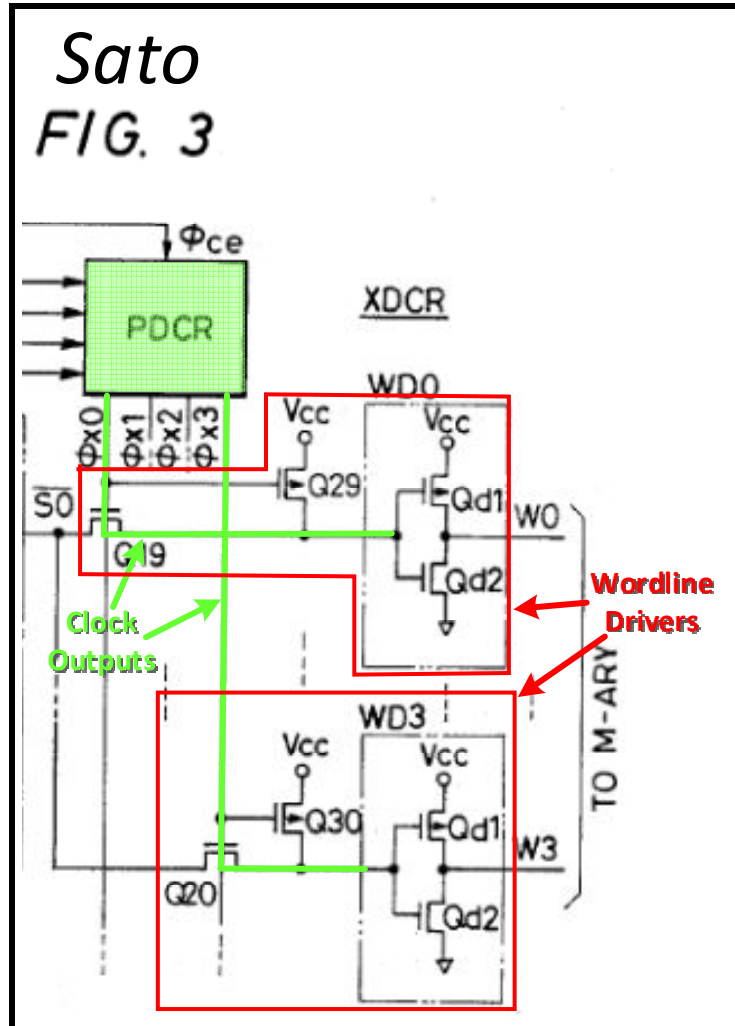
See Ground-1, [1.1], [1.5], [6.1]; APPLE-1005, Figure 3. Each of Sato’s wordline drivers WD0-WD3 is coupled to the address input (see below) through the decoding NAND gate circuit.



See Ground-2, [1.0], [1.1], [1.4] (Each of the AND gate wordline drivers is coupled to the address input through the latch, final decoder, and predecoder).

[17.4]: and [each wordline driver] coupled to a respective clock output of the plurality of clock outputs; and

See Ground-1, [1.3]; Sato Figure 3 (below), 9:60-10:4 (each outputs $\phi x0$ - $\phi x3$ (red) is coupled to one of the wordline drivers WD0-WD3 through a respective capacitance cut MOSFET Q19-Q20).



See Ground-2, [1.3]; Asano Figure 2 (Each AND gate wordline driver is coupled to an output of one of the LCBs). Asano also states at [0019] that “[t]he first AND gate 212 receives a clocking signal from the first LCB 208 through the fifth communication channel 228, while the second AND gate 236 receives a clocking signal from the second LCB 234 through the sixth communication channel 240.”

[17.5]: logic comprising: first logic . . . and second logic . . .

See Ground-1 and Ground-2, [1.0].

[17.6]: [the first logic] to receive a clock signal and a first portion of a memory address of the memory array,

See Ground-1 and Ground-2, [1.1], [13.0].

[17.7]: the first logic to decode the first portion of the memory address and

See Ground-1 and Ground-2, [1.2].

[17.8]: [the first logic . . .] to apply the clock signal to a selected clock output of the plurality of clock outputs; and

See Ground-1 and Ground-2, [1.3].

[17.9]: [the second logic] to decode a second portion of the memory address,

See Ground-1 and Ground-2, [1.4].

[17.10]: the second logic to selectively activate a particular wordline driver of the group of wordline drivers according to the second portion of the memory address.

See Ground-1 and Ground-2, [1.5].

Claim 18-[18.0]: The circuit device of claim 17, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state

Sato discloses, “the selected wordline driver of the group of wordline drivers is in an active evaluation state.” APPLE-1005, 3:65-4:2; APPLE-1003, ¶¶105-106.

Sato explains that the “XDCR is selectively actuated by the timing control signal ϕ_{ce} , [and] decodes the complementary internal address signals ax0-axi and sets one of the word lines designated by the X address signals AX0-AXi to the high level selection state.” APPLE-1005, 3:65-4:2. Therefore, when, as explained in

Ground-1, [1.5], a particular one of the wordline drivers (e.g., WD0) is selected and activated, the selected wordline driver is placed in an active evaluation state by asserting its associated wordline. APPLE-1003, ¶106.

[18.1]: wherein other wordline drivers of the group of wordline drivers are in a static precharge state.

Sato discloses, “other wordline drivers of the group of wordline drivers are in a static precharge state.” APPLE-1005, 9:65-10:55; APPLE-1003, ¶¶103-105. In reference to Figure 3, Sato explains that reset MOSFETs Q29-Q30—also referred to as “precharge MOSFETs” (*see* claims 12-16)—are turned ON when the corresponding selection signals ϕ_{x0} - ϕ_{x3} of the pre decoder PDCR are at the low logic level and the corresponding word line drive circuits are under the non-selection state.” APPLE-1005, 10:5-9. Each reset MOSFET pulls the input of its associated wordline driver to a high precharge voltage when the in the non-selection state. APPLE-1003, ¶104; APPLE-1005, 9:65-10:55. Moreover, “each reset MOSFET and corresponding capacitance cut MOSFET are turn ON complementarily” so that the voltage “level of the input terminal of each wordline drive circuit does not enter a floating state.” APPLE-1005, 10:18-22. Thus, Sato discloses that the non-selected wordline drivers are held at a high precharge voltage (i.e., precharge state).

Claim 19-[19.0]: The circuit device of claim 18, wherein a state of the wordline driver is determined by the selective application of the clock signal.

Sato discloses, “a state of the wordline driver is determined by the selective application of the clock signal.” APPLE-1005, 3:65-4:2, 6:40-59, 9:31-43, 9:65-10:27; APPLE-1003, ¶¶72, 103. Sato explains that the active one of the selection signals $\phi_{x0}-\phi_{x3}$ turns on one of the capacitance cut MOSFETs associated with a particular wordline driver allowing a selection signal ($\overline{S0}-\overline{Sk}$), generated by one of decoding NAND gate circuits, “to be transmitted to only the word line drive circuit corresponding to one word line that is designated by the X address signal $Ax0-Axi$.” APPLE-1005, 6:40-59, 9:31-43, 9:65-10:27; APPLE-1003, ¶¶72, 103-106. In other words, the selective application of input clock signal ϕ_{ce} to a particular one of PDCR outputs $\phi_{x0}-\phi_{x3}$ determines which one of the wordline drivers is activated by the active selection signal ($\overline{S0}-\overline{Sk}$). *Id.*; *see also* Ground-1, [1.3], [1.5], [17.1], [18.0].

Claim 37-[37.0]: The circuit device of claim 17, wherein the selected wordline driver of the group of wordline drivers is in an active evaluation state, wherein other wordline drivers of the group of wordline drivers are in a static precharge state, and

See Ground-1, [18.0]-[18.1] (this language is identical to claim 18).

[37.2]: wherein the logic comprises a conditional clock generator.

See Ground-1, [2.0].

Claims 20-28 and 31-36

Claims 20-28 and 31-36 simply restate and rearrange features previously addressed with respect to claims 1-7 and 10-14. Consequently, claims 20-28 and 31-36 are unpatentable for the same or similar reasons as those discussed *supra* with respect to Ground-1 and Ground-2, [1.0]-[7.4], [10.0]-[14.0].

IV. PAYMENT OF FEES – 37 C.F.R. § 42.103

Apple authorizes the Patent and Trademark Office to charge Deposit Account No. 06-1050 for the fee set in 37 C.F.R. § 42.15(a) for this Petition and further authorizes payment for any additional fees to be charged to this Deposit Account.

V. CONCLUSION

The cited prior art references identified in this Petition contain pertinent technological teachings (both cited and uncited), either explicitly or inherently disclosed, which were not previously considered in the manner presented herein, or relied upon on the record during original examination of the '002 patent. In sum, these references provide new, non-cumulative technological teachings which indicate a reasonable likelihood of success as to Petitioner's assertion that the Challenged Claims of the '002 patent are not patentable pursuant to the grounds presented in this Petition. Accordingly, Petitioner respectfully requests institution of an IPR for those claims of the '002 patent for each of the grounds presented

herein.

VI. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Petitioner, Apple Inc., is the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for inter partes review for the '002 patent. The '002 patent is the subject of a number of civil actions including: *ITC investigation Mobile Electronic Devices and Radio Frequency and Processing Components* (ITC-337-TA-1093) and *Qualcomm Inc. v. Apple Inc.*, 3:17-CV-02398 (S.D. Cal.).

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Apple provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

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Respectfully submitted,

Dated June 18, 2018

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,855 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated June 18, 2018

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on June 18, 2018, a complete and entire copy of this Petition for *Inter partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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