

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc.
Petitioner

v.

Qualcomm Incorporated
Patent Owner

Case IPR2018-01249
Patent 7,693,002

DECLARATION OF DR. MASSOUD PEDRAM

I, Massoud Pedram, do hereby declare:

1. I am making this declaration at the request of Qualcomm Incorporated (“Qualcomm” or “Patent Owner”) in the matter of the *Inter Partes* Review of U.S. Patent No. 7,693,002 (“the ’002 patent”).

2. I am being compensated for my work in this matter at my standard hourly rate of \$900 for consulting services. My compensation in no way depends on the outcome of this proceeding.

3. In preparing this Declaration, I considered the following materials:

a. The ’002 patent (Ex. 1001) and its file history (Ex. 1002);

- b. Petition for *Inter Partes* Review of U.S. Patent No. 7,693,002, IPR2018-01249 (Paper 2);
- c. The Declaration of Dr. Robert W. Horst (Ex. 1003);
- d. U.S. Patent No. 4,951,259 to Sato (Ex. 1005) (“Sato”);
- e. U.S. Patent Pub. No. 2006/0098520 to Asano (Ex. 1006) (“Asano”);
- f. Kiyoo Itoh, VLSI Memory Chip Design, Springer 2001 (Ex. 1007) (“Itoh”);
- g. U.S. Patent No. 5,602,796 to Sugio (Ex. 1012);
- h. U.S. Patent No. 5,291,076 to Bridges (Ex. 1008);
- i. Decision - Institution of *Inter Partes* Review (Paper 6);
- j. IEEE Dictionary (Ex. 2002);
- k. Additional portions of Itoh (Ex. 2003) not included in Petitioner’s Ex. 1007; and
- l. Any other materials referenced herein.

I. Professional Background

4. I am a Professor of Electrical Engineering and Charles Lee Powell Chair in Electrical Engineering and Computer Science in the Viterbi School of Engineering at the University of Southern California (USC). From 2013 until early 2017 I held the Stephen and Etta Varra Professorship in the Viterbi School of Engineering at USC.

5. I am an expert on electronic design automation (EDA), Very Large Scale Integration (VLSI) design including digital integrated circuits and semiconductor memory, energy efficient design, hybrid electrical energy storage

systems (HEESS), and power/thermal modeling and management in integrated circuits and systems including multiple-supply-voltage designs and power collapsing techniques and voltage regulation. I also have expertise in building, validating, and delivering voltage regulation and conversion and management circuits and, more generally, nano-electronic circuits and system-on-chip designs targeting applications ranging from high performance computing to low-power embedded computing.

6. I earned my B.S. in Electrical Engineering from the California Institute of Technology in 1986. I earned my M.S. in Electrical Engineering and Computer Sciences from the University of California at Berkeley in 1989. During my Masters and Doctoral degree programs, I was a Graduate Student Researcher in the Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley from 1986-1991. Concurrently I held a part-time Research Position, at the Xerox Palo Alto Research Center (“Xerox PARC”) from 1987-1989. I then earned my Ph.D. in Electrical Engineering and Computer Sciences from the University of California at Berkeley in 1991.

7. After receiving my doctorate, I was an Assistant Professor in the Department of Electrical Engineering at USC from 1991-1996. I was then an Associate Professor in the Department of Electrical Engineering at USC from 1996-2000. After that I have been a Professor of Electrical Engineering and

Computer Science in the Viterbi School of Engineering at the University of Southern California (USC).

8. I am a named inventor on ten U.S. patents and a U.S. patent application. These patents relate to topics ranging from novel address bus encoding techniques to charge recycling based multi-threshold CMOS design, and from low leakage SRAMs to dynamic backlight scaling for power minimization. The recently-filed patent application focuses on design and implementation of a superconductive Field Programmable Gate Array (FPGA) fabric.

9. I have (co-) published four books and more than 650 archival and conference papers and book chapters. My research ranges from computer-aided design techniques and tools targeting VLSI circuit and system design to FPGA fabric design and FPGA synthesis, from low power electronics and battery-powered embedded system design to power distribution, conversion and regulation. For this research, my students and I have received ten conference and journal Best Paper awards.

10. In addition to my work at Xerox PARC, I have been a member of multiple technical and scientific advisory boards for high-tech companies, including EPIC Design, Magma Design Automation, and Atrenta Inc., all of which went on to have successful initial public offerings (IPOs) or were acquired.

11. I have served as the (lead) principal investigator on many US government (including the National Science Foundation, the Defense Advanced Research Projects Agency, U.S. Department of Defense, and the Intelligence Advanced Research Projects Activity) and private industry (including the Semiconductor Research Corporation) research projects, for some of which I have been the lead investigator of a team comprised of tens of faculty, students, and industry collaborators.

12. I was a recipient of the 1996 Presidential Early Career Award for Scientists and Engineers, and in 2000 I was selected as a Fellow of the IEEE and in 2008 named as an ACM Distinguished Scientist.

13. I received the 2015 IEEE Circuits and Systems Society Charles A. Desoer Technical Achievement Award for my contributions to modeling and design of lower power VLSI circuits and systems, and energy efficient computing.

14. I was recognized as the Third Most Cited Author at the 50th anniversary of the Design Automation Conference, Austin, TX, in June 2013. I received a Top Three Author Award at the 20th Anniversary Asia and South Pacific Design Automation Conference, Chiba/Tokyo, Japan, in January 2015, and was named as the Second Most Prolific and Second Most Cited Author at the 20th Anniversary International Symposium on Low Power Electronics and Design, Rome, Italy, in July 2015.

15. I received the USC Viterbi School of Engineering Senior Research Award in 2017.

16. Since July 2012, I have been the Executive Committee Chair of the IEEE/ACM International Symposium on Low Power Electronics and Design, a technical conference which I co-founded in 1996.

17. I was the Editor-in-Chief of the ACM Transactions on Design Automation of Electronic Systems from June 2008-May 2014. I was also the Inaugural Editor-in-Chief of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems from January 2010-December 2013.

18. I served as the VP of Publications and Chair of the Distinguished Lecturer Program of the IEEE Circuits and Systems Society in 2005-2006 and 2003-2004, respectively. I served as a member of the Board of Governors, IEEE Circuits and Systems Society in 2000-2003. I served as the Technical Program Chair of the International Symposium on Low Power Electronics and Design, Monterey, CA, in August 1996 and the International Symposium on Physical Design, Del Mar, CA, in April 2002. I also served as the General Chair of the International Symposium on Low Power Electronics and Design, Monterey, CA, in August 1997, the International Symposium on Physical Design, Monterey, CA, in April 2003, and the International Symposium on Quality of Electronic Design, San Jose, CA, in April 2007.

19. My curriculum vitae is attached to this declaration as Appendix A.

II. Relevant Legal Standards

20. I have been asked to provide my opinion as to whether claims 1-28 and 31-37 of the '002 patent would have been obvious to a person of ordinary skill in the art ("POSA") at the time of the invention, in view of the alleged prior art.

21. I am an engineer by training and profession. The opinions I am expressing in this Declaration involve the application of my engineering knowledge and experience to the evaluation of certain alleged prior art with respect to the '002 patent. Aside from my experience in litigation support, my knowledge of patent law is no different than that of any lay person. Therefore, I have requested the attorneys from Jones Day, who represent Qualcomm, to provide me with guidance as to the applicable patent law in this matter. The paragraphs below express my understanding of how I must apply current principles related to patentability.

22. It is my understanding that in determining whether a patent claim is obvious in view of the alleged prior art, the Patent Office must construe the claim by giving the claim its broadest reasonable interpretation consistent with the specification as it would have been understood by one of ordinary skill in the art. For the purposes of this review, I have construed each claim term in accordance

with its plain and ordinary meaning under the required broadest reasonable interpretation.

23. It is my understanding that a claim is unpatentable under 35 U.S.C. § 103 if the claimed subject matter as a whole would have been obvious to a POSA at the time of the invention. I also understand that an obviousness analysis takes into account the scope and content of the prior art, the differences between the claimed subject matter and the prior art, and the level of ordinary skill in the art at the time of the invention.

24. In determining the scope and content of the prior art, it is my understanding that a reference is considered appropriate prior art if it falls within the field of the inventor's endeavor. In addition, a reference is prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

25. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires the claimed invention be considered as a whole. This "as a whole" assessment requires showing that one of ordinary skill in the art at the time of invention, confronted by the same

problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

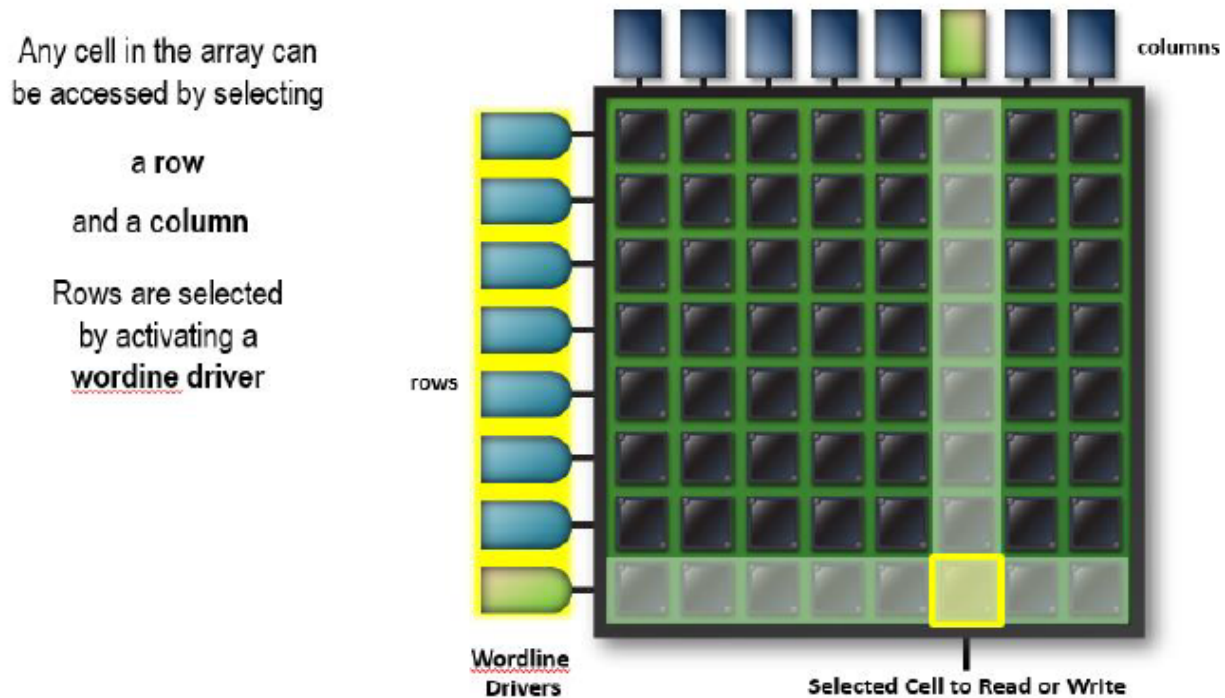
26. It is my further understanding that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; a predictable use of prior art elements according to their established functions; applying a known technique to a known device (method or product) ready for improvement to yield predictable results; choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

III. THE '002 PATENT

A. Technology Background and Overview of the '002 Patent

27. The '002 patent generally relates to circuits and methods for accessing memory arrays in integrated circuits. The title of the patent is “Dynamic Word Line Drivers and Decoders for Memory Arrays.”

28. Random Access Memory (RAM) is generally organized into rows and columns, as shown in the following image:



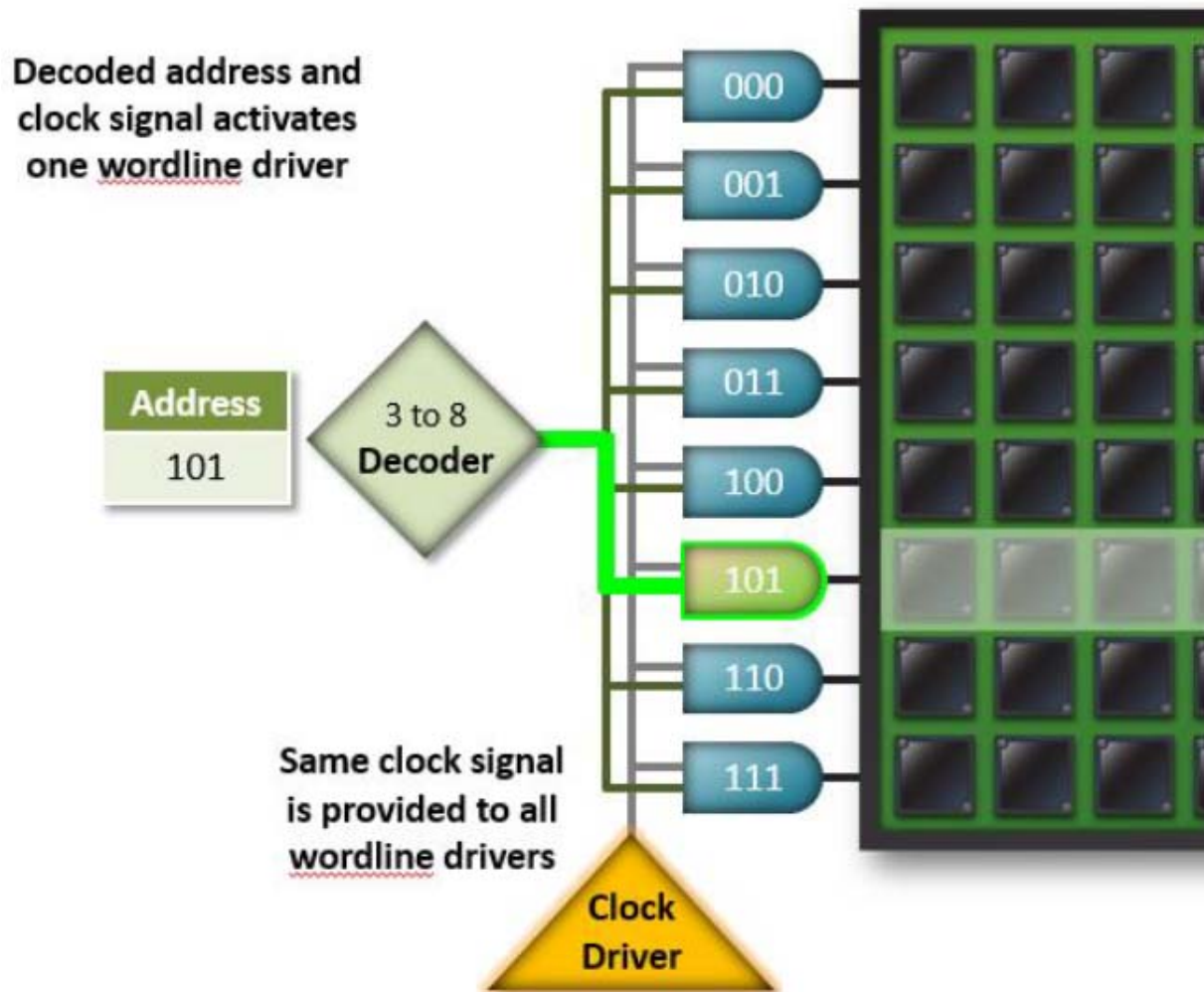
29. Cells are read from or written to by activating a wordline driver, which selects the appropriate row, and then using bitlines to either read from or write to a particular column. The cell that is in the row selected by the wordline driver and in the column selected by the bitline is the cell that is read from or written to.

30. A cell in a memory array is addressed using a memory address, which can be split into a row address and a column address. Wordlines are selected by decoding the row address, and bitlines are selected by decoding the column address. Because the '002 patent discloses structures and methods for activating wordlines

of a memory array, the relevant memory address for purposes of the '002 is the row address.

31. SRAM (static random access memory) is used on processor chips to implement caches and scratchpad memory. SRAM, which is organized as a two-dimensional array of memory cells comprising row and columns, stores bits in a cross-coupled inverter pair configuration with two access transistors within an integrated circuit. Dynamic random-access memory (DRAM) is a type of storage that is widely used as the main memory for a computer system. DRAM, which is also organized as a two-dimensional memory array, stores each bit of data in a separate capacitor with a single access transistor within a DRAM chip. SRAM cells are bigger than DRAM cells (which explains the much higher density of DRAM storage) but have much lower access latency (mainly because they are on-chip.) Both SRAM and DRAM requires row and column address decoders to translate addresses to a desired group of bits (one word of 32 or 64 bits of data in case of caches, one block of 4 to 8 words in case of main memory) within the memory array. DRAM cells require periodic refresh to avoid data loss to leakage. SRAM cells do not require refresh since data is stored in a cross-coupled pair of inverters. Both SRAM and DRAM are examples of volatile memory, meaning that data is lost once power is removed.

32. One method of activating a particular wordline driver of a memory array that the '002 patent discloses was in the prior art was to decode the entire row address at once and use the decoded signal, along with a clock signal, to activate a particular wordline driver. For example, the following simplified figure shows how a three-bit address can be decoded in a 3-to-8 bit decoder to activate a particular wordline driver when that decoded signal is combined with the output of a clock driver:



33. Some disadvantages of using such a decoding scheme to activate wordline drivers include high power consumption and reduced access speed. Each wordline driver has an input capacitance that the clock driver must drive. Because most of the wordline drivers are not used, this scheme results in wasted power. In addition, because the clock driver needs to drive a relatively large capacitive load, the SRAM access time will be increased. Moreover, a full decoder would need to be larger to decode a desired number of address bits. For example, a full row address decoder for 6 bits will have to do a 6-to-64 bit decoding to generate 64 decoded row line addresses, whereas a split row address decoder with 3-bit pre-decoding will have to do a 3-to-8 bit decoding to generate decoded addresses for eight groups of row addresses followed by eight other 3-to-8 bit decoders to pick the desired row address within a selected group. The logic realization cost of the latter design is much less than that of the former. The larger the decoder necessary to decode the row address, the more power it consumes, the more time it takes to decode the address, and the more area is needed to implement the decoder in silicon.

34. The '002 patent discloses improved structures and methods of activating a wordline driver that save power and increase the maximum speed of the circuit by providing a clock signal to only a selected group of wordline drivers, rather than all wordline drivers and address decoders. The patent discloses splitting

the address into two portions. Each address portion is decoded separately. A first logic decodes the first portion of the memory address, and a second logic decodes the second portion of the memory address. The first logic also receives a clock signal and applies the clock signal to selected clock output of a plurality of clock outputs. Each of the clock outputs is associated with a group of the wordline drivers. Only one of the clock outputs is selected at any time, which means only one group of wordline drivers is selected. The second logic decodes the second portion of the memory address and selectively activates a particular wordline driver according to the second portion of the memory address.

35. An advantage of the patented circuit device of the '002 patent is that a timing delay from the clock to the activation of a particular wordline is reduced. The first and second logics operate independently of each other and apply their respective outputs directly to wordline drivers in parallel, thus reducing a timing delay in providing the clock signal to a particular wordline driver. Still another advantage is that capacitive loading on the clock driver is reduced, thereby lowering power dissipation of the clock driver. Another advantage is that use of a conditional clock to apply a clock signal to a selected group of wordline drivers reduces power consumption of an address decoder of a memory device.

B. Prosecution History of the '002 Patent

36. I have reviewed the prosecution history of the '002 patent. See Ex. 1002. The following is a summary of key events.

37. The initial application (Application No. 11/548,132) was filed on October 10, 2006. Ex. 1002 at 257-91.

38. In a November 19, 2007 Office Action (Ex. 1002 at 226-35), claims 2, 3, 5, 6, 10, 13, 14, 19-21, 23 and 24 were objected to as being dependent upon a rejected base claim, but the examiner indicated that they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The examiner rejected (i) claims 1, 4, 7-9, 11, 12, 15, and 16 under § 102(b) as allegedly being anticipated by Iwahashi (U.S. Patent 6,856,574), (ii) claims 17 and 18 under § 102(b) as allegedly being anticipated by Sugio (U.S. Patent 5,602,796), and (iii) claims 22 and 25 under § 102(b) as allegedly being anticipated by Kato (U.S. Patent Application 2001/0015926).

39. Applicant filed an amendment on February 19, 2008. Ex. 1002 at 193-212. The only amendments to the rejected claims were minor and made to overcome an objection and fix a typo. Applicant added thirteen new claims, with the new claims including previously objected to claims rewritten in independent form. Applicant argued that the cited references did not anticipate any of the claims.

40. On April 28, 2008, the examiner issued a restriction requirement (Ex. 1002 at 181-85), asserting that certain claims were directed to addressing (Species I, claims 1-16, 22-25, 28-35, 39 and 40), while others were directed to particular wordline drivers (Species II, claims 17-21, 26, 27 and 36-38). On May 20, 2008, in response to the restriction requirement, the Applicant elected Species I. Ex. 1002 at 179-80.

41. In a July 30, 2008 non-final rejection (Ex. 1002 at 160-66), the examiner rejected claims 22-25, 39, and 40 under § 102(b) as allegedly being anticipated by Iwahashi. The examiner allowed all other pending claims and noted that the prior art did not disclose a second logic to decode a second portion of the memory address to selectively activate a particular wordline driver.

42. Applicant filed an amendment on December 6, 2008. Ex. 1002 at 141-55. In this amendment, claims 22 and 39 were amended to recite limitations directed to the second logic. Applicant also added eight new claims. Seven of the new claims depended from claims noted to be allowable by the Office. New claim 48 was independent.

43. In a January 28, 2008 final rejection, the examiner found that all pending claims were allowable, except for independent claim 48. Ex. 1002 at 120-26. Applicant subsequently canceled this claim in an amendment filed March 19, 2009. *Id.* at 106-16.

44. On April 2, 2009, the Office issued a notice of allowance. Ex. 1002 at 85-88. On June 4, 2009, Applicant filed a request for continued examination (RCE) with an information disclosure statement listing Watanabe (U.S. Patent 7,092,305). *Id.* at 64-83.

45. In a non-final rejection dated June 17, 2009, the examiner rejected claims 7-10, 11-16, 22, 25, and 46 under § 102(b) as allegedly being anticipated by Watanabe. Ex. 1002 at 40-46. The examiner stated that claims 1-6, 28-35, 39, and 40 were allowable over the prior art and noted that the prior art did not disclose “second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address,” among other limitations. Applicant subsequently filed an amendment on September 15, 2009 to amend rejected claims 7, 11, and 22 to include this allowable subject matter and thus overcome the rejections. *Id.* at 25-38.

46. The Office issued a second notice of allowance on November 11, 2009. Ex. 1002 at 15-18. A March 10, 2010 Issue Notification states that the patent has a PTA of 0 days. *Id.* at 9-10.

47. A Certificate of Correction issued July 5, 2011 corrects typographical errors. Ex. 1002 at 1-4.

C. Level of Skill in the Art

48. I understand that Petitioner has proposed that a person of ordinary skill in the art relevant to the '002 patent would have had at least an undergraduate degree in electrical engineering, or a related field, and three years of experience in the design of memory systems and circuits. Petition at 2. Petitioner has also proposed that a person of ordinary skill with less than the amount of experience noted above would have had a correspondingly greater amount of educational training such as a graduate degree in a related field. *Id.*

49. I further understand that for purposes of its Institution Decision (“the Decision”), the USPTO’s Patent Trial and Appeal Board (“the Board”) accepted the assessment of the POSA offered by Petitioner, with the exception of the language “at least.” Institution Decision at 6.

50. I do not dispute Petitioner’s proposed level of ordinary skill in the art as modified by the Board.

51. It is my understanding that when interpreting the claims of the '002 patent, I must do so based on the perspective of one of ordinary skill in the art at the relevant priority date. I understand that the '002 patent has a priority date as of its filing date, October 10, 2006, and so I have interpreted the claims of the '002 patent based on the perspective of the POSA as of that date.

D. Claim Construction

52. It is my understanding that in determining whether a patent claim is obvious in view of the prior art, the Patent Office must construe the claim by giving the claim its broadest reasonable interpretation consistent with the specification. For the purposes of this review, I have construed each claim term in accordance with its plain and ordinary meaning under the required broadest reasonable interpretation, as a person having ordinary skill in the art would understand. In my opinion, the claim term “clock signal” is in need of construction, and I provide my interpretation of this term below. I also address Petitioner’s proposed constructions below.

“clock signal”

53. The term “clock signal,” as recited in each of the independent claims of the ’002 patent, should be interpreted to mean “a periodic signal used for synchronization.” This interpretation is consistent with the plain and ordinary meaning of the term as understood by the POSA. The POSA’s understanding of the term is reflected, for example, by the IEEE Dictionary, which defines the term “clock signal” as “[a] periodic signal used for synchronizing events.” Ex. 2002 at 9. The IEEE Dictionary is a reliable, unbiased authority, and in my opinion, it sets forth the definition of clock signal that would be understood by the POSA as of the filing date of the ’002 patent.

54. Support for this interpretation is also found in the '002 patent itself. Specifically, the POSA would understand that the '002 patent describes a synchronous memory system that uses a periodic clock signal. It does not describe an asynchronous memory system that uses multiple, non-periodic timing signals. The POSA would understand that the non-periodic timing signals of an asynchronous memory system are different than the periodic clock signal of a synchronous memory system. This is explained in detail below.

55. Conventional SRAM and DRAM (RAM for short) are controlled asynchronously. Therefore, the memory latency and data toggle rate can be some fractional number of CPU clock cycles. More importantly, what makes the RAM asynchronous is that externally provided command inputs control latches and I/O buffers/drivers internal to RAM, and those external command inputs can arrive at the RAM's pins at any time. Since asynchronous RAM does not operate based on any kind of periodic system clock that it shares with the CPU, the timings of the control signals, addresses, and data have to be consciously taken into account. In such asynchronous systems, where pulses or strobe signals are used to activate certain portions of the circuitry, the timing and duration of such signals must be explicitly specified. Furthermore, in such systems, the characteristics of the circuitry generating these timing signals must be clearly specified.

56. Asynchronous static RAMs (SRAMs) respond to asynchronous changes at the device's address pins by generating multiple internal timing signals that are used to orchestrate the operation of the SRAM's internal circuitry during a read or a write operation. Essentially, this means that there exists some control logic circuitry in the asynchronous SRAM that can asynchronously accept externally asserted control signals, read row and column addresses, and then generate appropriately timed sequences of internal timing signals (in the form of pulses or strobe signals) to direct the movement of data onto, within, and off of the SRAM. The external interface to the control logic on the asynchronous SRAM consists of essentially two signals: the active-low chip-select (CS#)¹ and the active-low write enable (WE#). Various timing constraints among the external control signals and address/data signals must be satisfied in order to ensure correct operation.² The duration and precise timing of internal timing signals is also key to

¹ In this declaration, the # symbol after a signal name means the complemented (active-low) form of the signal. For example, CS# (which is the same as CS_bar) indicates that the chip is selected when the value of the chip select signal CS is low.

² Typical timing specs for asynchronous SRAMs include many complicated requirements on and/or among external input/output signals. Examples include requirements on maximum access times from address and CS# low to data valid, maximum output disable times after CS# high, minimum write pulse width, minimum address setup time with respect to WE# low, minimum address hold time with respect to WE# high, minimum CS# setup time with respect to WE# high, minimum data setup and hold times with respect to WE# high, minimum output data valid after address change, and so on.

the correct operation of the device. Guaranteeing that the controller can successfully orchestrate various activities within the asynchronous SRAM under subtle process-voltage-temperature (PVT) variations is an intricate task, which becomes ever more daunting as the access latencies are shortened and supply voltages are reduced. Asynchronous SRAMs thus run into limitations at the high end of the performance range.

57. Asynchronous dynamic RAM (DRAM) devices likewise contain control logic circuitry to direct the movement of data onto, within, and off of the DRAM device. The control logic accepts externally asserted control (command) signals and then orchestrates precisely timed sequences of internal control signals to direct the movement of data. The external interface to the control logic comprises active low Row Address Strobe (RAS#), active low Column Address Strobe (CAS#), and active low Write Enable (WE#).

58. In an asynchronous DRAM device, the logic control circuitry and an external memory controller directly control the movement of data. Moreover, the external interface is an asynchronous interface. The direct control of the internal circuitry of the DRAM device by the external memory controller means that the DRAM device cannot be well pipelined, and new commands to the DRAM device cannot typically be initiated until the previous command completes the movement of data. The movement of data is measured and reported by DRAM manufacturers

in terms of nanoseconds. The asynchronous nature of the interface means that each time a new DRAM device is introduced, a new and different memory controller has to be developed. This fact also gives rise to a complex set of timing constraints that must be satisfied by the DRAM device.³

59. The following diagram illustrates aspects of asynchronous memory systems:

³ Typical timing specs for asynchronous DRAMs include many complicated requirements on and/or among external input/output signals. Examples include requirements on maximum data access times from RAS# low and CAS# low, maximum output disable time from CAS# high, minimum RAS# high (precharge) and low (access) durations, minimum CAS# high (precharge) and low (access) durations, minimum write pulse duration, minimum row address setup and hold times with respect to RAS# low, minimum column address setup and hold times with respect to CAS# low, minimum and maximum delays from RAS# low to CAS# low and from RAS# low to WE# low, minimum Read command setup time, minimum Write command hold times from RAS# and CAS#, minimum data hold times after RAS#, CAS#, and WE#, and so on.

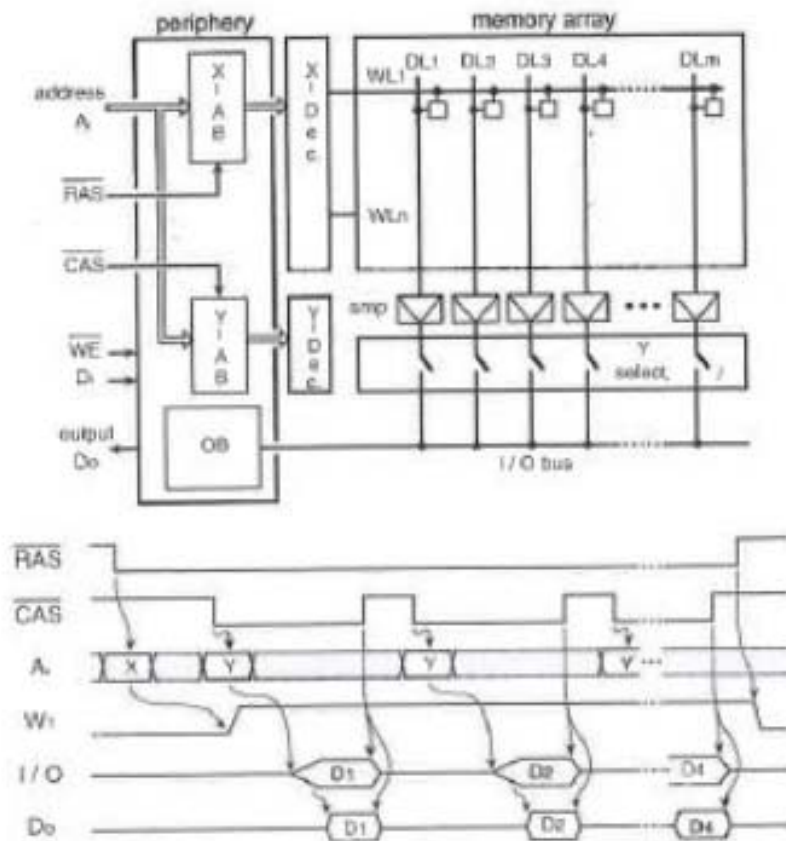


Fig. 6.14. The asynchronous operation of a DRAM chip [6.8]. AB, address buffers; OB, data-output buffer; X, row; Y, column

Ex. 2003 (Itoh) at 18. In the asynchronous operation of the DRAM chip depicted above, periodic clock signals are not used. Rather, the system is event-driven based on multiple, non-periodic timing signals RAS#, CAS#, and WE#. The timing signals RAS#, CAS#, and WE# are pulses or strobes without a periodic component. Internal activities of the DRAM chip (e.g. activation of a selected wordline (for example, W₁) and appearance of data on I/O bus following the sensing of the data stored in a selected memory cell (D₁...D₄)) are initiated by asynchronous transitions on RAS# and CAS#. The delay between values appearing

on the I/O bus and the output signals D0 are not synchronized with any transitions on CAS# or RAS#. Indeed, this delay can only be reported in units of nanoseconds, rather than in multiples of a system clock cycle. Finally, the RAS# and CAS# timing signals are not referred to as clock signals, as seen above.

60. The POSA would understand that asynchronous systems do not use a periodic clock signal – rather, they use multiple, non-periodic timing signals, such as the RAS# and CAS# strobe signals shown above. As explained below, synchronous systems, by contrast, use a periodic clock signal, with all events being synchronized to the periodic signal.

61. An alternative to asynchronous memory is to make the RAM interface synchronous, such that requests can only arrive at regular intervals of a periodic clock signal. This allows the latches internal to the RAM to be controlled by a common, periodic system clock signal. The primary benefit of synchronous RAM, or synchronizing RAM operation with the CPU clock, is that it improves the predictability of event timing—put simply, events such as the arrival of commands or the driving of output data either occur in synchrony with the periodic clock, or they do not occur. Stated differently, synchronous RAM drives internal activities (row select, column select, data read-out, or data write) by a periodic clock, as opposed to the non-periodic RAS#, CAS#, and WE# timing signals.

62. The following diagram illustrates aspects of synchronous memory systems:

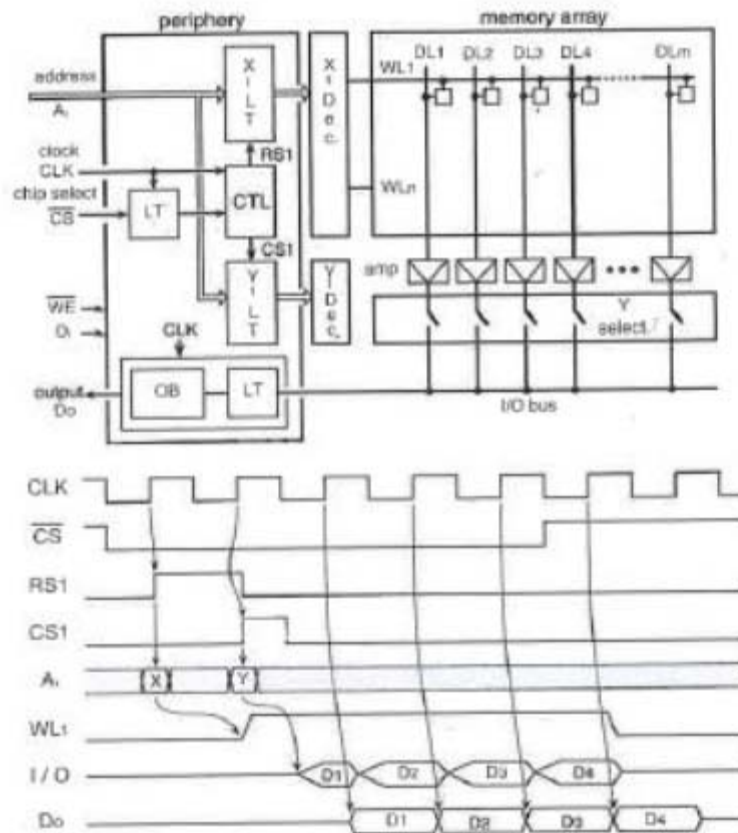


Fig. 6.15. The synchronous operation of a DRAM chip [6.8]. LT, latch; CTL, control circuit; OB, data-output buffer

Ex. 2003 (Itoh) at 19. In the synchronous system depicted above, a periodic clock signal “CLK” is used, and all events occur in synchrony with the periodic clock signal CLK. In particular, a row address strobe signal RS1 is generated from the CS# signal at the rising edge of the CLK so that row addresses are strobed and the corresponding wordline (for example, WL1) is activated. The resulting cell signals on m data lines are amplified. On the other hand, a column address strobe signal

CS1 is generated by the next rising edge of the CLK so that the column addresses are strobed and the amplified signal on the corresponding bitline (for example, DL1) is outputted on the common I/O bus line. Then, the data output Do is available from the chip synchronously with the succeeding CLK, resulting in a two-cycle latency for the read operation. Notice that, as Itoh also points out, synchronous operation can even eliminate the roles of RAS# and CAS# which are used in asynchronous operation, since the same functions are carried out by the internally generated clock-synchronous signals RS1 and CS1.

63. The fastest SRAMs are synchronous. Synchronous SRAMs use an external synchronizing clock to time the operation of SRAM's internal circuitry based on externally provided control signals such as CS# and WE#. Control signals and address/data signals of synchronous SRAMs are synchronized with respect to this clock and must be valid when the triggering (active) clock edge occurs (i.e., satisfy setup and hold time constraints). In other words, all read and write operations start on the triggering edge(s) of the clock and complete in synchrony with the clock. Because of the simpler timing constraints which enable improved timing control,⁴ access latencies and clock cycle times can be reduced to match the

⁴ Typical timing specs for synchronous SRAMs include, for example, requirements on setup and hold times of address and CS# with respect to the triggering edge of the clock (CK), setup time of WE# with respect to the triggering edge of CLK, setup and hold times of write data with respect to the triggering edge

clock cycles of the fastest microprocessors. Indeed, all access latencies are described in terms of number of cycles of a shared synchronizing clock signal (CK). Finally, the synchronous control logic circuits can be designed to support pipelining naturally, and the ability to support pipelining greatly increases the sustainable bandwidth of the synchronous SRAMs. Because of easier-to-meet timing constraints in synchronous SRAMs, timing margins in view of PVT variations are improved, which in turn enables higher speed of operation.

64. Similarly, in synchronous DRAMs, all timing requirements (e.g., setup and hold time constraints) on command inputs (RAS#, CAS#, WE#, and CS#) and row and column addresses are described with respect to the triggering edge(s) of the clock signal. Furthermore, all access latencies are described in terms of cycle (or half-cycle) counts of this same clock for single (or dual) data rate synchronous DRAM devices.

65. The POSA would understand that the '002 patent discloses a synchronous memory system that uses a periodic clock signal. Indicia of this can be found in the fact that the patent does not describe a timing generator circuit to generate various internal timing signals in response to externally provided control

(continued...)

of CK. Furthermore, the access latency to read data is also in terms of the cycle counts of the CLK.

signals (such as CS# and WE#). If the '002 patent invention disclosed an asynchronous memory system, it would need multiple precisely timed internal timing signals to be generated in response to CS# going low and the appearance of new row and/or column addresses. These signals would then have to be used to initiate bitline precharging, cause activation of wordline drivers, enable bitline sensing or data writing, and enable output drivers for read operation (or input buffers for write operation) etc. Yet such multiple timing signals are not disclosed by the '002 patent. These internal timing signals are needed for correct operation of an asynchronous memory, but they are generally not employed in synchronous memory systems that use a periodic clock signal.

66. Moreover, the '002 patent does not describe any timing considerations respecting address and data bits on one hand and externally provided (asynchronous) control signals on the other. These timing constraints, as described above, are important considerations in asynchronous memory systems, but no such timing constraints exist in synchronous memory systems. Further, a POSA would understand that all operations of the memory system of the '002 patent are synchronized by a single, periodic clock signal, consistent with what is found in synchronous systems. The '002 patent would not make sense to a POSA in the context of the clock signal being an asynchronous timing signal.

67. The '002 patent starts off by describing memory systems that operate with a clock and place a heavy load on the clock. For example, the '002 patent describes memory systems that require the clock to drive multiple wordline drivers and multiple address decoders, and therefore place a large electrical load on the clock. '002 patent, 1:11-16. The inventive solution of the '002 patent is to have (i) a first logic that decodes a first portion of a memory address, and (ii) a second logic that decodes a second portion of the memory address. The first logic further receives the clock signal and applies the clock signal to a selected clock output associated with a group of wordline drivers, whereas the second logic selectively activates a particular wordline driver. The clock signal thus drives only certain wordline drivers, rather than all of them, thus reducing a load on the clock signal, a timing delay from the clock to a selected wordline, and clock power consumption. *Id.* at 1:64-66 and 2:2-12.

68. The above description means that the memory system is a synchronous one, relying on the synchronizing action of a clock signal. Precisely the fact that the clock signal is directly sent to address decoders and wordline drivers implies that the target memory system is synchronous, and its pipeline depth is at least two clock cycles. See, e.g., Ex. 2003 (Itoh) at 21, reproduced below, showing that in a synchronous memory system, the memory access time can be expressed as an integer multiple of the system clock cycle, and all the

relevant signals need to be synchronized with only one system clock. Thus, it is enough for system designers to pay attention only to the set-up and hold time for one clock without paying any attention to the phase relations between various signals.

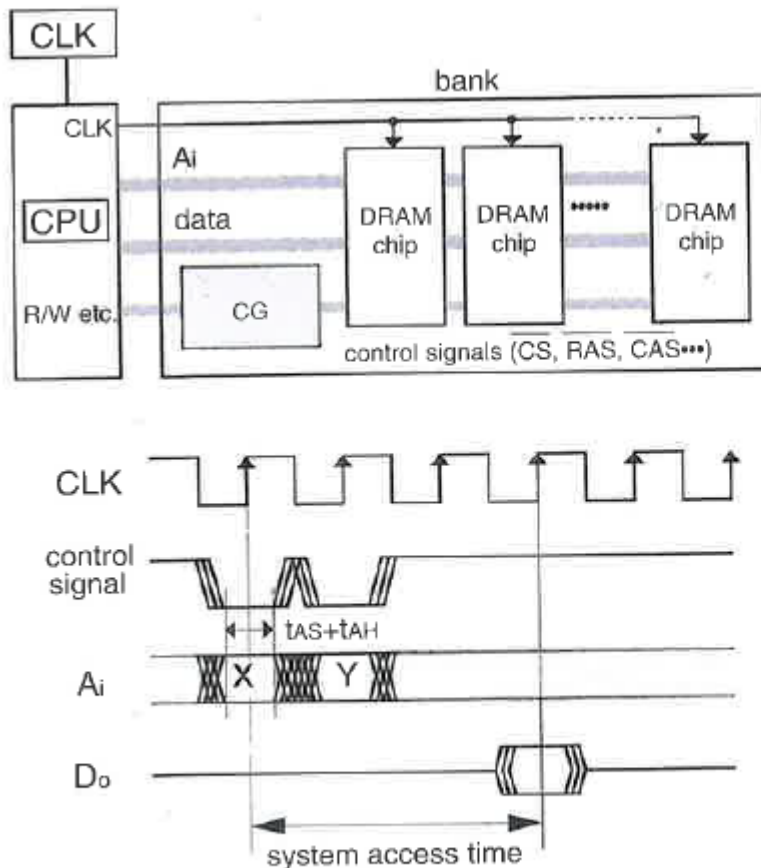


Fig. 6.17. The synchronous operation of the memory system [6.8]. CG, command generator

69. In sum, the '002 specification describes a synchronous memory system that uses a periodic clock signal for synchronization. The intrinsic evidence thus supports the interpretation of the claim term “clock signal” as “a periodic signal used for synchronization.”

70. For all of these reasons, the term “clock signal” should be interpreted to mean “a periodic signal used for synchronization.”

Petitioner’s Proposed Claim Interpretations

71. I have reviewed the claim interpretations proposed by Petitioner for the terms “static precharge state” (claims 18 and 37), “conditional clock generator” (claim 2), “means for decoding a first portion of a memory address of a memory array” (claim 11), “means for selectively providing a clock signal to a selected group of wordline drivers based on the first portion of the memory address [of a memory array]” (claims 11 and 27), “means for decoding a second portion of the memory address” (claims 11 and 14), “means for activating a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address” (claims 11 and 27), and “means for applying the second portion of the memory address to a shared address line” (claim 14). See Petition at 3-7. However, my analysis regarding the patentability of claims 1-28 and 31-37 does not depend on the constructions of these terms. Therefore, I do not dispute Petitioner’s proposed claim interpretations for the purpose of these proceedings.

IV. OVERVIEW OF THE CITED REFERENCES

A. Overview of Sato

72. U.S. Patent Number 4,951,259 (“Sato”) is titled “Semiconductor Memory Device with First and Second Word Line Drivers.” Sato was filed on February 18, 1988 and issued on August 21, 1990.

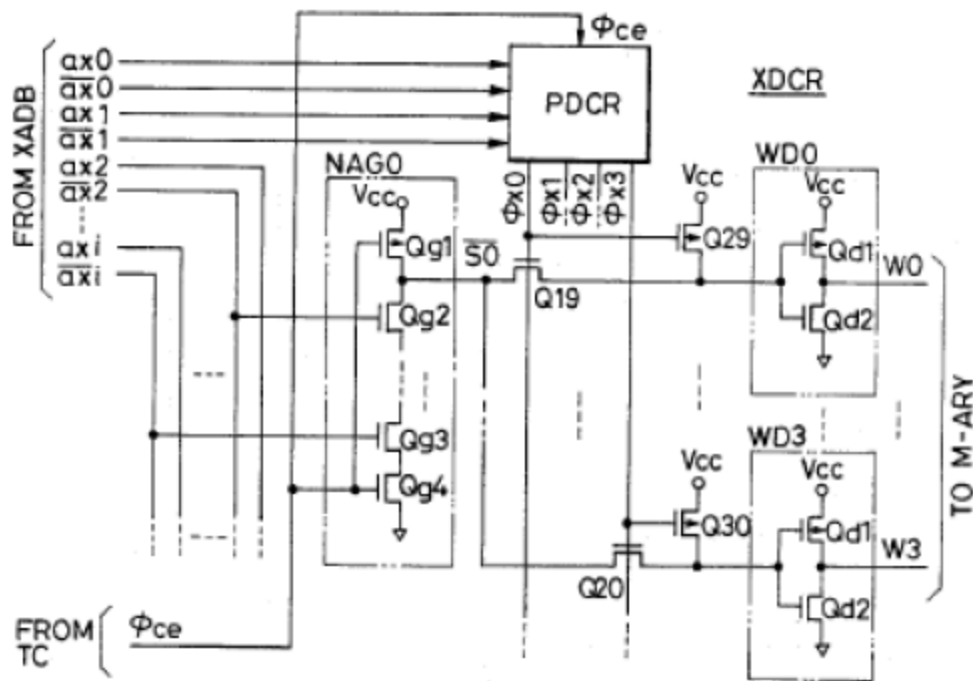
73. Sato pertains to a “semiconductor memory device...which includes a plurality of word line drivers and logic decoding circuitry coupled to the inputs of the word line drivers.” Sato at Abstract. Sato teaches reducing the “large capacitive loads on the output of the logic decoding circuit...which adversely effects the operating speed and memory.” Sato at Abstract. This is done by a “switching arrangement [that] can be controlled to respectively connect the output of the decoding logic circuit to the wordline drivers based on control output signals of a pre-decoder.” *Id.*

74. Sato describes as an object of his invention to provide a semiconductor memory device, such as CMOS static RAM, which speeds up the selection operation of the X address decoder and the operation speed of memory access. *Id.* at 2:9-13. To meet this objective, Sato utilizes (i) a “capacitance cut MOSFET” for receiving a corresponding output signal of a pre-decoder, for example, at the gate input terminal of the said MOSFET, and (ii) a “reset MOSFET” connected at its drain terminal, for example, to the input terminal of each wordline

drive circuit and at its source terminal to the power source voltage of the circuit. The reset MOSFET receives at its gate a selection control signal. Since the capacitance cut MOSFET is disposed in such a manner as to correspond to each wordline drive circuit, drivability of the wordline drive circuit can be increased without increasing loading on the output signals of the pre-decoder and on the decoding logic gate circuit, that is, without exerting any undesirable influences on the selection operation of the X address decoder. Accordingly, it becomes possible to increase the memory capacity of a semiconductor memory device such as a CMOS static RAM and to attain its higher operation speed. *Id.* at 2:20-47.

75. Fig. 3 of Sato is reproduced below.

FIG. 3



76. The circuit receives ϕ_{ce} , which is a “timing signal ... generated in accordance with a chip enable signal CE supplied as a control signal from outside.” Sato at 3:62-64. Sato also refers to the signal ϕ_{ce} as a “selection control signal.” *Id.* at 5:48-50. The circuit further receives a set of complementary internal address signals, ax_0 through ax_i . A predecoder, PCDR, receives the lower 2-bit complementary internal address signals ax_0 and ax_1 , and generates four outputs: ϕ_{x0} - ϕ_{x3} . *Id.* at 5:25-42. Sato refers to these outputs from the predecoder as “selection signals” that “control output signals of a predecoder.” *Id.* at Abstract and 1:30. The predecoder PCDR is a black box. Sato provides no disclosure on its internal circuitry.

77. The selection control signal ϕ_{ce} and complementary internal address signals ax_2 - ax_i other than the lower two bits in respective combinations are supplied to $k+1$ decoding NAND gate circuits NAG0-NAG k . *Id.* at 1:19-54 and 5:43-65. The NAND gates precharge their outputs to a high level when the timing signal ϕ_{ce} is low and evaluate to the result of applied input signals (decoding logic) when the timing signal ϕ_{ce} is high. *Id.* at Fig 1, 5:66-6:4, 6:8-13. Thus, the NAND gate circuits NAG0-NAG k operate in two phases, an output evaluation phase and a precharge phase. *Id.* at 5:66-6:21, Fig. 1. When the selection control signal ϕ_{ce} is high, the NAND gate circuits NAG0-NAG k are in the output evaluation phase, and the circuits output the selection control signal ϕ_{ce} to exactly one of their outputs

$\overline{S0} \sim \overline{Sk}$ based on the decoding of the signals $ax2$ - axi . When the selection control signal ϕ_{ce} is low, the NAND gate circuits NAG0-NAG k are in the precharge phase, and the circuits output the selection control signal ϕ_{ce} to all of the outputs $\overline{S0} \sim \overline{Sk}$. Outputs of the NAND gate circuits are supplied to the wordline drive circuits through N-channel capacitance cut MOSFETs (e.g., Q13-Q16), the gates of which are controlled by selection signals $\phi_{x0} \sim \phi_{x3}$. *Id.* at 5:66-6:21, 6:40-65, Fig. 1.

78. Exactly one of the selection signals $\phi_{x0} \sim \phi_{x3}$ is active at any time. *Id.* at 3:67-4:3. If, for example, ϕ_{x0} is high, input terminals of the wordline drive circuits that are connected to outputs of NAND gate circuits through N-channel capacitance cut MOSFETs driven by ϕ_{x0} but are not under the selection state will be floating because the corresponding P-channel reset MOSFET (e.g., Q23-Q26) will be off. *Id.* at 7:12-20. Note, however, that since the time in which CMOS static RAM is under the selection state is short, the input terminals of the wordline drive circuits which are under the non-selection state can maintain a high voltage level due to the high level of charge built up in the gate capacitances of MOSFETs Qd1 and Qd2 of each wordline drive circuit (this charge was accumulated when the P-channel reset MOSFET was on), i.e., the output of the corresponding non-selected wordline drivers will be low. On the other hand, the input terminal of the wordline drive circuit that is under the selection state will be driven low by the

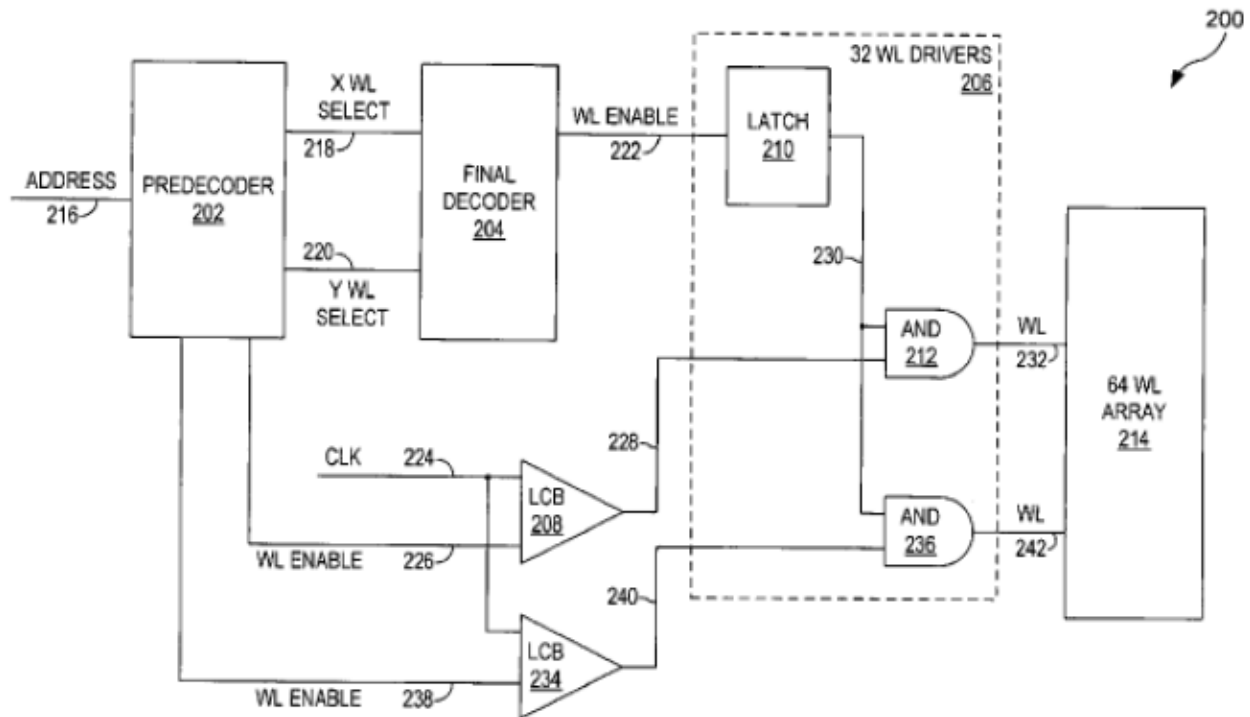
pull-down section of the corresponding NAND gate (i.e., one of the NAND gate circuits NAG0-NAG_k), and thus, the output of the selected wordline driver will be high. *Id.* at 7:1-30.

B. Overview of Asano

79. U.S. Patent No. 7,139,215 (“Asano”) is titled “Apparatus and Method of Word Line Decoding for Deep Pipelined Memory.” It was filed on November 5, 2004 and issued on November 21, 2006.

80. Asano discloses a “method, an apparatus, and a computer program...to reduce the number of required latches in a deep pipeline wordline (WL) decoder.” Asano at Abstract. It teaches that “[t]raditionally, a signal local clock buffer (LCB) has been responsible for providing a driving signal to a WL driver,” and the prior art thus required “a large number of latches.” *Id.* Therefore, Asano sought to “reduce this latch usage” so that “one latch can enable an increased number of WLs.” *See id.*

81. Fig. 2 of Asano is reproduced below.



82. In this figure, the predecoder 202 receives the full row address index 216. Asano at 2:59-63. For the 64 wordline drivers depicted in 214, this corresponds to predecoder 202 receiving 6 row address index inputs. *Id.* This predecoder produces a 1-bit decoding, resulting in WL ENABLE 226 and WL ENABLE 238 which are complements of one another, subsequently resulting in the selection of the adjacent top or bottom wordlines in the 64 WL Array 214. *Id.* at 2:53-58. In addition, predecoder 202 produces an X wordline select signal 218 and a Y wordline select signal 220. *Id.* at 2:1-16. Final Decoder 204 receives the X wordline select signal 218 and the Y wordline select signal 220 as inputs and produces 32 outputs. Each of the 32 outputs is latched and subsequently goes to exactly one of the 32 WL drivers 206. *Id.* at 3:3-12. A clocking signal 224 is input

into LCBs 208 and 234 (the internal circuitry of which are not explained in Asano), and based on WL ENABLE signals 226 and 238, respectively, exactly one of the outputs to the LCBs will be driven high at a time (i.e., either 228 or 240). The output of latch 210 is logic gated with the outputs of the LCBs to drive exactly one of the 64 wordlines in the memory array. Note that one latch 210 is shared between two wordline drivers, thereby lowering the latch count and reducing the clock power.

C. Overview of Itoh

83. VLSI Memory chip Design by Kiyoo Itoh (“Itoh,” Ex. 1007) was published in 2001 by Springer-Verlag Berlin Heidelberg.

84. Itoh discusses an address decoder for DRAM circuits and states that “[a] predecoding scheme achieves a faster decoding and area reduction of [the] decoder.” Ex. 1007 at 14. Itoh provides a Figure 3.46 that “compares predecoding schemes” (*id.*):

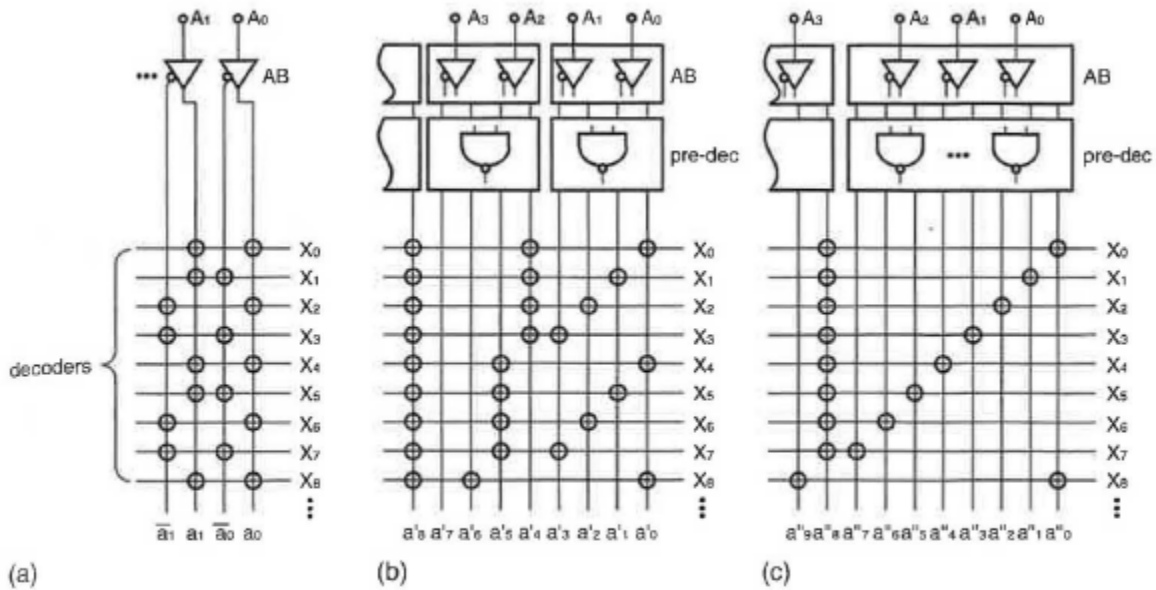


Fig. 3.46. Predecoding [3.4]. (a) no predecoding; (b) 2-bit predecoding; (c) 3-bit predecoding

85. “Direct decoding, 2 bit predecoding, and 3 bit predecoding are shown in Figs. 3.46a-c, respectively.” *Id.* at 14. The direct decoding shown in Fig. 3.46a shows circuit components that each receive a single input (e.g., A_1) and generate two outputs (e.g., $\overline{a_1}$ and a_1). *Id.* at 15. Itoh states that “[e]ach 2 bit predecoder can select one of four address input lines coming to the decoders ...[,] while each 3 bit decoder can select one of eight address input lines.” *Id.*

V. SATO DOES NOT RENDER CLAIMS 1-28 AND 31-37 OBVIOUS (GROUND 1)

86. The Board instituted trial on the ground that claims 1-28 and 31-37 are allegedly obvious over Sato. In my opinion, Sato does not render obvious any of these claims.

A. Sato Does Not Teach or Suggest a “Clock Signal,” As Required by Claims 1-28 and 31-37.

87. Independent claims 1, 7, 11, 17, 21, and 23-27 recite a “clock signal.”

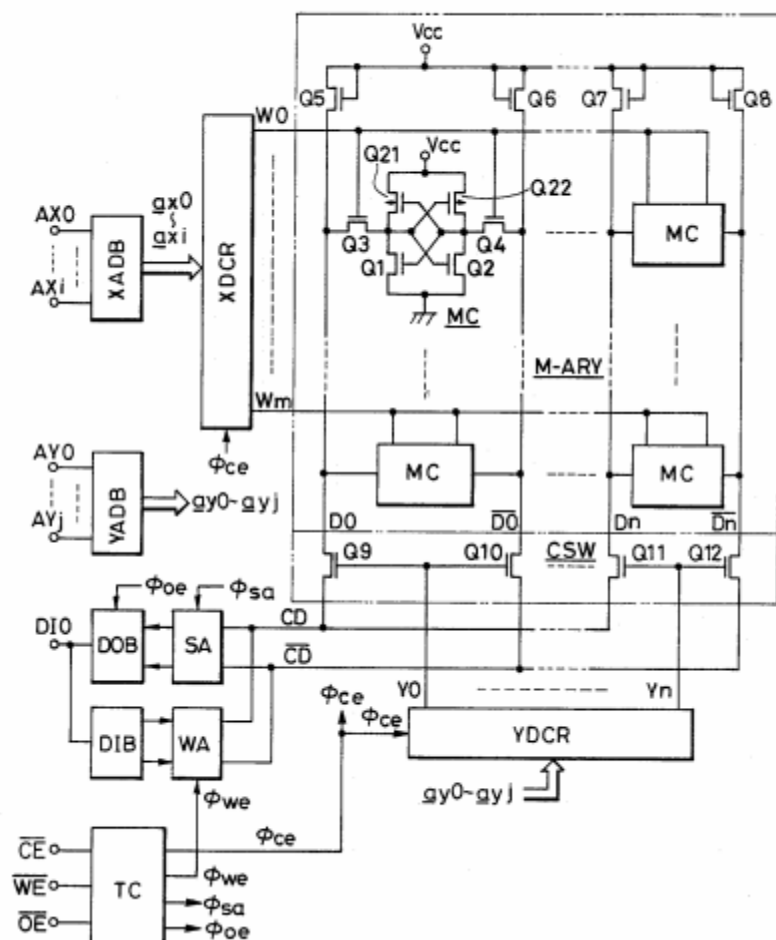
Petitioner argues that Sato’s selection control signal ϕ_{ce} meets the claimed “clock signal.” However, I disagree for the reasons provided below.

1. Sato’s Selection Control Signal is Not a “Periodic Signal Used for Synchronization,” As Required Under the Proper Construction of the Term “Clock Signal.”

88. As explained in Section III.D above, the claim term “clock signal” should be interpreted to mean “a periodic signal used for synchronization.” Sato’s selection control signal ϕ_{ce} is not a periodic signal used for synchronization, and the reference thus fails to disclose the claimed “clock signal.”

89. Sato’s selection control signal ϕ_{ce} is generated by a timing circuit TC as shown in Fig. 4 of Sato:

FIG. 4



90. The timing circuit TC generates the selection control signal ϕ_{ce} “in accordance with a chip enable signal CE supplied as a control signal from outside and is kept at a high level under the selection state of this CMOS static RAM.” Sato at 3:59-65. The timing circuit TC generates and controls the timing and sequence of various timing signals for the sensing and movement of data on the semiconductor memory device. More precisely, the TC takes as input external control signals chip enable signal CE#, write enable signal WE#, and output enable

signal OE#, and generates timing signals ϕ_{ce} , ϕ_{sa} , ϕ_{oe} , and ϕ_{we} . No clock signal is used in the generation of the ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} timing signals.

91. Particularly, ϕ_{ce} is generated by the TC in accordance with CE# and is used to selectively actuate the X and Y address decoders (XDCR and YDCR), set one of the wordlines designated by the X address signals to a high selection state, and select one set of complementary data lines and connect them to the complementary common data lines CD and CD#. In this way, a particular memory cell MA is selected.

92. ϕ_{sa} is generated by the TC to cause selective operation of the sense amplifier SA to amplify the read signal outputted from the selected memory cell MC through the complementary common data lines CD and CD#. The output signal of the sense amplifier SA is supplied to the data output buffer DOB.

93. ϕ_{oe} is generated by the TC in the read mode of the CMOS static RAM of Sato to selectively operate the DOB to further amplify the read signal of the MC outputted from the SA and deliver it to external devices through the input/output terminals DIO. Notice that the output of the data output buffer DOB is in a high impedance state under the non-selection state of CMOS static RAM in which the timing signal ϕ_{oe} is at the low level and in the write mode. *Id.* at 4:54-57.

94. ϕ_{we} is generated by the TC in the write mode of the CMOS static RAM of Sato to selectively operate the write amplifier, which in turn supplies a write current, reliant on the complementary write signals supplied from the data input buffer DIB, to the selected MC through the complementary common data lines CD and CD#. Notice that the output of the write amplifier WA is in a high impedance state under the non-selection state of CMOS static RAM where the timing signal ϕ_{we} is at the low level, and in its read mode. *Id.* at 5:2-6.

95. As described earlier, Sato's X (row) and Y (column) address decoders are operated selectively in accordance with the selection control signal ϕ_{ce} supplied from the timing control circuit TC. *Id.* at 4:27-31.

96. Sato provides no indication that the selection control signal ϕ_{ce} is a periodic signal used for synchronization. Rather, the only relevant disclosure of Sato indicates that ϕ_{ce} is not periodic. Specifically, as noted above, Sato states that the selection control signal ϕ_{ce} "is generated in accordance with a chip enable signal CE# supplied as a control signal from outside and is kept at a high level under the selection state of this CMOS static RAM." Sato at 3:59-65. In other words, when the chip enable signal CE# is low, the selection control signal ϕ_{ce} is kept high.

97. Sato provides no teaching that the chip enable signal CE# is periodic, and in fact, this signal would not be periodic. CE# assumes a low value only when

the CMOS static RAM of Sato is selected for read or write operations, and otherwise assumes a high value. The signal ϕ_{ce} has a value that is opposite that of the $CE\#$ signal, such that ϕ_{ce} assumes a high value only when the CMOS static RAM of Sato is selected for read or write operation, and otherwise assumes a low value. The access pattern to a static RAM is determined by the access needs of the component or device using the static RAM as memory. For example, in the very common case of the static RAM serving as a data cache for a CPU, the runtime characteristics of the application executing on the CPU (i.e., the mix of memory load/store instructions vs. register-type instructions) determines the frequency and persistence of any access to the static RAM.

98. The resulting access pattern is highly irregular and does not result in a periodic high/low state of $CE\#$, and therefore, ϕ_{ce} is not a periodic signal. Sato does not suggest that its static RAM would be accessed in a regular manner. A similar reasoning shows that other timing signals e.g., ϕ_{oe} , and ϕ_{we} are also non-periodic (the mix of read and write operations is highly application-dependent; moreover, the mix can dramatically change during different execution phases of the same application program).

99. Because Sato does not teach or suggest “a periodic signal used for synchronization,” it does not meet the “clock signal” limitation of the challenged claims. For at least this reason, claims 1-28 and 31-37 are not obvious over Sato.

2. Sato Discloses an Asynchronous Circuit That Does Not Use a Periodic Clock Signal.

100. Sato discloses an asynchronous circuit. As explained below, the POSA would understand that asynchronous circuits, such as those disclosed by Sato, do not use a periodic clock signal for synchronization, as required by the '002 patent claims. Further, asynchronous systems are not configured to use a periodic clock signal, and the POSA therefore would not be motivated to modify Sato to use such a signal.

101. As explained in Section III.D above, asynchronous memory systems require control logic circuitry for receiving asynchronous inputs to the memory system. These inputs can arrive at any time and are not synchronized with edges of a periodic clock signal. Based on these inputs, the control logic circuitry generates appropriately timed sequences of internal timing signals to control the movement of data in memory. The internal timing signals are not periodic and are instead generally pulses or strobes without a periodic characteristic. Thus, asynchronous systems do not use a periodic clock signal and instead use multiple, non-periodic internal timing signals.

102. The POSA would understand Sato's memory system to be asynchronous because it is an exact match of the asynchronous systems described above. In Sato, the timing control circuit TC is the control logic circuitry required by asynchronous memory systems. The timing circuit TC takes as input

asynchronous external control signals (chip enable signal CE#, write enable signal WE#, and output enable signal OE#) and generates timing signals ϕ_{ce} , ϕ_{sa} , ϕ_{oe} , and ϕ_{we} . These timing signals are used to effect address decoding and memory cell selection, sense amplifier activation and data readout, output buffer enablement and, in case of write operation, write data enablement, as described above. Thus, in Sato, there is no single, periodic clock signal to which memory operations are synchronized, but rather multiple internal timing signals ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} for controlling different components of the memory system.

103. Sato does not suggest that any of the signals ϕ_{ce} , ϕ_{we} , ϕ_{sa} , and ϕ_{oe} are periodic, which is consistent with asynchronous systems' use of multiple, non-periodic internal timing signals. Further, the inputs to the timing control circuit TC are non-periodic and asynchronous (i.e., they can arrive at any time and need not be synchronized to a clock edge), and because the outputs are dependent in a one-to-one manner on these inputs, the outputs will also be non-periodic and asynchronous. Accordingly, Sato's selection control signal ϕ_{ce} is not a "periodic signal used for synchronization."

104. The asynchronous memory system of Sato is fundamentally different than the synchronous memory system of the '002 patent. Synchronous memory systems use a periodic clock signal to time all memory operations. By contrast, asynchronous memory systems, like those of Sato, are not configured to use a

periodic clock signal—instead, they use non-periodic timing signals generated based on asynchronous, external input events. Accordingly, the POSA would not be motivated to modify Sato to use a periodic clock signal because the use of such a signal would be contrary to how asynchronous systems operate.

105. Sato does not meet the “clock signal” limitation of the challenged claims for these additional reasons and claims 1-28 and 31-37 are therefore not obvious over Sato.

3. Petitioner’s Arguments That Sato’s Selection Control Signal “Represents or Renders Obvious a Clock Signal” Are Erroneous.

106. The petition asserts that Sato’s selection control signal ϕ_{ce} “represents or renders obvious a clock signal.” Petition at 14. The petition provides a number of arguments in support of its assertion, but all of them are erroneous.

107. The petition argues that

[a] POSITA would have “viewed the function of the timing signal ϕ_{ce} as similar to or equivalent to that of a clock signal because 1) “clock” is another name for a timing signal, 2) the Greek symbol phi (ϕ) is frequently used in the art to indicate clock signals, 3) this signal performs the same function as the clock signal in the ’002 patent and 4) ϕ_{ce} performs the same function as the clock signal in a clocked decoder such as that described by Bridges.

Petition at 14-15, citing Horst Decl. ¶64. However, these arguments are erroneous, and none of them supports Petitioner's assertion that Sato's selection control signal ϕ_{ce} represents or renders obvious a clock signal.

108. First, the word "clock" or "clock signal" is not another name for a timing signal. Neither Petitioner nor Dr. Horst provide any evidence or reasoning to support their argument that "clock is another name for a timing signal," which is a false statement. The words "clock signal" and "timing signal" are not interchangeable, nor would the POSA have understood them as such. In fact, Petitioner's own reference, Itoh, reinforces the notion that clock signals and timing signals are separate and not interchangeable. As described in Section III.D above, Figure 6.14 of Itoh depicts asynchronous DRAM with non-periodic timing signals RAS# and CAS#. By contrast, Figure 6.15 of Itoh discusses a synchronous DRAM as utilizing a periodic clock signal CLK. The fact that Itoh only calls the periodic clock signal in the synchronous RAM a "clock" and does not call any of its asynchronous, non-periodic timing signals a "clock" reinforces the proposition that timing signals are distinctly different from clock signals.

109. Second, contrary to Petitioner's argument, the Greek symbol phi would not be understood by the POSA to refer to a clock signal. Rather, the POSA would understand that the Greek symbol phi is used in the art to denote a phase signal, not a clock signal. The POSA would further understand that the ϕ signals

used in Sato are in fact non-periodic signals having positive (high) and negative (low) phase levels, where the phase level determines their precise effect on the memory device.

110. Third, I disagree with Petitioner's argument that Sato's selection control signal ϕ_{ce} "performs the same function as the clock signal in the '002 patent." A race condition leading to a complete breakdown of circuit functionality can result if the NAND gate circuits NAG0-NAG k do not receive the selection control signal ϕ_{ce} . Specifically, in the embodiment of Fig. 3 of Sato, if NAND gates circuits NAG0-NAG k do not receive the ϕ_{ce} timing signal e.g., they are implemented as static logic (fully-complementary) NAND gates, then when the CMOS static RAM transitions from the non-selection state to the selection state (i.e., the ϕ_{ce} timing signal transitions from low to high), a race condition can result between output signals from the PDCR and the said NAND gates, causing an unwanted hazard activity on some wordline. For example, consider that NAND gates circuits NAG0-NAG k do not receive the ϕ_{ce} timing signal, and that the previously decoded row address bits $ax2-axi$ had discharged the output of NAG K static NAND gate. Timing signal ϕ_{ce} transitions from low to high, and the PDCR sets one of the selection signals $\phi_{x0}-\phi_{x3}$ to logic high as a result of decoding the (current) address bits $ax0-ax1$. For purposes of this example, assume that the selected output signal of the PDCR is ϕ_{x0} . This causes a group of N-channel

capacitance cut MOSFETs (the gates of which are driven by $\phi x0$) to turn on and pass the outputs of the corresponding static NAND gates to their inverting wordline drivers.

111. Continuing with this example, since the NAGK output is low and $\phi x0$ is high, the Wm-3 output of the inverting driver WDm-3 will be driven high (wordline Wm-3 will be selected).⁵ Next, the NAG0-NAGk will complete the decoding of current address bits $ax2-axi$, and as a result of this, possibly some other NAND gate's output will switch from high to low (and of course, in such a case, the output of NAGk will go from low to high). For example, consider that, under the current decoding of address bits $ax2-axi$, the NAG0 output switches to low. This means that the output W0 of the inverting driver WD0 will go high (and of course, the output Wm-3 of inverter WDm-3 will go low), indicating the final and correct activation of wordline W0 and deactivation of wordline Wm-3.

112. However, under this scenario, an unwanted hazard activity will have occurred on wordline Wm-3, which can subsequently result in creating a voltage differential between selected bitline (D0) and bitline# (D0#) based on the stored value of a memory cell that connected to the bitline and bitline# but is located on

⁵ Unfortunately, we have to go back and forth between Fig. 1 and Fig. 3 of Sato because Fig. 1 shows details of those circuit portions of Sato's invention which are not found in the incomplete drawing of Fig. 3 of Sato. See Sato at 9:31-43.

the wrong row of the memory device. This is a deleterious and dangerous effect that would greatly and adversely affect the reliability of the row decoding process of Sato and correct operation of Sato's memory device, rendering the Sato design useless. For these reasons, the embodiment of Fig. 3 of Sato needs the selection control signal ϕ_{ce} , which pre-charges all NAND gate outputs to a high level (between consecutive accesses to the memory device) and discharges the output of exactly one selected NAND gate to a low level after the memory device has transitioned from the non-selection state to the selection state.

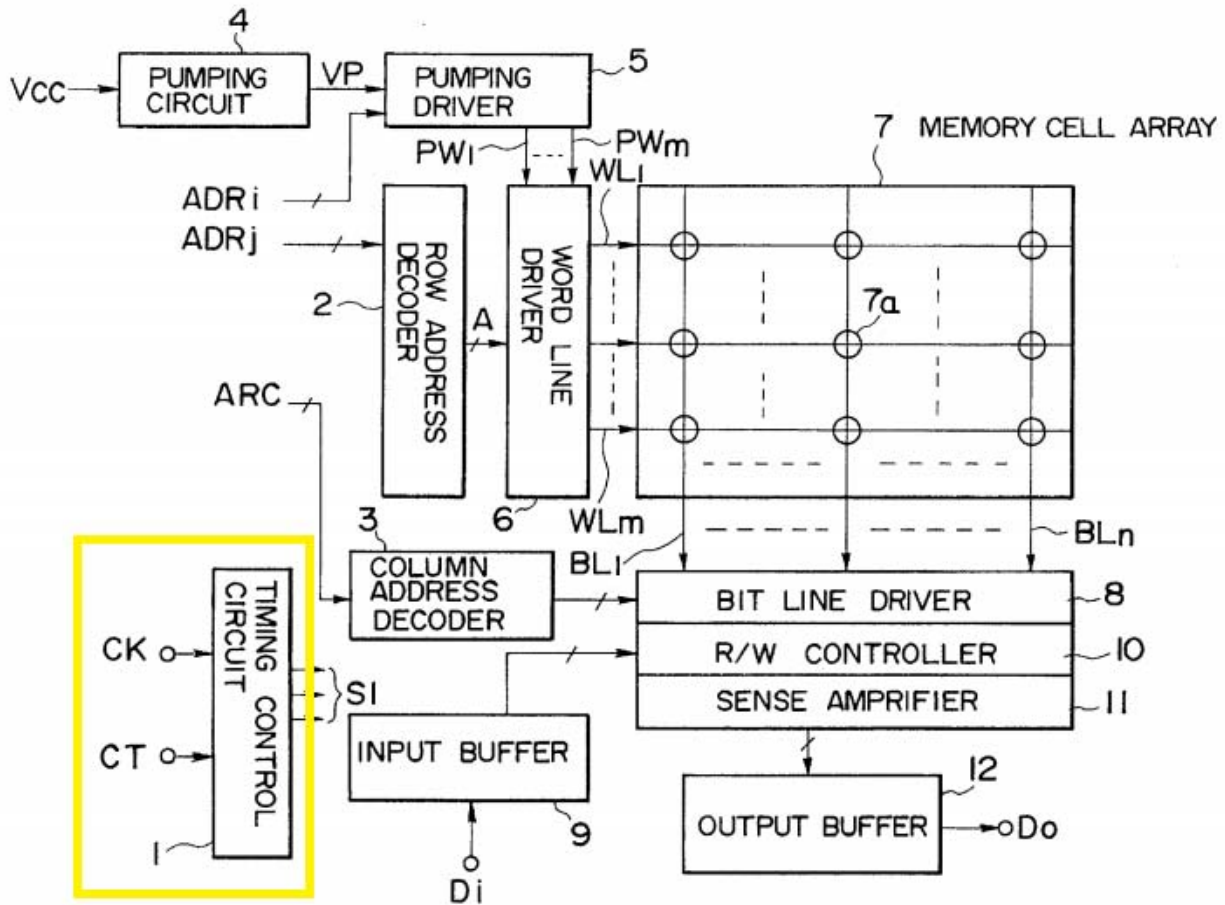
113. The above-described function performed by the selection control signal ϕ_{ce} of Sato—ensuring that the memory system does not enter into an unstable race condition—is entirely different than any function performed by the clock signal of the '002 patent claims. The clock signal of the '002 patent claims does not prevent an unstable race condition from occurring. Petitioner's assertion that Sato's selection control signal ϕ_{ce} “performs the same function as the clock signal in the '002 patent” is wrong.

114. Fourth, I disagree with Petitioner's argument that Sato's selection signal ϕ_{ce} “performs the same function as the clock signal in a clocked decoder such as that described by Bridges.” Unlike Bridges, Sato does not disclose a clocked decoder because none of its decoders operate based on a periodic, synchronizing clock signal. Sato's selection control signal ϕ_{ce} does not meet the

“clock signal” limitation because it is not a periodic signal used for synchronization but rather one of multiple non-periodic timing signals (ϕ_{ce} , ϕ_{we} , ϕ_{sa} , ϕ_{oe}) used in an asynchronous system. Any similarity between the uses of Sato’s selection control signal ϕ_{ce} and the clock signal of Bridges does not transform the signal ϕ_{ce} into a periodic clock signal.

115. The petition also argues that “even the examiner and Patent Owner recognized a timing signal as being equivalent to a clock signal during prosecution of the ’002 patent.” Petition at 15. The petition cites to the November 19, 2007 Office Action, where the Office rejected originally filed claims 17 and 18 as allegedly being anticipated by U.S. Patent No. 5,602,796 (“Sugio”). *Id.* Petitioner argues that the Office “equat[ed] the claimed clock outputs with timing control signal outputs of Sugio’s timing control circuit 1.” *Id.* But Petitioner’s argument fails because Sugio is entirely different from Sato and does, in fact, expressly disclose a clock signal. As shown below, Sugio discloses a timing control circuit 1 that receives a clock signal CK:

FIG. 2



Ex. 1012 (Sugio) at Fig. 2 (annotations added). “[T]he timing control circuit 1 outputs the control signals $S_1 \dots$ based on the control signal CT and the clock CK.” *Id.* at 3:58-61. The control signals S_1 are “for controlling timings provided for respective components.” *Id.* at 2:10-14. Sugio does not disclose whether the control signals S_1 are periodic clock signals. However, it is possible that they are periodic because Sugio states that they are generated based on the clock signal CK.

116. In Sato, by contrast, the selection control signal ϕ_{ce} is not generated based on a clock signal but is instead generated based on the non-periodic chip

enable signal CE#, as explained above. The disclosures of Sugio and Sato are not the same at all. To the extent that the Office previously found that Sugio's control signals S₁ are clock signals, this is not relevant to whether Sato's selection control signal ϕ_{ce} is a clock signal because the respective disclosures of the two references are completely different.

117. The petition also highlights the statement in the Background section of Sato that "CMOS static RAMs including clocked static decoders are known in the art." Sato at 1:10-11. However, this is just a general statement, and it is not describing any of the embodiments of Sato. And this general statement is not related at all to the selection control signal ϕ_{ce} , and thus, it provides no support for Petitioner's position that the signal ϕ_{ce} is a clock signal. Rather, this statement from Sato's Background section tends to show that the selection control signal ϕ_{ce} is *not* a clock signal. The statement shows that Sato is aware of the term "clock" and uses it to describe the state of the art. But when Sato describes his own invention, he never refers to any clocks or clock signals. This fact further evidences that no such clock signal is used in the embodiment of Sato cited by Petitioner.

118. The petition further argues that "Sato states that his invention 'can be applied widely to semiconductor memory devices having at least a clocked static type address decoder[,] ... which further corroborates Dr. Horst's opinion."

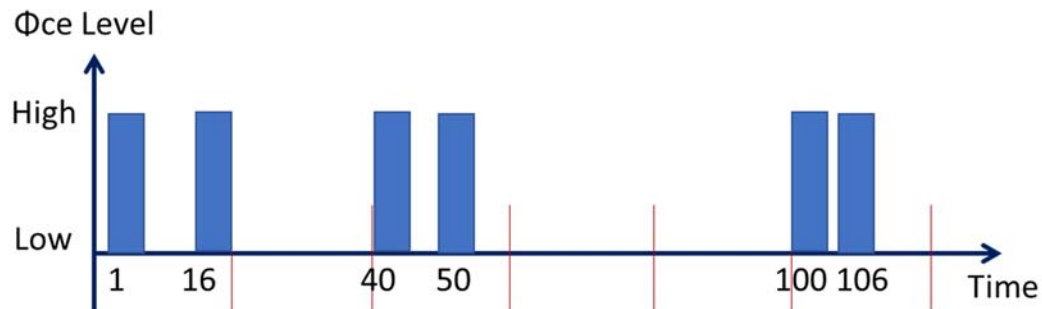
Petition at 15, citing Ex. 1001 at 12:4-6. But this portion of Sato does not support Petitioner's assertion that Sato's selection control signal ϕ_{ce} represents or renders obvious a clock signal. Rather it is only stating Sato's opinion that his invention can be applied to semiconductor memory devices having a clocked static type address decoder in the same way that he opines that his invention can also be applied to dynamic RAMs or other semiconductor memory devices. Sato at 11:66-12:3. None of the X address decoders disclosed in Figs. 1-5 of Sato are clocked because they do not use a periodic, synchronizing clock signal, and Sato never equates any of its X address decoders with clocked decoders.

119. Sato provides no disclosure on how its invention could allegedly be applied to devices having a clocked static logic address decoder. Sato also does not describe whether any modifications would be required to use Sato's invention in this manner. Sato does not suggest that the non-periodic selection control signal ϕ_{ce} would be replaced with a periodic clock signal when its invention is applied to a device having a clocked static logic address decoder. Petitioner likewise provides no explanation or evidence on how Sato's invention could be applied to such a device. Sato's vague statement about potential uses for its invention cannot transform the reference's non-periodic timing signal ϕ_{ce} into a periodic clock signal.

120. The petition also argues that “[a]lthough Sato includes an obscure statement suggesting that the timing signal could be kept at a high level, in contrast, a POSITA would not have read this statement as one embodiment, distinct of other aspects described within the Sato disclosure,” and that “POSITA would have understood that the Sato system would perform poorly or malfunction if the timing signal in Sato were kept at a high level throughout operation.” Petition at 16-17, citing Horst declaration ¶¶68-69. Dr. Horst’s example of how Sato’s address decoder XDCR would fail if it was supplied with two consecutive addresses 000000 and 111100 (the rightmost two bits correspond to $ax0$ and $ax1$, respectively) without the timing signal ϕ_{ce} changing state from a selected state to a non-selected state to a selected state (high to low to high) simply confirms the fact that ϕ_{ce} cannot stay in a selected state while the row address is changing. In fact, there is a return to non-selected state requirement after a row address is correctly decoded and before a new row address comes in, and the dynamic NAND gates NAG0-NAGk would fail if one was to evaluate them multiple times without precharging them in between evaluations. These facts were well known to a POSA. However, if Dr. Horst and Petitioner are using these facts to imply that ϕ_{ce} is a periodic signal, then they are wrong.

121. Consider the memory device of Sato being accessed at time instances 1, 16, 40, 50, 100, 106, and so on. In this case, the ϕ_{ce} signal would look like the

following, which is a non-periodic signal. By way of example only, I have assumed that Sato's memory device stays in its selected state for a fixed period of time (e.g., 4 units of time) before returning to its non-selected state in preparation for the next transition to a selected state:



122. As described in Section V.A.1 above, Sato's signal ϕ_{ce} varies based on the highly irregular access patterns for reading and writing to the memory. Thus, to the extent that the signal ϕ_{ce} must change from high to low to high, as Dr. Horst opines, it does so in an irregular, non-periodic manner and not at a fixed frequency, as would be found in a periodic signal. Thus, Dr. Horst's argument does not show that the selection control signal ϕ_{ce} is a periodic clock signal.

123. For all of the above reasons, Sato does not disclose or suggest the claimed "clock signal." Therefore, in my opinion, Sato does not render obvious any of challenged claims 1-28 and 31-37.

VI. ASANO AND ITOH DO NOT RENDER CLAIMS 1-17, 20-28, AND 31-36 OBVIOUS (GROUND 2)

124. The Board instituted trial on the ground that claims 1-17, 20-28, and 31-36 are obvious over Asano and Itoh.

125. Petitioner argues that Asano “represents the predecoder 202 simply using a block element in a block diagram,” and Itoh “illustrate[s] a possible implementation of the internal structure for the predecoder 202.” Petition at 35. But Petitioner has not sufficiently articulated why the POSA allegedly would have been motivated to combine these references, and challenged claims 1-17, 20-28, and 31-36 are therefore not obvious over these references.

A. Asano Does Not Disclose or Suggest a Circuit Device Including Distinct “First Logic” and “Second Logic.”

126. As explained above, the '002 patent claims require first and second logics. Claim 1, for instance, requires a “first logic to receive a clock signal and a first portion of a memory address of a memory array” and a “second logic to decode a second portion of the memory address,” among other limitations. This is a fundamental aspect of the '002 patent: The memory address is split into different portions, with one portion of the memory address being received at the first logic, and the other portion of the memory address being received at the second logic.

127. Petitioner states that “Asano forms ... the base reference of Ground-2 of [the] Petition,” but this reference does not disclose splitting a memory address

into first and second portions, nor does it disclose decoding the first and second portions using distinct first and second logics, respectively. Petitioner cites to the predecoder 202 of Asano as meeting the “first logic” and “second logic” limitations of the claims (see Petition at 36), but the predecoder 202 is a single logic circuit that receives the entire memory address:

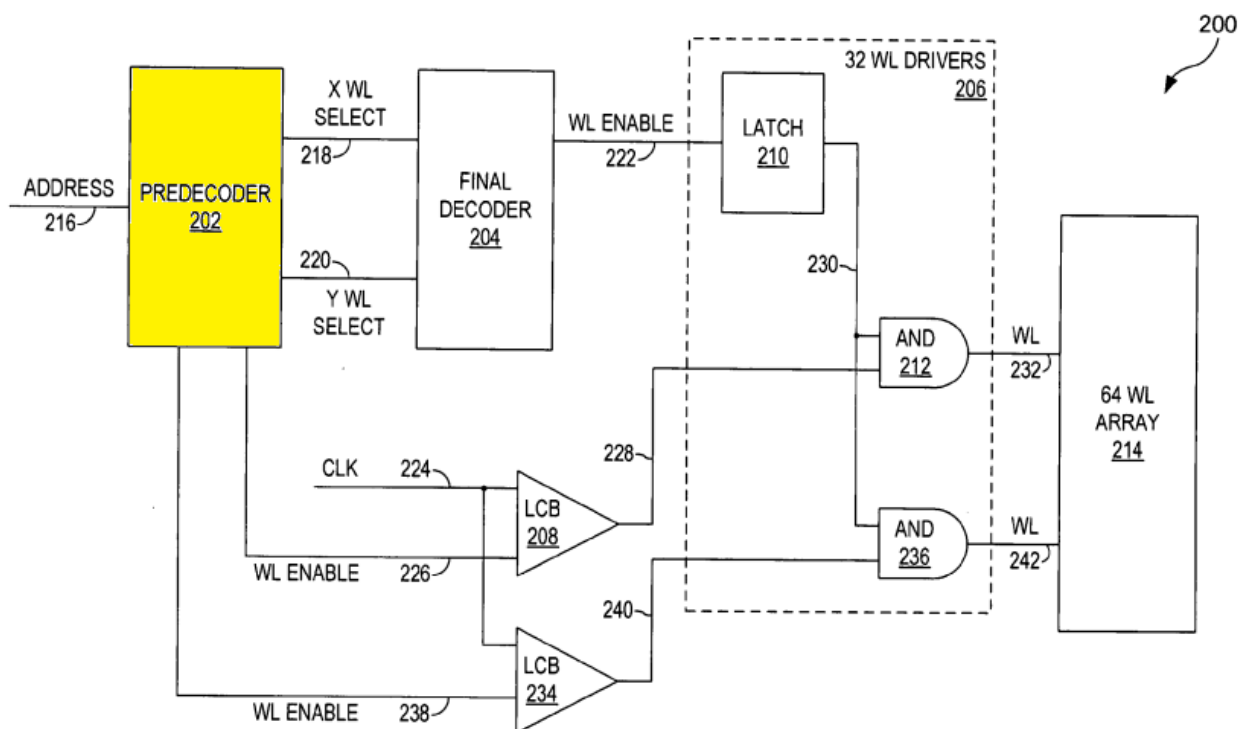


FIG. 2

Moreover, Asano contains no teaching or suggestion that the predecoder can or should be split into multiple different logics. In fact, Asano contains no disclosure at all on the internal circuitry of the predecoder 202. Accordingly, Asano does not disclose or suggest the “first logic” and “second logic” required by the claims.

128. Petitioner argues that Asano's predecoder 202 generates (i) the X wordline select signal that is 8 bits long, (ii) the Y wordline select signal that is 4 bits long, and (iii) two WL ENABLE signals. Petition at 38-39. Petitioner further argues that "Asano's predecoder uses three address bits to produce the X wordline select signal and two address bits to produce the Y," and "[t]ogether, the three-bit and two-bit predecoders represent the 'second logic' portion of the predecoder." *Id.* at 39. Petitioner also argues that "a POSITA would have found it obvious to implement the "first logic" portion of Asano's predecoder ... using a 1 to 2 decoder." *Id.*

129. I disagree. Petitioner is attempting to read disclosure into Asano that does not exist and would not have been clear to the POSA. Specifically, Petitioner is relying on predecoder 202 of Asano as allegedly performing both the first logic decoding and the second logic decoding, and this runs contrary to the '002 patent's specification and claims, which make clear that the first and second logics comprise separate and distinct decoding circuits. Contrary to Petitioner's assertion, there is nothing in Asano to suggest that predecoder 202 can or should be implemented using multiple predecoders, as opposed to a single predecoder, as the reference teaches. If Asano intended its predecoder 202 to include multiple predecoders or multiple logic circuits, it could have specified as such, just as

Asano specified two separate LCBs (208 and 234) and two separate AND gates (212 and 236) within that very same figure.

130. Asano thus runs contrary to the '002 patent teaching that a memory address is split into two portions, and the portions are then input into two separate logics with two separate decoders for each portion of the memory address. The reference fails to disclose the claimed “first logic” and “second logic” for at least these reasons.

B. The Petition Does Not Sufficiently Articulate Why a POSA Would Allegedly Have Been Motivated to Combine Asano and Itoh.

131. Recognizing that Asano includes no teaching or suggestion of separate and distinct “first logic” and “second logic,” Petitioner argues

[b]ecause Asano represents the predecoder 202 simply using a block element in a block diagram, a POSITA would have looked to Itoh’s textbook circuits in determining how the internal structure of the predecoder 202 would be built as separate logic sections for decoding different portions of the 6-bit memory address.

Petition at 35. Petitioner specifically argues that the POSA would be motivated to implement (i) a “first logic” in Asano’s predecoder 202 using a 1-to-2 decoder disclosed by Itoh, and (ii) a “second logic” in the predecoder 202 using 2-to-4 and 3-to-8 decoders disclosed by Itoh. *Id.* at 36-41.

132. I disagree. As explained below, Petitioner has not adequately explained why the POSA would allegedly be motivated to combine Asano and Itoh as proposed.

133. Petitioner argues that “[b]ecause Asano represents the predecoder 202 simply using a block element in a block diagram, a POSITA would have looked to Itoh’s textbook circuits” in determining how to implement the predecoder. Petition at 35. But in my opinion, Petitioner has not provided any reasons why the POSA allegedly would have looked specifically to Itoh. Petitioner admits that Itoh discusses just one of the many different ways that Asano’s predecoder 202 could possibly be implemented:

Itoh discloses well-known circuits that illustrate *a possible implementation of the internal structure for the predecoder 202*.

Id. (emphasis added).

[A] POSITA *could have* implemented Asano’s predecoder using a combination of the predecoder circuits disclosed by Itoh.

Id. at 37 (emphasis added).

[T]he “first logic” portion of Asano’s predecoder could be implemented using known logic circuitry such as that disclosed by Itoh.

Id. at 42. These statements from Petitioner acknowledge that Asano’s predecoder 202 could be implemented in various different ways, and that Itoh’s circuits are just one “possible implementation of the [predecoder’s] internal

structure.” Petitioner has not provided any reasons why the POSA allegedly would have selected Itoh’s implementation instead of the other possible implementations.

134. Petitioner also argues that “[a] POSITA designing Asano’s memory circuit would have naturally turned to a textbook such as Itoh’s for details on memory design techniques for a predecoder.” Petition at 35. Similarly, Petitioner asserts that “[a]n artisan endeavoring to practice Asano’s invention would have looked to known circuit designs when seeking to implement the Asano predecoder since Asano describes it at only a functional level.” *Id.* at 41. But Petitioner has provided no reasoning as to why the POSA would have been motivated to use Itoh’s decoding circuits, specifically, instead of other circuits described in various other textbooks and sources.

135. The thrust of Petitioner’s argument appears to be that Asano’s predecoder 202 outputs an 8-bit X wordline select signal and a 4-bit Y wordline select signal, and “[a]s such, it would have been obvious for a POSITA to implement Asano’s predecoder using Itoh’s three-bit predecoder to generate the 8 bits of the X wordline select signal and Itoh’s two-bit predecoder to generate the 4 bits of the Y wordline select signal.” Petition at 39. Likewise, Petitioner argues, because Asano’s predecoder 202 outputs two WL enable signals, it would have been obvious for the POSA to implement Asano’s predecoder using Itoh’s 1-to-2 decoder to generate the two WL enable signals. *Id.*

136. But here again, Petitioner provides no reasons why the POSA would use Itoh's 1-to-2, 2-to-4, and 3-to-8 decoders to generate the outputs of Asano's predecoder. Itoh discloses a specific type of decoder, known as a "one-hot decoder." There are many other ways to implement the decoding functions of Asano's predecoder 202, including, for example, zero-hot decoders, balanced decoders, and constant-weight decoders. Petitioner has not provided any reasons why the POSA allegedly would have selected Itoh's one-hot decoder implementation instead of another possible implementation.

137. Additionally, even if the POSA was motivated to implement Asano's predecoder 202 using the decoders of Itoh, this combination would still not yield the claimed invention of the '002 patent. In the claims of the '002 patent, each of the first and second logics performs distinct functions. Among other functions, the first logic receives a clock signal and applies the clock signal to a selected clock output, whereas the second logic selectively activates a particular wordline driver. See, e.g., Ex. 1001 at 10:65-11:10. Asano uses a single predecoder 202 and thus fails to disclose the distinct first and second logics. Itoh does not remedy this deficiency of Asano because Itoh also fails to disclose first and second logics that perform different functions. At most, Itoh discloses standard k -to- 2^k bit decoders—1-to-2 bit, 2-to-4 bit, and 3-to-8 bit decoders. All of Itoh's decoders perform standard decoding functions, and none of Itoh's decoders are configured

to receive a clock signal and apply the clock signal to a selected clock output. Accordingly, Itoh fails to disclose the claimed “first logic” and “second logic” of the '002 patent that perform different functions, and it does not remedy the deficiencies of Asano.

138. For at least these reasons, it is my opinion that the combination of Asano and Itoh does not render claims 1-17, 20-28, and 31-36 obvious.

Declaration

139. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

By:

A handwritten signature in black ink, appearing to read "M Pedram", is written over a horizontal line.

Massoud Pedram, Ph.D.

Appendix A

CURRICULUM VITA

MASSOUD PEDRAM

Personal Information

Charles Lee Powell Chair in Electrical Engineering and Computer Science
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URL: <http://www.mpedram.com/>
Wiki: https://en.wikipedia.org/wiki/Massoud_Pedram

Impact on the Field

- Advancing the theory and practice of energy-efficient computing and introducing methodologies, design solutions, and automation algorithms for reducing power dissipation in electronic circuits and systems, wireless ad hoc networks, computation/communication tradeoffs, wired and wireless routing protocols, and modeling/design of electrical energy storage systems, and power conversion circuitry

Research Interests

- Energy-efficient computing, power-aware design methodologies and techniques, power/timing modeling and analysis in VLSI circuits, power/thermal management and control, power conversion and regulation, smart grid technologies, electrical energy storage systems, embedded systems, power-aware wireless networks and mobile ad hoc networks, cloud computing and data center resource provisioning and management, beyond-CMOS devices and circuits, superconductive electronics

Education

- University of California at Berkeley, Ph.D. in Electrical Engineering and Computer Sciences, 1991
- University of California at Berkeley, M.S. in Electrical Engineering and Computer Sciences, 1989
- California Institute of Technology, B.S. in Electrical Engineering, 1986

Employment History

- Charles Lee Powell Chair in Electrical Engineering and Computer Science in the Viterbi School of Engineering, University of Southern California, 2017-present
- Stephen and Etta Varra Professor in the Viterbi School of Engineering, University of Southern California, 2013-2017

- Professor, Department of Electrical Engineering, University of Southern California, 2000-2012
- Associate Professor, Department of Electrical Engineering, University of Southern California, 1996-2000
- Assistant Professor, Department of Electrical Engineering, University of Southern California, 1991-1996
- Part-time Research Position, Xerox Palo Alto Research Center, 1987-1989
- Graduate Student Researcher, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, 1986-1991

Honors and Awards

- Best Paper Award of the *Asia and South Pacific Design Automation Conference*, Jan. 2019
- USC Viterbi School of Engineering Senior Research Award, 2017
- "For contributions to modeling and design of low power VLSI circuits and systems, and energy efficient computing," *IEEE Circuits and Systems Society Charles A. Desoer Technical Achievement Award*, 2015
- The *Second Most Prolific and Second Most Cited Author Awards* from the 20th Anniversary *Int'l Symp. on Low Power Electronics and Design*, Rome, Italy, Jul. 2015
- *Frequent Author Award* (Top Three Author Award) at the 20th Anniversary *Asia and South Pacific Design Automation Conference*, Chiba/Tokyo, Japan, Jan. 2015
- ACM SIGDA *Distinguished Service Award*, 2014
- Best Paper Award of the *ACM/IEEE Int'l Symp. on Low Power Design and Electronics*, Aug. 2014
- Best Paper Award of the IEEE Computer Society Annual Symp. on VLSI, Jul. 2014
- Recognized as one of the four DAC Prolific Authors (with 50+ papers) and the DAC Bronze Cited Author at the 50th anniversary of the Design Automation Conf., Austin, TX, Jun. 2013
- 2013 DAC Volunteer Service Award sponsored by IEEE CEDA
- Best Paper Awards of the 1989, 2000, and 2012 IEEE Int'l Conference on Computer Design, VLSI in Computers and Processors
- ACM Distinguished Scientist, 2008
- ACM SIGDA Service Award, 2004
- "For contributions to the theory and practice of low-power design and CAD," IEEE Fellow, 2001
- ACM SIGDA Distinguished Service Award, 2000
- Presidential Early Career Award for Scientists and Engineers, 1996
- NSF's Young Investigator Award, 1994
- NSF's Research Initiation Award, 1992
- 2007 IEEE Trans. on Circuits and Systems Guillemin-Cauer Best Paper Award
- Honorable Mention Award at the 2008 Int'l Symp. on Low Power Electronics and Design
- Best Paper Awards of the 33rd ACM/IEEE Design Automation Conference, Jun. 1996 and the 42nd ACM/IEEE Design Automation Conference, Jun. 2005
- Distinguished Paper Citation of the IEEE Int'l Conference on Computer Aided Design, 1990
- 1996 IEEE Circuits and Systems Society VLSI Systems Transactions Best Paper Award

University Service

- Member of the Computer Engineering Faculty Recruitment Committee, 2010-2011, 2013/2014, 2014/2015, 2016-2017
- Member of the VSoE Research Committee at USC, Sept. 2013 - 2017
- Member of the VSoE Transformative Faculty Hire Committee, Sept. 2013 - 2016
- Member of the Ming Hsieh Institute's Advisory Council, Jul. 2013 – Dec. 2015
- Chair of a faculty Promotion Committee in the EE department, 2014/2015, 2016-2017
- Member of the EE Dept. Faculty Recruitment Committee, 2014/2015
- Served on the Best Dissertation Selection Committee in the EE Dept., 2013
- Internal reviewer for an NSF Career Program proposal, 2013
- Chaired committee for evaluating Janet Roveda's Recruitment as an associate professor, 2012
- Division Director of USC Computer Engineering Division, Dec. 2005-Jun. 2010, and Acting Division Director at the end of 2012 and early 2013
- Served as the Chair of the 2005 Distinguished Lecture Series of the EE Dept.
- Served as the Associate Director of the CENG division of the EE Department at USC from 1998 to 2001
- Served on various departmental committees including the Faculty Merit Review Committee, Faculty Recruitment Committee, and the Promotion Committees in the EE department
- Chaired the Outstanding Research Paper Award Committee of the EE-Systems Department at USC in 1999
- Served on the Graduate Student Admissions Committee for entering M.S. and Ph.D. students in the CENG division of the EE-Systems Department at USC

Professional Service

- Participated in and contributed to the Computing Community Consortium (CCC) "Next Steps in Quantum Computing: Computer Science's Role," May 22-23, 2018
- Associate Editor of *Research, A Science Partner Journal*, 2018-present
- Served on the IEEE CASS Fellow (Selection) Committee, 2018
- Executive Committee Chair of the *Int'l Symp. on Low Power Electronics and Design*, July 2012 - present
- Editor-in-Chief of the *ACM Trans. on Design Automation of Electronic Systems*, Jun. 2008–May 2014
- Inaugural Editor-in-Chief of the *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Jan. 2010–Dec. 2013
- Served as a member of the 2011 Selection Committee for the ACM SIGDA Outstanding New Faculty Award
- Served as the Chair of the Selection Committee for the IEEE CEDA and ACM SIGDA 2010 *A. Richard Newton Technical Impact Award in Electronic Design Automation*
- General Co-chair of the 2010 *IEEE Int'l Symp. on Circuits and Systems*, Paris, France
- Associate Editor
 - Foundations and Trends in Electronic Systems and Circuits Journal, Now Publishers, Inc. of Delft, 2006-2014
 - Journal of Low Power Electronics, 2005-2014
 - IEEE Trans. on Computer Aided Design, 1997-2006

- IEEE Trans. on Circuits and Systems I, 2002-2003
- ACM Trans. on Design Automation of Electronic Systems, 1998-2004
- Distinguished Lecturer/Speaker
 - Association for Computing Machinery (ACM), 2007-2015
 - IEEE Solid State Circuits Society, 2001-2007
- VP of Publications of the IEEE Circuits and Systems Society, 2005-2006
- Chair of the Distinguished Lecturer Program, IEEE Circuits and Systems Society, 2003-2004
- Member of the Board of Governors, IEEE Circuits and Systems Society, 2000-2003
- Member of the ACM-SIGDA Advisory Board, managing the ACM Outstanding Ph.D. Dissertation Award in Electronic Design Automation, the DAC Young Student Support Program, the Multimedia Monograph Series, and the SIGDA Technical Committees, 1996-2009
- Chair of the Best Paper Award Committee for the IEEE Trans. on Computer Aided Design, 1999
- Member of the Research or Technical Advisory Board
 - Atrenta Inc., 2003-2015
 - Envis Inc., 2006-2009
 - PwrLite Inc., 2007-2009
 - Fulcrum Microsystems, 2001-2004
 - Aplus Design Technologies Inc., 2000-2003
 - Magma Design Automation Inc., 1997-2002
 - EPIC Design Technology, 1994-1997
- General Chair
 - *Int'l Symp. on Quality of Electronic Design*, San Jose, CA, Apr. 2007
 - *Int'l Symp. on Physical Design*, Monterey, CA, Apr. 2003
 - *Int'l Symp. on Low Power Electronics and Design*, Monterey, CA, Aug. 1997
 - *Int'l Symp. on Low Power Design*, Laguna, CA, Apr. 1995
- Technical Chair
 - *Int'l Symp. on Physical Design*, Del Mar, CA, Apr. 2002
 - *Int'l Symp. on Low Power Electronics and Design*, Monterey, CA, Aug. 1996
 - *Int'l Workshop on Low Power Design*, Napa Valley, CA, Apr. 1994
- Executive Committee Member
 - *Int'l Symp. on Low Power Electronics and Design*, since 1996
 - *Int'l Conference on Computer Aided Design*, since 2006
- Technical Program Committee Member
 - *The 18th CSI International Symposium on Computer Architecture & Digital Systems*, Tehran, Iran, Oct. 7-8, 2015
 - *Int'l Conference on Hardware/Software Codesign and System Synthesis*, 2013-2015
 - *Symp. on Embedded Systems for Real-Time Multimedia (ESTIMedia)*, 2007-2012
 - *Symp. on VLSI Design, Automation and Test (VLSI-DAT)*, 2012
 - 2009 *Great Lakes Symp. on VLSI*
 - 2008 IEEE Int'l Design and Test Workshop, Tunisia
 - *Symp. on VLSI Design, Automation and Test (VLSI-DAT)*, Hsinchu, Taiwan, 2009
 - NanoArch, 2007-2008
 - *The 13th CSI Computer Conference (CSICC'08)*, Kish Island, Iran, March 9-11, 2007
 - Conference on VLSI – *Design Automation Technologies*, Taipei, Taiwan, 2006-2007
 - 1998-2000 *Int'l Conference on Computer Aided Design*
 - 1998-2001 *Int'l Symp. on Physical Design*
 - 1997-2000 *Int'l Workshop on Logic Synthesis*
 - 2000 *Asia and South Pacific Design Automation Conference*

- 1998-2003 *Design Automation and Test in Europe Conference*
- 1994-2000 *Int'l Symp. on Low Power Electronics and Design*
- 2001-2003 *Int'l Symp. on Quality of Electronic Design*

US Patents

- [S1] Pedram; Massoud (Beverly Hills, CA); Iranli; Ali (Los Angeles, CA), United States Patent Filed. "Dynamic backlight scaling for power minimization in a backlit TFT-LCD," United States Patent **8,094,118**, Issued: Jan 10, 2012, Filed: Mar 2, 2006.
- [S2] Fallah; Farzan (San Jose, CA); Pakbaznia; Ehsan (Los Angeles, CA); Pedram; Massoud (Beverly Hills, CA); "Sizing and placement of charge recycling (CR) transistors in multithreshold complementary metal-oxide-semiconductor (MTCMOS) circuit," United States Patent **7,834,684**, Issued: Nov 16, 2010, Filed: Oct 31, 2008.
- [S3] Fallah; Farzan (San Jose, CA); Abdollahi; Afshin (Los Angeles, CA); Pedram; Massoud (Los Angeles, CA); "Power mode transition in multi-threshold complementary metal oxide semiconductor (MTCMOS) circuits," United States Patent **7,613,942**, Issued: November 3, 2009, Filed: May 31, 2006.
- [S4] Fallah; Farzan (San Jose, CA); Amelifard; Behnam (Los Angeles, CA); Pedram; Massoud (Beverly Hills, CA); "Setting threshold voltages of cells in a memory block to reduce leakage in the memory block," United States Patent **7,573,775**, Issued: August 11, 2009, Filed: February 9, 2007.
- [S5] Fallah; Farzan (San Jose, CA); Amelifard; Behnam (Los Angeles, CA); Pedram; Massoud (Beverly Hills, CA); "PG-Gated Data Retention Technique for Reducing Leakage in Memory Cells," United States Patent **7,447,101**, Issued: November 4, 2008, Filed: December 22, 2006.
- [S6] Fallah; Farzan (San Jose, CA); Pakbaznia; Ehsan (Los Angeles, CA); Pedram; Massoud (Beverly Hills, CA); "Recycling Charge to Reduce Energy Consumption During Mode Transition in Multi-Threshold Complementary Metal-Oxide-Semiconductor (MTCMOS) Circuits," United States Patent **7,400,175**, Issued: July 15, 2008, Filed: May 30, 2007.
- [S7] Fallah; Farzan (San Jose, CA), Aghaghiri; Yazdan (Los Angeles, CA), Pedram; Massoud (Los Angeles, CA). "System and method for identifying optimal encoding for a given trace," United States Patent **7,236,107**, Issued: June 26, 2007, Filed: September 20, 2004.
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- [S9] Fallah; Farzan (San Jose, CA); Aghaghiri; Yazdan (Los Angeles, CA); Pedram; Massoud (Los Angeles, CA). "System and method for reducing transitions on address buses," United States Patent **6,834,335**, Issued: December 21, 2004, Filed: August 9, 2002.
- [S10] Fallah; Farzan (San Jose, CA); Aghaghiri; Yazdan (Los Angeles, CA); Pedram; Massoud (Los Angeles, CA), United States Patent **6,813,700** "Reduction of bus switching activity using an encoder and decoder," Issued: November 2, 2004, Filed: June 3, 2002.

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Google Scholar: total citations: 25,452, h-index=80, g-index=133, and i10-index = 399

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2. JM. Chang and M. Pedram. "Energy minimization using multiple supply voltages," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 5, no. 4, Dec. 1997, pages 436-443. [422 citations]
3. K. Choi, R. Soma, and M. Pedram. "Fine-grained dynamic voltage and frequency scaling for precise energy and performance trade-off based on the ratio of off-chip access to on-chip computation times," *IEEE Trans. on Computer Aided Design*, vol. 24, no. 1, Jan. 2005, pp.18-28. [378 citations]
4. M. Pedram and S. Nazarian. "Thermal modeling, analysis and management in VLSI circuits: Principles and methods," *Proc. of IEEE, Special Issue on Thermal Analysis of ULSI*, vol. 94, no. 8, Aug. 2006, pages 1487-1501. [376 citations]
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7. Q. Wu, M. Pedram, and X. Wu. "Clock-gating and its application to low power design of sequential circuits," *IEEE Trans. on Circuits and Systems—I*, vol. 47, no. 3, Mar. 2000, pages 415-420. [330 citations]
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Other Scholarly Publications

- [W1] N. Katam and M. Pedram. "Timing Characterization and Enabling Static Timing Analysis in Rapid Single Flux Quantum Circuits," Presented at *13th Biennial European Conference on Applied Superconductivity* (EUCAS), Geneva, Switzerland, Sept. 2017.
- [W2] N. Katam, A. Shafaei, and M. Pedram. "Design of Complex Rapid Single Flux Quantum Cells with Application to Logic Synthesis," Presented at *16th International Superconductive Electronics Conference* (ISEC), Sorrento, Italy, Jun. 2017.
- [W3] S. Nazar Shahsavani, A. Shafaei, C. J. Fourie, and M. Pedram. "An Integrated Cell Placement and Interconnect Synthesis Tool for Large-scale SFQ Logic Circuits," Presented at *Applied Superconductivity Conference* (ASC), Denver, United States, Sept. 2016.
- [W4] T. Cui, Y. Wang, S. Nazarian, and M. Pedram. "Statistical static timing analysis based on current source modeling of ASIC gates," *ICCAD Workshop on Variability Modeling and Characterization*, Nov. 2013.
- [W5] A. Abdollahi and M. Pedram. "Efficient Synthesis of Quantum Logic Circuits by Rotation-based Quantum Operators and Unitary Functional Bi-decomposition," *Proc. of Int'l Workshop on Logic and Synthesis*, Jun. 2005.
- [W6] S. Nazarain and M. Pedram. "Sensitivity-based gate delay propagation in static timing analysis," *ACM/IEEE Int'l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, Feb. 2005.
- [W7] A. Iranli, K. Choi and M. Pedram. "Energy-aware wireless video streaming," *Proc. of 1st Workshop on Embedded Systems for Real-Time Multimedia*, Oct. 2003, pages 48-53.
- [W8] CW. Kang and M. Pedram. "Technology mapping for low leakage power with hot-carrier effect consideration," *Proc. of Int'l Workshop on Logic Synthesis*, May 2002, pages 295-300.
- [W9] A. Abdollahi, F. Fallah, M. Pedram. "Runtime mechanisms for leakage current reduction in CMOS VLSI circuits," *Proc. of Int'l Workshop on Logic Synthesis*, May 2002, pages 419-424.
- [W10] P. Rezvani and M. Pedram. "Concurrent extraction of partial kernels with timing consideration," *Proc. of Int'l Workshop on Logic Synthesis*, May 2001, pages 213-218.
- [W11] Y. Aghaghiri, F. Fallah, M. Pedram. "ALBORZ: Address Level Bus Power Optimization," *Proc. of Int'l Workshop on Logic Synthesis*, May 2001, pages 332-337.
- [W12] P. Rezvani, A.H. Ajami, M. Pedram, and H. Savoj. "LEOPARD: A logical effort-based fanout optimizer for area and delay," *Proc. of Int'l Workshop on Logic Synthesis*, May 1999.

- [W13] P. Cocchini, M. Pedram, G. Piccinini, and M. Zamboni. "Fanout optimization under a submicron transistor-level delay model," *Proc. of Int'l Workshop on Logic Synthesis*, May 1998.
- [W14] J. Lou, A. Salek, and M. Pedram. "An exact solution to simultaneous technology mapping and linear placement problem for trees," *Proc. of Int'l Workshop on Logic Synthesis*, May 1997, session 4, paper 4.
- [W15] S. Iman and M. Pedram. "POSE: A power optimization and synthesis environment," *Proc. of TechCon*, Sept. 1996.
- [W16] CS. Ding and M. Pedram. "A comparative study of switching activity estimators," *Proc. of Int'l Workshop on Power and Timing Modeling, Optimization, and Simulation*, Oct. 1995, pages 377-396.
- [W17] H. Vaishnav and M. Pedram. "Logic extraction using fanin ranges," *Proc. of Int'l Workshop on Power and Timing Modeling, Optimization, and Simulation*, Oct. 1995, pages 331-349.
- [W18] S. B. K. Vrudhula, YT. Lai, and M. Pedram. "Efficient computation of the probability and Reed-Muller spectra of Boolean functions using EVBDDs," *Proc. of IFIP WG 10.5 Workshop on Application of Reed-Muller Expansions in Circuit Design*, Chiba, Japan, Aug. 1995, pages 4.1-4.8.
- [W19] H. Vaishnav and M. Pedram. "A new method for performance oriented logic extraction," *Proc. of Int'l Workshop on Logic Synthesis*, May 1995, pages 1.53-1.59.
- [W20] K. R. Pan and M. Pedram. "LUT-based FPGA synthesis for low power," *Proc. of Int'l Workshop on Power and Timing Modeling, Optimization, and Simulation*, Oct. 1994, pages 124-131.
- [W21] D. Mukherjee, M. Pedram, and M. A. Breuer. "CONSYST - an integrated test controller synthesis system," Presented at the *Int'l Test Synthesis Workshop*, May 1994.
- [W22] J. Monteiro, S. Devadas, B. Lin, CY. Tsui, M. Pedram, and A. M. Despain. "Exact and approximate methods of switching activity estimation in sequential logic circuits," *Proc. of 1994 Int'l Workshop on Low Power Design*, Apr. 1994, pages 117-122.
- [W23] C. Ding and M. Pedram. "Efficient symbolic simulation under the extended bounded delay model," *Proc. of Tau'93: Int'l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, Sept. 1993.
- [W24] S. Iman, M. Pedram, C. Fabian, and J. Cong. "Finding uni-directional cuts based on physical partitioning and logic restructuring," *Proc. of 4th ACM/IEEE Physical Design Workshop*, Apr. 1993, pages 187-198.
- [W25] M. Pedram, B. S. Nobandegani, and B. T. Preas. "On the segmentation design and routability analysis for row-based FPGAs," *Proc. of 4th ACM/IEEE Physical Design Workshop*, Apr. 1993, pages 213-214.
- [W26] YT. Lai, KR. Pan, M. Pedram, and S.Vrudhula. "FGMap: a technology mapping algorithm for Look-Up Table Type FPGAs based on function graphs," *Proc. of Int'l Workshop on Logic Synthesis*, pages 9b.1-9b.4, May 1993.
- [W27] M. Pedram, N. Bhat, K. Chaudhary, S. Mayrhofer, and E. S. Kuh. "Layout considerations in combinational logic synthesis," *Proc. of Int'l Workshop on Logic Synthesis*, May 1991, pages 11.1-11.16.
- [W28] M. Pedram, W-W. Dai, M. Marek-Sadowska, and Y. Ogawa. "Ongoing research and development of BEAR layout," *Proc. of Int'l Workshop on Layout Synthesis*, May 1990, pages 1-17.

Invited Talks and Tutorials

- [T1] M. Pedram. "Design Automation Methodology and Tools for Superconductive Electronics," Invited talk at the *Int'l Conf. on Computer Aided Design*, Nov. 7, 2018.
- [T2] M. Pedram. "ColdFlux: CAD Methodologies and Tools for Single Flux Quantum Based Superconductive Electronics," Invited talk at the *Applied Superconductivity Conference*, Nov. 1, 2018.
- [T3] M. Pedram. "Energy-Efficient Computing: Datacenters, Mobile Devices, and Mobile Clouds," Keynote Speech of the *Int'l Symp. on Green Computing*, Oct. 23, 2019
- [T4] M. Pedram. "An Ultra-Low-Power High-Speed Cache Memory Comprising of Hybrid TFET-FinFET SRAM Cells," Invited talk at the Int'l Conf. on Solid State Materials and Devices, Sep. 11. 2018.
- [T5] M. Pedram. "ColdFlux: CAD Methodologies and Tools for Single Flux Quantum Based Superconductive Electronics, Project Progress Report," talk given at the First Annual Program Review Meeting, IARPA SuperTools program, Aug. 28, 2018.
- [T6] M. Pedram. "ColdFlux: CAD Methodologies and Tools for Single Flux Quantum Based Superconductive Electronics," Presentation at the IARPA SuperTools Site Visit, Jun. 20, 2018.
- [T7] M. Pedram. "ColdFlux: CAD Methodologies and Tools for Single Flux Quantum Based Superconductive Electronics--Project Progress Report," Presentation at the IARPA SuperTools Technical Exchange Meeting 1, Apr. 10, 2018.
- [T8] M. Pedram. "Coldflux: CAD Tools and Methodologies for SFQ-based Superconductive Electronics." Presentation at the IARPA SuperTools Kickoff meeting, 30 Oct. 2017
- [T9] M. Pedram and C. Fourie. "Summary and Perspectives of the Seedling on SCE Design Tools and Methodologies," Presentation at the IARPA C3 Team Meeting, Baltimore, MD, 26 Oct. 2017.
- [T10] M. Pedram. "VINE: A Variational Inference-Based Bayesian Neural Network Engine." Presentation to DARPA MTO, Los Angeles CA, 8 Aug. 2017.
- [T11] M. Pedram, S. Chen, and E. Eshratifar. "Game Theoretic Approaches to Cyber Security," Presentation to DARPA MTO, Los Angeles CA, 27 Jun. 2017.
- [T12] N. Katam, A. Shafaei, and M. Pedram. "Design of Complex Rapid Single-Flux-Quantum Cells with Application to Logic Synthesis," Presentation at the Intern. Superconductive Elec. Conf., Sorrento (Napoli), Italy, 13 Jun. 2017.
- [T13] M. Pedram. "Design flow and tool chain for Synthesis and Physical Design of SFQ Circuits. IARPA C3 PI meeting, Baltimore, MD, 7 Apr. 2017.
- [T14] M. Pedram. "Review of Superconductive Electronics Technology and SFQ Circuit Design." Presentation at ARM Research (arranged by IARPA), Austin TX, 6 Mar. 2017.
- [T15] M. Pedram and C. Fourie. "Design, Optimization, and Demonstration of an FPGA Device for SFQ Circuits and Hybrid SFQ/FinFET Memory," Presentation to IARPA, Baltimore, MD, 21 Feb. 2017.
- [T16] M. Pedram and Y. Wang. "SpiNN-SC: Stochastic Computing-Based Realization of Spiking Neural Networks," Presentation to DARPA MTO, Los Angeles CA, 17 Feb. 2017.
- [T17] "Inference and Learning with Bayesian Neural Networks: Architecture and Hardware Realization," Invited presentation at DARPA MTO SAGA Concept Summit, Dayton OH, Nov 14, 2016
- [T18] "Designing Energy-Efficient and High-Performance VLSI Circuits and Systems in 7nm FinFET Technology," Presentation at Samsung Austin R&D Center Technical Forum, Austin TX, Oct. 18, 2016
- [T19] "Cell Library Design and an Integrated Place & Route Tool for RSFQ Logic", Invited Presentation at IARPA C3 Program Review Meeting, Baltimore, MD, Sept. 30, 2016

- [T20] "Designing Energy-Efficient and Robust Circuits in 7nm FinFET Technology," Talk at Cadence Distinguished Speaker Series, San Jose, CA, Sept. 21, 2016
- [T21] "Designing Energy Efficient Circuits and Systems on Chip," Presentation at CDN Live Event, Santa Clara CA, Apr. 6 2016
- [T22] "Power Management and Low-Power Design Techniques," Two-day tutorial at the Qualcomm Inc., San Diego, CA, Dec. 8-9, 2015.
- [T23] "Design Optimization and Power/Performance Characterization of Sub-10 nm Devices and Logic Cells," Invited talk at the *Workshop on Modeling & Simulation of Systems and Applications (ModSim)*, Seattle, WA, Aug. 13, 2015.
- [T24] "Designing Energy-Efficient Information Processing Systems: Lessons Learned and the Path Forward," Keynote (banquet) speech at the Int'l Conf. on Computer Design, Seoul, Korea, Oct 20, 2014.
- [T25] "Designing Energy-Efficient Information Processing Systems," Invited talk at the Nanyang Technological University, Singapore, Jan. 22, 2014.
- [T26] "Energy Efficient Datacenters," Half-day tutorial at the *Asia and South Pacific Design Automation Conf.*, Singapore, Jan. 20, 2014.
- [T27] "Energy-Driven Design and Optimization of Electronic Circuits and Servers,"
 - a. Presentation at SNU-ESRC and Samsung ATTI Joint Workshop, Soul, South Korea, Sept. 9, 2013.
 - b. Presentation at Energy Efficient Design Institute, Beijing University, Beijing, China, Sept. 6, 2013.
- [T28] "Designing Energy-Efficient Information Processing Systems,"
 - a. EE Dept., Hong Kong University of Science and Technology, Dec. 3, 2013.
 - b. Eminent Scholar Seminar Series speaker, Texas A&M University, Nov. 12, 2013.**
 - c. Sharif University of Technology, Tehran, Iran, Sept. 29, 2013.
 - d. Samsung Advanced Technology Training Institute, Sept. 11, 2013.
 - e. EE Dept., Yale University, Apr. 5, 2013.
- [T29] "Reducing Energy Cost and Environmental Impacts of Information Processing and Communications Systems," **ISTeC Distinguished Lecture, Colorado State University**, Oct. 21, 2013.
- [T30] "Creating a Sustainable Information and Communication Infrastructure," **Keynote Speaker, Design Automation and Test in Europe Conf., Grenoble, France**, Mar. 19, 2013.
- [T31] "Design and Optimization of Electrical Energy Storage Systems," Mitsubishi webinar, April 4, 2012.
- [T32] "Design and Optimization of Electrical Energy Storage Systems," MIT Electrical Engineering Dept., Cambridge, MA, February 145, 2012.
- [T33] "Robust Performance Optimization of Chip Multiprocessors under Power and Thermal Constraints," Presentation at the Atrenta TAB Meeting, November 30, 2011.
- [T34] "Energy Efficient Computing and Information Processing," Presentation at the DASAN Conf., Jeju Island, South Korea, Sponsored by the Korean Federation of Science and Technology Societies, November 3, 2011.
- [T35] "Demand-Side Load Scheduling Incentivized by Dynamic Energy Prices," Presentation at the Smart Grid Workshop, San Diego Convention Center, June 9, 2011.
- [T36] "Green Computing: Reducing Energy Cost and Carbon Footprint of Information Processing Systems," ACM DSP Lecture, United Arab Emirates University, Al Ain, UAE, May 11, 2011

- [T37] "Robust Design of Power-Efficient VLSI Circuits," Keynote speech at ISPD, Santa Barbara, CA, March 28, 2011.
- [T38] "Hybrid Electrical Energy Storage Systems," Joint tutorial with Prof. N. Chang, Presentation at the ISQED, March 14, 2011.
- [T39] "Variability-Aware Power-Efficient Circuits and Systems," Presentation at Broadcom Inc., February 4, 2011.
- [T40] "Energy Efficient Enterprise Computing," Presentation at the Second IEEE Summer School in Cuzco, Peru, January 19, 2011.
- [T41] "Energy Efficient Enterprise Computing and Hybrid Energy Storage Systems," Sharif University of Technology, Tehran, Iran, October 3, 2010.
- [T42] "Sustainable Digital Infrastructure: Reducing Energy Cost and Life Cycle Environmental Impacts of Information Processing and Communications Systems," Presentations at
 - a. CADS Conf., IPM, Tehran, Iran, September 23, 2010,
 - b. Global Center of Excellence in VLSI Design, Waseda University, Tokyo, Japan, June 28, 2010
- [T43] "Energy Efficient Enterprise Computing and Green Data Centers," Invited talks and/or presentations at
 - a. Keynote Speech at Smart Energy Day, Integrated Systems Center, EPFL, Lausanne, Switzerland, December 14, 2010
 - b. Keynote Speech at SASIMI workshop, Taipei, Taiwan, October 18, 2010,
 - c. Workshop on IT and Future Society, Jeju Island, South Korea, October 8, 2010,
 - d. Seoul National University Seminar, Seoul, South Korea, October 7, 2010,
 - e. KAIST Seminar, Daejeon, South Korea, October 7, 2010,
 - f. Northrop Grumman Technology Day, USC, May 6, 2010,
 - g. 4th Annual THU-USC Faculty Forum on Green and Smart for a Sustainable Future, USC, April 1, 2010,
 - h. LADWP Green Datacenters Workshop, Los Angeles, CA, February 25, 2010,
 - i. EE Dept. of University of California, Los Angeles, February 22, 2010,
 - j. ECE Dept. of University of California, San Diego, November 19, 2009.
- [T44] "Future of Publishing," Panelist presentation at the IEEE Int'l Conf. on Computer Aided Design, San Jose California, November 2, 2009.
- [T45] "Energy Efficient Enterprise Computing," Presentation at IEEE CANDE Workshop, Monterey, California, Oct. 30, 2009.
- [T46] "Energy Efficient Enterprise Computing," Presentation at Intel Research, Hillsboro, Oregon, Oct. 29, 2009.
- [T47] "Green Computing: Reducing the Carbon Footprint of Information Processing Systems in an Energy-Constrained World," Keynote talk given at the 18th *Int'l Conf. on Computer Communications and Networks (ICCCN)*, San Francisco, CA, Aug. 3, 2009.
- [T48] "Energy-Efficient Computing," Tutorial given at the *ACM SIGDA DA Summer School*, San Francisco, CA, Jul. 25, 2009.
- [T49] "Green Computing: Reducing Energy Cost and Carbon Footprint of Information Processing Systems," Keynote talk given at the *Great Lakes Symp. on VLSI in Boston*, Massachusetts, May 11, 2009.
- [T50] "Power-Efficient Servers and Green Data Centers," Presentation given at Fujitsu Central, Tokyo Japan, Feb 19, 2009.

- [T51] "Minimizing Power Density and Energy Consumption in VLSI Circuits and Systems," Talk Given at Graduate School of Information, Production and Systems, Waseda University, Fukuoka, Japan, February 17, 2009
- [T52] "Green Data Centers," Presentation given as the introduction to a session with the same title at the 2008 Int'l Conf. on Computer Aided Design, San Jose CA, Nov. 10, 2008.
- [T53] "ASIC Design with Dynamic Voltage Scaling," Envis Corp, Santa Clara, CA, Aug. 5, 2008.
- [T54] "Minimizing Leakage Power in CMOS: Technology Issues," EPFL, Lausanne, Switzerland, July 15, 2008.
- [T55] "Electrical Cell Modeling using Current Sources," ExtremeDA, Santa Clara, CA, Jun. 26, 2008.
- [T56] "Power Minimization in VLSI Circuits," Atrenta Meeting, San Jose, CA, May 22, 2008.
- [T57] "Advances in Statistical Modeling and Characterization of Combinational and Sequential Logic Cells Using Current Source Models," IBM TJ Watson Research, White Plains, NY, Apr. 3, 2008.
- [T58] "Coarse-Grain Power Gating in ASIC Designs," ECE Seminar at the Carnegie-Mellon University, Pittsburgh, PA, Feb 14, 2008.
- [T59] "Low-Leakage SRAM Design in Deep Submicron Technologies," Invited talk at the EE Dept. of the Seoul National University, Seoul, South Korea, Jan. 25, 2008.
- [T60] "Design Challenges and Solutions for MTCMOS Circuits," Lecture at LSI Logic, Milpitas, CA, Mar. 26, 2007.
- [T61] "Physical Design Challenges for Row-Based MTCMOS Circuits," Keynote speech, Great Lakes Symp. on VLSI, Stresa-Lago Maggiore, Italy, March 12, 2007.
- [T62] "Circuits and architectures targeting ultra low power," *SSCS DLP Lecture*, Univ of Texas, Austin, Nov. 16, 2006.
- [T63] "More Moore: Manufacturing Challenges, System Drivers, and Design Technology Solutions for Late-Silicon Age and Beyond," Keynote speech, *Int'l SoC Design Conf.*, Seoul, South Korea, Oct 26, 2006.
- [T64] "New laws / cycles that could 'destroy' the EDA industry," *CANDE Workshop*, Whistler, British Columbia, Canada, Sept. 22, 2006.
- [T65] "Power-aware VLSI Design Methodologies and Techniques," *IEEE Circuits and Systems Society Workshop in New and Emerging Technologies*, Buenos Aires, Argentina, March 20, 2006.
- [T66] "Models and Techniques for Active and Leakage Power Minimization in CMOS VLSI Circuits," *FTFC Workshop*, Paris, France, April 20, 2005.
- [T67] "Canonical Representation and Direct Synthesis of Quantum Circuits," Univ of Leuven, Belgium 11, March 2005 and JPL, Pasadena, CA, Sept. 11 2005.
- [T68] "Circuit and Architectural Optimization Techniques for Power Minimization in CMOS VLSI Circuits and Systems," Broadcom, Irvine, CA, May 6, 2005.
- [T69] "Design of a Variable-Band UWB Radio with Integrated Power Management," DARPA/MTO ULP Workshop, Washington D.C., Aug. 4, 2005.
- [T70] "Circuit and Design Automation Techniques for Power Minimization in CMOS VLSI Circuits," *VLSI-TSA Symp.*, Taiwan, 2005.
- [T71] "Timing Analysis for UDSM Technologies," Synopsys Inc., Mountain View, CA, Mar. 11, 2005.
- [T72] "Best Practices in Low-Power Design: Power Reduction Techniques," Half-Day Tutorial at ICCAD, jointly with E. Macii, Nov. 11, 2004.
- [T73] "Energy-Awareness in Distributed Battery-Powered Systems," Univ of California, Irvine, May 12, 2004.

- [T74] "Quo Vadis Multimedia? From Desktop Multimedia to Distributed Multimedia Systems," Embedded tutorial at European Design and Test Conf., Jointly with R. Marculescu and J. Henkel, Feb. 19, 2004.
- [T75] "Design and Runtime Techniques for Leakage Control and Minimization of CMOS VLSI Circuits in Active and Sleep Modes," Full day tutorial at Asia and South Pacific Design Automation Conf., jointly with F. Fallah, Jan. 27, 2004.
- [T76] "Energy-Aware Networked Multimedia Systems: Modeling, Analysis and Optimization," Full day tutorial at Asia and South Pacific Design Automation Conf., jointly with R. Marculescu, Jan. 21, 2003.
- [T77] "Power-aware On-Demand Routing in Mobile Ad Hoc Networks," *IEEE CAS Workshop on Wireless Communications and Networking, Focus Area: Power Efficient Wireless Ad hoc Networks*, Pasadena, California, Sept. 5, 2002.
- [T78] "System-wide Power Optimization and Control in the Apollo Testbed," Ecole Polytechnique de Montreal, Canada, SSCC Distinguished Lecturer, Mar. 2002
- [T79] "System-wide Power Optimization and Control in the Apollo Testbed," tutorial given at *ACEED 2002 / Austin Conf. on Energy-Efficient Design*, IBM Austin Research Lab, Feb. 2002.
- [T80] "An integrated model for battery and circuit co-design," tutorial given at ASP-DAC, Jan. 1999.
- [T81] "Logical-physical co-design for deep submicron circuits," tutorial given at ASP-DAC, Jan. 1998.
- [T82] "Performance and Power Optimization in Synthesis and Layout of VLSI Circuits and Systems," full-day tutorial at the European Design Automation Conf., Geneva, Switzerland, Sept. 20, 1996 (jointly with Prof. J. Cong).
- [T83] "Low Power Design in Microelectronics," lectures at the NATO Advanced Study Institute Summer Course in Il Ciocco, Italy, Aug. 1996.
- [T84] "Design technologies for Low Power LSI," full-day tutorial at the 1st Asia and South Pacific Design Automation Conf., Chiba, Japan, Aug. 29, 1995 (jointly with Dr. A. Matsuzawa, Dr. T. Sakurai, and Prof. A. Chandrakasan).
- [T85] "Low power design: a systems perspective," full-day tutorial at the 32nd Design Automation Conf., San Diego, CA, Jun. 16, 1995 (jointly with Prof. J. Rabaey and Dr. J. Kardach).
- [T86] "Design solutions and challenges for low power systems," full-day tutorial at the 1994 Int'l Conf. on Computer Aided Design, Santa Clara, CA, Nov. 10, 1994 (jointly with Prof. J. Rabaey).
- [T87] "Low power system design: solutions and challenges," full-day tutorial at the 31st Design Automation Conf., San Diego, CA, Jun. 17, 1994 (jointly with Prof. J. Rabaey).