IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the *Inter Partes* Review of U.S. Patent No. 6,356,122

Trial No.: IPR2015-00148

Issued: March 12, 2002

Filed: August 4, 1999

Inventors: Piyush Sevalia, *et al.*

Assignee: PLL Technologies, Inc.

Title: CLOCK SYNTHESIZER WITH PROGRAMMABLE INPUT- OUTPUT PHASE RELATIONSHIP

DECLARATION OF DONALD ALPERT, Ph.D., UNDER 37 C.F.R.§ 1.68, IN SUPPORT OF PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

I, Dr. Donald Alpert, do hereby declare:

1. I am making this declaration in support of Petitioner's Reply to Patent Owner's Response at the request of Xilinx, Inc. ("Xilinx") in the matter of the *Inter Partes* Review of U.S. Patent No. 6,356,122 ("the '122 patent"), Case No. IPR2015-00148.

2. I previously submitted a declaration in this matter. [Ex. 1010] In that Declaration, I provided my opinions concerning the patentability of certain claims of the '122 patent in consideration of the prior art references of Exhibits 1003 – 1009. Of these references, U.S. Patent No. 4,611,230 ("Nienaber") (Ex. 1003) and U.S. Patent No. 5,446,867 ("Young") (Ex. 1004) are discussed below.

3. In preparing this Declaration, I have been asked to review Patent Owner's Response (Paper 14) and the Declaration of Dr. John P. Hayes (Ex. 2002), prepared on behalf of the Patent Owner. In preparing this Declaration, I also considered the following materials:

- Institution Decision (Paper 8);
- Exhibits 2001- 2012, submitted by the Patent Owner;
- Patent Owner Preliminary Response (Paper 6);
- *IEEE Standard Glossary of Computer Hardware Terminology*, IEEE Std 610.10-1994 (Ex. 1013);
- McCharles, R.H. and Hodges, D., "Charge circuits for analog LSI," in IEEE Transactions on Circuits and Systems, vol. 25, no.7, Jul 1978, pp. 490-497 (Ex. 1015);
- U.S. Patent No. 3,691,297 to Merrell, et al. (Ex. 1016);
- U.S. Patent No. 3,426,344 to Clark (Ex. 1017);
- IEEE Standard Dictionary of Electrical & Electronics Terms (6th ed. 1996) (selected pages) (Ex. 1018);
- Transcript of November 20, 2015 Deposition of John Hayes (Ex. 1019);
- U.S. Patent No. 5,654,657 to Pearce (Ex. 1020);
- U.S. Patent No. 5,706,004 to Yeung (Ex. 1021);
- U.S. Patent No. 2,931,024 to Slack (Ex. 1023);
- Wilcox, Milton, "A Highly Stable Integrated Sync System," in IEEE Transactions on Consumer Electronics, vol. CE-24, no.3, Aug. 1978, pp. 284-290 (Ex. 1024);
- Doyle, N.; Hamaoui, H.; Nichols, J., "Some Applications of Digital Techniques in TV Receivers," in IEEE Transactions on Broadcast and

Television Receivers, vol. BTR-18, no.4, Nov. 1972, pp. 245-249 (Ex. 1025); and

- U.S. Patent No. 4,409,665 to Tubbs (Ex. 1026).

4. In this Declaration, I document certain issues where I disagree with the opinions expressed in Patent Owner's Response or Dr. Hayes' Declaration. My silence in this Declaration about any other issue in no way means that I agree with opinions on that issue expressed in Patent Owner's Response or Dr. Hayes' Declaration.

5. In my previous declaration [Ex. 1010], I provided a summary of my professional background and qualifications, relevant legal standards, and summaries of the '122 patent and the references of Exhibits 1003 through 1009.

I. Claim Construction for "clock"

6. In Ex. 2002 at Section VII.A, Dr. Hayes documents his opinion that the broadest reasonable interpretation of the term "clock" for the '122 patent is a "periodic signal used for synchronization in a digital system." [Ex. 2002 par. 42] The basis for Dr. Hayes' opinion starts with citations to definitions for the term "clock" that appear in in the *IEEE Standard Dictionary of Electrical and Electronics Terms* ("IEEE Standard Dictionary"), including "a periodic signal used for synchronization." [Ex. 2002 par. 40, citing Ex. 2007 at p. 163] In my opinion, this IEEE Standard Dictionary definition is consistent with the broadest

reasonable interpretation of the term, as well as with the Board's interpretation of "a periodic timing control signal" [Paper 8 at p. 9].

A clock is not limited to digital systems.

7. In Ex. 2002 at par. 42, Dr. Hayes contends that the interpretation for clock should be further limited beyond the IEEE Standard Dictionary's definition to digital systems only: "[a] periodic signal used for synchronization in a digital system." The basis documented for this opinion includes two contentions: (1) the IEEE Standard Dictionary limits the cited definition of "clock" to digital computer systems, and (2) the term "clock" has no recognized meaning in connection with analog circuits. These contentions are wrong for at least the reasons explained below. Similarly, I disagree with Patent Owner's contention that goes beyond the scope of Dr. Hayes' declaration: "the IEEE Dictionary demonstrates that a 'clock' signal is *inherently* for digital systems." [Paper 14 at. p. 12, emphasis added]

8. Dr. Hayes asserts that the IEEE Standard Dictionary definition for "clock" should be limited to digital systems because the cited definition relates to the field of computers.

> **42.** All of the definitions of the term "clock" or "clock signal" are in the "C" category, which signifies "computer." Since all the relevant definitions of the term "clock" in the IEEE Dictionary originate from the field of computers or at least digital systems, the interpretation of the term "clock" in this case should be as follows: "Periodic signal used for synchronization in a digital system."

[Ex. 2002 at par. 42]

9. This assertion is incorrect at least because the definitions from the "computer" category are not limited to digital systems. Rather, the "computer" category includes definitions for numerous analog and mixed signal terms. For example, the "computer" category includes the following definitions for "analog," "analog computer," "hybrid circuit," and "operational amplifier":

analog (1) (analog computer) Pertaining to representation by means of continuously variable physical quantities; for example, to describe a physical quantity, such as voltage or shaft position, that normally varies in a continuous manner, or devices such as potentiometers and synchros that operate with such quantities. (C) 165-1977w
(2) (data transmission) Used to describe a physical quantity, such as voltage or shaft position, that normally varies in a continuous manner. (PE) 599-1985w
(3) Pertains to information content that is expressed by signals dependent upon magnitude. *See also:* control system, feedback. (IA) [60]
(4) (computers) Pertaining to data in the form of continuously variable physical quantities. *Contrast:* digital. *See also:* analog computer. (C) 1084-1986w, 610.10-1994

[Ex. 1018 p. 9]

analog computer (1) (A) (general) An automatic computing device that operates in terms of continuous variation of some physical quantities, such as electrical voltages and currents, mechanical shaft rotations, or displacements, and that is used primarily to solve differential equations. The equations governing the variation of the physical quantities have the same or very nearly the same form as the mathematical equations under investigation and therefore yield a solution analogous to the desired solution of the problem. Results are measured on meters, dials, oscillograph recorders, or oscilloscopes. *See also:* simulator. **(B) (direct current)** An analog computer in which computer variables are represented by the instantaneous values of voltages. **(C) (alternating current)** An analog computer in which electrical signals are in the form of amplitude modulated suppressed carrier signals where the absolute value of a computer variable is represented by the amplitude of the carrier and the sign of a computer variable is represented by the phase (0° or 180°) of the carrier relative to the reference alternating-current signal. (C) 165-1977w **(2)** A computer that processes analog data. *Synonym:* electronic analog computer. *Contrast:* digital computer; hybrid computer. *See also:* ac analog computer; dc analog computer. (C) 610.10-1994

[Ex. 1018 p. 9]

hybrid circuit (A) A circuit, usually in the form of a module or substrate, that is made up of discrete components and integrated circuits. *Contrast:* monolithic integrated circuit. **(B)** A circuit that uses a combination of digital and analog components, modes of operation, or techniques. (C) 610.10-1994

[Ex. 1018 p. 12]

operational amplifier (1) (analog computer)

1) An amplifier, usually a high-gain dc amplifier, designed to be used with external circuit elements to perform a specified computing operation or to provide a specified transfer function.
2) An amplifier, usually a high-gain dc amplifier, with external circuit elements, used for performing a specified computing operation.

Notes: 1. The gain and phase characteristics are generally designed to permit large variations in the feedback circuit without instability. 2. The input terminal of an operational amplifier (1) is the summing junction of an operational amplifier (2) and is generally designed to draw current that is negligibly small relative to signal currents in the feedback impedance. (C) 165-1977w

(2) A two-input amplifier designed to perform control or mathematical operations by means of an external feedback circuit connecting the output to one input, and very high gain for voltage differences of either polarity at the inputs. *Note:* Operational amplifiers are used in analog computers to provide mathematical operations such as summing and integration. *See also:* integrating amplifier; summing amplifier. (C) 610.10-1994

[Ex. 1018 pp. 14-15]

10. The "computer" category of the IEEE Dictionary includes definitions for numerous other analog and mixed signal terms. [See, e.g., Ex. 1018 at 8 ("ac analog computer"), 10 ("dc analog computer"), 11 ("gain integrator"), 12 ("hybrid computer"), and 13 ("integrating amplifier")]

11. At deposition, Dr. Hayes stated that "it's possible there are terms among what I suspect are thousands of terms that might appear under the C category that are possibly analog or mixed signal." [Ex. 1019, 31:20-32:10]

Dr. Hayes is correct – there are many analog and mixed signal terms included in the "C" category of the IEEE Dictionary. Dr. Hayes' argument that all of the definitions in the "C" category are related to digital systems is erroneous.

12. Further, as shown in the definitions reproduced above, many of the definitions in the "C" category are from the IEEE Standard 610.10-94, which has the title *IEEE Standard Glossary of Computer Hardware Terminology*. The definitions of this standard relate to computer hardware, as the title indicates, but the definitions are not limited to digital systems, as shown by the definitions reproduced above. Specifically, the overview of IEEE Standard 610.10-94 describes the Standard's scope as follows: "This glossary defines terms pertaining to computer hardware. It includes terms from the following areas[,]" where the areas include "general circuit concepts" and "analog computer concepts." [Ex. 1013 p. 7]

13. Consequently, Dr. Hayes and Patent Owner's argument fails to recognize the breadth of the "C" category of the IEEE Dictionary. Not all definitions in the "C" category are related to digital systems (e.g., the category includes a definition for "analog computer," as noted above). At least in light of the computer category's breadth, it is improper to read the phrase "in a digital system" into the definition of "clock," as proposed by Dr. Hayes and Patent Owner.

Dr. Hayes' testimony that clock signals are used only in digital systems is erroneous.

14. Dr. Hayes has stated that there is no such thing as an "analog clock signal" and that clock signals are only used in digital systems. [Ex. 1019, 26:8-9; Ex. 2002 pars. 39-46.] Dr. Hayes is incorrect. For example, Exs. 1020 and 1021, U.S. Patent Nos. 5,654,657 and 5,706,004, respectively, both disclose analog clock signals. U. S. Patent 5,654,657 [Ex. 1020], titled "Accurate Alignment Of Clocks In Mixed-Signal Tester" and issued on August 5, 1997, discloses techniques for synthesizing an analog clock signal used in a tester for mixed-signal integrated circuits (ICs). A mixed-signal IC has both digital and analog subsystems, and is commonly tested using a tester that controls the device's inputs and observes the device's outputs according to deterministic, reproducible patterns. Such testing practice allows the digital subsystem to be tested synchronously with a digital clock input, but requires an analog clock signal to be aligned with the digital clock. The analog subsystem is tested with the analog clock signal. [Ex. 1020 at 4:7-9 ("[Analog] [c]lock signal generator 200 provides a clock signal for use in a first analog channel . . . .")]

[57] **ABSTRACT**

Asynchronously-generated digital and analog clocks in a mixed-signal test system are accurately aligned for repeatable and deterministic testing. A variable-frequency digital master clock signal is used in direct digital synthesis of an analog clock signal which is asynchronous to the master clock signal. A resync command inhibits the analog clock signal until the analog clock signal is in a desired phase relationship to the master clock signal. The analog clock signal is thus phase-aligned with the master clock signal in a known and deterministic relationship. The resync command also aligns the phase of the analog clock signal with the pattern of stimulus signals applied to the device under test. Aligning the analog clock signal with the master clock signal and with the stimulus pattern assures that test results are consistent from test-to-test. A phase-locked loop removes spurs from the synthesized analog clock signal. A jitter generator is provided for controlled jittering of the analog clock signal as needed for some types of test. An Nth occurrence counter allows for programmable introduction of an extra master-clock signal period in the test pattern when needed to avoid creating a metastable condition in the device under test.

[Ex. 1020 at Abstract, emphasis added]

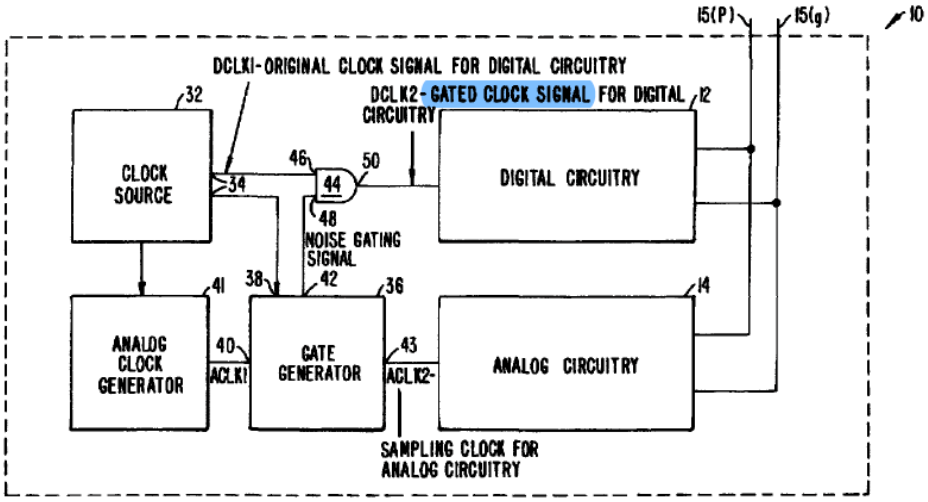
15. Similarly, U. S. Patent No. 5,706,004 [Ex. 1021], which was issued on January 6, 1998, discloses techniques for reducing noise coupling between analog and digital circuits in a mixed-signal integrated circuit. More specifically, the patent discloses gating off a digital clock[1] during periods when an analog clock signal triggers the sampling of analog signals.

[1] Dr. Hayes attempts to introduce an additional requirement that a clock signal cannot be gated: "…and it is generally considered a poor design practice to process a clock signal, as passing a clock signal through a logic gate creates a propagation

[57] **ABSTRACT**

A system for reducing noise coupling in a mixed-signal IC includes a digital clock, an analog clock, and gating signal generator, and a gating circuit. The gating circuit receives a digital clock signal and the gating pulse to generate a gated digital clock signal having no pulses at a sampling edge of the analog clock signal to provide a "quiet time" for analog sampling.

[Ex. 1021 at Abstract, emphasis added; see also 1:13-31, 2:44-65]



[Ex. 1021 Fig. 1, emphasis added]

16. As described above, Exs. 1020 and 1021 both disclose analog clock signals. Dr. Hayes' assertion that analog clock signals do not exist is erroneous.

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delay that skews the clock, causing the clocks signals before and after the gate to have a phase difference. An old adage of digital design is 'never gate a clock.'" [Ex. 2002 par. 62] I disagree with the contention that a clock cannot be gated; U. S. Patent 5,706,004 expressly refutes this contention by disclosing "a gated digital clock signal." [Ex. 1021 at Abstract, 2:17-18, 5:4]

II. Claim Construction for "programmable delay circuit"

17. In Ex. 2002 at Section VII.B, Dr. Hayes documents his opinion that the broadest reasonable interpretation of the term "programmable delay circuit" for the '122 patent requires a "memory" for accepting data and/or instructions for programming the programmable delay circuit. [Ex. 2002 pars. 47-53] I disagree with Dr. Hayes for the reasons stated below.

The '122 patent does not require a "memory" for configuring or adjusting a programmable delay circuit.

18. As acknowledged by Dr. Hayes at deposition [Ex. 1019, 34:3-10], the word "memory" does not appear anywhere in the claims of the '122 patent. Further, the specification of the '122 patent also does not require a memory for configuring or adjusting a programmable delay circuit. To the contrary, the '122 patent expressly describes programmable delay circuits that are configured or adjusted without the use of a memory. I described this in my previous declaration, Ex. 1010, at paragraphs 33 and 43. As detailed in these paragraphs, the specification of the '122 patent discloses that delay times of a programmable delay circuit can be set by various means that do not require a memory, including blowing fuses and changing a metal mask. For example, a fuse or metal mask can be used to configure the programmable delay circuit during manufacture by hardwiring circuit inputs to a logic 0 or 1. Dr. Hayes agrees that a metal mask is not a memory device. [Ex. 1019, 38:22-23]

19. Based on the above, it is my opinion that Dr. Hayes' proposed narrowing of the term "programmable delay circuit" is not supported by the '122 patent.

A memory is not "inherently necessary" to accept data and/or instructions for configuring a programmable delay circuit.

20. Dr. Hayes cites the IEEE Dictionary's definition of "programmable" and concludes that based on this definition, the term should be defined as "capable of accepting data and/or instructions to alter a device's state to perform specific task(s) or to alter its basic function." [Ex. 2002 par. 48] Not content with this definition, Dr. Hayes states that "[t]he IEEE definition refers to the capability of 'accepting' data and/or instructions (IEEE Dictionary at 826), and a memory is inherently necessary to accept the data and/or instructions." [Ex. 2002 par. 49]

21. Dr. Hayes' statement that "a memory is inherently necessary to accept the data and/or instructions" is erroneous. As explained above, the '122 patent describes that a delay time of a programmable delay circuit can be configured or adjusted by various means that do not require a memory, such as via the one-time programming techniques of blowing fuses and changing a metal mask. [Ex. 1001, 4:37-45.] Such configuration techniques are examples where data, namely the associated configuration information, is accepted by the programmable delay circuit to alter its delay time, with no memory being required to accept the data.

Furthermore, as described below (see Section IV), one-time programming without the use of a memory is also disclosed in the Young reference (Ex. 1004), which is intrinsic evidence cited during the '122 patent's prosecution.

22. Based on the above, a person having ordinary skill in the art would understand that a "programmable delay circuit" does not require a "memory."

III. Nienaber Discloses a Hybrid System That Uses a Digital Clock Signal for Timing Control

23. In Ex. 2002 at Section VIII.A, Dr. Hayes documents his opinion that the vertical sync signal disclosed by Nienaber is not a "clock" because (1) the vertical sync signal for an NTSC television receiver disclosed by Nienaber is used in a purely analog system, not a digital system [Ex. 2002, par. 54, stating that Nienaber discloses an "analog television," and par. 57, stating that Nienaber's disclosed computer monitors are "analog CRT (cathode ray tube) devices"], (2) the vertical sync signal for a computer monitor functions the same as in a television receiver, and (3) vertical sync signals must be processed, whereas clock signals are not typically processed. [Ex. 2002 par. 54, 57, 61, and 62] Notably, Dr. Hayes agrees that Nienaber's vertical sync signal is periodic and used for synchronization, as the signal's name implies. [Ex. 2002 par. 61, stating "[T]he incoming vertical sync signal [of Nienaber] is a periodic signal used for synchronization or timing control . . . ."] Dr. Hayes' objection depends entirely on

his contention that the claim construction for "clock" should be limited to digital systems; as explained above, I disagree that the claim construction of "clock" should be limited to digital systems.

24. As noted above, Dr. Hayes argues that Nienaber is a purely analog system, and that therefore, it cannot disclose the claimed clock signals. [Ex. 2002, par. 54, stating that Nienaber discloses an "analog television," and par. 57, stating that Nienaber's disclosed computer monitors are "analog CRT (cathode ray tube) devices"] But even assuming that purely analog systems do not use clock signals, as Dr. Hayes contends, such a contention would be irrelevant because Nienaber does not disclose a purely analog system. Rather, Nienaber discloses a hybrid system (*i.e.*, mixed signal system) that utilizes a digital clock signal for timing control. This is explained below.

Dr. Hayes' characterization of Nienaber's system as purely analog is erroneous.

25. Dr. Hayes' assertion that televisions were at least predominantly, if not entirely, analog devices in the mid 1980's is incorrect. From the time of early television receivers in the 1940's-1950's until the mid 1980's, much analog circuitry had been replaced or augmented with digital technology, for example to display text on-screen for channel numbers, closed-captioning, and teletext. By the early-1970's, the transition from analog to digital circuit techniques was underway,

as explained in Ex. 1025, the paper "Some Applications Of Digital Techniques in TV Receivers" published in the IEEE Transactions on Broadcast and Television Receivers in 1972. Digital techniques for television receivers were economical, technically feasible, and necessary to meet regulatory requirements.

> *"Until comparatively recently the concept of using digital methods in consumer equipment was dismissed as impractical, unnecessary and prohibitively expensive. New developments in semiconductor technology, transmission systems and FCC regulations have brought about a situation where digital techniques are now not only economically and technically feasible but also necessary. Some of the factors involved include the availability of complex MOS LSI {Large Scale Integration) devices, the National Bureau of Standards time code transmission system and the UHF tuning parity regulations. This paper will endeavor to discuss these factors and how they may affect future TV receiver design."* [Ex. 1025 at p. 245]

26. More specifically, it was known to use digital vertical sync circuits for both television receivers and computer monitors with analog CRTs (cathode ray tubes), as explained below. Thus, a person having ordinary skill in the art would have understood that by the early 1980's, television receivers and computer monitors were not entirely analog systems, but instead were hybrid systems that commonly deployed a combination of digital and analog circuits.

27. The IEEE Standard Dictionary [Ex. 1018 at 12] defines "hybrid circuit" as follows:

> ***hybrid circuit*** *– A circuit that uses a combination of digital and analog components, modes of operation, or techniques. (C) 610.10-1994*

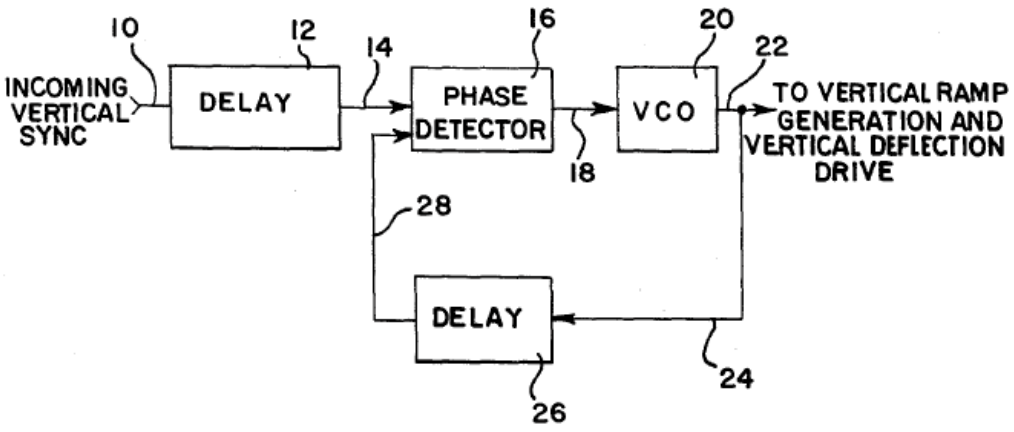
28. At deposition, Dr. Hayes stated that the terms "hybrid circuit" and "mixed signal circuit" can be used interchangeably. [Ex. 1019, 27:25-28:11] I agree with this statement.

29. Nienaber discloses that the preferred embodiment for his invention is in conjunction with a computer monitor, and that the invention can also be used with a standard television receiver for a vertical sync signal that has been separated from the composite video signal.

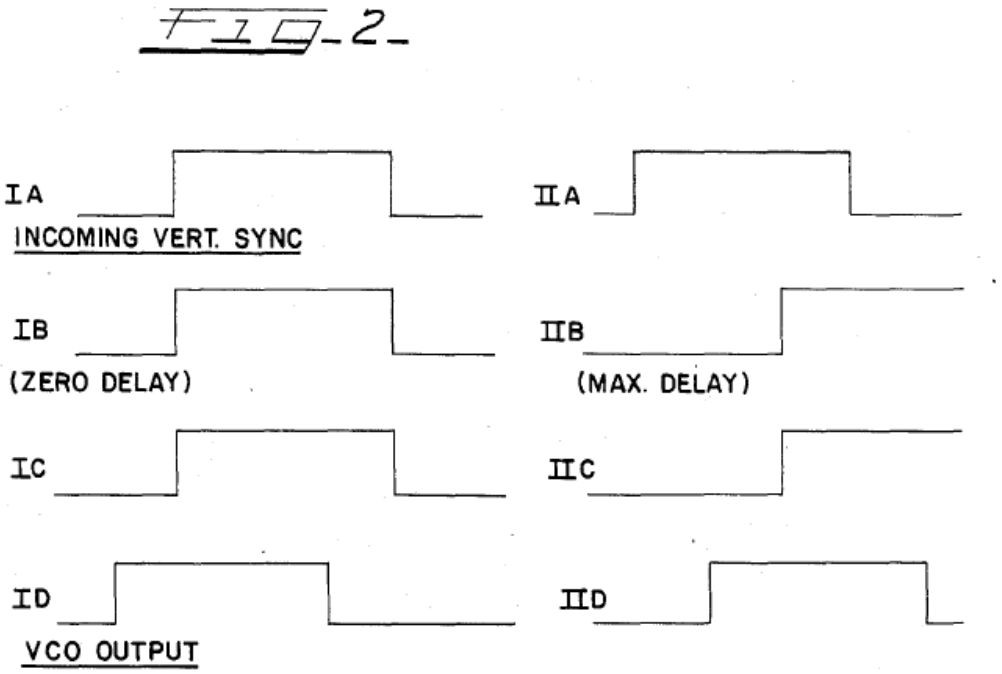
> *"Although it is envisioned that the present invention may be utilized in a preferred environment with a video monitor in conjunction with computers or other non-standard television applications, the present invention may be readily used in any circuitry for which a separate vertical sync signal may be supplied or derived. For example, in a standard television receiver, the vertical sync signal may be separated and supplied to the circuitry of the preferred embodiment."* [Ex. 1003, 3:34-42]

30. Nienaber discloses that the incoming vertical sync signal is input 10 to the circuit shown in Fig. 1. A typical waveform for the incoming vertical sync signal is shown in Fig. 2, labeled IA and IIA. [Nienaber Fig. 1, Fig. 2, 3:8-11, 4:24-30, 4:57-61] At deposition, Dr. Hayes stated that the incoming vertical sync

signal shown in Nienaber's Fig. 2 is a digital signal [Ex. 1019, 42:8-16], and I agree with this. A person of ordinary skill in the art would understand that the incoming vertical sync signal disclosed by Nienaber is a digital signal at least because the waveform of Fig. 2 shows that the signal takes on discrete values. This is the true for applications in either a computer monitor or standard television. Similarly, the output signal (22 labeled ID and IID) and internal signals (14 labeled IB and IIB, 28 labeled IC and IIC) are digital signals, and thus Nienaber's circuit uses digital techniques to process digital signals. [Nienaber 4:24-5:18]



[Nienaber Fig. 1]



[Nienaber Fig. 2]

31. Computer monitors were known to use digital vertical sync signals at least 15 years before the filing date of Nienaber. For example, U.S. Patent No. 3,426,344, which was issued to Clark in 1969 and assigned to RCA, discloses a digital vertical sync signal (V. SYNC.) that is a periodic signal used for synchronization or timing control in a computer monitor. [Ex. 1017] Sync Generator 36 outputs the digital V. SYNC. signal, as well as a SYNC signal that controls analog vertical deflection circuit 42 to position the CRT beam on the screen. [Ex. 1017, Fig. 3, 5:4-24, 6:28-57] Thus, U.S. Patent No. 3,426,344 discloses a computer monitor with hybrid circuitry, combining digital and analog techniques, where a digital vertical sync signal is used for synchronization or timing control.

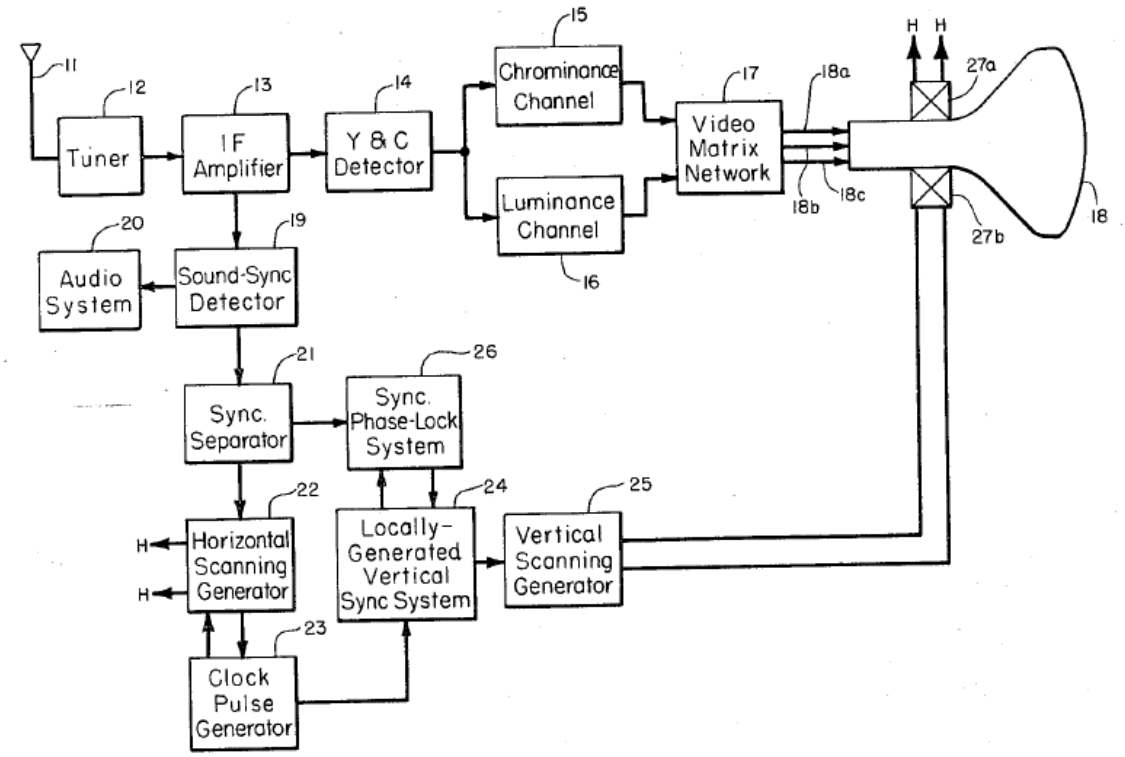
32. By the early 1980's, display monitors attached to personal computers, such as IBM PCs, commonly received a separate digital vertical sync directly from the computer's graphics adapter. [Ex. 2011, 71:4-72:5] Nienaber discloses that the vertical sync signal for computer monitors depends on the computer manufacturer's specifications and that his circuit is compatible with various systems, both computer monitors and television receivers. [Ex. 1003 1:29-35, 1:48-51]

33. At deposition, Dr. Hayes stated that computer monitors in the mid-1980s used digital vertical sync signals. [Ex. 1019, 44:6-9] I agree with this statement, as shown by the discussion above.

34. Similarly, by the early 1980's, television receivers were known to use a digital vertical sync signal. For example, Ex. 1016, U.S. Patent No. 3,691,297, published in September 1972 and assigned to Zenith Radio Corporation, describes known benefits of digital vertical synchronization systems in television receivers, including improved noise immunity and elimination of the external vertical hold control, such as a user-adjustable knob for a potentiometer in older televisions. [Ex. 1016, 1:12-51]

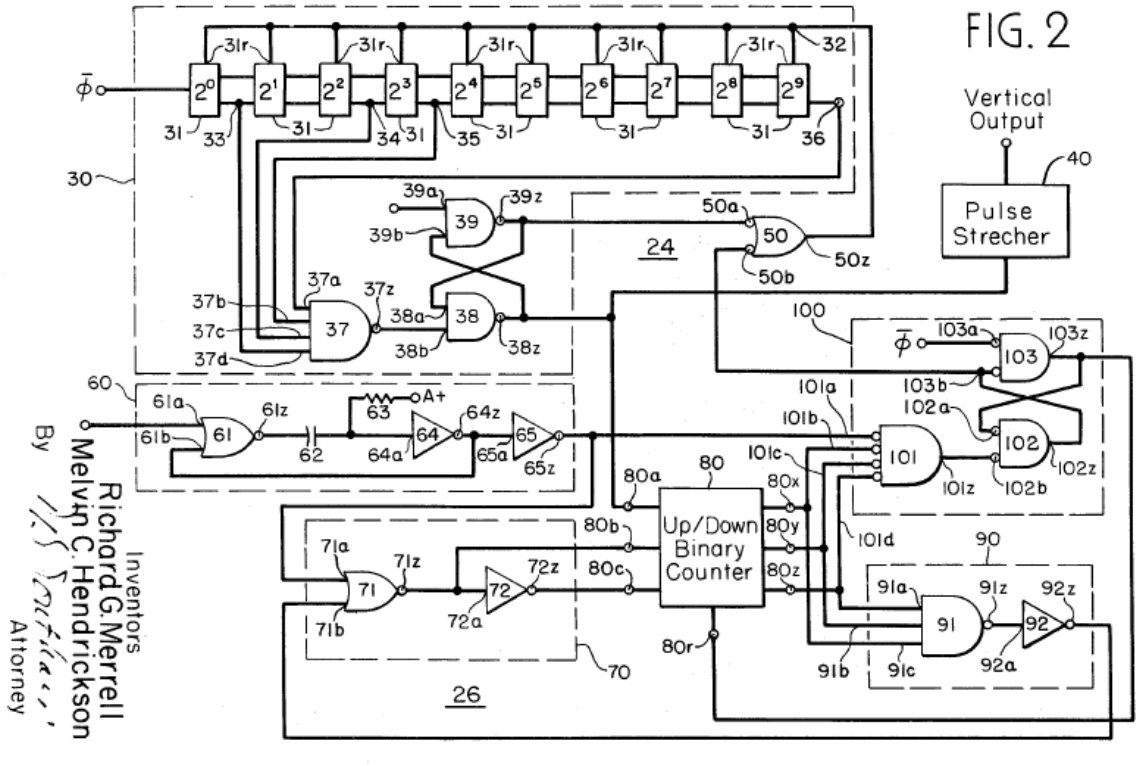
35. Ex. 1016 also discloses a hybrid circuit with a digital vertical sync signal used to control digital circuits and the analog CRT retrace. For example, the digital vertical sync signal (*38z* of Fig. 2) controls timing of the up/down binary counter 80 and also controls timing of the vertical scanning generator 25, which

outputs analog signals to control the vertical deflection yoke 27b. [See Ex. 1016, 4:9-18 and 7:6-9]



[Ex. 1016 Fig. 1]

In turn, a locally generated vertical synchronization system 24 is coupled to the output of clock pulse generator 23 thereby developing locally generated vertical synchronization pulses from the clock pulse train. The locally generated vertical synchronization pulses are then coupled to a vertical scanning generator 25 wherein appropriate scanning signals are developed for application to the appropriate deflection yoke 27b positioned about the image reproducer 18. [Ex. 1016, 4:9-18]



[Ex. 1016 Fig. 2]

36. For another example, Milton Wilcox published a paper in the IEEE Transactions on Consumer Electronics in August 1978, which described the National Semiconductor Corporation LM1880 horizontal/vertical sync system chip. [See Ex. 1024] The chip includes a digital circuit that counts horizontal sync pulses to generate a digital vertical sync signal, as well as an analog circuit that uses an RC delay to generate the vertical retrace signal. [See Ex. 1024 at pp. 286, 289, and Figs. 7 and 10]

37. Thus, digital vertical sync circuits were widely available by the early 1980s, including proprietary circuits for television manufacturers, such as RCA

and Zenith, and from chip vendors, like National Semiconductor. These circuits generated digital vertical sync signals that were used in televisions at this time.

38. At deposition, Dr. Hayes stated that televisions in the mid-1980s used digital vertical sync signals. [Ex. 1019, 43:7-9] I agree with this statement, as shown by the discussion above.

39. Based on the above, a person having ordinary skill in the art would have understood that by the early 1980's, television receivers and computer monitors, such as those described by Nienaber, were not entirely analog systems, but instead were hybrid systems that commonly deployed a combination of digital and analog circuits. These hybrid systems used digital vertical sync signals, as acknowledged by Dr. Hayes [Ex. 1019, 43:7-9 and 44:6-9] and as shown in Fig. 2 of Nienaber. [See Ex. 1019, 42:8-16, Dr. Hayes referring to incoming vertical sync signal shown in Nienaber's Fig. 2 and stating "The figure shows a digital signal."] Dr. Hayes' characterization of Nienaber's system as purely analog is erroneous.

Hybrid systems commonly use clock signals for timing control.

40. Hybrid systems commonly use clock signals for timing control.[2] For example, the paper "Charge Circuits for Analog LSI," [Ex. 1015] describes general usage of clock signals in a variety of hybrid circuits and provides explanations for specific circuits.

> *"Problems in analog LSI can be reduced by using the **clocked** analog circuits discussed here,"* [Ex. 1015 p. 490, emphasis added]
>
> *"In this circuit, as in all other circuits, we will assume a two-phase nonoverlapping **clock**, and that positive voltage, switch closure, and logic one are all equivalent."* [Ex. 1015 p. 490, emphasis added]
>
> *"Charge circuits are **clocked** quasi-static[1] analog circuits which use the **clock** as a reference for time-dependent functions."* [Ex. 1015 p. 491, emphasis added]
>
> *[1]Quasi-static means that the transient behavior of the circuit during any **clock** cycle has no effect on the behavior of the circuit during subsequent cycles."* [Ex. 1015 p. 491, emphasis added]
>
> *"Charge circuits minimize some problems that have limited the size of analog integrated circuits. RC time constants are eliminated by using a **clock** as a time reference."* [Ex. 1015 p. 496, emphasis added]

[2] At deposition, Dr. Hayes stated that the terms "hybrid circuit" and "mixed signal circuit" can be used interchangeably. [Ex. 1019, 27:25-28:11] I agree with this statement.

41. "Charge Circuits for Analog LSI" at Fig. 1 (reproduced below), shows a hybrid circuit with two capacitors (C_1 and C_2) and switches (S_1 and S_2) that are controlled by a two-phase non-overlapping clock (Φ_1 and Φ_2). The digital clock signal provides periodic timing control by opening and closing switches S_1 and S_2 based on the state, i.e., phase, of the clock. "The two switches of the filter are connected to the clock phases as shown so that in each clock cycle a charge of (Vin – Vout)*C_2 is transferred from C1 to C2." [Ex. 1015 p. 490] This hybrid circuit combines analog components (e.g., capacitors and switches) with digital control (clock signal phases) to function like a purely analog RC low-pass filter.

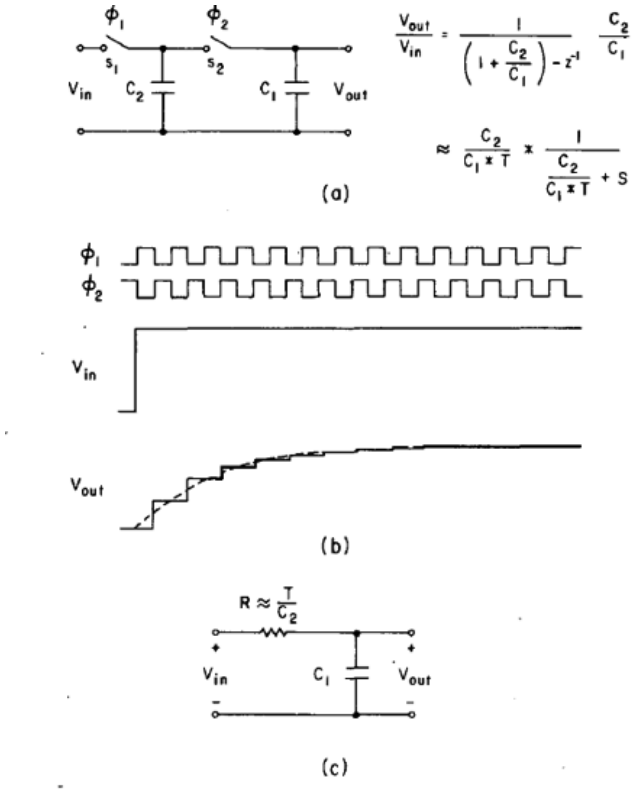


Fig. 1. (a) Charge circuit filter. (b) Step response. (c) Equivalent continuous time filter.

[Ex. 1015 p. 490]

42. "Charge Circuits for Analog LSI" describes additional examples of hybrid circuits that use clock signals for timing control, including a clocked analog inverter and delay element, an analog shift register, D/A and A/D converters, analog filters, and analog arithmetic circuits: "By combining one sum and delay stage with analog storage and digital logic, any analog function can be performed." [Ex. 1015 p. 494, Figs. 3, 4, 6, 8-11]

43. Additional examples of hybrid systems using clock signals for timing control are shown in Exs. 1020 and 1021, as discussed above in Section I.

44. Further, hybrid circuits that perform analog-to-digital conversion under timing control of a digital clock were know at least four decades before the '122 patent was filed. For example, U.S. Patent No. 2,931,024 [Ex.1023], which was filed in 1957, describes a hybrid analog-to-digital converter that comprises analog circuits (e.g., comparison amplifier 272, current switch 126, voltage regulator 258, and clamp 260) and digital circuits (e.g., converter control flip-flop 54, sequencing flip-flops 1-8, and subtract pulse gate 72) under control of a digital clock (64). [Ex. 1023 Fig. 1-2, 6:9-36, 7:30-58, 7:60-8:3, 4:69-5:5, 3:23-35, 5:28-6:2, 5:12-26]

45. Based at least on the references described above, a person having ordinary skill in the art would understand that clocks are used in hybrid systems (i.e., mixed signal systems) for timing control. The person having ordinary skill in

the art would know this at least based on that person's training (e.g., circuit design classes) and experience (e.g., using analog-to-digital converters).

Nienaber's incoming vertical sync signal and output signal are periodic digital signals used for timing control in a hybrid system and thus disclose "clocks."

46. Nienaber's incoming vertical sync signal and output signal (labeled 22 in Nienaber's Fig. 1) are digital, periodic signals used for synchronization or timing control of a vertical retrace function in a hybrid system or a mixed signal system. Thus, a person of ordinary skill in the art would understand these signals to be clock signals.

Dr. Hayes' statement that clock signals are not processed is incorrect.

47. Dr. Hayes argues that Nienaber's vertical sync signal is not a clock because "clock signals are not typically processed" and "it is generally considered a poor design practice to process a clock signal." [Ex. 2002 par. 62] As explained above in Section I, this contention is an attempt to place a further claim construction limitation on "clock," namely that a "clock" cannot be "processed," such as by gating the clock. Such a limitation has no support in the intrinsic evidence or the IEEE Standard Dictionary definition for "clock" upon which Dr. Hayes relies for his claim construction analysis. U. S. Patent 5,706,004, Ex, 1021, cited above in Section I, provides an example of a gated clock that refutes Dr. Hayes' contention. Furthermore, I disagree with Dr. Hayes' contention

because a person having ordinary skill in the art would know that "clock gating" has been a well-known technique for reducing power consumption of microelectronic circuits since at least the 1970s. For example, U.S. Patent No. 4,409,665 to Graham S. Tubbs from Texas Instruments, discloses the use of clock gating for a hand-held calculator. [Ex. 1026, 2:17-39]

IV. Young discloses a "programmable delay circuit."

48. As the Board has recognized (Paper 8 at 15-19), Young's delay line 27 discloses a programmable delay circuit. In my previous declaration, I discuss Young's disclosure of a programmable delay circuit. [Ex. 1010, pars. 117-121.]

49. PLL argues that Young does not disclose a memory, and that therefore, the delay line 27 is not programmable. [Response at 41-42; Ex. 2002, par. 64] I disagree with PLL's claim construction argument for the reasons detailed above in Section II. Moreover, Young discloses that its delay line 27 is programmed using the same methods that are used in embodiments of the '122 patent. Specifically, the '122 patent describes that its programmable delay circuit can be "one-time programmable," with its delay value being set during fabrication of the chip. ['122 patent, 4:37-45] The one-time programming achieved during chip fabrication may be carried out using fuses or metal masks, as stated in the '122 patent. When such one-time programming is used, the delay value of the delay circuit cannot be changed subsequently. Young similarly discloses that a

delay value of its delay line 27 can be set during manufacturing, specifically, when the chip is bonded to the package. [Ex. 1004, 3:67-4:10] In Young, when the delay value is set in this manner, the delay value cannot be changed subsequently. In both the '122 patent and in Young, a programmable delay circuit is configured during manufacture by hardwiring circuit inputs to a logic 0 or 1.

50. At deposition, Dr. Hayes acknowledged that Young discloses setting a delay value of a delay circuit during manufacture, such that the delay value cannot be changed subsequently. [Ex. 1019, 45:11-20] Dr. Hayes further acknowledged that one-time programming, as referred to in the '122 patent, means that a delay value is set once and cannot be changed again or changed easily. [Ex. 1019, 37:19-22.] I agree with Dr. Hayes on both points and note again the similarities in the programming of the '122 patent and Young.

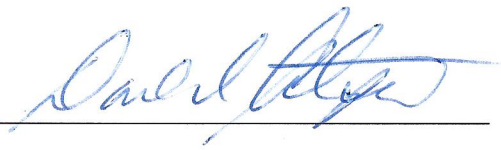
51. Dr. Hayes further testified that in Young, metal masks and fuses could be used to set a delay time of the delay line 27. [Ex. 1019, 45:25-46:11] I agree with Dr. Hayes on this point and note that the '122 patent discloses the use of metal masks and fuses for carrying out one-time programming of its programmable delay circuit.

52. Young also discloses that its delay line 27 can be programmed following manufacturing via input pins connected to a system circuit board.

[Ex. 1004, 4:10-14] Such programming via input pins is the same as is used in embodiments of the '122 patent. ['122 patent, 4:39-43]

V. Declaration

53. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

By: 

Donald Alpert, Ph.D.