

1 UNITED STATES PATENT AND TRADEMARK OFFICE

2
3 BEFORE THE PATENT TRIAL AND APPEAL BOARD

4
5 Apple Inc.,

6 Petitioner,

7 v.

8 Qualcomm Incorporated,

9 Patent Owner.

10
11 Case IPR2018-1249

12 U.S. Patent No. 7,693,002

13
14
15 ORAL DEPOSITION OF ROBERT W. HORST, Ph.D.

16 MARCH 20, 2019

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19
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21
22 Reported by:

23 Dana Welch, CSR, RPR, CRR

24 Job 157424

25 QUALCOMM EXHIBIT 2005

Apple v. Qualcomm

IPR2018-01249

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March 20, 2019

10:02 a.m.

Deposition of ROBERT W. HORST, Ph.D., held
at the offices of Fish & Richardson P.C., One
Marina Park Drive, Boston, MA 02210-1878, before
Dana Welch, Certified Shorthand Reporter,
Registered Professional Reporter, Certified
Realtime Reporter and Notary Public of the
Commonwealth of Massachusetts.

1 APPEARANCES:

2 For the Petitioner:

3 FISH & RICHARDSON

4 BY: WHITNEY REICHEL, ESQ.

5 KENNETH HOOVER, ESQ.

6 One Marina Park Drive

7 Boston, MA 02210

14 For the Patent Owner:

15 JONES DAY

16 BY: DAVID COCHRAN, ESQ.

17 North Point

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19 Cleveland, OH 44114

1 HORST

2 P R O C E E D I N G S

3 ROBERT W. HORST, Ph.D.,

4 having been first duly sworn on oath,
5 was examined and testified as follows:

6 EXAMINATION

7 BY MR. COCHRAN:

8 Q. Good morning.

9 A. Good morning.

10 Q. Thanks for coming.

11 Can you go ahead and state your name,
12 please, full name.

13 A. Robert Horst.

14 Q. Robert Horst.

15 And you have a Ph.D., correct?

16 A. Yes.

17 Q. I'll probably call you Dr. Horst during
18 the course of the deposition. I hope that's okay.
19 Or sir; I'm sure that's okay with you, too.

20 A. Yes.

21 Q. Can you tell us what your home address is,
22 sir?

23 A. 1182 Glenn Avenue in San Jose, California.

24 Q. And you understand that you're under oath
25 this morning, right?

1 HORST

2 A. Yes.

3 Q. Is there any reason that you can't testify
4 truthfully today?

5 A. No.

6 Q. Great.

7 Dr. Horst, have you been deposed before?

8 A. Yes.

9 Q. How many times?

10 A. Not sure exactly, but it's over a dozen
11 times.

12 Q. Over a dozen times.

13 When was the last time you were deposed?

14 A. The last time was in another IPR last
15 year.

16 Q. Do you remember what that matter was?

17 A. I could look at my CV and give you the
18 exact numbers. I can't remember the IPR number,
19 but it was a computer networking IPR.

20 Q. Were you testifying on behalf of Apple in
21 that IPR?

22 A. No.

23 Q. Were you engaged by Fish & Richardson in
24 that IPR?

25 A. No.

1 HORST

2 Q. Have you been engaged by Fish & Richardson
3 previously?

4 A. Yes, I have.

5 Q. Approximately how many times have you been
6 engaged by Fish & Richardson?

7 A. About two other times.

8 Q. And what did those matters relate to?

9 A. They were other computer design type
10 matters, IPRs.

11 Q. So the deposition today is going to relate
12 to your declaration in IPR2018-01249.

13 Is that your understanding?

14 A. Yes.

15 Q. Great.

16 So I'm handing the court reporter, she's
17 now handing to you what has previously been marked
18 as Apple 1003.

19 I'm going to ask you whether you recognize
20 this document, Dr. Horst?

21 MS. REICHEL: Do you have a copy?

22 MR. COCHRAN: Yes, I do.

23 A. This is my declaration related to patent
24 7,693,002.

25 Q. Could you turn to page 75 of Apple 1003,

1 HORST

2 Dr. Horst. Is that your signature on page 75?

3 A. Yes, it is.

4 Q. Thank you.

5 Did you write this document, Dr. Horst?

6 A. Yes. I wrote this document in conjunction
7 with counsel.

8 Q. Can you explain the process you went
9 through from the beginning of when you started
10 writing the document until its final form?

11 MS. REICHEL: I'll just caution the
12 witness, the parties do have an agreement not to
13 take discovery on the drafting process or the
14 substance of communications with counsel.

15 If you have any questions about what
16 you're able to reveal and not reveal in response to
17 counsel's question, please let me know. But you
18 can go ahead and respond with that caveat.

19 A. I don't know what I can reveal and not
20 reveal about those conversations with counsel.

21 Q. How long did it take you to create the
22 document?

23 A. I started on this case in early 2018, and
24 so the document has been in process since then,
25 including all the stages of finding and reviewing

1 HORST

2 prior art and doing figures and actually drafting
3 the document.

4 Q. Inside your declaration, there are several
5 drawn figures that you created; is that right?

6 A. Yes.

7 Q. Approximately how much time have you spent
8 on this matter, Dr. Horst?

9 A. I haven't separately accounted for my time
10 on this matter versus another IPR I'm working for,
11 so I don't know what the split would be.

12 Q. Can you approximate?

13 A. It would be hard to break it down. I
14 really wouldn't know.

15 Q. 100 hours?

16 MS. REICHEL: Objection, calls for
17 speculation.

18 A. I really don't know if it would be over or
19 under 100 hours.

20 Q. Are there any mistakes in your
21 declaration?

22 A. There's nothing that I have found at this
23 point that would be a mistake, but it's possible
24 that I've overlooked something.

25 Q. Are there any opinions set forth in the

1 HORST

2 declaration that you'd like to change?

3 A. No. There are no opinions that I would
4 change at this time.

5 MR. COCHRAN: By the way, I'm not throwing
6 those at you. It's the only way I can get it to
7 you.

8 MS. REICHEL: The numbers on the bottom of
9 these, may I just ask were those on the original
10 documents or were they appended in preparation for
11 the deposition to be exhibit numbers or what was
12 the source of those?

13 MR. COCHRAN: That's a good question. I
14 believe those were put on there by Fish &
15 Richardson when the IPRs were filed.

16 MS. REICHEL: And you're not planning to
17 use a different exhibit number consistent --

18 MR. COCHRAN: I'm not. I'm going to use
19 your numbers.

20 Q. So the court reporter has handed you a
21 document that is marked Apple 1004.

22 Do you recognize this document, Dr. Horst?

23 A. Yes. This is a version of my CV that was
24 submitted along with my declaration.

25 Q. Is this a current copy of your CV?

1 HORST

2 A. I currently have a more up-to-date version
3 of the CV that has a few more items.

4 Q. Can you take a look at pages 3, 4, 5 of
5 the CV, Dr. Horst. This appears to include a list
6 of patents which list you as an inventor; is that
7 correct?

8 A. That's correct.

9 Q. Is this list current?

10 A. No. There are currently four more patents
11 that have issued since I produced this document.

12 Q. Do any of these patents relate to the
13 subject matter of the '002 patent?

14 MS. REICHEL: Objection to form.

15 A. There are several of these patents that
16 relate to memory design and circuit design, and
17 I've called those out in my expert report.

18 Q. Can you take a look at page 6 of the CV.
19 This appears to be a list of publications that name
20 you as an author, starting on page 6, going through
21 page 8.

22 Do you see that?

23 A. Yes.

24 Q. And is this list current?

25 A. Yes. This list is current. I have no new

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publications since this version of the CV.

Q. Thank you, sir.

The court reporter has now handed you a document that's been marked Apple 1001.

Do you recognize this document, Dr. Horst?

A. Yes. This is the Lin patent, the 7,693,002 patent which is the subject of this IPR.

Q. So for purposes of the deposition today, I'm going to generally refer to this as the '002 patent.

Is that okay with you?

A. Yes.

Q. That's how we refer to these.

In connection with the preparation of your declaration which we've previously marked as Apple 1003, did you review the '002 patent?

A. Yes, I did.

Q. How many times have you read it?

A. I haven't counted them up, but I've read it many times.

Q. Did you review the entire document?

A. Yes. I reviewed the entire document.

Q. Approximately how long would you say you've spent studying the '002 patent, Dr. Horst?

1 HORST

2 A. I can't really estimate that. I've always
3 done it in conjunction with reviewing other
4 materials.

5 Q. Can you turn to Figure 1 of Apple 1001.

6 Figure 1 is a block diagram of a wordline
7 driver system labeled 100, correct?

8 A. Yes.

9 Q. And in Figure 1, there is a 6-bit memory
10 address specifying one of 64 wordlines in a memory
11 array; is that right?

12 A. The 6-bit address will select one of 64
13 wordlines of the array.

14 Q. And Figure 1 includes a 2 to 4-bit decoder
15 marked 112, and a 4 to 16-bit address decoder
16 marked 108; is that correct?

17 A. That's correct.

18 Q. What is the function of the 2 to 4-bit
19 memory address decoder that's labeled 112?

20 A. The 2 to 4 decoder is part of the
21 conditional clock generator that's used to select
22 one of the clocks to apply to the wordline circuit.

23 Q. In Figure 1, the first portion of the
24 memory address includes bits 0 and 1; is that
25 correct?

1 HORST

2 A. By first logic, are you referring to the
3 claims, the way it uses first logic?

4 Q. I don't think I said first logic.

5 I said in Figure 1, the first portion of
6 the memory address is bits 0 and 1; is that
7 correct?

8 A. Two bits of the address are bits 0 and 1;
9 whether you call that first or last depends on the
10 way the address is specified.

11 Q. And the 2 to 4-bit decoder that's labeled
12 112 decodes those two address bits and provides a
13 decoded portion to the conditional clock generator
14 that's labeled 110; is that correct?

15 A. The decoded outputs are used by the
16 conditional clock generator.

17 Q. What is the function of the conditional
18 clock generator that's labeled 110 in Figure 1?

19 A. The conditional clock generator is used to
20 select one wordline out of a group of wordlines,
21 and the group has been selected by the other bits
22 of the address through the 4 to 16 decoder.

23 Q. And how does it do that?

24 A. I don't understand the question.

25 Q. How does it function to do that?

1 HORST

2 A. I'm still not sure what you mean by "do
3 that."

4 Q. Well, what is the structure of the
5 conditional clock generator that enables it to
6 select a wordline?

7 A. Figure 3 shows more details about that
8 structure.

9 Q. What are the outputs of the conditional
10 clock generator that's labeled 110 in Figure 1?

11 A. Those outputs are labeled in Figure 3 as
12 clocks 0, 1, 2, and 3.

13 Q. Are those clock signals?

14 A. Yes. Those are clock signals, each for a
15 different bitline.

16 Q. And what is the relationship between the
17 clock signals that are output from the conditional
18 clock generator and the clock input labeled 118 in
19 Figure 1?

20 A. The clock input 118 is conditionally
21 passed to one of those clock outputs while the
22 other ones are held low.

23 Q. The circuit shown in Figure 1 includes
24 groups of wordline drivers that are labeled 104 and
25 106; is that correct?

1 HORST

2 A. That's correct. Not shown are the other
3 wordline drivers. It only shows the first and last
4 group of wordline drivers.

5 Q. And each of the clock outputs labeled 124,
6 126, 128, and 130 is coupled to each of the groups
7 of wordline drivers labeled 104 and 106; is that
8 correct?

9 A. Those clock lines at 124, 126, 128, and
10 130 are each coupled to all of the groups of
11 wordline drivers.

12 Q. And by "all of the wordline drivers,"
13 you're referring to the blocks labeled 104 and 106;
14 is that correct?

15 MS. REICHEL: Objection to form, misstates
16 his testimony.

17 A. I said "all of the groups." They're
18 coupled to all of the groups 104 through 106.

19 Q. What is the function of the 4 to 16
20 decoder labeled 108 in Figure 1?

21 A. The 4 to 16 decoder selects one of those
22 16 groups to be active.

23 Q. And in Figure 1, there are four address
24 bits labeled address 5:2 that are input to the 4 to
25 16 decoder; is that correct?

1 HORST

2 A. Yes. Address bits 5 through 2 go to that
3 4 to 16 decoder.

4 Q. So in Figure 1, there are two address bits
5 that are supplied to the 2 to 4 decoder labeled
6 112, and there are four address bits supplied to
7 the 4 to 16 decoder labeled 108; is that correct?

8 A. Yes. Those six address bits are shown at
9 the bottom of Figure 1.

10 Q. So in Figure 1, the address bits are
11 decoded separately by the decoder 112 and the
12 decoder 108, correct?

13 A. This shows separate decoders doing those
14 decoding functions.

15 Q. Can you turn to page 11 of the '002 patent
16 that's marked as page 11, column 9 and 10 of the
17 patent.

18 Do you see that, sir?

19 A. Yes. I'm there.

20 Q. Down in the bottom right-hand corner of
21 page 11 is the beginning of claim 1.

22 Do you see that?

23 A. Yes.

24 Q. And do you also see that claim 1 extends
25 onto page 12 in the upper left-hand portion.

1 HORST

2 Do you see that?

3 A. Yes.

4 Q. Claim 1 of the '002 patent recites first
5 logic and second logic, correct?

6 A. Correct.

7 Q. And according to claim 1, the first logic
8 receives a clock signal and a first portion of a
9 memory address of a memory array; is that correct?

10 A. That's part of what it says.

11 Q. What is the first logic as claimed in
12 claim 1 that's shown in Figure 1 of the '002
13 patent?

14 MS. REICHEL: Objection to form.

15 A. In Figure 1, the first logic includes the
16 2 to 4 decoder and the conditional clock generator.

17 Q. And if you look further in claim 1 at the
18 top left portion of page 12, claim 1 recites
19 "second logic to decode a second portion of the
20 memory address," correct?

21 A. That's part of what it says.

22 Q. And what is the second logic as claimed in
23 claim 1, shown in Figure 1 of the '002 patent?

24 MS. REICHEL: Objection to form.

25 A. The second logic includes that the 4 to 16

1 HORST

2 decoder, based on selecting from address bits 5
3 through 2.

4 Q. Anything else?

5 MS. REICHEL: Objection to form.

6 A. The output of decoder 4 -- the 4 to 16
7 decoder is shown further in Figure 3, and there's
8 an inverter 302 that's logically part of that
9 selection.

10 Q. The inverter 302 that's shown in Figure 3
11 is part of the second logic that's claimed in claim
12 1; is that correct?

13 MS. REICHEL: Objection to form.

14 A. The second logic acts to selectively
15 activate a particular wordline driver. So the path
16 from that second logic to the activation includes
17 that inverter. So I would include that inverter as
18 part of that second logic.

19 Q. Okay. Back to Figure 1 for a moment,
20 Dr. Horst.

21 The 4 to 16 decoder labeled 108 in
22 Figure 1 does not receive the clock signal 118,
23 correct?

24 MS. REICHEL: Objection to form.

25 A. This diagram does not show a clock signal

1 HORST

2 going to that decoder.

3 Q. Is there any part of the '002 patent that
4 would indicate that the clock signal 118 is
5 provided to the 4 to 16 decoder labeled 108 in
6 Figure 1?

7 A. No. In these figures, there's no clock
8 signal that's going to that decoder.

9 Q. Why is that?

10 MS. REICHEL: Objection to form,
11 foundation.

12 A. I don't -- there are many ways to
13 implement a decoder. Decoders can have clocks and
14 they can be designed without clocks. The designers
15 of the -- and inventors of the '002 evidently
16 decided to illustrate this with a non-clock
17 decoder.

18 Q. In decoding the address bits that are
19 labeled 5:2 in Figure 1, the 4 to 16-bit decoder
20 labeled 108 does not use the clock signal labeled
21 118, correct?

22 A. In the embodiment shown in Figure 1, they
23 do not show a clock decoder.

24 Q. The 4 to 16-bit decoder labeled 108 shown
25 in Figure 1 of the '002 patent operates

1 HORST

2 independently of the clock signal labeled 118,
3 correct?

4 A. The embodiment shown here does not use a
5 clock and is independent of the clock signal.

6 Q. I want to turn back to claim 1 for a
7 minute, which is pages 11 and 12.

8 In claim 1, the first logic receives a
9 clock signal, correct?

10 A. The first line of claim 1 says "the first
11 logic" -- "a first logic to receive a clock
12 signal."

13 Q. Claim 1 does not recite that the second
14 logic receives the clock signal, correct?

15 A. The portion of the claim talking about the
16 second logic is silent about whether the clock
17 signal goes to the second logic or not.

18 Q. So in claim 1, the second logic does not
19 receive the clock signal, correct?

20 MS. REICHEL: Objection to form,
21 mischaracterizes his testimony.

22 A. Claim 1 is not restricted to second logic
23 that uses the clock signal, but it could include
24 second logic that does include the clock signal.

25 Q. Does claim 1 recite that the second logic

1 HORST

2 receives the clock signal?

3 A. It does not say that it receives a clock
4 signal, but there's no prohibition of a clock
5 signal going there. So a system that has a clock
6 signal still would have all the elements of the
7 second logic of claim 1.

8 Q. I'm just asking whether the claim recites
9 the second logic receives the clock signal. Does
10 it or not?

11 MS. REICHEL: Objection to form.

12 A. The second logic does not require a clock
13 signal.

14 Q. Claim 1 also recites that the first logic
15 is to apply the clock signal to a selected clock
16 output, correct?

17 A. It actually states that "and to apply the
18 clock signal to a selected clock output of a
19 plurality of clock signals associated with a
20 selected group of a plurality of wordline drivers
21 that are associated with the memory array."

22 Q. Fair enough.

23 Claim 1 of the '002 patent also recites
24 that the second logic is to decode a second portion
25 of the memory address, correct?

1 HORST

2 A. That's part of what the claim says. It
3 says, "the second logic to decode a second portion
4 of the memory address, the second logic to
5 selectively activate a particular wordline driver
6 of the selected group of wordline drivers according
7 to the second portion of the memory address."

8 Q. And claim 1 does not recite that the
9 second logic uses the clock signal, correct?

10 MS. REICHEL: Objection to form.

11 A. As I previously answered, it -- the second
12 logic does not require a clock signal, but it
13 doesn't preclude a clock signal.

14 Q. Could you take a look at -- still in the
15 '002 patent, Dr. Horst, column 1, which is on
16 page 7, column 1, lines 64 to 66.

17 You there?

18 A. Yes, I'm there.

19 Q. Here at column 1, lines 64 to 66 of the
20 '002 patent, it states that "One particular
21 advantage of a particular illustrative embodiment
22 of the circuit is that a timing delay from a clock
23 to a particular wordline is reduced," correct?

24 A. That's what it says.

25 Q. Do you understand what that means?

1 HORST

2 A. It's talking about an advantage in
3 reducing the number of loads on a single clock
4 line.

5 Q. Why is that relevant?

6 A. The performance of a memory system
7 partially depends on how fast the wordline drivers
8 can be driven, and if there's excessive loading on
9 a clock, the rise time of the clock is slow and it
10 affects the performance.

11 Q. One of the stated advantages of the '002
12 patent is to reduce timing delay from a clock to a
13 particular wordline, correct?

14 MS. REICHEL: Objection to form,
15 mischaracterizes the document.

16 A. The statement we just read says, "One
17 particular advantage of a particular illustrative
18 embodiment of the circuit is that a timing delay
19 from a clock to a particular wordline is reduced."

20 So there is one embodiment, at least,
21 which has reduced clock loading.

22 Q. Would you agree that that's an advantage
23 of the invention described in the '002 patent,
24 Dr. Horst?

25 MS. REICHEL: Objection to form.

1 HORST

2 A. That is an advantage of any system that
3 reduces the number of clock loads, and including
4 the '002 patent and the prior art that I cited.

5 Q. Thank you, sir.

6 Can you move to column 1, starting line 66
7 and going over to column 2, line 2. And here the
8 '002 patent states that "Still another particular
9 advantage of a particular illustrative embodiment
10 of the circuit device is that the clock driver's
11 capacitance loading may also be reduced."

12 Do you see that?

13 A. Yes, I see that.

14 Q. Do you understand what that means?

15 A. Yes.

16 Q. Can you explain to me what that means?

17 A. The number of places a clock drives on a
18 chip increases the capacitance because the gate of
19 the MOSFETs all have high capacitance, and so the
20 more places it drives, the more capacitance there
21 is and the more loading is on that signal.

22 Q. Would you agree that that is an advantage
23 of the invention described in the '002 patent?

24 MS. REICHEL: Objection to form.

25 A. Again, that's an advantage in the '002

1 HORST

2 patent and the prior art that have fewer loads per
3 clock.

4 Q. Can you turn to column 2, lines 2 to 5 of
5 the '002 patent. And here the '002 patent states
6 that "Another particular advantage of a particular
7 illustrative embodiment is that use of multiple
8 conditional clocks to selectively apply a clock
9 signal reduces power consumption."

10 Do you see that, sir?

11 A. Yes.

12 Q. And do you understand what that means?

13 A. Yes.

14 When there are fewer loads on the clock
15 that's switching, power consumption is reduced
16 because the power consumption largely depends on
17 the frequency and the capacitance of the signals
18 that are changing.

19 Q. And finally, sir, can you turn to column
20 3, lines 13 -- which is on page 8 of the document,
21 lines 13 to 16.

22 And here the '002 patent states that
23 "Still another particular advantage of a particular
24 illustrative embodiment may be realized by sharing
25 a common address signal among multiple wordline

1 HORST

2 decoders, which reduces power consumption and
3 conserves layout area."

4 Do you see that, sir?

5 A. Yes.

6 Q. And do you understand what that means?

7 A. Can you read that section again that
8 you're referring to?

9 Q. Column 3, lines 13 to 16.

10 MS. REICHEL: I'm also having trouble
11 finding the text you just read at that citation.

12 MR. COCHRAN: Well, that's because I
13 pointed you to the wrong spot. I meant to say
14 column 2, lines 13 to 16. I apologize for that.

15 Q. Have you had a chance to read that,
16 Dr. Horst?

17 A. Yes.

18 Q. Can you explain to me what that means?

19 A. They are saying that there's an advantage
20 to having only a single common address signal,
21 which is the line that they use to select the
22 group. By having multiple bits per group, there's
23 fewer of those signal lines, and so if there's
24 fewer lines, that would reduce power consumption
25 and conserve layout area.

1 HORST

2 Q. The court reporter handed you a document
3 that is labeled Apple 1005.

4 Do you recognize this?

5 A. Yes. This is U.S. Patent 4,951,259, with
6 the first author's name Sato, and I generally refer
7 to this as the Sato patent.

8 Q. That's what I'll call it too.

9 How many times would you say you've read
10 the Sato reference, Dr. Horst?

11 A. I've read this many times, I couldn't
12 estimate how many.

13 Q. But you're very familiar with the subject
14 matter of the Sato patent, correct?

15 A. That's correct.

16 Q. Can you turn to Figure 3 of Sato, the Sato
17 patent. Figure 3 of the Sato patent depicts a
18 circuit diagram showing an X address decoder of a
19 static RAM, correct?

20 A. Figure 3 of Sato is showing a wordline
21 driver circuit. It's not necessarily restricted to
22 a static RAM.

23 Q. Can you turn to column 2, lines 57 to 59
24 of the Sato reference that's on page 6. And do you
25 see there, Dr. Horst, where the Sato patent says --

1 HORST

2 states, "Figure 3 a circuit diagram showing the X
3 address decoder of the static RAM in accordance
4 with the third embodiment of the present
5 invention," correct?

6 A. It states, "Figure 2 is a circuit diagram
7 showing the X address decoder of the static RAM in
8 accordance with the second embodiment of the
9 present invention."

10 Q. And I'm sorry, I was talking about lines
11 57 to 59 state, "Figure 3, a circuit diagram
12 showing the X address decoder of the static RAM in
13 accordance with the third embodiment of the present
14 invention," correct?

15 A. That's correct, that's what it states.

16 Q. Now, can you turn to -- I'm going to have
17 you look at a couple of things simultaneously,
18 Dr. Horst. Just two for now, so hopefully it will
19 work out.

20 Can you turn to paragraph 59 of your
21 declaration, which was marked Apple 1003.

22 A. Yes, I'm there.

23 Q. In paragraph 59 of your declaration, you
24 state, "Annotated Figure 3 (below) of Sato shows
25 Sato's X address decoder including structures

1 HORST

2 meeting the limitations of the first and second
3 logic of the '002 patent," correct?

4 A. That's correct, that's what it states.

5 Q. What portion of Figure 3 of Sato do you
6 contend meets the first logic limitation of the
7 '002 patent?

8 A. In my report, I have highlighted that in
9 the annotated figure of Figure 3 on page 25, which
10 shows that the first logic is the pre-decoder that
11 receives the clock signal and generates the
12 conditional clock outputs.

13 Q. Can you turn to paragraph 60 of your
14 declaration.

15 In paragraph 60, you state, "The
16 pre-decoder PDCR meets the limitation for the first
17 logic because it receives both a timing (clock)
18 signal and a portion of the memory address,"
19 correct?

20 A. Yes, that's what it states.

21 Q. What is the timing signal that is received
22 by the pre-decoder PDCR in Figure 3 of Sato?

23 A. That's the symbol labeled Phi subscript
24 ce. It's the Greek symbol Phi.

25 Q. And what is the portion of the memory

1 HORST

2 address received by the pre-decoder PDCR in
3 Figure 3 of Sato?

4 A. The address received is the true and
5 complemented bits of two bits of the address
6 labeled ax0 and ax1.

7 Q. The Sato patent does not provide a figure
8 showing the circuitry of the PDCR block shown in
9 Figure 3, correct?

10 A. Sato does not show a figure for that, but
11 it describes in words in sufficient detail that I
12 was able to draw a diagram of what is in that
13 block.

14 Q. The Sato patent does not include a figure
15 showing the circuitry in the PDCR block, correct?

16 A. It describes it in words instead of in a
17 picture.

18 Q. Sato refers to the four outputs Phi x0
19 through Phi x3 as "selection signals," correct?

20 A. I'd have to read through all of Sato to
21 know the different ways it might refer to those
22 signals.

23 Q. Why don't you turn to column 1, line 51 of
24 Sato.

25 At column 1, line 51, what does Sato refer

1 HORST

2 to with respect to the signals Phi x0 through Phi
3 x3, Dr. Horst?

4 A. In this instance, it says the
5 corresponding selection signals Phi x0 through x3
6 is supplied from the pre-decoder PCDR described
7 above to the source of the P-channel MOSFET.

8 Q. So column 1, line 51, the Sato patent
9 refers to the signals Phi x0 through Phi x3 as
10 "selection signal," correct?

11 A. In this instance, it calls these signals
12 selection signals, although this is still in the
13 Background of the Invention section of the patent,
14 so --

15 Q. Why don't you turn to column 5, line 28
16 and 29 of the Sato patent; and while you're at it,
17 you can look at line 34 as well.

18 A. Yes. It calls them selection signals
19 here.

20 Q. Take a look at column 7, line 42.

21 What does the Sato patent refer to Phi x0
22 through Phi x3 at column 7, line 42, Dr. Horst?

23 A. It, again, calls them selection signals
24 here.

25 Q. Can you turn to column 9, and I'll have

1 HORST

2 you look at lines 9, 19, 59, and 61.

3 A. Yes. It also calls them selection signals
4 here. Of course, this is actually a translation of
5 a Japanese patent, and so that's the term the
6 translator used.

7 Q. Can you also look at column 10 of the Sato
8 patent, lines 3, 6, 11, 27, and 38 and tell me what
9 the Sato patent refers to the signals Phi x0
10 through Phi x3 as?

11 A. It refers to them as selection signals
12 there also.

13 Q. Are you aware of any portion of the Sato
14 reference that refers to the signals Phi x3 through
15 Phi x --

16 MR. COCHRAN: Excuse me.

17 Q. Are you aware of any portion of the Sato
18 reference that refers to the signals Phi x0 through
19 Phi x3 as anything other than a selection signal?

20 A. I have not reviewed the patent to know if
21 there's other ways it refers to them.

22 Q. The Sato reference never refers to the
23 signals Phi x0 through Phi x3 as timing signals,
24 correct?

25 MS. REICHEL: Objection to form,

1 HORST

2 foundation.

3 A. The Sato patent may not call them timing
4 signals, but it does call the signal Phi sub ce a
5 timing signal. And based on the discussion of how
6 those other signals are generated, a person of
7 ordinary skill in the art would also understand
8 those signals to be timing signals.

9 Q. But the reference doesn't call them timing
10 signals, correct?

11 MS. REICHEL: Objection to form.

12 A. I would have to search the entire document
13 to know if they're ever referred to that way. I
14 can't say that for sure.

15 Q. Why would the Sato reference use the
16 phrase "selection signals" for the outputs of the
17 pre-decoder and the phrase "timing signal" for the
18 Phi ce signal that's input to the pre-decoder?

19 MS. REICHEL: Objection to form,
20 foundation.

21 A. These signals are timing signals that
22 include a selection because they're also based on
23 the decoded address bits. So they chose to label
24 them based on its selection function instead of
25 based on its timing function.

1 HORST

2 Q. What are the signals selecting?

3 A. The signals are supplying both timing and
4 selection information for one of the word drivers
5 in the selected group of word drivers.

6 Q. Back to Figure 3, Dr. Horst, of Sato.
7 What portion of Figure 3 of Sato do you contend
8 meets the second logic limitation of claim 1 of the
9 '002 patent?

10 A. As I show in the annotated figure on
11 page 25, the second logic is the NAND decoder
12 labeled NAG0 here. This is only showing one of the
13 decoders, but each group of decoders would have one
14 of these decoders.

15 Q. In Figure 3, the gates of MOSFETs Qg1 and
16 Qg4 are connected in common, and the signal Phi ce
17 is supplied to the gates of these two transistors,
18 correct?

19 A. That's correct.

20 Q. And the signal Phi ce is similarly
21 supplied to the gates of the MOSFETs that are in
22 the other NAND circuits labeled NAG0 through NAGk,
23 correct?

24 A. Can you repeat that? I don't --

25 Q. Why don't you turn to Figure 1 of the Sato

1 HORST

2 reference, this question will be easier to
3 decipher.

4 A. Can you repeat the question?

5 MR. COCHRAN: Can you read it back,
6 please?

7 (Whereupon, the record was read as
8 follows: Question: "And the signal Phi ce is
9 similarly supplied to the gates of the MOSFETs that
10 are in the other NAND circuits labeled NAG0 through
11 NAGk, correct?")

12 MS. REICHEL: Objection to form.

13 A. Okay. Now I understand.

14 MS. REICHEL: I'm sorry. Can you just
15 confirm for the record what the question was that
16 you read back because he asked two questions and it
17 started with a question directed to Figure 3, and
18 now he's asking about Figure 1, so I just want the
19 record to be clear about which figure the basis of
20 the question is.

21 So please either read both questions
22 together or if you want to ask the question a
23 different way, obviously free to do that.

24 MR. COCHRAN: The previous question
25 relates to Figures 1 and 3, but if you could read

1 HORST

2 it back again.

3 COURT REPORTER: You want me to read the
4 last two questions, then?

5 MR. COCHRAN: Please.

6 (Whereupon, the record was read as
7 follows: QUESTION: "In Figure 3, the gates of
8 MOSFETs Qg1 and Qg4 are connected in common, and
9 the signal Phi ce is supplied to the gates of these
10 two transistors, correct?"

11 ANSWER: "That's correct."

12 QUESTION: "And the signal Phi ce is
13 similarly supplied to the gates of the MOSFETs that
14 are in the other NAND circuits labeled NAG0 through
15 NAGk, correct?")

16 MS. REICHEL: And you want him to answer
17 that question looking at Figure 1 or --

18 MR. COCHRAN: Both Figures 1 and 3.

19 A. Okay. The confusion was that I understood
20 you to say NE, as in echo, G, instead of NAG, which
21 is the way the figure is labeled. Assuming you're
22 talking about NAG?

23 Q. I am, yes, sir.

24 A. Then yes, figure Phi ce goes to the other
25 copies of this decoder circuit, and NAG, the rest

1 HORST

2 of these NAND decoders.

3 Q. Sticking with Figure 1, the output of the
4 NAND gate circuits labeled NAG0 through NAGk varies
5 based on the signal Phi ce, correct?

6 A. I didn't understand what you said.
7 Varies?

8 Can you repeat the beginning of that.

9 MR. COCHRAN: Can you repeat that?

10 (Whereupon, the record was read as
11 follows: Question: "Sticking with Figure 1, the
12 output of the NAND gate circuits labeled NAG0
13 through NAGk varies based on the signal Phi ce,
14 correct?")

15 A. The Phi ce signal is used in those decoder
16 circuits, but the decoders' outputs in terms of the
17 bits selected does not depend on the Phi ce signal.

18 Q. Does the output of the NAND gate circuit
19 NAG0 through NAGk depend on the value of the signal
20 Phi ce?

21 MS. REICHEL: Objection to form.

22 A. The value of the output is affected by the
23 Phi ce signal, but, again, the selected bit depends
24 on the address lines.

25 Q. Can you turn to column 3, lines 59 to 61

1 HORST

2 of the Sato patent.

3 Column 3 lines 59 to 61 of Sato states, "A
4 timing signal Phi ce (a selection control signal)
5 is supplied, too, from a later-discussed timing
6 control circuit TC to the X address decoder XDCE,"
7 correct?

8 A. That's what it states, yes.

9 Q. The Sato patent refers to the signal Phi
10 ce as a timing signal, correct?

11 A. Here it refers to it as a timing signal,
12 and parenthetically, as also a selection control
13 signal.

14 MR. COCHRAN: Would you like to take a
15 break, Dr. Horst? It's been about an hour and ten
16 minutes. I recommend a break for us, if that's
17 okay with you.

18 THE WITNESS: Yes.

19 (Proceedings interrupted at 11:09 a.m. and
20 reconvened at 11:16 a.m.)

21 BY MR. COCHRAN:

22 Q. Can you turn to Figure 4 of the Sato
23 patent, Dr. Horst. Figure 4 depicts a block
24 labeled TC, correct?

25 A. Yes.

1 HORST

2 Q. The block labeled TC represents a timing
3 control circuit; is that right?

4 A. Can you point me to where it describes
5 that in the text?

6 Q. If you look at column 5, lines 7 to 12, it
7 should help.

8 A. Yes. In line 7 it says, "The timing
9 control circuit TC generates various timing signals
10 described above on the basis of a chip enable
11 signal CE, a write enable signal WE and an output
12 enable signal OE supplied as control signals from
13 outside, and supplies each timing signal to each
14 circuit in the manner described above."

15 Q. Thank you.

16 What does it mean in column 5, line 7 to
17 12 when it says that the chip enable, the write
18 enable, and the output enable signals are provided
19 as control signals from outside?

20 A. It's describing an integrated circuit
21 where the signals driven to the circuit come into
22 those terminals while other signals shown in the
23 patent are the internal signals inside the
24 integrated circuit.

25 Q. In Figure 4 of Sato, the signals CE for

1 HORST

2 chip enable, WE for write enable, and OE for output
3 enable are coming from outside of the static RAM
4 integrated circuit, correct?

5 A. That's right.

6 Q. At column 5, lines 7 to 12 of Sato, which
7 you just read from, Sato does not refer to the
8 write enable signal as being periodic, correct?

9 A. In the section I just read, it doesn't
10 talk about how any of these signals are driven and
11 whether they're periodic or not.

12 Q. By "any of these signals," are you
13 referring to the write enable, output enable, and
14 chip enable signals to the timing control block
15 shown in Figure 4?

16 A. That's correct; those are the signals I
17 was talking about.

18 Q. Could you turn to column 3, lines 59
19 through 65 of Sato.

20 Do you see that, Dr. Horst?

21 A. Yes.

22 Q. In column 3, lines 59 through 65, Sato
23 does not refer to the chip enable signal as being
24 periodic, correct?

25 A. It says that the timing signal is

1 HORST

2 generated in accordance with the chip enable signal
3 CE. It does not specifically say anything about
4 the waveform on the CE line.

5 Q. And column 3, lines 59 through 65 of Sato
6 does not refer to the signal Phi ce as being
7 periodic either, correct?

8 A. It doesn't say whether it is or is not
9 periodic. That would depend on the design of the
10 system that this chip is used in and whether it
11 drives that signal periodically or not.

12 Q. At column 3 lines 59 through 65 of Sato,
13 Sato states that when the chip enable signal is
14 low, the Phi ce signal is kept high, correct?

15 MS. REICHEL: Objection to form.

16 A. The wording of this is not -- does not
17 clearly show what it means to be in accordance with
18 a chip enable signal, so it does not directly say
19 what you just stated.

20 Q. When the chip enable signal is low in
21 Sato, the Phi ce signal is high, correct?

22 MS. REICHEL: Objection to form.

23 A. In Sato, there's no circuit diagram for
24 that timing control block shown in Figure 4, so it
25 doesn't say specifically exactly how those timing

1 HORST

2 signals are generated based on the chip inputs.

3 Q. If Sato doesn't provide a circuit
4 schematic for the block labeled TC in Figure 4, how
5 are we to determine how that works to generate the
6 timing control signal Phi ce?

7 A. Sato is primarily concerned with the X
8 decoder circuit, and the different ways that those
9 timing signals can be derived are not critical to
10 understanding how the X decoder works.

11 Q. The Sato patent doesn't tell you how the
12 Phi ce signal is generated by the timing control
13 block, correct?

14 MS. REICHEL: Objection to form.

15 A. The sentence we just read is the
16 description that it uses, which says that the
17 timing signal is generated in accordance with the
18 chip enable signals CE.

19 Q. Other than that portion that we read,
20 there's no other teaching in Sato that would
21 instruct how the Phi ce signal is generated by the
22 timing control block shown in Figure 4, correct?

23 A. I would have to read through the whole
24 patent to know if there's any other mentions of
25 that block of logic.

1 HORST

2 Q. Are you aware of any other off the top of
3 your head?

4 A. No. I'm not aware of other areas that
5 describe that in more detail.

6 Q. Can you turn to the front page of Sato,
7 the paragraph that's labeled Abstract.

8 Do you see that in the abstract of Sato,
9 it says, "In large memory arrays, the wordline
10 driver circuits can place large capacitive loads on
11 the output of the logic decoding circuit because
12 the wordline driver transistors must be relatively
13 large. This large load on the logic decoding
14 circuitry adversely affects the operating speed of
15 the memory."

16 Do you see that?

17 A. Yes.

18 Q. In the Sato patent, the problem identified
19 is that of large capacitive loads on the output of
20 a logic decoding circuit; is that right?

21 A. That's one of the things it addresses,
22 yes.

23 Q. Are there any other problems that are
24 addressed by Sato, other than that one?

25 A. The Sato circuit can be used in many

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2 different ways, so it doesn't attempt to describe
3 all the different benefits.

4 Q. The Abstract paragraph of Sato goes on to
5 say, "Accordingly, to reduce this load, a switching
6 arrangement is provided between the output of the
7 logic decoding circuitry and the wordline drivers."

8 Do you see that?

9 A. Yes.

10 Q. In Figure 3 of Sato, what is the wordline
11 driver circuit?

12 A. The wordline driver circuit in Figure 3 is
13 illustrated, again, on page 25 of my report, and it
14 includes the final drivers to the wordlines, as
15 well as Q19, Q29, Q20, Q30 and so on, the
16 transistors that connect to those final drivers.

17 Q. In Sato Figure 3, what is the switching
18 arrangement?

19 A. I don't understand the question.

20 Q. In Figure 3 of Sato, what is the switching
21 arrangement that was referred to in the abstract of
22 the patent?

23 A. I read the switching arrangement to just
24 mean the general -- a broad description of this
25 whole logic diagram shown in Figure 3.

1 HORST

2 Q. Can you turn back to your declaration,
3 Dr. Horst, paragraph 153.

4 A. Yes. Paragraph 153.

5 Q. Paragraph 153 of your declaration includes
6 a statement of the law of anticipation, as you've
7 been instructed in preparing your declaration,
8 correct?

9 A. Correct.

10 Q. And in paragraph 153, you state that
11 you've "been informed that a patent claim is
12 invalid as anticipated... if each and every element
13 of a claim, as properly construed, is found either
14 explicitly or inherently in a single prior art
15 reference," correct?

16 A. Yes. That's what it says.

17 Q. That's your understanding of the law of
18 anticipation, correct?

19 A. Yes. Anticipation requires all the
20 elements to be included in the reference.

21 Q. Can you now turn to paragraph 8 of your
22 declaration, please.

23 A. Yes.

24 Q. Paragraph 8 of your declaration explains
25 the conclusions that you have formed, and there are

1 HORST

2 two conclusions: The first conclusion is that you
3 believe the claims 1 through 28 and 31 through 37
4 of the '002 patent are rendered obvious by the Sato
5 patent, correct?

6 A. Correct.

7 Q. And in your declaration, you did not
8 provide an opinion that any of the claims of the
9 '002 patent are anticipated by the Sato reference,
10 correct?

11 A. I did not in my report say that they are
12 anticipated, although I believe that they are both
13 anticipated and obvious based on Sato.

14 Q. So why didn't you provide an opinion that
15 the claims are anticipated by Sato if you believe
16 that's the case?

17 MS. REICHEL: I'm going to instruct you to
18 the extent that that decision was done in
19 conjunction with the attorneys, you should not
20 provide any testimony about that decision-making
21 process.

22 To the extent you made an independent
23 decision outside of communications with counsel as
24 to which opinions you were going to disclose in the
25 report, you can testify as to that. I'm not aware

1 HORST

2 of an independent decision. But I do instruct you
3 not to answer that question in a way that reveals
4 any communications you had with counsel or any work
5 product arising from communications with counsel.

6 A. I can't answer this question based on work
7 product with counsel.

8 Q. But you believe that the claims of the
9 '002 patent are anticipated by the Sato reference?

10 A. I believe they are anticipated, yes.

11 Q. But you don't have an opinion in your
12 declaration to that effect, correct?

13 A. That's correct.

14 Q. Okay. The court reporter has handed you,
15 Dr. Horst, a document that was previously marked as
16 Apple 1006.

17 Do you recognize this?

18 A. Yes. This is a published patent by Asano,
19 which is one of the primary references I used in my
20 report.

21 Q. How many times have you read the Asano
22 patent -- sorry -- publication?

23 A. I've read it several times.

24 Q. So you're very familiar with the subject
25 matter of the Asano publication, correct?

1 HORST

2 A. That's correct.

3 Q. If you look at the abstract paragraph on
4 the cover page of the Asano reference, it says, in
5 part, that Asano discloses an apparatus and method
6 "to reduce the number of required latches in a deep
7 pipeline wordline (WL) decoder."

8 Do you see that?

9 A. Yes.

10 Q. What is a deep pipeline wordline decoder,
11 Dr. Horst?

12 A. A pipeline decoder is one in which stages
13 of the decoding are held in pipeline registers and
14 are to increase the throughput of the decoding
15 process.

16 Q. Is that what's shown in the Sato patent as
17 well?

18 A. The Sato patent shows one latch in the
19 decoding process. Depending on the level of
20 pipelining, there could be more or fewer latches.

21 Q. If you could turn to Figure 2 of Asano.

22 Figure 2 of Asano depicts a memory labeled
23 200 that includes 32 wordline drivers labeled 206,
24 correct?

25 A. Yes, that's what Figure 2 shows.

1 HORST

2 Q. And still referring to Figure 2, each of
3 the 32 wordline drivers includes a latch and two
4 AND gates, correct?

5 A. Figure 2 shows the latch and two AND gates
6 in box 206.

7 Q. And still referring to Figure 2, the
8 memory labeled 200 in Asano includes a 64 wordline
9 array that's labeled 214, correct?

10 A. Yes, that's correct.

11 Q. And the memory labeled 200 includes a
12 final decoder labeled 204, correct?

13 A. Yes. The final decoder is 204.

14 Q. And the memory labeled 200 in Asano's
15 Figure 2 includes a first LCB circuit labeled 208
16 and a second LCB circuit labeled 234, correct?

17 A. That's correct.

18 Q. And the memory labeled 200 in Asano
19 includes a single pre-decoder block labeled 202,
20 correct?

21 A. Yes, that's correct.

22 Q. In Figure 2 of Asano, the address labeled
23 216 is received by the single pre-decoder block
24 labeled 202, correct?

25 MS. REICHEL: Objection to form.

1 HORST

2 A. The diagram shows all the decoding
3 happening in that decoder block, that's correct;
4 although the actual implementation would have
5 separate gates that are driving those different
6 outputs.

7 Q. Does the Asano publication include a
8 schematic of the pre-decoder 202, Dr. Horst?

9 A. Asano does not show a diagram of that, but
10 it describes it in words in sufficient detail that
11 I was able to draw the diagram myself of what's in
12 those -- in that decoder block.

13 Q. Let's look at that. Page 51 of your
14 declaration, if you could turn to that page,
15 Dr. Horst.

16 Are you there?

17 A. Yes.

18 Q. Page 51 of your declaration includes a
19 figure labeled "Asano Figure 2 redrawn showing
20 structure as described in specification"; is that
21 correct?

22 A. That's correct.

23 Q. And in this figure which you drew, you
24 have shown a 1 to 2 decoder, a 2 to 4 decoder, and
25 a 3 to 8 decoder; is that right?

1 HORST

2 A. That's right.

3 Q. Can you now turn to page 55 of your
4 declaration.

5 And page 55 of your declaration includes
6 another drawing figure which you drew, correct?

7 A. That's correct.

8 Q. And on page 55, you have labeled that
9 "Asano Figure 2 redrawn with 4 LCBs per group,"
10 correct?

11 A. That's correct.

12 Q. And in this figure, you show a 2 to 4
13 decoder, a 1 to 2 decoder and a 3 to 8 decoder,
14 correct?

15 A. That's correct.

16 Q. The pre-decoder block labeled 202 in
17 Figure 2 of Asano could be implemented many
18 different ways, correct?

19 MS. REICHEL: Objection to form.

20 A. The specification says how that decoder is
21 implemented in the case where there's two LCBs and
22 I drew that in the figure on page 51.

23 Q. Well, are there other ways you could
24 implement the pre-decoder 202 shown in Figure 2 of
25 Asano, other than the figures you drew on pages 51

1 HORST

2 and 55 of your declaration?

3 A. This is the figure that one of ordinary
4 skill in the art would have drawn based on the
5 description of Asano.

6 Q. Are there other ways you could implement
7 it?

8 A. Decoders can be implemented in a single
9 stage or in multiple stages. As I pointed out in
10 the Itoh reference, the most natural way to design
11 it is as it's described in the specification, which
12 would have been this 3 to 8 decoder and the 2 to 4
13 decoder.

14 Q. So there are other ways that it could be
15 implemented, correct?

16 MS. REICHEL: Objection to form.

17 A. There are other ways, but those ways are
18 equivalent and obvious.

19 Q. The court reporter has handed you a
20 document previously marked Apple 1007, Dr. Horst.

21 Do you recognize this document?

22 A. Yes. This is what I've called the Itoh
23 reference. This is some selected pages from a
24 textbook titled "VLSI Memory Chip Design."

25 Q. And how many times would you say you've

1 HORST

2 read the Itoh reference, Dr. Horst?

3 A. I've read this several times, these pages
4 I've read. I've not read the entire Itoh
5 reference.

6 Q. Can you turn to paragraph 124 of your
7 declaration, please.

8 In paragraph 124 of your declaration, you
9 refer to an annotated figure showing Asano's
10 pre-decoder 202 implemented using Itoh's
11 pre-decoder circuitry.

12 Do you see that?

13 A. Yes.

14 Q. And is that annotated figure shown on
15 page 61 of your declaration?

16 A. Yes, it is.

17 Q. Does the figure shown on page 61 of your
18 declaration show one possible way of implementing
19 Asano's pre-decoder?

20 MS. REICHEL: Objection to form.

21 A. This shows a way of implementing Asano's
22 pre-decoder based on Itoh.

23 Q. But a person of ordinary skill in the art
24 would understand how to implement the pre-decoder
25 in many different ways; isn't that correct?

1 HORST

2 MS. REICHEL: Objection to form.

3 A. The function of a decoder is the same,
4 depending on the implementation. So there could be
5 different numbers of gate levels, for instance, but
6 they would all be equivalent.

7 Q. Putting functionality aside for a minute
8 and just focusing on the implementation of the
9 pre-decoder, you'd agree that a person of skill in
10 the art would understand how to implement the
11 pre-decoder circuit like you show on page 61 of
12 your declaration in many different ways, correct?

13 MS. REICHEL: Objection to form.

14 A. A person of ordinary skill would know how
15 to implement it in different ways. The ways that
16 I've shown in my document are the most natural ways
17 that a person of ordinary skill would have decided
18 to use.

19 Q. Could you turn to page 22 of your
20 declaration.

21 A. Yes, I'm there.

22 Q. Page 22 of your declaration is the
23 beginning of your analysis of the Sato reference,
24 correct?

25 A. That's correct.

1 HORST

2 Q. And your analysis of the Sato reference
3 begins on page 22 and proceeds on to page 49, I
4 believe, of your declaration; is that correct?

5 A. Yes, that's the section devoted to the
6 Sato reference.

7 Q. So it's about 27 pages, correct?

8 A. I haven't done the math, but that sounds
9 about right.

10 Q. In those 27 pages of analysis in your
11 declaration, Dr. Horst, you don't actually set
12 forth any of the claims of the '002 patent; isn't
13 that correct?

14 MS. REICHEL: Objection to form.

15 A. I do not show the claims themselves, but I
16 describe the claim elements that are in the claims
17 of the '002 patent.

18 Q. All of them?

19 A. I've included certain claim terms. I
20 haven't included all of them.

21 Q. Can you turn to page 64 of your
22 declaration.

23 Page 64 of your declaration is the
24 beginning of the detailed analysis of the Asano and
25 Itoh references; is that correct?

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A. I'm sorry. Where are you at?

Q. Page 64 of your declaration.

MS. REICHEL: Are you referring specifically to the combination as opposed to the individual references?

Q. I'm referring to the title of the section called "Detailed Analysis of Asano and Itoh."

A. Yes, that's the title just before paragraph 131 on page 64.

Q. So this is the beginning of your analysis of the Asano and Itoh references, correct?

MS. REICHEL: Objection to form, mischaracterizes the document.

A. That's the section that talks about the combination of the two. Earlier, I'm talking only about the -- well, primarily about the Asano, but I do mention Itoh even in the Asano section.

Q. And this section proceeds on to page 72 of your declaration, correct?

A. Yes. The end of the section is on 72.

Q. So that's about eight pages of analysis, correct?

MS. REICHEL: Objection to form.

A. Yes.

1 HORST

2 Q. And in eight pages of analysis where you
3 discuss the Asano and Itoh references, you don't
4 show any of the claims of the '002 patent; isn't
5 that correct?

6 MS. REICHEL: Objection to form,
7 mischaracterizes the document.

8 A. Instead of showing the claims in this
9 section, I described the claim elements and show
10 how the combination describes and meets those claim
11 elements.

12 Q. Do you know how many claims there are in
13 the '002 patent, Dr. Horst?

14 A. The last claim of the '002 is claim 38.

15 Q. So how many claims are there in the '002
16 patent, Dr. Horst?

17 A. There's 38 claims.

18 Q. Do you know the difference between an
19 independent claim and a dependent claim?

20 A. Yes.

21 Q. What's the difference?

22 A. A dependent claim is based on one of the
23 independent claims and adds other elements to that
24 claim.

25 Q. How many independent claims are there in

HORST

the '002 patent, Dr. Horst?

A. I believe there's about seven. I'd have to count them up.

There's more than seven. I'd have to count them again. I count ten independent claims.

Q. Ten?

MR. COCHRAN: Okay. No further questions from me.

MS. REICHEL: Why don't we take a quick break and come back to confirm.

(Proceedings interrupted at 11:56 a.m. and reconvened at 12:00 p.m.)

MS. REICHEL: We have no questions for the witness at this time.

(Whereupon, this deposition was concluded at 12:00 p.m.)

ROBERT W. HORST, Ph.D.

Subscribed and sworn to before me

this ____ day of _____, 2019.

1 CERTIFICATE

2 Commonwealth of Massachusetts
3 Suffolk, ss.
4

5 I, Dana Welch, Registered Professional
6 Reporter, Certified Realtime Reporter and Notary
7 Public in and for the Commonwealth of
8 Massachusetts, do hereby certify that ROBERT W.
9 HORST, Ph.D., the witness whose deposition is
10 hereinbefore set forth, was duly sworn by me and
11 that such deposition is a true record of the
12 testimony given by the witness.

13 I further certify that I am neither related
14 to nor employed by any of the parties in or counsel
15 to this action, nor am I financially interested in
16 the outcome of this action.

17 In witness whereof, I have hereunto set my
18 hand and seal this 1st day of April, 2019.

19 
20

21 Dana Welch

22 Notary Public

23 My Commission Expires:

24 September 13, 2024
25

I N D E X

WITNESS: ROBERT W. HORST, Ph.D.

EXAMINATION: PAGE:

BY MR. COCHRAN 4

EXHIBITS MARKED:

NO. DESCRIPTION PAGE:

None marked

EXHIBITS PREVIOUSLY MARKED:

Apple 1001, U.S. Patent 7,693,002 11

Apple 1003, Declaration of Robert W. 6

Horst, Ph.D.

Apple 1004, Curriculum Vitae Robert W. 9

Horst, Ph.D.

Apple 1005, U.S. Patent 4,951,259 27

Exhibit Apple 1006, U.S. Patent 47

Application 2006/0098520 (Asano patent)

Apple 1007, VLSI Memory Chip Design by 52

Kiyoo Itoh

NOTATIONS:

Instruction of counsel 7

Instruction of counsel 46

Exhibits retained by reporter.

ERRATA SHEET

Case Name:

Deposition Date:

Deponent:

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Signature of Deponent

SUBSCRIBED AND SWORN BEFORE ME

THIS ____ DAY OF _____, 2019.

(Notary Public) MY COMMISSION EXPIRES: _____