Apple Inc.
v.
Qualcomm Incorporated

IPR2018-01249

U.S. Patent No. 7,693,002

Patent Owner's Demonstrative Exhibits

U.S. Patent No. 7,693,002

(12) **United States Patent**
Lin

(10) **Patent No.: US 7,693,002 B2**
(45) **Date of Patent: Apr. 6, 2010**

(54) **DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS**

(75) Inventor: **Jentsung Lin**, Cardiff by the Sea, CA (US)

(73) Assignee: **QUALCOMM Incorporated**, San Diego, CA (US)

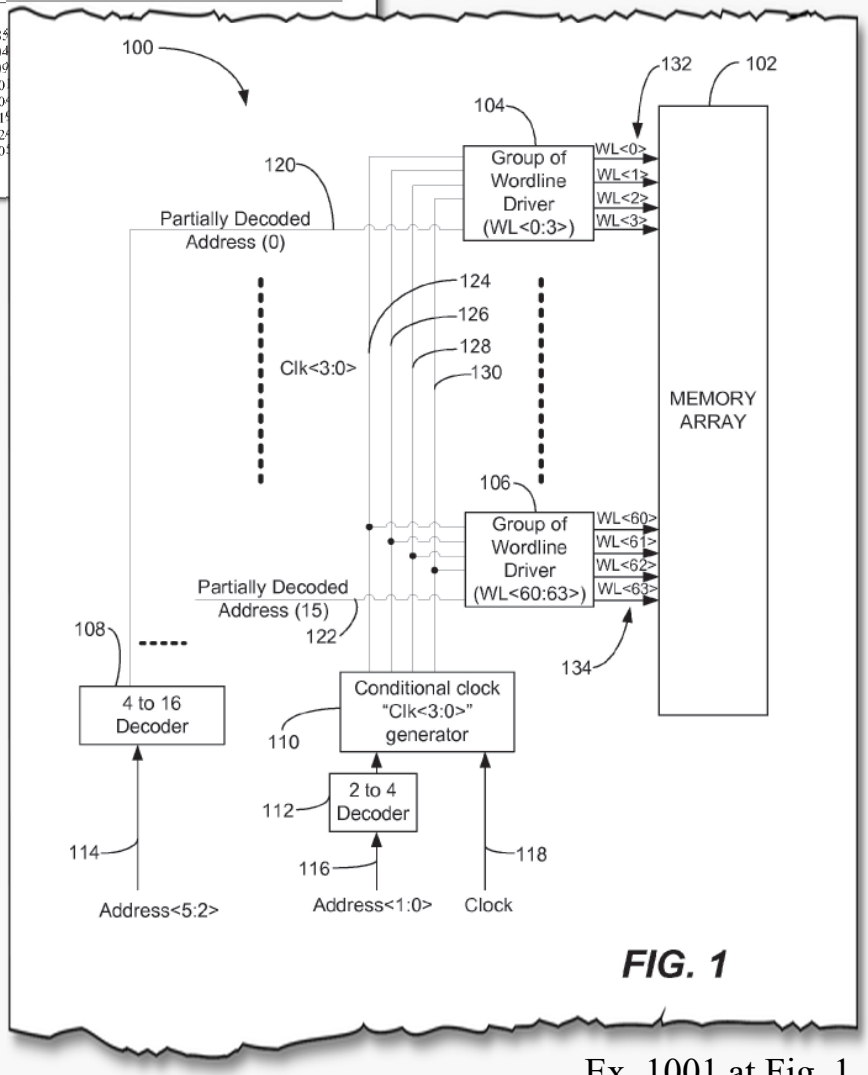

FIG. 1

Ex. 1001 at Fig. 1

U.S. Patent No. 7,693,002

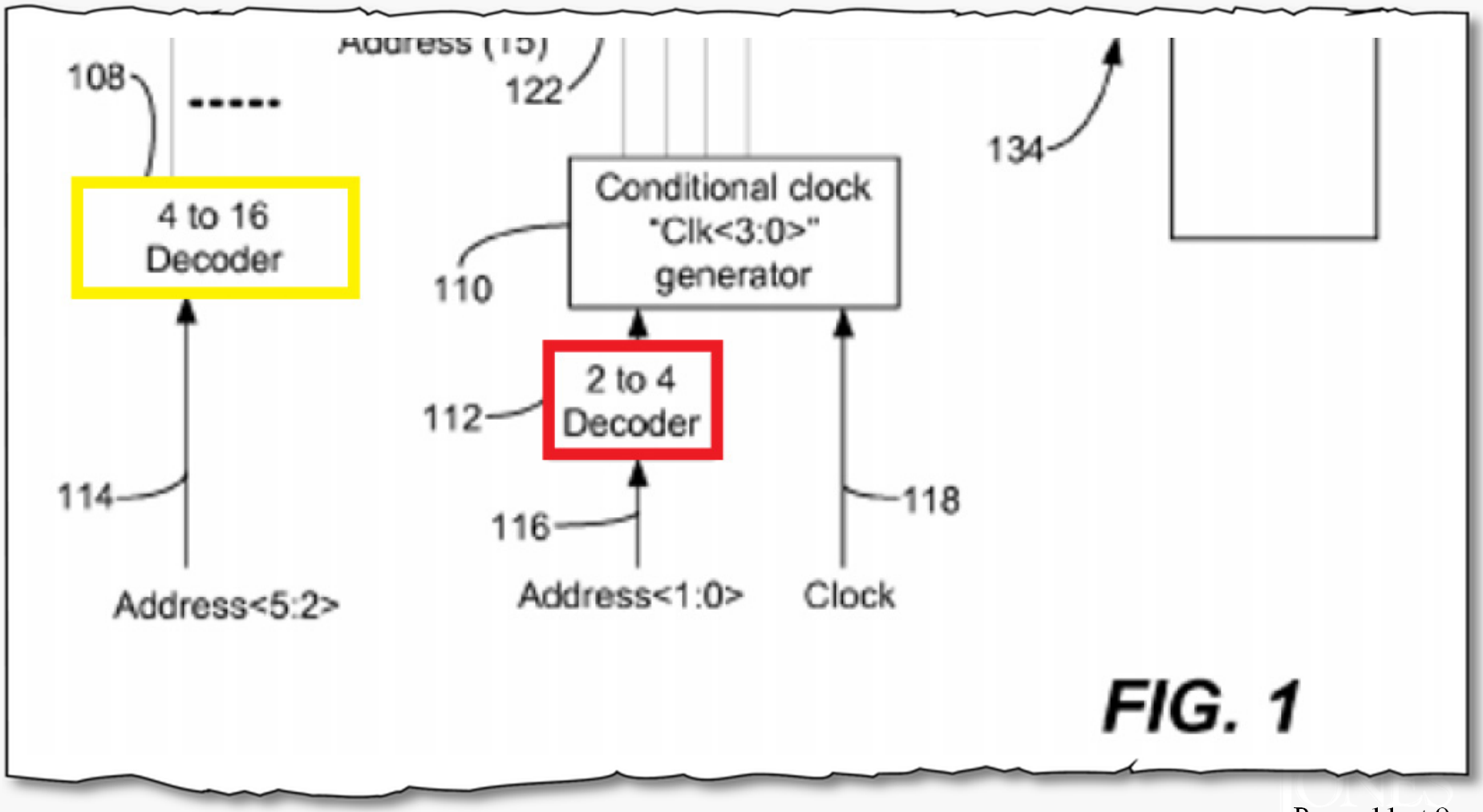

FIG. 1

Paper 11 at 9

'002 Patent – Claim 1

1. A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

Ex. 1001 at 10:65-11:10

Contested Grounds

Ground	Claims	Grounds for Review
1	1-28 and 31-37	Obvious over Sato
2	1-17, 20-28, 31-36	Obvious over Asano and Itoh

Paper 2 at 2

Patentability

I. SATO DOES NOT RENDER CLAIMS 1-28 AND 31-37 OBVIOUS

- The Petition Fails to Establish a *Prima Facie* Case of Obviousness
- Sato Does Not Teach or Suggest the Claimed "Clock Signal"
- Sato Does Not Teach or Suggest the Claimed "Clock Output"

II. ASANO AND ITOH DO NOT RENDER CLAIMS 1-17, 20-28, AND 31-36 OBVIOUS

- Petitioner's Combination is Based on Impermissible Hindsight
- The Petition's Motivation to Combine Argument is Flawed

Patentability

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Sato § 103: The Petition Fails to Establish a *Prima Facie* Case of Obviousness

A. Claim 1 is Obvious Over Sato [GROUND-1]

A claim may be rendered unpatentable by a single reference if a POSITA would have been motivated to modify that reference in an obvious way. *SIBIA Neurosciences, Inc. v. Cadus Pharm. Corp.*, 225 F.3d 1349, 1356 (Fed. Cir. 2000). Notably, motivations to modify may be found implicitly in the prior art based on what the teachings of the art, a POSITA's knowledge, and the nature of the problem to be solved would have suggested to a POSITA. *See In re Kahn*, 441 F.3d 977, 987-88 (Fed. Cir. 2006); *see also Cross Medical Prods., Inc. v. Medtronic Sofamor Danek, Inc.*, 424. F.3d 1293, 1322 (Fed. Cir. 2005) (motivation "equally can be found in the knowledge generally available to" a POSITA). The

Paper 2 at 9

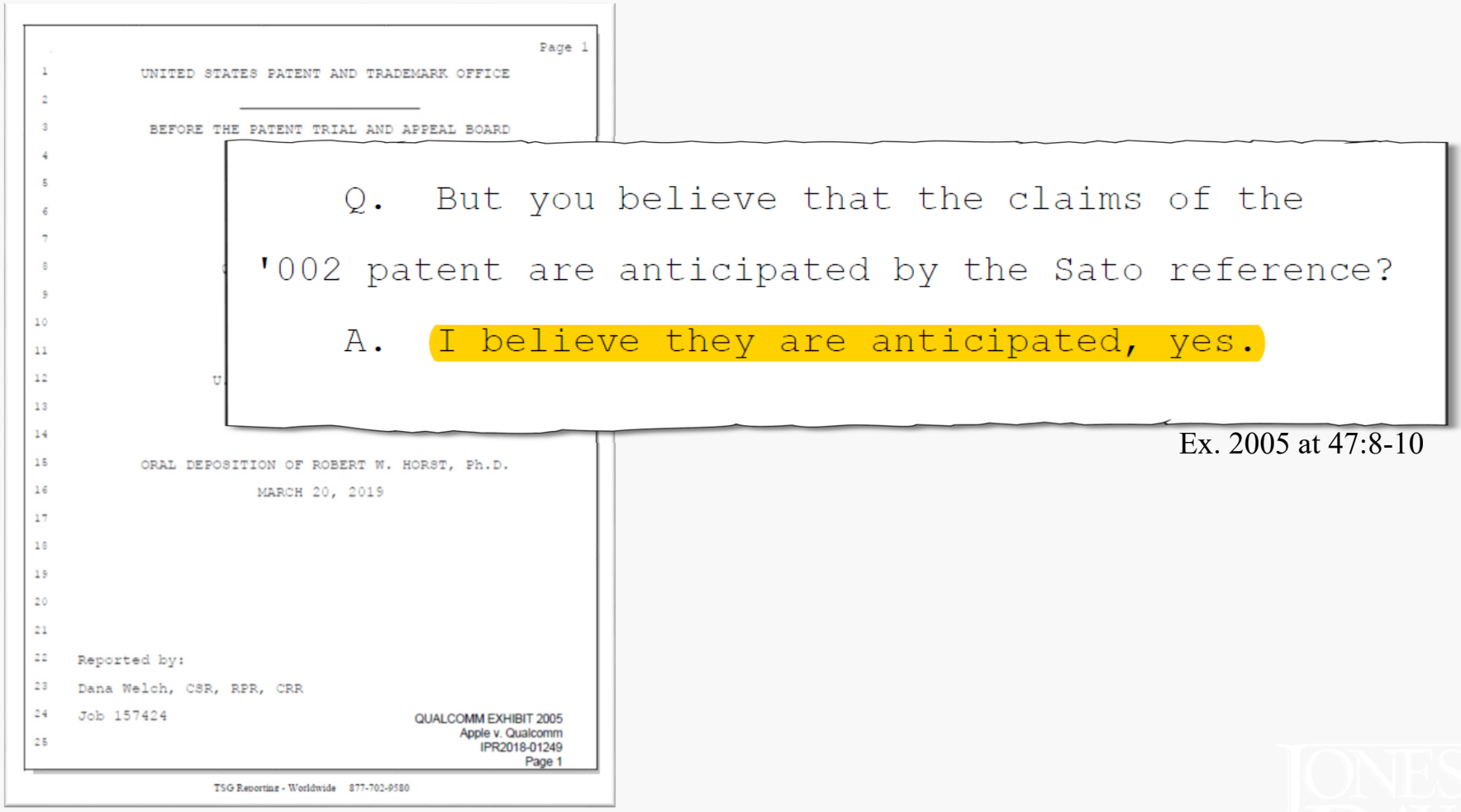
Sato § 103: The Petition Fails to Establish a *Prima Facie* Case of Obviousness

> The Board has recognized that the question of obviousness is resolved on the basis of the four *Graham* factors:
>
> (1) the scope and content of the prior art;
>
> (2) *the differences between the claimed subject matter and the prior art*;
>
> (3) the level of ordinary skill in the art; and
>
> (4) objective evidence of nonobviousness.
>
> *See, e.g., Zetec, Inc. v. Westinghouse Elec. Co., LLC*, IPR2014-00384, Paper 10 at 11-12 (P.T.A.B. July 23, 2014) (citing *Graham*, 383 U.S. at 17-18) (emphasis added).

Paper 11 at 28

Sato § 103: The Petition Fails to Establish a *Prima Facie* Case of Obviousness

Deposition of Petitioner's declarant:



Page 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Q. But you believe that the claims of the '002 patent are anticipated by the Sato reference?

A. I believe they are anticipated, yes.

ORAL DEPOSITION OF ROBERT W. HORST, Ph.D.

MARCH 20, 2019

Reported by:

Dana Welch, CSR, RPR, CRR

Job 157424

QUALCOMM EXHIBIT 2005
Apple v. Qualcomm
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Page 1

TSG Reporting - Worldwide 877-702-9580

Ex. 2005 at 47:8-10

Sato § 103: The Petition Fails to Establish a *Prima Facie* Case of Obviousness

The Petition:

> Sato forms the basis of the Ground-1 in this Petition. As shown in Figure 3 below, Sato selectively applies a clock signal (ϕce) to wordline drivers in a group of wordline drivers using a wordline decoder circuit (X address decoder XDCR) and separate logic circuitry (predecoder (PDCR)).

Paper 2 at 10

> below). Like the first logic in the '002 patent (conditional clock generator 110 and decoder 112-green outline) Sato's PDCR (green) receives both a clock signal (blue) and a first portion of a memory address (purple). APPLE-1001, Figure 1,

Paper 2 at 17

> its output. APPLE-1003, ¶¶14, 65-72. For instance, the PDCR applies a clock signal to one of a plurality of outputs similar to the conditional clock generator 110 of the '002 patent. *Id.* For example, compare the Figure 1 of the '002 patent with

Paper 2 at 19

Sato § 103: The Petition Fails to Establish a *Prima Facie* Case of Obviousness

The Petition:

> Timing signal ϕce represents or renders obvious a clock signal. APPLE-1003, ¶¶64-69. A POSITA would have "viewed the function of the timing signal ϕce as similar to or equivalent to that of a clock signal because 1) "clock" is

Paper 2 at 14-15

> In view of the apparent similarity, Horst explains that a POSITA would have concluded that Sato's timing signal provides a comparable function for the PDCR as a clock signal does for a clocking clocked decoder. *Id.* Dr. Horst also notes that Sato's timing signal provides a comparable function as the clock 118 signal of the '002 patent. *Id.*, ¶¶65-66. Consequently, the POSITA would have reasonably viewed Sato's timing signal as disclosing or rendering obvious a clock signal.

Paper 2 at 16

> Thus, Sato discloses this limitation or at least renders it obvious.

Paper 2 at 17

Patentability

I. SATO DOES NOT RENDER CLAIMS 1-28 AND 31-37 OBVIOUS

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- Sato Does Not Teach or Suggest the Claimed "Clock Signal"
- Sato Does Not Teach or Suggest the Claimed "Clock Output"

II. ASANO AND ITOH DO NOT RENDER CLAIMS 1-17, 20-28, AND 31-36 OBVIOUS

- Petitioner's Combination is Based on Impermissible Hindsight
- The Petition's Motivation to Combine Argument is Flawed

Claim Construction – "Clock Signal"

Qualcomm's proposed construction:

"Clock Signal"

The term "clock signal," as recited in each of the independent claims of the '002 patent, should be interpreted to mean "a periodic signal used for synchronization." This interpretation is consistent with the plain and ordinary

Paper 11 (Qualcomm's Response) at 11

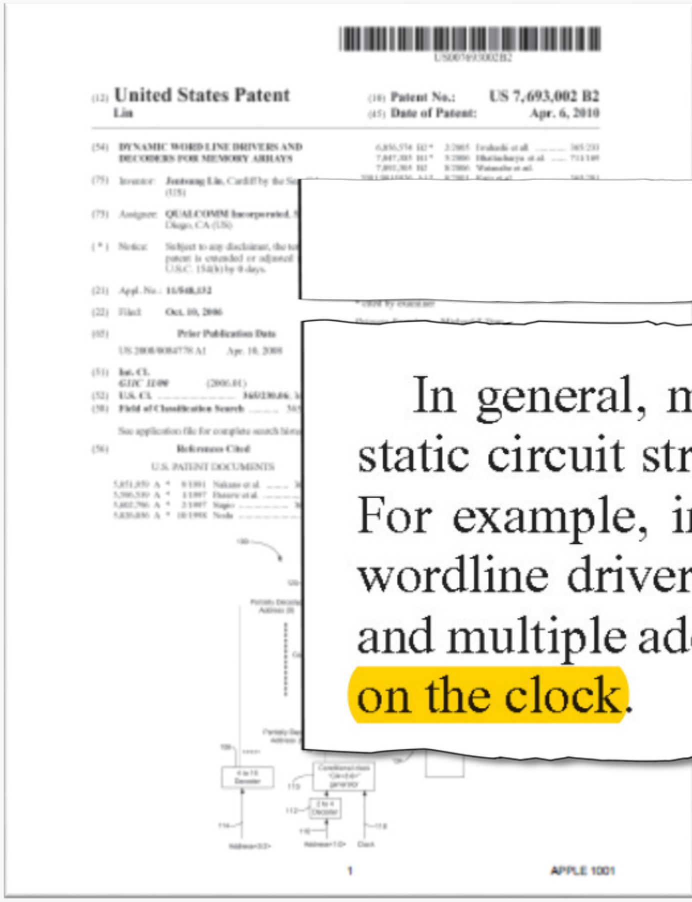
Petitioner's proposed construction:

and objective extrinsic evidence. Petitioner proposes "clock signal" be given its plain meaning, or, if the Board views it necessary to construe the term, "clock signal" should be interpreted as "a signal used for synchronization."

Paper 15 (Petitioner Reply) at 1

Claim Construction – "Clock Signal"

The '002 patent:



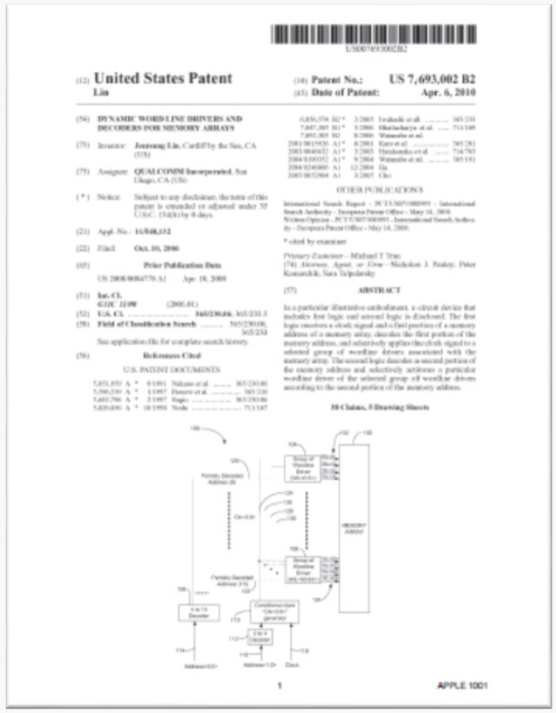
BACKGROUND

In general, memory systems with a traditional dynamic/static circuit structure may place a heavy load on the clock. For example, in a memory structure having a plurality of wordline drivers, a single clock may drive multiple drivers and multiple address decoders, placing a large electrical load on the clock.

Ex. 1001 at 1:11-16

Claim Construction – "Clock Signal"

The '002 patent:



US007693002B2

(12) **United States Patent**
Lin

(10) **Patent No.: US 7,693,002 B2**
(45) **Date of Patent: Apr. 6, 2010**

(54) **DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY ARRAYS**

(75) Inventor: **Jintung Lin**, Cardiff by the Sea, CA (US)

(73) Assignee: **QUALCOMM Incorporated**, San Diego, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/548,132**

(22) Filed: **Oct. 10, 2006**

(65) **Prior Publication Data**

US 2008/0084770 A1 Apr. 10, 2008

(51) **Int. Cl.**
G11C 11/00 (2006.01)

(52) **U.S. Cl.** **365/230.06**; 365/233.5

(58) **Field of Classification Search** 365/230.06, 365/233
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

OTHER PUBLICATIONS

* cited by examiner

Primary Examiner—Michael T Tran
(74) Attorney, Agent, or Firm—Nicholas J. Pauley; Peter Kamarchik; Sara Tolpadosky

(57) **ABSTRACT**

30 Claims, 5 Drawing Sheets

1

APPLE 1001

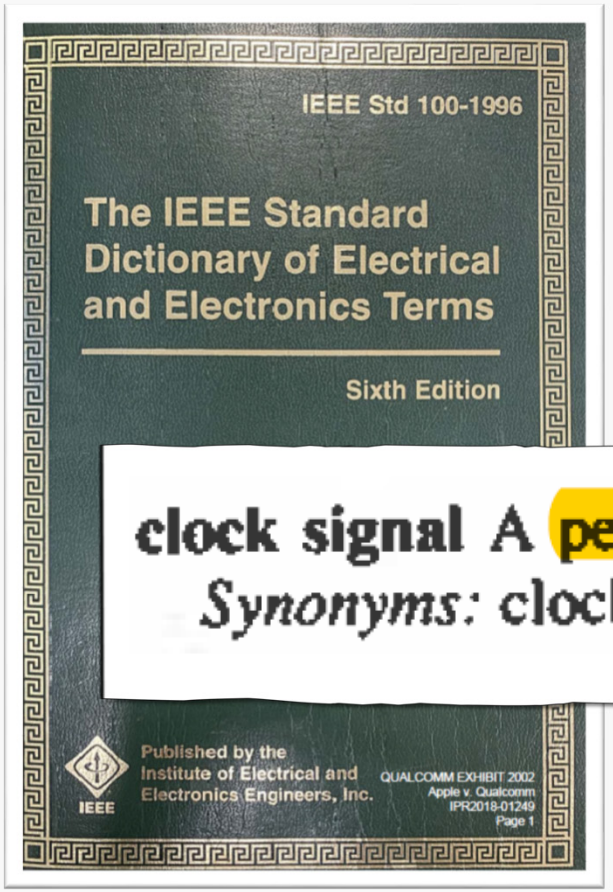
SUMMARY

One particular advantage of a particular illustrative embodiment of the circuit device is that a timing delay from a clock to a particular wordline is reduced. Still another particular advantage of a particular illustrative embodiment of the circuit device is that the clock driver's capacitance loading may also be reduced. Another particular advantage of a particular illustrative embodiment is that use of multiple conditional clocks to selectively apply a clock signal reduces power consumption. In a particular embodiment, the clock power consumption may be reduced to one-fourth of the power consumed by a single clock system (e.g. the power consumption of a clock generator may be reduced by 75%). This reduction in power consumption provides an additional advantage in that power is conserved for use in other processes and/or to extend an operational life of a power source, such as a battery.

Ex. 1001 at 1:64-2:12

Claim Construction – "Clock Signal"

The IEEE Dictionary:



clock signal A **periodic signal** used for synchronizing events.
Synonyms: clock pulse; timing pulse. (C) 610.10-1994

Ex. 2002 at 9

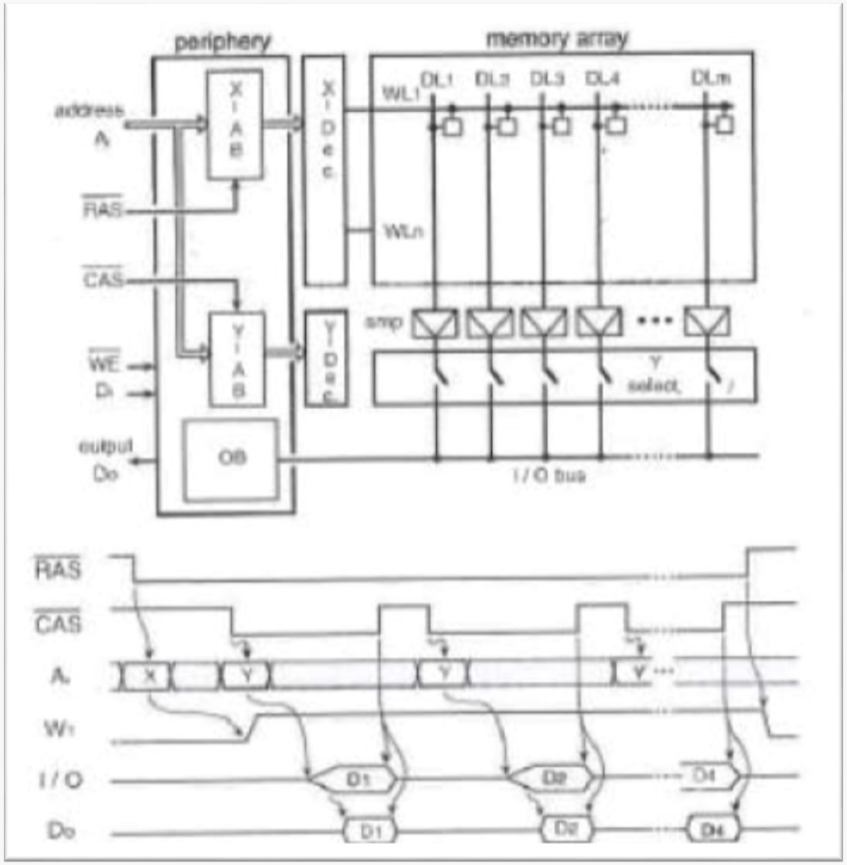
Claim Construction – "Clock Signal"

Asynchronous memory systems:

56. Asynchronous static RAMs (SRAMs) respond to asynchronous changes at the device's address pins by generating multiple internal timing signals that are used to orchestrate the operation of the SRAM's internal circuitry during a read or a write operation. Essentially, this means that there exists some control logic circuitry in the asynchronous SRAM that can asynchronously accept externally asserted control signals, read row and column addresses, and then generate appropriately timed sequences of internal timing signals (in the form of pulses or strobe signals) to direct the movement of data onto, within, and off of the SRAM. The external interface to the control logic on the asynchronous SRAM

low write enable (WE#). Various timing constraints among the external control signals and address/data signals must be satisfied in order to ensure correct operation.[2] The duration and precise timing of internal timing signals is also key to the correct operation of the device. Guaranteeing that the controller can

Ex. 2001 (Pedram Decl.) at ¶56



Itoh Fig. 6.14 – "The asynchronous operation of a DRAM chip." (Ex. 2003 at 18.)

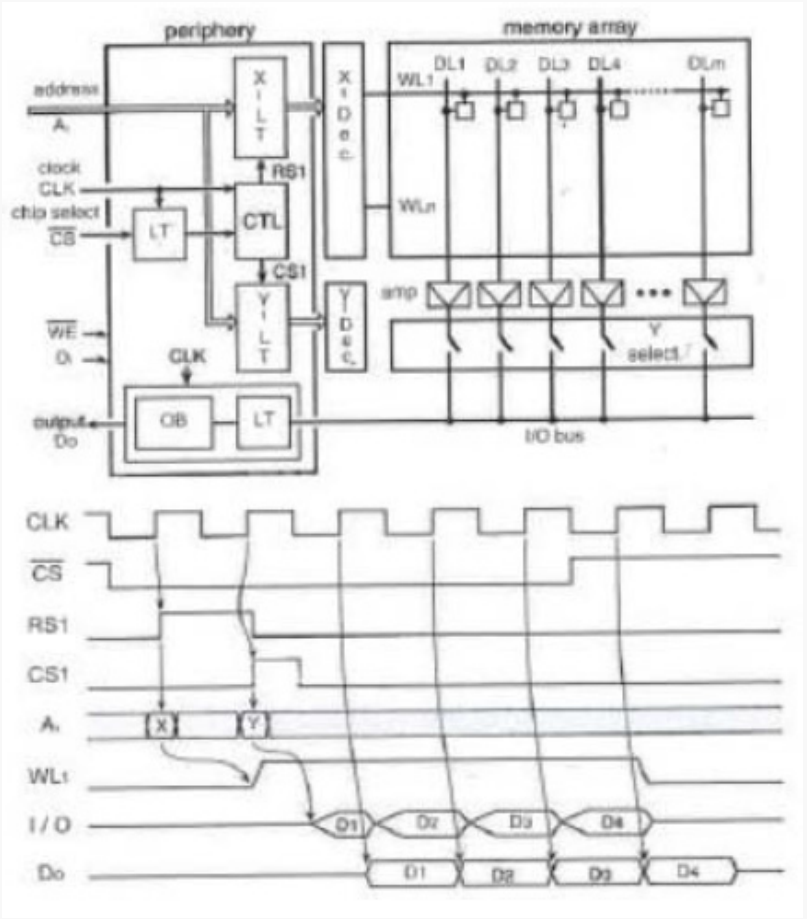
Claim Construction – "Clock Signal"

Synchronous memory systems:

61. An alternative to asynchronous memory is to make the RAM interface synchronous, such that requests can only arrive at regular intervals of a periodic clock signal. This allows the latches internal to the RAM to be controlled by a common, periodic system clock signal. The primary benefit of synchronous RAM, or synchronizing RAM operation with the CPU clock, is that it improves the predictability of event timing—put simply, events such as the arrival of commands or the driving of output data either occur in synchrony with the periodic clock, or they do not occur. Stated differently, synchronous RAM drives internal activities

Ex. 2003 (Itoh) at 19. In the synchronous system depicted above, a periodic clock signal "CLK" is used, and all events occur in synchrony with the periodic clock signal CLK. In particular, a row address strobe signal RS1 is generated from the

Ex. 2001 (Pedram Decl.) at ¶¶61-62



Itoh Fig. 6.15 – "The synchronous operation of a DRAM chip." (Ex. 2003 at 19.)

Claim Construction – "Clock Signal"

Dr. Massoud Pedram:

65. The POSA would understand that the '002 patent discloses a synchronous memory system that uses a periodic clock signal. Indicia of this can be found in the fact that the patent does not describe a timing generator circuit to generate various internal timing signals in response to externally provided control

Patent 7,693,002

DECLARATION OF DR. MASSOUD PEDRAM

I, Massoud Pedram, do hereby declare:

1. I am making this declaration at the request of Qualcomm Incorporated ("Qualcomm" or "Patent Owner") in the matter of the *Inter Partes* Review of U.S. Patent No. 7,693,002 ("the '002 patent").

2. I am being compensated for my work in this matter at my standard hourly rate of $900 for consulting services. My compensation in no way depends on the outcome of this proceeding.

3. In preparing this Declaration, I considered the following materials:

   a. The '002 patent (Ex. 1001) and its file history (Ex. 1002);

QUALCOMM EXHIBIT 2001
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Page 1

Ex. 2001 (Pedram Decl.) at ¶65

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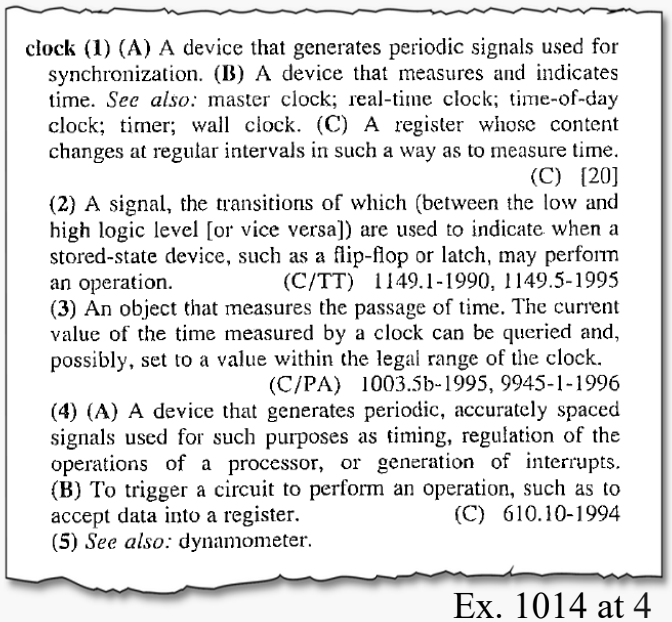
Claim Construction – "Clock Signal"

Petitioner's dictionary definitions for the term "clock":



clock (1) (A) A device that generates periodic signals used for synchronization. **(B)** A device that measures and indicates time. *See also:* master clock; real-time clock; time-of-day clock; timer; wall clock. **(C)** A register whose content changes at regular intervals in such a way as to measure time. (C) [20]

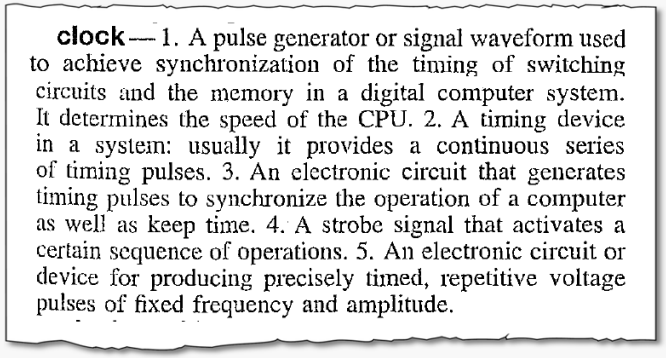
(2) A signal, the transitions of which (between the low and high logic level [or vice versa]) are used to indicate when a stored-state device, such as a flip-flop or latch, may perform an operation. (C/TT) 1149.1-1990, 1149.5-1995

(3) An object that measures the passage of time. The current value of the time measured by a clock can be queried and, possibly, set to a value within the legal range of the clock. (C/PA) 1003.5b-1995, 9945-1-1996

(4) (A) A device that generates periodic, accurately spaced signals used for such purposes as timing, regulation of the operations of a processor, or generation of interrupts. **(B)** To trigger a circuit to perform an operation, such as to accept data into a register. (C) 610.10-1994

(5) *See also:* dynamometer.

Ex. 1014 at 4



clock—1. A pulse generator or signal waveform used to achieve synchronization of the timing of switching circuits and the memory in a digital computer system. It determines the speed of the CPU. 2. A timing device in a system: usually it provides a continuous series of timing pulses. 3. An electronic circuit that generates timing pulses to synchronize the operation of a computer as well as keep time. 4. A strobe signal that activates a certain sequence of operations. 5. An electronic circuit or device for producing precisely timed, repetitive voltage pulses of fixed frequency and amplitude.

Ex. 1015 at 3-4

IEEE Dictionary

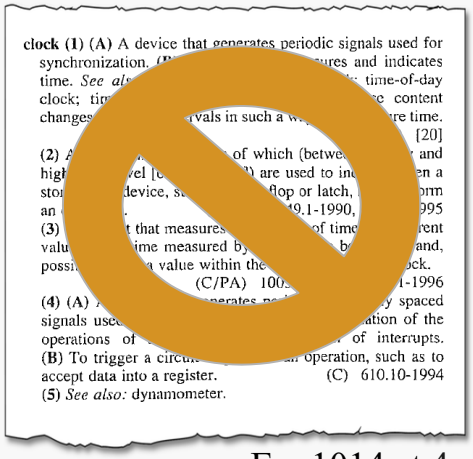
Seven (7) entries for the term "clock"

Modern Dictionary of Electronics

Five (5) entries for the term "clock"

Claim Construction – "Clock Signal"

Petitioner's dictionaries:

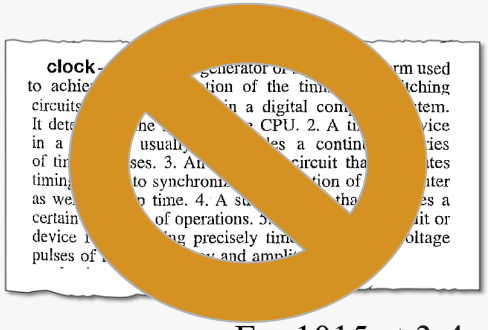


Ex. 1014 at 4

IEEE Dictionary

clock signal A periodic signal used for synchronizing events. *Synonyms:* clock pulse; timing pulse. (C) 610.10-1994

Ex. 2002 at 9



Ex. 1015 at 3-4

Modern Dictionary of Electronics

clock frequency — In digital computers, the master frequency of periodic pulses that are used to schedule the operation of the computer.

Ex. 1015 at 4

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Signal"

The '002 patent claims:

1. A circuit device comprising:

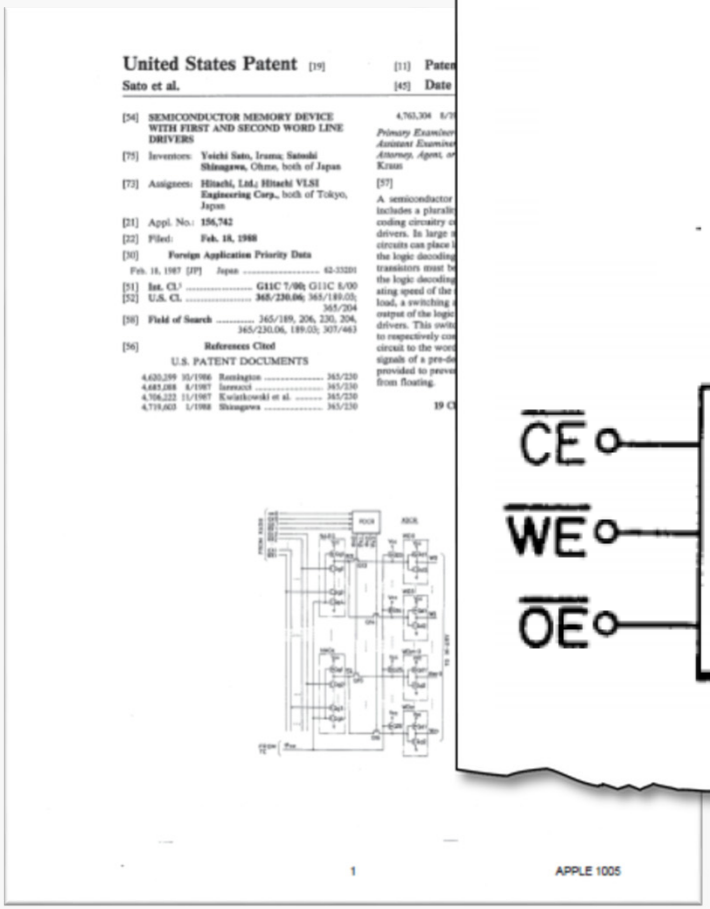
first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

Ex. 1001 at 10:65-11:10

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Signal"

Sato:



United States Patent [19]

Sato et al.

[54] SEMICONDUCTOR MEMORY DEVICE WITH FIRST AND SECOND WORD LINE DRIVERS

[75] Inventors: Yoichi Sato, Iruma; Satoshi Shinagawa, Ohme, both of Japan

[73] Assignees: Hitachi, Ltd.; Hitachi VLSI Engineering Corp., both of Tokyo, Japan

[21] Appl. No.: 156,742

[22] Filed: Feb. 18, 1988

[30] Foreign Application Priority Data

Feb. 18, 1987 [JP] Japan 62-33201

[51] Int. Cl.[3] G11C 7/00; G11C 8/00

[52] U.S. Cl. 365/230.06; 365/189.03; 365/204

[58] Field of Search 365/189, 206, 230, 204, 365/230.06, 189.03; 307/463

[56] References Cited

U.S. PATENT DOCUMENTS

4,620,299 10/1986 Remington 365/230
4,685,088 8/1987 Iaresci 365/230
4,706,222 11/1987 Kwiatkowski et al. 365/230
4,719,603 1/1988 Shinagawa 365/230

[11] Paten

[45] Date

4,763,304 8/1

Primary Examiner
Assistant Examiner
Attorney, Agent, or
Kraus

[57]

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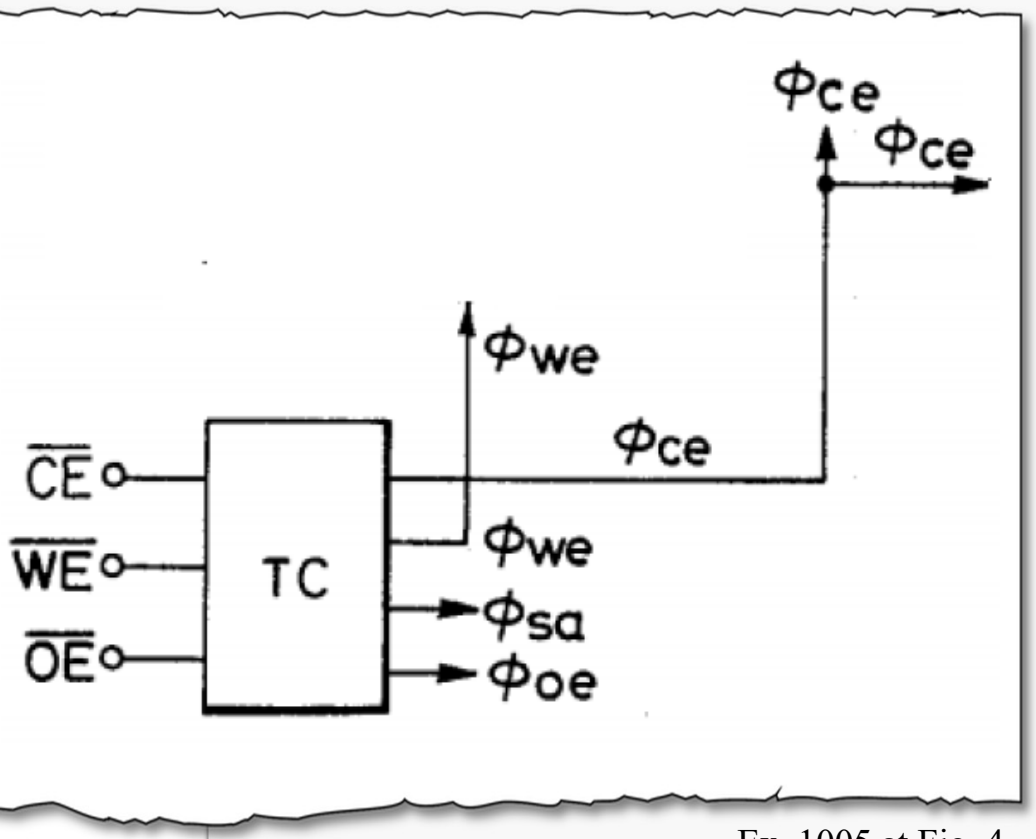
APPLE 1005



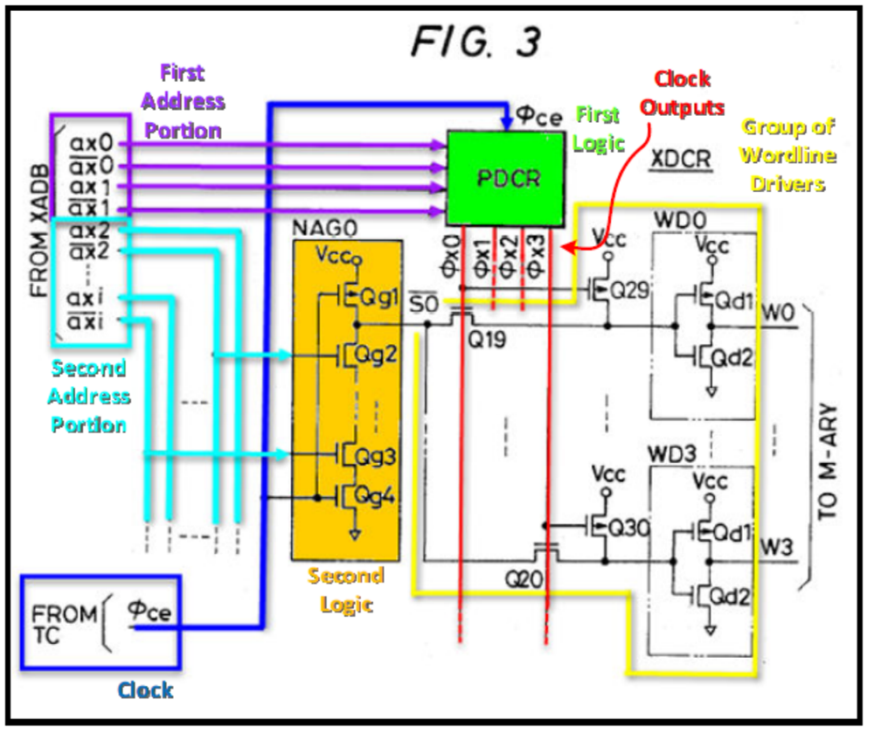
Ex. 1005 at Fig. 4

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Signal"

The Petition:

Sato forms the basis of the Ground-1 in this Petition. As shown in Figure 3 below, Sato selectively applies a clock signal (ϕce) to wordline drivers in a group of wordline drivers using a wordline decoder circuit (X address decoder XDCR) and separate logic circuitry (predecoder (PDCR)).

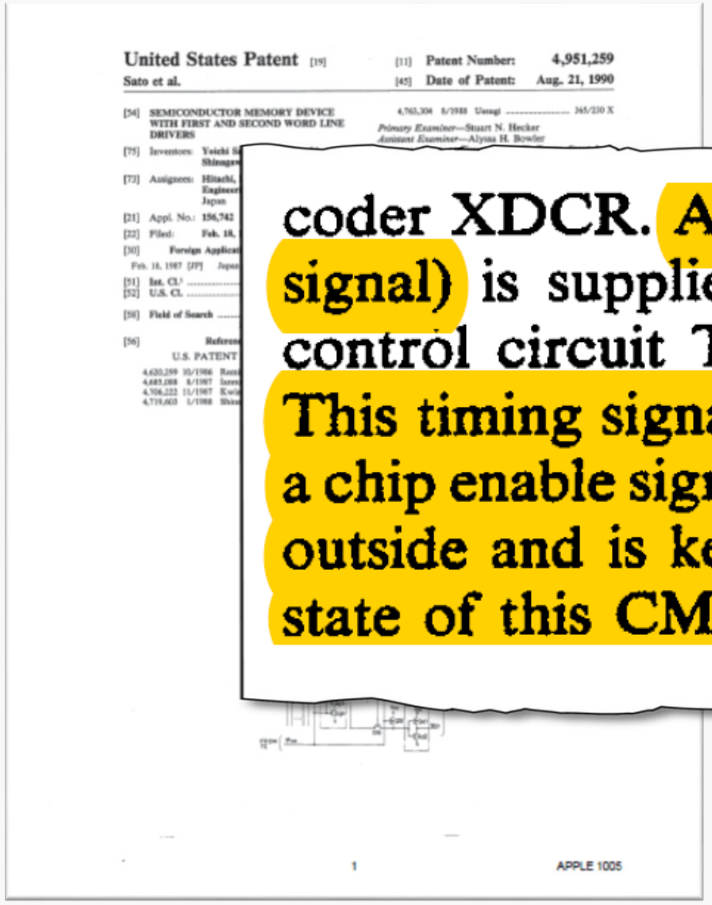
FIG. 3



Paper 2 at 10

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Signal"

Sato:


United States Patent [19]
Sato et al.

[11] Patent Number: 4,951,259
[45] Date of Patent: Aug. 21, 1990

[54] SEMICONDUCTOR MEMORY DEVICE WITH FIRST AND SECOND WORD LINE DRIVERS

1

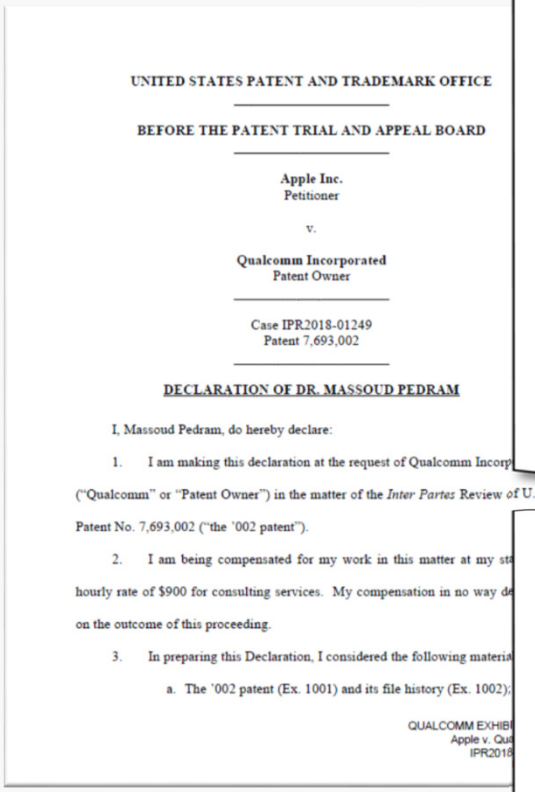
APPLE 1005

coder XDCR. A timing signal ϕce (a selection control signal) is supplied, too, from a later-discussed timing control circuit TC to the X address decoder XDCR. This timing signal ϕce is generated in accordance with a chip enable signal $\overline{CE}$ supplied as a control signal from outside and is kept at a high level under the selection state of this CMOS static RAM. As will be described

Ex. 1005 at 3:59-65

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Signal"

Dr. Massoud Pedram:



UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc.
Petitioner

v.

Qualcomm Incorporated
Patent Owner

Case IPR2018-01249
Patent 7,693,002

DECLARATION OF DR. MASSOUD PEDRAM

I, Massoud Pedram, do hereby declare:

1. I am making this declaration at the request of Qualcomm Incorp
("Qualcomm" or "Patent Owner") in the matter of the *Inter Partes* Review of U.S.
Patent No. 7,693,002 ("the '002 patent").

2. I am being compensated for my work in this matter at my st
hourly rate of $900 for consulting services. My compensation in no way de
on the outcome of this proceeding.

3. In preparing this Declaration, I considered the following materia

a. The '002 patent (Ex. 1001) and its file history (Ex. 1002);

QUALCOMM EXHIB
Apple v. Qua
IPR2018

97. Sato provides no teaching that the chip enable signal CE# is periodic, and in fact, this signal would not be periodic. CE# assumes a low value only when the CMOS static RAM of Sato is selected for read or write operations, and otherwise assumes a high value. The signal ϕce has a value that is opposite that of the CE# signal, such that ϕce assumes a high value only when the CMOS static RAM of Sato is selected for read or write operation, and otherwise assumes a low value. The access pattern to a static RAM is determined by the access needs of the component or device using the static RAM as memory. For example, in the very

98. The resulting access pattern is highly irregular and does not result in a periodic high/low state of CE#, and therefore, ϕce is not a periodic signal. Sato does not suggest that its static RAM would be accessed in a regular manner. A

Ex. 2001 at ¶¶97-98

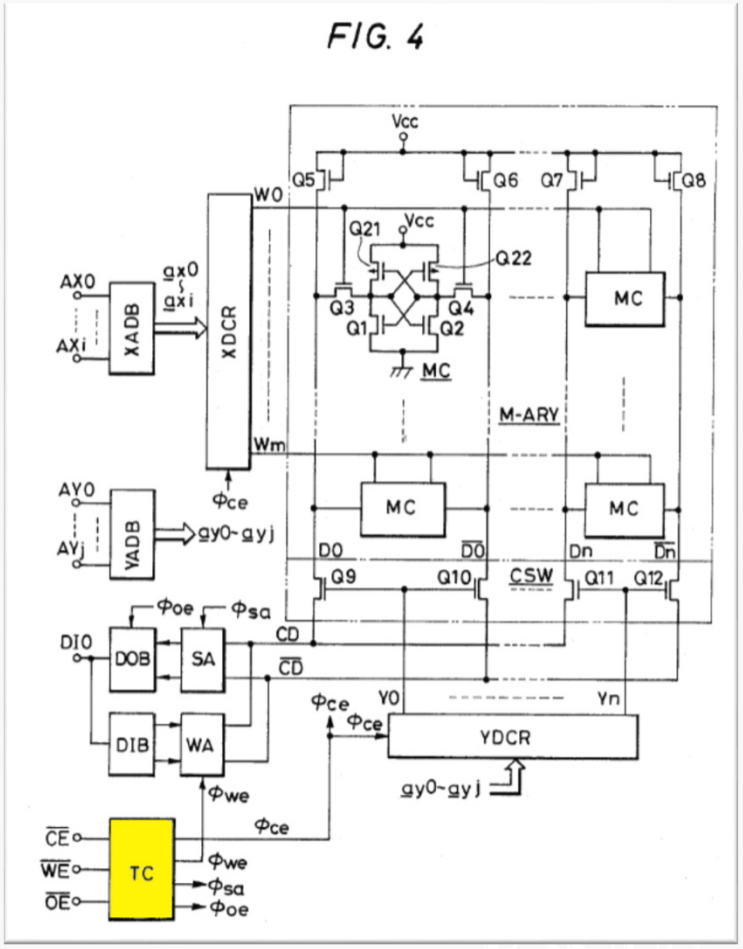
Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Signal"

Dr. Massoud Pedram:

102. The POSA would understand Sato's memory system to be asynchronous because it is an exact match of the asynchronous systems described above. In Sato, the timing control circuit TC is the control logic circuitry required by asynchronous memory systems. The timing circuit TC takes as input asynchronous external control signals (chip enable signal CE#, write enable signal WE#, and output enable signal OE#) and generates timing signals ϕce, ϕsa, ϕoe, and ϕwe. These timing signals are used to effect address decoding and memory

above. Thus, in Sato, there is no single, periodic clock signal to which memory operations are synchronized, but rather multiple internal timing signals ϕce, ϕwe, ϕsa, and ϕoe for controlling different components of the memory system.

Ex. 2001 at ¶102



Ex. 1005 at Fig. 4

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Signal"

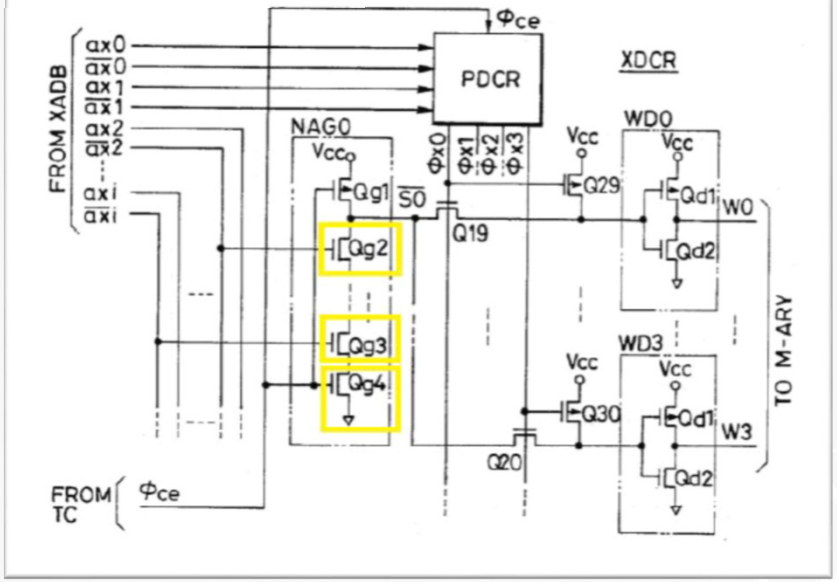
Deposition of Petitioner's declarant:

> Q. Well, what if they're not fast enough? Then would it work?

> THE WITNESS: If the transistors weren't fast enough and you gave it a clock that was too fast, it wouldn't function.

Ex. 2006 at 87:24-88:5

FIG. 3



Ex. 1005 at Fig. 3

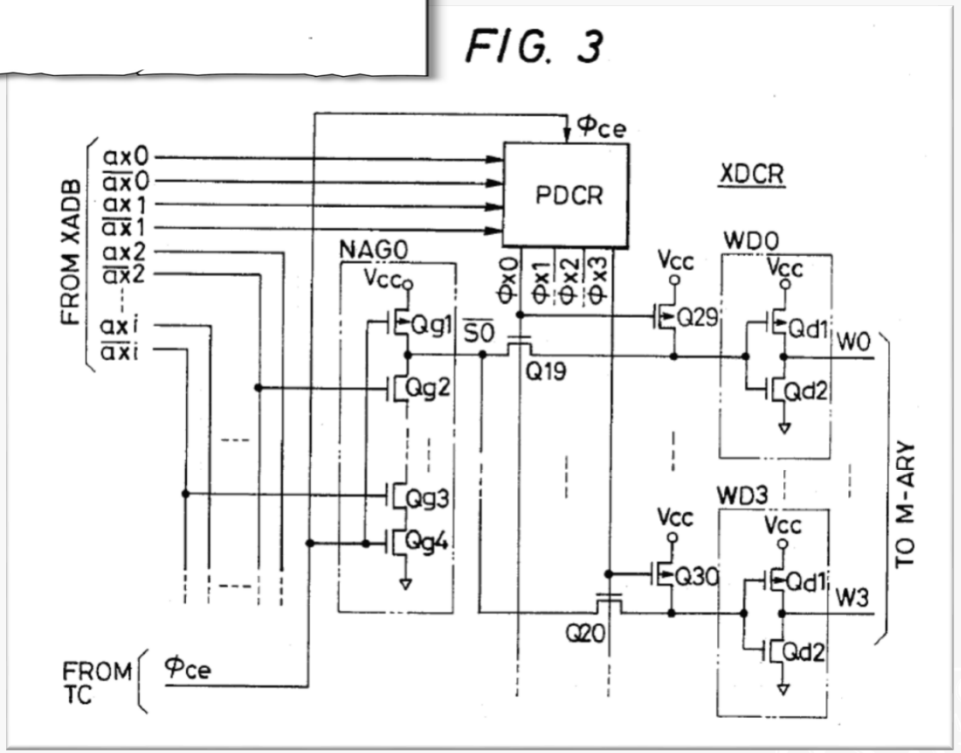
Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Signal"

Sato:

the circuit. The gates of these reset MOSFETs Q29~Q30 are connected in common to the gates of the corresponding capacitance cut MOSFET Q19~Q20, and the corresponding selection signals $\phi x0 \sim \phi x3$ are supplied to them, respectively.

Ex. 1005 at 9:68-10:4

FIG. 3



Ex. 1005 at Fig. 3

Patentability

I. SATO DOES NOT RENDER CLAIMS 1-28 AND 31-37 OBVIOUS

- The Petition Fails to Establish a *Prima Facie* Case of Obviousness
- Sato Does Not Teach or Suggest the Claimed "Clock Signal"
- Sato Does Not Teach or Suggest the Claimed "Clock Output"

II. ASANO AND ITOH DO NOT RENDER CLAIMS 1-17, 20-28, AND 31-36 OBVIOUS

- Petitioner's Combination is Based on Impermissible Hindsight
- The Petition's Motivation to Combine Argument is Flawed

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Output"

The '002 patent claims:

1. A circuit device comprising:

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

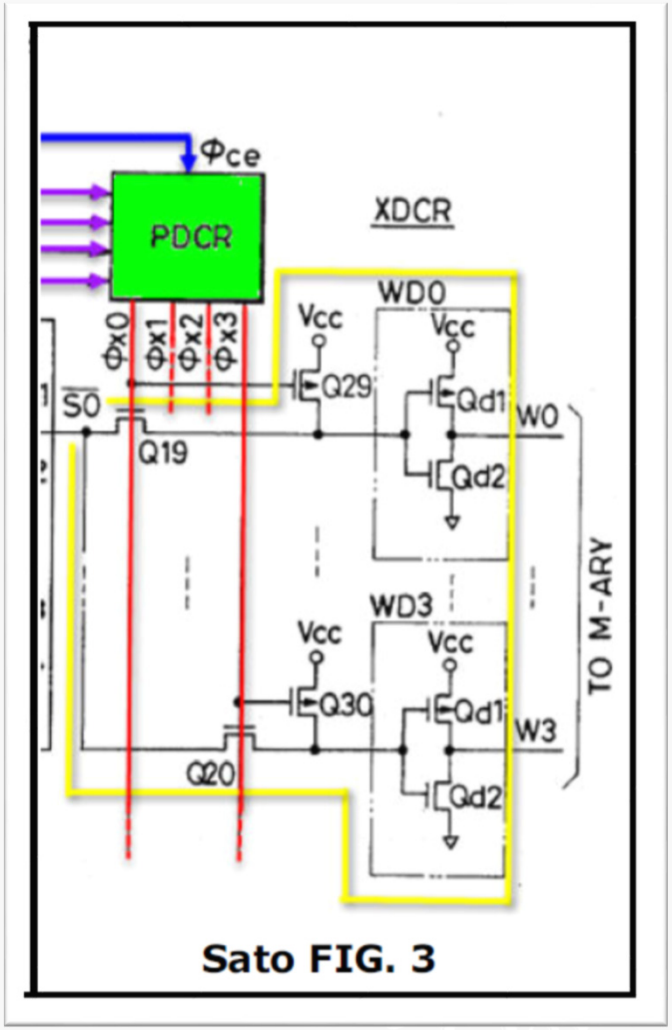
Ex. 1001 at 10:65-11:10

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Output"

The Petition:

110 (green outline) in the '002 patent, the PDCR (green) applies the clock signal (blue) to one of four outputs (red) according to the first portion of the memory address (purple). *Compare* APPLE-1001, 3:26-36 *with* APPLE-1005, 5:25-31, 10:36-39; *see also* APPLE-1003, ¶¶14, 65-72.

Paper 2 at 19



Paper 2 at 20

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Output"

Sato's "timing signal" or "selection control signal" ϕce:

coder XDCR. A timing signal ϕce (a selection control signal) is supplied, too, from a later-discussed timing control circuit TC to the X address decoder XDCR.

Ex. 1005 at 3:59-61

plied from the Y address buffer YADB. This Y address decoder YDCR is operated selectively in accordance with the timing signal ϕce supplied from the timing control circuit TC in the same way as the X address decoder XDCR.

Ex. 1005 at 4:27-31

potential. The gates of MOSFETs Qg1 and Qg4 are connected in common and the timing signal ϕce (selection control signal) described above is supplied to them.

Ex. 1005 at 5:48-50

source voltage Vcc of the circuit. The timing signal ϕce described above is supplied in common to the gates of these reset MOSFETs. These reset MOSFETs

Ex. 1005 at 7:1-3

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Output"

Sato's "selection signals" ϕx0, ϕx1, ϕx2, and ϕx3:

gate circuit of the X address decoder XDCR. Each word line drive circuit has the function of a part of the X address decoder XDCR when the corresponding selection signal ϕx0~ϕx3 is supplied from the pre-decoder PDCR descri[illegible] to the source of the P-channel MOSFET [illegible] drive circuit.

Ex. 1005 at 1:48-54

The pre-decoder PDCR decodes the lower 2-bit complementary internal address signals ax0 and axl supplied thereto from the X address buffer XADB and generates selection signals ϕx0~ϕx3. These selection signals ϕx0~ϕx3 are formed selectively in accordance with the complementary internal address signals ax0 and ax1. In other words, the selection signal ϕx0 is set to the high logic level when both the inversed internal address signals $\overline{ax0}$ and $\overline{ax1}$ are at the high logic level. Similarly, the selection signals ϕx1, ϕx2 and ϕx3 are set to the high logic level when both the non-inversed internal address signal ax0 and the inversed internal address signal $\overline{ax1}$ are at the [illegible] the inversed internal add[illegible] inversed internal address sig[illegible] level and when both the no[illegible] signals ax0 and ax1 are at t[illegible] tively.

Ex. 1005 at 5:25-42

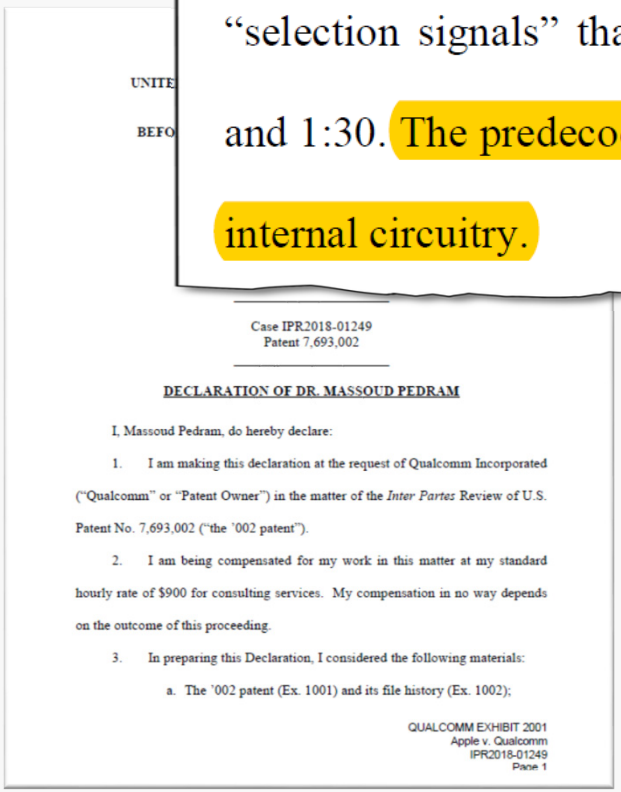
Q15~Q16, respectively. Among the four capacitance cut MOSFETs of each set, the selection signal ϕx0 is supplied in common from the pre-decoder PDCR to the gate of the first MOSFET represented by MOSFETs Q13 and Q15, and the selection signal ϕx3 is supplied in common to the gate of the fourth MOSFET represented by MOSFETs Q14 and Q16. Similarly, the selection signals ϕxl and ϕx2 are supplied in common from the pre-decoder PDCR to the gates of the second and third MOSFETs among the four capacitance cut MOSFETs of each set, respectively. Accordingly, the in-

Ex. 1005 at 6:45-56

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Output"

Dr. Massoud Pedram:

ϕx0-ϕx3. *Id.* at 5:25-42. Sato refers to these outputs from the predecoder as "selection signals" that "control output signals of a predecoder." *Id.* at Abstract and 1:30. The predecoder PDCR is a black box. Sato provides no disclosure on its internal circuitry.



UNITE

BEFO

Case IPR2018-01249
Patent 7,693,002

DECLARATION OF DR. MASSOUD PEDRAM

I, Massoud Pedram, do hereby declare:

1. I am making this declaration at the request of Qualcomm Incorporated ("Qualcomm" or "Patent Owner") in the matter of the *Inter Partes* Review of U.S. Patent No. 7,693,002 ("the '002 patent").

2. I am being compensated for my work in this matter at my standard hourly rate of $900 for consulting services. My compensation in no way depends on the outcome of this proceeding.

3. In preparing this Declaration, I considered the following materials:

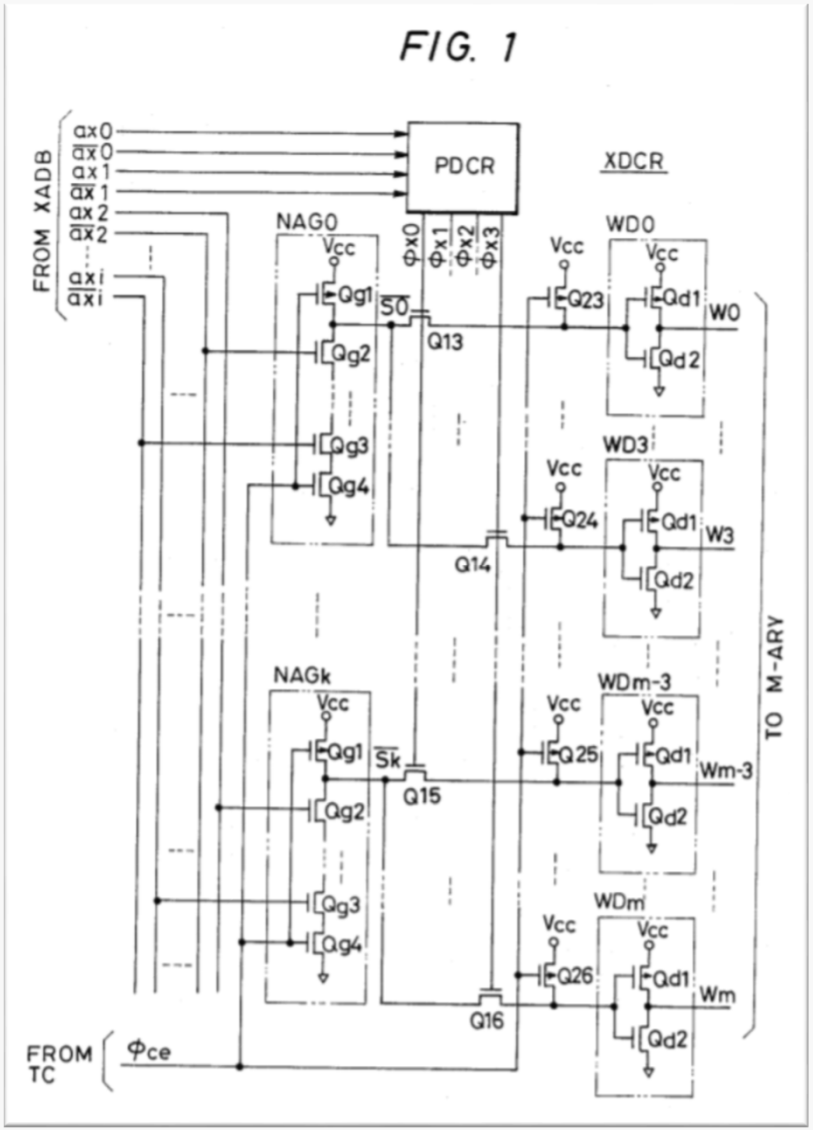
a. The '002 patent (Ex. 1001) and its file history (Ex. 1002);

QUALCOMM EXHIBIT 2001
Apple v. Qualcomm
IPR2018-01249
Page 1

Ex. 2001 at ¶76

Sato § 103: Sato Does Not Teach or Suggest the Claimed "Clock Output"

Sato:



Ex. 1005 at Fig. 1

The pre-decoder PDCR decodes the lower 2-bit complementary internal address signals ax0 and axl supplied thereto from the X address buffer XADB and generates selection signals $\phi x0 \sim \phi x3$. These selection signals $\phi x0 \sim \phi x3$ are formed selectively in accordance with the complementary internal address signals ax0 and ax1. In other words, the selection signal $\phi x0$ is set to the high logic level when both the inversed internal address signals $\overline{ax0}$ and $\overline{ax1}$ are at the high logic level. Similarly, the selection signals $\phi x1$, $\phi x2$ and $\phi x3$ are set to the high logic level when both the non-inversed internal address signal ax0 and the inversed internal address signal $\overline{ax1}$ are at the high logic level, when both the inversed internal address signal $\overline{ax0}$ and non-inversed internal address signal ax1 are at the high logic level and when both the non-inversed internal address signals ax0 and ax1 are at the high logic level, respectively.

Ex. 1005 at 5:25-42

Patentability

I. SATO DOES NOT RENDER CLAIMS 1-28 AND 31-37 OBVIOUS

- The Petition Fails to Establish a *Prima Facie* Case of Obviousness
- Sato Does Not Teach or Suggest the Claimed "Clock Signal"
- Sato Does Not Teach or Suggest the Claimed "Clock Output"

II. ASANO AND ITOH DO NOT RENDER CLAIMS 1-17, 20-28, AND 31-36 OBVIOUS

- Petitioner's Combination is Based on Impermissible Hindsight
- The Petition's Motivation to Combine Argument is Flawed

Asano and Itoh: Petitioner's Combination is Based on Impermissible Hindsight

(12) **United States Patent**
Lin

(10) **Patent No.:** **US 7,693,002 B2**
(45) **Date of Patent:** **Apr. 6, 2010**

(54) **DYNAMIC WORD LINE DRIVERS AND DECODERS FOR MEMORY**

6,856,574 B2 * 2/2005 Iwahashi et al. 365/233

(75) Inventor: **Jentsung Lin**, Card (US)

(73) Assignee: **QUALCOMM Inc** Diego, CA (US)

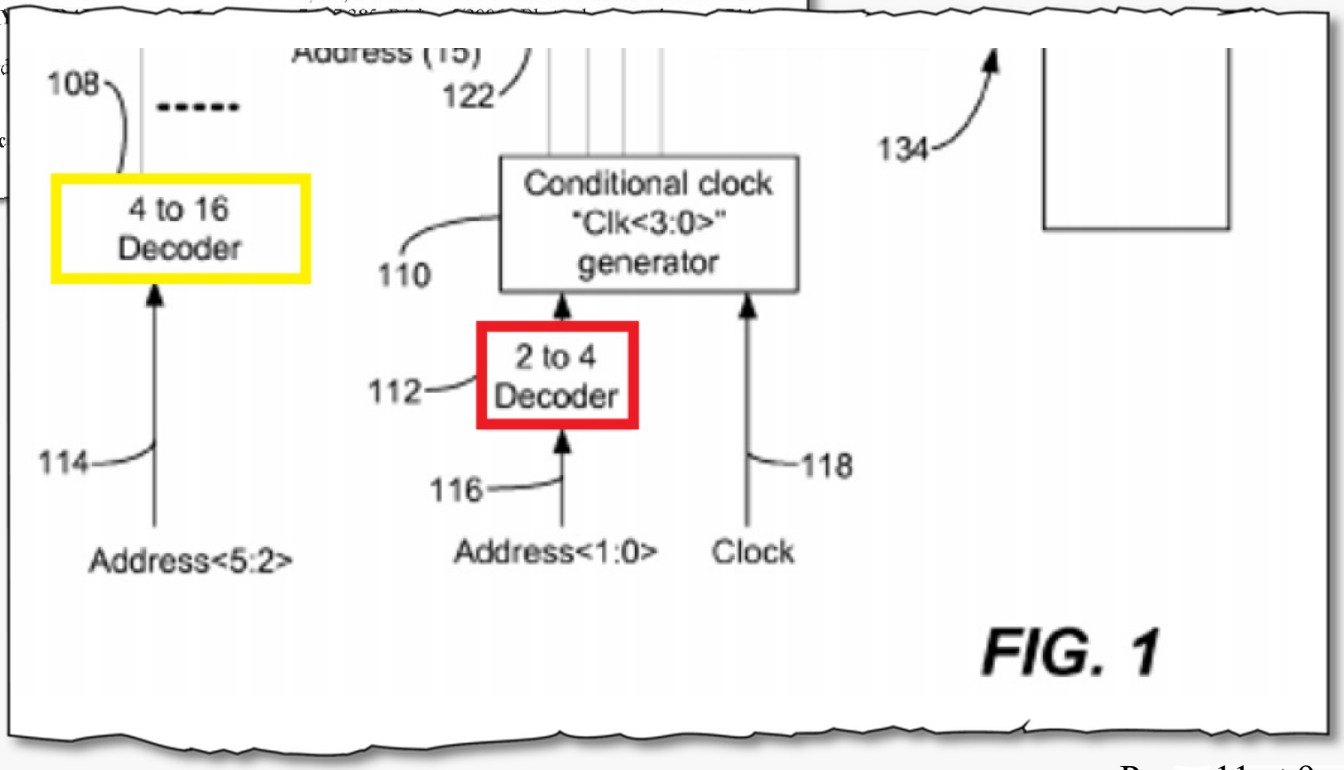
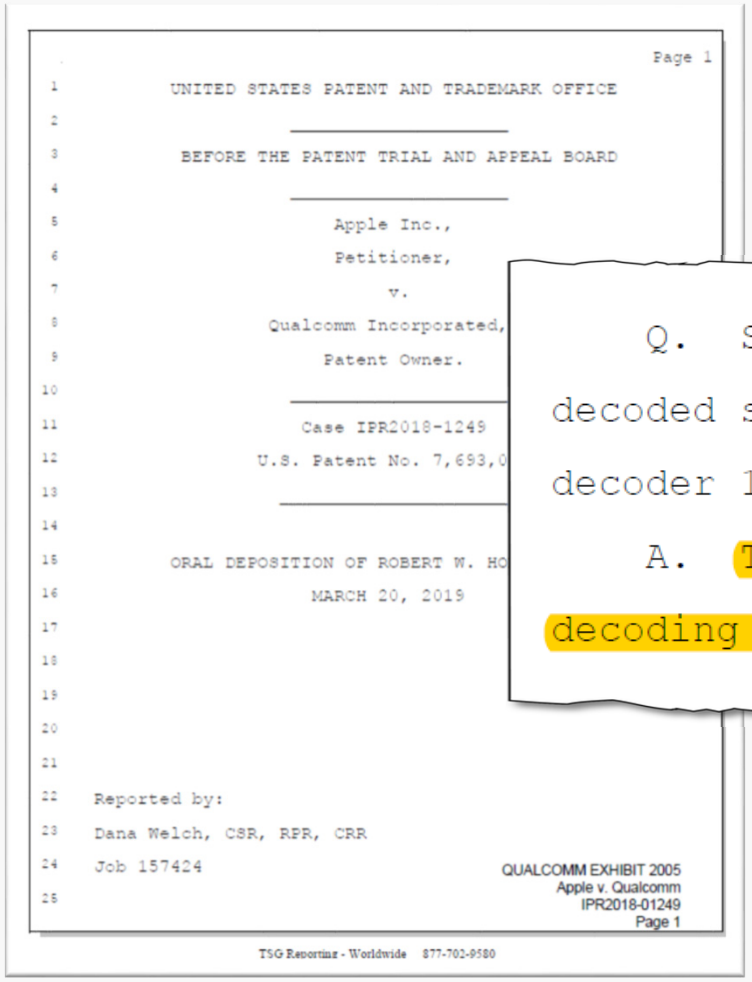


FIG. 1

Paper 11 at 9

Asano and Itoh: Petitioner's Combination is Based on Impermissible Hindsight

Deposition of Petitioner's declarant:



Page 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc.,
Petitioner,
v.
Qualcomm Incorporated,
Patent Owner.

Case IPR2018-1249
U.S. Patent No. 7,693,0

ORAL DEPOSITION OF ROBERT W. HO
MARCH 20, 2019

Reported by:
Dana Welch, CSR, RPR, CRR
Job 157424

QUALCOMM EXHIBIT 2005
Apple v. Qualcomm
IPR2018-01249
Page 1

TSG Reporting - Worldwide 877-702-9580

Q. So in Figure 1, the address bits are decoded separately by the decoder 112 and the decoder 108, correct?

A. This shows separate decoders doing those decoding functions.

Ex. 2005 at 16:10-14

Asano and Itoh: Petitioner's Combination is Based on Impermissible Hindsight

Asano:

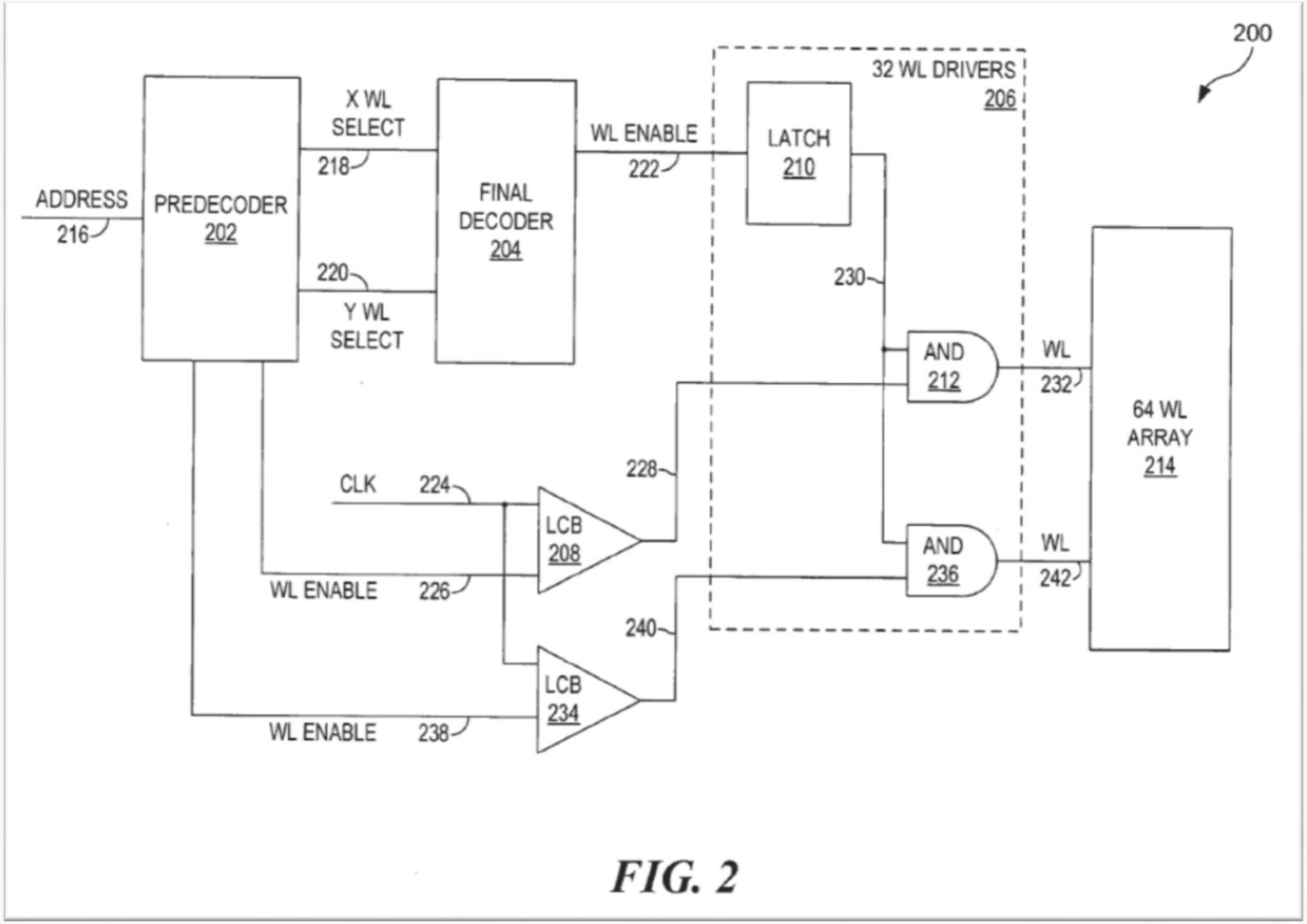


FIG. 2

Ex. 1006 at Fig. 2

Asano and Itoh: Petitioner's Combination is Based on Impermissible Hindsight

Petition:

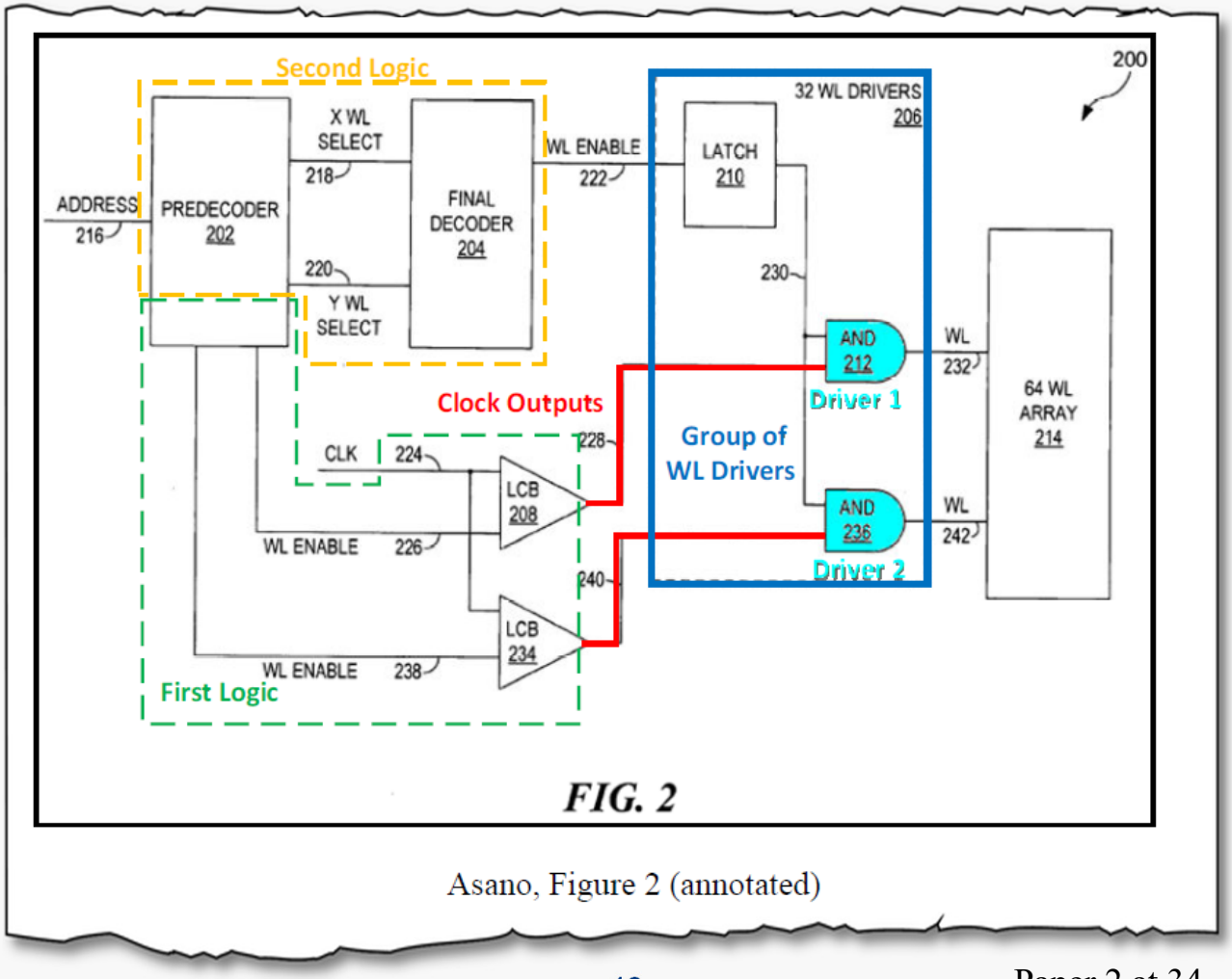


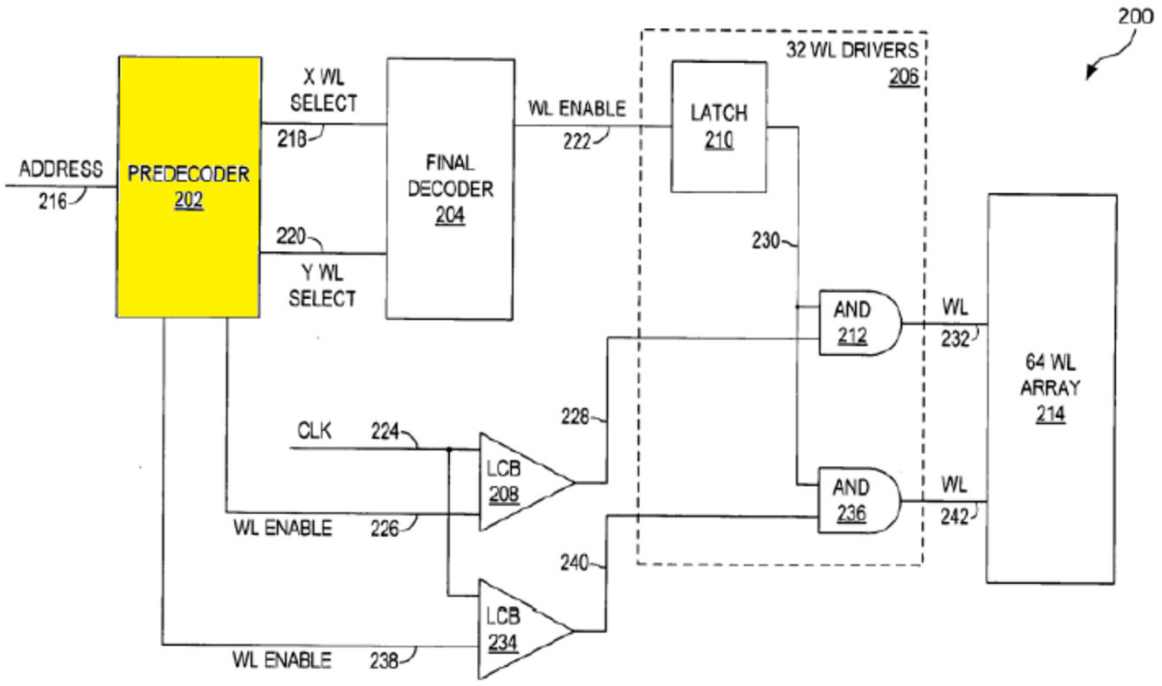
FIG. 2

Asano, Figure 2 (annotated)

Asano and Itoh: Petitioner's Combination is Based on Impermissible Hindsight

Dr. Massoud Pedram:

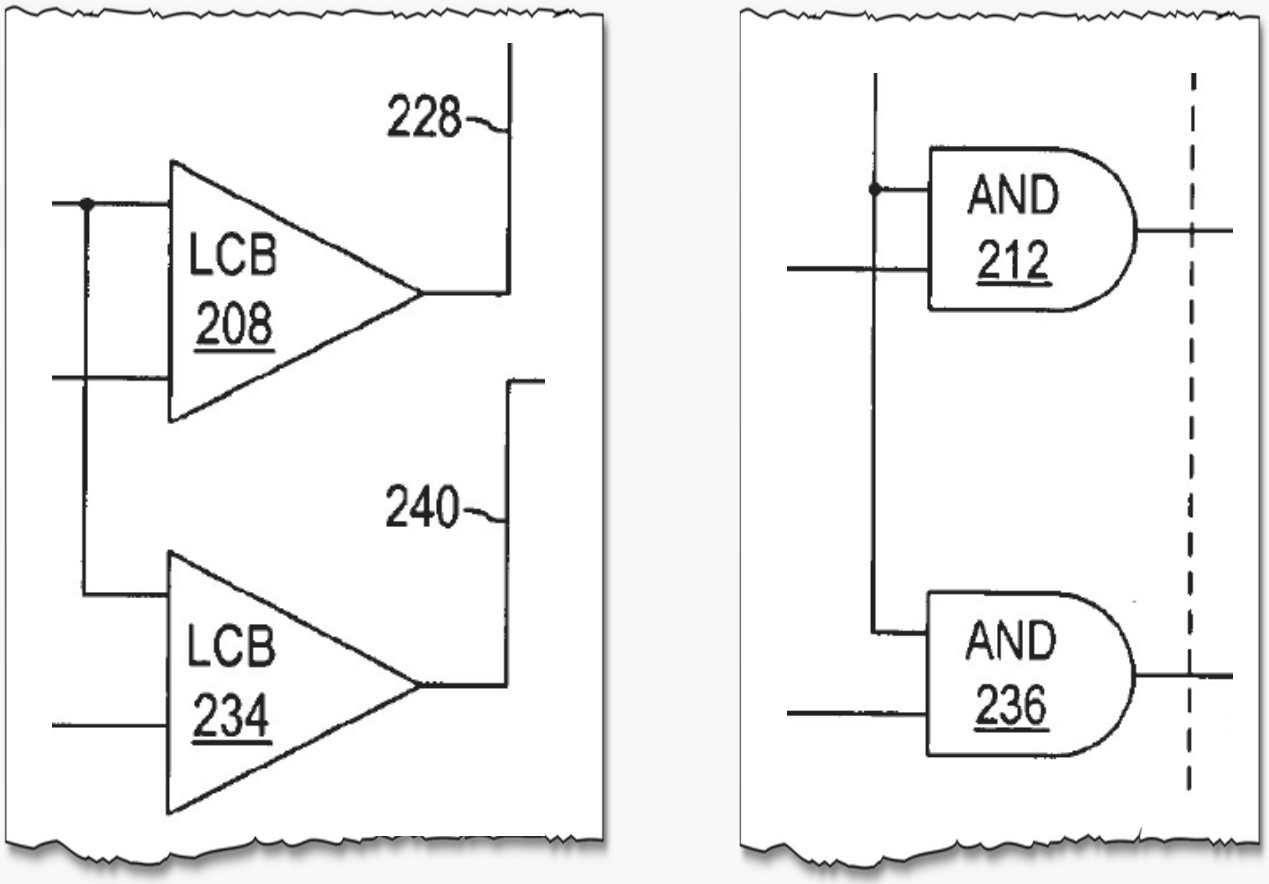
portions using distinct first and second logics, respectively. Petitioner cites to the predecoder 202 of Asano as meeting the "first logic" and "second logic" limitations of the claims (see Petition at 36), but the predecoder 202 is a single logic circuit that receives the entire memory address:



Ex. 2001 at ¶127

Asano and Itoh: Petitioner's Combination is Based on Impermissible Hindsight

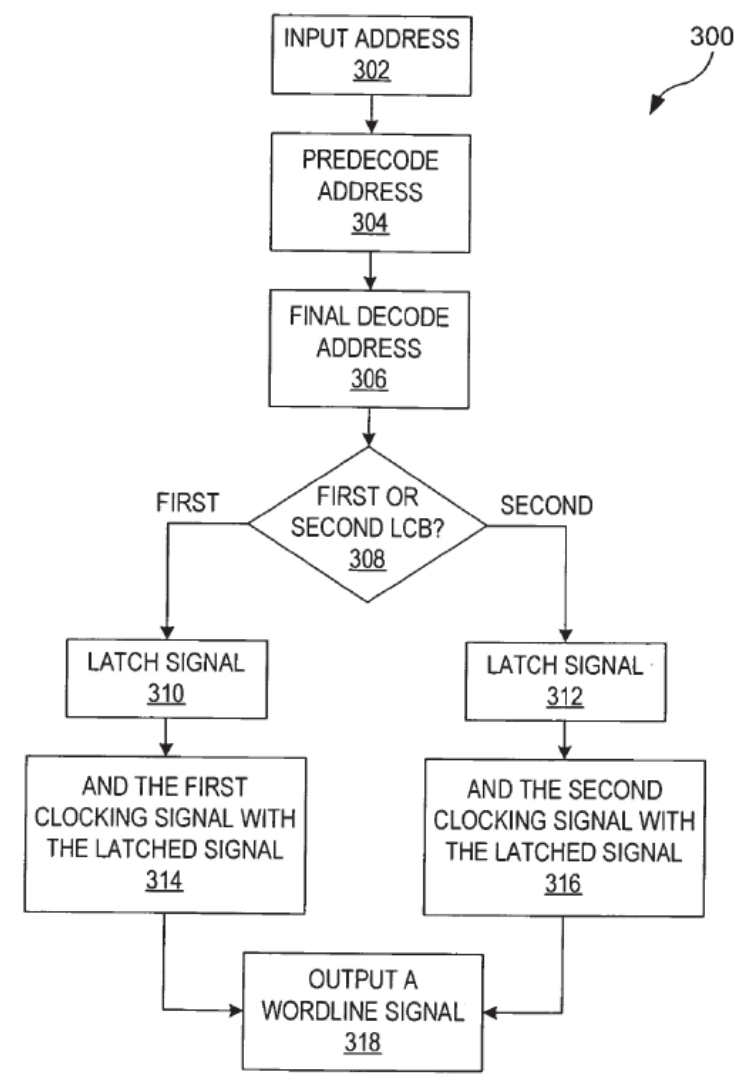
Asano:



Ex. 1006 at Fig. 2

Asano and Itoh: Petitioner's Combination is Based on Impermissible Hindsight

Asano:



Ex. 1006 at Fig. 3

Asano and Itoh: Petitioner's Combination is Based on Impermissible Hindsight

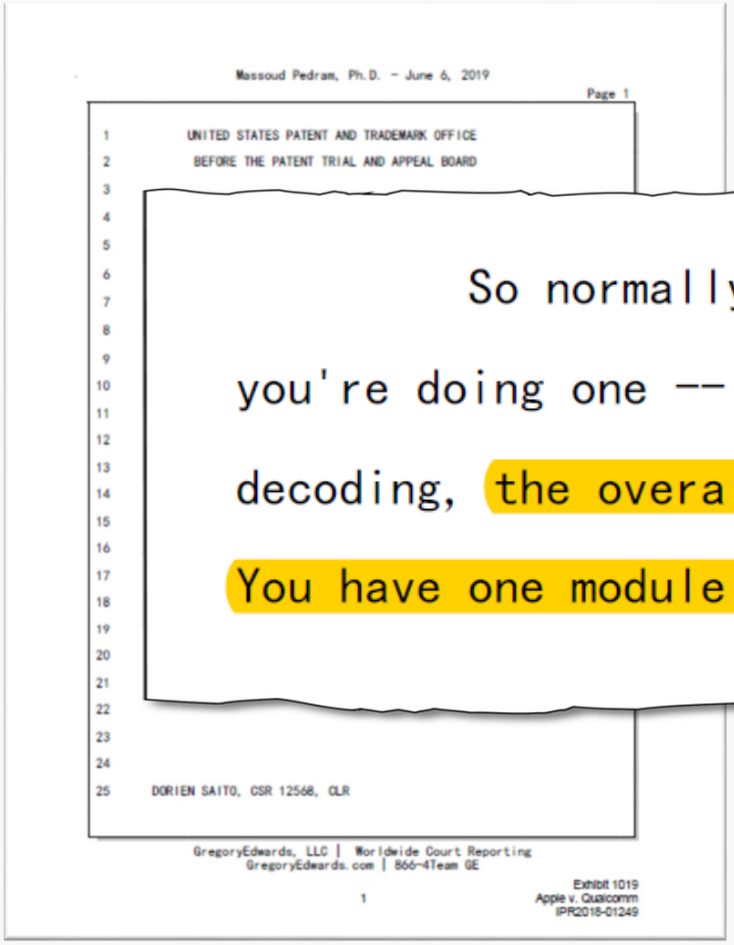
Petition:

¶¶121-122. Because Asano represents the predecoder 202 simply using a block element in a block diagram, a POSITA would have looked to Itoh's textbook circuits in determining how the internal structure of the predecoder 202 would be built as separate logic sections for decoding different portions of the 6-bit memory address. A POSITA designing Asano's memory circuit would have naturally

Paper 2 at 35

Asano and Itoh: Petitioner's Combination is Based on Impermissible Hindsight

Deposition of Dr. Massoud Pedram:



Massoud Pedram, Ph.D. - June 6, 2019

Page 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

So normally, I would consider this even, if you're doing one -- one shot decoding or multistage decoding, the overall module is just your decoder. You have one module doing decoding. Internal to

DORIEN SAITO, CSR 12568, CLR

GregoryEdwards, LLC | Worldwide Court Reporting
GregoryEdwards.com | 866-4Team GE

1

Exhibit 1019
Apple v. Qualcomm
IPR2018-01249

Ex. 1019 at 21:18-21

Patentability

I. SATO DOES NOT RENDER CLAIMS 1-28 AND 31-37 OBVIOUS

- The Petition Fails to Establish a *Prima Facie* Case of Obviousness
- Sato Does Not Teach or Suggest the Claimed "Clock Signal"
- Sato Does Not Teach or Suggest the Claimed "Clock Output"

II. ASANO AND ITOH DO NOT RENDER CLAIMS 1-17, 20-28, AND 31-36 OBVIOUS

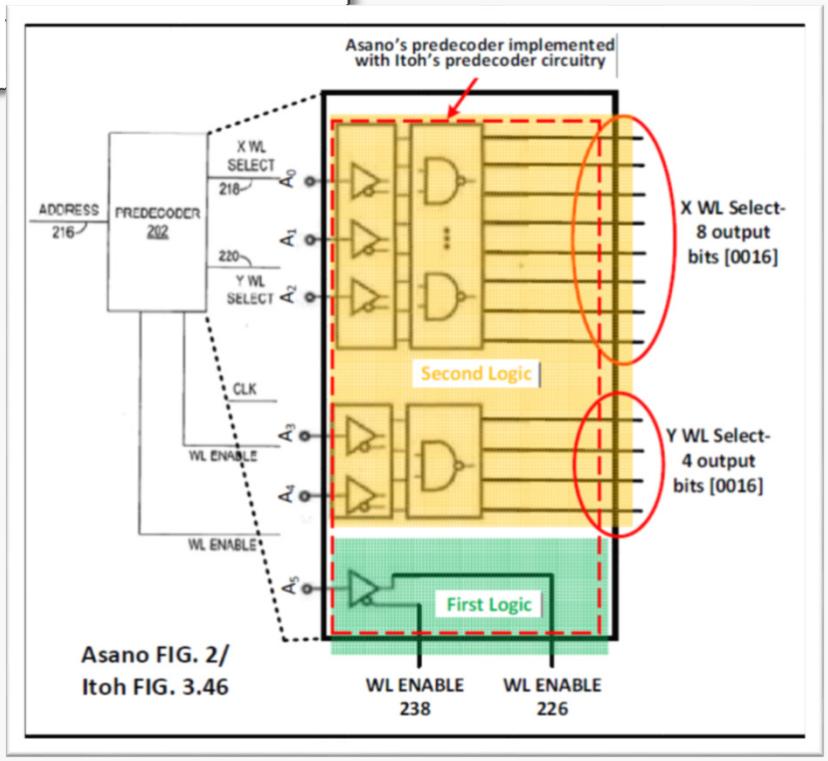
- Petitioner's Combination is Based on Impermissible Hindsight
- The Petition's Motivation to Combine Argument is Flawed

Asano and Itoh: The Petition's Motivation to Combine Argument is Flawed

Petition:

¶¶121-122. Because Asano represents the predecoder 202 simply using a block element in a block diagram, a POSITA would have looked to Itoh's textbook circuits in determining how the internal structure of the predecoder 202 would be built as separate logic sections for decoding different portions of the 6-bit memory address. A POSITA designing Asano's memory circuit

Paper 2 at 35



Asano FIG. 2/ Itoh FIG. 3.46

Paper 2 at 38

Asano and Itoh: The Petition's Motivation to Combine Argument is Flawed

Petition:

> Specifically, Itoh discloses well-known circuits that illustrate a possible implementation of the internal structure for the predecoder 202. APPLE-1003,

Paper 2 at 35

Deposition of Petitioner's declarant:

> Q. So there are other ways that it could be implemented, correct?
>
> MS. REICHEL: Objection to form.
>
> A. There are other ways, but those ways are equivalent and obvious.

Ex. 2005 at 52:14-18

Asano and Itoh: The Petition's Motivation to Combine Argument is Flawed

not done so, and its obviousness ground is therefore deficient. In fact, the Board routinely rejects obviousness arguments where, as here, a petitioner fails to provide a sufficient factual basis for its assertions. *See, e.g., Heart Failure Techs., LLC v. Cardiokinetix, Inc.*, IPR2013-00183, Paper 12 at 9 (PTAB July 31, 2013) ("Petitioner must show some *reason* why a person of ordinary skill in the art would have thought to combine *particular* available elements of knowledge, as evidenced by the prior art, to reason the claimed invention.") (emphasis in original).

Paper 11 at 54-55

Asano and Itoh: The Petition's Motivation to Combine Argument is Flawed

Petition:

> circuits in Figure 3.46. As an example, a POSITA could have implemented Asano's predecoder using a combination of the predecoder circuits disclosed by Itoh as shown in the annotated version of Asano's Figure 2 below.

Paper 2 at 37

> As discussed above, a POSITA would have understood that the "first logic" portion of Asano's predecoder could be implemented using known logic circuitry such as that disclosed by Itoh. Such circuitry would have been a 1:2 decoder that

Paper 2 at 42

"The issue is not whether a skilled artisan ***could*** [combine the references] or whether it would have been trivial to do so. The issue is whether a skilled artisan ***would have been motivated to do so*** based on teachings of the references ...." *TRW Automotive US LLC v. Magna Elecs., Inc.*, IPR2014-01355, Paper 21 at 15 (PTAB Nov. 19, 2015) (emphasis added).

Asano and Itoh: The Petition's Motivation to Combine Argument is Flawed

Petition:

> **[1]** Itoh illustrates the circuit design of several predecoder circuits … which a POSITA would have readily applied if seeking to implement Asano's predecoder 202.

Why?

> **[2]** Because Asano represents the predecoder 202 simply using a block element in a block diagram, a POSITA would have looked to Itoh's textbook circuits in determining how the internal structure of the predecoder 202 ….

Why?

> **[3]** A POSITA designing Asano's memory circuit would have naturally turned to a textbook such as Itoh's for details on memory design techniques for a predecoder.

Why?

> **[4]** The POSITA would have understood that Itoh's individual predecoder circuits would merely perform their intended functions when implemented in Asano's predecoder 202.

Why?

Paper 17 at 23-25 (quoting Paper 2 at 35)

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing Patent Owner's Demonstrative Exhibits was served on October 7, 2019 by email, as follows:

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