

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

Case IPR2018-01249
Patent 7,693,002 B2

Record of Oral Hearing
Held: October 10, 2019

Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and
SCOTT B. HOWARD, *Administrative Patent Judges*.

APPEARANCES:

ON BEHALF OF THE PETITIONER:

KEN HOOVER, ESQUIRE
W. KARL RENNER, ESQUIRE
TIMOTHY W. RIFFE, ESQUIRE
WHITNEY A. REICHEL, ESQUIRE
Fish & Richardson P.C.
1000 Maine Avenue, S.W.
Washington, D.C. 20024
202-626-6447

ON BEHALF OF THE PATENT OWNER:

DAVID B. COCHRAN, ESQUIRE
JOSHUA R. NIGHTINGALE, ESQUIRE
Jones Day
North Point
901 Lakeside Avenue
Cleveland, Ohio 44114-1190
216-586-7302

The above-entitled matter came on for hearing on Tuesday, October 10, 2019, commencing at 3:58 p.m., at the U.S. Patent and Trademark Office, 600 Dulany Street, Alexandria, Virginia.

P R O C E E D I N G S

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JUDGE JEFFERSON: Thank you. You can be seated we'll wait for the other judges to join us, although I think they can hear us.

JUDGE GALLIGAN: This is Judge Galligan in the Texas Regional Office. Can you hear me?

JUDGE JEFFERSON: Yes, I can.

JUDGE GALLIGAN: Great.

JUDGE HOWARD: And this is Judge Howard, can you hear me?

JUDGE JEFFERSON: Yes; yes, we can. You can proceed, Judge Galligan -- or, Judge Howard, I'm sorry.

JUDGE GALLIGAN: Great. Thank you. Good afternoon, I'm Administrative Patent Judge Galligan; and I'm joining from the Texas Regional Office as I said. Before you is Judge Jefferson; and on video is Judge Howard. This an IPR, an Inter Partes Review in IPR 2018-1249; U.S. Patent 7,693,002. Petitioner is Apple, and Qualcomm is the Patent Owner; and we issued an oral hearing in this case allocating 45 minutes of argument to each party; and now I'd like to ask Counsel for each side to come forth and make appearances at the podium and please make sure the green light is on, on the microphone. Petitioner, please, first.

MR. RENNER: Good afternoon, Your Honors. This is Karl Renner from Fish & Richardson; and I'm joined by several colleagues -- Tim Riffe, Ken Hoover, and Whitney Reichel on behalf of Apple.

JUDGE GALLIGAN: Great. And while I have you up there, how much rebuttal time would you like to reserve of your 45 minutes?

1 MR. RENNER: Thank you, Your Honor; we'll reserve 15 minutes.

2 JUDGE GALLIGAN: Okay; thank you.

3 MR. RENNER: Also we have printed demonstratives. May we
4 approach Judge Jefferson with them?

5 JUDGE GALLIGAN: Yes.

6 MR. RENNER: Thank you.

7 JUDGE GALLIGAN: Patent Owner?

8 MR. COCHRAN: Good afternoon. Dave Cochran from Jones Day
9 on behalf of the Patent Owner, Qualcomm. With me today is an associate
10 from Jones Day, Josh Nightingale. We also have our trial technician, Alan
11 Eaton; and with us in the audience we have Ron Zhang, Ken Vu, Steve
12 Worth, and Yi Tang who are representatives of Qualcomm.

13 JUDGE GALLIGAN: Thank you. And would you like to reserve
14 sur-rebuttal time?

15 MR. COCHRAN: Yeah; I'd like to reserve 10 minutes; and we also
16 have a set of demonstratives for Judge Jefferson if you'd like to receive
17 those.

18 JUDGE JEFFERSON: Thank you.

19 JUDGE GALLIGAN: Thank you, Counsel. Petitioner, you may
20 proceed first; after that Patent Owner may respond. Petitioner, you'll get
21 your 15 minutes of rebuttal time if you have that much left; and then Patent
22 Owner, you are entitled to your sur-rebuttal time. Because Judge Howard
23 and I are remote, please identify with particularity and for the purpose of the
24 record, the transcript, anything you cite -- for instance, the demonstratives
25 and the briefing. We have access to everything. Just please state the slide

1 number, or the page of the petition, or whatever you're looking at. And with
2 that, Petitioner, you may begin.

3 MR. HOOVER: Good afternoon, Your Honors. My name is Ken
4 Hoover; along with my colleagues Tim Riffe, Karl Renner, and Whitney
5 Reichel. We represent Petitioner, Apple.

6 Slide 2 -- Your Honors, during our presentation today, we plan to
7 focus our time on several distinct issues that have arisen during the briefings
8 in this IPR rather than repeating an element-by-element analysis of the
9 petition. I will be providing an overview of the '002 Patent itself, and
10 addressing issues 1 and 3; my colleague, Tim Riffe, will address issue 2.

11 Slide 3 - First, I'd like to provide a very brief overview of the '002
12 Patent. On slide 4, the focus of the '002 Patent is on a wordline driver
13 system for memory arrays; and in particular, figure 1 of the '002 Patent
14 provides the most high level illustration of the patent's content. The '002
15 Patent, itself, describes figure 1 as a block diagram of a particular illustrative
16 embodiment of a wordline driver system, including a plurality of groups of
17 wordline drivers associated with the memory array.

18 On slide 5, we see that Qualcomm's expert, Dr. Pedram explained
19 during his deposition that figure 1 is a functional block diagram and as such
20 a POSITA wouldn't understand such drawings to provide the artisan with a
21 functional illustration of a system; and is not intended to illustrate the
22 specific circuit implementation of that system.

23 Slide 6 - So we intend to begin with issue 1, with the Asano/Itoh
24 ground. We're beginning with what is the second ground from our petition
25 because it's the most straightforward one of the two grounds presented and

1 it's not dependent on the claim construction issue. Furthermore, this ground
2 addresses all but three of the challenged claims in the IPR.

3 Slide 7 - Slide 7 provides the text to claim 1 of the '002 Patent. Claim
4 1 of the '002 Patent is directed to a circuit device comprising separate first
5 and second logic. Among other things, the first logic decodes the first
6 portion of the memory and the second -- MAC memory address, excuse me -
7 - and the second logic decodes the second portion of the memory address.

8 Notably, however, Patent Owner does not argue that Asano and Itoh
9 do not teach the elements of the claims, instead they're arguing it boils down
10 to the idea that a POSITA would not be motivated to build a decoder using
11 textbook circuits.

12 Slide 8 - Shows figure 2 from Asano. Similar to the '002 Patent,
13 Asano discloses a wordline driver/address decoder system for a computer
14 memory. Also similar to figure 1 of the '002 Patent, Asano represents its
15 system as a functional block diagram. As we have seen, Dr. Pedram noted
16 that the POSITA would understand such a diagram to be intended to show
17 the function of system, not necessarily a circuit layout.

18 The point of dispute for this ground is about the overlapping green
19 and yellow lines on Asano's predecoder, 202, in this annotated figure.
20 However, as we'll demonstrate, within the predecoder both experts agree that
21 there is separate and distinct logic circuitry to produce separate and distinct
22 predecoder outputs.

23 In slide 9 -- And when you take a close look at Asano's figure, there's
24 a single address coming in to the predecoder; but the reference teaches that
25 this six-bit address is used to produce three separate and distinct outputs.

1 The circled outputs on the annotated diagram in the second logic, the x or
2 line select signal and the y or line select signal, and then separately the
3 wordline enable signals as part of the first logic.

4 In the interest of time, we're going to move to slide 12. In slide 12,
5 Dr. Horst analyzes -- actually, slide 12 provides a summary of Dr. Horst's
6 analysis of the text of Asano and his conclusion that of those six address
7 input bits, three of those bits are decoded to create the eight-bit x wordline
8 select signal; two of those bits are used to create the four-bit wordline select
9 signal; and one address bit is decoded to produce the two-bit wordline
10 enable signal -- that's per Asano.

11 So, the question becomes -- and I would like to mention that the slides
12 I skipped over provide a summary of Dr. Horst's analysis. So, the question
13 then at issue becomes how would a POSITA have implemented the structure
14 of the predecoder in Asano in order to produce these results. The evidence
15 shows that the experts agree that in implementing Asano's predecoder, the
16 POSITA would require separate logic circuits to decode each of these
17 separate output signals.

18 In slide 13 -- One reason we know that's the case is that's precisely
19 how Dr. Pedram, Qualcomm's expert, said that he would teach his students
20 to produce a similar set of outputs based on a similar grouping of bits.
21 Specifically, when asked, are you saying you would use one set of AND
22 gates to decode one bit; another set to decode two bits; and another to
23 decode three bits, Dr. Pedram agreed. He did, however, note that -- on slide
24 13 -- instead of using an AND gate to decode one bit -- he wouldn't use an

1 AND gate to decode one bit, but he would use -- that would be decoded
2 differently -- but he would use separate AND gates for the other sets of bits.

3 And then when we turn to slide 14, that's, precisely, what we see in
4 Asano's textbook. We see a figure that shows -- in the subfigure a -- one
5 input bit coming in to decode and produce two output bits. In subfigure b,
6 we see two address input bits coming in to decode four output bits; and in
7 subfigure c, we see three input address bits coming in to decode and produce
8 eight output bits. Hence, the artisan's motivation for looking to this textbook
9 is simply his or her desire to build Asano's predecoder circuit using standard
10 logic circuits. And what would this implementation look like? In slide 15,
11 Dr. Horst provided an annotated diagram where what we see here is in
12 green, we see separate first logic circuitry decoding one bit to produce the
13 wordline enable signals, and separate yellow, second logic circuitry to
14 decode the remaining five bits and produce the x, y select output signals.

15 Slide 16 - While the Patent Owner has characterized this motivation
16 for this ground as impermissible hindsight, as the petition explained and Dr.
17 Horst supported, the person of ordinary skill would have been motivated to
18 use Itoh's textbook logic circuits to build Asano's predecoder, which was
19 represented just by a functional element in a functional block diagram.
20 There's really nothing more here at issue than the use of old elements,
21 according to their known and intended function, to produce a predictable
22 result. Your Honors have any questions?

23 JUDGE GALLIGAN: Nothing from me; thank you.

24 MR. HOOVER: Then, I'll introduce Tim to discuss the claim
25 construction.

1 MR. RIFFE: Good afternoon, Your Honors -- Tim Riffe on behalf of
2 Apple, again. I'll be speaking with you for the next few minutes regarding
3 Patent Owner's construction of a clock signal and why that's improper. In
4 order to overcome the prior art of records -- some of which that you just
5 heard from Mr. Hoover on which is part of the record -- Qualcomm
6 proposes, effectively, to add a limitation to the claims being a narrowing
7 claim construction that we believe is improper.

8 Specifically, Qualcomm proposed adding a limitation to establish an
9 undisclosed characteristic of an inferentially claimed signal -- an input signal
10 to the '002 memory encoder circuit. There's no intrinsic evidence that
11 supports this narrowing construction. Instead the intrinsic evidence
12 confirms that the term is agnostic to either type of system. Prior art in the
13 same field will confirm this -- as we've shown in the record, and which I'll
14 go through with you briefly this afternoon. Qualcomm's only supporting
15 evidence is a single generic dictionary that's not of specific to this field and
16 an expert that didn't do the correct analysis.

17 Slide 18, please. Now the primary point of dispute, of course in
18 ground 1 of the Sato reference is the term clock signal that appears twice in
19 claim 1. In the context of claim 1 -- as I mentioned earlier -- this term is an
20 electronic input signal to the '002 Patent's wordline driver and address
21 decoder system. Nothing in claim 1 itself, or the written description,
22 indicates that the specific characteristics of this signal are critical to or even
23 change the function of the claimed circuit device. Indeed, as we can see
24 reproduced on slide 18, the term clock signal is, at best, inferentially claimed

1 as I mentioned earlier; and simply is the input to the wordline driver, the
2 address decoder.

3 As the record shows, the only alleged intrinsic evidence that supports
4 Patent Owner's narrow construction is the patent's use of the term clock
5 signal itself; and to support Patent Owner's contention, you must find that in
6 spite of the evidence to the contrary -- some of which we'll go over with you
7 this afternoon -- intrinsically, the term clock signal, itself, requires it to be
8 periodic because Patent Owner provides no additional support.

9 Slide 19, please. Here we show the competing constructions. Now,
10 Petitioner -- in our petition and as we stand here today -- believes that this
11 should get its plain and ordinary meaning. However, because Qualcomm
12 raised this as a claim construction issue we, of course, responded to that
13 proposed construction.

14 Now, the next slides I go over with Your Honors -- slides 20 and 21 --
15 support the notion that clock signal must be interpreted broad enough to
16 encompass certain types of clock signals -- and those are modified clock
17 signals; and those are termed conditional clock signals in the art -- we'll see
18 some examples of those, and there are examples of those in the '002 Patent --
19 and gated clock signals. And these particular types of clock signals are
20 actually claimed in the '002 Patent; and as the record shows Patent Owner's
21 construction reads out these particular claim signals. So, let's take a look at
22 some of the examples of why that is.

23 Slide 20 -- In fact Patent Owner's own expert, Dr. Pedram, admitted
24 during his deposition that the conditional clock signals, which are shown as
25 124 through 130, in figure 1 of the '002 Patent, those are outputs of the '002

1 Patent's conditional clock generator, 110 -- as we see in figure 1. Dr.
2 Pedram admitted during his deposition that those would not meet Patent
3 Owner's construction of the term. But why is that? Because Dr. Pedram
4 explicitly stated that the Patent Owner's claim construction requires "always
5 running, continuously running" periodic signal being applied to the address
6 decoder or what's claimed as the first logic.

7 Dr. Pedram's acknowledgement about the scope of the Patent Owner's
8 claim construction even reads dependent claims -- such as claims 5 and 7 --
9 outside the scope of this construction because under Patent Owner's
10 construction the conditional clock outputs of claim 5 would no longer
11 conform to the scope the applied clock signal of claim 1 under Dr. Pedram's
12 reading of the claims; hence, reading the narrowing dependent claim outside
13 of the scope of the claims from which it depends.

14 Now, in Patent Owner's sur-reply they tried to take us to task for this;
15 and they make an argument that a person of skill in the art would understand
16 that in the '002 Patent, all of the clock outputs are not carrying a clock signal
17 at all times -- and the clock signals we're referring to again here are signals
18 124 through 130 -- those are the conditional clock signals, if you will -- and,
19 therefore, Patent Owner says that the fact that the Patent Owner's
20 construction of clock signal does not encompass the fixed voltage levels of
21 the non-selected clock outputs is consistent with the intrinsic evidence.
22 That's simply not the case.

23 As Qualcomm's own expert, Dr. Pedram testified, as shown on slide
24 20 -- the expert that we have -- he testified that none of the signals -- 124,
25 126, 128, and 130 -- meet Qualcomm's definition. So, despite the fact -- we

1 don't disagree with them that these clock signals that are output from the
2 conditional clock generator -- there may be times where if one is output, the
3 others have fixed voltage on the output -- that's okay; we agree with them on
4 that. What Dr. Pedram says is when you have one of these conditionally
5 generated clock signals, they will not meet the definition of Patent Owner's
6 proposed construction because of that periodic signal.

7 Slide 21 - The Petitioner's reply brief presented several of Dr.
8 Pedram's own publications that refer to clock signals that can be stopped
9 when not in use. In other words, non-periodic clock signals -- as gated
10 clocks -- again, the term that we're using here in view of the '002 Patent's
11 clock signals.

12 The Patent Owner acknowledged in its sur-reply that these gated
13 clocks are different from a clock signal; and Petitioner agrees. The gated
14 clocks represent a subset of clock signals that are not always running; and as
15 Dr. Pedram told us such gated clock signals do not meet Patent Owner's
16 construction. So, here again, their construction of clock signals, unduly
17 restrictive, even though its own expert referred to gated clock signals as
18 clock signals in certain of his publications.

19 The broader term clock signal should be construed to encompass the
20 subsets. Why is that? Otherwise, as noted, the gated or conditional clock
21 outputs, as claimed in the dependent claims, are read outside of the scope of
22 the claims themselves, and that cannot stand. This is especially true where
23 neither the claims themselves, nor the intrinsic record provides such
24 limitations on the claim term.

1 Now let's look at slide 22 because this is interesting. Qualcomm
2 provided a definition from the *IEEE Dictionary* that indicates that the term
3 timing signal used by Sato is synonymous with clock signal of the '002
4 Patent. Indeed, let's talk about that. As we can see on the slide 22,
5 Qualcomm's *IEEE Dictionary*, specifically, says that clock signal is
6 synonymous with clock pulse and timing pulse. So, therefore, we have a
7 relationship between clock signal, clock pulse, timing pulse. What is the
8 rational deduction from that relationship. Is that clock signal synonymous
9 with clock pulse; clock pulse is synonymous with timing pulse; and,
10 therefore, clock signal is synonymous with timing signal -- drawing from
11 deductive reasoning from their own definition.

12 We've talked about how clock signals is not limited to the periodic
13 signal by virtue of the intrinsic record now; Dr. Pedram's publications, and
14 additional intrinsic evidence; now, we'd like to discuss how some non-
15 periodic signals of the prior art are actually referred to as clock signals in
16 those prior art references such that a person of skill in the art coming to look
17 at the '002 Patent would understand that a clock signal is not limited to the
18 restrictive periodic clock signal that Qualcomm would have you believe it is.

19 Let's go look at slide 24. Slide 24, we're looking at the Hayakawa
20 reference that we cited to in our Petitioner's briefs. The Hayakawa reference
21 provides an example of a prior art reference that refers to a non-periodic
22 signal as a clock signal. Specifically, Hayakawa states that its clock signal
23 ϕ_s is generated in response to an address transition detect signal. Now,
24 Petitioner's expert, Dr. Horst, explained in his second declaration that this
25 means that Hayakawa's clock signal is triggered based on changes to an

1 address signal applied to Hayakawa's static RAM. Consequently, the
2 generated clock signal follows the pattern of address changes, and would
3 generally not be periodic.

4 Slide 25 -- This is similar to what Dr. Pedram -- again, Qualcomm's
5 expert -- said in his declaration with respect to Sato's timing signal because
6 it too follows memory access patterns that he characterizes as "highly
7 irregular." The point being here is that Dr. Pedram's own analysis supports
8 Dr. Horst's opinion that Hayakawa's clock signal would, in fact, be non-
9 periodic -- which is what Hayakawa refers to as the clock signal.

10 Let's go to Slide 26. Now, looking at their supposed intrinsic
11 evidence. Dr. Pedram acknowledged that the '002 Patent -- during his
12 deposition -- does not contain a specific definition of clock signal. He was
13 specifically asked on slide -- and we've reproduced this on slide 26 -- the
14 question was, is there any place in the specification of the '002 Patent where
15 you believe the inventors have set forth a particular definition of the term
16 clock signal? Dr. Pedram responded to that by saying "I've not seen in the
17 '002 Patent a precise definition of the clock." And there he was referring
18 specifically to the question being asked about clock signal.

19 Now, the record shows, as we've developed in our briefing, that the
20 '002 Patent also does not contain any references to asynchronous vs.
21 synchronous systems; any references to the period characteristics of the
22 clock signal, e.g., it's frequency, it's period -- some of those other types of
23 characteristics; and there's no disclosure of timing control circuitry for either
24 synchronous or asynchronous systems, such as those of the Itoh reference --

1 which you'll hear about -- that Qualcomm points to as support for its
2 construction.

3 So, ultimately, a POSITA would have understood that the focus of the
4 '002 Patent is not on a particular type of clock signal. That's an inferentially
5 claimed input into what is claimed, which is the generic wordline driver
6 system that's agnostic to the implementation in particular types of memory
7 systems.

8 Slide 27, please. So, Patent Owner's intrinsic -- alleged intrinsic
9 evidence -- of the periodic clock signal is merely that the '002 Patent does
10 not disclose an asynchronous memory system. Patent Owner's support of
11 this notion is in paragraph 54 of Dr. Pedram's declaration which merely
12 parrots the same statement. But, in fact, the '002 doesn't describe the
13 synchronous system either. To be fair, the Patent Owner's response cites to
14 several other paragraphs -- and, specifically, 54 through 69 of Dr. Pedram's
15 declaration. But if you look at those paragraphs -- and I would ask the
16 Board to please do so before the final written decision -- you will note that
17 the '002 Patent is not once cited in those paragraphs of Dr. Pedram's
18 analysis. So, in essence, the Patent Owner's only intrinsic evidence for
19 interpreting clock signal, as narrowly as they would have you do it, is the
20 term itself and nothing more. Any questions, Your Honor?

21 JUDGE JEFFERSON: I don't have any; thanks.

22 MR. RIFFE: Thank you. I'll turn it back over to Mr. Hoover.

23 MR. HOOVER: Thank you, Tim. We're on slide 31, and our last
24 issue is whether Sato renders obvious the '002 Patent claims. Initially, I
25 would like to note that the Board adopts Apple's claim construction, there is

1 actually no dispute that Sato invalidates the claims of the '002 Patent. What
2 I would like to address in the next few minutes, however, is -- time
3 permitting -- is first that the Patent Owner's erroneous and irrelevant
4 argument that Sato is somehow fundamentally different from the '002
5 Patent; but, in fact, they are nearly identical in function and structure. Then
6 after that -- time permitting -- I'll discuss how the evidence shows that Sato
7 renders the claims obvious even under Patent Owner's narrow construction
8 of a mere input signal to the '002 Patent -- the '002 Patent wordline drivers.
9 And, finally -- time permitting -- I'll address a few arguments that the Patent
10 Owner had about the clock outputs in Sato's predecoder.

11 Slide 32, claim 1 -- So, just to be clear, there are no specific transistor
12 configurations required by the claims; but just to give you a sense for how
13 flawed Patent Owner's argument that Sato is somehow fundamentally
14 different than the '002 Patent, I'll briefly describe for you how even the
15 specific embodiments of both patents operate nearly identically and have
16 similar structure. I'll also describe for you how the evidence shows that even
17 the disputed clock signal or timing signal serve a similar function in the
18 particular embodiments of each system and, consequently, that the Patent
19 Owner's attempt to introduce undisclosed characteristics of a clock signal
20 into the claim is a last ditch effort to save the patent.

21 Slide 33 -- By way of reintroducing the Board to Sato, slide 33
22 provides a color-coded comparison from the petition between the particular
23 embodiments of Sato's figure 3 and the '002 Patent's figure 1. And again,
24 the claims do not recite the wordline driver system -- the '002 Patent

1 wordline driver system -- at this level of particularity. This is an exemplary
2 -- this is for example, to show just how similar the two are.

3 On slide 34, shows a closer comparison of the first logic of each
4 embodiment of the respective systems. Here we can see that in green, the
5 first logic of each system receives a portion of a memory address, in purple.
6 It receives a synchronization signal -- timing signal or a clock signal,
7 respectively -- in blue; and it provides four red output signals based on those
8 input signals. The output signals are each connected to particular wordline
9 driver circuitry in each system, in yellow.

10 Slide 35 - Illustrates claim 1 with the same color-coded mapping of
11 the individual elements from those particular embodiments of each to the
12 language of the claims. This is provided for the Board's reference.

13 Slide 36 -- This slide illustrates -- I'm not going to go through this
14 chart in detail; that would be very tedious -- but this provides Dr. Horst's
15 chart explaining his detailed transistor-by-transistor analysis of the two
16 patents -- the embodiments of the two patents -- to show the near identical
17 operations of their respective embodiments and their near-identical usage of
18 the clock/timing signals. The chart's reproduced for your convenience.

19 But in the next three slides what I do plan to do is summarize Dr.
20 Horst's analysis graphically. Again, showing that even the particular
21 embodiments in each patent apply the synchronization -- respectively,
22 clock/timing signals -- identically at the transistor level or line activation
23 circuitry; and, hence, Patent Owner's characterization of Sato as
24 fundamentally different is just wrong.

1 Slide 37 -- This slide shows at steady state -- prior to wordline
2 activation -- shows the signals that are applied to the wordline driver
3 transistors in each system prior to the wordline activation.

4 In slide 38, the clock signals are activated. The clock output's in red
5 of the first logic; and the second logic selection signal, in orange, are applied
6 to identical transistors, indicated in purple and blue, in an identical manner.
7 These are even the same types of transistors.

8 On slide 39, the wordline is activated. Both Sato's and the '002
9 Patent's wordline drivers, in yellow, are activated by the orange selection
10 signal from the second logic, as the red clock output is used to operate the
11 identical transistors indicated in slide 38.

12 In slide 40, we have provided a summary for your reference that
13 shows the complete mapping between the embodiments of each of the two
14 systems; and this image is also provided, annotated, in our petition.

15 Slide 41 -- Slide 41 now takes the claim -- and we highlight the
16 operations that we just described. Again in red, is highlighted the claim
17 language that relates to the application of the red clock outputs; and in
18 orange, it's highlighted the operations that pertain to the orange second logic
19 system as they're applied to the wordline circuitry.

20 Again, the claims don't require this transistor-to-transistor level of
21 detail that we just walked through, but from that discussion, it's clear that
22 Sato functions fundamentally the same as the '002 Patent. Thus, these more
23 general claim languages -- a lot more general claim language is met. Are
24 there any questions on that analysis?

1 On slide 42 -- Next we show Your Honors -- even if Your Honor is
2 determined that Apple is wrong on the claim construction; and that the term
3 clock signal, as used in the '002 Patent, requires continuous, unceasing
4 periodic clock signals, as Dr. Pedram's described, Sato expressly teaches that
5 his wordline driver -- the x-address decoder -- can be applied in clocked
6 static address decoders. Although disputed by the Patent Owner as mere
7 opinion of Sato's invention, this disclosure by Sato falls squarely within the
8 teaching-suggestion-motivation test for obviousness. The reference, itself,
9 suggest an obvious motivation to its disclosed invention.

10 Indeed, if simply the use of the term clock signal in the '002 Patent is
11 sufficient to prove it's limited to synchronous systems and, therefore,
12 periodic -- as Tim explained -- surely, Sato's reference to a clock, clocked
13 address decoder, provide similar evidence to support its suggested use in
14 synchronous systems with a periodic clock input to its address decoder.

15 And on slide 43, the experts agree that if the person of ordinary skill
16 at the time would have had the knowledge and ability to build a clock
17 generator, for either the Sato or the '002 Patent -- Dr. Pedram testified as to
18 the undisclosed clock generation circuitry in the '002 Patent -- that yes, a
19 person of ordinary skill would have been able to use known components and
20 build one.

21 And in the interest of time -- so, in slide 45 -- basically, the Patent
22 Owner -- and I would like to touch really briefly -- the Patent Owner has
23 suggested that Sato's predecoder doesn't directly apply that same timing
24 signal to its outputs and the input; and that somehow that means that Sato
25 fails to disclose the outputs, the claimed clock outputs. However, Dr. Horst

1 provided nine paragraphs of analysis of how Sato's description of the
2 operation would be understood by a POSITA.

3 Instead, Patent Owner provides an argument that's form over
4 substance -- they argue semantics rather than substance. With that I'd like to
5 preserve the remainder of my time for rebuttal. Thank you.

6 JUDGE GALLIGAN: Thanks. You have about 16 minutes left.
7 Whenever you're ready, Patent Owner. Thanks.

8 MR. COCHRAN: Yeah; turning first to slide 2 of our demonstrative
9 presentation, this is a figure showing figure 1 of the '002 Patent. I want to
10 go back and say a few comments about that before I dive into the two
11 grounds. The '002 Patent describes a dynamic wordline driver system for
12 selectively activating a wordline in a group of wordline drivers in a
13 synchronous memory system.

14 Slide 3 -- I've blown up here the bottom part of the figure 1 to focus
15 on the critical part of the claimed invention -- and the concept here in the
16 '002 Patent is that instead of having a single decoder for the wordline, you
17 purposely split the memory address up into two portions -- two distinct
18 portions -- and you decode those portions separately in a parallel. That is a
19 critical part of what's claimed; that's a critical part of the invention.

20 And as we'll see -- I mean I'll turn first to the Asano/Itoh grounds
21 because the Petitioner's Counsel dealt with that ground first; so, I'll turn to
22 that one first as well -- but as we'll see that the Asano/Itoh ground lacks both
23 of those critical features. In the Asano/Itoh ground, there is a single
24 decoding; there is not a first and second portion of the address. And so,

1 that's going to be an important thing to remember when we turn to that
2 ground.

3 Still focused on figure 1, we see that in addition to the address being
4 split into two portions, there's a clock input -- and we'll talk about what that
5 means in the context of the '002 Patent -- feeding into this circuit that's
6 called the conditional clock generator. And as we discussed earlier, that
7 conditional clock generator selectively applies the clock signal to one of the
8 outputs.

9 Now, what's important is that the invention in the '002 Patent is
10 specifically directed to dealing with the problems of a synchronous memory
11 system that has a periodic clock signal. The periodic clock signal in a
12 synchronous memory system -- because it's constantly activating the
13 wordlines; activating the rest of the circuitry in the system -- is a power
14 draw.

15 And if we turn to slide 16, Allen. This is from the summary of the
16 invention section of the '002 Patent where it specifically talks about the
17 problems associated with clocking in this kind of system where you have
18 capacitive loading in the clock system and you have problems with power
19 consumption. So, this is a real part of the '002 invention.

20 Back to slide number 3, Allen. So, they're essentially two critical
21 advantages of this technique. One is the parallel decoding of the addresses;
22 and the other is the reduced clock loading, and reduced power consumption
23 that occurs because the clock signal is only applied to one of the wordline
24 drivers at a time -- only one of the clock outputs. And, again, we'll see that
25 in the prior art -- particularly the Asano/Itoh combination -- this is not met.

1 Slide 6 -- I'm sorry, 4. So, claim 1 of the '002 Patent, which is what
2 we're talking about here today -- and you can see that it specifically has two
3 separate logics. There's a first logic and a second logic; and you have a first
4 portion of the memory address; and you have a second portion of the
5 memory address. So, this maps exactly with figure 1. And you'll also notice
6 that in the first logic, in addition to receiving the first portion of the memory
7 address, you also receive the clock signal; and the clock signal is then
8 selectively applied to one of the clock outputs -- and that's referring to the
9 conditional clock generator that we just saw a minute ago.

10 42 -- Now, I'm going to jump to the Asano/Itoh ground. So, the
11 ground is an obviousness combination of the Asano patent -- which is
12 approximately one-page of text -- in combination with the Itoh textbook --
13 which is a 500-page textbook on memory system design. It's important to
14 remember that Asano is the base reference here for their obviousness
15 combination; and you can see in the diagram of Asano that all of the address
16 bits -- labeled 216 -- are provided to his predecoder circuit, 202. There is
17 not a first and second portion; there is not a first and second separate
18 decoding logic in the Asano reference.

19 46 --

20 JUDGE GALLIGAN: Except the disclosure of Asano says that you
21 split the address in the component portions in paragraph 16, correct?

22 MR. COCHRAN: Paragraph 16 -- which we'll get to -- talks about
23 the outputs of the decoder, right; the output there. The outputs of the
24 decoder -- there are separate outputs -- but the address bits are all decoded
25 by the one circuit, 202.

1 On 46 -- this is figure 3 of the Asano reference -- and you can see that
2 the input address, 302, is provided to the block, 304; and there's no splitting
3 of the address into two portions. There's just one portion of the input
4 address; and it is decoded in block 304.

5 Go back to 43. Now, what Petitioner does with respect to Asano is
6 they need to have the first and second logic; they need to somehow find the
7 first and second portion. And so, what they do is in the petition, they draw
8 this green box around part of the predecoder and then some other circuitry --
9 there is a clock input, and they call that the first logic; and then they draw
10 this yellow box around the other part of the predecoder and the final
11 decoder, and they say well, that's the second logic.

12 47 -- But they concede in the petition that the predecoder is simply a
13 block element. We don't know exactly what circuitry is in the predecoder;
14 and there is no disclosure at all on the internal circuitry of that element, 202.
15 The petition concedes that this is just a block diagram. So, there's simply no
16 teaching or suggestion in the Asano reference that the predecoder has first
17 logic and second logic.

18 Can you pull up Petitioner's slide 9? In slide 9, the Petitioner refers to
19 paragraph 16 -- that Judge Galligan, you just referred to -- and as I
20 mentioned at the beginning, the entire Asano reference is about one page;
21 and there's only one paragraph that really presents any detail whatsoever
22 with respect to the critical thing here, which is the predecoder. And, yes,
23 this is in paragraph 16 -- it does talk about the separate outputs -- the x-
24 wordline select; y-wordline select; and the WL enable signal coming out of
25 the bottom of the predecoder; but you can see from this paragraph in the

1 highlighted portion the Petitioner has highlighted, it says from those six bits
2 the predecoder derives all of those signals; and those six bits are the input
3 bits. So, again, from those six bits, all of these signals are generated. This
4 does not suggest, as they have suggested in their slide, that there are three
5 separate portions that are then used to generate the three distinct output
6 signals. That's not what it says; it's the opposite of that. It says off of all of
7 these six bits that are coming in are used to generate the output signals. So,
8 if anything, this suggests that there is a single predecoder circuit that is
9 receiving all of these six bits, and is generating the various output signals.

10 JUDGE GALLIGAN: As I understand the Petitioner's contentions,
11 that's the entire reason they brought in Itoh because it shows you -- Asano
12 shows you what the function is and Itoh supplies what is -- it seems to be
13 nothing more than common knowledge in the art as to how you decode
14 addresses. We're talking about a person of skill in the art with a bachelor's
15 degree in electrical engineering, and three years of experience in memory
16 systems and circuits here.

17 MR. COCHRAN: Right; but the only way you would even get -- and
18 I'll get to Itoh in a minute and why you wouldn't go to those specific circuits
19 that they picked out of the textbook -- but the only way you would ever get
20 to Itoh is if there were some suggestion in Asano to break the address up into
21 different portions and decode those things separately. That's not what this
22 says. This says from those six bits generate all of the signals. This is
23 suggesting one circuit generating all of those signals, not separate circuits as
24 they're suggesting you would find in Itoh. So, this is not --

1 JUDGE HOWARD: Doesn't the Supreme Court, though, in KSR, say
2 you don't need a suggestion in the prior art reference? So, we don't need a
3 suggestion in Asano in order to go to Itoh.

4 MR. COCHRAN: I don't think that's exactly what they said. You
5 have to have some -- to go through -- the key -- remember, back to the
6 claim, we have first and second logic; first and second portion of address
7 decoding; and to go from that claim -- this is their primary reference -- the
8 primary reference tells you use one decoder; and that's exactly what this
9 paragraph 16 says -- from those six bits generate all of these signals. So,
10 how do you go from a reference that has one decoder and decide that well,
11 I'm going to do this separately and generate first and second portion using
12 first and second logic. I would suggest the only way you would come to that
13 conclusion is if you read the '002 Patent. And, in addition, they haven't
14 provided any reason other than well, it's in a textbook; so, it's common
15 knowledge; and the person of skill in the art would go into this 500-page
16 textbook and find these, you know, find these circuits; but there's nothing in
17 either Asano -- or certainly, the textbook -- that would lead you to that
18 conclusion.

19 JUDGE GALLIGAN: Let's go back to paragraph 16 here because I
20 think your argument is that there's nothing in there that would suggest this
21 first and second logic, the splitting the different logic to decode an address,
22 correct?

23 MR. COCHRAN: Correct; yes. Correct.

24 JUDGE GALLIGAN: So, we have six bits coming in and that the
25 expressed disclosure of Asano says an x -- you know, you got a wordline

1 enable signal, which it shows going in and being combined with the clock;
2 and you get a x-wordline select and y-wordline select. The x is eight bits
3 long, and the y is four bits long, so -- I mean 2^3 is 8; 2^2 is 4 -- that's five bits;
4 and the wordline enable bit's 1 -- why isn't that telling -- that's just screaming
5 to the person of skill in the art that's what it is -- it's breaking up the address.
6 I guess I'm not following.

7 MR. COCHRAN: Well, I don't think --

8 JUDGE GALLIGAN: I didn't tell you to do it; I mean that's the
9 express disclosure is to tell you to break up the address.

10 MR. COCHRAN: I don't think that's what it says. I think it just as
11 easily could be read that you would do this with one circuit like a
12 programmable logic array or a single decoding circuit. This portion of
13 Asano is telling you to take these six bits and generate these three signals;
14 but it's not telling you at all how to do that. So, I don't think --

15 JUDGE HOWARD: And I think that's why it doesn't tell you how to
16 do it or a reason why you would turn somewhere else to say let's go and find
17 the circuitry to go and figure out how to implement it?

18 MR. COCHRAN: Well, let's take a look at that -- we'll have to have
19 you do it -- turn to our 50. So, Asano doesn't -- we agree that Asano doesn't
20 provide any specific disclosure as to what is in the predecoder; and so, even
21 though it would have to have first logic and second logic, and first portion
22 and second portion in order to meet the language of the claims -- so, the
23 primary reference does not have that, and that point is conceded. So, then
24 we go to the Itoh textbook; and this is their -- on the bottom right-hand side -
25 - this is their figure combining Asano figure 2 and Itoh's figure 3.46.

1 Can you pull up their 14? So, this is the picture of the Itoh reference
2 3.46; and here are the three circuits; and you can see the first circuit is not a
3 predecoder; and the second and the third circuits have some predecoding
4 function.

5 You can go back to our 50. Then you can see here in slide 50 what
6 they've done is they haven't taken all of figure 3.46 from Asano; they've only
7 taken some of it; and they have then put it into this block which they
8 concede is just a block element; but yet they didn't pull in all the circuitry;
9 and there's no explanation as to why they only pulled this part and not all of
10 the circuitry. And I would also point out that the green block down here at
11 the bottom, labeled first logic, when we were looking at the 3.46 of Itoh,
12 that's not even the predecoder circuit; that's just an inverter circuit. So, it's
13 not clear why the person of skill in the art with the limited teaching of Asano
14 would end up going to this one page in this 500-page textbook and would
15 find parts of these circuits, not all of them; and then would use a circuit that's
16 not even labeled a predecoder, and suggest that this combination would be
17 obvious to the person of ordinary skill in the art.

18 JUDGE JEFFERSON: Counsel, are you claiming that it's beyond the
19 knowledge of a person of ordinary skill in the art to be able to turn to a
20 textbook, a core textbook in the field, and apply it to Asano?

21 MR. COCHRAN: No; but that gets us to the next point, which is the
22 motivation to combine. And if you turn to 53. In the petition, the Petitioner
23 repeatedly said that well, somebody could have done it this way; and that's
24 right -- somebody could have. Somebody could have cherry picked these
25 things out of the textbook and created this circuit that they have put into the

1 petition; but that's not the issue. The issue is given the limited teaching of
2 Asano, what would have caused somebody to go find these particular pages,
3 use some of the circuitry but not all of it, and stick it into his block diagram?
4 And when we called them on this, they repeatedly said he could have done
5 this, or he could have done that.

6 Next slide, 54 -- we said that's not good enough; and in response to
7 that, they came back in the reply brief and they cited to several sections
8 where they said well, he would have done it. But there's no explanation as
9 to why he would have done it other than well, it's a textbook and somebody
10 would have gone and looked in this textbook to find these circuits. Even
11 though, again, there's no teaching in Asano that you would break up the
12 address into multiple parts and have different decoding logic circuits.

13 JUDGE GALLIGAN: And just going back to that again -- I'm still
14 having trouble understanding your argument there. Why is paragraph 16 of
15 Asano not telling you to break up the address into the parts?

16 MR. COCHRAN: Because it's just telling you what the outputs are;
17 it's not telling you anything about the inputs. In fact, that there's one
18 sentence that we focused on is suggesting that you would use all of the
19 inputs to generate the outputs; and you just don't know from this --

20 JUDGE GALLIGAN: You do. Yeah, I mean you use six bits of input
21 to get, you know, eventually, what would select one of 64 -- because 2 to the
22 6th is 64, right?

23 MR. COCHRAN: Right. The lead from that one paragraph is how do
24 you do it; and it doesn't tell you how to do it. It doesn't tell you that you
25 have different logic circuits in the predecoder. (Inaudible).

1 JUDGE JEFFERSON: But, Counsel, I thought we agreed it was
2 within the knowledge of a person with skill in the art to apply the logic -- the
3 knowledge that's in Itoh -- and apply it to Asano. So, I mean are we back to
4 it's beyond the level of skill in the art?

5 MR. COCHRAN: No, I'm not suggesting that. I said that somebody
6 could -- I mean you could do a lot of things. The question is whether, given
7 the teaching of Asano, you would be motivated to even go and look for
8 multiple decoding circuits; and I would suggest that given that limited
9 teaching that you would not.

10 JUDGE JEFFERSON: So, it's the limit of teaching in paragraph 16 of
11 Asano that would thwart, or leave a person of ordinary skill in the art
12 stymied into knowing exactly what to go to, to fill in the block.

13 MR. COCHRAN: Correct.

14 JUDGE JEFFERSON: It tells you how to go from six bits of input to,
15 I believe, a wordline and two different outputs, circuit outputs?

16 MR. COCHRAN: Given the limited teaching of Asano -- that's our
17 position -- there would be no motivation to go look for multiple decoding
18 circuits.

19 I'd like to turn to the other ground in the time that I have, which is the
20 Sato ground. Go to slide 6.

21 So, there's three issues I'm going to try and squeeze in on the Sato
22 ground. Issue 1 is whether they have properly made it a *prima facie* case of
23 obviousness; and then I'm going to talk about the clock signal and the clock
24 output. So, if you could turn to slide 8.

1 So, they present the ground in Sato is a single reference obviousness
2 ground, which you can do -- and this is from their petition. You know, the
3 claim can be rendered unpatentable by a single reference; but the POSITA
4 has to be motivated to modify that reference in an obvious way. The
5 requirement here presumes that there's some difference between the prior art
6 and the invention. Otherwise, the reference would be anticipatory. But as
7 we'll see, when the Petitioner presented this ground, they established it as an
8 obviousness ground, but they're really presenting it as if it's anticipation.
9 They don't identify any differences between the prior art Sato reference and
10 the claims. Slide 9.

11 JUDGE GALLIGAN: I thought in the --

12 JUDGE HOWARD: Is it your contention that there aren't any
13 differences between Sato and the claim?

14 MR. COCHRAN: No. Our contention is there are differences. But
15 the point I'm trying to make here is that by presenting Sato as an
16 obviousness ground, they should have pointed out some difference between
17 Sato and the claimed invention so that they could then come up with some
18 reason to modify that reference in an obvious way. This is required by the
19 Graham analysis. You can't say something's obvious but not identify any
20 difference between the reference and the claimed invention; otherwise you're
21 making an anticipation argument. Here they never identified any
22 differences.

23 JUDGE GALLIGAN: Counsel, I'm going to point you to the petition
24 at page, around 14. You know, if they had styled this as an anticipation

1 argument, you would have said the clock -- the timing signal isn't the clock
2 signal.

3 MR. COCHRAN: Correct.

4 JUDGE GALLIGAN: So, they styled this as an obviousness
5 argument; anticipation is the, you know, epitome of obviousness; but we
6 don't have anticipation as obviousness; but they have come through and they
7 at least have addressed the Graham factors to some extent by saying, look,
8 the timing signal represents or renders obvious a clock signal -- and go
9 through -- and, you know, maybe there's a slight difference there but the
10 subject matter of the claims still would have been obvious. So, why
11 wouldn't that address the Graham factors to your satisfaction?

12 MR. COCHRAN: Well, I agree with what you said about the
13 anticipation is the epitome of obviousness; but, you know, here the
14 Petitioner has an obligation, and under PTAB rules, of setting forth exactly
15 what the ground is; but I think it's pretty clear here that they believe that this
16 was an anticipation ground; and if you look at slide number 10, this is what
17 their expert said. He believes that it was anticipated. So, they knew coming
18 in that the clock signal was going to be an issue -- they knew that. You can
19 tell that by the way they styled the petition. They didn't make it an
20 anticipation ground; they didn't provide any claim construction for clock
21 signal in the petition; but, instead, they presented it as if it was an
22 obviousness ground, no claim construction; and they were, essentially,
23 hedging their bets so that they could have whatever wiggle room they
24 needed to argue that these selection control signals in Sato were clock
25 signals -- and what I'm suggesting is that's an improper thing to do in a

1 petition. If you think it's an anticipatory reference, you should present it as
2 anticipatory reference. If you don't, and you present it as an obviousness
3 ground, then you should be bound by the Graham factors; and they should
4 have gone to that additional part of the task of identifying a difference; but
5 they didn't do that.

6 JUDGE GALLIGAN: Thank you. You can continue to argue. It's
7 your time, but I did want to move on to the clocks -- the definition of clock
8 signal, if we could. Now, I don't want to cut you off; it's your time to argue
9 as you see fit.

10 MR. COCHRAN: Okay; that's fine. I'll move on to the clock signal -
11 - if you could go to slide 14.

12 So, we have two competing interpretations of the clock signal. Both
13 sides, by the way, agree that the plain meaning should apply. The question
14 is what is the plain meaning. It's not enough just to say plain meaning. That
15 doesn't give any, you know, meaning to the claim at all -- to the claim term
16 at all. And the issue is what is the clock signal. We proposed that the plain
17 meaning should be construed according to the *IEEE Dictionary*, and that has
18 a single definition of clock signal, and it's a periodic signal used for
19 synchronization.

20 Petitioner came back in the reply and they said well, it should be
21 given their plain meaning; they don't say what that is; but then they come up
22 -- their definition is the same as ours, except they drop the word periodic.
23 So, the real issue here is what is the plain meaning.

24 JUDGE GALLIGAN: Before we get to the extrinsic evidence in the
25 *IEEE Dictionary*, so what -- I've looked through this patent many times, I

1 don't see a reference to synchronous and periodicity or anything; so, what is
2 the intrinsic evidence that supports your definition that a clock must be a
3 periodic signal?

4 MR. COCHRAN: Yes. If you turn to slide 16. So, the intrinsic
5 evidence that supports this is the description of the problems that the
6 invention was directed to -- and these are the capacitive loading problem;
7 reducing power consumption -- these are problems that only exist when you
8 have a synchronous memory system. If you have an asynchronous memory
9 system like in Sato, which doesn't have a clock signal at all, you wouldn't
10 have these same problems. So, it's this teaching of the problems that the
11 invention is directed to. This is the intrinsic evidence we have that would
12 lead to the definition that we've proposed from the *IEEE Dictionary*. These
13 problems only exist if you have a periodic clock signal.

14 JUDGE JEFFERSON: So, a person of ordinary skill in the art would
15 understand that the claims that you don't use the word periodic are restricted
16 to a periodic signal based on the nature of the problem --

17 MR. COCHRAN: Correct.

18 JUDGE JEFFERSON: -- with capacity and loading, basically?

19 MR. COCHRAN: Right. You can turn to 17, then.

20 JUDGE HOWARD: Does the claim actually require the clock signal?

21 MR. COCHRAN: Yes.

22 JUDGE HOWARD: Or does it require logic that does something in
23 response to a clock signal?

24 MR. COCHRAN: Turn back to 4. You know, the claim requires a
25 clock signal.

1 JUDGE HOWARD: The claim requires a circuit.

2 MR. COCHRAN: Yeah.

3 JUDGE HOWARD: By just physically having this circuit, and it's not
4 connected to anything -- no power on; it's not generating any clock signal;
5 it's not doing any work -- but the circuit is designed to do everything that's
6 recited in the claim, would that be covered by the claim?

7 MR. COCHRAN: Not if it doesn't receive a clock signal.

8 JUDGE HOWARD: Isn't it just requiring a device that if it had a
9 clock signal, it's a circuit that receives a clock signal --

10 MR. COCHRAN: Correct.

11 JUDGE HOWARD: -- and it doesn't think; but it's not -- is the claim
12 anywhere requiring this clock signal, to be generated?

13 MR. COCHRAN: No. The claim doesn't --

14 JUDGE HOWARD: The generation of the clock signal?

15 MR. COCHRAN: No. It just goes through the receipt of the clock
16 signal and then the application of the clock signal to a selected clock output.
17 So, it's got to be in (inaudible).

18 JUDGE HOWARD: And if you had Sato, and you just had changed it
19 so it was sending out a synchronous signal -- what you would consider a
20 clock signal -- would the circuit do everything that claim 1 says it has to do?

21 MR. COCHRAN: No; because in the Sato circuit -- hopefully, we'll
22 look into -- the Sato circuit does not create any clock outputs. So, hopefully,
23 I'll have time; I'll be able to get to that and explain that to you.

24 So, with respect to the dispute over clock signal, if you go to 22, the
25 Petitioner spends a lot of time poking holes in our definition, referring to all

1 kinds of other things saying that this isn't periodic, and this isn't periodic, or
2 this is dated; but they also refer to the *IEEE Dictionary*; and in their briefing;
3 except that they refer to the definition of clock, which is broader than the
4 definition of clock signal. You remember the term here isn't clock, it's clock
5 signal. And all this really shows is that the phrase clock signal is narrower
6 than the phrase clock. So, you know, at the end of the day here, on the term
7 clock signal, both sides agree that the plain meaning should apply; both sides
8 agree that the *IEEE Dictionary* is an unbiased reliable source of information;
9 and on that basis I would suggest that the correct definition that ought to be
10 applied is the one that we have proposed. But -- as I also, hopefully, point
11 out here in a second -- at some level it's not going to matter because whether
12 the signal is periodic or not, the Sato reference -- the critical element in the
13 Sato reference, which is the 5 chip-enable signal -- doesn't synchronize
14 anything. It's merely an on/off signal.

15 JUDGE GALLIGAN: So -- and I've been thinking about the clock
16 signal interpretation for a while, and it seems like the Patent Owner's point
17 is the absence of any specification or -- that's not a good word -- the absence
18 of any definition in the patent supports our position that it's limited. The
19 converse to that seems to be that any evidence that clock signal actually
20 doesn't have to be periodic would kind of contradict your argument, I would
21 think; and Petitioner has provided some other evidence that clock signal is
22 used to describe other types of signals that are not periodic.

23 MR. COCHRAN: Yeah; that's true; yeah, they can. But as I said I
24 think that whether you ultimately decide it has to be periodic or not, you

1 know, the question is whether the signal is synchronizing anything; and we'll
2 see in Sato that doesn't happen there -- whether it's periodic or not.

3 JUDGE GALLIGAN: And yet you're putting aside even the
4 construction of the clock signal whether it's periodic or not, column 12 of
5 Sato, which Petitioner raised in its briefing, says the present invention can be
6 applied widely to semiconductor memory devices having at least a clocked
7 static-type address decoder and semiconductor memory devices of the types
8 described above. So, putting aside whatever definition you come up with,
9 that's an express teaching of a clock signal, or a device that is used with a
10 clock signal; and so, in your briefing you said that's unsupported opinion.
11 That's just express disclosure of the reference; it's not an opinion of an
12 expert, for instance. It's the reference says what it says, right?

13 MR. COCHRAN: Yeah. I think that portion you're referring to Judge
14 Galligan -- that just shows that in the Sato patent he knew how to use the
15 word clock when he was describing those other things. He says when an
16 invention could be applicable to these other things which have a clock, but
17 all that shows you is what he actually discloses -- particularly, in figure 3 --
18 is it clocked; otherwise, he would have called his integral timing signals
19 clock signals. So, that's all we were -- the point we were trying to make
20 there is that's just further evidence that what's in Sato -- the selection control
21 signal is what it's called -- is not a clock signal.

22 (Time noted: 5:00 p.m.)

23 JUDGE GALLIGAN: Okay; thank you.

24 MR. COCHRAN: Can you go to 25? So turning then quickly to the
25 teaching of Sato -- Sato teaches a device called the TC block, which takes a

1 chip-enable, the write-enable, and the output-enable signals from external to
2 the chip; and generally it's these internal signals, which he sometimes calls
3 timing signals, but he also calls these selection control signals. And what we
4 know about these signals -- slide 27 -- in particular, the selection control
5 signal -- the key one that they're calling -- well, they say it's a clock signal or
6 it represents a clock signal -- as we talked about that before -- the timing
7 signal Φ_{ce} -- all we know about that signal for sure is from this paragraph
8 of Sato where it basically just says it follows the external chip-enable signal.
9 So, what is this signal -- this Φ_{ce} signal? It's simply following the external
10 chip-enable signal. Clearly, it's not periodic; there's no disclosure of it being
11 a periodic signal; and there's really no disclosure of it synchronizing
12 anything. So, even if you were to adopt their definition of clock signal, the
13 selection control signal, Φ_{ce} , is not synchronizing anything; it's merely -- it's
14 like an on/off switch, just powering up or powering down.

15 You can go to 31 -- I'm sorry, 32. Want to make sure I have a few
16 minutes to talk about the clock output limitation.

17 It's 33 -- So, the claim requires that the first logic applies the clock
18 signal to a selected clock output of the plurality of clock outputs.

19 34 -- And in the petition, the petition refers almost exclusively to
20 figure 3 and argues that the PDCR block in Sato's figure 3 is creating the
21 claimed clock outputs.

22 36 -- If you look at Sato, though, you'll see that he doesn't provide any
23 -- there's no indication that these selection signals that are labeled Φ_{x1} , Φ_{x2} , Φ_{x3} -- that these are clock signals or that they are synchronizing

1 anything. In fact, he never calls them timing signals; he never calls them
2 clock signals; he exclusively refers to these as the selection signals.

3 38 -- Now, the one portion of the Asano reference that provides any
4 significant detail on the PDCR block is not with respect to figure 3. When
5 you look to the description of figure 3, it's vague and unclear as to how the
6 PDCR block is generating these Φ -x1 zero signals in connection with the
7 selection control signal. But here in figure 1, this is where the description of
8 that block is included. And you can see that here, he still refers to these as
9 selection signals, but the selection control signal, Φ ce is not even provided
10 to that block. So, I don't think it's fair for them to assume that those signals
11 are clock outputs since the alleged clock signal in figure 1 isn't even
12 provided to that block.

13 So, I think, with respect to this issue, I think that at the end of the day,
14 there isn't enough explicit disclosure in Sato of the operation of the PDCR
15 block to know how these clock outputs are even generated; and for that
16 reason, and additionally, the ground ought to be dismissed. And I'll reserve
17 the rest of my time.

18 JUDGE GALLIGAN: Thanks, Counsel. You have about 11-1/2
19 minutes. Thank you.

20 MR. COCHRAN: Thank you, Your Honors.

21 MR. HOOVER: Slide 15. I'll refer you back to slide 15. The Patent
22 Owner was describing how Asano doesn't teach portioning of addresses in
23 some sense; but I would like to note that -- as Your Honors pointed out
24 correctly -- in paragraph 16 of Asano -- and Asano does describe several bits
25 that the x-address line is eight bits, which Dr. Horst's analysis showed that

1 just using the powers of two that requires three address bits; and similar for
2 the wordline select and the wordline enable signal. But also Dr. Pedram
3 acknowledged during his deposition -- we've cited that on page 21 of our
4 reply -- that partitioning of addresses is not a physical partition, it's a logical
5 partition. So, the fact that we have a one single group of address bits going
6 into the predecoder is irrelevant.

7 In addition, they have brought up a point about simultaneous decoding
8 in the '002 Patent, but that's not anywhere in the claims; and, likewise, as far
9 as looking where to look for different decoding circuits from a textbook, the
10 patent itself doesn't teach decoding circuitry. So, are we to expect that if
11 someone wouldn't look to a textbook, or even a particular textbook, to
12 determine how to decode groups of logic bits in using separate circuitry that
13 the '002 Patent is somehow not enabled?

14 And I would also like to address the -- I'm not going to change a slide
15 -- but as to why would someone have looked to Itoh when they were trying
16 to implement Asano. The claims, first of all, don't require any specific
17 configuration of logic circuitry. In our present record, both Apple's and
18 Qualcomm's experts agreed that the POSITA would have implemented
19 Asano circuit using distinct logic paths. Dr. Pedram even explained that's
20 how he taught his students to decode that type of partitioning of addresses.

21 If we go to slide 46 -- Regarding the explanation of the argument that
22 somehow Sato's predecoder does not actually apply the timing signal in the
23 same way as claimed in the '002 Patent. Part of what Dr. Horst's analysis --
24 that he presented in his first declaration in paragraph 62 -- specifically, he
25 provided this illustration of how he understood a POSITA would interpret

1 the textual description in Sato in column 9, lines 44 to 59 of the operation of
2 the predecoder in the figure 3 embodiment. Notably, the Patent Owner, in
3 their slides, cited to several different portions. In slide 36 of their slides,
4 they've cited to several different portions of Sato -- did not cite to this
5 column.

6 Likewise, they're referring to the embodiment of figure 1 which Sato
7 explains is a different embodiment -- a different exemplary embodiment.
8 The petition is not saying that embodiment of Sato renders the claims
9 obvious, but the embodiment of figure 3. In addition, the other slide that
10 I've skipped, 47, shows that Dr. Horst, in his analysis of the operation of the
11 predecoder, he corroborated his analysis on slide 47 with another textbook --
12 Brown's digital logic textbook -- just to provide additional support that his
13 understanding of how this predecoder worked based on Sato's explanation of
14 it was correct.

15 Another additional point on Sato's predecoder is that during
16 deposition -- during Dr. Horst's -- I think it was his second deposition -- it's
17 Exhibit 2005, on page 30 -- Dr. Horst explained to counsel that Sato
18 describes the predecoder operation in words instead of a picture, and in
19 sufficient detail that he was able to draw the diagram that we showed on
20 slide 46 of what the internal circuitry of the predecoder would look like.

21 Lastly, I would like to turn to slide 40. The statement that Sato's
22 timing signal does not perform any synchronization is just false. And there's
23 with the understanding of how Dr. Pedram explains how the predecoder
24 operates to apply the timing signal through the predecoder to these red
25 outputs in figure 3 of Sato, these red outputs are definitely synchronizing

1 something. They're synchronizing the operation of the purple and blue
2 transistors -- just the exact same way -- and they're synchronizing them the
3 exact same way that the clock signal is synchronizing the same transistors in
4 the '002 Patent. Your Honors have any questions?

5 JUDGE GALLIGAN: Nothing from me; thank you.

6 MR. HOOVER: Thank you. I'll turn this to Mr. Riffe to address
7 some additional rebuttal points.

8 MR. RIFFE: Just a few more points, Your Honors. I'll like to address
9 an issue that each of you raised earlier with my colleague for Qualcomm.
10 The first issue was -- Judge Jefferson you mentioned that you had a
11 discussion around the teaching of the problem, providing a basis for limiting
12 the clock signal to a periodic clock signal in terms of loading and things of
13 that nature. And it's interesting in addition to what Counsel said -- there
14 they also raised that point in their sur-reply. And they said the reduced load
15 on the clock is achieved because the clock is provided to only the first logic
16 and not the second logic. What really what that's admitting is that any
17 benefit from the reducing the load is attributable not to the clock signal but -
18 - not to the type of clock -- but to an unclaimed feature of one embodiment
19 shown in the '002 Patent. There's nothing in the claim that precludes the
20 second logic from receiving the clock signal. And interestingly enough --
21 and I'll give you a citation of this. I don't think we have a copy of it in our
22 demonstratives -- but at Apple 1019, Exhibit 1019, at pages 74 through 75 --
23 and which is Dr. Pedram's deposition -- he conceded that claim 1 does not
24 preclude the clock signal from reaching the second logic -- or vice versa of
25 the second logic -- from receiving the clock signals. He agreed with that.

1 So, for them to base their claim construction on this supposed problem, we
2 believe, is incorrect.

3 Now, Judge Galligan you mentioned the Graham factors and the
4 analysis there, and Patent Owner's counsel said we had an obligation to say
5 what the ground was. I don't think there's any dispute -- if I'm not mistaken -
6 - that we did that -- we asserted obviousness. Why did we do that? Judge
7 Galligan, as you recognize, we recognized that there were differences in
8 terminology between Sato -- which uses the phrase timing signal, and the
9 '002 Patent, clock signal. And while, Judge Galligan, as you recognize,
10 that's a thin difference -- it is a difference nonetheless. And under Graham,
11 we were required to address that; and we, specifically, addressed that in the
12 petition; and we noted that. I'm going to stop on that.

13 And Judge Howard, finally, if I could have slide 7 pulled up -- you
14 asked do the claims require the clock signal; and I think Counsel tried to
15 answer your question -- I'm not sure if he did or not -- but I will; and I'll say
16 it doesn't. The claim requires two things if we wanted to look at them. It
17 requires a first logic to receive a clock signal and to do other things with
18 other pieces of data, and a second logic to decode a second portion of the
19 memory; and to do other things. So, it only requires two things -- the first
20 logic and the second logic -- inferentially claims a clock signal -- so, it's
21 agnostic to that. And with that, with any questions, I'll rest Your Honor;
22 and, I think, we'll surrender our time.

23 JUDGE GALLIGAN: Thank you, Counsel.

24 MR. RIFFE: Thank you.

1 JUDGE GALLIGAN: Patent Owner? Patent Owner, you have 11-1/2
2 minutes left.

3 MR. COCHRAN: Just a couple of follow-up points. I wanted to
4 clarify that one thing that my colleague said. There's no question the patent
5 specifically discloses separate decoding circuits as a critical part of the
6 claimed invention that you have first and second logic circuits, and you have
7 separate portions that are then provided in parallel to the wordline decoder.

8 If you turn to Asano 46 -- I'm sorry not Asano -- our slide, 46. This is
9 the flowchart from Asano; and as I said, you can see that the single input
10 address is coming in. It's being decoded in the predecoder; and then,
11 ultimately, if we go down further, you can see that the final decode address
12 is used in combination with these latches to latch the signal, the other signal
13 that comes out of the predecoder. So, it's a single portion; there's one
14 address; there is no parallel processing of the addresses in the Asano
15 reference.

16 If you turn to 38 -- With respect to the Sato description of the
17 predecoder block, if they were relying entirely on figure 3, but in the
18 petition, they repeatedly come back to the description of the predecoder
19 block in figure 1; and if you look at that, that's the only meaningful teaching
20 in Sato of the functionality of the predecoder. And as I pointed out
21 previously, you can see that block does not even receive this chip enable
22 Φ_{ce} signal. So, I would suggest that should raise some significant doubt as
23 to whether the outputs, the selection signals --

24 JUDGE GALLIGAN: Are we talking about slide 38?

25 MR. COCHRAN: Yeah.

1 JUDGE GALLIGAN: Yeah; the reason they relied on figure 3 was
2 because it shows the Φ_{ce} signal into the predecoder and figure 1 does not.
3 That was my understanding.

4 MR. COCHRAN: My point is if you look at the description of that in
5 figure 3, it provides almost no detail as to what's happening there. So,
6 there's a lack of evidence in terms of what is coming out of the predecoder
7 block in number three. This is the only description.

8 JUDGE GALLIGAN: Okay; thank you.

9 MR. COCHRAN: With respect to the power savings, the power
10 savings part of the invention that we mentioned earlier comes from two
11 things. Yes, it comes from breaking up the address; but it also comes from
12 the selective application of the clock signal to one of the clock outputs. That
13 is a critical part of the invention, and they have not demonstrated that is
14 shown in Sato.

15 And, finally, I'd like to say with respect to the selection control signal
16 of Sato, it is not synchronizing anything; it is simply turning circuits on and
17 off; and if you just raise the chip enable signal, the selection control signal
18 will activate certain circuits but nothing will happen unless the other
19 asynchronous signals, like the address lines and the other enable signals, are
20 provided to his memory device; and for that reason, it should not be
21 considered a clock signal. Thank you.

22 JUDGE GALLIGAN: Questions?

23 JUDGE JEFFERSON: No questions from me.

24 JUDGE GALLIGAN: No questions. Thank you very much to both
25 Counsel, or all three Counsel, for their excellent presentations. The matter is

1 submitted and we will issue final written decisions in due course. We are
2 adjourned, and enjoy the rest of the evening; and safe travel home. I guess
3 there are some hearings tomorrow.

4 (Whereupon, the proceedings at 5:18 p.m. were concluded.)

PETITIONER:

Walter Renner
Thomas Rozylowicz
Timothy Riffe
Kenneth Hoover
Whitney Reichel
FISH & RICHARDSON P.C.
axf-ptab@fr.com
tar@fr.com
riffe@fr.com
hoover@fr.com
wreichel@fr.com

PATENT OWNER:

David Cochran
Matthew Johnson
Joshua Nightingale
Joseph Sauer
David Maiorana
Richard Graham
JONES DAY
dcochran@jonesday.com
mwjohnson@jonesday.com
jrnightingale@jonesday.com
jmsauer@jonesday.com
dmaiorana@jonesday.com
ragraham@jonesday.com