

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

Case IPR2018-01249
Patent 7,693,002 B2

Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and
SCOTT B. HOWARD, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Apple Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–28 and 31–37 of U.S. Patent No. 7,693,002 B2 (“the ’002 patent,” Ex. 1001). Paper 2 (“Pet.”). Qualcomm Incorporated (“Patent Owner”) did not file a Preliminary Response. Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute review.

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response, if one is filed, shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

After considering the Petition and associated evidence, we institute an *inter partes* review as to all challenged claims and on all grounds raised in the Petition.

A. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), each party identifies various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 82; Paper 3, 2.

B. The ’002 Patent and Illustrative Claim

The ’002 patent generally relates wordline drivers and decoders for memory arrays. Ex. 1001, [57], 1:7–9. Figure 1 of the ’002 patent is reproduced below.

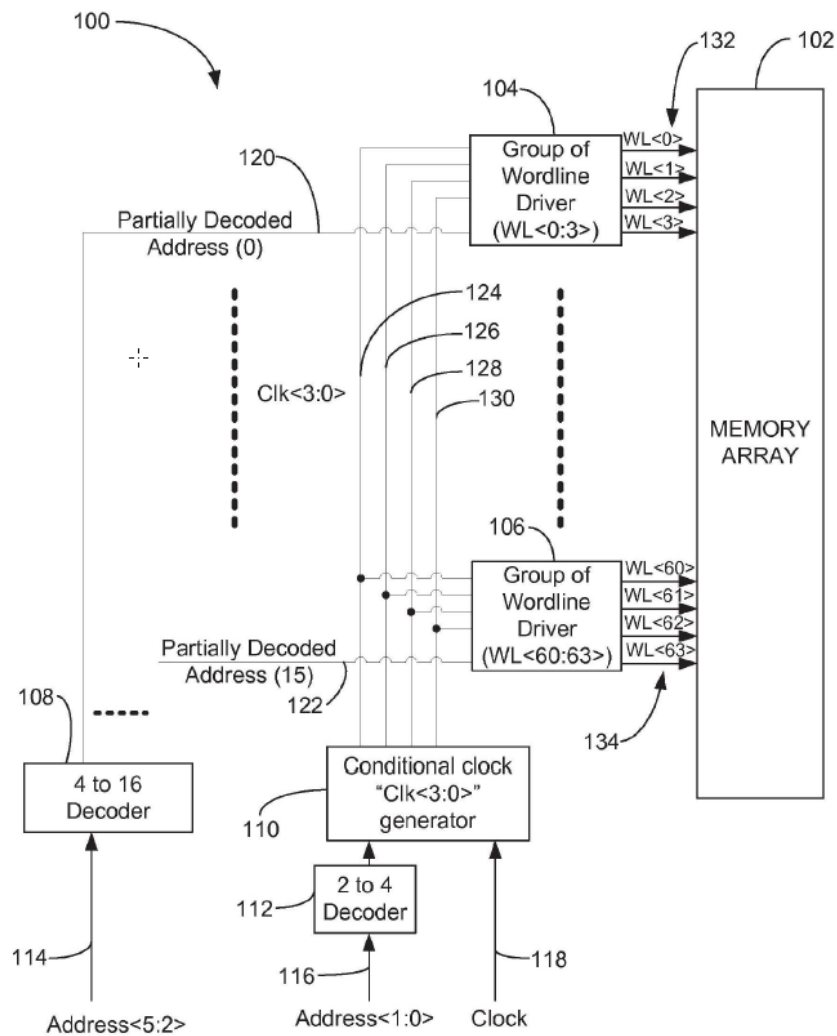


FIG. 1

Figure 1 is a block diagram of an embodiment of a wordline driver system 100. Ex. 1001, 2:31–34. Figure 1 shows groups of wordline drivers 104 and 106 that control particular wordlines in memory array 102. *Id.* at 2:53–3:8. Group of wordline drivers 104 drives wordlines WL<0> through WL<3>, and group of wordline drivers 106 drives wordlines WL<60> through WL<63>. *Id.* Additional wordline drivers that are not shown control the wordlines between WL<3> and WL<60>. *Id.* at 3:4–8.

In operation, two-to-four bit decoder 112 decodes the first portion (such as bits 0 and 1) of a six-bit memory address, and four-to-sixteen bit decoder decodes the remaining portion of the address (bits 2 through 5). Ex. 1001, 3:9–25. Based on the decoded first portion of the address received from decoder 112, conditional clock generator 110 “selectively applies the clock signal to a selected one of the clock outputs 124, 126, 128 and 130,” each of which is coupled to a particular wordline driver in each group of wordline drivers. *Id.* at 3:26–34. “The four-to-sixteen bit memory address decoder 108 decodes the remainder of the six-bit memory address (e.g. bits two to five) and applies a partial address input to the wordlines that are related to the decoded memory address.” *Id.* at 3:37–40. For example, if the partially-decoded address indicates that the first group of wordlines is addressed (WL<0> through WL<3>), decoder 108 applies a signal to address line 120, which, as shown in Figure 1, connects to group of wordline drivers 104. Ex. 1001, 3:41–67. The ’002 patent explains that “the decoded output of the two-to-four decoder 112 with clock generator 110 and the decoded output of the four-to-sixteen bit memory address decoder 108 may be utilized via a logical AND operation to selectively activate a wordline driver of the group of wordline drivers 104.” *Id.* at 4:3–8.

Of the challenged claims, claims 1, 7, 11, 17, 21, and 23–27 are independent. Claim 1, reproduced below, is illustrative.

1. A circuit device comprising:
first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

C. References

Petitioner relies upon the following references:

Sato	US 4,951,259	Aug. 21, 1990	Ex. 1005
Asano	US 2006/0098520 A1	May 11, 2006	Ex. 1006
Kiyoo Itoh,	<i>VLSI Memory Chip Design</i> , 2001 (“Itoh”)		Ex. 1007

D. Asserted Grounds of Unpatentability

Petitioner asserts claims 1–28 and 31–37 of the ’002 patent are unpatentable based on the grounds set forth in the table below.

Reference(s)	Basis	Claims
Sato	§ 103	1–28 and 31–37
Asano and Itoh	§ 103	1–17, 20–28, and 31–36

II. ANALYSIS

A. Claim Construction

Petitioner proposes constructions for various claim terms. Pet. 3–7. For purposes of deciding whether to institute a trial, we do not find it necessary to construe expressly any claim terms. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

C. Level of Ordinary Skill in the Art

Relying on the testimony of Dr. Robert Horst, Petitioner offers the following assessment as to the level of ordinary skill in the art:

A person of ordinary skill in the art (“POSITA”) as of October 10, 2006 would have had at least an undergraduate degree in electrical engineering, or a related field, and three years of experience in the design of memory systems and circuits. Alternatively, a person of ordinary skill with less than the amount of experience noted above would have had a correspondingly greater amount of educational training such a graduate degree in a related field.

Pet. 2 (citing Ex. 1003 ¶¶ 27–29). To the extent necessary, and for purposes of this Decision, we accept the assessment offered by Petitioner, with the exception of the language “at least,” because this assessment is consistent with the ’002 patent, the asserted prior art, and the evidence of record. See Ex. 1003 ¶ 27.

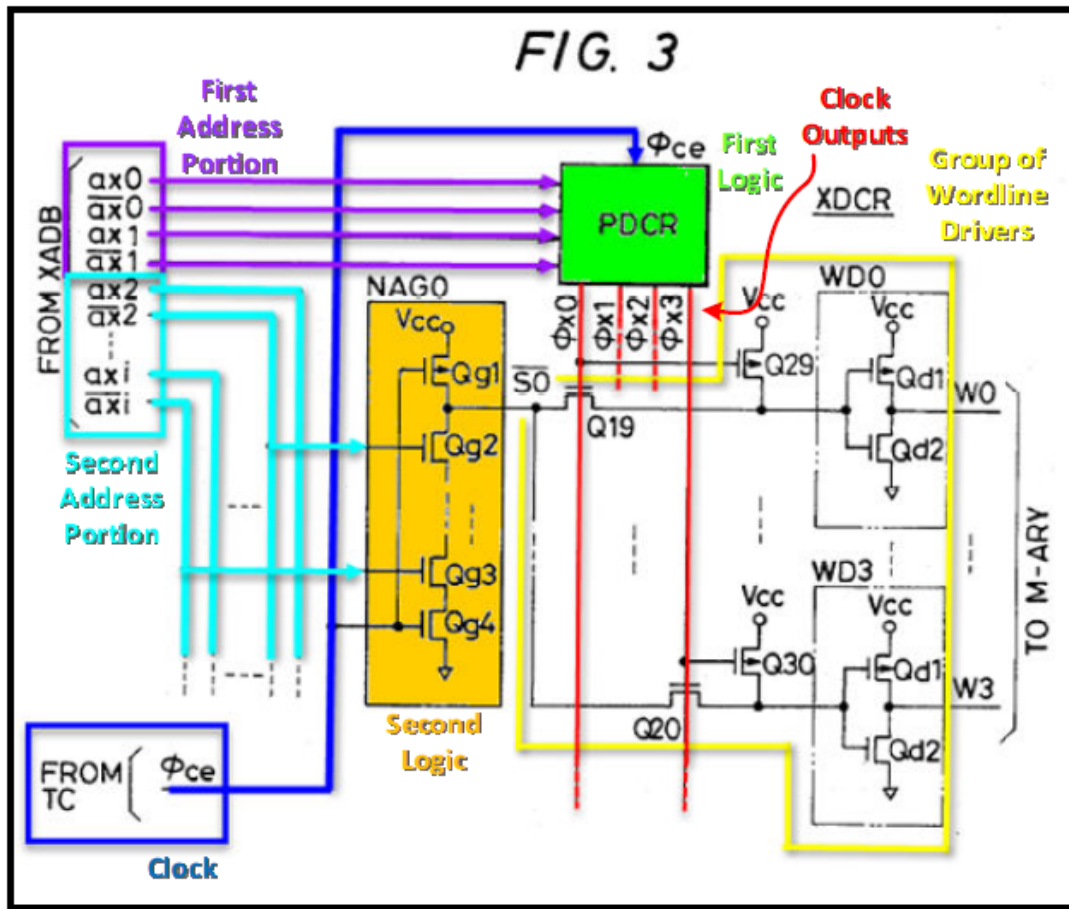
decoder PDCR and its output signal, that is, the selection signal $\phi_{x0} \sim \phi_{x3}$, is generated in accordance with this timing signal ϕ_{ce} .” Ex. 1005, 10:36–39. Decoding NAND gate circuits, of which only one, NAG0, is shown in Figure 3, are used to decode the remaining address bits to select the appropriate wordline drive circuit. Ex. 1005, 5:43–6:59.

2. Independent Claim 1

Independent claim 1 is reproduced above and is directed to “[a] circuit device” having

first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array.

With its obviousness contentions, Petitioner provides the following annotated version of Sato’s Figure 3:



Pet. 10. In the annotated version of Sato’s Figure 3, Petitioner identifies particular components that it contends teach various limitations recited in claim 1. Pet. 10. In particular, Petitioner identifies Sato’s PDCR and NAND gate circuits as teaching, respectively, first logic and second logic. Pet. 12.

Petitioner contends Sato’s disclosure of pre-decoder PDCR receiving timing signal ϕ_{ce} and address signals ax_0 and ax_1 , along with their complements, teaches “first logic to receive a clock signal and a first portion of a memory address of a memory array,” as recited in claim 1. Pet. 14 (citing Ex. 1005, 3:9–15, 3:50–59, 4:6–11, 5:16–24, 9:44–54, Fig. 3). Petitioner contends (Pet. 18) Sato teaches “the first logic to decode the first portion of the memory address” because Sato discloses that “pre-decoder

PDCR decodes the lower 2-bit complementary internal address signals $\underline{ax}0$ and $\underline{ax}1$ ” (Ex. 1005, 5:25–26). Petitioner also contends Sato teaches the first logic “to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array” through its disclosure of PDCR generating selection signals $\phi x0$ through $\phi x3$ based on input timing signal ϕce . Pet. 18–23 (citing, *inter alia*, Ex. 1005, 5:25–31, 6:40–55, 9:30–51, 9:52–65, 10:36–39, claim 1, Fig. 3). For example, Sato discloses that “timing signal ϕce described above is supplied to the pre-decoder PDCR and its output signal, that is, the selection signal $\phi x0 \sim \phi x3$, is generated in accordance with this timing signal ϕce .” Ex. 1005, 10:36–39. Citing the testimony of Dr. Horst, Petitioner argues that “[t]iming signal ϕce represents or renders obvious a clock signal.” Pet. 14–17 (citing, *inter alia*, Ex. 1003 ¶¶ 64–69).

As to the claimed “second logic,” Petitioner contends Sato discloses that NAND gate circuits, such as NAG0 in Figure 3, decode the address bits other than those decoded by pre-decoder PDCR, thereby teaching “second logic to decode a second portion of the memory address.” Pet. 24–27 (citing, *inter alia*, Ex. 1005, 5:19–22, 5:53–58, 5:66–6:21, 9:44–48, Fig. 3). Sato discloses that its RAM has “k+1 decoding NAND gate circuits NAG0 ~ NAGk to which the complementary internal address signals $ax2 \sim axi$ other than the lower two bits in respective combinations are supplied.” Ex. 1005, 5:19–22; *see also id.* at 9:45–48 (explaining that the Figure 3 “embodiment includes one pre-decoder PDCR and k+1 decoding NAND gate circuits NAG0-NAGk in the same way as in the foregoing embodiments”). Petitioner also contends that Sato teaches “selectively activat[ing] a

particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address” through its disclosure of activating a particular wordline based on the address signal. Pet. 27–32 (citing, *inter alia*, Ex. 1005, 5:66–6:21, 6:40–44, 6:55–59, 8:27–32, 9:31–51, 9:60–10:13, 10:36–39, claim 1, Fig. 3). In particular, Sato discloses that, based on address decoding by the NAND gates in combination with the operation of the PDCR, a selection signal “is transmitted to only the word line drive circuit corresponding to one word line that is designated by the X address signal Ax0 ~ Axi.” Ex. 1005, 6:55–59.

On this record, we are persuaded Petitioner has shown sufficiently for purposes of institution that Sato teaches the subject matter recited in claim 1. Therefore, Petitioner has demonstrated a reasonable likelihood that it would prevail in showing that claim 1 would have been obvious over Sato.

3. *Claims 2–28 and 31–37*

We have reviewed Petitioner’s contentions in this ground as to claims 2–28 and 31–37, and we are persuaded Petitioner’s arguments and evidence are sufficient to show a reasonable likelihood Petitioner would prevail in proving unpatentability of these claims.

E. Alleged Obviousness over Asano and Itoh (Claims 1–17, 20–28, and 31–36)

Petitioner contends claims 1–17, 20–28, and 31–36 of the ’002 patent are unpatentable under 35 U.S.C. § 103 as obvious over the combined teachings of Asano and Itoh. Pet. 2, 33–59, 61–62, 64–78, 80–81. For purposes of determining whether to institute, we focus on Petitioner’s contentions with respect to claim 1 in this ground.

1. Asano

Like the '002 patent, Asano is directed to wordline drivers for memory. Ex. 1005, [54], [57]. Figure 2 of Asano is reproduced below.

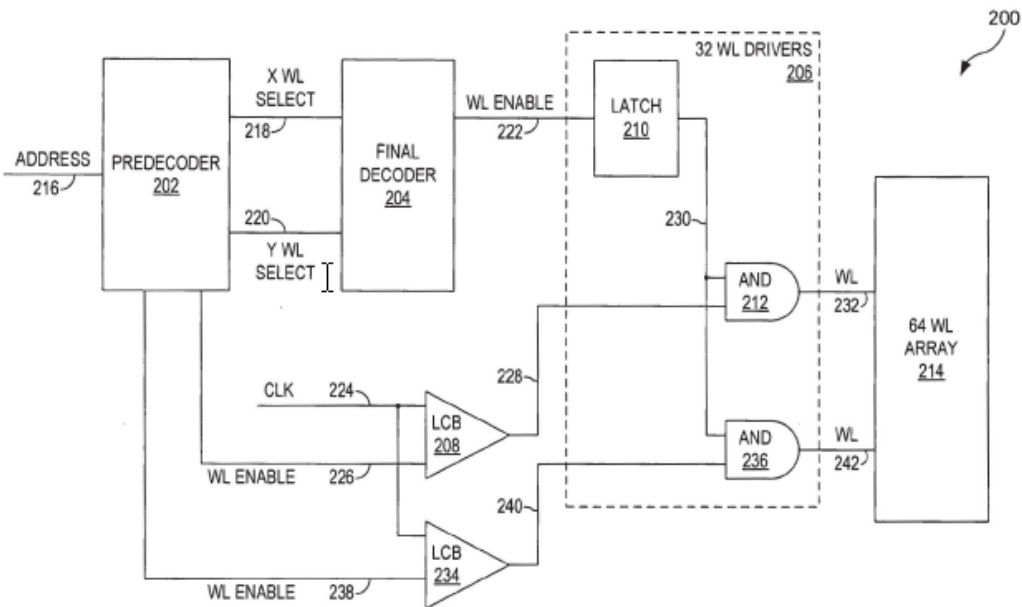


FIG. 2

Figure 3 is a diagram of memory 200 having predecoder 202, final decoder 204, 32 wordline drivers 206, first local clock buffer (LCB) 208, second LCB 234, and 64 wordline array 214. Ex. 1006 ¶ 15. Asano explains that final decoder 204 “determines which of the 32 wordline drivers 206 are to be enabled” and also that predecoder 202 provides a selection signal either to first LCB 208 or second LCB 234 based on the most significant bit of the address. Ex. 1006 ¶¶ 17–19. “By providing selection signals to the LCBs, the last decoding can be delayed until the wordline driver stage.” Ex. 1006 ¶ 18. Thus, one of the 32 wordline drivers is selected, and, within each wordline driver, one of the two AND gates 212 and 236 is selected by virtue of the selection of either LCB 208 or LCB 234 based on the most significant

bit of the address. Asano explains, therefore, that “[o]ne of the respective AND gates 212 and 236 can then output a wordline signal in step 318 to a wordline within the 64 wordline array 214.” Ex. 1006 ¶ 19.

2. Itoh

Itoh is a textbook on memory design, and, in a chapter on DRAM circuits, it provides examples of predecoding circuits in Figure 3.46, reproduced below.

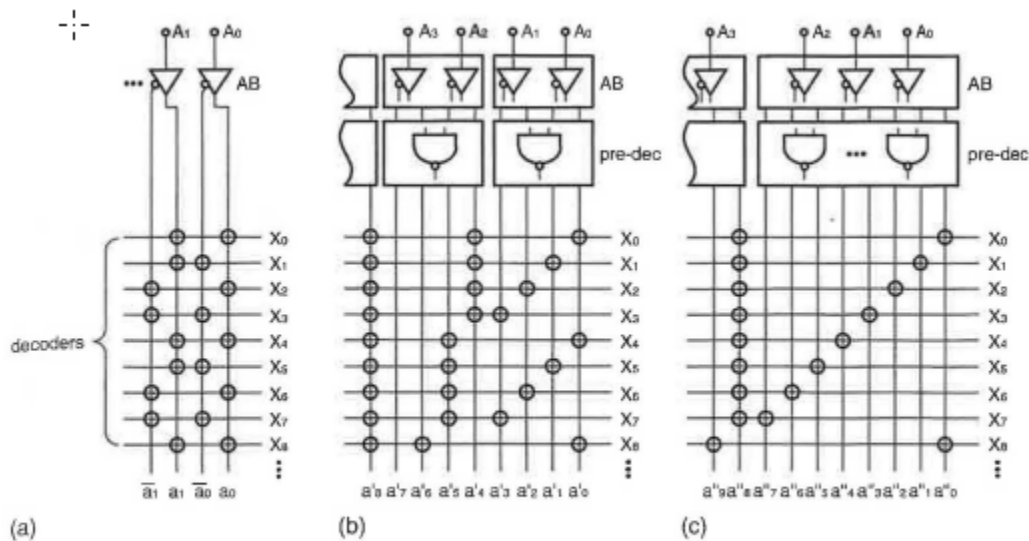
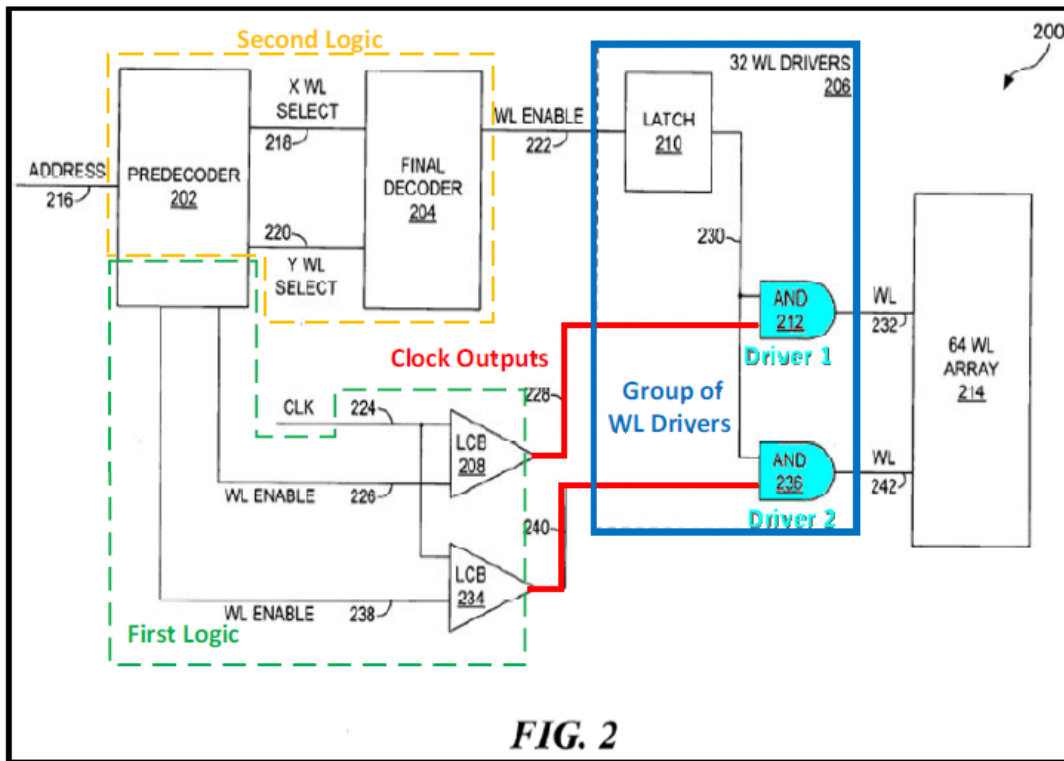


Fig. 3.46. Predecoding [3.4]. (a) no predecoding; (b) 2-bit predecoding; (c) 3-bit predecoding

Figure 3.46 illustrates a 2-bit predecoding circuit and a 3-bit predecoding circuit in (b) and (c), respectively. Ex. 1007, 146–47.

3. Independent Claim 1

With its obviousness contentions, Petitioner provides the following annotated version of Asano’s Figure 2:



Pet. 34. In the annotated version of Asano’s Figure 2, Petitioner identifies particular components that it contends teach various limitations recited in claim 1. Pet. 34.

Petitioner notes that “Asano represents the predecoder 202 simply using a block element in a block diagram,” and Petitioner argues that a person of ordinary skill in the art “would have looked to Itoh’s textbook circuits in determining how the internal structure of the predecoder 202 would be built as separate logic sections for decoding different portions of the 6-bit memory address.” Pet. 35. Petitioner contends a person of ordinary skill in the art “designing Asano’s memory circuit would have naturally turned to a textbook such as Itoh’s for details on memory design techniques for a predecoder” and “would have understood that Itoh’s individual predecoder circuits would merely perform their intended

functions when implemented in Asano's predecoder 202." Pet. 35 (citing Ex. 1003 ¶¶ 121–123).

Petitioner contends that, in combination with Itoh, Asano's disclosure of LCB 208 and LCB 234, each with a clock input and a selection signal input from predecoder 202 based on the most significant bit of the address, teaches "first logic to receive a clock signal and a first portion of a memory address of a memory array." Pet. 41 (citing Ex. 1006 ¶¶ 16, 19, 21, Fig. 2; Ex. 1003 ¶¶ 117–120, 131). Petitioner contends that, in combination with Itoh, Asano's disclosure that predecoder 202 provides wordline enable signals (or "selection signals," as stated in paragraph 18) to LCB 208 and LCB 234 based on the most significant bit of the address teaches "the first logic to decode the first portion of the memory address." Pet. 42–44 (citing Ex. 1006 ¶¶ 16, 18–21, Fig. 2; Ex. 1003 ¶¶ 115, 117–120, 123). Petitioner contends that providing the clock outputs from either LCB 208 or LCB 234 based on the most significant bit of the address teaches "apply[ing] the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array." Pet. 45–48 (citing, *inter alia*, Ex. 1006 ¶¶ 16–21, Fig. 2; Ex. 1003 ¶¶ 14, 113–118, 132–133). In particular, Asano discloses that, "[d]epending on the most significant bit of the address signal that is input into the predecoder 202, either the first AND gate 212 or the second AND gate 236 is selected, wherein the clocking signal is ANDed with the output of the latch 210 in steps 314 and 316." Ex. 1006 ¶ 19.

As to the claimed "second logic," Petitioner contends "Asano's predecoder 202 and final decoder 204 decode five of six address bits (e.g., the second portion) of memory address 216" to produce an 8-bit X wordline

select signal and a 4-bit Y wordline select signal. Pet. 48 (citing Ex. 1006 ¶ 16; Ex. 1003 ¶¶ 110–111, 118). In particular, Asano discloses that “the address is 6 bits long, and from those 6 bits, the predecoder derives a wordline enable signal and two wordline select signals in step 304, an X wordline select signal and a Y wordline select signal.” Ex. 1006 ¶ 16. Petitioner argues that “it would have been an obvious design choice for a [person of ordinary skill in the art] to implement Asano’s predecoder using Itoh’s three-bit and two-bit predecoders to generate the X and Y wordline select signals,” and Petitioner provides an annotated figure showing Asano’s predecoder implemented with Itoh’s predecoder circuitry. Pet. 48–49 (citing Ex. 1003 ¶¶ 110–111, 118, 122–124). Petitioner contends that Asano’s “final decoder decodes the X and Y wordline select signals to determine which of the 32 wordline groups to enable.” Pet. 49 (citing Ex. 1006 ¶ 17; Ex. 1003 ¶ 112). In particular, Asano discloses that, “[o]nce the X wordline select signal and the Y wordline select signal have been transmitted to the final decoder 204, the final decoder 204 in step 306 determines which of the 32 wordline drivers 206 are to be enabled.” Ex. 1006 ¶ 17.

On this record, we are persuaded Petitioner has shown sufficiently for purposes of institution that the combination of Asano and Itoh teaches the subject matter recited in claim 1, and we also are persuaded that Petitioner has set forth sufficient reasoning, supported by evidence in the record, for why a person of ordinary skill in the art would have combined the teachings of Asano and Itoh. In particular, on this record, we credit Dr. Horst’s testimony that a person of ordinary skill in the art “would have naturally turned to a textbook such as Itoh” for details on specific predecoder circuits “to determine how the internal circuitry for Asano’s predecoder and decoder

would be built,” and we also credit his testimony that “Itoh’s predecoder circuits . . . represent well-known predecoder circuit designs.” Ex. 1003 ¶¶ 121–122. Therefore, Petitioner has demonstrated a reasonable likelihood that it would prevail in showing that claim 1 would have been obvious over the combined teachings of Asano and Itoh.

4. *Claims 2–17, 20–28, and 31–36*

We have reviewed Petitioner’s contentions in this ground as to claims 2–17, 20–28, and 31–36, and we are persuaded Petitioner’s arguments and evidence are sufficient to show a reasonable likelihood Petitioner would prevail in proving unpatentability of these claims.

III. CONCLUSION

For the foregoing reasons, we determine that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in challenging at least one of claims 1–28 and 31–37 of the ’002 patent. At this stage of the proceeding, we have not made a final determination with respect to the patentability of these challenged claims or the construction of any claim term. Because Petitioner has satisfied the threshold for institution as to one claim, we institute *inter partes* review on all claims and all grounds raised in the Petition. *See SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018) (holding that a decision to institute under 35 U.S.C. § 314 may not institute on fewer than all claims challenged in the petition); *see also* “Guidance on the impact of SAS on AIA

trial proceedings”¹ (stating that, “if the PTAB institutes a trial, the PTAB will institute on all challenges raised in the petition”).

IV. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, an *inter partes* review is hereby instituted as to all claims challenged (claims 1–28 and 31–37 of the ’002 patent) and on all challenges raised in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which will commence on the entry date of this decision.

¹ <https://www.uspto.gov/patents-application-process/patent-trial-and-appeal-board/trials/guidance-impact-sas-aia-trial>.

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