

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

Cases IPR2018-01315
Patent 8,063,674 B2

Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and
SCOTT B. HOWARD, *Administrative Patent Judges*.

HOWARD, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Apple Inc. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1, 2, and 5–7 of U.S. Patent No. 8,063,674 B2 (Ex. 1001, “the ’674 patent”) pursuant to 35 U.S.C. §§ 311–319. Paper 2 (“Petition” or “Pet.”). Qualcomm Incorporated (“Patent Owner”) filed a Patent Owner Preliminary Response. Paper 6 (“Preliminary Response” or “Prelim. Resp.”).

We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). *Inter partes* review may not be instituted unless “the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). On April 24, 2018, the Supreme Court held that a decision to institute under 35 U.S.C. § 314 may not institute on fewer than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

For the reasons set forth below, upon considering the Petition, Preliminary Response, and evidence of record, we determine that the information presented in the Petition establishes a reasonable likelihood that Petitioner will prevail with respect to at least one of the challenged claims. Accordingly, we institute *inter partes* review on all of the challenged claims based on the all of the grounds identified in the Petition.

A. *Real Party-In-Interest*

Petitioner identifies Apple, Inc. as the real party-in-interest. Pet. 64.

B. Related Proceedings

The parties identify the following currently pending patent litigation proceedings in which the '674 patent is asserted: *In re Certain Mobile Electronic Devices and Radio Frequency and Processing Components Thereof* (ITC Inv. No. 337-TA-1093) and *Qualcomm Inc. v. Apple Inc.*, Case No. 3:17-cv-02398 (S.D. Cal.). *Id.* at 64–65; Paper 3, 2. Patent Owner identifies a second *inter partes* review for the '674 patent: *Apple Inc. v. Qualcomm Inc.*, Case IPR2018-01316. Paper 3, 2.

C. The '674 Patent

The '674 patent is titled “Multiple Supply-Voltage Power-Up/Down Detectors.” Ex. 1001, [54]. According to the '674 patent, “many newer integrated circuit devices include dual power supplies: one lower-voltage power supply for the internally operating or core applications, and a second higher-voltage power supply for the I/O circuits and devices.” *Id.* at 1:22–25.

The '674 patent further states that “[i]n order to facilitate communication between the core and I/O devices, level shifters are employed.” *Id.* at 1:28–29. However, “[b]ecause the I/O devices are connected to the core devices through level shifters, problems may occur when the core devices are powered-down.” *Id.* at 1:29–32. An example of such a problem described in the '674 patent is how stray currents while the core is powering down can cause the level shifters to “send a signal to the I/O devices for transmission” resulting in the I/O devices “transmit[ting] the erroneous signal into the external environment.” *Id.* at 1:34–40.

One prior art solution identified in the '674 patent is the use of “power-up/down detectors to generate a power-on/off-control (POC) signal

internally [which] instructs the I/O devices when the core devices are shut down.” *Id.* at 1:55–58. Figure 1 of the ’674 patent is reproduced below.

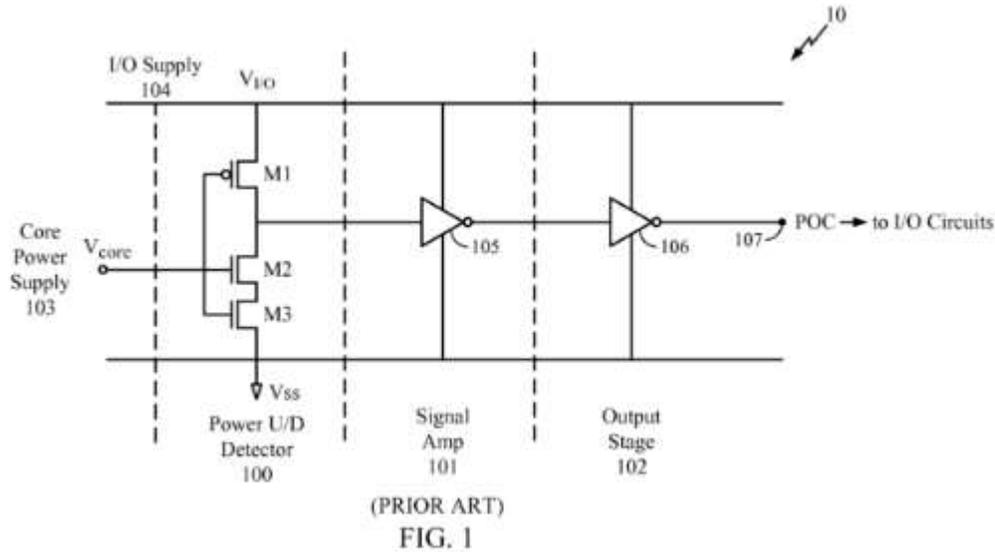


Figure 1 “is a circuit diagram illustrating a conventional POC system for multiple supply voltage devices” which is identified as being prior art. *Id.* at 4:18–19, Fig. 1.

The ’674 patent identifies a number of issues associated with the Figure 1 design. For example, when I/O power supply 104 is on and core power supply 103 is off, powering on the core power supply results in “a period in which all three transistors within power up/down detector 100 are on,” resulting a virtual short “to ground causing a significant amount of current to flow from I/O power supply 104 to ground.” *Id.* at 2:21–29. “This ‘glitch’ current consumes unnecessary power.” *Id.* at 2:29–30. Although the glitch current can be reduced by reducing the size of transistors M1-M3, such a reduction limits “the actual amount of current that can pass through the transistors” and reduces their switching speeds, which “translates into less sensitivity in detecting power-up/down of core supply

voltage 103 or longer processing time for power-up/down events.” *Id.* at 2:31–39; *see also id.* at 2:63–3:11.

According to the ’674 patent, these problems can be solved by using “one or more feedback circuits coupled to the up/down detector” that “are configured to provide feedback signals to adjust a current capacity of said up/down detector.” *Id.* at 3:31–34. An example of such a feedback circuit is shown in Figure 4, reproduced below:

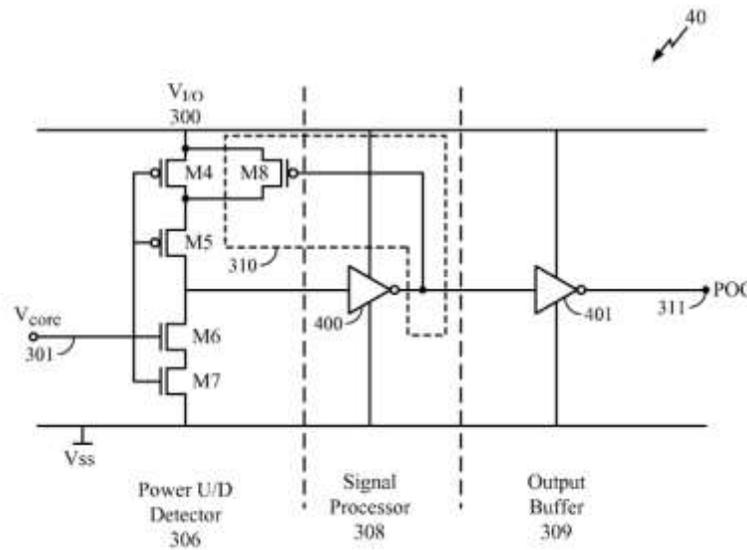


Figure 4 “is a circuit diagram illustrating another POC network configured according to the teachings of the present disclosure.” *Id.* at 4:28–30. The ’674 patent describes the operation of the feedback circuit in Figure 4 as follows:

The feedback network 310 comprises a transistor M8 connected in parallel to the transistor M4. The transistor M8 is also configured as a p-type transistor, such that when the feedback signal from the inverting amplifier 400 is high, the transistor M8 is switched off, and when the feedback signal is low, the transistor M8 is switched on. Thus, when the V_{core} 301 is off, producing a high detection signal, the inverting amplifier 400 inverts that signal to a logic low which causes the transistor M8 to switch on. As the V_{core} 301 is powered-on, the detection

signal changes to a logic low, which changes the feedback signal from the inverting amplifier 400 to a logic high, which, in turn, turns the transistor M8 off. While the transistor M8 is off, the power up/down detector 306 has a decreased current capacity, i.e., smaller current will flow through the transistor M8 because of the amplified low signal. The voltage level caused by the V_{core} 301 on the gate terminals of M4 and M5 could in some glitch or stray signal situations, cause leakage through M4 and M5. Because the feedback signal for the transistor M8 is received from the inverting amplifier 400, when the V_{core} 301 powers-down, the feedback signal will switch quickly from a logic high to a logic low, which will then switch the transistor M8 on. Thus, in the circuit configuration depicted in FIG. 4, the power up/down detector 40 will detect the V_{core} 301 powering down more quickly than the existing POC networks.

Id. at 6:4–28

D. The Challenged Claims

Petitioner challenges claims 1, 2, and 5–7 of the '674 patent. Pet. 1. Claim 1 is independent, is illustrative of the subject matter of the challenged claims, and reads as follows:

1. A multiple supply voltage device comprising:
 - a core network operative at a first supply voltage; and
 - a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state;
 - one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector;

at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on;

at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down;

at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor.

Ex. 1001, 8:44–9:3.

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

| Reference(s) | Basis ¹ | Challenged Claim(s) |
|---|--------------------|---------------------|
| Steinacker ² in view of Doyle ³ and Park ⁴ | § 103(a) | 1, 2, and 5–7 |
| AAPA ⁵ in view of Majcherczak ⁶ | § 103(a) | 1, 2, 5, and 6 |

¹ The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. § 103 that became effective on March 16, 2013. Because the ’674 patent issued from an application filed before March 16, 2013, we apply the pre-AIA versions of the statutory bases for unpatentability.

² U.S. Patent No. 7,279,943 B2 (issued Oct. 9, 2007) (Ex. 1005).

³ U.S. Patent No. 4,717,836 (issued Jan. 5, 1988) (Ex. 1006).

⁴ Jun Cheol Park and Vincent J. Mooney III, Sleepy Stack Leakage Reduction, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 14, No. 11, 1250–63 (Nov. 2006) (Ex. 1007).

⁵ Petitioner identifies Figure 1 and the text at column 1, line 22 through column 2, line 39 of the ’674 patent as Applicant Admitted Prior Art. *See* Pet. 37, 43, 46

⁶ U.S. Published Patent Application No. 2002/0163364 A1 (published Nov. 7, 2002) (Ex. 1008).

| Reference(s) | Basis ¹ | Challenged Claim(s) |
|---|--------------------|---------------------|
| AAPA in view of Majcherczak and Matthews ⁷ | § 103(a) | 7 |

Pet. 1. In its analysis, Petitioner relies on the declaration testimony of Robert W. Horst, Ph.D. (Ex. 1003) and Jacob Robert Munford (Ex. 1016).

II. ANALYSIS

A. Claim Construction

In this *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2016).⁸ “Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history.” *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016). In addition, the Board may not “construe claims during [an *inter partes* review] so broadly that its constructions are unreasonable under general claim construction principles.” *Microsoft Corp. v. Proxycor, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) (emphasis omitted). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with

⁷ U.S. Patent No. 6,646,844 B1 (issued Nov. 11, 2003) (Ex. 1009).

⁸ Per recent regulation, the Board will apply the *Phillips* claim construction standard to petitions filed on or after November 13, 2018. *See Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board*, 83 Fed. Reg. 51340 (Oct. 11, 2018) (to be codified at 37 C.F.R. pt. 42). Because Petitioner filed the Petition before November 13, 2018, we apply the BRI standard.

reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner proposes a claim construction for “processing circuitry.” Pet. 10. Having considered the evidence presented, we conclude that no express claim construction of any term is necessary for our determination of whether to institute review of the challenged claims. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”).

B. Legal Principles

Section 103(a) forbids issuance of a patent when “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when available, evidence such as commercial success, long felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *see KSR*, 550 U.S. at 407 (“While the sequence of these questions might be reordered in any particular case, the [Graham] factors continue to define the inquiry that controls.”). The Court in *Graham* explained that these factual inquiries promote “uniformity and definiteness,” for “[w]hat is obvious is not a

question upon which there is likely to be uniformity of thought in every given factual context.” 383 U.S. at 18.

The Supreme Court made clear that we apply “an expansive and flexible approach” to the question of obviousness. *KSR*, 550 U.S. at 415. Whether a patent claiming the combination of prior art elements would have been obvious is determined by whether the improvement is more than the predictable use of prior art elements according to their established functions. *Id.* at 417. To reach this conclusion, however, it is not enough to show merely that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). Rather, obviousness additionally requires that a person of ordinary skill at the time of the invention “would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention.” *Id.*

Moreover, in determining the differences between the prior art and the claims, the question under 35 U.S.C. § 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 164 (Fed. Cir. 1985) (“It is elementary that the claimed invention must be considered as a whole in deciding the question of obviousness.” (citation omitted)); *see also Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537 (Fed. Cir. 1983) (“[T]he question under 35 U.S.C. § 103 is not whether the differences themselves would have been obvious. Consideration of differences, like each of the findings set forth in *Graham*, is but an aid in reaching the ultimate determination of whether the claimed invention as a whole would have been obvious.” (citation omitted)).

“A reference must be considered for everything it teaches by way of technology and is not limited to the particular *invention* it is describing and attempting to protect.” *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985). Additionally, “the question under 35 USC § 103 is not merely what the references expressly teach but what they would have suggested to one of ordinary skill in the art at the time the invention was made.” *Merck & Co. v. Biocraft Laboratories, Inc.*, 874 F.2d 804, 807–08 (Fed. Cir. 1989) (quoting *In re Lamberti*, 545 F.2d 747, 750 (CCPA 1976)). “Every patent application and reference relies to some extent upon knowledge of persons skilled in the art to complement that [which is] disclosed” *In re Bode*, 550 F.2d 656, 660 (CCPA 1977) (quoting *In re Wiggins*, 488 F.2d 538, 543 (CCPA 1973)). Those persons “must be presumed to know something” about the art “apart from what the references disclose.” *In re Jacoby*, 309 F.2d 513, 516 (CCPA 1962).

As a factfinder, we also must be aware “of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning.” *KSR*, 550 U.S. at 421. This does not deny us, however, “recourse to common sense” or to that which the prior art teaches. *Id.*

Against this general background, we consider the references, other evidence, and arguments on which the parties rely.

C. Level of Ordinary Skill in the Art

The level of ordinary skill in the art is “a prism or lens” through which we view the prior art and the claimed invention. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Factors pertinent to a determination of the “level of ordinary skill in the art include (1) educational level of the inventor; (2) type of problems

encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of workers active in the field.” *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case. *Id.* Moreover, “[t]hese factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art.” *Daiichi Sankyo Co. Ltd, Inc. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007). In determining a level of ordinary skill, we also may look to the prior art, which may reflect an appropriate skill level. *Okajima*, 261 F.3d at 1355. Additionally, the Supreme Court informs us that “[a] person of ordinary skill is also a person of ordinary creativity, not an automaton.” *KSR*, 550 U.S. at 421.

Dr. Horst testifies that a person having ordinary skill in the art would have had “at least an undergraduate degree in electrical engineering, or a related field, and three years of experience in circuit and system design.” Ex. 1003 ¶ 33. Additionally, Dr. Horst testifies that “a person of ordinary skill with less than the amount of experience noted above could have had a correspondingly greater amount of educational training such a graduate degree in a related field.” *Id.*

Patent Owner does not dispute that definition in its Preliminary Response. Additionally, Patent Owner does not rely on any testimonial evidence on the level of ordinary skill in the art.

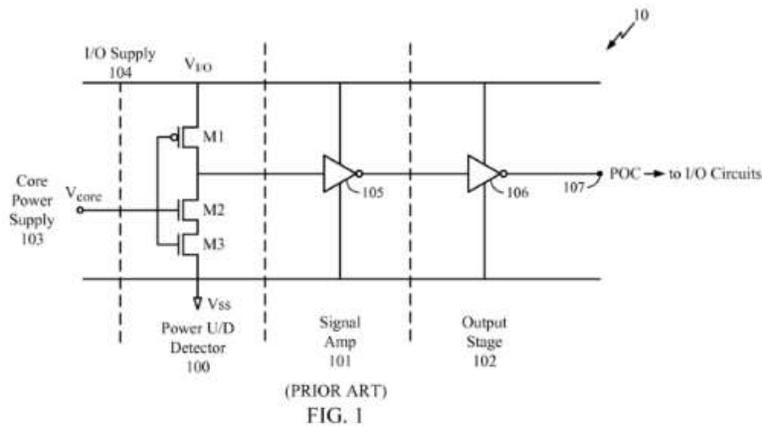
Accordingly, we adopt Dr. Horst’s definition of the level of ordinary skill in the art, with the exception of the language “at least,” for purposes of this Decision.⁹

D. Obviousness over AAPA in View of Majcherczak

Petitioner argues the subject matter of claims 1, 2, 5, and 6 would have been obvious to a person of ordinary skill in the art at the time of the invention in light of the teachings of AAPA in view of Majcherczak (Ex. 1008). Based on the current record, we are persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted obviousness ground with respect to claims 1, 2, 5, and 6.

1. Summary of AAPA

The ’674 patent describes a prior art “power-up/down detector[] to generate a power-on/off-control (POC) signal internally.” Ex. 1001, 1:55–57, Fig. 1. The prior art design is shown in Figure 1, reproduced below.



⁹ If Patent Owner proposes a different level of ordinary skill in the art in the Patent Owner’s Response, the parties are encouraged to address whether there are any material differences between the two proposals and what impact, if any, the different level has on the obviousness analysis.

Id. at Fig. 1. “FIG. 1 is a circuit diagram illustrating a conventional POC system for multiple supply voltage devices” and is identified as prior art. *Id.* at 4:18–19, Fig. 1. According to the ’674 patent, the POC “is made up of three functional blocks: power-up/down detector 100, signal amplifier 101, and output stage 102. Power-up/down detector 100 has PMOS transistor M1 and NMOS transistors M2-M3.” *Id.* at 1:60–63.

2. Summary of Majcherczak

Majcherczak is titled “Power Supply Detection Device” and relates “to a power supply detection device for an integrated circuit using at least two power supply voltages.” Ex. 1008, [54], ¶ 1. Majcherczak describes a voltage detection device that detects when the core voltage is powered down or there is an excessively slow build-up of the voltage. *Id.* at [57], ¶¶ 8–11.

Figure 2 of Majcherczak is shown below.

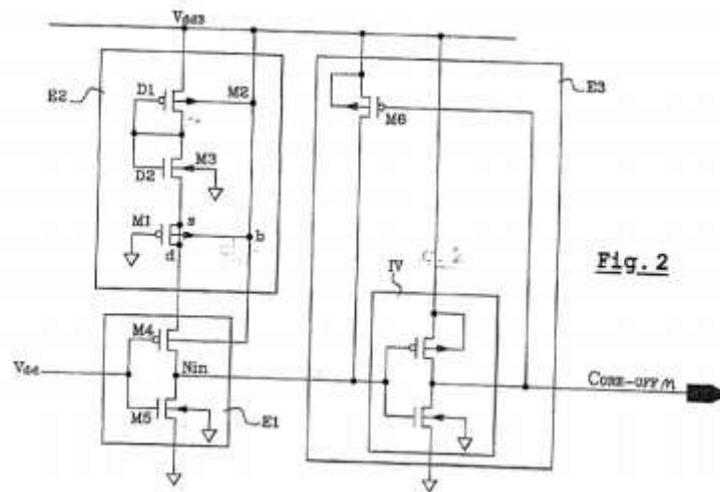
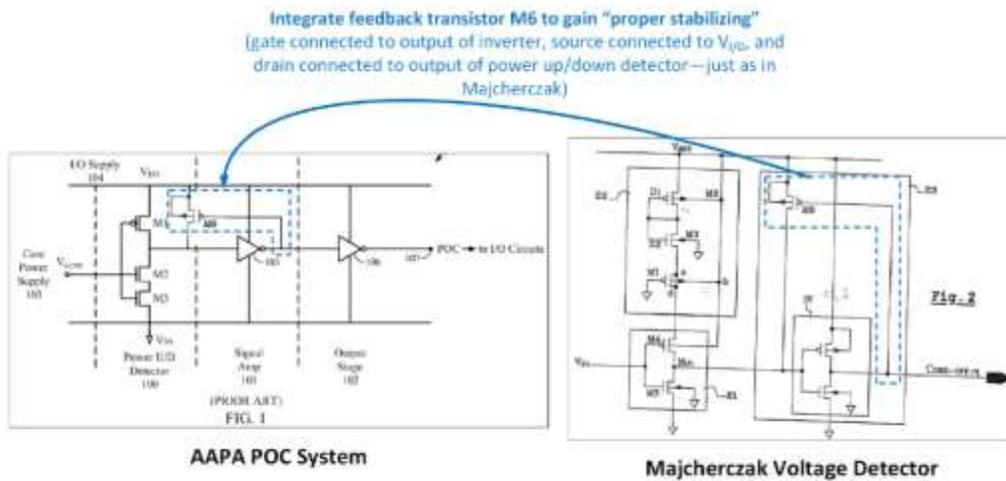


Figure 2 shows a detection device “compris[ing] an output stage E3 following the input stage E1, to obtain the desired output levels for the inverse detection signal CORE-OFFn.” *Id.* ¶¶ 35–37

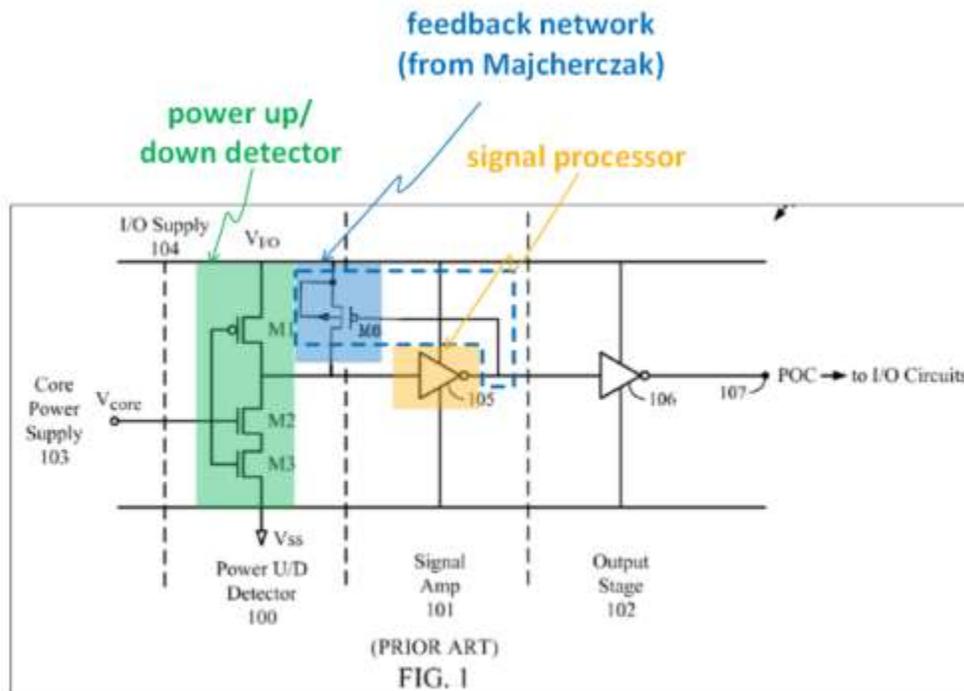
3. Claim 1

a. Petitioner's Arguments

Petitioner argues that the combination of AAPA and Majcherczak teaches all of the limitations recited in claim 1. See Pet. 37–56. Specifically, Petitioner argues a person of ordinary skill in the art would have combined the feedback circuit of Majcherczak with the POC described in AAPA as shown in the annotated figure reproduced below.



Id. at 44. The figure reproduced above shows Majcherczak's Figure 2 annotated by Petitioner (right) and a version of Figure 1 of the '674 patent (AAPA) modified by Petitioner to integrate the feedback transistor M6 from Majcherczak's Figure 2 (left). *Id.* Petitioner also provides a differently annotated version of its proposed combination (*id.* at 50) as reproduced below.



AAPA + Majcherczak POC System

The figure above shows what Petitioner contends is the combination of the feedback network of Majcherczak with the POC of AAPA. *Id.* Petitioner's annotations show what Petitioner argues is the power up/down detector in green, the signal processor in yellow, and the feedback network from Majcherczak in blue. *Id.*

Petitioner argues AAPA in combination with Majcherczak teaches “[a] multiple supply voltage device” as recited in claim 1. *Id.* at 46. According to Petitioner, “AAPA describes that the prior art POC system 10 is useful in ‘newer integrated circuit devices include dual power supplies: one lower-voltage power supply for the internally operating or core applications, and a second higher-voltage power supply for the I/O circuits and devices.’” *Id.* (quoting Ex. 1001, 1:22–25).

Petitioner also argues AAPA in combination with Majcherczak teaches “a core network operative at a first supply voltage” as recited in claim 1. *Id.* at 46–47. Specifically, Petitioner argues AAPA includes power up/down detector 100 which is connected to the core power supply, which is a “lower-voltage power supply for the internally operating or core applications.” *Id.* (citing Ex. 1001, 1:22–25, 1:60–64).

Petitioner further argues AAPA in combination with Majcherczak teaches “a control network coupled to said core network wherein said control network is configured to transmit a control signal” as recited in claim 1. *Id.* at 47. Specifically, Petitioner argues “[t]he prior art power-on/off-control (POC) system 10 is a control network coupled to said core network (via core power supply V_{core}), and the POC system 10 is configured to transmit a power-on/off-control (POC) signal 107.” *Id.* at 47 (citing Ex. 1001, 1:55–58, 1:65–2:13).

Petitioner also argues AAPA in combination with Majcherczak teaches “said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state” as recited in claim 1. *Id.* at 48–49. Specifically, Petitioner directs us to a comparison of Figure 4 of the ’674 patent and the combination of AAPA and Majcherczak, both of which show a power/up down detector and a signal amplifier portion. *Id.* at 48. Petitioner further argues that “[t]he signal amplifier 101 and output stage 102 are processing circuitry coupled to said up/down detector and configured to generate the power-on/off-control (POC) signal 107 based on said power state.” *Id.* at 49.

Petitioner argues the combination of AAPA and Majcherczak teaches “one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/ down detector” as recited in claim 1. *See id.* at 49–52. Specifically, Petitioner argues that when the teachings of AAPA and Majcherczak are combined as shown in the figure reproduced above, “the feedback transistor M6 is a feedback circuit coupled to the up/down detector 100 via its output.” *Id.* at 51 (citing Ex. 1003 ¶ 141); *see also id.* at 51–52 (citing Ex. 1003 ¶¶ 142–143). That is, according to Petitioner, “when both transistors M1 and M6 are ‘on’ (i.e., V_{core} is off), the transistor M6 increases the current capacity of the power up/down detector 100” but “when both transistors M1 and M6 are ‘off’ (i.e., V_{core} is on), the transistor M6 decreases the current capacity of the power up/down detector 100.” *Id.* (citing Ex. 1003 ¶¶ 142–143).

Petitioner also argues that AAPA in combination with Majcherczak teaches “at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on” as recited in claim 1. *See id.* at 52–53. More specifically, Petitioner argues M1—a first transistor—is coupled to $V_{\text{I/O}}$ —the I/O power supply or second supply voltage. *Id.* (citing Ex. 1003 ¶ 141; Ex. 1001, 1:62–2:1, 2:8–9). Petitioner further argues that “AAPA explains that the transistor M1 is configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on.” *Id.* at 53 (citing Ex. 1001, 1:65–67, 2:8–9).

Petitioner further argues that AAPA in combination with Majcherczak teaches “at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down” as recited in claim 1. *See* Pet. 54–55. More specifically, Petitioner argues transistor M3 is a second transistor and “AAPA explains that the transistor M3 is configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on.” *Id.* (citing Ex. 1003 ¶¶ 141, 144–147; Ex. 1001, 1:65–67, 2:8–9).

Petitioner also argues that AAPA in combination with Majcherczak teaches “at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor” as recited in claim 1. *Id.* at 55–56. Specifically, Petitioner points us to transistor M2,¹⁰ which, according to Petitioner, “is coupled in series between transistor M1 (i.e., the first transistor) and transistor M3 (i.e., the second transistor).” *Id.* at 56 (citing Ex. 1003 ¶ 144).

Finally, Petitioner argues that a person of ordinary skill in the art “would have been motivated to integrate the feedback transistor M6 from Majcherczak’s voltage detector into the POC system 10 of AAPA in order to ‘enable[] the proper stabilizing of the detection device.’” *Id.* at 45 (quoting

¹⁰ The Petition interchangeably refers to transistor M2 and M3 as the third transistor. Pet. 56. However, the Petition specifically refers to the transistor highlighted in brown, which is transistor M2. We treat the reference to transistor M3 as a typographical error.

Ex. 1008 ¶ 37) (citing Ex. 1003 ¶ 150). According to Petitioner, the “combination would result in AAPA’s POC system 10 observing the ‘hysteresis detection’ described by Majcherczak, facilitating controlled operation of the I/O devices instructed by the POC signal on communications from the core devices when the core supply voltage is stably on.” *Id.* (citing Ex. 1003 ¶ 150). Moreover, according to Petitioner, a person of ordinary skill in the art would have a reasonable expectation of success:

A POSITA would have perceived a reasonable expectation of success in making this modification to the POC system 10 of AAPA, because the POC system 10 and Majcherczak’s voltage detector share many functionally commensurate elements, operate in a corresponding manner, and are used in the similar types of multiple supply voltage devices. [Ex. 1003] ¶ 151. Indeed, the integration of the feedback transistor M6 from Majcherczak’s voltage detector would have simply been the use of a known technique (a feedback transistor to improve hysteresis) to improve similar devices (detection circuits in multiple supply voltage devices) in the same way. *Id.*

Id.

b. Patent Owner’s Arguments

Patent Owner does not dispute Petitioner’s contention that claim 1 would have been obvious to a person of ordinary skill in the art in over the combination of AAPA and Majcherczak. *See* Prelim. Resp. 27–35. Instead, Patent Owner argues (1) that we should exercise our discretion and deny institution on the basis of 35 U.S.C. § 325(d) and (2) that we cannot consider applicant admitted prior art during an *inter partes* review.

Specifically, Patent Owner argues that the Examiner was required to review and consider the specification, including AAPA. *Id.* at 28. Patent

Owner further argues the Examiner not only considered Majcherczak, but the Examiner also considered “an [International Search Report (ISA)] and Written Opinion of the International Searching Authority that provided a detailed discussion of how Majcherczak allegedly reads on the claims.” *Id.* According to Patent Owner, “because the Office considered both the alleged AAPA and Majcherczak and found the claims to be patentable over them,” we should exercise our discretion and deny institution. *Id.* at 29–34.

Additionally, Patent Owner argues because “[n]either the alleged AAPA nor the ’674 Patent containing it qualifies as a prior art patent or printed publication,” we should deny institution on the grounds based on AAPA. *Id.* at 34–35. According to Patent Owner, “PTAB panels have previously held that AAPA does not qualify as prior art under Section 311(b).” *Id.* at 35 (citing *LG Elecs., Inc. v. Core Wireless Licensing S.A.R.L.*, IPR2015-01987, Paper 7 at 18 (PTAB Mar. 24, 2016); *Sony Corp. v. Collabo Innovations, Inc.*, IPR2016-00940, Paper 7 at 30 (PTAB Oct. 24, 2016)).

c. Our Analysis

(1) Applicant Admitted Prior Art

As a preliminary matter, we disagree with Patent Owner that we cannot consider applicant admitted prior art during an *inter partes* review. In considering Federal Circuit precedent and our rules, we conclude that a petition for an *inter partes* review can rely on applicant admitted prior art in combination with a prior art patent or printed publication. *Cf. In re Nomiya*, 509 F.2d 566, 570–71 (CCPA 1975) (“We see no reason why appellants’ representations in their application should not be accepted at face value as admissions that Figs. 1 and 2 may be considered ‘prior art’ for any purpose,

including use as evidence of obviousness under § 103. . . . By filing an application containing Figs. 1 and 2, labeled prior art, *ipsissimis verbis*, and statements explanatory thereof appellants have conceded what is to be considered as prior art in determining obviousness of their improvement.”). That conclusion is consistent with other decisions in *inter partes* review proceedings that addressed a near identical circumstance as we do here. *See, e.g., One World Techs., Inc. v. Chamberlain Group, Inc.*, IPR2017-00126, slip op. at 9–10 (May 4, 2017) (Paper 8) (holding that “a patentee’s admission made in a challenged patent is literally ‘prior art consisting of patents’ as required by 35 U.S.C. § 311(b)”). We share the same view as the Panel in *One World* that such a conclusion is consistent with the statutory language and the holding in *Nomiya*.

Because we determine applicant admitted prior art is “prior art consisting of patents,” the request falls within the scope of 35 U.S.C. § 311(b).

(2) Discretion Under 35 U.S.C. § 325(d)

Institution of *inter partes* review is discretionary. *Harmonic Inc. v. Avid Tech, Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (holding “the PTO is permitted, but never compelled, to institute an IPR proceeding”). Moreover, 35 U.S.C. § 325(d) provides, in relevant part: “In determining whether to institute or order a proceeding under this chapter, chapter 30, or chapter 31, the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.”

“While petitioners may have sound reasons for raising art or arguments similar to those previously considered by the Office, the Board

weighs petitioners’ desires to be heard against the interests of patent owners, who seek to avoid harassment and enjoy quiet title to their rights.” *Neil Ziegman, N.P.Z., Inc. v. Stephens*, Case IPR2015-01860, slip op. at 12–13 (PTAB Feb. 24, 2016) (Paper 11) (citing H. Rep. No. 112-98, pt. 1, at 48 (2011)). “On the one hand, there are the interests in conserving the resources of the Office and granting patent owners repose on issues and prior art that have been considered previously.” *Fox Factory, Inc. v. SRAM, LLC*, Case IPR2016-01876, slip op. at 7 (PTAB Apr. 3, 2017) (Paper 8). “On the other hand, there are the interests of giving petitioners the opportunity to be heard and correcting any errors by the Office in allowing a patent—in the case of an *inter partes* review—over prior art patents and printed publications.” *Id.*

The Board considers the following non-exclusive factors in determining whether to deny institution under 35 U.S.C § 325(d):

- (1) the similarities and material differences between the asserted art and the prior art involved during examination;
- (2) the cumulative nature of the asserted art and the prior art evaluated during examination;
- (3) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
- (4) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
- (5) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
- (6) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Office Patent Trial Practice Guide Update (“Trial Practice Guide Update”) referenced at 83 Fed. Reg. 39,989 (Aug. 13, 2018) at 12, 13 (citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, Case IPR2017-01586, slip op.

at 17–18 (PTAB Dec. 15, 2017) (Paper No. 8) (footnote omitted) (informative)).

We turn first to the extent of the Examiner’s prior consideration of the prior art. As pointed out by Patent Owner, Examiners are supposed to review the complete specification. *See* MPEP 2103, 2129; Prelim. Resp. 29. Additionally, as noted by Patent Owner, Majcherczak was included on an IDS mailed on September 8, 2010, which the Examiner initialed on February 11, 2011. *See* Ex. 1002, 125–26 (initialed version), 166–68 (submitted version). Similarly, a search report for a related PCT application that cited Majcherczak as an “X” reference—“document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone”—was also included in an IDS that was signed by the Examiner. *See id.* at 30, 47–59.

However, as Patent Owner acknowledges, neither AAPA nor Majcherczak—let alone the two of them combined—was used to reject claims in the application issuing as the ’674 patent. *See* Prelim. Resp. 33. The fact that neither AAPA nor Majcherczak was the basis of rejection weighs strongly against exercising our discretion to deny under 35 U.S.C. § 325(d). *See* Trial Practice Guide Update at 12, 13 (considering six nonexclusive factors in deciding whether to deny institution under § 325(d), including “(c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis of rejection”); *Kayak Software Corp. v. Int’l Bus. Machs. Corp.*, Case CBM2016-00075, Paper 16 at 11 (PTAB Dec. 15, 2016) (informative) (stating that “[t]here could be situations where, for example, the prosecution is not as exhaustive, where there are clear errors in the original prosecution, *or where the prior*

art at issue was only cursorily considered that can weigh against exercising the discretion” under § 325(d) (emphasis added)).

Although Patent Owner points to a search report from an international search report identifying Majcherczak as an X reference and providing a “[r]easoned statement with regard to novelty” (Ex. 1002, 56–57), the search report by itself does not demonstrate the extent to which the Examiner considered the reference. Nor does the search report demonstrate that the Examiner considered the combination of AAPA and Majcherczak as relied on in the Petition.

Additionally, neither of the cases cited by Patent Owner involves a situation where the PTAB denied institution under 35 U.S.C. § 325(d) on the basis of only prior art merely listed in an IDS but not used as the basis of a rejection. *See* Prelim. Resp. 29–30 (citing *R.J. Reynolds Vapor Co. v. Fontem Holdings I B.V.*, IPR2017-01642, slip op. at 12 (PTAB Jan. 16, 2018) (Paper 10); *Benitec Biopharma Ltd. v. Cold Spring Harbor Lab.*, IPR2016-00014, slip op. at 10 (PTAB Mar. 23, 2016) (Paper 7)).

In *R.J. Reynolds*, the Panel found that Whittemore, one of the references relied on in the petition, was both listed on an IDS signed by the Examiner and used by the Examiner to reject the pending claims. *R.J. Reynolds*, slip op. at 13–14. Because the facts in *R.J. Reynolds* are distinguishable from those here, we do not reach the same conclusion as the panel in that proceeding.

Moreover, *Benitec* did not even involve an analysis under section 325(d); instead, trial was not instituted because the petitioner failed to demonstrate a reasonable likelihood of success. *Benitec*, slip op. at 24.

Because the Examiner relied on neither AAPA nor Majcherczak to reject the claims during prosecution, we decline to exercise our discretion under 35 U.S.C. § 325(d) to deny institution.

(3) Whether Claim 1 Would Have Been Obvious

After reviewing Petitioner's arguments and information, including the Horst Declaration, which are unchallenged by Patent Owner at this stage, we are persuaded that Petitioner sufficiently demonstrates how the combination of AAPA and Majcherczak teaches each of the limitations recited in claim 1 and that a person of ordinary skill in the art had a reason to combine the teachings of the references with a reasonable expectation of success. Accordingly, Petitioner has demonstrated, on this record, a reasonable likelihood of prevailing on its assertion that claim 1 is obvious over AAPA in view of Majcherczak.

4. *Claims 2, 5, and 6*

Because Petitioner has demonstrated a reasonable likelihood of success in proving that at least one claim of the '674 patent is unpatentable, we will institute on all grounds and all claims raised in the Petition. *See SAS*, 138 S. Ct. at 1359–60 (holding an *inter partes* review may not institute on less than all claims challenged in the petition); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (indicating that a decision whether to institute an *inter partes* review “require[s] a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”). Therefore, at this stage of the proceeding, it is not necessary for us to provide an assessment of every ground raised by Petitioner.

Nevertheless, we note that Petitioner provides detailed explanations supported by the testimony of Dr. Horst and specific citations to AAPA and Majcherczak indicating where in the references the limitations of claims 2, 5, and 6 are taught. Pet. 57–62. We have reviewed Petitioner’s contentions as to claims 2, 5, and 6 and find them persuasive on this record.

At this stage of the proceeding, we are persuaded that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail with respect to claims 2, 5, and 6.

E. Obviousness over AAPA, Majcherczak, and Matthews

Petitioner argues the subject matter of claim 7 would have been obvious to a person of ordinary skill in the art at the time of the invention in light of the teachings of AAPA in view of Majcherczak and Matthews (Ex. 1009). Based on the current record, we are persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted obviousness ground with respect to claim 7.

1. Overview of Matthews

Matthews is titled “Apparatus for Power-on Disable in a Multiple Power Supply System and a Method Therefor” and is directed “to a system such as an embedded system that has multiple power supplies that are synchronized during initialization of the system.” Ex. 1009, [54], 1:9–12. More specifically, Matthews teaches an apparatus “for disabling portions of a system, circuit, etc. having multiple power supplies,” which provides the advantages of disabling “certain portions of a system” “during system power-on or other times when power supply voltage levels may be changing,” in order to prevent those portions “from generating erroneous data.” *Id.* at 1:63–2:10.

2. *Claim 7*

As noted above, because Petitioner has demonstrated a reasonable likelihood of success in proving that at least one claim of the '674 patent is unpatentable, we will institute on all grounds and all claims raised in the Petition. Therefore, at this stage of the proceedings, it is not necessary for us to provide an assessment of every ground raised by Petitioner.

Nevertheless, we note that Petitioner provides detailed explanations supported by the testimony of Dr. Horst and specific citations to AAPA, Majcherczak, and Matthews indicating where in the references the limitations of claim 7 are taught and why a person of ordinary skill in the art would have combined the teachings of the references. *See* Pet. 62–64. We further note that Patent Owner does not argue in the Preliminary Response that the prior art does not teach the limitations of claim 7 or that a person of ordinary skill in the art would not have combined the references in the manner asserted in the Petition. *See* Prelim Resp. 27–35. We have reviewed Petitioner's contentions as to claim 7 and find them persuasive on this record.

At this stage of the proceeding, we are persuaded that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail with respect to claim 7.

F. Obviousness over Steinacker, Doyle, and Park

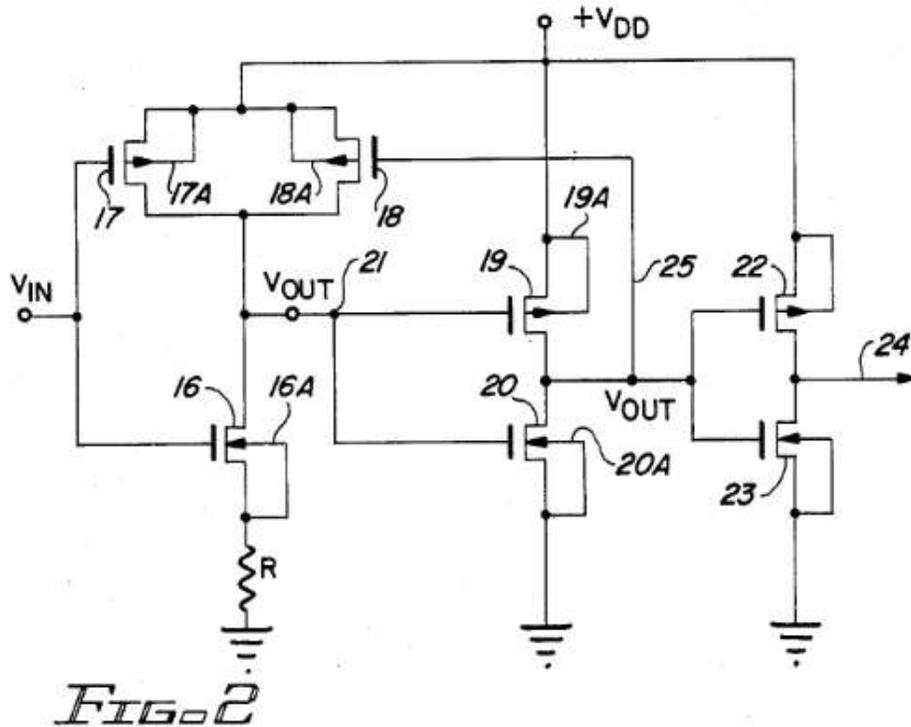
Petitioner argues the subject matter of claims 1, 2, and 5–7 would have been obvious to a person of ordinary skill in the art at the time of the invention in light of the teachings of Steinacker (Ex. 1005) in view of Doyle (Ex. 1006) and Park (Ex. 1007).

1. *Overview of Steinacker*

Steinacker is titled “Circuit Arrangement Receiving Different Supply Voltages” and is directed to a circuit arrangement including a first circuit block operating at a first supply voltage and second circuit block operating at a second supply voltage. Ex. 1005, [54], [57]. According to Steinacker, such an arrangement is frequently used in mobile radio technology. *Id.* at 1:18–29.

2. *Overview of Doyle*

Doyle is titled “CMOS Input Level Shifting Circuit with Temperature-Compensating N-Channel Field Effect Transistor Structure” and is directed “to temperature-compensated field effect transistor circuits and to inverting CMOS circuits having trip points or switching points that are compensated for variations in temperature and are relatively independent of certain manufacturing process parameter variations.” Ex. 1006, [54], 1:7–13. Doyle’s Figure 2 is reproduced below.



Id. at Fig. 2. Figure 2 “is a schematic circuit diagram of a self adjusting TTL [(transistor-transistor logic)] compatible input circuit according to the present invention.” *Id.* at 3:35–37. According to Doyle, an “object of the invention [is] to provide a MOSFET circuit structure that, in effect, produces a MOSFET drain current having a predetermined amount or range of variation with respect to temperature and/or certain MOS processing parameters.” *Id.* at 2:32–36.

3. Park

Park is titled “Sleepy Stack Leakage Reduction” and is directed to an “ultra-low leakage CMOS circuit structure” that “can retain logic state during sleep mode while achieving ultra-low leakage power consumption.” Ex. 1007, 1250. According to Park, “[a]lthough the sleepy stack incurs some delay and area overhead, the sleepy stack technique achieves the lowest leakage power consumption among known state-saving leakage

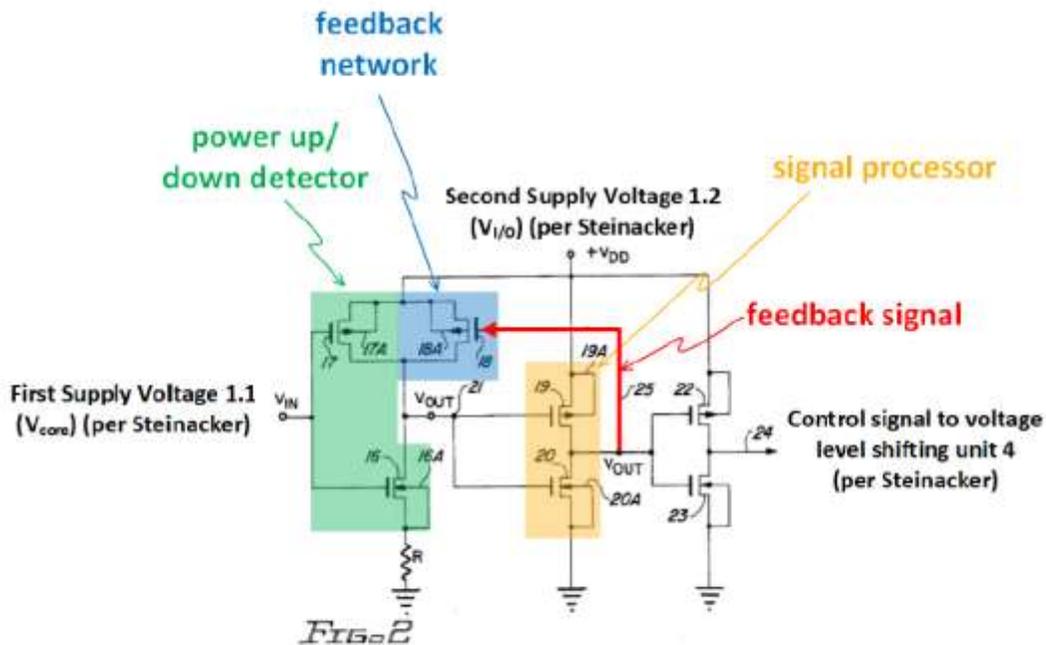
reduction techniques, thus, providing circuit designers with new choices to handle the leakage power problem.” *Id.*

Park briefly mentions the forced stack technique, an older technique “to reduce leakage power.” *Id.* at 1251. According to Park, the “sleepy stack structure can achieve more power savings than the forced stack technique and the self-controlled stacked transistors” and “can save exact logic state unlike gated- V_{dd} and gated-Gnd techniques (conventional sleep transistor technique) and the zigzag technique.” *Id.*

4. *Claims 1, 2, and 5–7*

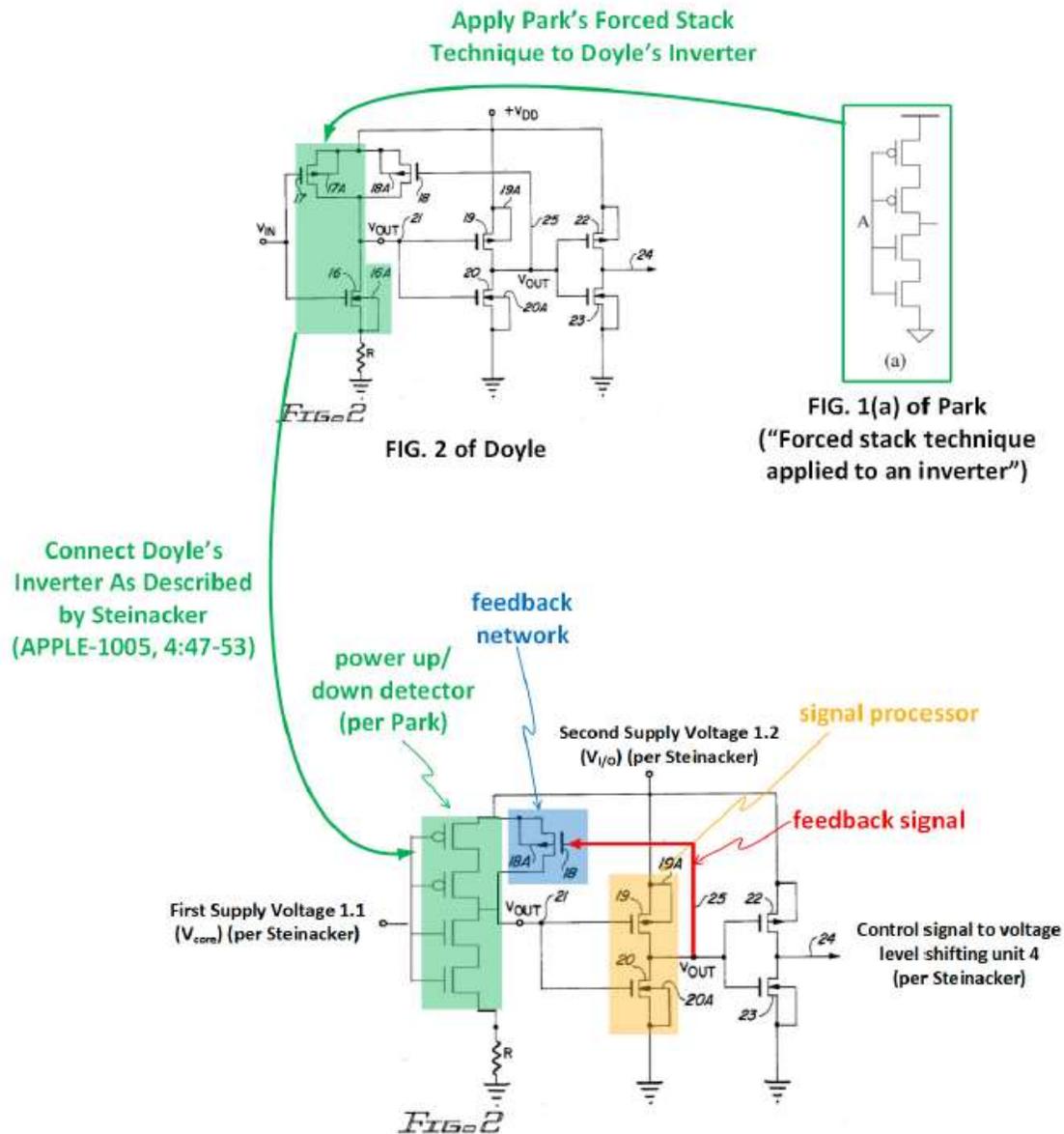
a. *Petitioner’s Arguments*

Petitioner argues that the combination of Steinacker, Doyle, and Park teaches all of the limitations of claims 1, 2, and 5–7. Pet. 11–37. Specifically, Petitioner argues that a person of ordinary skill in the art “would have found it obvious that the voltage detector 5 of Steinacker’s circuit arrangement 1 to be implemented as shown in the following reproduction of Doyle’s FIG. 2 in which black annotations describing how the inverter would be connected in the circuit arrangement have been added.” Pet. 18



Id. at 19. According to Petitioner, the figure above shows the combination of the teachings of Steinacker—the first supply voltage, the second supply voltage, and the control signal to voltage shifting unit 4—with the Figure 2 embodiment of Doyle. *Id.* at 18–19. Additionally, the figure has been annotated by Petitioner to identify what Petitioner argues are various claim limitations, such as the power up/down detector, the feedback network, the signal processor, and the feedback signal. *Id.*

Petitioner further argues that a person of ordinary skill in the art would have employed “Park’s forced stacking technique in the inverter taught by Doyle” so “that the P channel MOSFET 17 of Doyle’s inverter could be replaced by two P channel MOSFET’s having half the size and the N channel MOSFET 16 of Doyle’s inverter could be replaced by two N channel MOSFET’s having half the size.” *Id.* at 19. The figure reproduced below illustrates Petitioner’s combination.



Id. at 20. According to Petitioner, the figure reproduced above shows Park's Figure 1(a), which shows the forced stack technique applied to an inverter, Doyle's Figure 2, and a modified version of Doyle's Figure 2 showing the application of the forced stack technique applied to transistors 17 and 18. *Id.*

Petitioner further argues that "Steinacker describes that the voltage level detector 5 of circuit arrangement 1 can take the form of an inverter, but

leaves selection of an appropriate inverter to a POSITA.” *Id.* at 21 (citing Ex. 1003 ¶¶ 93, 103; Ex. 1005 4:49–55). Petitioner further argues that because “Doyle describes that its inverter ‘has a trip point that is relatively stable with respect to temperature and/or to certain CMOS manufacturing process parameters,’ particularly as compared to the basic well-known CMOS inverter shown in FIG. 2A,” a person of ordinary skill in the art would have used the inverter shown in Doyle’s Figure 2 with Steinacker. *Id.* (citing Ex. 1003 ¶ 108; Ex. 1006, 2:37–40, 5:60–61). Petitioner further argues that the combination “would have been simple substitution of one known element (basic well-known CMOS inverter) for another (Doyle’s improved inverter) to obtain predictable results.” *Id.* (citing Ex. 1003 ¶ 108).

Petitioner further argues that a person of ordinary skill in the art would have used the forced stack technique of Park with the Doyle inverter in order to reduce the subthreshold leakage current. *Id.* at 21–22 (citing Ex. 1003 ¶ 112). Petitioner also argues that “using Park’s forced stack technique would have been simple substitution of one known element (a two-transistor inverter) for another (a four-transistor inverter) to obtain predictable results (improve leakage current).” *Id.* at 22 (citing Ex. 1003 ¶ 112).

b. Patent Owner’s Arguments

Patent Owner argues Petitioner has failed to demonstrate a reason to combine the teachings of Steinacker, Doyle, and Park. Prelim. Resp. 16–27.

First, Patent Owner argues Petitioner is relying on an improper hindsight reconstruction. *Id.* at 16–24. Specifically, Patent Owner argues that “[i]nstead of starting with a relevant primary reference and explaining why the person of ordinary skill in the art would have been motivated to

modify that reference to derive the claimed invention, the Petitioner pieces together a hypothetical ‘prior art’ circuit from three entirely unrelated references.” *Id.* at 16–17. Patent Owner further argues that none of the references “disclose an up/down detector” and, therefore, “the petition must rely on impermissible hindsight reconstruction in its attempt to show motivation to combine the references into something resembling the claimed invention.” *Id.* at 17. Patent Owner also points out that Petitioner’s hypothetical circuit does not contain a single element from Steinacker, the primary reference, and that none of the references is directed to the same problem as the ’674 patent. *Id.* at 17–22; *see also id.* at 23–24 (arguing Doyle is actually the primary reference). Patent Owner also argues because neither Steinacker nor Doyle discuss problem with leakage, there was no reason to modify Doyle’s solution using the teaching of Park. *Id.* at 22–23.

Second, Patent Owner argues Park teaches away for Petitioner’s combination. *See id.* at 24–25. Specifically, Patent Owner argues that even if a person of ordinary skill in the art would have been motivated to use Park to lower leakage current, the person of ordinary skill in the art “would have used the superior ‘sleepy stack’ technique that is the focus of Park.” *Id.* at 24 (citing Ex. 1007). According to Patent Owner, Park teaches that the sleepy stack technique is superior to the forced stack technique Petitioner relies on. *Id.* at 24–25 (citing Ex. 1007, 1250–51).

Third, Patent Owner argues Petitioner “fails to provide the required ‘articulated reasoning with some rational underpinning’ and instead makes arguments that are generic and not tailored to the references being applied.” *Id.* at 25. Specifically, Patent Owner argues Petition does not address any of the disadvantages associated with the combination or explain why Park’s

forced stacking technique is only applied to some FETs. *Id.* at 25–26. Similarly, Patent Owner argues Petitioner’s reasoning regarding Doyle “is not tailored to the references under consideration and provides no explanation of why a stable trip point would be desirable in Steinacker” nor does it address why a person of ordinary skill in the art “would look to a CMOS-TTL interface, much less one aimed at compensating for changes in temperature, to provide an inverter in Steinacker’s system that includes no TTL components.” *Id.* at 26.

c. Our Analysis

As noted above, because Petitioner has demonstrated a reasonable likelihood of success in proving that at least one claim of the ’674 patent is unpatentable, we will institute on all grounds and all claims raised in the Petition. Therefore, at this stage of the proceedings, it is not necessary for us to provide an assessment of every ground raised by Petitioner.

However, in order to provide guidance to the parties, we address Patent Owner’s argument that the Petition fails to provide a sufficient reason to combine the references. For the reasons given below, based on the current record, we question the sufficiency of Petitioner’s evidence.

It is Petitioner’s “burden to demonstrate both that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) (quotations omitted); *see also KSR*, 550 U.S. at 418. Moreover, a petitioner cannot satisfy this burden by “employ[ing] mere conclusory statements” and “must instead articulate specific reasoning, based on evidence of record” to

support an obviousness determination. *Magnum Oil*, 829 F.3d at 1380. Stated differently, there must be “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

The “factual inquiry” into the reasons for “combin[ing] references must be thorough and searching, and the need for specificity pervades” *In re Nuvasive, Inc.*, 842 F.3d 1376, 1381–82 (Fed. Cir. 2016) (quotations omitted). The reason cannot focus on generic statements divorced from the prior art elements, such as the generic desire to “build something better” or to make it “more efficient, cheaper, or . . . more attractive to your customers.” *ActiveVideo Networks, Inc. v. Verizon Cooms, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012). A determination of obviousness cannot be reached where the record lacks “explanation as to *how* or *why* the references would be combined to produce the claimed invention.” *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1066 (Fed. Cir. 2016); *see Nuvasive*, 842 F.3d at 1382–86 (holding that an obviousness determination cannot be reached where there is no “articulat[ion of] a *reason why* a [person having ordinary skill in the art] would combine” and “modify” the prior art teachings). This required explanation as to why the references would be combined avoids an impermissible “hindsight reconstruction,” using “the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit.” *TriVascular*, 812 F.3d at 1066; *see also In re NTP, Inc.*, 654 F.3d 1279, 1299 (Fed. Cir. 2011).

In the obviousness inquiry, we must also consider whether “a person of ordinary skill, upon reading the reference, would be discouraged from

following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.” *In re Gurley*, 27 F.3d 551, 553 (Fed Cir. 1994). A reference “does not teach away. . . [if] it merely expresses a general preference for an alternative invention but does not ‘criticize, discredit, or otherwise discourage’ investigation into the invention claimed.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) (quoting *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)). However, “even if a reference is not found to teach away, its statements regarding preferences are relevant to a finding regarding whether a skilled artisan would be motivated to combine that reference with another reference.” *Polaris Indus. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 (Fed. Cir. 2018) (citing *Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1051 n.15 (Fed. Cir. 2016) (en banc)).

Based on the evidence in the current record, we have concerns regarding whether Petitioner’s arguments and evidence are based on impermissible hindsight. For example, Petitioner provides generic reasons for combining the various limitations. That is, although Petitioner argues that person of ordinary skill in the art would select the inverter from Doyle to be incorporated into Steinacker because it “has a trip point that is relatively stable with respect to temperature and/or to certain CMOS manufacturing process parameters,” (Pet. 21 (quoting Ex. 1006, 2:37–40)), Petitioner does not explain persuasively why a person of ordinary skill in the art at the time of the invention would have considered those factors important. Nor does Petitioner explain why a person of ordinary skill in the art in 2009 (the filing date of the ’674 patent) would turn to a 1986 reference (Doyle) to select an inverter to be used in a circuit from 2005 (U.S. filing

date of Steinacker). Although the evidence shows that a person of ordinary skill in the art *could* have used the Doyle inverter, we have concerns whether the evidence is sufficient to demonstrate why a person of ordinary skill in the art *would* have done so. *See Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017) (“But that reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.”).

Similarly, Petitioner’s reason for using forced stack technique mentioned in Park also raises issues. According to Petitioner, a person of ordinary skill in the art would use transistor stacking to reduce leakage power. *See* Pet. 21–22. However, there is nothing in either Steinacker or Doyle to suggest that leakage is a problem. Moreover, Petitioner’s reasoning is generic and, taken to the extreme, would apply to every transistor in every device. Nor does Petitioner address the issues associated with a smaller transistor, such as less sensitivity or longer processing times. *See* Ex. 1001, 2:31–39.

Moreover, even if a person of ordinary skill in the art would have been concerned about leakage, we question whether the evidence sufficiently shows why a person of ordinary skill in the art would use the forced stack technique over the sleepy stack technique. Although Park briefly discusses the forced stack technique, the focus of Park—as demonstrated by the title and abstract—is on the newly developed sleepy stack structure. *See* Ex. 1007. In fact, Park indicates that the “sleepy stack structure can achieve more power savings than the forced stack technique

and the self-controlled stacked transistors (e.g., 100x compared with 10x for the forced stack transistor or the self-controlled stacked transistors).” *Id.* at 1251. Although a person of ordinary skill in the art *could* have selected the less effective forced stack over the sleepy stack, we question whether Petitioner has sufficiently demonstrated why a person of ordinary skill in the art *would* have selected forced stack transistors. Without such an explanation, a reasonable inference is that the forced stack was selected using impermissible hindsight because it could be used to modify Doyle to make a circuit claimed in the ’674 patent.

At this stage of the proceedings, it is not necessary for us to determine whether Petitioner has sufficiently articulated why a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention. However, we request the parties to brief this issue further during the trial, and in particular to focus on the following issues: (1) whether impermissible hindsight was used in the selection and combination of the prior art, (2) whether the reasons given in the Petition are generic statements divorced from the prior art elements or focus on the specific references used, and (3) whether a person of ordinary skill in the art would have selected the forced stack technique over the sleepy stack technique.

III. CONCLUSION

Our review of the Petition under 35 U.S.C. § 314 is not to determine whether an individual asserted fact is indisputable or whether a preponderance of the evidence supports Petitioner. Our review is to determine whether the totality of the information presented in the Petition and Preliminary Response shows that there is a reasonable likelihood that

Petitioner would prevail with respect to at least one of the claims challenged in the Petition. For the reasons expressed above, we determine that Petitioner has established the requisite reasonable likelihood of prevailing as to claims 1, 2, and 5–7 of the '674 patent.

Our factual findings, conclusions of law (including claim constructions), and determinations at this stage of the proceeding are preliminary, and based on the evidentiary record developed thus far. This is not a final decision as to the patentability of claims for which *inter partes* review is instituted. Our final decision will be based on the record as fully developed during trial.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review of all challenged claims of the '674 patent is instituted with respect to all grounds set forth in the Petition (*see* Section I.E, *supra*); and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '674 patent is hereby instituted commencing on the entry date of this Decision, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

IPR2018-01315
Patent 8,063,674 B2

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