

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

QUALCOMM, INC.,
Patent Owner.

IPR2018-01261¹
Patent 9,535,490 B2

Before DANIEL N. FISHMAN, DANIEL J. GALLIGAN, and
AARON W. MOORE, *Administrative Patent Judges*.

FISHMAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ IPR2018-01293, IPR2018-01295, IPR2018-01344, and IPR2018-01346, each directed to claims of this same patent, have been consolidated with the instant proceeding in accord with 37 C.F.R. § 42.122(a).

I. INTRODUCTION

A. *Background and Summary*

Intel Corporation (“Petitioner”) requests *inter partes* review of claim 31 of U.S. Patent No. 9,535,490 B2 (the “’490 patent,” Ex. 1001) pursuant to 35 U.S.C. § 311 *et seq.* Paper 3 (“Petition,” “Pet.,” or “1261PET”). Qualcomm, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). On January 15, 2019, based on the record before us at that time, we instituted an *inter partes* review of claim 31 on the sole ground of unpatentability asserted in the Petition. Paper 8 (“Decision on Institution” or “Dec. on Inst.”).

Concurrently with the filing of this Petition, Petitioner filed four additional petitions in each of IPR2018-01293, IPR2018-01295, IPR2018-01344, and IPR2018-01346. Each of those four petitions challenge other claims of the ’490 patent.² Patent Owner filed a Preliminary Response in each of these additional cases presenting similar arguments to those presented in the Preliminary Response in the instant case. The grounds asserted, the references relied upon for those grounds, and the arguments presented, in each of these four additional petitions are similar to those of the instant matter. In each of these four additional, concurrently filed petitions, based on the record before us and for reasons similar to those in the instant case, we instituted review on all asserted grounds for the claims challenged in each petition. In an Order entered January 29, 2019, we consolidated cases IPR2018-01293, IPR2018-01295, IPR2018-01344, and

² Where all five petitions are substantively the same, we cite only to the petition in the instant case (IPR2018-01261). In like manner, where each of our five Decisions on Institution reaches the same conclusion, we cite only to our Decision on Institution for the instant case (IPR2018-01261).

IPR2018-01346 into the instant case. Paper 10. Having instituted all challenged claims in each of the petitions on all grounds, the consolidated proceeding involves *inter partes* review of claims 1–6, 8, 9, 11–13, 16, 17, 20, 22–24, 26–28, 30, and 31 (the “challenged claims”).

In this consolidated proceeding, Patent Owner filed a Patent Owner’s Response (Paper 21, “PO Resp.”),³ Petitioner filed a Reply (Paper 20, “Reply”), and Patent Owner filed a Sur-Reply (Paper 23, “Sur-Reply”).

Oral argument was held on October 9, 2019 and a transcript of that hearing is in the record. Paper 29 (“Tr.”).

Upon consideration of the complete record, we determine by a preponderance of the evidence that claims 1–6, 8, 9, 11–13, 16, 17, 20, 22–24, 26–28, 30, and 31 (all challenged claims) are unpatentable.

B. Consolidated Papers and Exhibits

The petitions filed in each of the consolidated cases are entered in the record of this case (IPR2018-01261) as exhibits, namely the petition in IPR2018-01293 (“1293PET,” Ex. 1028), the petition in IPR2018-01295 (“1295PET,” Ex. 1029), the petition in IPR2018-01344 (“1344PET,” Ex. 1030), and the petition in IPR2018-01346 (“1346PET,” Ex. 1031).

Several exhibits in each of the consolidated cases are identical but are numbered differently in each of the consolidated cases. The parties jointly filed a paper describing the correspondence of the substantively identical exhibits. Paper 13. For example, Exhibit 1001 in this proceeding (IPR2018-

³ Patent Owner filed an earlier Response as Paper 17, which lacked proper page numbering. Patent Owner later filed an authorized, corrected version of its Response as Paper 21 (PO Resp.) with page numbers added and no substantive changes to the arguments. We address Patent Owner’s arguments as presented in that corrected Patent Owner Response.

01261), the '490 patent, is identified as Exhibit 1101 in 1293PET, as Exhibit 1201 in 1295PET, as Exhibit 1301 in 1344PET, and as Exhibit 1401 in 1346PET. Paper 13, 1. For all such substantively identical exhibits, despite each consolidated petition referring to its unique exhibit numbers, we refer to the exhibit numbers used in IPR2018-01261 (this proceeding).

Of particular note, Petitioner's expert, Dr. Bill Lin, provides a declaration in each of the five consolidated petitions (Ex. 1002 in IPR2016-01261, Ex. 1102 in IPR2018-01293, Ex. 1202 in IPR2018-01295, Ex. 1302 in IPR2018-01344, and Ex. 1402 in IPR2018-01346). Although much of Dr. Lin's analysis is similar or identical in the five cases, the declarations are not substantively identical (some arguments apply to claims only challenged in the corresponding petition) nor syntactically identical (even for similar arguments, page and paragraph numbers are different). Exhibits 1102, 1202, 1302, and 1402 from these four consolidated proceedings are entered in the record of this consolidated case (IPR2018-01261) as Exhibits 1018, 1019, 1020, and 1021, respectively.

C. Real Parties in Interest

Petitioner identifies both Intel Corporation and Apple Inc. as real parties in interest. Pet. 1. Patent Owner identifies itself (Qualcomm, Inc.) as the sole real party in interest for Patent Owner. Paper 5, 2.

D. Related Matters

The parties informed us that the '490 patent is presently asserted against Petitioner in the litigation *Qualcomm Inc. v. Apple Inc.*, Case No. 3:17-cv-01375-DMS-MDD (S.D. Cal.), and against Apple in a proceeding before the International Trade Commission ("ITC") captioned *In the Matter of Certain Mobile Electronic Devices and Radio Frequency Components Thereof*, Inv. No. 337-TA-1065. Pet. 1–2; Paper 5, 2. The ITC investigation

addressed claim 31 of the '490 patent and we find the Commission's final Commission Opinion informative in this Decision. *See* Ex. 1022.

The parties further informed us that the '490 patent is at issue in the above-identified, concurrently filed petitions for *inter partes* review of claims of the '490 patent (i.e., cases IPR2018-01293, IPR2018-01295, IPR2018-01344, and IPR2018-01346). *See* Pet. 2; Paper 5, 2. As noted above, these four related proceedings before the Board have been consolidated into this proceeding.

E. The '490 Patent

The '490 patent is generally directed to power saving techniques in computing devices. Ex. 1001, code (54), code (57). According to the '490 patent, although stationary desktop computers and servers are generally immune to power consumption issues, “mobile devices constantly struggle to find a proper balance between available functions and battery life.” *Id.* at 1:28–31. The '490 patent further indicates that mobile devices utilize internal bus structures to connect components within the mobile device and that increased performance demands have led to use of faster, higher-power-consuming interconnect bus structures within mobile devices (e.g., Peripheral Component Interconnect Express “PCIe” and Universal Serial Bus “USB” 3.0). *Id.* at 1:36–60.

Figure 1C of the '490 patent is reproduced below.

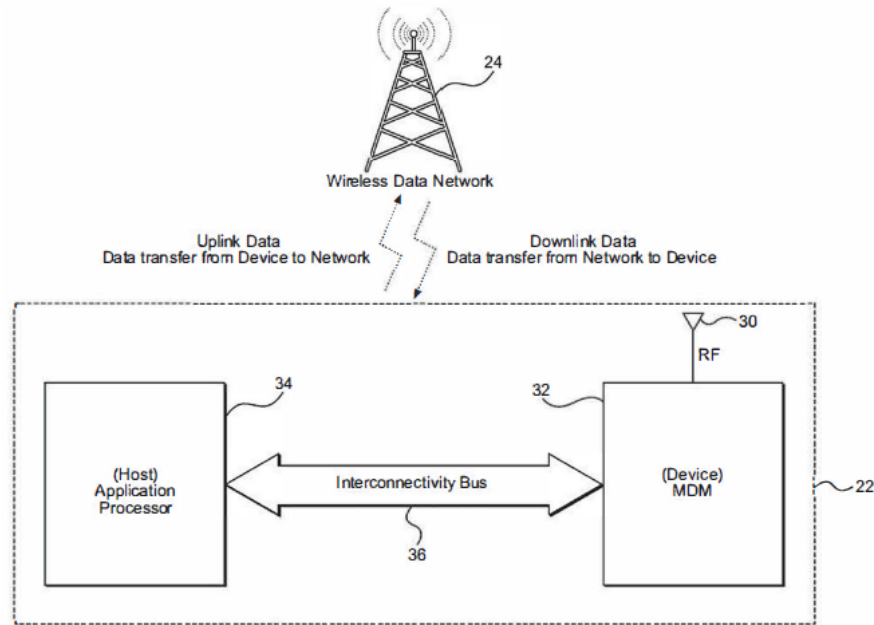


FIG. 1C

Figure 1C is a block diagram of mobile terminal 22 with interconnectivity bus 36 coupling application processor 34 and modem processor 32. In one embodiment disclosed by the '490 patent, bus 36 may be a PCIe bus. *Id.* at 8:6–9. According to the '490 patent, “[w]hile placing the interconnectivity bus 36 in a sleep mode generally saves power, such sleep modes do have a drawback in that they consume relatively large amounts of power as they transition out of the sleep mode.” *Id.* at 8:9–12.

According to the '490 patent, the PCIe bus can be transitioned from a low power state (e.g., saving battery life) to an active state in which information may be exchanged. *Id.* at 8:23–26. Figure 3 of the '490 patent is reproduced below.

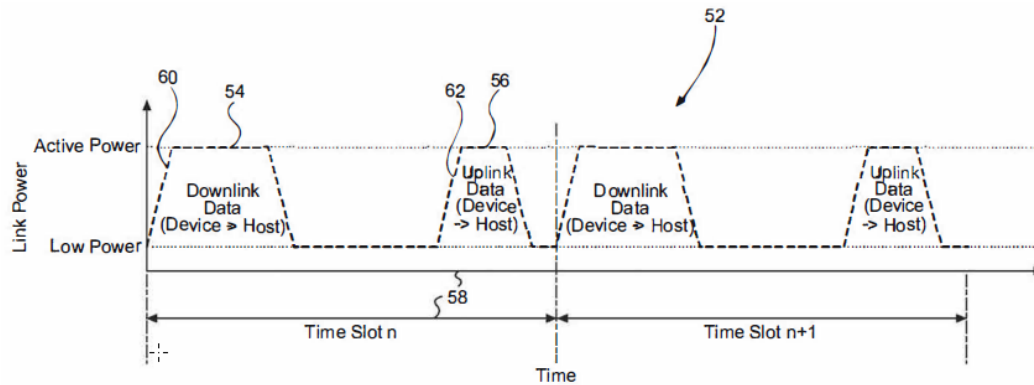


FIG. 3

Figure 3 depicts graph 52, without the purported improvement of the '490 patent, presenting time on the X-axis versus the power state of a PCIe link on the Y-axis. “Downlink data” refers to data received by the device (i.e., from a connected network) destined for the host/application processor of the device, and “uplink data” refers to data to be sent from the device (i.e., from the host/application processor) to the device (i.e., for transmission to a network). Time is shown as a sequence of time slots 58 (n, n+1, etc.). *Id.* at 8:20–40, Fig. 3. The '490 patent asserts that, as practiced prior to its purported invention, within a given time slot 58, exchange of downlink data 54 requires first transition 60 from a low power state to an active power state and back to a low power state, followed by a similar second transition 62 for exchange of uplink data 54. *Id.* at 8:21–34. According to the '490 patent, where the time slot duration is one millisecond, as is common, there may be thousands of such transitions (60, 62) per second. *Id.* at 8:34–38. Thousands of such transitions per second consume a significant amount of power in a battery powered mobile terminal. *Id.* at 8:38–40.

The '490 patent purports to improve battery life by reducing the number of such transitions. *See, e.g., id.* at 5:32–35. Figure 5 of the '490 patent is reproduced below.

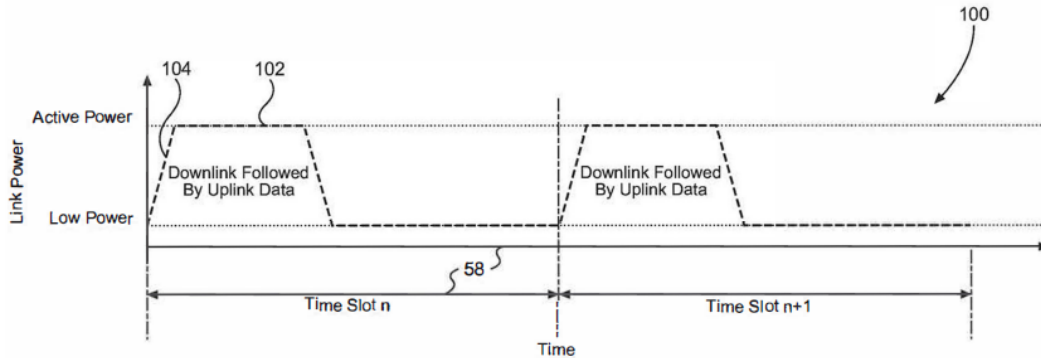


FIG. 5

Figure 5 depicts graph 100, as purportedly improved by the '490 patent, presenting time on the X-axis versus the power state of a PCIe link on the Y-axis. According to the '490 patent, combining transmission of downlink data and uplink data during a single active power state period 102 requires only one transition 104 from a low power state to an active power state during a time slot 58. *Id.* at 10:36–40. According to the '490 patent, reducing the number of transitions increases the duration of the low power state in each time slot, thus conserving battery power in a mobile terminal. *Id.* at 10:40–45.

The '490 patent proposes a number of structures and techniques within a mobile terminal for combining uplink and downlink transmissions to reduce the number of low power to active power transitions.

Figure 2 of the '490 patent is reproduced below.

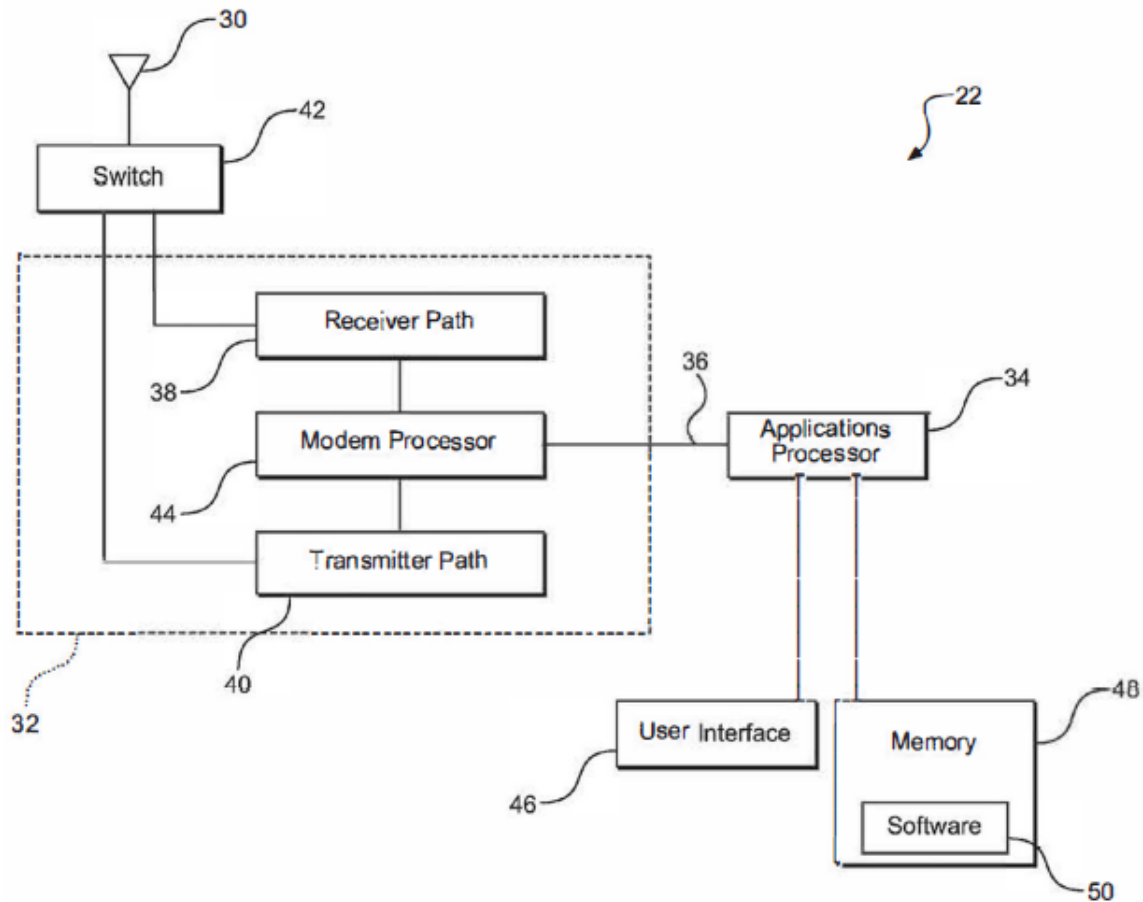


FIG. 2

Figure 2 is a block diagram of exemplary mobile terminal 22. Mobile terminal 22 comprises application processor 34 and modem 32. Ex. 1001, 6:58–63, 7:4–12. Modem 32 further comprises modem processor 44, receiver path 38, and transmitter path 40. *Id.* at 6:58–63, 7:7–10. Modem processor 44 and application processor 34 are coupled by interconnectivity bus 36. *Id.* In one embodiment, bus 36 may be a PCIe compliant bus. *Id.* at 6:66–67, 7:14–15. Mobile terminal 22 further comprises a modem timer (not shown). *Id.* at 4:30–31.

In one disclosed embodiment of the '490 patent, the modem processor is configured to hold data it has received that is ready to send to the application processor (“downlink” data) until a programmed time period of

the modem timer expires. *Id.* at 4:32–34. The application processor is configured to hold data it has ready to send to the modem processor (“uplink” data) until the modem processor pulls any held data from the application processor. *Id.* at 4:38–42.

In another disclosed embodiment of the ’490 patent, the application processor is configured to hold data it has ready to send to the modem processor (“uplink” data) until downlink data is received at the application processor from the modem processor, which triggers the application processor to send its held data to the modem processor. *Id.* at 2:56–62.

In yet another disclosed embodiment of the ’490 patent, the application processor is configured to hold data it has ready to send to the modem processor (“uplink” data) until downlink data is received at the application processor from the modem processor or until a programmed time period of an uplink timer expires, which triggers the application processor to send its held data to the modem processor. *Id.* at 3:2–6.

In other disclosed embodiments of the ’490 patent, a variety of threshold measures may be used to override the wait for a timer to expire including, for example, a byte count threshold, a packet size threshold, a packet number threshold, etc. *Id.* at 2:23–34.

F. Illustrative Claims

Independent claims 1 and 31 are illustrative of the claimed subject matter and are reproduced below.

1. A mobile terminal comprising:
 - a modem timer;
 - a modem processor, the modem processor configured to hold modem processor to application processor data until expiration of the modem timer;
 - an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

Ex. 1001, 17:55–18:5.

31. A mobile terminal comprising:

a modem timer;

a modem processor, the modem processor configured to hold modem processor to application processor data until expiration of the modem timer;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until the modem processor pulls data from the application processor after transmission of the modem processor to application processor data,

wherein the modem processor is further configured pull data from the application processor after transmission of the modem processor to application processor data and before the interconnectivity bus transitions from an active power state to a low power state.

Id. at 21:4–21.

G. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–6, 8, 9, 11–13, 16, 17, 20, 22–24, 26–28, 30, and 31 are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	References
1, 4–6, 8, 9, 11–13, 16, 20, 22–24, 26–28, 30, 31	103 ⁴	Heinrich, ⁵ Balasubramanian ⁶
2, 3, 17	103	Heinrich, Balasubramanian, Tsai ⁷

Petitioner relies on the declarations of Bill Lin, Ph.D. (Exs. 1002, 1018–1021,⁸ 1023) in support of its assertions. Patent Owner relies on the declaration of R. Jacob Baker, Ph.D. (Ex. 2007⁹).

II. ANALYSIS

A. *Legal Standards*

1. *Obviousness*

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are “such that the subject matter[,] as a whole[,] would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

⁴ The Leahy-Smith America Invents Act (“AIA”) amended 35 U.S.C. § 103. *See* Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011). Because the application that resulted in the ’490 patent was filed after the effective date of the post-AIA amendment, the post-AIA version of § 103 applies. For the same reasons, the post-AIA version of § 102 applies in determining whether the applied references qualify as prior art.

⁵ Heinrich, US 9,329,671 B2, issued May 3, 2016 (Ex. 1004).

⁶ Balasubramanian, US 8,160,000 B2, issued Apr. 17, 2012 (Ex. 1005).

⁷ Tsai, US 8,112,646 B2, issued Feb. 7, 2012 (Ex. 1017).

⁸ Exhibit 1018 herein is referred to as Exhibit 1002 in 1293PET. Exhibit 1019 herein is referred to as Exhibit 1002 in 1295PET. Exhibit 1020 herein is referred to as Exhibit 1002 in 1344PET. Exhibit 1021 herein is referred to as Exhibit 1002 in 1346PET.

⁹ Patent Owner filed two exhibits with the exhibit number 2007—Dr. Baker’s declaration and a transcript of a hearing before the International Trade Commission (“ITC”). In this decision, we refer to Dr. Baker’s declaration as “Ex. 2007” and we do not need to refer to the ITC transcript.

said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of non-obviousness, i.e., secondary considerations.¹⁰ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner argues a person of ordinary skill in the art related to the ’490 patent would have a Master’s degree in electrical engineering, computer engineering, or computer science, and would also have at least two years of experience in “mobile device architecture and multiprocessor systems.” Pet. 20. In the alternative, Petitioner argues the ordinarily skilled artisan would have a Bachelor’s degree in one of the above-identified programs and at least four years of experience in the above-identified fields. *Id.*

Patent Owner agrees with Petitioner’s definition of the level of skill, emphasizing that “‘relevant experience’ in the context of the ’490 Patent refers to experience with mobile device architecture and multiprocessor systems.” PO Resp. 19.

In our Decision on Institution, we adopted Petitioner’s definition of the level of ordinary skill in the art, with the exception of the language “at least,” and determined that a person of ordinary skill in the art at the time of the invention of the ’490 patent would have had a Master’s degree in

¹⁰ Patent Owner does not present arguments or evidence of such secondary considerations in its briefs. Therefore, secondary considerations do not enter into our analysis.

electrical engineering, computer engineering, or computer science, and two years of experience in mobile device architecture and multiprocessor systems or, in the alternative, a Bachelor's degree in one of the above-identified programs and four years of experience in the above-identified fields. Dec. on Inst. 9–10. On the complete record, we discern no reason to modify our determination regarding the level of ordinary skill.

C. Claim Construction

In an *inter partes* review for a Petition filed before November 13, 2018, a claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears. 37 C.F.R. § 42.100(b) (2017); *see also* *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016) (upholding the use of the broadest reasonable interpretation standard (“BRI standard”)). Under the BRI standard, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). “[A] claim construction analysis must begin and remain centered on the claim language itself” *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004). “Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not a part of the claim.” *SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004).

By contrast, for an expired patent or an unexpired patent challenged in a petition filed on or after November 13, 2018, we apply the principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en

banc) (“*Phillips* standard”). See 37 C.F.R. § 42.100(b) (2019); *Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1279 (Fed. Cir. 2017).

Under either standard for claim construction in our proceedings, there is no presumption of validity, and Petitioner’s burden of proof is still by a preponderance of the evidence. Moreover, a “claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history.” *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002). Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). In the absence of such a special definition or other consideration, “limitations are not to be read into the claims from the specification.” *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

Petitioner applies the *Phillips* standard for interpreting terms of the ’490 patent but argues “Petitioner is not aware of any difference in how the claims would be construed under the BRI standard.” Pet. 19. Patent Owner notes that Petitioner failed to timely file a motion requesting use of the *Phillips* standard for claim construction (under 37 C.F.R. § 42.100(b)) but waives any objection to that deficiency. PO Resp. 27. Patent Owner agrees with Petitioner that “there is no difference in how the claims would be construed under the BRI standard.” *Id.*

The ’490 patent is not expired, will not likely expire prior to entry of this final written decision, neither party has made a request in compliance with our rules that the *Phillips* standard be applied, and the Petition was filed prior to the change of our rules regarding claim construction effective for petitions filed on or after November 13, 2018. Therefore, as we did in our

Decision on Institution (*see* Dec. on Inst. 11–12), we apply the broadest reasonable interpretation for any needed claim construction.

Although the broadest reasonable interpretation standard is broad, the Board cannot interpret the words of a claim without regard for the full claim language and the written description. *See TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016); *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015). Our reviewing court has emphasized the importance of a patent’s specification as intrinsic evidence for construing claim terms. *See Phillips*, 415 F.3d at 1315–17. Specifically, the Court has explained that “the specification . . . is the single best guide to the meaning of a disputed claim term.” *Id.* at 1314 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). The court in *Phillips* stated that extrinsic evidence, such as dictionary definitions, may be useful, but is unlikely to result in a reliable interpretation of claim scope unless considered in the context of the intrinsic evidence. *See Phillips*, 415 F.3d at 1319.

Furthermore, only terms that are in controversy need to be construed and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Other than the terms interpreted below, we discern no reason to expressly construe any other claim terms.

1. “Pull”

Claim 31 includes the recitation, “wherein the modem processor is further configured pull data from the application processor.”¹¹

a) The Parties’ Interpretations

Petitioner contends “pull,” in the context of the ’490 patent would have been understood to mean “receiving data in response to a request for the data.” Pet. 20. Petitioner argues “[i]n a pull data transfer, the data is transferred in response to a request for data by the intended recipient of the data.” Pet. 21 (citing Ex. 1002 ¶ 68). Petitioner further argues the ’490 patent Specification is consistent with this interpretation in that, although not expressly defining the term “pull,” the Specification discloses pulling data with no mention of a required address/location, refers to both pulling and pushing of data as distinct modes of transfer, and discloses that both techniques may be implemented “based on polling, setting doorbell registers, or other techniques.” Pet. 20–21 (citing Ex. 1001, 9:61–10:1, 16:34–37). Petitioner cites extrinsic evidence in support of its proffered construction. Pet. 21 (citing Exs. 1008 (an electrical engineering technical dictionary defining “pull technology” to mean “[d]ata distribution, such as that over the Internet, in which users receive information by requesting it”), 1009 (a computer and Internet technical dictionary defining “pull” to mean “the

¹¹ Claim 14 includes a similar recitation that the modem processor is configured to pull data from the application processor. Claim 14 is not challenged in this consolidated proceeding. However, we may consider use of the term “pull” in the context of claim 14 to the extent it aids in our construction of the term.

process whereby the user retrieves information from a network at the user's request, as in traditional web browsing"), 1010 (an academic paper discussing push and pull data transmission techniques and stating: "In the receiver-pull model, it is the receiver who initiates the message transfer by explicitly contacting the sender. The sender passively waits for the receiver and delivers the entire content upon receiving a request.")).

Patent Owner argues that, in the context of the '490 patent, a pull operation requires that the requesting recipient provide location information to the sender to locate the data to be sent in response to the pull. *See* PO Resp. 27–28 ("With knowledge of where in a shared memory the application-processor-held data, the modem processor is able to reach out and access the data from the shared memory based on that specified address (*i.e.*, pull the data)." (citing Ex. 2007 ¶ 61)). Patent Owner cites the same two portions of the '490 patent Specification as cited by Petitioner but adds that surrounding disclosure of each citation allegedly clarifies that a pointer (*i.e.*, an address or location) is provided by the application processor for the modem processor to know where data to be transferred is stored. *Id.* at 29 (citing Ex. 1001, 9:41–10:10, 15:61–16:37).

In support of its proffered construction, Patent Owner points to deposition testimony of Petitioner's expert in the parallel ITC proceeding, Dr. Yalamanchili, who testifies, *inter alia*, that, in a pull operation, "[t]he location of the data has to be known in order to effect any transfer, so the data can be accessed," that, in a pull operation, supplying an address of the data "would be typical," and that some identifier or information related to where the data is located would be part of the initiation of the pull. PO Resp. 28–29 (quoting excerpts of Ex. 2008). Patent Owner further argues Petitioner's expert in this proceeding (Dr. Lin) agrees that an exemplary pull

operation in the '490 patent “uses doorbell registers and *address-indicating pointers*” in performing a pull operation. *Id.* at 29 (citing Ex. 2010, 27:5–7). Furthermore, Patent Owner argues the extrinsic evidence proffered by Petitioner (Exs. 1008–1010) in support of its interpretation of “pull” supports Patent Owner’s position because they refer to typical Internet access such as web browsing in which a user supplies an address or hyperlink that specifies the location of the data to be pulled. PO Resp. 29–30.

Moreover, Patent Owner asserts Petitioner’s proffered construction, as supported by Dr. Lin’s testimony, is contrary to positions articulated by Petitioner’s expert (Dr. Yalamanchili) in the related ITC proceeding and, thus, Dr. Lin’s testimony interpreting “pull” should be given little weight. PO Resp. 29; *see also* Sur-Reply 2–6.

Accordingly, Patent Owner argues “pull” should be interpreted to mean “accessing data based on a specified location of that data.” PO Resp. 32 (citing Ex. 2007 ¶ 66).

Petitioner replies that Patent Owner’s narrower construction requiring that a “pull” operation include a “specified location of the data” to be pulled is inconsistent with the intrinsic and extrinsic evidence. Reply 4. In particular, Petitioner argues Patent Owner relies on an exemplary embodiment in the '490 patent that uses a direct memory access (“DMA”) read transaction on a PCIe bus, which includes specifying an address in memory for the data to be pulled from the application processor. Reply 5 (citing PO Resp. 29, 55 (“DMA read request includes the address in memory of the data to be pulled”)). Petitioner contends the '490 patent Specification does not “suggest any intent to limit the ‘pull’ of claim 31 to PCIe and/or DMA-based transfers,” but, instead, repeatedly refers to pulling data without

reference to DMA or PCIe exemplary embodiments. *Id.* (citing Ex. 1001, 4:40–41, 9:66–10:2, 16:35–37). Petitioner further contends that the ’490 patent Specification makes clear that a PCIe implementation is intended merely as exemplary and discloses other interconnectivity busses and techniques that may be employed. Reply 7 (citing Ex. 1001, 6:66–7:3).

b) Analysis

Both parties’ proffered interpretations are consistent with the Specification of the ’490 patent. However, we are persuaded that the broadest reasonable interpretation of “pull,” consistent with the Specification and the plain meaning, at least encompasses Petitioner’s proffered interpretation, which is broader than Patent Owner’s proffered interpretation because it does not require that a “pull” specify a location from which the data is to be pulled.

As our reviewing court held, we focus on the intrinsic evidence (claims, Specification, prosecution history) to construe the terms in the claims. *DePuy*, 469 F.3d at 1014. Here, the intrinsic evidence provides scant aid in interpreting the term “pull.” There is no express definition of “pull” in the intrinsic evidence. Claim 14 (not challenged here) recites, in essence, that the modem processor pulls uplink data from the application processor in response to receipt of downlink data or the expiration of information. Claim 31 recites, in essence, that the application processor holds (e.g., buffers) uplink data until the modem processor pulls the held data and the modem processor *pulls* the held uplink data from the application processor after transmitting downlink data to the application processor and before the interconnectivity bus transitions to a low power state. Although both proffered interpretations are consistent with these

claims, we discern nothing in these claims that limits the claims requiring a “pull” to specify an address or location of the data to be pulled.

Like the claims, we find the ’490 patent Specification provides little aid in interpreting the term “pull.” Both parties point to portions of the Specification in columns 9–10 and 15–16. Pet. 20 (citing Ex. 1001, 9:61–10:1, 16:34–37); PO Resp. 29 (citing Ex. 1001, 9:41–10:10, 15:61–16:37); *see also* PO Resp. 55. We are unpersuaded that the cited portions of the Specification limit the interpretation of “pull” to require an address be specified. These and other portions of the Specification merely discuss an *exemplary embodiment* in which the processors are coupled by a PCIe bus using the MHI protocols. *See, e.g.*, Ex. 1001, 9:42–46 (“*For example*, on a fusion device using MHI over PCIe, the modem processor 44 may poll (read) the MHI channel Context Write Pointer to determine data buffers where downlink packets can be transferred.” (emphasis added)). In like manner, the ’490 patent Specification at columns 15 and 16 refers to the same “write pointers” of the PCIe/MHI exemplary embodiment. Although this is the only exemplary embodiment discussed in any detail in the ’490 patent Specification, we remain disinclined to import such a narrow limitation from an exemplary embodiment of the Specification into the claims. *See SuperGuide*, 358 F.3d at 875. Patent Owner acknowledges that its claims are not limited to this disclosed PCIe-based embodiment:

And you have to read the claims in the context of the specification of which they are a[]part. The only examples given in the patent of a pull both used a DMA process over a PCIe bus. And, yes, Dr. Baker said that the claims aren’t limited to that, but to interpret the claims, you have to read in the specification, and the specification makes it clear that these Patentees meant a pull to be more than just simply receiving data passively.

Tr. 66:2–9. We agree that the claims are not limited by the Specification’s disclosure of an exemplary PCIe bus embodiment, but we disagree that “the specification makes it clear that these Patentees meant a pull to be more than just simply receiving data passively.” To the contrary, although the Specification at column 15, line 61 through column 16, line 30 discloses a method depicted in Figure 12 that, *inter alia*, updates a write pointer in the application processor for the modem processor to “pull” data, the next paragraph states, “once a timer has expired, data can be pulled or pushed across the interconnectivity bus 36 based on polling, setting doorbell registers, *or other technique[s]*.” Ex. 1001, 16:34–37 (emphasis added). The phrasing “pulled or pushed . . . based on . . . other technique[s],” clearly suggests that techniques for pulling data, other than those that require a “write pointer,” are within the meaning of “pull.” In like manner, disclosure of “a fusion device using MHI over PCIe” is clearly disclosed as a non-limiting, exemplary embodiment. *Id.* at 9:40–60. Lastly, the Specification includes a typical “savings clause” that clearly discloses that the exemplary embodiments are not intended to limit the scope of the claims—including the scope of claimed “pull” operations. *Id.* at 17:44–53. As above, although both proffered interpretations are consistent with the ’490 patent Specification, we discern nothing in Specification that limits the claims requiring a “pull” to specify an address or location of the data to be pulled.

Neither party identifies relevant prosecution history (Ex. 1003) to be considered in interpreting “pull.”

Accordingly, the intrinsic evidence supports Petitioner’s broader interpretation. Although we find the intrinsic evidence sufficient to interpret “pull” in accord with Petitioner’s broader interpretation, we turn next to consideration of the extrinsic evidence. Patent Owner argues the dictionary

definitions proffered by Petitioner in support of its broader interpretation actually support Patent Owner's narrower interpretation of "pull" because each dictionary points to Internet access as an example of a pull request and argues that each such exemplary Internet use includes a receiver of the pulled data specifying an address or location of the data to be retrieved. PO Resp. 29–30. We are unpersuaded by Patent Owner's argument. A first technical dictionary defines "pull"¹² as "[d]ata distribution, such as that over the Internet, in which users receive information by requesting it" and then provides a specific example of requesting data by providing an address. Ex. 1008, 3. Another technical dictionary defines "pull" to mean "the process whereby the user retrieves information from a network at the user's request" and, like the first dictionary, then follows with an example such as web browsing on the Internet. Ex. 1009, 3. These dictionaries are consistent with Petitioner's broader interpretation, consistent with the '490 patent Specification, and merely provide common examples of pull operations in the context of Internet accesses where the request includes an address. Such examples are common in the Internet context but do not limit the ordinary meaning of "pull" to require specification of a location in all contexts. In particular, in the context of the '490 patent claims, the "pull" operation is unrelated to typical Internet access but, instead, relates to a more generic pull operation of data between two processors.

Furthermore, we credit Dr. Lin's testimony that, unlike the PCIe exemplary embodiments of the '490 patent Specification, at least one other known interconnectivity bus does not require an address or location to be

¹² More precisely, Exhibit 1008 defines "pull" as substantively the same as "pull technology" and then defines "pull technology" as stated.

specified for a pull operation. Ex. 1023 ¶ 9 (citing Ex. 1027 describing the I²C interconnectivity bus standard, which utilizes only a single bit to request a pull of data from another device). Dr. Lin's deposition testimony describes such a single bit that may be used to initiate a "pull" operation without any express specification of an address or location. Ex. 2010, 32:10–38:5. Rather, so long as the sender and receiver know what data is to be transmitted, the "pull" operation need not specify the location of the data to be pulled but merely sends the request to the processor that has the data to be sent.

Q. So a pull request does not need to include an address?

A. Well, so if I want to pull data from you, I have to send a request to you. I can't just send a request to -- out in the air or out to nobody. So, in a sense, I'm specifying location where the request is going, to you.

Q. Do you need to tell me what data you're requesting?

A. Well, if I'm requesting a particular data, the data that's in your packet queue, I'm asking you for the data that's in the packet queue, and you are sending that data back to me in response to that request.

...

Q. So if I just asked you to send me what data you have queued, is that a pull request?

A. Yes, because you're identifying what data you want.

Q. So if I ask you to send me the data you have, is that a pull request?

A. Yes.

Ex. 2010, 30:2–14, 32:10–16. In other words, if a first processor wishes to pull data that is queued by a second processor, queued (held) specifically for transmission to the first processor as is the case in the '490 patent, a "pull"

request need only be directed from the first processor to the second processor because the second processor already knows the request from the first processor is for the data queued (held) for such transmission. The '490 patent's non-limiting, exemplary embodiment happens to use the MHI protocol over a PCIe bus such that a "pull" request in that context may need to specify an address for the data to be pulled in accord with the MHI/PCIe standards.¹³ Therefore, we credit Dr. Lin's testimony that there were, at the time of the '490 patent, known techniques to "pull" data, such as the I²C protocol standards, that do not require specifying an address to request pulled data and, therefore, the ordinary meaning of "pull" at the time of the '490 patent does not require a pull request to specify an address of the data to be pulled.

We are also unpersuaded by Patent Owner's argument that Dr. Lin's testimony should be accorded less weight because it allegedly conflicts with Dr. Yalamanchili's testimony on behalf of the Petitioner in the related ITC matter and, thus, Dr. Lin is not credible. Sur-Reply 2–3, 6 (citing *Ultratec, Inc. v. CaptionCall, LLC*, 872 F.3d 1267, 1273 (Fed. Cir. 2017) and *Nissan North America, Inc. v. Board of Regents, the University of Texas System*, IPR2012-00035, Paper 30 at 7 (PTAB 2013)). Initially, we note that in both *Ultratec* and *Nissan*, the *same* expert offered allegedly conflicting testimony. By contrast, here, Dr. Yalamanchili did not testify in this matter but testified

¹³ Neither party positively asserts that DMA techniques are disclosed in the '490 patent but both parties discuss DMA techniques as they would be expected to be used in the context of the '490 patent. Although the '490 patent makes no mention of DMA techniques for such MHI transfers over the PCIe bus, such an embodiment may indeed require the "pull" request to specify an address for the DMA controller to access in the application processor's memory.

before the ITC—a different expert witness, testifying in a different proceeding, in a different forum that applies different claim construction standards and standards of proof. Thus, Patent Owner’s reliance on *Nissan* and *Ultratec* in arguing we should accord less weight to Dr. Lin’s testimony is inapposite.

Moreover, we are not persuaded Dr. Lin’s testimony conflicts with Dr. Yalamanchili’s testimony. Dr. Yalamanchili testified that it is “typical” that a pull operation requires some identification of the location of data to be pulled. Ex. 2008, 187:24–188:3, 188:17–18, 190:23–24, 191:3. However, Dr. Yalamanchili also testified, “the pull of data is a situation where the destination is responsible for the transfer of data from the source, as opposed to a push, where the source controls the transfer of data to a destination,” and “the flow of data to the destination under the control of the destination would be considered a pull.” Ex. 2008, 187:12–20, 188:12–14. Lastly, Dr. Yalamanchili’s testimony in our record consists of only a brief excerpt of the transcript of his deposition in the ITC proceeding. Such a scant record of a witness (testifying in another proceeding in another forum applying different claim construction standards) is deserving of less weight in this proceeding as compared to Dr. Lin’s full testimony (including two declarations and two complete deposition transcripts).

Still further, we note that the ITC Commission Opinion finds, “[a] ‘pull’ means the receiving processor (the modem processor in claim 31) requests or initiates the transfer of data from a remote source (the application processor). This understanding is consistent with the plain meaning of ‘pull’ and its usage in the ’490 patent.” Ex. 1022, 42 (citation omitted). Although we are not bound by the claim construction of another forum (particularly a forum that applies a different claim construction standard), it is noteworthy

that the Commission, applying the potentially narrower *Phillips* standard for claim construction, arrives at essentially the same construction we adopt—namely, Petitioner’s broader construction.

Lastly, we acknowledge Patent Owner’s argument that Petitioner’s Exhibit 1027 was filed late and should be accorded no weight in interpreting the term “pull.” Sur-Reply 32–33. As seen above in our analysis to interpret “pull,” we do not rely on Exhibit 1027 as providing a definition of “pull” but, instead, refer to it only as evidence that the ordinarily skilled artisan, at the time of the ’490 patent, would have known of interconnectivity busses and corresponding protocols that, unlike the PCIe exemplary embodiment of the ’490 patent, do not require any address or location indicia be specified to perform a “pull” consistent with our interpretation of the term. Even assuming, *arguendo*, that Exhibit 1027 was improperly filed, Patent Owner did not timely object to the new evidence and, accordingly, cannot file a motion to exclude. *See* 37 C.F.R. § 42.64. We accord Exhibit 1027 some weight as supporting Dr. Lin’s arguments that there were known interconnectivity busses at the time of the ’490 patent that used pull operations that did not specify an address or location with the pull operation. Furthermore, we agree with Dr. Lin that Exhibits 1008 through 1010 provide sufficient extrinsic evidence in support of his positions. *See* Sur-Reply 32–33 (quoting Ex. 2012, 21:16–25, 22:5–15, 23:7–9).

Weighing all intrinsic and extrinsic evidence of record, we determine that, although both proffered interpretations of “pull” are reasonable and consistent with the evidence, Petitioner’s proffered interpretation is the broader reasonable interpretation. Accordingly, we interpret “pull” to mean “*receiving data in response to a request for the data.*”

2. “*Triggered By*” and “*Triggers*”

Challenged independent claims 1, 16, 26–28, and 30, as well as their respective challenged dependent claims, recite that transmission of held data in one direction is “triggered by” or “triggers” transmission of data in the other direction between the application and modem processors of the ’490 patent. Petitioner argues the term “triggered by” means “initiated in response to.” 1293PET 19. Petitioner further argues the ’490 patent Specification does not expressly define the term but the Specification, prosecution history, and the claims impliedly support its proffered construction. *Id.* at 19–20 (citing Ex. 1001, 2:3–6, 11:15–18, 11:39–46; Ex. 1003, 45¹⁴). Petitioner cites extrinsic evidence (three dictionaries defining “trigger”) in support of its proffered construction of “triggers” and “triggered by.” *Id.* at 20 (citing Exs. 1012, 1013, 1014).

Patent Owner does not expressly address construction of this term. *See* PO Resp. 26–32.

We find Petitioner’s argument for its proffered construction of “triggered by” persuasive. Specifically, claim 1 sufficiently defines the condition that triggers the defined response—i.e., data is held by a first processor until receipt of data from a second processor, after which the first processor sends its held data to the second processor. The receipt of data is

¹⁴ Petitioner cited “[8/24/2016 Response], 14” in this exhibit of prosecution history. Although Petitioner correctly numbered pages of the exhibit sequentially starting at page “1,” in the lower right corner of each page, Petitioner cites to page “14” of the original, underlying documents that comprise the prosecution history. We find the cited page “14” at page 45 of the exhibit (Ex. 1003 in this consolidated proceeding) and request that all parties, in all proceedings before the Board, number exhibits with sequential page numbers starting at “1” and use those sequential page numbers in all citations in papers and other exhibits.

the event that triggers further action (transmission of the held data from the first processor to the second processor) following the event. In like manner, the other independent claims that refer to an event that “triggers” a next event (i.e., receipt of some data that triggers transmission of other data), sufficiently define the relevant conditions that trigger the next action. Petitioner’s interpretation is consistent with the claims in that a recited next action/event is *initiated in response to* some other recited action/event.

Therefore, we adopt the Petitioner’s definition and find that an action “triggered by” a recited condition means the action is “*initiated in response to*” the condition. In like manner, we interpret “triggers” in the context of a condition that “triggers” some action to mean that the action is “*initiated in response to*” the specified condition.

D. Obviousness Over Heinrich and Balasubramanian

In this consolidated proceeding, Petitioner relies on the combined disclosures of Heinrich and Balasubramanian in contending certain claims are unpatentable as obvious under 35 U.S.C. § 103 (post-AIA) as follows: claim 31 (Pet. 30–56); claims 1, 4–6, and 8 (1293PET 29–63); claims 16 and 22–24 (1295PET 29–67); claims 20, 28, and 30 (1344PET 56–72) and claims 9, 11–13, 26, and 27 (1346PET 55–69).

1. Overview of Heinrich (Ex. 1004)

Heinrich is directed to problems of power efficiency in inter-processor communications (“IPC”) among multiple processors of a system. Ex. 1004, 1:6–2:8. In battery-powered systems in particular, power consumption is a critical issue. *Id.* at 1:18–23. Figure 1 of Heinrich is reproduced below.

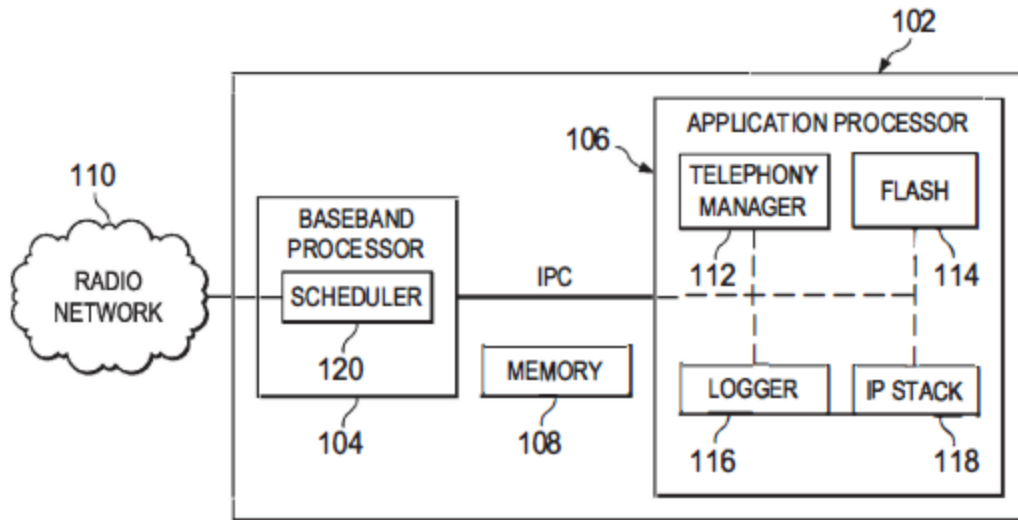


FIG. 1

Heinrich's Figure 1 is a schematic illustration of a communication system including mobile device 102. *Id.* at 3:19–20, 4:18–19. Mobile device 102 may be a mobile phone or tablet connected to radio network 110. *Id.* at 4:19–21. Mobile device 102 comprises baseband processor 104 and application processor 106. *Id.* at 4:26–29. Baseband processor 104 acts as a radio frequency (“RF”) modem to modulate and demodulate data exchanged between mobile device 102 and network 110. *Id.* at 4:30–33. Physical interface (labeled IPC in Figure 1) communicatively couples baseband processor 104 and application processor 106. *Id.* at 4:44–46. The physical interface to the IPC may be, for example, a USB interface. *Id.* at 4:46–48.

Each processor of mobile device 102 may operate in one of a plurality of modes, including an “awake” mode ready to process data and a “sleep” mode not ready to process data but saving power. *See id.* at 1:54–62. According to Heinrich, in the prior art, each time baseband processor 104 receives any quantum of data to be sent to application processor 106, application processor 106 would have to already be in the awake mode or would have to be transitioned from the sleep mode to the awake mode. *See*

id. at 1:65–2:2. Frequent transitions out of sleep mode consume additional power in mobile device 102. *See id.* at 2:2–8.

To reduce power consumption of mobile device 102, Heinrich discloses that baseband processor 104 includes scheduler 120. *Id.* at 7:8–10. Scheduler 120 may be configured to reduce power consumption by reducing the number of times a processor is awakened from its sleep mode. *Id.* at 7:16–19. Scheduler 120 may be configured to schedule communication in either direction between baseband processor 104 and application processor 106. *Id.* at 7:19–21. Alternatively, scheduler 120 may schedule only communication from baseband processor 104 to application processor 106, and another scheduler (not shown) implemented within application processor 106 may schedule communication in the opposite direction. *Id.* at 7:21–27. In general, scheduler 120 is operable to identify communications awaiting transmission from one processor to the other processor that are not real-time critical so that they may be delayed until a later time to avoid causing another sleep-to-awake mode transition of the other processor. *Id.* at 7:65–8:1. By grouping the non-real-time sensitive exchanges together and scheduling them for communicating to the other processor during a period in which the other processor is continuously in the awake mode, the number of times that the other processor enters and exits the sleep mode is reduced. *Id.* at 4:6–11.

Heinrich's Figure 3 is reproduced below.

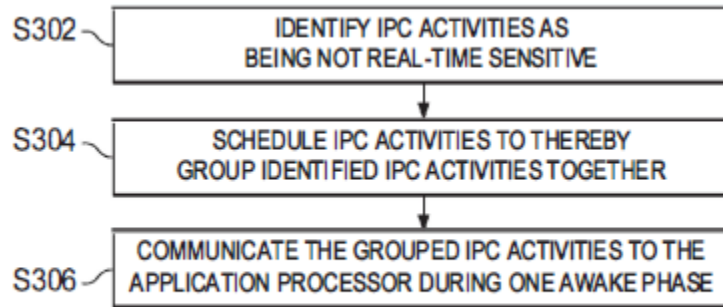


FIG. 3

Figure 3 is a flowchart describing operation of a scheduler. At step S302, scheduler 120 determines which pending communications awaiting transmission to the other processor are not real-time sensitive. *Id.* at 8:10–16. Non-real-time data is that which may be delayed, and, conversely, real-time data is that which must be transmitted without delay (e.g., voice communications). *Id.* at 8:14–20. Step S304 groups the identified non-real-time data for delayed transmissions and schedules them for transmission during a single awake mode of the other processor. *Id.* at 8:21–32. Step S306 transmits the grouped, delayed, non-real-time data to the other processor during a single awake mode—i.e., during a period of time in which the other processor is continuously awake. *Id.* at 8:33–49.

2. Overview of Balasubramanian (Ex. 1005)

Balasubramanian is directed to grouping packets of data to be exchanged by buffering packets destined for a device that is presently in a low power mode. Ex. 1005, 1:16–45. Balasubramanian’s Figure 1 is reproduced below.

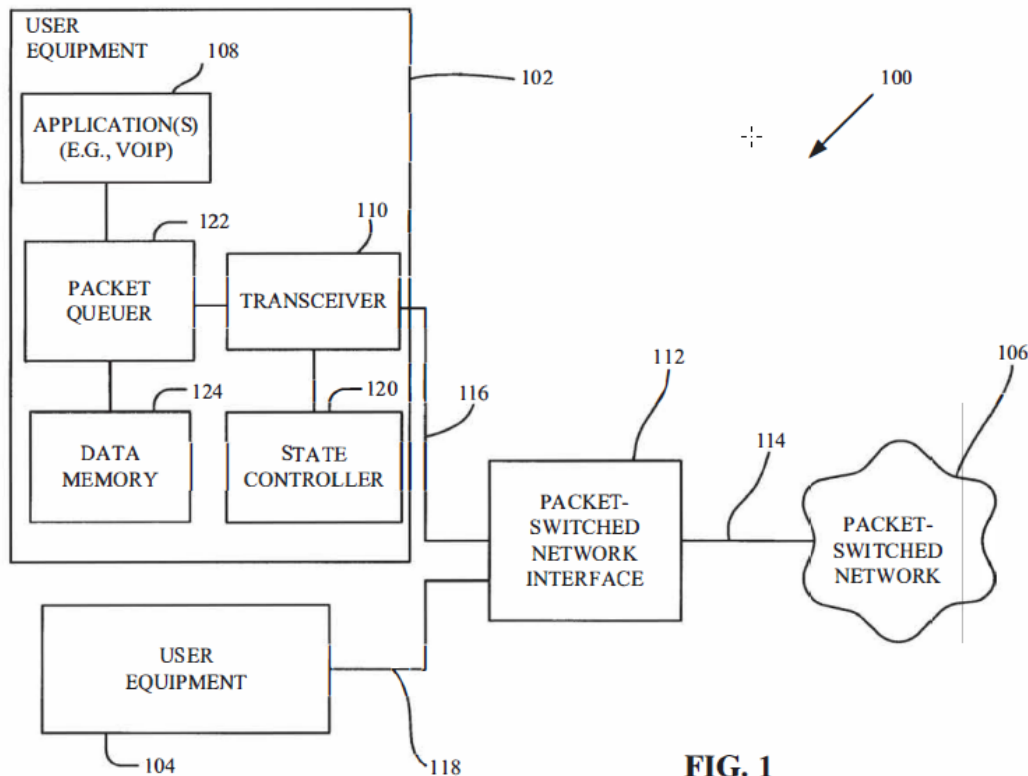


FIG. 1

Figure 1 depicts a system adapted to transmit and receive groups of packets. *Id.* at 3:15–17. System 100 includes user equipment 102 and 104 coupled to packet-switched network 106 to group packets for transmission and, thereby, reduce power consumption. *Id.* at 4:1–5. User equipment 102 and 104 may each be, for example, a mobile phone, a laptop computer, a wireless device or modem, or other types of communication devices wishing to connect with another user equipment or with packet-switched network 106. *Id.* at 4:24–29. User equipment 102 includes transceiver 110 to provide a physical layer interface for transmissions to and from user equipment 102. *Id.* at 4:37–42. User equipment 102 and 104 communicate with packet-switched network 106 through packet-switched network interface 112 (via communication links 116, 118, and 114). *Id.* at 4:43–57.

Transceiver 110 in user equipment 102 may be switched between an active state (ready to send or receive data) and a suspended state (saving

power but not ready to send or receive data). *Id.* at 5:30–46. To conserve power, while transceiver 110 is in a suspended state, user equipment 102 and interface 112 may queue packets to be sent through transceiver 110. *Id.* at 5:47–51.

Here, power may be conserved by not transitioning the transceiver **110** from the suspended state to the active state every time a packet has been generated for transmission by the user equipment **102** or every time it is expected that the user equipment **102** will receive a packet. Accordingly, power savings may be achieved by rescheduling the packet traffic into groups of traffic.

Id. at 5:55–61. To enable this power saving, “user equipment **102** and/or the network interface **112** may be adapted to queue packets while the transceiver **110** is in the suspended state.” *Id.* at 5:47–51.

Figure 2 of Balasubramanian is reproduced below.

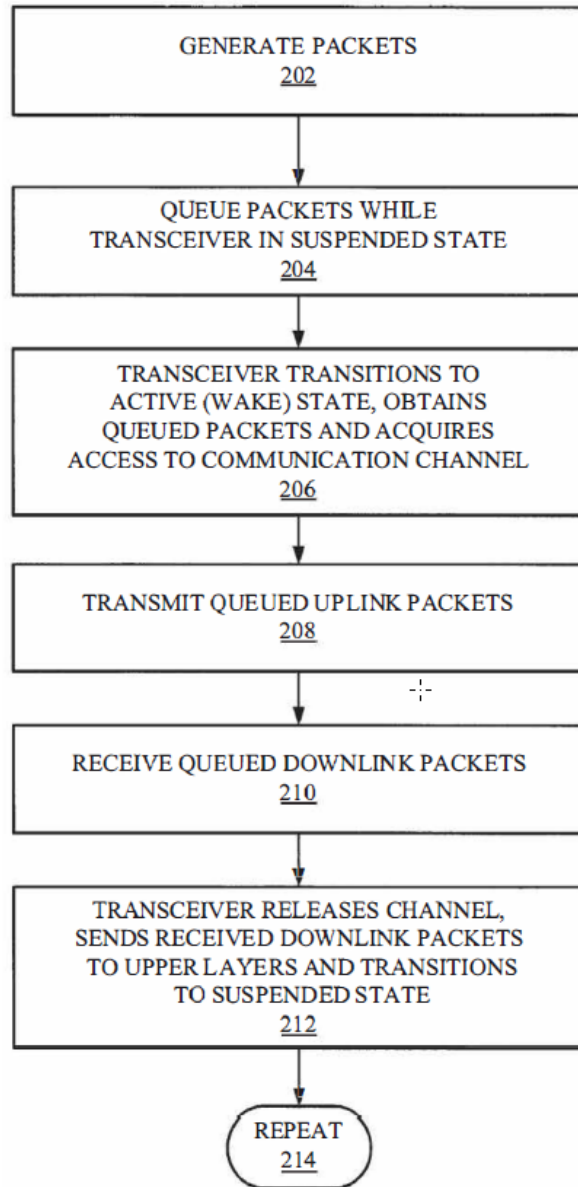


FIG. 2

Figure 2 is a flowchart of operations to send or receive a group of packets. *Id.* at 3:18–20. At step 202, user equipment 102 generates data as packets to be sent to packet-switched network 106. *Id.* at 6:29–31. At step 204, user equipment 102 queues the generated packets while transceiver 110 is in a suspended state. *Id.* at 6:40–43. At step 206, transceiver 110 awakens from its suspended state and obtains queued packets for transmission to packet-switched network 106. *Id.* at 6:55–62. At step 208, transceiver 110

transmits the queued packets over path 116—all queued packets may be retrieved and transmitted during the present single awake state of transceiver 110. *Id.* at 6:63–67. In addition, during the same single awake state at step 210, network interface 112 may “use the receipt of an uplink packet as a trigger to transmit any downlink packets in its queue” to transceiver 110. *Id.* at 7:4–8. Alternatively, transceiver 110 may send a message to interface 112 requesting transmission of any queued downlink packets up to transceiver 110. *Id.* at 7:8–13.

3. *Motivation to Combine Heinrich and Balasubramanian*

Petitioner argues the ordinarily skilled artisan would have been motivated to combine Balasubramanian’s disclosed pulling of data with Heinrich’s disclosed inter-processor communication scheduling for the following reasons.

a) *Analogous Art*

Whether a reference in the prior art is “analogous” is a factual question. *In re Clay*, 966 F.2d 656, 658–659 (Fed. Cir. 1992) (citing *Panduit Corp. v. Dennison Mfg.*, 810 F.2d 1561, 1568 n.9 (Fed. Cir. 1987)). Two criteria have evolved for determining whether prior art is analogous: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the inventor’s endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved. *Id.* (citing *In re Deminski*, 796 F.2d 436, 442 (Fed. Cir. 1986); *In re Wood*, 599 F.2d 1032, 1036 (CCPA 1979)).

(1) *Same Field of Endeavor*

Petitioner argues Balasubramanian and Heinrich are in the same field of endeavor addressing the same issues of reducing power consumption

when transitioning from low power to high power states. Pet. 47–48. In particular, Petitioner argues Heinrich and Balasubramanian disclose “similar architectures that include two processing nodes coupled by a bus, buffering data on both sides of the bus to allow for power savings states, and the use of a timer in one or both processing nodes to determine when to send queued data to the other processing node.” *Id.* (citing Ex. 1004, 4:6–11; Ex. 1005, 5:55–61; Ex. 1002 ¶ 100). Second, Petitioner argues both references “solve the power consumption problem in the same way: minimizing the number of transitions from low power-to-high power states.” Pet. 48 (citing Ex. 1002 ¶ 101).

Patent Owner argues Petitioner’s analysis depends on an overly broad characterization of the relevant field of endeavor and the teachings of Balasubramanian because the claims of the ’490 patent are directed to a mobile terminal comprising multiple processors but Petitioner broadens that field to encompass Balasubramanian’s two separate processing nodes coupled by a network. PO Resp. 62–63. Patent Owner contends that framing the field so broadly “conceivably encompasses any two electronic devices, as long as they are connected over a network.” *Id.* at 63. Patent Owner asserts that the proper field of endeavor is “power saving in a single mobile terminal and intra-device communication.” Sur-Reply 38. In other words, Patent Owner argues the field is defined as power savings where the two devices connected by the interconnectivity bus must physically reside within the same single mobile terminal. By contrast, Patent Owner argues, “Balasubramanian, on the other hand, relates to communications between different devices” and “devices connected over a network have a different set of power consumption objectives and different power management

schemes than IPC activities on a single user device.” *Id.* at 38–39 (citing Ex. 2007 ¶¶ 123–127).

We are persuaded that Heinrich and Balasubramanian are in the same field of endeavor as the ’490 patent. Initially, we observe the ’490 patent broadly characterizes its field of endeavor as “power saving techniques in computing devices.” Ex. 1001, 1:20–21. Heinrich appears on its face to be in the same field in that it is directed to saving power in a computing system. *See, e.g.*, Ex. 1004, code (54) (“POWER-EFFICIENT INTER PROCESSOR COMMUNICATION SCHEDULING”), 1:16–17 (“[I]t is important to keep the power consumption of the computer system at a low level.”), 4:6–11 (“By grouping the non real-time sensitive IPC activities together and scheduling them for communicating to the second processor during a period in which the second processor is continuously in the first mode, the number of times that the second processor enters and exits the second mode (e.g. sleep mode) is reduced. This reduces the power consumed by the computer system in handling the IPC activities.”). In like manner, Balasubramanian appears on its face to be in the same field. *See, e.g.*, Ex. 1005, code (54) (“ACHIEVING POWER SAVINGS THROUGH PACKET GROUPING”), code (57) (“Power savings may be achieved in a packet-switched system by grouping packets.”), 1:52–53 (“In some aspects power savings are achieved in an apparatus by grouping packets.”), 5:55–61 (“Here, power may be conserved by not transitioning the transceiver 110 from the suspended state to the active state every time a packet has been generated for transmission by the user equipment 102 or every time it is expected that the user equipment 102 will receive a packet. Accordingly, power savings may be achieved by rescheduling the packet traffic into groups of traffic.”). Furthermore, both Heinrich and Balasubramanian disclose these problems and solutions arise in

the context of mobile devices. Ex. 1004, 1:14–17 (“However, for computer systems implemented on user devices, such as mobile smart phones and tablets, it is important to keep the power consumption of the computer system at a low level”), Ex. 1005, 1:30–34 (“Also, mobile devices traditionally operate on battery power. In this case, reducing the power consumed by the mobile device effectively increases the talk time of the device between recharges of the battery.”). Still further, both Heinrich and Balasubramanian disclose a solution to the problem by grouping transmissions between two processors to save power by reducing the number of transitions of a processor into a sleep mode. Pet. 47 (citing Ex. 1004, 4:6–11, Ex. 1005, 5:55–61).

Both references expressly disclose the same advantage, reducing power consumption, by essentially the same techniques, grouping transmissions between processors to reduce power state transitions of the processors. Thus, we are persuaded the references are in the same field of endeavor—reducing power consumption in mobile devices—as the ’490 patent.

We are not persuaded by Patent Owner’s argument that the field of endeavor is narrowed to “power saving in a single mobile terminal and intra-device communication.” Sur-Reply 38. Patent Owner argues that the agreed upon level of skill in the art requires experience in “mobile device architecture and multiprocessor systems” and, apparently believes such a skilled person would not consider Balasubramanian because the identified processors (110 and 112) are not both within the user equipment 102 (the mobile device). *Id.* at 38–40. Patent Owner’s analysis is premised on its suggested narrow field of endeavor—a field essentially limited to that of the

claims of the '490 patent. We decline to so narrow the field of endeavor of the references.

(2) *References Solve a Reasonably Pertinent Problem*

Patent Owner argues Balasubramanian is “not pertinent to the problems and solutions of the '490 patent” because,

Balasubramanian is concerned only with managing processor wake states, not activity states of any interconnectivity bus. In contrast, the '490 Patent is directed towards the more granular technique of minimizing the active state and the state transitions of the *interconnectivity bus*. Accordingly, Petitioner fails to present any persuasive reason why a POSITA would look to Balasubramanian to address the problems solved by the '490 Patent.

Sur-reply 40.

For essentially the same reasons as above regarding the field of the invention, we are not persuaded by Patent Owner’s argument that, again, narrowly focuses on the problems addressed by the claimed invention. We are persuaded both Heinrich and Balasubramanian address a problem reasonably pertinent to the particular problem addressed in the '490 patent. As discussed *supra* in the invention’s field of endeavor, we understand the problem addressed by the '490 patent more broadly as reducing power consumption of a computing device by reducing power state transitions within the device. *See, e.g.*, Ex. 1001, 1:20–21 (“[t]he technology of the disclosure relates generally to power saving techniques in computing devices”). The '490 patent specifically addresses this problem by synchronizing transmissions in both directions between processors, thereby reducing the number of low to high (active) power state transitions of an interconnectivity bus between processors. *See, e.g., id.* at 2:12–15 (“By holding or accumulating the data at a source processor in this fashion,

unnecessary transitions between low power states and active states on the PCIe bus are reduced and power is conserved.”), 5:33–35 (“By holding or accumulating the data at a source processor in this fashion, unnecessary transitions between low power states and active states on the PCIe bus are reduced and power is conserved.”), 8:41–48 (“[e]xemplary aspects of the present disclosure reduce the number of transitions (i.e., 60, 62) from low power to active power by synchronizing packet transmission from the modem processor 44 and the application processor 34”).

However, as noted *supra*, Patent Owner acknowledges that the ’490 patent is not limited to the exemplary embodiments disclosed therein. Thus, we find the problem addressed more generally to be reducing power consumption of a computing device by reducing power state transitions within the device. Whether the transitions are those of processors within the device or an interconnectivity bus within the device, the broader problem being addressed is the same—reduce power consuming power state transitions.

Furthermore, Patent Owner acknowledges that a “bus,” per se, is merely a collection of wires/conductors—a passive entity over which interface circuits exchange information. *See* Tr. 40:17–42:14. In other words, a PCIe or USB bus is merely a passive collection of wires that has no power states itself but becomes a PCIe bus, having various power states, by virtue of being coupled to a PCIe interface circuit—i.e., coupled to a processor/circuit that senses and applies signals to the wires in accord with the PCIe standards. Thus, a bus, per se, does not have any associated power states but, rather, the interface circuits coupled to the conductors/wires of the bus may transition between power states as data is transferred over the bus in accord with the specific protocol employed.

Based on our determination of the problem addressed by the '490 patent, Heinrich resolves a similar problem, which would be reasonably pertinent to the ordinarily skilled artisan, by holding data until a more opportune time to send data from one processor to another to eliminate some low to high power transitions within the computing device. *See, e.g.*, Ex. 1004, 4:6–15 (“By grouping the non real-time sensitive IPC activities together and scheduling them for communicating to the second processor during a period in which the second processor is continuously in the first mode, the number of times that the second processor enters and exits the second mode (e.g. sleep mode) is reduced. This reduces the power consumed by the computer system in handling the IPC activities.”), 10:44–47 (“delaying some of the IPC activities to thereby group them together . . . results in fewer transitions between the sleep and awake modes on the application processor 106”). Balasubramanian also resolves a similar problem, which would be reasonably pertinent to the ordinarily skilled artisan, by holding data until a more opportune time to send data from one processor to another to eliminate some low-to-high power transitions within the computing device. *See, e.g.*, Ex. 1005, 1:52–53 (“In some aspects power savings are achieved in an apparatus by grouping packets.”), 5:55–61 (“Here, power may be conserved by not transitioning the transceiver 110 from the suspended state to the active state every time a packet has been generated for transmission by the user equipment 102 or every time it is expected that the user equipment 102 will receive a packet. Accordingly, power savings may be achieved by rescheduling the packet traffic into groups of traffic.”), 14:56–59 (“By ‘waking’ less often to transmit and/or receive packets, the number of transitions between active and suspended states (e.g., turning the transceiver on and off) will be reduced.”).

(3) Heinrich and Balasubramanian are Analogous Art

Accordingly, we are persuaded by Petitioner's arguments that Heinrich and Balasubramanian are analogous art to the '490 patent both because they are in the same field of endeavor and because they address a problem that is reasonably pertinent to the particular problem with which the '490 patent inventor is involved. However, that finding alone is insufficient to establish a reason why the ordinarily skilled artisan would have combined the references.

b) Balasubramanian's Pulling Fits in Heinrich's Scheduling of a "Good Time"

As discussed further below, Petitioner relies on Balasubramanian primarily for its disclosure of one device pulling data from another device (as the term "pull" has been construed) (*see* Pet. 51–56) and for its disclosure of an event being "triggered by" another event (as the term "triggered by" has been construed) (*see* 1293PET 39–45). Petitioner argues Balasubramanian's disclosure of sending data from a first node to a second node and then, following the transmission, pulling data from the second node to the first node, fits well in the scheduler architecture of Heinrich. Pet. 48. In particular, Petitioner argues "Heinrich teaches that a 'good time' to schedule communications over the IPC link is when the application processor is in the awake state, and one way to know that a processor is in an awake state is when data is being transmitted to it." *Id.* at 48–49 (citing Ex. 1004, 7:19–21, 9:13–21; Ex. 1002 ¶ 102); *see also* 1293PET 53–54. Petitioner further argues Balasubramanian's approach of combining transmission and receipt of packets into a single active power state of its transceiver saves power and contends the ordinarily skilled artisan "would realize that the same advantages taught by Balasubramanian would be

gained by applying the same approach to the system in Heinrich.” Pet. 49–50 (citing Ex. 1005, 1:52–62, 5:55–61, 14:49–63; Ex. 1002 ¶ 103); *see also* 1293PET 53–54. Petitioner contends, “Applying the power-saving approach in Balasubramanian to Heinrich would result in a system in which the application processor buffers its data until it is pulled by the modem processor, which occurs after the modem processor transmits data to the application processor and during the same active state of the apparatus.” Pet. 50 (citing Ex. 1002 ¶ 103). Still further, Petitioner contends,

Because Heinrich similarly discloses a bus with low and high power states and performing a data transfer between two processors during a single wake state of a bus, a person of ordinary skill in the art would have been motivated to apply Balasubramanian’s teaching of performing push and pull transactions during a single wake state of communication link 116, to the system of Heinrich, to create a system in which a modem processor pushes data to, and pulls data from, an application processor during a single active state of the communication link between the modem processor and application processor.

Pet. 53 (citing Ex. 1002 ¶ 109).

Patent Owner argues there is no motivation to combine Balasubramanian with Heinrich because “[n]either reference recognizes the problem addressed by the ’490 Patent” and “[t]hus there is no motivation to combine the references in the manner claimed to solve this unrecognized problem.” PO Resp. 58 (citing Ex. 2007 ¶ 114); *see also id.* at 61 (“[T]here is certainly no motivation to combine the references in the manner claimed to address a problem that no prior art of record recognizes as even being a problem” (citing Ex. 2007 ¶ 120)); *id.* at 65 (arguing that a “POSITA would not have been motivated to combine Heinrich and Balasubramanian in the

manner proposed by Petitioner to address a problem unrecognized by the prior art evidence of record”); Sur-Reply 36–38.

We are not persuaded by Patent Owner’s argument because it is premised on Patent Owner’s narrower understanding of the field of endeavor and the corresponding problem addressed by the ’490 patent and the references. As discussed *supra*, we are persuaded by Petitioner that the references are in the same field of endeavor and address a problem reasonably pertinent to the inventor of the ’490 patent.

In support of its position, Patent Owner further argues that the Federal Circuit has held that one small design change can cause unpredictable results. PO Resp. 61–62 (citing *Nichia Corp. v. Everlight Americas, Inc.*, 855 F.3d 1328, 1339 (Fed. Cir. 2017)).

We are unpersuaded by this argument. Initially, it is unclear to us what one small design change Patent Owner is referring to in the proposed combination. Regardless, as Petitioner correctly observes, the Court in *Nichia* found that the prior art reference at issue disclosed “different structures, resolve[d] dissimilar problems, and propose[d] dissimilar solutions.” Reply 38 (quoting *Nichia*, 855 F.3d at 1339). Here, as discussed *supra*, we have determined that the references disclose similar structures (a mobile device with two processors coupled by a bus), resolve similar problems (reduce power consumption by reducing power state transitions within the mobile device), and propose similar solutions (pull data from the first processor when the second processor has sent data to the first processor or triggering transmission of held data following receipt of data—i.e., during a single power state).

Patent Owner also contends Heinrich and Balasubramanian solve the power consumption problem in different ways that are “in conflict” and,

thus, there would be no motivation to combine the references. PO Resp. 64. Specifically, Patent Owner argues Balasubramanian's approach "contemplates that the intra-device processes and processing components must remain active in order to queue packets for transmission," which conflicts with Heinrich's goal to "minimize the time the application processor or baseband processor spends in an active state." *Id.* at 64–65 (citing Ex. 1005, 5:20–22, 27–29; Ex. 2007 ¶ 126).

We remain unpersuaded by Patent Owner's argument. We discern no conflict in the references that negates Petitioner's proposed motivation for the ordinarily skilled artisan to have considered combining the references.

c) Reasonable Expectation of Success in the Combination

Petitioner argues the ordinarily skilled artisan would have had a reasonable expectation of success in combining Balasubramanian's data pull technique with Heinrich because both push and pull techniques for transferring data were well-known and the combination would not have required alterations to the bus protocols coupling Heinrich's processors but, instead, "would merely have involved routine scheduling, which would also have been considered trivial to a person of skill in the art." Pet. 50–51 (citing Ex. 1002 ¶ 104); *see also* 1293PET 54–57.

Patent Owner does not expressly direct any of its arguments toward these assertions of Petitioner.

On this record, we are persuaded by Petitioner's arguments that the ordinarily skilled artisan would have had a reasonable expectation of success in adding Balasubramanian's disclosure of pulling data to Heinrich's disclosures to achieve the benefits of Balasubramanian and thereby arrive at the claimed invention.

*d) Conclusion Regarding Motivation to Combine
Heinrich and Balasubramanian*

In view of the above discussion, we are persuaded by Petitioner's arguments that the ordinarily skilled artisan would have been motivated to add Balasubramanian's disclosure of pulling data or triggering a transmission of data to Heinrich's disclosures to achieve the express benefits of Balasubramanian and thereby arrive at the claimed invention. Thus, Petitioner has articulated reasons the ordinarily skilled artisan would have combined the references based on rational underpinnings with a reasonable expectation of success.

4. Claims 1 and 31

Petitioner identifies each structural element of claims 1 and 31 in Heinrich and the various functions of the recited elements in the combined teachings of Heinrich and Balasubramanian. Specifically, the "mobile terminal" recited in the preamble of each claim is identified as Heinrich's "user device 102." Pet. 30 (citing Ex. 1001, 6:37–41; Ex. 1004, 4:21–23, Fig. 1); 1293PET 29 (citing Ex. 1001, 6:37–41; Ex. 1004, 4:21–23, Fig. 1). The recited "modem timer" of claim 31 is identified as the "lazy timer" of Heinrich, one or more of which are used by scheduler 120 to control IPC activities in both directions of data exchange. Pet. 30–31 (citing Ex. 1004, 7:8–21, 9:2–6; Ex. 1002 ¶ 76); 1293PET 29–30 (citing Ex. 1004, 7:8–21, 9:2–6; Ex. 1018 ¶ 78).

The recited "modem processor" is identified as Heinrich's "baseband processor 104." Pet. 31–32 (citing Ex. 1004, 4:30–36, Fig. 1; Ex. 1002 ¶ 77); 1293PET 30–31 (citing Ex. 1004, 4:30–36, Fig. 1; Ex. 1018 ¶ 79). Claims 1 and 31 recite that the modem processor is "configured to hold modem processor to application processor data until expiration of the

modem timer.” In other words, the modem processor holds received downlink data from a network until the modem timer expires. Petitioner argues Heinrich discloses this function because “Heinrich teaches that baseband processor 104 delays sending certain data to the application processor 106 over the IPC interface, and transmits such data upon expiration of the modem timer.” Pet. 32–33; 1293PET 31–32. Specifically, Petitioner argues Heinrich discloses that IPC activities (i.e., data to be transferred between processor) that are not real-time sensitive “can be delayed until it is deemed profitable to run them.” Pet. 33 (citing Ex. 1004, 7:65–8:1); 1293PET 32 (citing Ex. 1004, 7:65–8:1). Heinrich associates a “lazy timer” with each such delayed IPC activity and when any one of the timers expires, all the delayed IPC activities are aggregated and transmitted at the same time. Pet. 33 (citing Ex. 1004, 9:5–13); 1293PET 32 (citing Ex. 1004, 9:5–13). Heinrich further discloses that buffering, delaying, and aggregating such IPC activities results in fewer sleep mode to awake mode transitions of the applications processor and, thus, reduces power consumption of the user device. Pet. 33–34 (citing Ex. 1004, 10:44–51, 11:57–58; Ex. 1002 ¶ 78); 1293PET 32 (citing Ex. 1004, 10:44–51, 11:57–58; Ex. 1018 ¶ 80).

The Petition identifies the recited “application processor” of claim 31 as Heinrich’s “application processor 106.” Pet. 37 (citing Ex. 1004, 4:36–42, Fig. 1; Ex. 1002 ¶ 84); 1293PET 35 (citing Ex. 1004, 4:36–42, Fig. 1; Ex. 1018 ¶ 86). We address the recited function of the application processor in both claims below.

Lastly, the Petition identifies the recited “interconnectivity bus communicatively coupling the application processor to the modem processor” as Heinrich’s “IPC” coupling baseband processor 104 (i.e., the

recited mode processor) to application processor 106 (i.e., the recited application processor). Pet. 38 (citing Ex. 1004, 4:65–5:1, Fig. 1; Ex. 1002 ¶¶ 85–86); 1293PET 36–37 (citing Ex. 1004, 4:44–50, Fig. 1; Ex. 1018 ¶ 88).

Patent Owner does not dispute the above mappings of recited elements of claims 1 and 31 to features of Heinrich. Patent Owner’s disputes derive from recitations of the claims regarding overall function of the claimed mobile terminal and some of the functional interactions between the claimed structural elements. In particular, the function of the application processor and its interactions with the modem processor over the interconnectivity bus, as identified in each of claims 1 and 31, form the basis of Patent Owner’s disputes.

We address Petitioner’s identification of these functions and the related disputes below.

a) Application Processor Holds Data Until...

Both claims 1 and 31 recite that the application processor is configured to “hold application processor to modem processor data until” a particular recited condition is met. The conditions to be met vary between claims 1 and 31 but the requirement that the application processor holds uplink data is common to both claims and is disputed between the parties. So too, the particular condition recited in each claim is disputed between the parties.

We address each of these disputes below.

(1) Application Processor Holds Uplink Data

Both claims 1 and 31 recite that the “application processor is configured to hold” uplink data until a condition occurs and the condition is different between claims 1 and 31. We address the recited condition of each

claim and the responsive functions below. First we address a dispute as to whether both the modem processor and the application processor, as disclosed in the proposed combination, can both store data as claimed. Thus, we address the arguments with respect to claim 31.

Regarding claim 31, Petitioner argues the combination of Heinrich and Balasubramanian discloses holding/buffering of data between the processors. Pet. 39–43. In particular, Petitioner argues Heinrich discloses scheduler 120 on baseband processor 104 (modem processor) holds downlink data bound for the application processor (an IPC activity) until a lazy timer expires and, when any one lazy timer expires, for any corresponding IPC activity that is held/buffered, transfers all such buffered IPC activity (i.e., held downlink data) to the application processor. Pet. 39–40, 32–34 (citing Ex. 1002 ¶ 78); *see also* Section II.D.4 above discussing the modem processor holding of downlink data. Petitioner further argues Heinrich discloses that the same buffering methods can be used for the opposite direction of transmissions (i.e., buffering uplink data in the application processor until a lazy timer expires). Pet. 40 (quoting Ex. 1004 12:52–55) (“A scheduler may implement the *same scheduling techniques* as those described above [for scheduling IPC activities from the baseband processor 104 to the application processor 106], but configured to schedule IPC activities *from the application processor 106 to the baseband processor 104.*”); Ex. 1002 ¶ 89. Petitioner contends Heinrich also discloses that a separate scheduler may control transmissions of uplink data from the application processor to the baseband processor in the same manner as the scheduler for the downlink data. Pet. 40–41 (citing Ex. 1004, 7:7–27, 7:65–8:1; Ex. 1002 ¶ 90).

Regarding claim 1, Petitioner identifies similar disclosures of Heinrich as discussed above for teaching the same function in claim 1 as in claim 31 (application processor configured to hold uplink data). *See* 1293PET 37–38; *see also id.* at 21–23, 29–33, 37–41, 45–47.

Patent Owner argues Heinrich cannot disclose an application processor holding uplink data as required “because, as admitted by Petitioner’s expert [(in the ITC proceeding)] Dr. Yalamanchili, there is no scenario in Heinrich where the baseband processor and the application processor accumulate data at the same time, a requirement of this limitation.” PO Resp. 42–43 (citing Ex. 2008, 206:5–11, 212:6–13, 207:15–17; Ex. 2007 ¶¶ 87–89). Patent Owner also argues that, “[b]ecause Petitioner’s expert [(Dr. Yalamanchili)] has admitted that Heinrich does not teach simultaneous accumulation on both processors on its IPC, and because the Institution Decisions have confirmed that Balasubramanian is not being cited for” this limitation of an application processor configured to hold uplink data, the requirement for an application processor holding uplink data is not met by the proposed combination. *Id.* at 43; *see also* Sur-Reply 8–10.

Petitioner argues in reply, “Heinrich describes a single ‘centralized scheduler’ 120 that can reside on the modem processor and can ‘control the scheduling of IPC activities *in both directions*.’” Reply 14 (citing Pet. 31, 40; Ex. 1004, 7:8–21; Ex. 1023 ¶ 16; Ex. 1026, 43:10–14). Petitioner further argues, “For an application processor to hold data and/or transmit held data, the application processor must be awake; and for a centralized scheduler running on the modem processor to control transmissions of held data from the application processor, the modem processor also must be awake.” *Id.* (citing Ex. 1023 ¶ 16; Ex. 1026, 44:22–45:4). Petitioner also argues that Dr. Yalamanchili’s testimony relied upon by Patent Owner does

not support Patent Owner's arguments but, instead, is consistent with Petitioner's position regarding the teachings of Heinrich. Reply 15–17.

Initially as discussed *supra*, we accord less weight to Dr. Yalamanchili's testimony because his testimony is incomplete in our record and he was testifying in a different proceeding, in a different forum (ITC), that applies a different claim construction standard and standard of proof. We find Patent Owner's arguments unavailing. We agree with Petitioner that Patent Owner fails to identify any disclosure of Heinrich that supports its proposition that Heinrich cannot accumulate data on both processors "at the same time." Reply 14; *see also* PO Resp. 42–43; Sur-Reply 10–11. Still further, there is no recitation in the '490 patent claims that either processor's hold of data destined for the other is conditioned on the other processor simultaneously holding data destined in the other direction. In other words, nothing in claims 1 or 31 expressly requires both processors to accumulate data (i.e., hold data) simultaneously (at the same time).

Moreover, we are persuaded Heinrich teaches, or at least suggests, the limitation that the application processor hold uplink data and, to whatever extent required by the '490 patent claims, also discloses that both processors may hold/accumulate data at the same time. Heinrich expressly discloses,

[T]here is a centralized scheduler 120 which is associated with the baseband processor 104. In the example shown in FIG. 1, the scheduler 120 is implemented as a software module on the baseband processor 104. However, in other embodiments the scheduler 120 may be implemented by one or more software and/or hardware modules on the user device 102. The scheduler 120 schedules the communication of IPC activities between the processors 104 and 106.

Ex. 1004, 7:8–16; *see also* Pet. 23, 30–34, 39–41. Heinrich further discloses that its scheduler, implemented in the baseband processor, "may control the

scheduling of IPC activities in both directions between the processors 104 and 106” and, in the alternative, separate, corresponding, schedulers may be implemented within each processor and may control IPC activities directed from its corresponding processor to the other processor. *Id.* at 7:19–27; *see also* Pet. 23, 30–34, 39–41. Still more explicitly, Heinrich discloses,

In the examples described in detail above, the scheduler 120 schedules the IPC activities for communicating from the baseband processor 104 to the application processor 106. In that case, the application processor 106 is the remote processor for the IPC and the baseband processor 104 is the local processor for the IPC. A scheduler may implement the same scheduling techniques as those described above, but configured to schedule IPC activities from the application processor 106 to the baseband processor 104. In the same way, as described above, the scheduler may group non real-time sensitive IPC activities together (e.g. using lazy timers) to thereby send IPC activities in a group from the application processor 106 to the baseband processor. The scheduler for scheduling IPC activities for communicating from the application processor 106 to the baseband processor 104 may, or may not, be the same as the scheduler 120 which schedules the IPC activities for communicating from the baseband processor 14 to the application processor 106 as described above.

Ex. 1004, 12:47–64 (emphasis added). Thus, Heinrich expressly discloses that IPC activities “*between the processors 104 and 106*” are scheduled by scheduler 120 without limitation as to the direction of information being transmitted. Ex. 1004, 7:15–16 (emphasis added). We discern no limitation in Heinrich that IPC activities, under control of a scheduler 120, can only be delayed by a processor when the other processor is not awake. Patent Owner asserts such limitations without pointing to any teachings of Heinrich. Accordingly, we determine that Heinrich expressly discloses one

or more schedulers that control data exchanges (IPC activities) in both directions between application processor 104 and baseband processor 106.

Furthermore, Heinrich's scheduler 120 is operable to control IPC activities by "delaying" an IPC activity until a more profitable time to send. Ex. 1004, 7:65–8:1; *see also* Pet. 23, 30–34, 39–41. We determine that a data exchange (an IPC activity) that is "delayed" by scheduler 120 in Heinrich is "held"¹⁵ as required by this limitation.

Moreover, even if such a requirement (accumulating data on both processors "at the same time") is inferred or implied in some manner in the limitations of claims 1 or 31, Heinrich meets such a limitation. Patent Owner's argument is supported only by Dr. Baker's declaration repeating the same assertions as Patent Owner, and quoting the same portions of Dr. Yalamanchili's deposition testimony, as evidence that Heinrich fails to disclose such a feature. *See* PO Resp. 43 (citing Ex. 2007 ¶¶ 87–89). Patent Owner's argument presumes that if both of Heinrich's processors are awake, scheduler 120, which controls IPC activities, would never delay/hold any IPC activity—i.e., if the other processor is awake, data is not delayed/held but sent immediately to the other processor. Again, Patent Owner points to

¹⁵ The parties have not proffered any construction of "hold," as recited in the claims, and we discern no need for an express construction. We note, however, that the ITC Commission Opinion, applying narrower *Phillips* standard construction, expressly construed "hold" to mean "prevent data from traveling across the bus or to store, buffer, or accumulate data." Ex. 1022, 15–17. To the extent any construction is needed, a need we do not perceive, we determine the broadest reasonable interpretation is at least as broad as the ITC Commission Opinion's interpretation. Under such an interpretation, Heinrich's disclosure of "delaying" IPC activities would be understood as "holding" IPC activities because it is preventing data from traveling across the bus, until a better time for the activity.

nothing in Heinrich in support of such a presumption and we discern no such limitation in Heinrich. Dr. Baker characterizes the teachings of Heinrich and, in a portion of that characterization, cites the entirety of Heinrich's column 7, lines 8–27, but quotes only selected portions thereof, seemingly ignoring the express disclosure that scheduler 120 controls IPC activities “in both directions.” *See* Ex. 2007 ¶¶ 73–74. Despite this clear disclosure of Heinrich, Dr. Baker suggests Heinrich's scheduler only delays non-real-time data in *one* direction. *Id.* ¶ 74 (delaying non real-time IPC activities “applies to one direction of the traffic between the processors, for example from an active secondary processor to the application processor.”). We do not find this testimony credible because it directly contradicts the clear disclosure of Heinrich that scheduler 120 controls IPC activities in both directions by delaying (holding) a transaction. Ex. 1004, 7:8–27, 12:47–64. Furthermore, as Petitioner asserts, if scheduler 120 operates on the modem processor, controlling IPC activities there, the modem processor must be awake and, if scheduler 120 also controls IPC activities on the application processor (i.e., in both directions), then the application processor must also be awake when such IPC activities are controlled by the scheduler. Reply 14–15. Thus, even assuming, *arguendo*, that claims 1 and 31 require accumulating/holding data on both processors “at the same time,” an assumption we do not adopt, Heinrich still meets this limitation.

We are also unpersuaded by Patent Owner's argument that Petitioner's Reply to the Patent Owner's Response raised a new argument not previously asserted in the Petition by referring to Heinrich's disclosure of a centralized scheduler running on the modem processor. Sur-Reply 11–14 (alleging Reply 14 puts forth a new argument). We are not persuaded that Petitioner's reference to a “centralized scheduler” in the Reply is a new

argument—regardless of where the “centralized scheduler” is implemented. Heinrich specifically discusses a “centralized scheduler 120” in the full paragraph starting at column 7, line 8 and clarifies that the “centralized scheduler “is associated with the baseband processor.” Ex. 1004, 7:8–9. Later in that same paragraph, Heinrich discloses that the scheduler “may be implemented by one or more software and/or hardware modules on the user device 102.” *Id.* at 7:12–14. Still further in the same paragraph, Heinrich discloses that each processor (application and baseband processors) may implement its own scheduler. *Id.* at 7:21–27. Petitioner has consistently identified Heinrich’s paragraphs at column 7, lines 8–27 and column 12, lines 47–64 for disclosures relating to Heinrich’s scheduler 120—paragraphs that clearly disclose a variety of configurations for scheduler 120, including a “centralized scheduler,” and clearly disclose that the scheduler controls exchanges in both directions (i.e., delays (holds) transmissions between the two processors). Pet. 24 (citing Ex. 1004, 12:52–55), 30–31 (citing Ex. 1004, 7:8–21), 40–41 (citing Ex. 1004, 7:19–27, 12:52–55), 48 (citing Ex. 1004, 7:19–21); 1293PET 22 (citing Ex. 1004, 12:52–55), 29–30 (citing Ex. 1004, 7:8–21), 38 (citing Ex. 1004, 12:52–55) , 40 (citing Ex. 1004, 12:52–55), 58 (citing Ex. 1004, 7:24–27), 41 (citing Ex. 1004, 12:47–64), 61–62 (citing Ex. 1004, 7:19–27). Even Patent Owner points to this same paragraph in characterizing the disclosures of Heinrich’s scheduler 120 (but, as with Dr. Baker’s testimony, seems to ignore the discussion of controlling exchanges “in both directions”). PO Resp. 34 (citing Ex. 1004, 7:8–27). Heinrich’s paragraph describing the scheduler discloses a number of exemplary embodiments for where the scheduler or schedulers may be implemented and both parties have pointed to that same paragraph

consistently through the briefs. Thus, we are not persuaded Petitioner's Reply improperly presents a new argument.

Accordingly, we are persuaded that Heinrich expressly discloses an "application processor configured to hold" uplink data as recited in claims 1 and 31.

We turn next to the conditions recited in claims 1 and 31 relating to how long the application processor holds uplink data.

(2) Until The Modem Processor Pulls Uplink Data (Claim 31) or Until Application Processor Triggered By Receipt of Uplink Data (Claim 1)

As noted above, claims 1 and 31 each recite a corresponding condition relating to the application processor holding uplink data. Claim 31 recites a condition that the application processor is configured to hold uplink data "until the modem processor pulls data from the application processor after transmission of the modem processor to application processor data." Petitioner argues Balasubramanian discloses this "pull" limitation in the proposed combination with Heinrich. Pet. 43–46. In particular, Petitioner argues,

Balasubramanian discloses that after transmission of data from a first processing node (*e.g.*, the transceiver 110) to a second processing node (*e.g.*, the network interface 112), the first processing node can then pull data from the second processing node. Ex-1005, 6:63-7:11 ("[T]he transceiver 110 ***then transmits the queued uplink packets over the communication link 116***. Advantageously, the queued packets may be grouped for transmission such that ***all of the packets are transmitted*** during a single wake state of the transceiver 110... As represented by block 210, during the ***same single wake state the transceiver 110 also receives any downlink packets queued in the network interface 112*** [T]he transceiver 110 may send a message to the network interface 112 ***requesting transmission of all queued packets***."); *see also id.* [at] 6:15-19 ("Conversely, in response to a ***request*** by the transceiver 110 or some other

indication, the network interface 112 may send any of its queued downlink packets to the transceiver 110 in succession over the communication link 116.”).

Pet. 45–46 (citing Ex. 1002 ¶ 97). Based on its proffered interpretation of “pull” as receiving data in response to a request for the data, an interpretation we have adopted, Petitioner argues,

Balasubramanian’s disclosure of the transceiver 110 receiving all queued packets from the network interface 112 in response to a message from the transceiver 110 requesting the queued data is a “pull” of data by the transceiver 110, because the transceiver 110 initiates and controls the transfer of the data from the network interface 112 to the transceiver 110.

Pet. 46 (citing Ex. 1002 ¶ 97). Therefore, Petitioner contends that Balasubramanian discloses a first processor holding data destined for a second processor until the second processor pulls the held data, but does not expressly disclose that the first and second processors are an application processor and a modem processor in a mobile terminal as claimed. Pet. 46. However, in the proposed combination, Petitioner argues Heinrich “teaches transmission of data between an application processor and a modem processor over a link, as well as the aggregation of such data (*i.e.*, buffering the data and sending it all at once)” and, thus, contends the combination of Heinrich and Balasubramanian discloses this limitation. *Id.* (citing Ex. 1002 ¶ 98).

Claim 1 recites a condition that the application processor is configured to hold uplink data “until *triggered* by receipt of the . . . [downlink] data from the modem processor . . . after which the . . . [uplink] data is sent to the modem processor . . . responsive to the receipt of the . . . [downlink] data from the modem processor.” In other words, the application processor holds uplink data until “triggered” by receipt of downlink data from the modem

processor after which the application processor sends the uplink data to the modem processor. Thus, claim 1 is similar to claim 31 in that, after downlink data is sent from the modem processor to the application processor, some event causes the held uplink data to be sent from the application processor to the modem processor. In claim 31 that event is a “pull” request from the modem processor to the application processor. In claim 1 that event is the completion of the receipt of the downlink data at the application processor.

Challenged independent claims 16, 26–28, and 30 include similar recitations of an action “triggered by” a recited condition or, alternatively, a recited condition that “triggers” some action. As discussed *supra*, we interpret “triggered by” and “triggers” to refer to actions that occur “*in response to*” a specified condition. *See* Section II.C.2.

Petitioner argues the combination of Heinrich and Balasubramanian teaches or suggests this limitation. 1293PET 39–49. In particular, Petitioner argues, “Heinrich also discloses that the scheduler of its baseband processor can detect that the physical IPC interface is in an active state, and the application processor is awake, when the baseband processor transmits data to the application processor.” *Id.* at 40 (citing Ex. 1004, 9:50–62).

Petitioner further argues Heinrich discloses that the “scheduling techniques described with respect to the baseband processor are also applicable to the application processor” and, thus, teaches the application processor can detect that the interface and the baseband processor are awake. *Id.* at 40–41 (citing Ex. 1004, 9:50–62, 12:47–64; Ex. 1018 ¶ 96). Petitioner contends,

While Heinrich does not explicitly disclose holding data intended for transmission to another processor until receipt of data from the other processor, Balasubramanian discloses . . . holding (e.g., queuing), at a second processing

node (e.g., network interface 112), data (e.g., downlink packets) to be sent to a first processing node (e.g., transceiver 110) until “trigger[ed]” by “receipt” of data (e.g., uplink packets) from the first processing node over a bus (e.g., communication link 116).

Id. at 41–42 (citing Ex. 1005, 6:63–7:8, Fig. 1). Petitioner contends “Balasubramanian discloses that the ‘trigger’ for the transmission of data from the second processing node (network interface 112) to the first processing node (transceiver 110) is the reception at the second processing node of all the queued packets from the first processing node.” *Id.* at 44–45 (citing Ex. 1018 ¶ 99).

Regarding the “pull” recitation of claim 31, Patent Owner argues Balasubramanian does not disclose any pull operation as Patent Owner has construed “pull” to require a specified address or location associated with the “pull.” PO Resp. 54–55. As discussed thoroughly above, we rejected Patent Owner’s narrower interpretation of “pull” as requiring that the pull specify an address or location from which the data is to be pulled. *See* Section II.C.1. Instead, we adopted Petitioner’s broader interpretation and we determine Balasubramanian discloses a “pull” operation where, for example, Balasubramanian discloses “in response to a request by the transceiver 110 or some other indication, the network interface 112 may send any of its queued downlink packets to the transceiver 110 in succession over the communication link 116.” Ex. 1005, 6:15–19; *see* Pet. 45–46 (citing Ex. 1005, 6:15–19, 63–7:8; Ex. 1002 ¶ 97).

Accordingly we are persuaded the combination of Heinrich and Balasubramanian discloses the application processor is configured to hold uplink data “until the modem processor pulls data from the application processor after transmission of the . . . [uplink] data” as recited in claim 31.

Regarding claim 1, Patent Owner argues that the combination of Heinrich and Balasubramanian fails to disclose the “triggered by” condition of claim 1 because Heinrich does not disclose holding (e.g., delaying, buffering, or accumulating) data in both processors “at the same time.” PO Resp. 41–43. Noting arguments in its Preliminary Responses, Patent Owner further argues that Balasubramanian uses receipt of uplink data to trigger transmission of downlink data—the opposite of the recited trigger condition of claim 1. *Id.* at 41 (citing its Preliminary Responses in IPR2018-01261 and IPR2018-01293). At oral argument, Patent Owner reiterated these arguments:

MR. MAIORANA: The reason that we focus on buffering of the data is that if you don’t buffer data on both sides, you can’t possibly teach using downlink data as a trigger for uplink data because you have to have queued data on both sides of the bus.

Heinrich doesn’t do that. Heinrich does queue data on one side or the other.

Now, Bala[subramanian] does do queued data on both sides, but it uses uplink data as a trigger for downlink data; the opposite of what the claim requires. So that’s why I was saying that their Slide 37 is proposing the question incorrectly. It’s not just whether either reference discloses holding data at both sides of the processor.

The references, either alone or in combination further have to disclose this claim limitation that the downlink data is the trigger for uplink data. And this Petition at 40 is where they are trying to show that Heinrich disclosed it, and then they said, well, Bala[subramanian] disclosed it. And that created this confusion where we thought they were relying on Bala[subramanian], and we said, well, that’s the opposite; that can’t be. The Board said in the ID, oh, no, they’re relying on Heinrich.

Tr. 48:20–49:16.¹⁶

As discussed *supra*, we are not persuaded by Patent Owner’s argument that Heinrich fails to disclose holding (e.g., delaying, buffering, or accumulating) data in both processors “at the same time.” *See* Section II.D.4.a.1. We incorporate that analysis here.

Regarding Patent Owner’s assertion that Balasubramanian’s “trigger” discloses transmissions in the opposite direction from that of claim 1, we agree with Patent Owner that Balasubramanian expressly discloses the opposite direction of transmission for the “triggered by” condition of claim 1—i.e., Balasubramanian discloses receipt of uplink data as a trigger to send buffered downlink data rather than receipt of downlink data as a trigger to send buffered uplink data as in claim 1. Ex. 1005, 7:6–8.

However, we are not persuaded by Patent Owner’s argument because it improperly attacks Balasubramanian individually rather than in the proposed combination. *See In re Keller*, 642 F.2d 413 (CCPA 1981); *see also In re Merck & Co.*, 800 F.2d 1091 (Fed. Cir. 1986)). Petitioner clearly relies on Heinrich in the proposed combination for disclosing the application processor holding uplink data destined for the baseband processor.

1293PET 37–39. Petitioner also relies on Heinrich for disclosing “various techniques to determine when to send data from the application processor to the baseband processor.” *Id.* at 39. Furthermore, Petitioner relies on Heinrich for disclosing that the scheduler on the baseband processor can

¹⁶ Patent Owner applies this same argument to claim 31 although claim 31 makes no reference to a “triggered by” or “triggered” condition. *See* PO Resp. 41 (applying the argument regarding “triggered by” to “(Independent Claims 1, 16, 26, 27, And 31; Dependent Claims 2-6, 8-9, 11-13, 17, And 20)”).

determine that the application processor is awake by receiving a notification that the IPC interface between the processors is active and, in response, sending held downlink data to the application processor. *Id.* at 40.

Petitioner relies on Heinrich for disclosing that “scheduling techniques described with respect to the baseband processor are also applicable to the application processor.” *Id.* The Petition relies on Heinrich as expressly disclosing controlling data (IPC activities) exchanged in *both directions* as well as disclosing a variety of conditions for causing buffered (held) data to be transmitted. *See Id.* at 39–40. Petitioner then argues,

While Heinrich does not explicitly disclose holding data intended for transmission to another processor until receipt of data from the other processor, Balasubramanian discloses such a technique. In particular, Balasubramanian discloses holding (e.g., queuing), at a second processing node (e.g., network interface 112), data (e.g., downlink packets) to be sent to a first processing node (e.g., transceiver 110) until “trigger[ed]” by “receipt” of data (e.g., uplink packets) from the first processing node over a bus (e.g., communication link 116).

Id. at 41–43 (citing Ex. 1005, 6:63–7:8, Fig. 1). Thus, Petitioner relies on Balasubramanian for disclosing a second processor that holds data destined for a first processor until triggered, by receipt of data from the first processor, to send its held data to the first processor. *Id.* at 41–45.

Therefore, we determine it is the combination that discloses bidirectional control of exchanges between an application processor and a modem processor as in Heinrich, including a variety of techniques for grouping activities to be exchanged as in Heinrich, and including one exemplary technique for such exchanges being receipt of data at a first processor from a second processor triggering the first processor to send its data to the second

processor as in Balasubramanian where such an exchange may occur in either direction as taught by Heinrich.

Patent Owner's arguments narrowly focus on the express language of Balasubramanian in isolation from the proposed combination and in disregard of what would be suggested to the ordinarily skilled artisan by the express disclosures of the references. "[I]t is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom." *In re Preda*, 401 F.2d 825, 826 (CCPA 1968). In an obviousness analysis, it is not necessary to find precise teachings in the prior art directed to the specific subject matter claimed, because inferences and creative steps that a person of ordinary skill in the art would employ can be taken into account. *See KSR*, 550 U.S. at 418.

Accordingly, we are persuaded the combination of Heinrich and Balasubramanian discloses that the application processor is configured to hold uplink data "until triggered by receipt of the . . . [downlink] data from the modem processor through the interconnectivity bus after which the . . . [uplink] data is sent [to] the modem processor through the interconnectivity bus responsive to the receipt of the . . . [downlink] data from the modem processor through the interconnectivity bus," as recited in claim 1.

(3) Pull Data Before The Bus Transitions To A Low Power State

Claim 31 further recites, "wherein the modem processor is further configured [to] pull data from the application processor after transmission of the . . . [downlink] data and before the interconnectivity bus transitions from an active power state to a low power state."

For the first portion of this limitation (pull uplink data “after transmission of” the downlink data), Petitioner refers to the preceding discussion of a “pull” operation as taught by the combination. Pet. 51. Patent Owner does not dispute this portion of the limitation apart from the above discussion of a “pull” operation. Thus, for the reasons above regarding the combination teaching or suggesting a “pull” operation, we are persuaded the combination teaches or suggests that the pull operation follows the transmission of downlink data between the processors.

Regarding the second portion of this limitation, Petitioner initially argues in a footnote that “Claim 31 does not require that the interconnectivity bus ever enter a low power state, and states merely that the modem processor transmit data to and pull data from the application processor before the interconnectivity bus enters a low power state (i.e., during the same active state).” Pet. 51 n.4.

Patent Owner does not respond to this argument.

We are persuaded by Petitioner’s argument that claim 31 (and likewise, similar recitation in claims 16 and 30) does not require that the interconnectivity bus ever transitions to a low power state. If the interconnectivity bus is *always* active, then any pull operation for uplink data that *follows any time* after some downlink data is transferred (i.e., after any transmission of downlink data to Balasubramanian’s transceiver), as taught by Balasubramanian, in combination with Heinrich’s disclosure of an interconnectivity bus (IPC), meets this limitation because the combined disclosures teach or suggest performing a pull while the interconnectivity bus is in a constant, single, always active state (a scenario within the scope of this recitation). Indeed, Petitioner argues that Balasubramanian teaches

such a pull of uplink data following a push of downlink data between its two processors. Pet. 52 (citing Ex. 1005, 2:23–24, 6:63–7:11; Ex. 1002 ¶ 107).¹⁷

Therefore, we are persuaded the combination of Heinrich and Balasubramanian meets the recitation of claim 31 that the application processor holds uplink data until the modem processor pulls the data, “wherein the modem processor is further configured [to] pull data from the application processor after transmission of the modem processor to application processor data and before the interconnectivity bus transitions from an active power state to a low power state.”

However, if this recitation of claim 31 is interpreted to require the interconnectivity bus to make one or more transitions between active and low power states—likely the scenario envisioned by the ’490 patent Specification but not necessarily required by the claimed limitations—Petitioner further argues Balasubramanian discloses “performing push and pull transactions during a single active state of the transceiver 110.” Pet. 52 (citing Ex. 1005, 6:63–7:11; Ex. 1002 ¶ 107). Petitioner next asserts “the single wake state of the transceiver 110 in Balasubramanian defines a single wake state of the communication link 116 because the transceiver 110 is the circuit that drives data onto and receives data from the communication link 116.” Pet. 53 (citing Ex. 1005, 4:39–42, 5:2–4, 5:10–29; Ex. 1002 ¶ 108). Therefore, Petitioner contends,

¹⁷ Even if Balasubramanian’s pull of uplink data precedes the push of downstream data, the opposite of the claimed ordering, the next pull operation will follow the preceding push operation during the same, single active state of the interconnectivity bus. Furthermore, it is a reasonable inference that another pull-then-push pair of operations will follow an earlier such pair of operations so long as there is continuing exchange of data during the same single active state of the interconnectivity bus.

Because Heinrich similarly discloses a bus with low and high power states and performing a data transfer between two processors during a single wake state of a bus, a person of ordinary skill in the art would have been motivated to apply Balasubramanian's teaching of performing push and pull transactions during a single wake state of communication link 116, to the system of Heinrich, to create a system in which a modem processor pushes data to, and pulls data from, an application processor during a single active state of the communication link between the modem processor and application processor.

Id. (citing Ex. 1002 ¶ 109).

In response to these further arguments of Petitioner, Patent Owner argues: (1) Balasubramanian does not control a powered interconnectivity bus (PO Resp. 44–47); (2) states of Balasubramanian's transceiver are not coterminous with any bus (PO Resp. 47–51); and (3) Balasubramanian does not disclose sending and receiving (pushing and pulling) in a single active state of any bus (PO Resp. 51–54). We address these arguments below.

(a) Combination Teaches or Suggests an Interconnectivity Bus

Patent Owner argues Balasubramanian does not control a powered interconnectivity bus as recited in claims 1 and 31. PO Resp. 44–47. In particular, Patent Owner argues “Balasubramanian does not mention any bus, much less an interconnectivity bus.” PO Resp. 45. Patent Owner further argues that the wired (rather than wireless) connection in Balasubramanian “is noted to be in a packet-switched context where data paths are shared among many users of the network” and, thus, “it does not make sense to power down a link in a packet switched network facilitating communications among more than two entities [(as in the '490 patent)] because Balasubramanian-type network links can be utilized by any of the many entities on that network.” *Id.* at 46–47 (citing Ex. 1005, 4:43–57, Fig.

1). Thus, Patent Owner contends, Balasubramanian “does not disclose an interconnectivity bus at all, much less identify the bus as a place to save power,” and “it is not even possible to shut down the shared wireless medium because it is not a powered medium.” *Id.* at 47 (citing Ex. 2007 ¶¶ 96–97).

Petitioner argues Balasubramanian discloses that communication link 116 may be a wired connection using any wired protocol and asserts that nothing in Balasubramanian discloses that link 116 *must* be a shared medium, as suggested by Patent Owner. Reply 26–27 (citing Ex. 1005, 4:48–53, 7:26–28). Petitioner further argues that Balasubramanian’s Figure 1 “shows communication link 116 connecting just ‘one’ user device 102, through transceiver 110, to network interface 112,” and, thus, Balasubramanian does not disclose that communication link 116 is shared by more than the two devices shown (e.g., transceiver 110 of device 102 and network interface 112). Reply 27.

Patent Owner responds that “Balasubramanian does not disclose using a point-to-point, powered-interconnectivity-bus protocol that keeps link 116 powered at all times transceiver 110 is active.” Sur-Reply 22. Patent Owner further argues “[w]hile Balasubramanian does not expressly exclude other protocols including wire-based protocols, that is not disclosure of a powered interconnectivity bus having active and inactive power states that would be relevant to the ’490 Patent claims.” *Id.* at 24 (citing Ex. 2007 ¶ 95).

We are persuaded that the combination of Heinrich and Balasubramanian teaches or suggests a modem processor that transmits downlink data to the application processor and pulls uplink data from the application processor “before the interconnectivity bus transitions from an active power state to a low power state.” As discussed *supra*, Heinrich, in

the proposed combination, is relied upon for disclosing the claimed interconnectivity bus. Pet. 38–39. As noted above, the claims do not require that the interconnectivity bus ever make a transition to a low power state. However, if such a requirement is inferred in the claims, in addition to the exemplary PCIe bus embodiment, the '490 patent discloses USB as another interconnectivity bus that may be used for the claimed mobile terminal.¹⁸ Ex. 1001, 6:66–7:3. Heinrich specifically discloses that its IPC can be any of several known inter-processor busses, including, for example USB. Ex. 1004, 4:44–50 (*quoted in* Pet. 39). Therefore, to whatever extent Patent Owner argues an “interconnectivity bus” must be capable of switching between active and low power states, the '490 patent claims and Heinrich both encompass USB as such an exemplary interconnectivity bus. In combination with Heinrich, Balasubramanian’s disclosure of transmitting and pulling data before its transceiver 110, which controls its communication link 116, transitions to a low power state teaches or suggests the type of “interconnectivity bus” recited in claim 31.

(b) Transceiver Driving the Bus Defines State of the Bus

As discussed *supra*, Petitioner asserts that a “single wake state of the transceiver 110 in Balasubramanian defines a single wake state of the communication link 116 because the transceiver 110 is the circuit that drives data onto and receives data from the communication link 116” and because Heinrich discloses an interconnectivity bus with high and low power states,

¹⁸ We note that claims 2 and 3, dependent from claim 1, specifically narrow the “interconnectivity bus” of claim 1 to “PCI compliant” and PCIe busses, respectively. Therefore, the term “interconnectivity bus” as used in the broader independent claims must be broader than these dependent claims and encompasses, at least, other exemplary interconnectivity busses disclosed in the '490 patent.

the combination teaches or suggests that a push and a pull operation occur in a single wake state of the interconnectivity bus. Pet. 53 (citing Ex. 1005, 5:39–42, 5:10–29; Ex. 1002 ¶¶ 108, 109).

Patent Owner argues the wake state of a processor on the interconnectivity bus does not define the wake state of the bus because “[t]he interconnectivity bus may transition between sleep and wake states thousands of times per second while the ’490 Patent’s modem processor and application processor are active during a voice telephone, video streaming, or audio streaming activity.” PO Resp. 47–48 (citing Ex. 2007 ¶ 98). Patent Owner argues Balasubramanian’s Figure 2 “illustrates that certain steps are performed by the transceiver 110 before it acquires access to any network communication channel” and contends Petitioner’s expert, Dr. Lin, agrees that Balasubramanian’s transceiver is awake before the link is accessed. *Id.* at 48–49 (citing Ex. 2010, 59:10–18). Patent Owner further argues Heinrich “explicitly states that wake states of its baseband processor 104 also do not correspond to active states of the IPC.” *Id.* at 50–51 (citing Ex. 1004, 6:36–39, Fig. 2); *see also id.* at 51–54.

Petitioner replies that Dr. Lin also testified that, in Balasubramanian, when a wired communication link is used between transceiver 110 and network interface 112, transceiver 110 has immediate access to link 116 because it is the circuit that controls signaling on that communication link. Reply 29–30 (citing Ex. 2010, 60:8–21, 59:22–60:7). Petitioner contends,

The reason “other components” of user device 102 can be active when transceiver 110 is asleep is because the state of the other components is independent of the state of transceiver 110. But transceiver 110, in a wired link, controls the state of the bus, and it is desirable to power down such “high-powered . . . transceiver components” as much as possible.

Reply 31–32 (citing PO Resp. 59; Ex. 1023 ¶ 36).

Patent Owner responds, “while Balasubramanian does mention in passing that link 116 may communicate via a wire-based protocol other than Ethernet, Balasubramanian does not disclose using a point-to-point, powered-interconnectivity-bus protocol that keeps link 116 powered at all times transceiver 110 is active.” Sur-Reply 22.

We are persuaded by Petitioner’s arguments that the combination of Heinrich and Balasubramanian teaches or suggests that the reception of data and subsequent pull of data occur during the same power state of the interconnectivity bus connecting the processors, i.e., “before the interconnectivity bus transitions from an active power state to a low power state.” First, as noted *supra*, Heinrich expressly discloses use of a USB interconnectivity bus noted as an equivalent, exemplary, interconnectivity bus structure in the ’490 patent. *See, e.g.*, Ex. 1004, 11:38–40, 13:41–42. Thus, to whatever extent the claims require a bus that provides transitions between active and low power states, Heinrich expressly discloses such a USB bus. Moreover, Balasubramanian’s transceiver 110 is the component that drives and receives signals on link 116 and, thus, when it is in a low power state, so too is communication link 116. Patent Owner’s counsel acknowledged that the state of an interface circuit on a bus determines the state of the bus because a “bus” is merely a collection of passive conductors (e.g., wires) the state of which is defined by the interface circuit(s) coupled to those wires and the protocols implemented by those interface circuits. *See* Tr. 40:17–42:25. Balasubramanian’s transceiver 110 is precisely such an interface circuit that drives signals on a bus (link 116) and, thereby, defines the state of the attached bus (link 116). Petitioner argues, and we agree,

But Balasubramanian teaches putting transceiver 110 to sleep while keeping some of the user device's processing circuitry awake—thus reinforcing that the sleep state of transceiver 110 defines the “low power” mode of a bus, even when other circuitry in user device 102 is awake. Ex. 1005 at 5:20-22 (“components that generate data and packets and perform the queuing and other related operations remain active (e.g., in a wake state)”); *id.*, 5:27-29 (“components associated with upper layers remain active to potentially provide packets for the lower layers once [] lower layers [such as transceiver 110] return to the active state”).

Reply 30–31 (alterations in original).

Accordingly, we are persuaded the combination of Heinrich and Balasubramanian teaches or suggests that the receipt of data followed by a “pull” operation is performed within a single awake state of the interconnectivity bus (i.e., before the interconnectivity bus transitions to a low power state—if it ever so transitions to a low power state).

b) Conclusion Regarding Claims 1 and 31

In view of the above discussion, we are persuaded by a preponderance of the evidence that the combination of Heinrich and Balasubramanian teaches or suggest all elements of independent claims 1 and 31 and that Petitioner has set forth sufficient articulated reasoning showing that a person of ordinary skill in the art would have combined the teachings of the references in the manner asserted. Thus we are persuaded Petitioner has established by a preponderance of the evidence that claims 1 and 31 are unpatentable as obvious over the combination of Heinrich and Balasubramanian.

5. Analysis of Dependent Claims 4 and 5

Claims 4 and 5 depend from claim 1. Claim 4 recites that the “application processor includes an uplink timer and the uplink timer has a period longer than a period of the modem timer.” Claim 5 depends from

claim 4 and further recites “wherein the application processor is configured to hold the application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor or expiration of the uplink timer having a period longer than a period of the modem timer, whichever occurs first.” In addition to the argument relating to base claim 1 as discussed above, Petitioner identifies each element of claims 4 and 5 in the combination of Heinrich and Balasubramanian in the petition in IPR2018-01293. 1293PET 57–62.

Specifically, regarding claim 4, Petitioner argues that Heinrich discloses an “uplink timer” because it discloses a “lazy timer” used by the scheduler (as discussed *supra*) and discloses that the same scheduling techniques may be applied on both processors of its mobile device. 1293PET 58. Petitioner further argues it would have been obvious to the ordinarily skilled artisan that such an uplink timer “can have a period longer than the modem timer” because “[t]here are only three possible ways to implement the relative lengths of the two timers,” two timers having equal periods, a first timer having a longer period than a second timer, or the second timer having a longer period than the first time. *Id.* at 58–59 (citing Ex. 1018 ¶ 117). Furthermore, Petitioner contends it would have been obvious to the ordinarily skilled artisan to design the uplink timer with a longer period than the modem timer because “[s]etting the uplink timer to be equal to or shorter than the modem timer would increase the chances that the uplink timer would expire first—thereby triggering a transmission of application processor data—before the application processor has had a chance to receive data from the modem processor.” *Id.* at 59 (citing Ex. 1018 ¶ 118). Petitioner contends such a design would reduce the opportunities to “piggyback” the transmission in both directions and, thus,

reduce the achievable power reductions, whereas setting the uplink timer *longer* than the modem time would increase the opportunities for such “piggybacking” of transmissions in both directions. *Id.* (citing Ex. 1018 ¶ 118). Petitioner further contends it was well-known that the volume of downlink data exceeds uplink data in typical mobile terminals and, thus, it would have been obvious to the ordinarily skilled artisan that “modem timer should be shorter than the application/uplink timer because the modem processor sends data more often and its buffer is likely to fill up more quickly.” *Id.* at 60 (citing Ex. 1018 ¶ 119; IPR2018-01293 Ex. 1015).

Patent Owner argues “[t]he Petition cites to no actual disclosure of either of these claim limitations” and “Petitioner’s expert agrees that none of the sentences cited at pages 57–61 of the -01293 Petition explicitly states that an uplink timer has a period longer than a period of the modem timer.” PO Resp. 56 (citing Ex. 2010, 78:25–79:9). Patent Owner further argues nothing in Heinrich teaches using both a modem timer and an uplink timer and argues “nothing in Heinrich discusses coordinating between lazy timers that are on different schedulers on different processors.” *Id.* at 58–59 (citing Ex. 2007 ¶¶ 111–112); Sur-Reply 35.

Petitioner replies that none of Patent Owner’s arguments rebut Petitioner’s arguments regarding obviousness. Reply 35. Petitioner notes that it is not contending this feature is anticipated but, instead, presented arguments that the feature would have been obvious. *Id.*

We are persuaded by Petitioner’s arguments. Heinrich discloses use of a lazy timer in its scheduler and clearly discloses each processor may be controlled by the scheduler (or by a corresponding scheduler) and that “the same scheduling techniques” may be used to control exchanges in both directions. 1293PET 58 (citing Ex. 1004, 7:24–27, 12:52–55). Thus, we

find it would have been obvious to the ordinarily skilled artisan to use a lazy timer in scheduling for each delayed (held) IPC activity on each of Heinrich's two processors—lazy timer(s) for scheduling on the application processor to send uplink data and lazy timer(s) for scheduling on the baseband processor to send downlink data.

Furthermore, we agree with Petitioner that, with the knowledge that downlink data is far more common than uplink data in typical mobile terminals, the ordinarily skilled artisan would have made the uplink timer longer so as to increase the number of opportunities to “piggyback” uplink data with the more frequent downlink data, thus, increasing power savings by transitioning the processors and/or interconnectivity bus to a low power state.

Still further, we also agree with Petitioner that there is a small finite number (three) of known solutions to the problem of the relative periods of the two timers—equal timer periods, the first period larger than the second, or the second period larger than the first. 1293PET 59. Thus, as Petitioner correctly observes, it would have been obvious to the ordinarily skilled artisan to try the design of setting the uplink time period (lazy timer for an IPC activity in the application processor scheduling) longer than the modem timer period (lazy timer for IPC activity in the baseband processor scheduling). 1293PET 60–61 (citing *KSR*, 550 U.S. at 421 (“When there is a design need . . . to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense.”); Ex. 1018 ¶ 120).

Patent Owner does not separately argue claim 5 (which depends from claim 4).

Having considered the full record developed during trial, we are persuaded Petitioner has established by a preponderance of the evidence that claims 4 and 5 are unpatentable as obvious over the combination of Heinrich and Balasubramanian.

6. Analysis of Dependent Claims 6, 8, 9, and 11–13

Claims 6 and 8 depend from claim 1. In addition to the arguments and supporting evidence relating to their base claim as discussed above, Petitioner identifies each element of claims 6 and 8 in the combination of Heinrich and Balasubramanian in the petition in IPR2018-01293. 1293PET 62–63. In our Decision on Institution in IPR2018-01293, we determined that Petitioner had established a reasonable likelihood of prevailing in showing these claims are unpatentable. IPR2018-01293, Paper 8, 38. Patent Owner does not argue these claims in its Patent Owner’s Response apart from the above issues relating to their base claim. Arguments not raised in the Patent Owner’s Response are waived. IPR2018-01293, Paper 9, 5.

Claims 9 and 11–13 depend from claim 1. In addition to the arguments and supporting evidence relating to their base claim as discussed above, Petitioner identifies each element of claims 9 and 11–13 in the combination of Heinrich and Balasubramanian in the petition in IPR2018-01346. 1346PET 55–64. In our Decision on Institution in IPR2018-01346, we determined that Petitioner had established a reasonable likelihood of prevailing in showing these claims are unpatentable. IPR2018-01346, Paper 8, 34–39. Patent Owner does not argue these claims in its Patent Owner’s Response apart from the above issues relating to their base claim.

Arguments not raised in the Patent Owner's Response are waived.

IPR2018-01346, Paper 9, 5.

We have reviewed Petitioner's arguments and supporting evidence regarding the limitations of claims 6, 8, 9, and 11–13 and find them persuasive. We are persuaded Petitioner has established by a preponderance of the evidence that claims 6, 8, 9, and 11–13 are unpatentable as obvious over the combination of Heinrich and Balasubramanian.

7. Analysis of Independent Claims 26 and 27

Independent apparatus claims 26 and 27 recite similar elements to those of claim 1 but rather than relying on timer expirations, they recite threshold values for counters of various elements of transmission (bytes or packets, respectively) to control various transmission between the processors. Petitioner identifies each element of claims 26 and 27 in the combination of Heinrich and Balasubramanian in the petition in IPR2018-01346. 1346PET 64–69. In our Decision on Institution in IPR2018-01346, we determined that Petitioner had established a reasonable likelihood of prevailing in showing these claims are unpatentable. IPR2018-01346, Paper 8, 39. Patent Owner does not argue these claims in its Patent Owner's Response apart from the above issues relating to similar claim 1. Arguments not raised in the Patent Owner's Response are waived. IPR2018-01346, Paper 9, 5.

We have reviewed Petitioner's arguments and supporting evidence regarding the limitations of claims 26 and 27 and find them persuasive. We are persuaded Petitioner has established by a preponderance of the evidence that claims 26 and 27 are unpatentable as obvious over the combination of Heinrich and Balasubramanian.

8. Analysis of Independent Claims 16 and 22 and Dependent Claims 23 and 24

Independent method claim 16 recites method steps essentially the same as the functions recited in the structure of apparatus claim 1. Independent apparatus claim 22 recites elements and functions similar to claim 1. Claims 23 and 24 depend from claim 22. Petitioner identifies each element of independent claim 16, independent claim 22, and dependent claims 23 and 24 in the combination of Heinrich and Balasubramanian in the petition in IPR2018-01295. 1295PET 29–68. In our Decision on Institution in IPR2018-01295, we determined that Petitioner had established a reasonable likelihood of prevailing in showing these claims are unpatentable. IPR2018-01295, Paper 8, 36–44. Patent Owner does not argue these claims in its Patent Owner’s Response apart from the above issues relating to similar claim 1. Arguments not raised in the Patent Owner’s Response are waived. IPR2018-01295, Paper 9, 5.

We have reviewed Petitioner’s arguments and supporting evidence regarding the limitations of claims 16 and 22–24 and find them persuasive. We are persuaded Petitioner has established by a preponderance of the evidence that claims 16 and 22–24 are unpatentable as obvious over the combination of Heinrich and Balasubramanian.

9. Analysis of Dependent Claim 20 and Independent Claims 28 and 30

Claim 20 depends from claim 16. Independent apparatus claim 28 recites elements similar to those of claim 1 but uses a byte counter threshold value in determining when certain transmissions occur. Independent method claim 30 recites method steps similar to the functions of apparatus of claim 1. Petitioner identifies each element of claims 20, 28, and 30 in the combination of Heinrich and Balasubramanian in the petition in

IPR2018-01344. 1344PET 56–72. In our Decision on Institution in IPR2018-01344, we determined that Petitioner had established a reasonable likelihood of prevailing in showing these claims are unpatentable. IPR2018-01344, Paper 8, 35–43. Patent Owner does not argue these claims in its Patent Owner’s Response apart from the above issues relating to similar claim 1. Arguments not raised in the Patent Owner’s Response are waived. IPR2018-01344, Paper 9, 5.

We have reviewed Petitioner’s arguments and supporting evidence regarding the limitations of claims 20, 28, and 30 and find them persuasive. We are persuaded Petitioner has established by a preponderance of the evidence that claims 20, 28, and 30 are unpatentable as obvious over the combination of Heinrich and Balasubramanian.

E. Obviousness Over Heinrich, Balasubramanian, and Tsai

In this consolidated proceeding, Petitioner relies on the combined disclosures of Heinrich, Balasubramanian, and Tsai in contending certain claims are unpatentable as obvious under 35 U.S.C. § 103 (post-AIA) as follows: claims 2 and 3 (1293PET 64–69) and claim 17 (1295PET 68–72).

1. Overview of Tsai (Ex. 1017)

Tsai is directed to buffering techniques for power management of a system. Ex. 1017, code (54), code (57). Figure 2 is reproduced below.

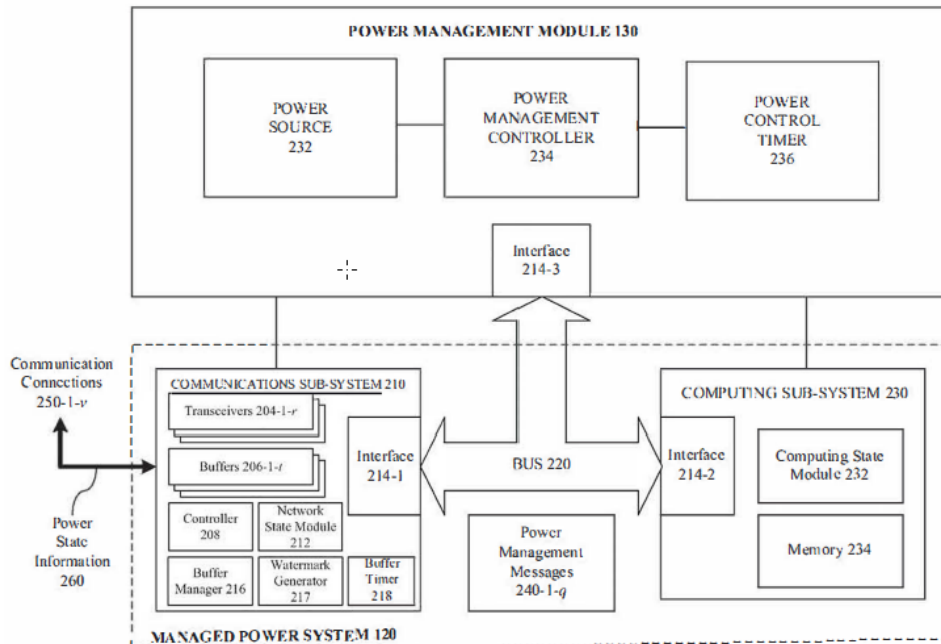


FIG. 2

Tsai’s Figure 2 discloses a device in which communications subsystem 210 communicates with computing sub-system 230 over bus 220. *Id.* at 8:16–21. According to Tsai, communications sub-system 210 includes a baseband processor (*id.* at 5:59–6:5) and computing sub-system 230 includes its own processor (*id.* at 7:33–44). Tsai further discloses that communication bus 220 can be implemented using a variety of protocols, “includ[ing] without limitation Peripheral Component Interconnect (PCI) [and] PCI Express (PCIe).” *Id.* at 8:25–30.

2. Analysis of Claims 2 and 3

Claims 2 and 3 depend, directly or indirectly, from claim 1 and further recite that the interconnectivity bus comprises a PCI and PCIe bus, respectively. Petitioner adds Tsai to the combination of Heinrich and Balasubramanian for its disclosure of a PCIe bus in a computing system, identifies the additional limitations of claims 2 and 3 in the combined teachings of Heinrich, Balasubramanian, and Tsai, and articulates a reason

the ordinarily skilled artisan would have been motivated to combine Tsai with Heinrich and Balasubramanian. 1293PET 64–69.

Patent Owner does not address these claims apart from the above discussion of claim 1. *See* PO Resp.

We have reviewed Petitioner’s arguments and supporting evidence regarding the limitations of claims 2 and 3 and find them persuasive. We are persuaded that Petitioner has established by a preponderance of the evidence that claims 2 and 3 are unpatentable as obvious over the combination of Heinrich, Balasubramanian, and Tsai.

3. Analysis of Claim 17

Claim 17 depends from claim 16 and further recites that the data is passed over a PCI compliant bus. Petitioner adds Tsai to the combination of Heinrich and Balasubramanian for its disclosure of a PCI bus in a computing system connecting an application processor and a baseband (modem) processor, identifies the additional limitations of claim 17 in the combined teachings of Heinrich, Balasubramanian, and Tsai, and articulates a reason the ordinarily skilled artisan would have been motivated to combine Tsai with Heinrich and Balasubramanian. 1295PET 68–72. Patent Owner does not address this claim apart from the above discussion of claim 16.

We have reviewed Petitioner’s arguments and supporting evidence regarding the limitations of claim 17 and find them persuasive. We are persuaded Petitioner has established by a preponderance of the evidence that claim 17 is unpatentable as obvious over the combination of Heinrich, Balasubramanian, and Tsai.

III. CONCLUSION¹⁹

For the foregoing reasons, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–6, 8, 9, 11–13, 16, 17, 20, 22–24, 26–28, 30, and 31 of the '490 patent are unpatentable.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–6, 8, 9, 11–13, 16, 17, 20, 22–24, 26–28, 30, and 31 of U.S. Patent No. 9,535,490 B2 are unpatentable; and

FURTHER ORDERED that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

¹⁹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

In summary:

Claims	35 U.S.C. §	References	Claims Shown Unpatentable	Claims Not shown Unpatentable
1, 4–6, 8, 9, 11–13, 16, 20, 22–24, 26–28, 30, 31	103	Heinrich, Balasubramanian	1, 4–6, 8, 9, 11–13, 16, 20, 22–24, 26–28, 30, 31	
2, 3, 17	103	Heinrich, Balasubramanian, Tsai	2, 3, 17	
Overall Outcome			1–6, 8, 9, 11–13, 16, 17, 20, 22–24, 26–28, 30, 31	

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